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JSS Focus Issue on GaN-Based Electronics for Power, RF, and Rad-Hard Applications

Buffer Trap Related Knee Walkout and the Effects of Self-Heating in AlGaN/GaN HEMTs

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Mixed-mode simulations of a class A amplifier is used to study the DC/RF dispersion commonly observed in AlGaN/GaN based HEMTs. We show that the observed knee walkout at frequencies greater than the emission rates of buffer traps (time constants $t^a{}_e > 1$ week) is related to the steady state trap density and spatial location due to the DC operational bias. An increase in the drain bias point and an initial distortion of the RF signal, that is expected to disappear as the device global temperature reduces, is observed when a self-heating model is included. Finally, we propose that a reduction in the DC/RF dispersion is possible with a suitable location and concentration of an acceptor doping in the buffer.

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Direct current (DC) to radio frequency (RF) dispersion highlighted in experimental studies[1,2] of Gallium Nitride (GaN) based High Electron Mobility Transistors (HEMTs) in the amplifier operation has been attributed to trapping in the device structure. The effect of this dispersion is a reduction in the available RF output power, and effectively results in the reduced performance of GaN HEMTs in RF and power applications in spite of its very promising material properties. The reduction in RF output power can be observed in a so-called knee walkout. The knee walkout describes a situation where the minimum drain voltage under RF drive is smaller than that obtained from DC as opposed to the current collapse (CC) which refers to the reduction in the RF maximum drain current compared to that observed under DC.[3]

Although experiments have revealed a dependence of the knee walkout on the DC operating point, it remains not understood to what extent degradation processes due to either the surface or the buffer traps affect the device's RF performance. Pulsed measurements of the device have been employed to study the collapse of the current and the dispersion at the knee of the output characteristics,[2] mirroring thus the expected behavior of the device in amplifier operation. This approach is useful in gaining important insights to possible trapping behavior but loses its accuracy in simulations due to the inaccurate determination of the pulsed knee voltage. The simultaneous application of voltages on the drain and the gate contacts in pulsed simulations is in reality achieved with one bias ensuing the other. Here, we have employed a mixed mode simulation of a GaN HEMT in class A operation, which ensures that the instantaneous applied biases depend only on the amplifier operation. The behavior of the device is thus accurately modeled using a physically based device simulator while the remaining part of the circuit is modeled using conventional circuit simulation techniques[4] in a real spirit of TCAD. In addition to the much more realistic simulation approach resulting in increased accuracy, the internal device conditions can be examined at any given point.

The investigations are carried out using the drift-diffusion transport model. The study is based on a careful calibration of device I-V characteristics to experimental data prior to simulations in mixed-mode. We limit our present study to the effects of trapping in the buffer on the knee walkout and the CC since the buffer traps are considered to be a major trapping mechanism. In the next section, we describe the device structure and simulation methodology. The results on the dependence of knee walkout on operational bias and evidence for the relation between buffer traps and the knee walkout are presented in DC/RF dispersion due to buffer traps section. Finally, we show the effects of self-heating on the device RF performance based on the assumption of an ideal thermal contact in Self-heating effects in GaN HEMTs section. The last section is dedicated to conclusions.

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Device Structure and Simulation Methodology

The device presented in this work is the same as in Ref. 5. Fig. 1 illustrates the schematic cross-section of an investigated asymmetrical $1\,\mu m$ gate length GaN HEMT. It consists of a $2\,nm$ GaN cap, $20\,nm$ AlGaN barrier, $1\,nm$ AlN spacer, and $3\,\mu m$ GaN buffer, all grown on a SiC substrate with source-to-gate and gate-to-drain separations of $L_{SG} = 2\,\mu m$ and $L_{GD} = 3\,\mu m$, respectively.

The modeled device has been calibrated against experimentally measured transfer characteristics ($I_D - V_{GS}$) using commercial simulation software Atlas by Silvaco as illustrated in Fig. 2. In the calibration, we have used donor interface traps located at the interface between the GaN cap and silicon nitride (SiN) layer with an energy, concentration and electron and hole capture cross-sections of $E_T = E_V + 2.9\,eV$,[6]

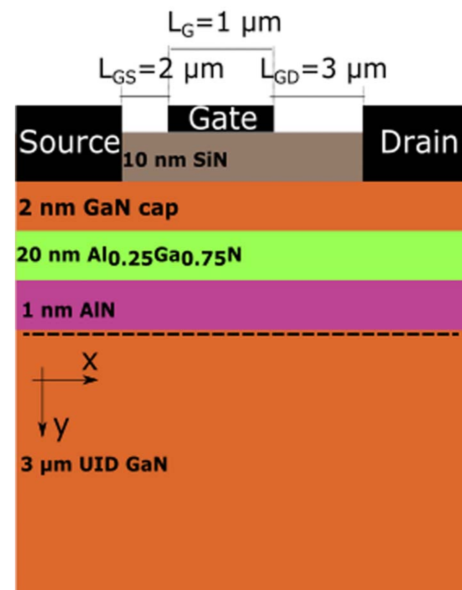

Figure 1. Device heterostructure of the investigated $1\,\mu m$ gate length GaN HEMT.

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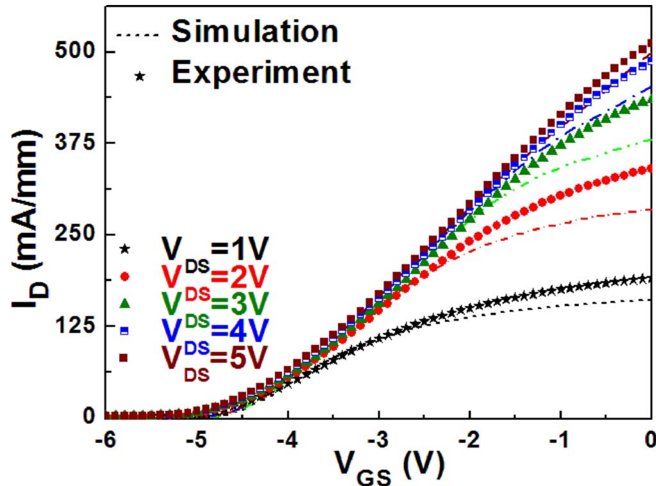

Figure 2. Transfer characteristics ($I_D - V_{GS}$) at $V_{DS} = 1\ V$ to $V_{DS} = 5\ V$ in a step of $1\ V$ comparing calibrated simulations (dotted lines) to experimental measurements (symbols).

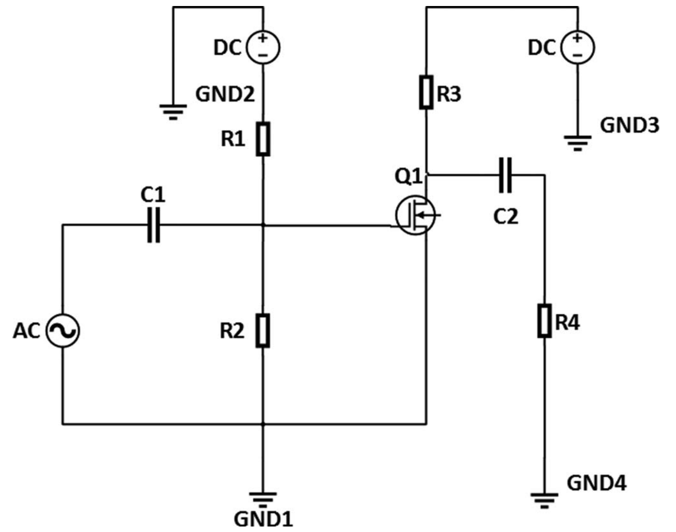

Figure 3. Schematic of the simulated class A RF amplifier circuit where the drain voltage is the voltage before the blocking capacitor, C2, while the output voltage is the voltage across the load resistor, R4.

$N_D = 0.7 \times 10^{13}\ cm^{-2}$ and $\sigma_{n,p} = 1 \times 10^{-13}\ cm^2$,[7] respectively, in order to pin the Fermi level at the surface. The calibration process also revealed acceptor traps located in the GaN buffer with an energy, concentration and electron and hole capture cross-sections of $E_T = E_C - 2.2\,eV$,[8] $N_A = 2.95 \times 10^{16}\ cm^{-3}$ and $\sigma_{n,p} = 1 \times 10^{-15}\ cm^2$,[9] respectively, which help to control a leakage current through the buffer and thus to better confine electrons into the channel. The free carrier distribution is modeled using the Boltzmann statistics and Shockley-Read-Hall recombination model is used for carrier generation and recombination. The device is uniformly n-type doped with a concentration of $2.7 \times 10^{16}\ cm^{-3}$ which well reproduces an intrinsic doping occurring in III-Nitrides. We have modeled the effects of spontaneous and piezoelectric polarizations by including an interface charge, Q_{IT} at the inter-layers between the GaN cap, aluminum gallium nitride (AlGaN) barrier, aluminum nitride (AlN) spacer and the GaN buffer of $-0.749 \times 10^{13}\ cm^{-2}$, $-3.101 \times 10^{13}\ cm^{-2}$ and $3.85 \times 10^{13}\ cm^{-2}$ respectively.

In order to model carrier velocity variation with field strength, we have used a combination of the parallel field dependent mobility model,[10] a nitride specific field dependent model that is based on a fit to Monte Carlo data,[11] and the Albrecht mobility model[12] which gives a dependence on doping concentration and temperature. The parallel field dependent mobility model can be expressed as[10]

$$\mu_{n,p}(E) = \mu_{n,p0}\left[1 + \left(\frac{\mu_{n,p0}E}{V_{SAT}^{n,p}}\right)^{\beta}\right]^{\frac{1}{\beta}} \quad [1]$$

where V_{SAT}^{n} and V_{SAT}^{p} are the saturation velocities for electrons and holes, μ_{n0} and μ_{p0} are the electron and hole low field mobility and β is a power coefficient to describe a strength of current saturation. The modeled transfer characteristics using parameters of Table I are compared in Fig. 2 against experimental data with a good agreement. The modeled device is thereafter used in a mixed-mode simulator along with other discrete circuit components, whose behavior is assumed to be ideal, to simulate a GaN HEMT amplifier in class A operation (see Fig. 3). The gate bias is $-2.3\ V$ and the maximum applied gate voltage is $+0.4\ V$ while the operating frequency is $1\ MHz$.

Table I. Material parameters used in the simulations.

Material Properties	GaN	AlN
Electron Saturation Velocity	$1 \times 10^7\ cms^{-1}$	$1 \times 10^7\ cms^{-1}$
Electron Mobility	$1120\,cm^2V^{-1}s^{-1}$	$135\,cm^2V^{-1}s^{-1}$
Hole Mobility	$30\,cm^2V^{-1}s^{-1}$	$14\,cm^2V^{-1}s^{-1}$
β	2	2

DC/RF Dispersion due to Buffer Traps

The dispersion at the knee of the DC-IV characteristics with increasing drain bias has been widely reported.[1,2] Here, we vary the voltage excursion at the drain whilst maintaining a fixed drain bias, V_{DS}, of $10\ V$ in all cases. As shown in Fig. 4, the RF drain current is able to reach the knee of the DC output characteristics. It therefore suggests that, at this bias, there is no observable DC/RF dispersion. The RF drain current thus appears to be independent of the maximum applied drain voltage. Interestingly, the inclusion of the effects of electric field generated traps[5,9] in the drain access region does not show any significant effect on the DC/RF dispersion (see Fig. 5). These results for low DC operating points are consistent with the experimental results of Ref. 1. However, when the drain bias is increased to $16\ V$, an extreme walk-out of the knee can be seen in Fig. 6, with the minimum drain voltage appearing to continuously reach

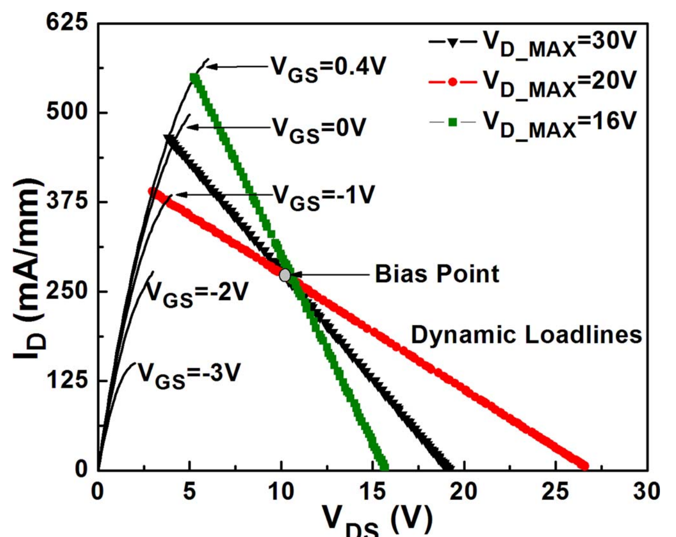

Figure 4. $I_D - V_{DS}$ characteristics showing increased RF excursions on the drain. There is no dispersion due to the increase in V_{DMAX}.

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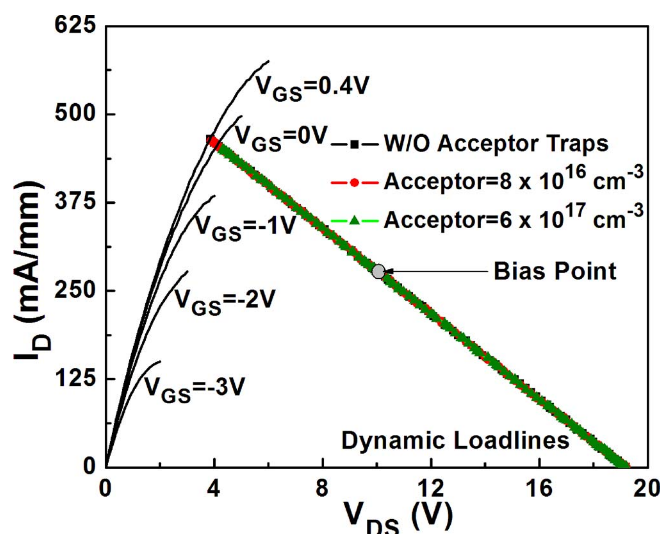

Figure 5. I_D–V_{DS} characteristics showing increasing trap density in the drain access region which does not show any significant knee walkout.

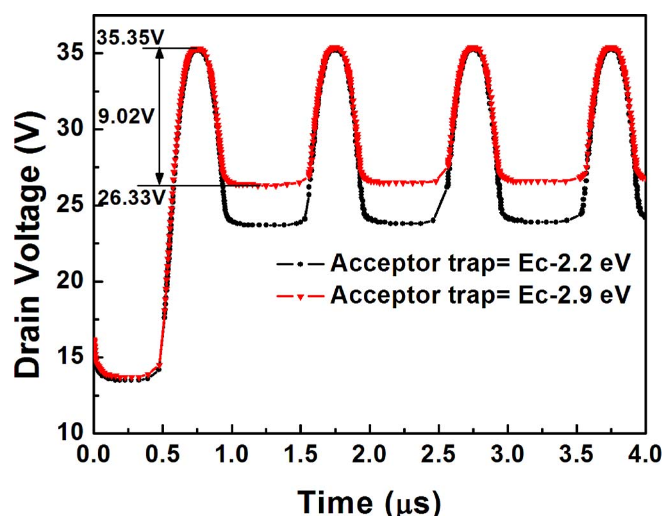

Figure 7. Dynamic drain voltages (V_{DS}) for two indicated acceptor trap energies in the buffer indicating that dispersion at the knee is affected by traps in the buffer.

23.67 V instead of the minimum estimated knee voltage of 4.0 V. The failure to reach the estimated knee voltage during the first half cycle is entirely due to trapping caused by the DC bias. In the next cycle, when the maximum drain voltage is attained, additional trapping occurs leading to an increased dispersion at the knee. This isolation of the separate contributions of the DC operating point and the RF drain voltage swing is difficult to achieve in measurements because of the limitations of measuring equipment in measuring and observing waveforms at such timescales. Although the magnitude of this walk-out is much more pronounced than the knee walkout seen in published experimental data,[3] it is very useful to study the quantitative cause of this behavior. Therefore, we have varied the trap energy level in the buffer. The result in Fig. 7 shows an increase in the minimum steady state RF drain voltage when the acceptor traps are assumed to be at an energy of $E_C - 2.9\,eV$. This result links the quality of the buffer properties determined by energy localization of the major traps to the observed degradation of the RF output power. It also suggests that some fraction of the trapped carriers are either too slow to respond to the fast changing bias or are trapped further away from the channel so that these carriers become inactive in the transport process.

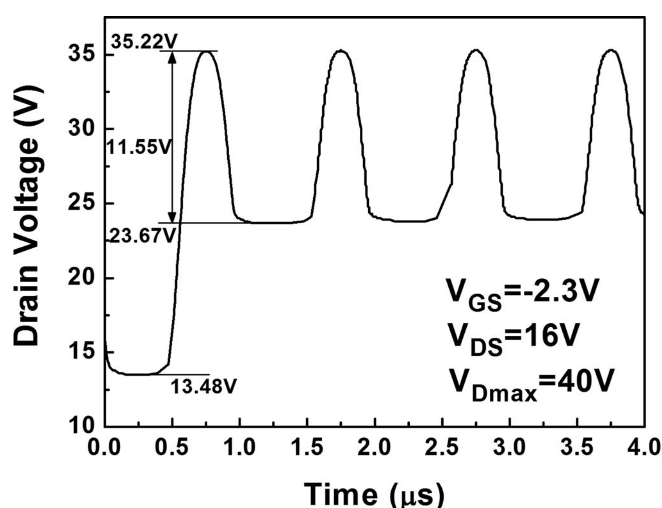

Figure 6. Dynamic drain voltage (V_{DS}) showing dispersion is observed at a fixed bias point, $V_{DS} = 16\,V$. The minimum drain voltage is increased to 23.67 V and a reduced voltage excursion on the drain.

Fig. 8 shows time dependence of the drain voltage when we vary the electron and hole capture cross-sections. The electron capture and emission probabilities were changed from $10^{-15}\,cm^2$ to $10^{-20}\,cm^2$ only in the buffer, and in the region from approximately 0.5 μm below the channel.

The increase by 37.3% in the drain voltage swing suggests that traps located spatially deep in the buffer play a significant role in the observed DC/RF dispersion. In addition to the longer de-trapping time constants caused by their spatial location, it is possible that these deep traps, when occupied, prevent the potential in a buffer from following the changing biasing potentials at the contacts and, hence, lead to an uncontrolled back biasing of the channel.[13] The investigations have shown that the acceptor doping of the buffer at suitable locations or depths can modify the energy bands and reduces the occurrence of deep acceptor trapping. This acceptor doping of the buffer could achieve a reduction in the DC/RF dispersion as illustrated in Fig. 8. Here, we have a p-type doped buffer in the drain access region from about 1.5 μm to 2 μm below the channel. Note also that the previous

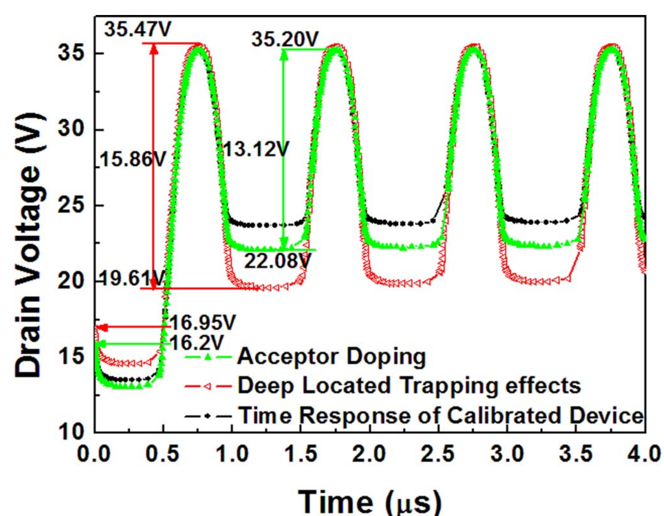

Figure 8. Simulated effects of spatially deep located traps in the buffer (Deep Located Trapping Effects) and improved time-dependent response due to a suitable acceptor doping in the buffer (Acceptor Doping) compared to the time-dependent response of the calibrated device as shown in Fig. 4 (Time Response of Calibrated Device).

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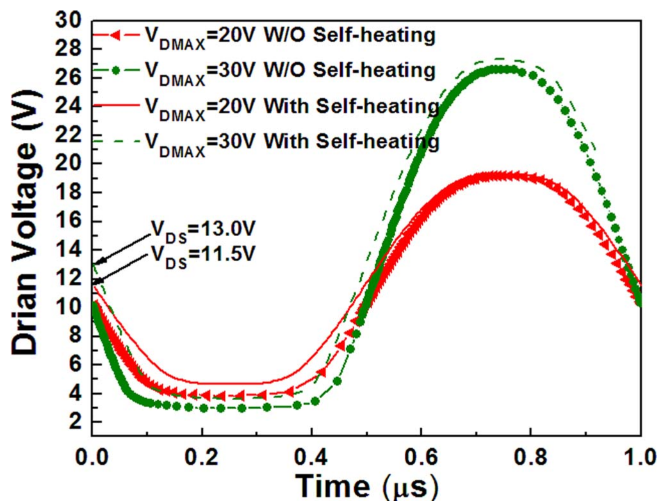

Figure 9. Dynamic drain voltage for V_{DMAX} at $20\,V$ and $30\,V$ with and without self-heating.

result is consistent with expectation that the continuous improvement in the buffer quality reduces buffer related degradation.

Self-Heating Effects in GaN HEMTs

Self-heating due to power dissipation in transistors are generally known to reduce device performance.[14] The increasing temperature affects material transport parameters like a carrier mobility which is reducing with increasing temperature due to enhanced scattering with phonons.[15] In the simulation, the self-heating effects in the AlGaN/GaN HEMT is modeled by solving the heat flow equation:

$$\rho\, C_p \frac{\partial T_L}{\partial t} = \nabla\left(\kappa(T_L)\,\nabla T_L\right) + H \qquad [2]$$

where ρ is the density of the material; C_p is the specific heat; κ is the thermal conductivity; H is the heat generation and T_L is the local lattice temperature. We have modeled the temperature dependence of thermal conductivity using a power law relation of the form:

$$\kappa(T_L) = \alpha_k \left(\frac{T_L}{300}\right)^{-\beta_k} \qquad [3]$$

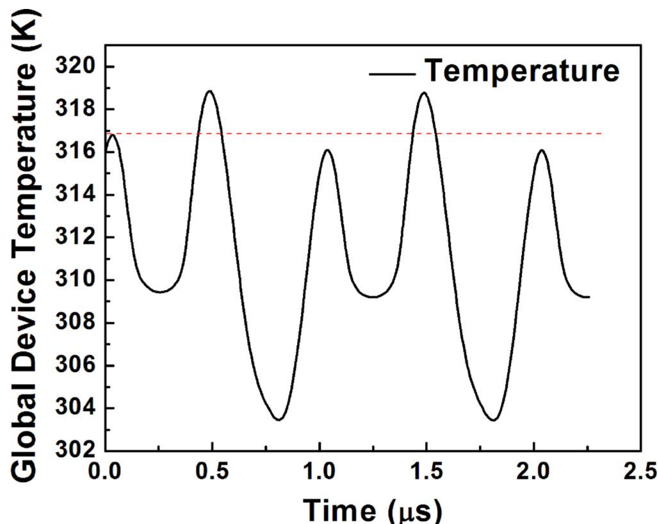

Figure 10. Average temperature of the device as a function of time.

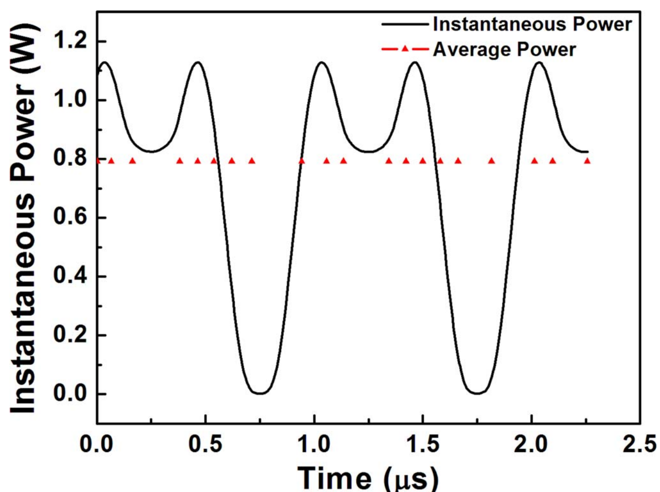

Figure 11. Instantaneous power as function of time. The symbols show calculated average dissipated power (0.79 W).

Using reported experimental data,[16] the optimal fitting coefficients are: $\alpha_k = 2.31\; W K^{-1} m^{-1}$ and $\beta_k = 1.56$.

The assumption of an ideal contact assumes that a thermal resistance, R_{TH}, is zero, which means that the expected results should give qualitative insights in the behavior of the device while still can be easily adapted to a particular device packaging for which the thermal resistance can be determined.

Fig. 9 shows the dynamic drain voltage for V_{DMAX} at $20\,V$ and $30\,V$ respectively, including and excluding the self-heating. One can observe the shift in the DC bias from $10\,V$ to $11.5\,V$ and $13\,V$ for V_{DMAX}, at $20\,V$ and $30\,V$, respectively, when the self-heating model is included. Notice that these results are contrary to those of Fig. 2. In addition, the minimum drain voltage (knee walkout) is increased and there is an initial phase distortion of the signal due to the self-heating. Fig. 10 shows the average device temperature. Fig. 11 plots how the anomalous temporal temperature behavior correlates with the instantaneous power. The average dissipated power is 0.79 W. Fig. 12 shows the lattice temperature profile indicating a peak temperature of

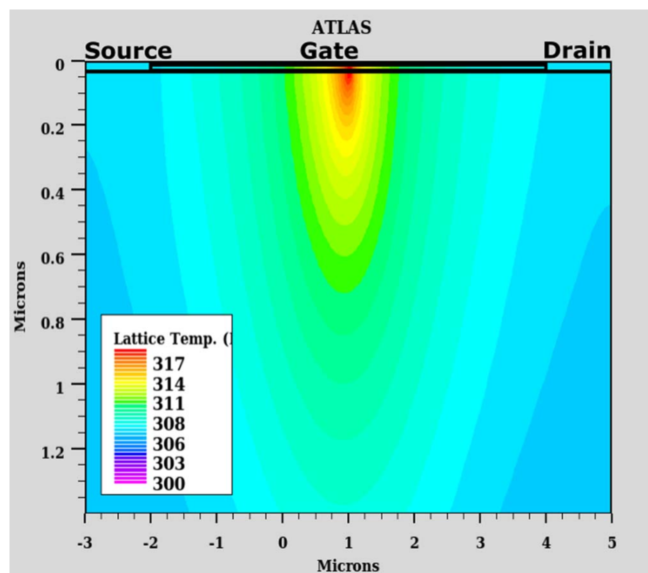

Figure 12. Lattice temperature profiles of the device showing a peak temperature around the gate edge. Instantaneous bias: $V_{DS} = 9.669\,V$, $V_{GS} = -1.678V$, $V_S = 0\,V$, $I_D = 291.8\,mA/mm$.

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318 K at the drain side of the gate edge. This temperature is expected to be higher if a realistic thermal resistance and a substrate thicker than 3 μm would be used in the simulations. Additional results have indicated that at higher operating frequencies, for example 1 GHz, the power dissipation in the device is reduced and the device temperature oscillations are strongly suppressed in time along a negative slope toward lower steady state temperatures.

Conclusions

We have shown that a better insight into trapping behavior can be gained when the physically modeled device is performed in realistic circuit operating conditions. The link between the experimentally observed increase in dispersion with the increasing drain operating bias[3] and the traps located in the buffer[5] have been established. We have reported that of significance is the extent of interaction of the channel carriers and the traps spatially located deep in the buffer. A part of the observed dispersion at the knee of the RF characteristics is attributed to the increased device temperatures due to an increase in a power dissipation. Based on this study, we have proposed that a suitable acceptor doping of the buffer in the region of about 1 μm thick and from around 1 μm below the channel could reduce the knee walkout which is severely affecting the performance and reliability of RF power GaN HEMTs.

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