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Spatial Sensitivity of Silicon GAA Nanowire FETs under Line Edge Roughness Variations

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***Abstract*—Standard analysis of variability sources in nanodevices lacks information about the spatial influence of the variability. However this spatial information is paramount for the industry and academia to improve the design of variability-resistant architectures. A recently developed technique, the Fluctuation Sensitivity Map (FSM) is used to analyse the spatial effect of the Line Edge Roughness (LER) variability in key figures-of-merit (FoM) in silicon Gate-All-Around (GAA) nanowire (NW) FETs. This technique gives insight about the local sensitivity identifying the regions inducing the strongest variability into the FoM. We analyse both 22 nm and 10 nm gate length GAA NW FETs affected by the LER with different amplitudes (0.6, 0.7, 0.85 nm) and correlation lengths (10, 20 nm) using in-house 3D quantum-corrected drift-diffusion simulation tool calibrated against experimental or Monte Carlo data. The FSM finds that the gate is the most sensitive region to LER deformations. We demonstrate that the specific location of the deformation inside the gate plays an important role in the performance and that the effect of the location is also dependent on the FoM analysed. Moreover, there is a negligible impact on the device performance if the LER deformation occurs in the source or drain region.**

***Index Terms*—Si GAA Nanowire; Variability Sources; Line-Edge Roughness (LER); Spatial Sensitivity; Density Gradient (DG) Quantum Corrections.**

I. Introduction

Gate–all-around (GAA) nanowire (NW) FETs are considered to have excellent electrostatic integrity [1]–[3] which makes them a promising alternative for the 5 nm technology node and beyond according the ITRS [4] and IDRS [5]. Their performance will be negatively affected by variability sources as any other semiconductor device. The nature of NW fabrication process [6] makes challenging to eliminate the effect of metal gate granularity (MGG), random dopants (RD), and line edge roughness (LER), which are recognised to be the major variability sources affecting nanoscale multi-gate transistors [7]–[11].

To assess the impact that different sources of variability have on the device performance [12], simulations of several hundreds or thousands of microscopically different configurations are required with corresponding statistical analysis of the resulting data [13]. The most common approach to perform this analysis is via the standard deviation of the figures of merit (FoM). However, the standard techniques that analyse variability effects do not provide an insight into the effect that the spatial location of the variation has on the device performance. Since conventional statistical studies do not account for the local effects of a variability source, the feedback they can provide to the industry is limited. To tackle this issue, the Impedance Field Method [14] was presented to understand the effect of small perturbations in the device (as long as these perturbations are small enough) for RD variability in MOSFETs. Another approach [15] analysed the impact of the dopant positions along the device, again for the RD variations, obtaining a measure of how sensitive different parts of the device are.

In this work, we introduce a technique, the Fluctuation Sensitivity Map (FSM), which provides a deeper understanding of how LER variability affects state-of-the-art Silicon GAA NWs. This technique was already successfully demonstrated for FinFET MGG variations [16], presenting an characterisation of the device sensitivity to the metal grains in the gate. In this approach, we are analysing how the placement and the type of LER deformations affect the device FoM. This data will be useful to improve the design of more reliable GAA NWs beyond the analysis that was previously done using mainly statistical measures.

The structure of this article is as follows. Section II presents the device under study and the simulation approach. Section III describes the FSM technique, shows how it is calculated, and gives results for 22 nm and 10 nm gate length GAA NW FETs. Section IV presents the predictive capability of the technique. Conclusions are drawn up in Section V.

II. Device structure and simulation methodology

The effect of the LER has been studied in two Si GAA NW FETs (shown in Fig. 1) with gate lengths of 22 nm and 10 nm representative of the 14 nm and 5 nm technology nodes, respectively. The 22 nm gate length device designed from a fabricated NW FET [17] has an elliptical cross–section with a shorter/longer diameter of 11.3/14.2 nm, resulting in an effective diameter (D_{ef}) of 12.8 nm. The EOT is 1.5 nm and the length of the source and drain ($L_{S/D}$) regions is 30.8 nm. The 10 nm gate length NW FET has been properly scaled from the 22 nm gate length structure following the ITRS specifications. The shorter/longer diameter of the elliptical cross–section are 5.7/7.2 nm, which makes a D_{ef} of 6.4 nm,

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the EOT is 0.8 nm and $L_{S/D}$ is 14.0 nm. Both device structures have Gaussian n–type doping in the S/D with a peak value of $5x10^{19}$ cm^{-3}. The spread σ determines the abruptness of the doping profile and is equal to 7.1 and 3.2 nm for the 22 and 10 nm gate length devices, respectively. In the channel, there is an uniform p–type doping (10^{15} cm^{-3}).

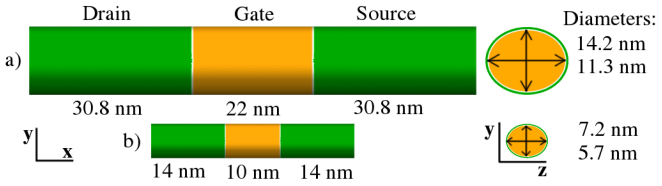

Figure 1. Schematic illustration of the 22 nm gate length GAA NW FET and its 10 nm version, with the same scale, corresponding to 14 nm and 5 nm technology nodes. We set X=0 at the middle of the gate, therefore the S/D contacts are located at both ends of the depicted devices (X=±41.8 and ±19 nm for the 22 and 10 nm gate length devices, respectively).

The devices have been modelled using an in–house built 3D finite–element (FE) density–gradient (DG) quantum–corrected drift–diffusion (DD) device simulator [18]. This simulation toolbox has been previously used for variability studies affecting different types of semiconductor devices and variability sources [11], [19], [20]. The FE tetrahedral mesh is able to accurately replicate the experimental elliptical shape of NW FETs. For the 22 nm gate length GAA NW FET, the I_D–V_G characteristics at both low (0.05 V) and high drain biases (1.0 V) obtained from 3D DD–DG simulations have been calibrated against experimental results [17] and 3D FE Monte Carlo (MC) simulations that include 2D anisotropic Schrödinger equation based quantum corrections (SEQC) along the device channel [11]. For the 10 nm gate length GAA NW FET, since there are no experimental data available, the DD–DG simulations were calibrated to ballistic Non-Equilibrium Green's Function (NEGF) simulations [21] in the sub-threshold region and to SEQC-MC simulations in the on-region (at drain biases of 0.05 V and 0.7 V). The doping profile in the 22 nm gate NW FET has been reverse engineered using I_D–V_G characteristics in the sub–threshold region (the region where electrostatic of transistors dominates) as described in detail in [11]. The DD–DG simulations use Caughey and Thomas low-field electron mobility model, which considers doping dependent mobilities [22], together with lateral and perpendicular electric field models [23]. The mobility model parameters included also the saturation velocity (v_{sat}) and the perpendicular critical electric field (E_{CN}). The work–function (set to 4.56 eV) and the standard deviation in Gaussian doping profile (σ), have also been employed as calibration parameters. The effective electron masses in the DG approach allow us to mimic the source-to-drain tunnelling, via the electron mass in transport direction (m_x), and quantum confinement effects [24], collected in Table I. We have obtained an excellent agreement in the I_D–V_G characteristics for both gate length devices as seen in Fig. 2. Note that, at gate biases larger than 0.5 V, the ballistic NEGF simulations overestimate the drain current since they do not consider scattering events (bottom figure).

Table I
CALIBRATION PARAMETERS FOR THE 22 AND 10 NM GATE LENGTH SI GAA NW FETS: SATURATION VELOCITY (v_{sat}), PERPENDICULAR CRITICAL ELECTRIC FIELD (E_{CN}), DG ELECTRON MASS IN THE TRANSPORT DIRECTION (m_x) AND STANDARD DEVIATION FOR GAUSSIAN DOPING IN THE SOURCE/DRAIN (σ_x).

L_G	22 nm		10 nm	
V_D	0.05 V	1.0 V	0.05 V	0.7 V
v_{sat} [cm/s]	1.0x10^9	1.0x10^9	1.0x10^9	1.0x10^9
E_{CN} [V/cm]	4.0x10^6	1.3x10^5	1.0x10^7	2.5x10^5
m_x [m_0]	0.4	0.32	0.4	0.25
σ_x [nm]	7.1	7.1	3.2	3.2

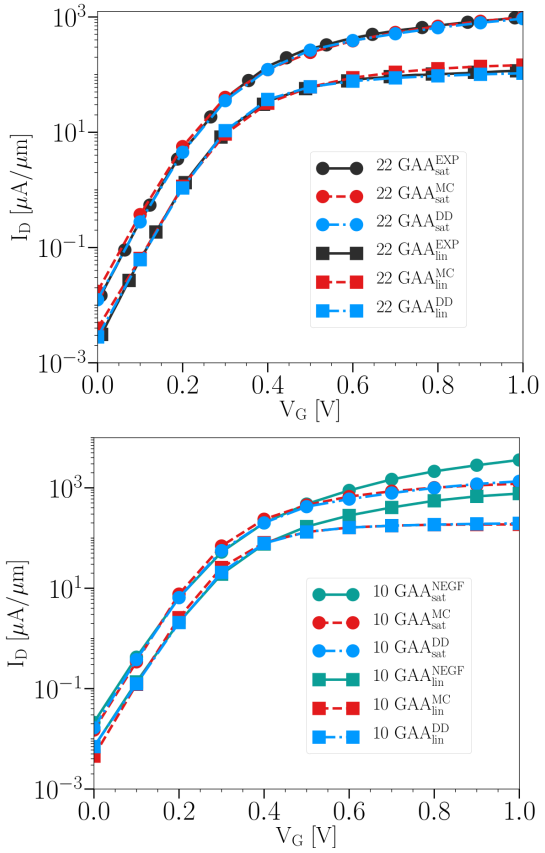

Figure 2. I_D–V_G characteristics comparing 3D density–gradient quantum–corrected drift–diffusion simulations (DD) against i) experimental data (EXP) [17] and Monte Carlo simulations (MC) for the 22 nm gate length Si GAA NW FET (top figure) and, ii) ballistic Non–Equilibrium Green's Function simulations (NEGF) and Monte Carlo data for the 10 nm gate length Si GAA NW FET (bottom figure).

The LER profile has been applied in the GAA NW FET via the Fourier synthesis method, as described in [19], [25]. LER is defined by two parameters: the correlation length (CL), that characterises the deformation along the x–direction of the device, and the root mean square (RMS) height, that describes the deformation in the y–direction. We have focused the study in uncorrelated LER in which different roughness profiles are applied to the positive and negative y-axis, effectively changing the device width in the x-axis. An example of these

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deformations can be seen in Fig. 3. We have analysed two CL values (20 and 10 nm) and three RMS heights (0.85, 0.7 and 0.6 nm) that are consistent with the values observed experimentally [17]. We have then generated sets of 300 realistic LER profiles for each CL and RMS height and applied them to the studied devices. Fig. 3 shows an example of the 22 nm gate length Si GAA NW FET under a LER deformation with a 0.8 nm RMS and a 10 nm CL.

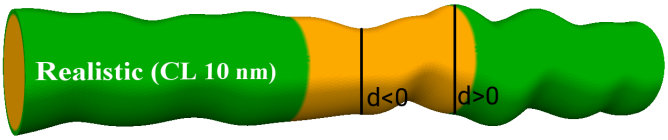

Figure 3. Example of the 22 nm gate length Si GAA NW FET affected by the LER (CL=10 nm and RMS=0.85 nm). Two locations are highlighted either with a positive ($d(x) > 0$) or a negative ($d(x) < 0$) change in width of the device cross-section with respect to the non-deformed device.

III. Construction of the FSM

The Fluctuation Sensitivity Map (FSM) is a tool that represents the spatial sensitivity of the device under a variability source, as previously demonstrated when characterizing the effect of the metal gate granularity [16]. To calculate the FSM, an ensemble of devices affected by some kind of fluctuation due to a variability source has to be simulated. At the end of each simulation, a set of FoMs (e.g. $I_{\rm off}$, V_T, $I_{\rm on}$) is extracted, and paired with the corresponding fluctuation. In a LER study, this fluctuation is the deformation that occurs at each location of the device along the x-direction, which can change the device width or its centre. It is important to bear in mind that the FSM will provide the sensitivity of the device to the type of deformation that has been used in the FSM construction.

$FSM(x)$ represents how sensitive a FoM, ϕ, is to the transversal deformation, $d(x)$, present at a x–coordinate, that changes the device width (see Fig. 3), and is given by:

$$FSM(x) = \frac{\partial \phi}{\partial d(x)} \tag{1}$$

Using the obtained $FSM(x)$, we can formulate the following equation for the k-th device affected by the corresponding LER deformation profile, $d^k(x)$:

$$\phi^k = FSM(x) \cdot d^k(x) + \phi_0^k, \quad k = 1, ..., N \tag{2}$$

where ϕ^k is the FoM obtained from the simulation of the k-th device, ϕ_0^k is a fitting parameter and N is the total number of studied devices.

This is the actual set of linear equations that has to be solved. We are running N simulations in total with different deformation profiles, so for each location x, we have N equations to solve. There is not a single value of the $FSM(x)$ that fulfils Eq. (2), so we solve a least squares problem instead to obtain a value for $FSM(x)$. Note that since we are using a discretized mesh, with P elements in the x-direction, we have a set of $N \times P$ equations to be solved. N and P have to be as large as possible to account for different deformations along the device, in our case, $N = 300$ and $P = 1670$ for this particular device. This $FSM(x)$ is presented in the following section for different scenarios.

A. FSM generated using realistic LER profiles

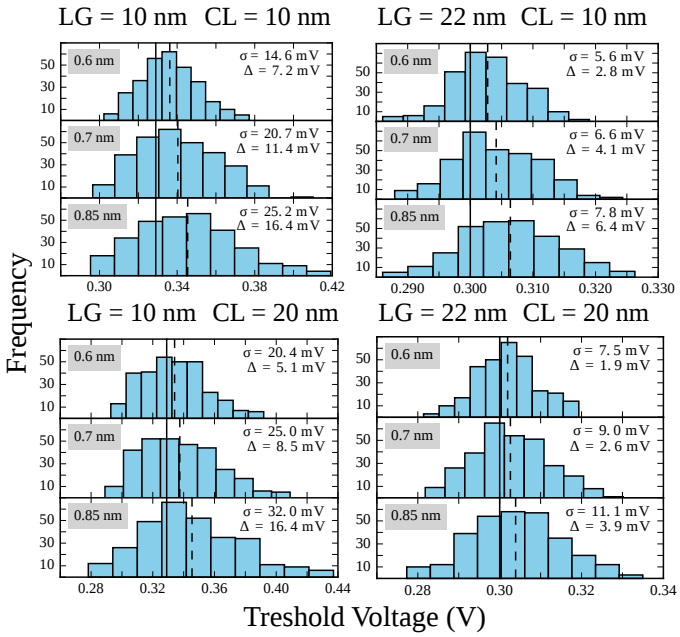

Figure 4. Distribution of V_T due to LER variability for the 22 and 10 nm gate length Si GAA NW FETs at a low drain bias of 0.05 V as a function of the CL (10, 20 nm) and the RMS height (0.6, 0.7, 0.85 nm as shown in the grey boxes). The standard deviation (σ) and mean value $\langle V_T \rangle$ (dashed line) of the distribution are indicated together with the V_T of the ideal device $\mathrm{V_{T_{ideal}}}$ (full lines) and the V_T shift Δ=$\langle V_T \rangle$–$\mathrm{V_{T_{ideal}}}$.

Fig. 4 shows the distribution of V_T due to LER variability in the 22 and 10 nm gate length Si GAA NW FETs at a $V_D = 0.05$ V as a function of the CL and the RMS height. The standard deviation (σ) and mean value $\langle V_{\rm T} \rangle$ (see dashed lines) of the distributions are also shown, together with the $V_{\rm T}$ of the ideal, not deformed device $\mathrm{V_{T_{ideal}}}$ (see full lines). The V_T shift $\Delta = \langle V_{\rm T} \rangle$-$\mathrm{V_{T_{ideal}}}$ due to LER is also included for comparison. As expected, the variability increases when the CL or the RMS amplitude of the LER are increased [26]. For both gate length devices, σV_T is approximately linearly proportional to the RMS height and can reach up to 11.1 mV in the 22 nm gate length NW FET (CL=20 nm and RMS=0.85 nm) and 2.9 times larger value (32.0 mV) in the 10 nm gate length device. The V_T shift increases with the RMS height and increases also for the smaller CL of 10 nm, a behaviour also observed in FinFETs [20].

The results of this statistical analysis are valuable but they do not provide any spatial information about the effect of the LER on the device performance. Therefore, the feedback provided to semiconductor industry and academia is very limited, without much information regarding how to make improvements in device design. For this reason, we have developed the FSM, that represents the spatial sensitivity of the device under the studied variability source (LER in this case). This allows us to understand how variations happening

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in different locations of the device impact the key FoM that characterize the behaviour of the device, hence getting more valuable information that can be used to improve device architecture.

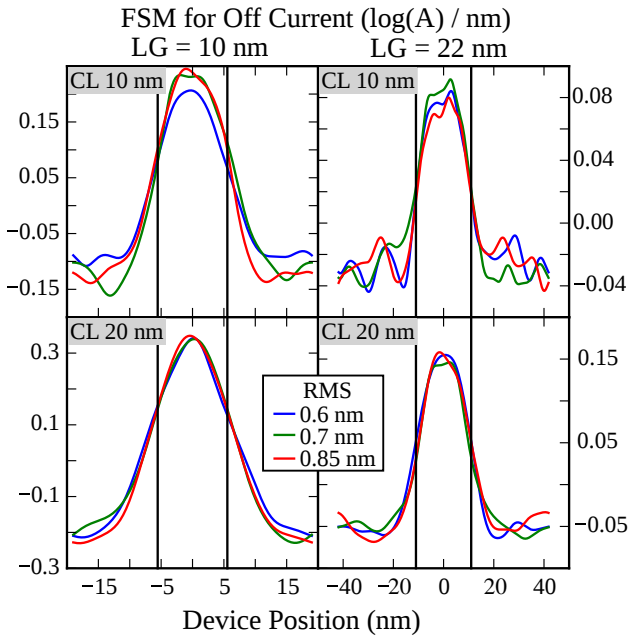

Figure 5. I_{off} Fluctuation Sensitivity Maps for an off-current along the transport direction in the 10 and 22 nm gate length Si GAA NW FETs at a low drain bias of 0.05 V. The maps are shown for CLs of 10 nm (top) and 20 nm (bottom) and the indicated RMS heights. The maps are obtained from 300 simulations. The area enclosed between the black lines is the gate region.

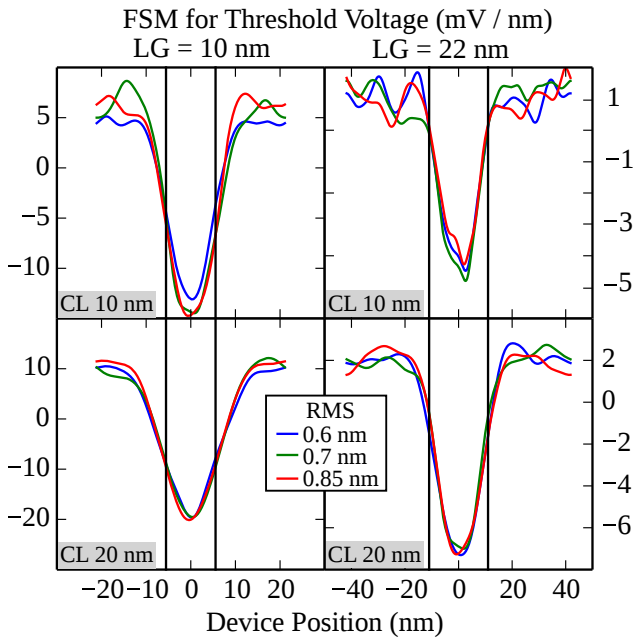

Figure 6. V_T Fluctuation Sensitivity Maps for a threshold voltage along the transport direction in the 10 and 22 nm gate length Si GAA NW FETs at a low drain bias of 0.05 V. The Maps are constructed for CLs of 10 nm (top) and 20 nm (bottom) and the indicated RMS heights.

Fig. 5 shows the I_{off} FSMs for the the 22 and 10 nm gate length GAA NW FETs due to LER variability generated via realistic profiles. Three different RMS values for 10 nm CL (top figures) and 20 nm CL (bottom figures) were considered. Note that positive/negative FSM values indicate that an increase in the device cross-section will lead to an increase/reduction in the I_{off} and a zero FSM indicates that there is no change.

For both gate length devices, the gate is the most sensitive region to LER variations, observing the I_{off} FSM maximum value at the middle of the device (X=0). A LER induced deformation which makes a device width wider at the source/drain leads to a narrower cross–section in the gate area, and vice versa, as a result of correlations in the LER profiles. The influence of the gate region on the sensitivity of the source/drain is more pronounced when the correlation length is larger, or the device shorter, as seen in Figs. 5 and 6. On the other hand, when the correlation length gets shorter, or the device larger, this effect is reduced and noise appears in the source-drain regions. This can be seen in Figs. 5 and 6 at the top-right subfigures, which are the cases of a lower CL and a larger LG. A similar behaviour was found when studying the metal gate granularity [16], where the device sensitivity was better represented when the grain sizes were large. In the following section we have developed a technique based on synthetic LER profiles that are able to capture the local effect of the perturbation, without any non-local interaction.

Fig. 6 presents the V_T FSMs for the the 22 and 10 nm gate length GAA NW FETs due to LER variability generated via realistic profiles. We have found a similar behaviour to the one shown in Fig. 5 but the results have the opposite sign. The sensitivity is lower and positive in the S/D regions, and larger and negative inside the gate area. Therefore, a widening of the device body in the gate region due to LER will imply both a reduction of V_T and an increase in I_{off}. To further demonstrate the validity of this affirmation, Fig. 7 presents schemes of the two GAA NW FETs under LER that produce extreme V_T values from the statistical distribution shown in Fig. 4 (when CL=10 nm and RMS=0.85 nm). The device that presents a substantial narrowing in the gate region when compared to the non-deformed device (shown in the grey rectangular shadow) requires the largest gate voltage to reach the threshold (top figure of Fig. 7). However, the device that requires the minimum gate voltage to reach the threshold (bottom figure of Fig. 7), has a wider gate than that of the non-deformed device (shown again the grey rectangular shadow).

B. FSM generated using synthetic LER profiles

As we have mentioned in the previous section, a problem that arises when studying the sensitivity to LER using realistic profiles, generated by Fourier synthesis method, is the spurious contribution of the S/D regions to the FSM. Therefore, in order to isolate the sensitivity of the gate, we have created a large set of synthetic profiles that will apply a single Gaussian vertical deformation at points along the device. This Gaussian deformation has an amplitude of 2 nm, and a full width at half maximum (FWHM) of 1.5 nm. Note that, the actual shape

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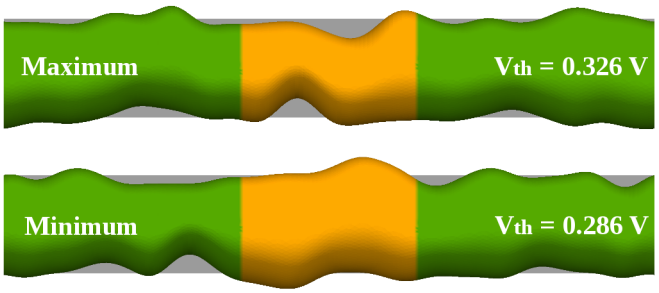

Figure 7. Maximum and minimum V_T values induced by the LER variability under 10 nm CL and 0.85 nm RMS deformations in the 22 nm GAA NW FET. The original shape of the device is shown in grey, underneath the figures. Note the device with the maximum V_T has a smaller width in the gate contact area as predicted in Fig. 6.

Figure 8. Example of the 22 nm gate length Si GAA NW FET affected by synthetic LER profiles that artificially change, only in a small region, the width of the device (top figure) or perform a transversal deviation, creating an offset (bottom figure).

of the perturbation has to be smooth, so it does not have a negative impact in the quality of the underlying mesh when applying the deformation to the device. We have selected the amplitude to represent a similar deformation to a realistic LER, and the FWHM to be as small as possible without impacting the quality of the mesh. Using these synthetic patches, we are able to sweep all the possible locations along the device measuring the spatial sensitivity to LER variations. We have tested two possible synthetic LER scenarios: i) width type deformations, where the centre of the NW does not change but the width of the device at a certain point does (see Fig. 8 top) or ii) offset type deformations, that have a fixed NW width but a varying centre, creating a transversal deviation (offset) at a certain point of the device (see Fig. 8 bottom).

Using the synthetic profiles to understand the sensitivity of the device under deformations will allow us to pinpoint the key locations of the gate that contribute the most to the sensitivity of the device under LER variability. We have localised five regions of the device that are found to be of interest when analysing V_T and I_{off}: i) the source region (S), ii) the section of the gate that is near the source–gate border (SG), iii) the middle of the gate (MG), iv) the section of the gate that is near the gate–drain border (GD) and v) the drain region (D).

The FSM obtained for the I_{off} using this synthetic profiles is shown in Fig. 9, for both types of deformations using 120 simulations for each case. In both cases, the sensitivity outside

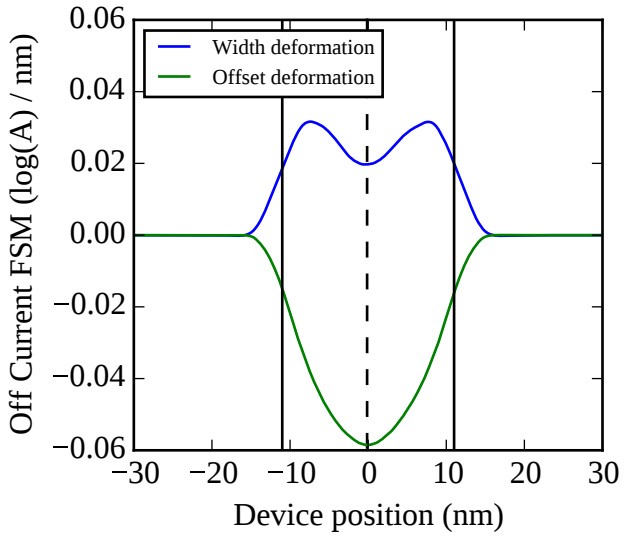

Figure 9. I_{off} FSM obtained from the synthetic LER generated for both width and offset deformation types for the 22 nm gate length Si GAA NW FET at a drain bias of 0.05 V. Each set is composed of 120 simulations.

the gate area is close to zero, because the applied deformations are localised and their effect does not extend to other regions of the device. The most sensitive regions of the device to LER variations are located inside the gate area, as also seen before in Fig. 5. When analysing the impact of the gate width deformations on the I_{off} FSM, we observe that the sensitivity is positive and has two maxima located in the SG and GD regions, and a minimum located in the middle of the gate. A positive sensitivity indicates that any width type deformation will lead to a overall widening of the device channel and an increase of the I_{off} when compared to the ideal device with no deformations. In order to understand this behaviour, Fig. 10 presents 2D cross–sectional plots showing the electron concentration (in a logarithmic scale) inside the device at V_G=0.0 V and V_D=0.05 V for the five previously indicated key regions and compares them with the ideal device (not affected by any deformation). Note that the iso–surfaces have been adjusted to help visualising the behaviour at the middle of the channel. As expected, both the S and D configurations do not influence the I_{off} of the device, yielding the same value as the ideal device (the electron concentration inside the device is the same for the Ideal, width S and width D cases). A deformation located inside the gate but near the border of the S/D regions leads to an increase of I_{off} with respect to the ideal device, which is consistent with both the two maxima observed in the FSM and the increase in the electron concentration seen in the middle of the device (see Fig. 10 width SG and width GD cases). However, if the deformation is placed in the MG, I_{off} drops with respect to the SG and GD cases due to a decrease in the electron concentration in the middle of the device (see Fig. 10 width MG case). This drop of off-current explains the lower sensitivity seen in the FSM (Fig. 9). We can see in these figures the quantum-mechanical confinement effect under the gate resulting in the electron concentration being pushed away from the oxide–

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semiconductor interface [27].

When analysing the impact of the gate offset deformations on the I_{off} FSM, we observe that the sensitivity inside the gate has a negative sign (opposite behaviour to the width deformations), which means that any offset deformation will lead to a reduction of the I_{off} with respect to the ideal device (see an example in the bottom cross–section of Fig. 10). Note that the real width of the device channel does not change with an offset deformation, but the effective channel for electrons to flow is reduced, which explains the negative sign of the FSM. The I_{off} FSM due to offset deformations has only a maximum sensitivity value (with negative sign) located in the MG. The spatial information provided by the FSM can serve as a guide to create LER–resistant device architectures. This information could not be known or understood if only pure statistical analysis (such as the one presented in Fig. 4) is used.

Fig. 11 shows for the 22 nm gate length Si GAA NW FET, the I_{off} FSM obtained from the synthetic LER for both width and offset deformation types at a high drain bias of 1.0 V. When analysing the impact of the width deformations in the gate, the two highest sensitivity regions are still located in the SG and GD, but they are not longer symmetric due to the displacement of the potential barrier; placing the maximum sensitivity in the SG, as previously seen in [16] for MGG variations. Similarly, when analysing the impact of the gate offset deformations on the I_{off} FSM, we observe that the highest sensitivity inside the gate is not longer in the middle of the gate (X=0) but slightly shifted towards the SG region.

Fig. 12 presents the V_T FSM calculated from all the configurations of the two synthetic deformation types using 120 simulations per set. As expected, the sensitivity in the S/D region is again close to zero when using the synthetic profiles. Both deformation types affect similarly the V_T FSM, unlike in the I_{off} case, although with an opposite sign. The gate region is the most affected by any LER variation. As previously seen with the I_{off} FSM, the SG, MG and GD regions show distinctive behaviours. Since an offset deformation produces a mirror image of the width one (not in scale) with respect to the V_T sensitivity, we have limited the analysis to the width type to understand the effect of the placement of a deformation inside the device. Fig. 13 presents 2D cross–sectional plots showing the electron concentration (in a logarithmic scale) inside the device at V_G=V_T for the five previously indicated key regions and compares them with the ideal device. Here, we have used a constant current criterion of ($1.47\ \mu A$) to determine the V_T value. A deformation of the width of the device in either the source or drain does not affect the performance of the device. Note that there is no difference between the V_T of width S and width D cases and that of the ideal device (see Fig. 13), which is consistent with the close-to-zero sensitivity seen in the FSM for the S/D. If the deformation happens in the MG position, there is an increase in V_T (in agreement with the positive FSM seen in Fig. 12) and in the electron concentration when compared to the ideal device.

In order to understand this increase in electron concentration, we have to bear in mind that following the constant

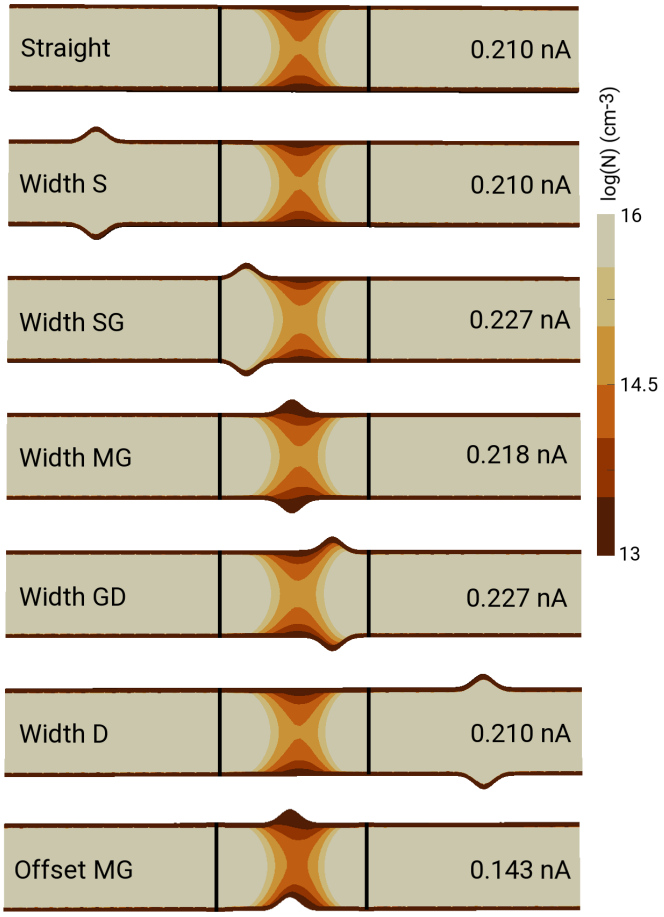

Figure 10. Illustration of several cross–sections (labels at the left) of the 22 nm gate length GAA NW FET under synthetic LER variability, showing iso–surfaces for the electron concentration (in a logarithmic scale). The cross–section of the straight ideal device is included for comparison at the top. In all cases, the device is polarized at $V_G = 0.0$ V and $V_D = 0.05$ V to identify the I_{off} sensitivity. The corresponding I_{off} values for each case are also shown (right hand side of the figures).

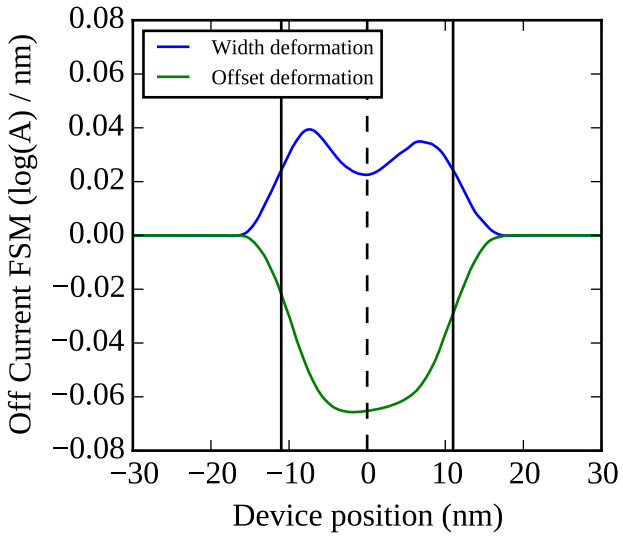

Figure 11. I_{off} FSM obtained from the synthetic LER generated for both width and offset deformation types for the 22 nm gate length Si GAA NW FET at a high drain bias of 1.0 V.

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current criterion chosen, V_T is the gate bias at which the current reaches a certain fixed value. Therefore, the MG configuration needs to be more polarised (hence the larger electron concentration) to reach the threshold than the ideal device. A width deformation in either the SG or GD leads to both a reduction in V_T (consistent with the negative FSM observed in Fig. 12) and in electron concentration in the middle of the gate when compared to the ideal devise. Note that, unlike the I_{off} FSM where both SG and GD provided the same sensitivity values, the V_T sensitivity due to LER is larger for the GD region than for the SG (see also their difference in V_T in Fig. 13). This is due to the influence of a drain bias that becomes more noticeable when a gate voltage is higher.

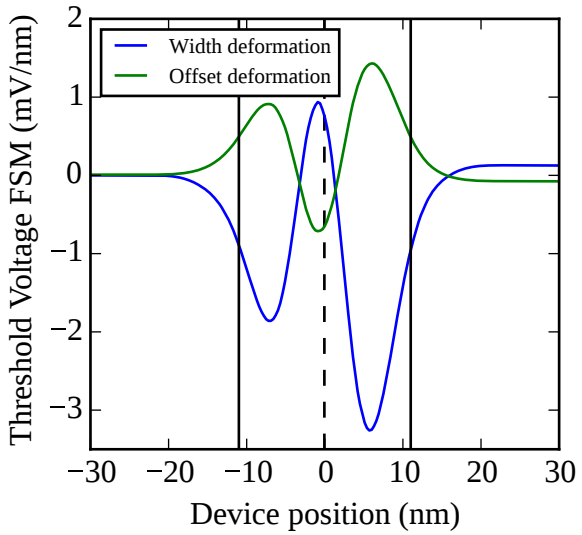

Figure 12. V_T Fluctuation Sensitivity Maps for the 22 nm gate length Si GAA NW FET obtained using synthetic profiles that perform either a width or an offset deformation. Each map is obtained from 120 simulations. The drain bias is 0.05 V.

Using the FSM, it is possible to understand where the sensitivity of the device is higher, how several FoM have different sensitivity and also how the behaviour of a transistor changes at a different bias conditions. For instance, the FSM presented in Figs. 9, 11 and 12 are examples of the feedback which this tool is capable to provide to the industry's R&D. Thanks to this tool, the industry can focus its efforts to reduce variability issues in the key locations of a device, or check how new architectures will be affected by these problems.

IV. Predictive power of the FSM

As we mentioned in the previous sections, the FSM represents the sensitivity of the different positions of the device to LER variations, therefore, is expected that it is also capable of obtaining an estimation of the device behaviour under a given LER deformation profile. The first step of this procedure is to obtain the FSM via Equation (1) that we have already done in previous section. Next, these obtained values of FSM can be used to estimate the value of a FoM, ϕ^k affected by a new deformation profile d^k as follow:

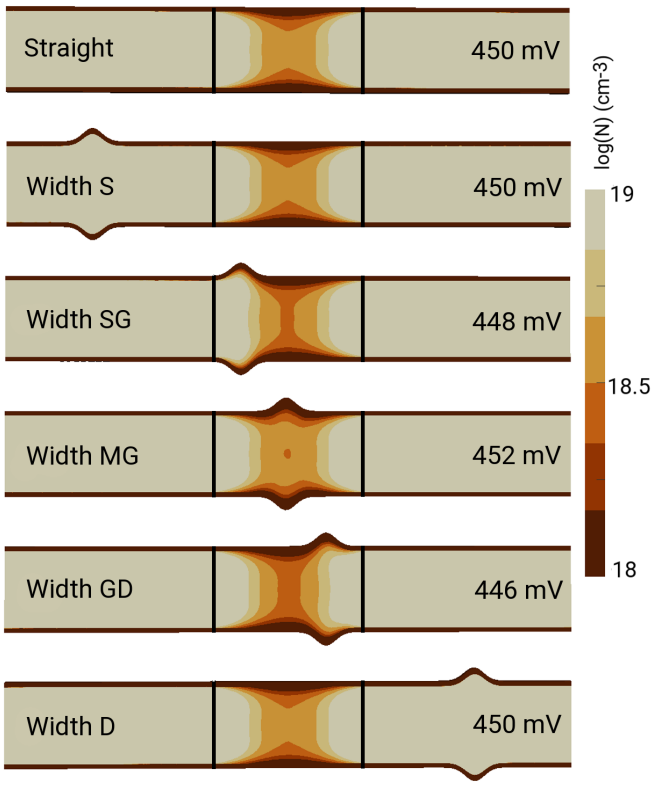

Figure 13. Illustration of several cross–sections of the 22 nm gate length GAA NW FET under synthetic LER variability, showing iso–surfaces for the electron concentration (in a logarithmic scale). The cross–section of the ideal device (top) is included for comparison. The device is polarized at V_G=V_T (obtained via a constant current criterion) to highlight the V_T sensitivity. V_T is shown at the right hand side of each device.

$$\phi^k = \sum_i FSM(x_i) d^k(x_i) \tag{3}$$

Fig. 14 shows a scatter plot of the simulated V_T versus the V_T predicted via the FSM presented in Fig. 6. We have obtained the predicted V_T values using only the FSM and the deformation profiles, and the values are highly correlated to the originally simulated ones (see correlation coefficient, r, printed inside the figures). We use arbitrary units to show the correlation between the predicted and the simulated values. There is an offset and also a scaling factor between both values, but they have no impact on r. The full procedure to take into consideration the scaling factor and offset was previously shown for MGG variability [16]. Note that, the larger the number of simulations used to calculate the FSM the higher the correlation coefficient will be, because the statistical error will be reduced. This large correlation between the predicted and the fully simulated values confirms that the FSM represents the device sensitivity, and also proves the validity of the FSM as a powerful tool to obtain the spatial dependence of the LER.

Another important benefit of this tool is the ability to provide an accurate prediction of simulation results without having to spend the necessary computational resources to run all the simulations. Using this predictive power capability and in order to save computational time, the FSM can be calculated

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for a single combination of CL and RMS values, and the other CL and RMS combinations can be estimated with the previous formula, as we have already demonstrated. This method was previously successfully applied [16] to MGG variability.

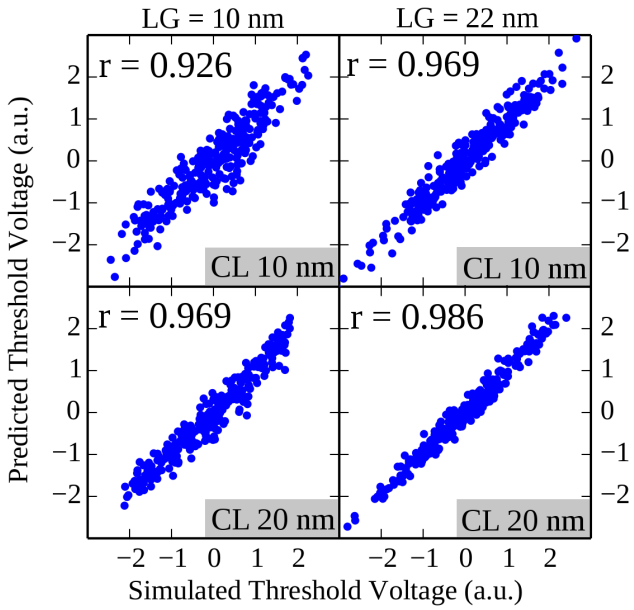

Figure 14. Scatter plot of the predicted V_T distribution using the FSM versus the simulated V_T for the 22 nm (right figures) and 10 nm gate (left figures) length GAA NW FETs as a function of the CL when the RMS height is 0.6 nm. The V_T values are normalized with respect to the mean value (set at 0). The correlation coefficients (r) are shown to validate the predictive capabilities of the method.

V. Conclusion

A technique based on the creation of a Fluctuation Sensitivity Map (FSM) has been presented for the investigation of LER induced variability in semiconductor transistors. As an example, we have applied the technique to two Si GAA NW FETs with 22 nm and 10 nm gate lengths. The shape and architecture of the 22 nm gate NW FET is modelled from an experimental structure thanks to a FE mesh of the simulation domain. Initially, the LER variability was statistically analysed and presented via histograms. For both gate length devices, σV_T, increased with both the RMS height and the CL, and reached up to 11.1 mV for the 22 nm gate length device (CL=20 nm and RMS=0.85 nm). The 10 nm NW FET has a value of σV_T of 32.0 mV, 2.9 times larger than for the 22 nm device. The impact of the V_T shift due to LER was also studied. We demonstrated that the shift increases with the RMS but decreases with the CL. After that, we used the FSM to investigate the spatial sensitivity of the different regions of the devices under the effect of LER. In order to complete the analysis, we have calculated the sensitivity of the devices using both realistic and synthetic deformation profiles.

We have established pointers using the FSM that could serve as a guidance for the design and fabrication of LER-resistant device architectures. We have demonstrated that any LER-type deformation located either in the source or drain regions will not affect the performance of the device. However, if the deformation is located inside the gate, it will significantly affect the device performance. Moreover, the deformation type and its precise location inside the gate plays also an important role. If the deformation widens the channel in the gate region, I_{off}/V_T will increase/decrease with respect to that of the non–deformed device. If the deformation produces a transversal deviation, the effective channel region will be reduced and I_{off}/V_T will decrease/increase when compared to that of the straight device. Also, if the deformation widens the channel in the middle of the gate there will be an increase in threshold voltage. If it is located close to the source or to the drain border, the threshold voltage will decrease when compared to that of the straight, LER unaffected NW.

We have also shown the predictive capabilities of the FSM with regard to the V_T, allowing to obtain the value of the FoM without requiring to run a full set of simulations. The FSM is capable of predicting the threshold voltage value with at least a correlation of $r = 0.926$ for the worst case scenario.

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