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Investigating the Electrical Properties of Zinc Oxide Nanostructures

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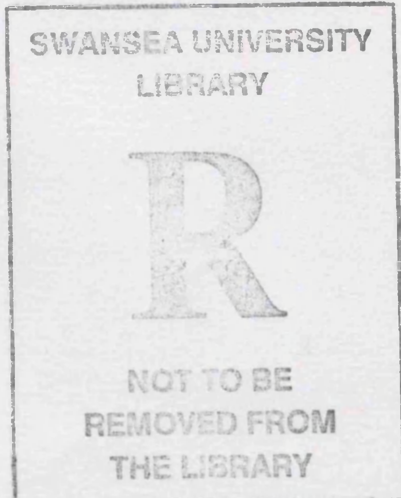
Submitted to the Swansea University in fulfilment of the requirements for the Degree of MRes Nanoscience to Nanotechnology 2011.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ABSTRACT

Electron transport characterisation is fundamental step forward in exploring the potential of a semiconductor material to be used as building material in electronic devices. Several device parameters such as channel length, gate thickness, extent of doping etc. are determined with the help of precise electron transport measurements. Four point probe measurement is considered as one of the reliable electrical characterisation technique especially in case of semiconductor materials. Several key parameters such as resistivity, carrier type, carrier concentration, carrier mobility etc., can be directly calculated to a high degree of accuracy by carefully following simple experimental procedures of four point probe. In this project fundamental electrical characteristic of two different nanostructures (1-D thin films and 2-D nanowires) of ZnO were studied. Resistivity of as grown ZnO thin films is found out to be of the order of $1000\ \Omega cm$, post-growth treatment of thin films in the presence of N_2O environment increases their stability and resistivity is reduced to less than $100\ \Omega cm$. This is considered to be due to the N-Zn bonding, as annealing in the presence of O_2 alone resulted in increase in the resistivity. From the measured resistivity of thin films of different thickness it is also established that resistivity of Cu doped ZnO thin films is inversely proportional to the film thickness. An exponential dependence of resistivity on the presence on Cu content in thin film was observed and their resistivity can be easily controlled by varying the percentage of Cu in ZnO thin films. In the case of nanowire devices the resistivity and trans-conductance measurements were performed using four point probe arrangement to determine the true characteristics of the nanowires. The resistivity of the samples was found out to be in the range of 1.10×10^{-1} to $5.58 \times 10^{-2} \Omega cm$. It was observed that with decrease in the width of nanowire beyond 90nm the resistivity decreases because of the decrease in surface vacancies, which result in reduced inelastic scattering events and electron mean free path increases. From the conductance versus gate voltage (V_g) plot, n-type nature of ZnO nanowires is observed. The carrier mobility for the ZnO nanowires was determined to be between 8 and $100\ cm^2/Vs$ and carrier concentration in the range of 5.66×10^{17} to $3.77 \times 10^{19}\ cm^{-3}$.

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Chapter 1. INTRODUCTION

1.1. Introduction

In this MRes thesis, the experimental results obtained from electrical transport characterization of two different kinds of semiconducting nanostructured materials, namely thin film and nanowire, will be presented. These nanostructured materials are classified as one-dimensional (1-D) nanowires [1] and two dimensional (2-D) thin films [2] on the bases of existence of electron confinement in them due to their nanoscopic shape and size [3]. Quantum size effect electron confinement is believed to be the fundamental reason for their different behaviour from the devices of same materials in their bulk/macroscopic sizes [4]. Transition metal (TM) doped ZnO semiconductors is of great interest due to its potential applications in spintronics technology [5-7], hence characterising these material is of great importance. In this chapter an overview of the origin and different generations of solid state devices are discussed, followed by current challenges in the area. Very briefly fundamental views of key concepts related to the experiment are discussed next. Objective and motivation for this work are discussed towards the end of the chapter and the chapter is concluded by giving the summary of structure and organisation of the complete thesis.

1.2. Solid State Electronic Devices – Origin, Generations and Commercial Driven Life Cycle

With the incredible success of first ever general-purpose electronic computer 'Electronic Numerical Integrator And Computer' (ENIAC) [8, 9]. Electronic computers was seen as the only option to invest in the future as ENIAC was about 1000 times faster than its counterparts based on the electromechanical principals at that time [8]. The success of ENIAC shifted huge research focus in the improvement of the system, vacuum tubes were identified as the weakest link in the chain with unfavourable features like large switch time, heat dissipation and big size etc., possibilities of their replacements with other novice components were explored. Key breakthrough towards this was reached with successful demonstration of first solid state transistor (Figure 1.1) based on germanium (Ge) [10], followed by reporting of physical principles involved in the solid state transistor action [11]. However it was soon realized that Ge based transistors are not the best and practical/real-time

solution and need for other better suitable material for solid state devices was felt and looked into. Although Ge is easier to work with and also offers higher frequency operations but it lags on several other key performance parameters [12] with high leakage current in "off" condition [13] and the operation of devices restricted to only in the temperature range of 0 to 70°C.

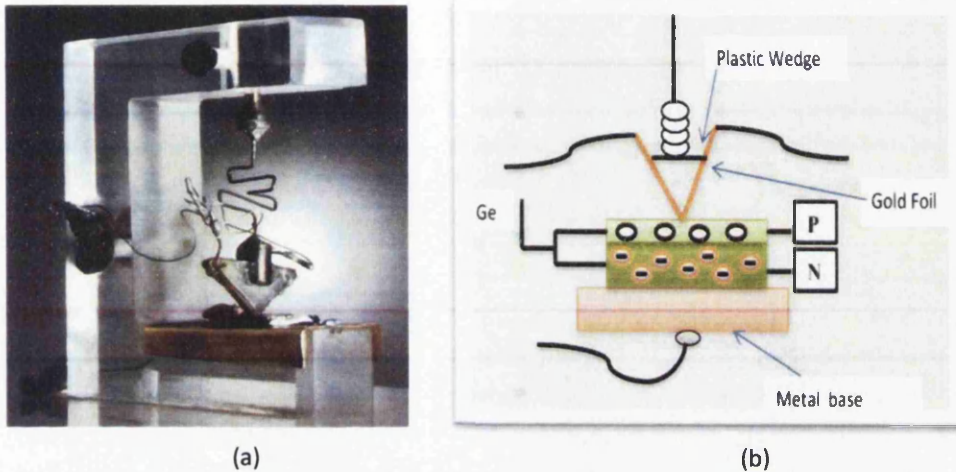

Figure 1.1: (a) Image of first transistor fabricated and successfully demonstrated by William Shockley at Bell Labs. (b) Schematic representation of first transistor (not drawn to scale).

Most of the limitations of Ge based transistors were overcome with the successful fabrication of first silicon (Si) based transistor [14]. Device made from Si offers lesser leakage current [15] and had broad range of operating temperature -55 to 125°C [14, 15]. With the availability of commercial high-purity "semiconductor-grade" Si wafers [16], it became the first choice for the solid state devices. While improving transistors performance and exploring other potential applications the main focus was shifted to reducing the feature size. This led to the next breakthrough of miniaturized electronic circuits called integrated circuits (IC) [17, 18]. IC performed the job of a number of electronic components from a single chip. With the developments of IC it was realized that more and more number of components can be added in an IC and from the empirical observation in the growth of IC component density it was predicted that the component density of IC's will double every year, this was changed latter to double every two year period [19, 20]. This observation has since been dubbed as "Moore's Law" and as it is never been violated and this now has become enormously influential. Some have even called it as a self-fulfilling

prophecy. Moore's law and its importance are discussed in more detail in the next chapter.

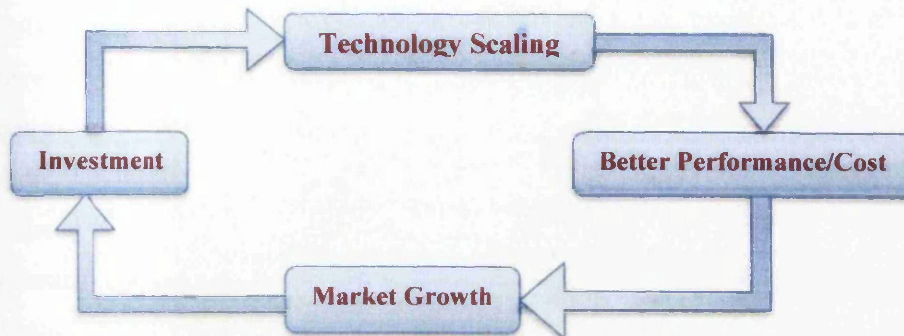

Figure 1.2: Market driven life cycle of solid state electronic devices.

Several factors other than just better performance, like cost per feature, cost for up-gradation/replacement of current manufacturing system govern the migration from one generation of technology to the next. In Figure 1.2 the commercially driven life cycle of solid state devices is presented. This cycle is repeating itself for past 55 years without any problem as the scaling down the feature size was always easily achieved with novice invocations over the course of time, however this time improving the device performance with simply scaling down the feature is not possible due to several scaling limitations like device cross talk, huge heat dissipation and large doping. So the efforts are made in making devices with alternate working principles. Technologies based upon optoelectronics and spin electronics have been reported as potential replacement of conventional present day electronic devices [21]. While the control/manipulation of charge is the fundamental principal of conventional electronic devices, the controlled transition/recombination of electrons between different energy levels which leads to the absorption/emission of photons in the different range of the electromagnetic spectrum, forms the basis of optoelectronics and devices classified as spinelectronics just work on the spin of electrons. Compared to the charge and the photon, it is rather difficult to manipulate/control and detect the spin of an electron [21]. In fact, most of the devices reported/fabricated working on the principles of spinelectronics to date still relies primarily on the spontaneous ordering of spins, in the form of different types of magnetic materials. Novice materials called dilute magnetic materials (DMS) having hybrid properties of semiconductors and magnetic are required for the

fabrication/realization of such devices. Charge-based devices (conventional electronic devices) are currently dominant in both areas of information processing and storage. Photonic devices are used largely in information transmission and display with limited/selective special requirement driven application in storage too. However in contrast to the wide range of application of the charge and photon based electronic devices presently the applications of spin-based materials and devices or spintronics, are still limited to just information storage [22]. But from a long term perspective, device made on the principle of spintronics has the potential of creating the next generation devices with faster response, low power consumption and less or no moving charges involved during their operation [23]. Also these devices promise integration between the information processing devices and information storage devices which enables them to be used for potential application in quantum information processing [24].

1.3. Objective and motivation of this work

The primary aim of this project is to investigate the electrical properties of ZnO and Cu doped ZnO nanostructures and explores their potential application as basic building material for the next generation solid state electronic devices. Recent research and findings in this area of research encourage and motivates us towards undertaking this project.

1.4. Thesis organisation

After giving a brief background of this research, an overview of the work done so far on ZnO and Cu-doped ZnO is provided in Chapter 2. Other TM doped ZnO also briefly introduced in this chapter. Chapter 3 Formulation and improvement of research methods and models and their validation is presented in this chapter. Growth and characterization techniques used in this work, in which the focus is on those which are more specific to this work. The structural and chemical analyses of the obtained films are given in Chapter 4, while Chapter 5 describes electrical transport properties, respectively. This work is summarized and some suggestions for future work are also provided in Chapter 6.

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Chapter 2. LITERATURE REVIEW

2.1. Introduction

Nanotechnology is defined, according to the National Science and Engineering Technology Council (NSET) as:

"Research and technology development at the atomic, molecular, or macromolecular levels, in the length scale of approximately 1-100 nm range, to provide a fundamental understanding of phenomena and materials at the nanoscale and to create and use structures, devices, and systems that have novel properties and functions because of their small and/or intermediate size. The novel and differentiating properties and functions are developed at a critical length scale of matter typically under 100 nm."

In this chapter experimental and theoretical work related to the experiments performed by me will be discussed. First Moore's law is discussed followed by scaling limitations of current technologies in keeping up with Moore's law and possible technologies having potential of replacing the current electronic devices. Importance and need of electrical characterisation is discussed next. Next generation of electronic devices based on novice nanomaterial properties is presented next. Dilute magnetic materials (DMS) as the building blocks of devices working on the principle of quantum electronics. The ZnO and Transition Metals doped ZnO nanostructures are discussed next towards the end of the chapter.

2.2. Moore's law

Moore's law is an empirical observation that feature size will be halved or component density and performance of integrated circuits doubles every year [1], this was later revised to doubling every two years [2]. Scaling rules were defined and put into practice shortly after development of IC's and for last 50 years, guided by these scaling laws [3], smart optimization by timely introduction of new processing techniques improving the weakest link present in the chain, device structures and materials (in many areas of the device except the channel), Moore's law has continued. Fabricated by lithography, the 65 nm logic technology node featuring ~30 nm transistors is currently in high volume production [4, 5], with 45 nm and 32 nm technologies with process targets defined to maintain Moore's law are currently under development.

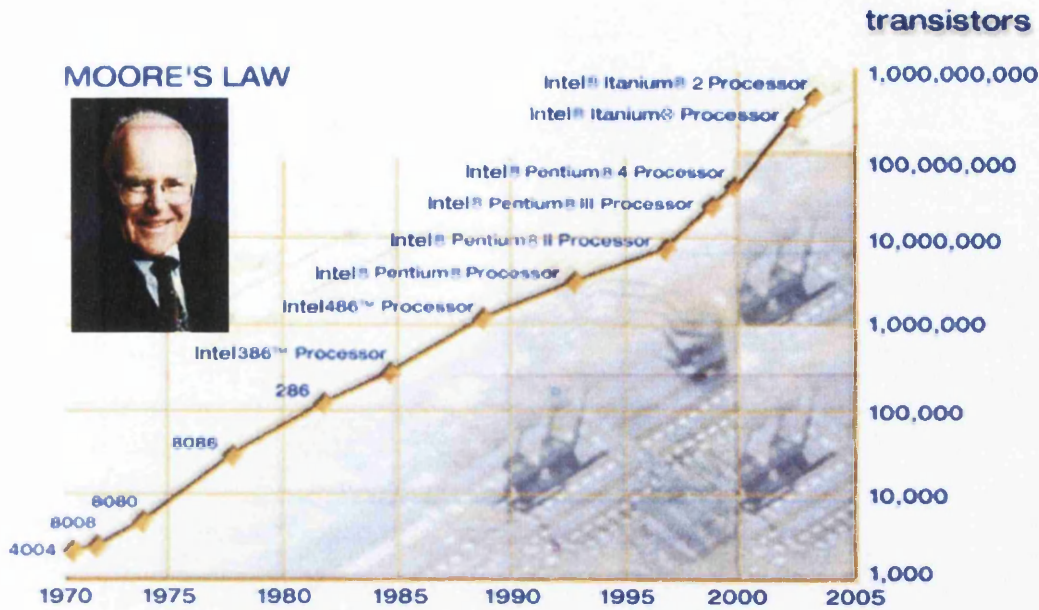


Figure 2.1: Number of transistors packed onto single chip – Moore's law [33].

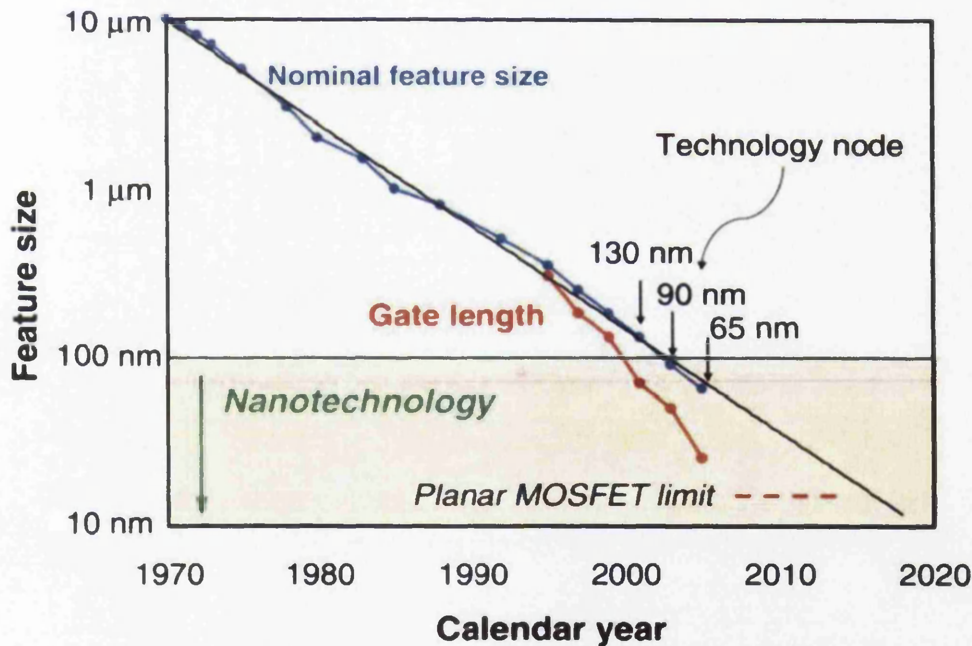


Figure 2.2: Reduction in feature size and technologies responsible for change [33].

Data presented in Figure 2.1 is in very good agreement with Moore's law, similarly in Figure 2.2 the feature size on a transistor has decreased as predicted by Moore. However there was another observation that is important for the technology to be successfully adapted is cost for the fabrication. From Figure 2.3 it is observed that

although overall fabrication for the device has increased over the years but the cost per transistor always decreases.

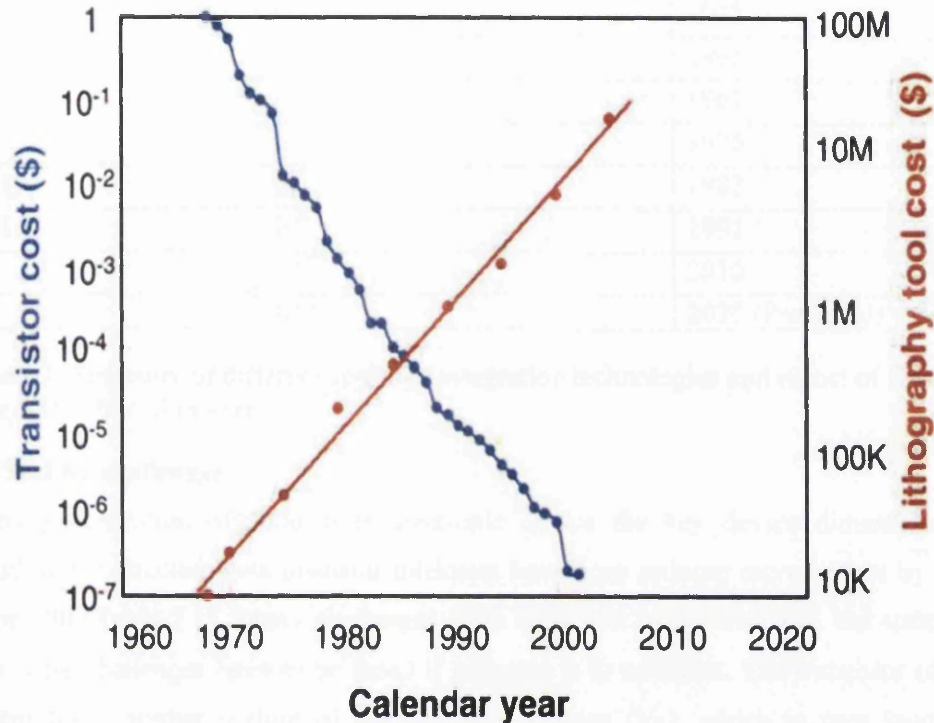


Figure 2.3: Change in overall process cost and cost per transistor [33].

From the development of first IC to the present date the IC's can be classified into seven categories/generations depending upon the component density packed per square centimetre and key break troughs achieved in fabrication process. These seven categories are, Small Scale Integration (SSI), Medium Scale Integration (MSI), Large Scale Integration (LSI), Very Large Scale Integration (VLSI), Ultra large Scale Integration (ULSI), Giga Scale Integration (GSI) and Atomic Scale Integration (ASI). Individual devices fabricated before the development of IC can be referred to as Zero Scale Integrated (ZSI) devices. Table 2.1 summarise these different technology with year they were first realized/fabricated.

As observed from Table 2.1 a revolutionizing growth is achieved consistently over the last 55 years in development of solid state device. However application/adaptation of the novice technology is mainly governed by the

commercial aspects of the devices. Even though the next generation of devices are fabricated in lab conditions they still may not be yet obsolete for commercial application.

Integration Class	Number of Components per cm^2	Year of Realization
ZSI	10^0	1955
SSI	10^1	1965
MSI	10^2	1967
LSI	10^4	1975
VLSI	10^6	1982
ULSI	10^8	1991
GSI	10^{10}	2010
ASI	10^{12}	2020 (Predicted)

Table 2.1: Summary of different scales of integration technologies and report of first successful fabrication year.

2.3. Scaling challenges

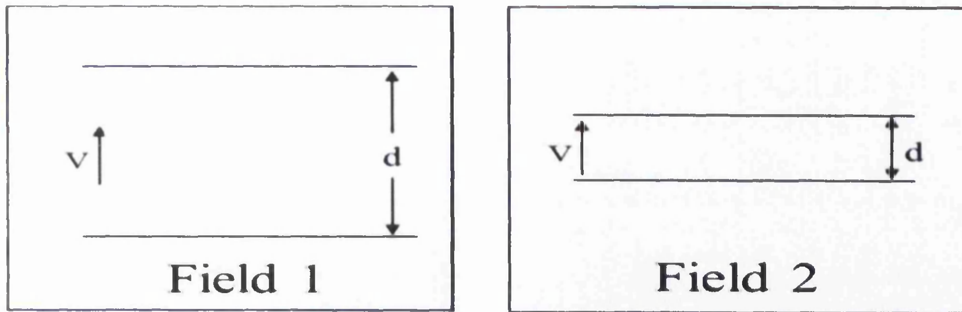
In every generation of solid state electronic device the key device dimensions including the effective gate insulator thickness have been reduced more or less by a factor 100 (Table 2.1). Many challenges have been met to achieve this, but today even more challenges have to be faced if progress is to continue. The transistor off current limits further scaling of the threshold voltage (V_T), which in turn limits scaling of the power supply voltage. Variability problems are increasing due to line edge control and roughness, doping fluctuations and soft errors. For the near term, strain engineering and hybrid surface orientation are being pursued to keep performance moving forward. Although several alternative structures are promising for the future, but they appear challenging to build. Some key scaling challenges faced today are discussed below.

2.3.1. Electric fields

As the induced electric field (E) between different layers of materials in a semiconductor device is proportional to the applied voltage (V) across the layers and the distance (d) that separates them.

$$E \propto \frac{V}{d}$$

Thickness of different layers of materials cannot be decreased beyond a certain limit otherwise a breakdown may occur due to presence of high field. As a result new metal materials will be needed in conjuction with high K dielectrics.



Field 2>>Field 1

Figure 2.4: Scaling effect of electric fields.

2.3.2. Heat dissipation

As the packing density of device increases, the heat dissipated per cm^2 also increases. This required to be properly scaled because with the present rate of heat dissipation the device with nanometer feature size would give off heat equivalent to gunpowder.

2.3.3. Device cross-talk

Separation distance between different devices on a chip is also a key parameter. As the size of barriers is scaled down to less than 50nm Quantum tunnelling causes the devices to function unpredictably which makes further scaling down of the devices impossible.

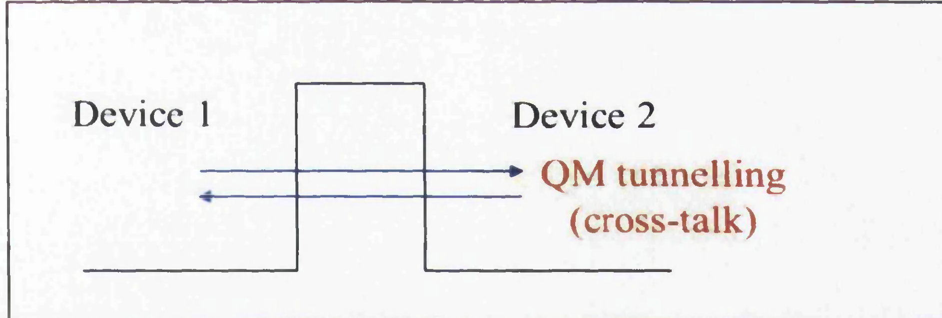


Figure 2.5: Device cross talk due to quantum tunnelling.

2.4. Next generation electronic devices

Spin electronics, also known as Spintronics, has the potential to create devices with superior performances due to the utilization of both the charge and spin degree of freedoms of electrons. On the bases of nature of material used to fabricate spintronics devices can be classified into the following categories:

(i) Metal-based

(ii) Dilute magnetic semiconductor based

(iii) Semiconductor based systems

(iv) Hybrid devices.

Further among different materials used in the fabrication of spinelectronics devices, the devices assembled from DMS based materials are most promising as they can integrate into the semiconductor technology and has the potential to operate at room temperature.

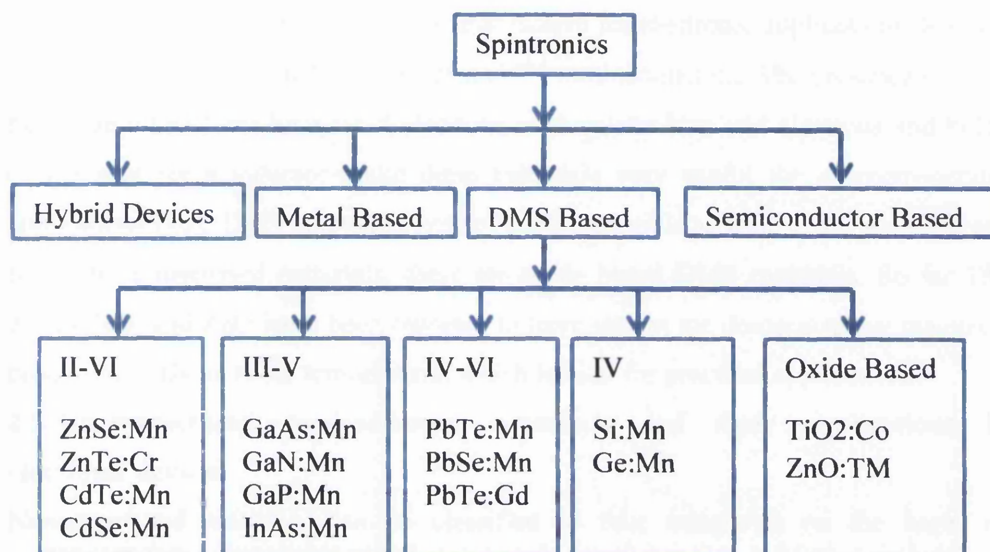


Figure 2.6: Classification of spintronics devices based on nature of material they been fabricated from.

Semiconducting and magnetic properties have been reported to coexist in some materials, like europium chalcogenides [6, 7] and ferrimagnetic or ferromagnetic semiconducting spinels [8]. Because of their novice properties in particular the properties resulting from the exchange interaction between itinerant electrons and localized magnetic spins, these materials have been extensively studied. These interactions give rise to a rich variety of novice optical and transport phenomena. These properties can be manipulated by magnetic field, however they are very sensitive to temperature and room temperature and existence of these properties is yet to be achieved. So far low Curie temperature (T_c) and difficulties in material preparation prevented them to be used as fundamental building material for electronic devices. But now with conventional electronic devices reaching to their peak, next generation of electronic devices is anticipated to be based upon these semiconductor materials with magnetic properties. These materials can be classified as concentrated semiconductor materials (CMS). In addition to these CMS, there is

also intensive researches on diluted magnetic semiconductors (DMS) which are obtained by doping them with a few percent of magnetic ions [9]. Initial work had been centred on II-VI semiconductors (A, X) B where A = Zn, Cd, Hg, X = Fe, Mn, Co, Ni, Cr and B = S, Se, Te, and in most cases the valence of group II cations is identical to that of most magnetic transition metals. Although these materials are relatively easy to prepare, most of them are random anti-ferromagnets or spin-glasses, which makes the II–VI DMS unattractive for electronic applications. Similar efforts are been made on III-V, IV-VI and IV semiconductors. The presence of sp-d exchange interactions between d electrons of magnetic ions and electrons and holes of the host semiconductor make these materials very useful for magneto-optical applications [10]. There is another type of DMS materials as well which are different from above discussed materials, these are oxide based DMS materials. So far TM doped TiO_2 and ZnO have been reported to have shown the demonstrating magnetic properties at above room temperature, which is vital for practical applications.

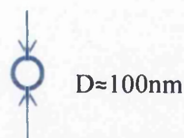
2.5. Nanostructured semiconductor materials and their applications in electronic devices

Nanostructured materials can be classified in four categories on the bases of dimensionality (Figure 2.7), namely 0-D clusters and particles, 1-D nanotubes and nanowires, 2-D nanoplates and layers/films and 3-D nanomaterials that involve 0-D,1-D or 2-D nanostructures such as fullerites, sols, colloids etc. [11, 12]. All of the dimensions of 0-D nanostructures are in the nanometric size range. The 1-D nanostructures have a dimension that is outside the nanometric size range. The 2-D nanostructures have two dimensions outside of the nanometric size range. The 3-D nanostructures have three dimensions outside of the nanometric size range. These bulk 3-D nanostructures consist of many various kinds themselves, and usually comprise nanocrystalline units that show the affected properties of nanoscale due to the size effect. In Figure 2.6 a schematic structural illustration of all four classes of nanostructures is presented. With a lot of research presently focused on nanostructures, these four classes of nanostructures are further sub divided into a total of 36 categories. These nanostructures differ from other in one way or the other and offer some novel properties. Electron confinement in nanostructures is considered to be the main reason for their different behaviour. Electron confinement in nanostructures particularly in thin films (0-D) and nanowires (1-D) is briefly discussed next.

0-D Nanostructures

-All three dimensions (x,y,z) at nanoscale.

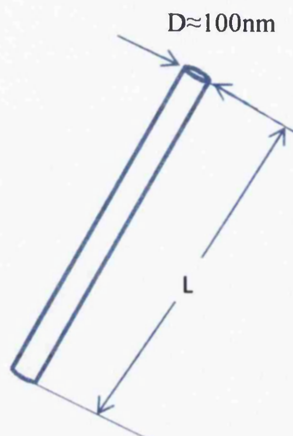
e.g. Molecules, Clusters, Fullerenes, Rings, Metacarbs, Thoroids, Domens, Nano powders/particles Schwartzons etc.



1-D Nanostructures

-Nanomaterials with two dimensions(x,y) in nanoscale and other (L) is not.

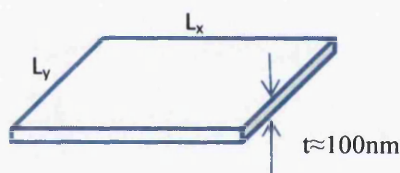
e.g. Nanotubes/Nanowires/Nanobelts, Filaments, Whiskers, Helicoids, needles etc.



2-D Nanostructures

-Nanomaterials with atleast one dimension (t) in nanoscale and other (L_x and L_y) are not.

e.g. Tiling, Mosaic, Layered Films



3-D Nanostructures

-Nanomaterials with all (L_x, L_y and L_z) dimensions not in nanoscale.

e.g. Fullerites, Clatherates, Composites etc

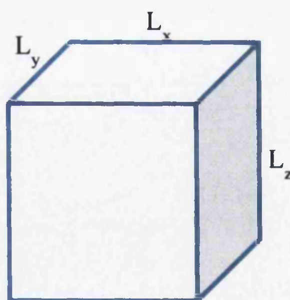


Figure 2.7: Classification of nanostructures according to their size.

2.6. Electron confinement in nanostructures - nanowires and thin films

Nanowires are 1-D nanostructures fabricated/synthesized from their respective bulk state by either bottom up or top down approach. Inorganic nanowires are nanostructures fabricated from inorganic materials and their typical growth methods are thermal, hydride vapour phase epitaxy, metal organic vapour phase epitaxy and

chemical vapour deposition, and growth mechanisms vapour-liquid- solid (VLS) and vapour solid (VS) methods.

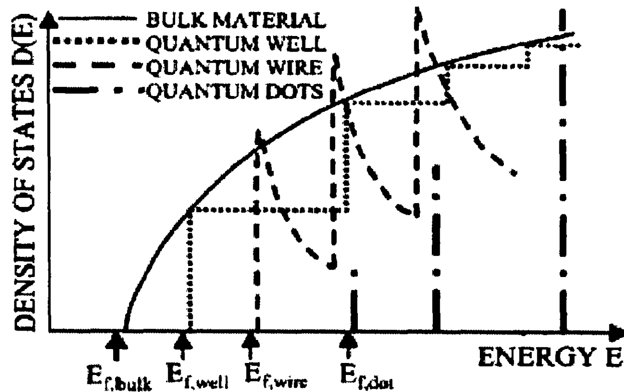


Figure 2.8: Schematic illustration of the density-of-states of electrons in bulk, quantum well, quantum wire, and quantum dots.

Nanowires use in integration of high-performance semiconductors in existing silicon technology is now well established [13].

Electrical transport measurements of such nanostructures are need to be investigated, because as the devices having dimensions comparable to the electron mean free path they tend to deviate from their bulk behaviour. Several test structures were created for a systematic study of their behaviour with respect to different key parameters such as film thickness, Cu concentration and wire length and width.

2.7. ZnO and ZnO nanostructures (thin films and nanowires) – importance and applications

Zinc oxide (ZnO) is a wide direct bandgap (3.2eV) semiconductor with a large exciton binding energy (60meV), which has potential applications in UV light emitters and detectors. Use of devices based upon ZnO has been investigated for use in short-wavelength light-emitting, transparent conducting and piezoelectric materials.

Recent years, there is an increasing interest in making ZnO a dilute magnetic semiconductor by doping it with transition metals (TM). As the valence of Zn in ZnO is +2, it can be easily replaced by TM ions, enabling interesting magnetic, optical and electrical properties. As compared to titanium dioxide (TiO_2), ZnO can accommodate more transition metal dopants while acting as a host material, making it a potential candidate for room temperature DMS. Theoretical models [14, 15] have predicted above room temperature Curie temperature (T_c) for TM doped ZnO thin films, following which has numerous experimental works in obtaining ZnO-based DMSs

using various approaches have been investigated. Most of the experimental work that has been reported to date is some sort of magnetic properties in TM doped ZnO (mostly Co and Mn), its origin still remains debatable and the phenomena being not fully understood. The magnetic properties reported so far for TM-doped ZnO range from intrinsic ferromagnetism with various T_c, [16-23] extrinsic ferromagnetism, [24-26] paramagnetism or super-paramagnetism [27, 28] to anti-ferromagnetism [29, 30].

Although the key device parameters in the electrical transport in a semiconductor, including resistivity, dynamic conductance, carrier concentration, magneto-resistance (MR), and Hall effect are temperature-dependent, yet studying their behaviour at the room temperature is of high importance. Conductance studies will enable better understanding of conduction mechanism in a material. The shape of a conductance curve is characteristic of the type of conduction. Transport measurements can determine the type of semiconductor of the films, carrier concentration of films and whether they are insulating in nature. Obtaining the carrier concentration is very important as it further determines if the material exhibits carrier-mediated ferromagnetism. Among all different types of potential DMS that have been investigated, oxide-based DMS systems have attracted special attention, in particular TiO_2 and ZnO based materials because of their attractive superior properties and a wide range of applications. In this work, the focus is on Cu doped ZnO DMS. Cu doped ZnO (ZnO:Cu), exhibits above-room-temperature ferromagnetism and can also be deposited on plastic substrates. On the basis of density functional calculations ZnO:Cu is predicted to be half metallic ferromagnate with 100% carrier polarization and a Curie temperature (T_C) of 380 K [31]. Because Cu has non-magnetic phases unlike other TM (Fe, Co, Ni, Mn), this makes Cu unique and important [32].

Compared to structural, chemical, optical and magnetic characterization, detailed study of electrical transport properties is still lacking. Electrical transport study is important in characterizing spintronic materials, in particular when the samples are inhomogeneous in nature. Inhomogeneity and disorder exist virtually in all types of materials. Most of the DMS can be considered in this regime because of the presence of precipitates of magnetic dopants, secondary phases, defects and random distribution of magnetic impurities. Inhomogeneity and disorder effect the transport and response of the system to external excitations such as electrical and magnetic field, light and thermal excitations. In the simplest transport measurement, one

measures the current-voltage (I-V) and other parameters can be derived from this I-V curve. In the case that the inhomogeneous region is much smaller than the specimen size, no noticeable effect originated from inhomogeneity will be observed in both the I-V and $dI - dV$ curves unless the density of inhomogeneity exceeds a certain percolation threshold. However, the situation will change when the samples are fabricated into one-dimensional nanowires. In this case, due to the geometrical confinement of current path, most of the electrons will have to encounter the inhomogeneous region before they could reach the other end of the sample. Depending on the nature of electrical conduction in both regions, one may observe I-V curves with different characteristics.

2.8. Summary

In this chapter an overview to electrical transport characterisation of ZnO and Cu-doped ZnO oxide systems through covering both the theoretical and experimental works. Although many factors may result in the scattered results, one of the factors is the lack of systematic study on a series of samples grown under same conditions. More attention should also be paid to the correlation of results obtained by different characterization techniques rather than focusing on one or two results. In the next chapter, the experimental details of this work including both the sample preparation and characterization will be covered.

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Chapter 3. METHODOLOGY AND APPLICATION

3.1. Introduction

In this chapter most common used techniques and approaches for resistivity measurement of semiconductors are discussed along with new improvised ways of modifying and applying these techniques for nanoscale devices. Correction factors that need to be considered also discussed. At the end of the chapter application of scanning electron microscopy in ensuring the device integrity of nanoscale systems fabricated for experiment is discussed. Electrical transport characterisation of a material is important for its use in solid state electronic devices. The determination of resistivity ρ of a semiconductor material plays an important role in design of a semiconductor device as several key device performance characteristics like heat dissipation [2, 3], cut-off voltage [3], feature size [4-6] etc., directly depends upon the resistivity. Although ρ can be carefully controlled during crystal growth, but it is not truly uniform in doped or non-epitaxially grown wafers. The resistivity of wafers epitaxially grown [7] and by other controlled methods like hydrothermal method [8, 9] is generally highly uniform [10]. So precise resistivity control is very important for the fabrication solid state devices because it's effect the behaviour/working of device by contributing to the device series resistance, capacitance, threshold voltage, hot carrier degradation of MOS devices, latch up of CMOS circuits, and other parameters.

3.2. Resistivity measurement

The resistivity ρ of a semiconductor material depends on the concentration of free electron n and concentration of hole densities p, and their respective mobilities μ_n and μ_p (i.e. μ_n electron mobility and μ_p hole mobility) [9].

Now if q is the charge then ρ of the semiconductor material can be expressed as

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \qquad 3.1$$

Thus if carrier densities and carrier mobilities are known or can be measured experimentally ρ can be calculated from the equation 3.1.

Further for intrinsic semiconductors at equilibrium $n = p = n_i$ and the expression for resistivity becomes

$$\rho_{intrinsic} \cong \frac{1}{qn_i(\mu_n + \mu_p)} \tag{3.2}$$

Although in case of extrinsic semiconductor materials in which the majority carrier density is much higher than the minority carrier density, it is generally sufficient to know the majority carrier density and the majority carrier mobility.

i.e. in case of n-type extrinsic semiconductors $n \gg p$ so the term $p\mu_p$ becomes negligible and resistivity of n-type extrinsic semiconductor materials can be approximated as

$$\rho_n \cong \frac{1}{q(n\mu_n)} \tag{3.3}$$

Similarly for p-type extrinsic semiconductors $p \gg n$ and the expression for approximate resistivity can be written as

$$\rho_p \cong \frac{1}{q(p\mu_p)} \tag{3.4}$$

The above equations are simple but the carrier densities and mobilities are generally not known and they cannot directly be obtained from experiments but this equation is important for theoretical considerations. So we have to look for alternative measurement methods to find out the resistivity.

3.3. Two point probe resistance measurement arrangement and its limitations

Two-point probe methods to measure the resistance is easiest to implement among the various methods to measure the resistance. But this method has many limitations and result obtained by this method contains higher percentage of error which not only makes interpretation of the measured data difficult but also put question marks over the credibility of the findings. The equivalent circuit of a typical two-point probe or two-contact arrangement is shown in the Figure. 3.1. Our aim is to determine the resistance of the device under test (DUT). Now if R_T is the total resistance of the circuit then by ohms law

$$R_T = \frac{V}{I} \tag{3.5}$$

From the equivalent circuit of the two point probe arrangement it is clear that R_T includes the wire and probe resistance R_w contact resistance R_{Contact} and the actual resistance of device under test R_{DUT}.

$$R_T = 2R_w + 2R_{\text{Contact}} + R_{DUT} \tag{3.6}$$

Now clearly from equation 3.5 and 3.6 it is not possible to calculate the required parameterR_{DUT}. This makes the scope of use of two point probe very limited and especially unsuitable for scientific purposes where high degree of accuracy is required.

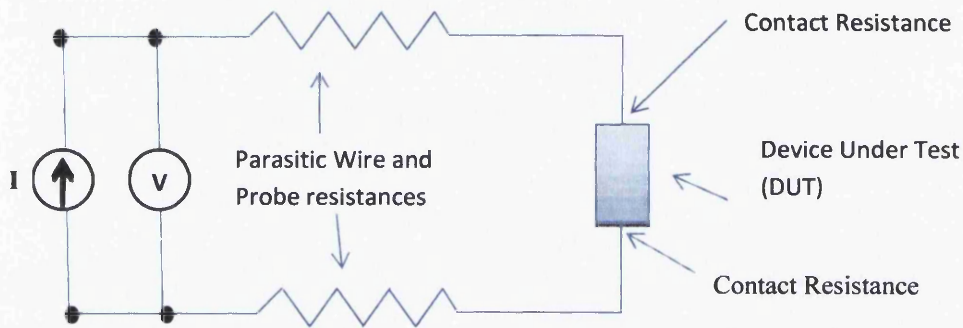

Figure 3.1: Equivalent circuit of two point probe resistance measurement arrangement

3.4. Parasitic resistances involved in electrical measurements

During the electrical characterisation of a device several unwanted resistances are also added to the measurements. These unwanted resistances are referred to as parasitic resistances. The parasitic resistances that could be involved in the experiments performed are discussed below.

3.4.1. Wire resistance (R_W)

A wire/cable carries the input signal from the source unit to the device under test through the probe and the output signal from the device to the measurement unit. Besides the resistance of the wire itself there are other unwanted noise signals in the circuit due called leakage currents. These are currents flowing through paths other than intended signal paths, such as current flowing through insulator materials that are part of interconnections. This leakage current can be a problem when the impedance of the device under test (DUT) is similar to that of the various insulators in the circuit or very precise measurement of resistance is required. The simple solution to this is to use a high quality cable with high resistance insulation such as teflon or polyethylene. Better quality cables often reduce the effects of dielectric absorption, which is typically a function of their high impedance insulation material. Although high quality cables can go a long way towards reducing leakage currents,

they may not always be sufficient. It's important to understand the nature of the leakage path in a shielded coaxial cable when it's used for the connection between a typical DC instrument, such as a source-measure unit (SMU), and the DUT. Leakage current flows from the centre of the conductor to the shield through the cable's insulation resistance. This causes the SMU to measure the sum of the current flowing through the DUT and the leakage current, rather than just the current flowing through the DUT.

A technique called guarding can eliminate the effects of leakage currents flowing through the insulation [11, 12]. A guard is a low-impedance point in the circuit that's at the same potential as the high-impedance lead in the circuit. In a guarded measurement, the shield is driven to the same potential as the Force Hi output terminal of the SMU using a unity-gain, low-impedance amplifier (guard). Therefore, no leakage current flows through the insulation resistance.

This technique requires a third (guard) connection on the instrument in addition to the usual cable shield and signal conductor. Although it's theoretically possible to use a guarded connection on a coaxial cable, it would be unsafe because the shield would be at the same potential as the Force Hi output terminal. The Guard of an SMU should never be connected to the shield of a coaxial cable. The correct solution is to use a tri-axial cable. Its inner shield is connected to the guard terminal of the instrument, and the outer shield is connected to the Force Low output terminal.

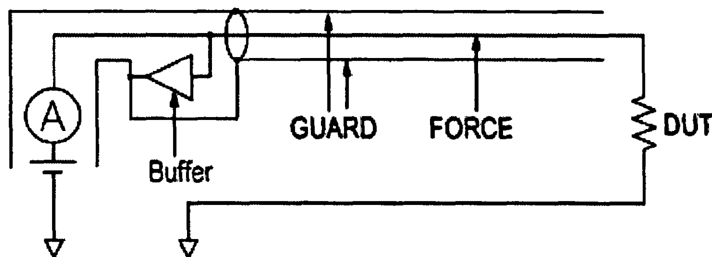

Figure 3.2: Schematic of a tri-axial cable.

A coaxial cable with its shield grounded at one point provides a substantial amount of protection from capacitive pickup. A double shielded or tri-axial cable with insulation between the two shields provides the maximum protection against noise coupling. Since the noise current flows through the outer shield and the signal return current flows through the inner shield, the two currents do not flow through common

impedance for noise coupling. Also length of cables used in the experiment must be short and stable for accurate measurement.

3.3.2. Probe resistance (R_p)

Probe resistance is the resistance of the probe itself that is used to in the experiment. Although the probe are made only from selective metals that reduces the probe resistance factor to a negligible amount but still during operation probe resistance can increase to a considerable amount due to the oxidation or accumulation of other impurities on the tip of the probe, regular cleaning or replacement of probes should be put into practice to lower the probe resistance. Probe resistance is considered single biggest factor that can adulterate the measurements and extra care should be made to limit it.

3.3.3. Contact resistance (R_C)

It is an empirical observation that access to a semiconductor region via a metal contact usually exhibits higher resistance than expected from an ideal contact. The additional resistance can be considered as a series resistor in the lead to the ideal contact. This extra resistance is called contact resistance (R_c). Fundamental assumption in contact theory is that, at some scale, the contact surfaces are never completely flat [1]. When two metallic conductors (e.g., a probe tip and aluminium contact pad) are pressed together, metal-to-metal contact is first made at various micro-protrusions across the surfaces (Figure 3.3).

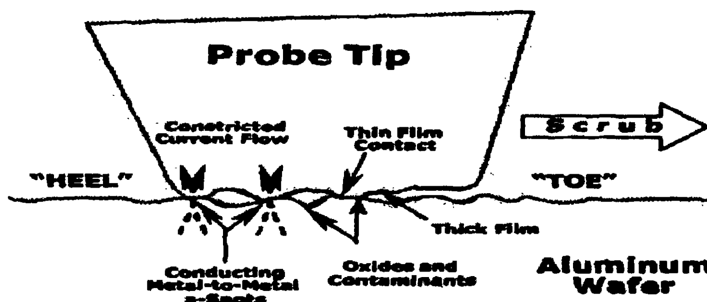

Figure 3.3: The contact interface between a probe tip and the contact pad of a DUT during measurements [1].

Initially, the metal-to-metal peaks deform elastically; however, as the overt ravel increases, the softer material deforms plastically until the entire contact force is supported [13]. The approximate size of these plastically deformed regions is directly proportional to the contact pressure and inversely proportional to the material hardness [14]. Consequently, the actual contact area of a probe needle is significantly

smaller than the total area of the probe tip. At full over travel the estimated maximum contact area is approximately 60-70% of the tip of the probe tip diameter (Figure 3.3) [15, 16].

The specific contact resistance at zero bias, R_c, serves as a measure of the ohmic or rectifying behaviour of a metal-semiconductor barrier under operating conditions.

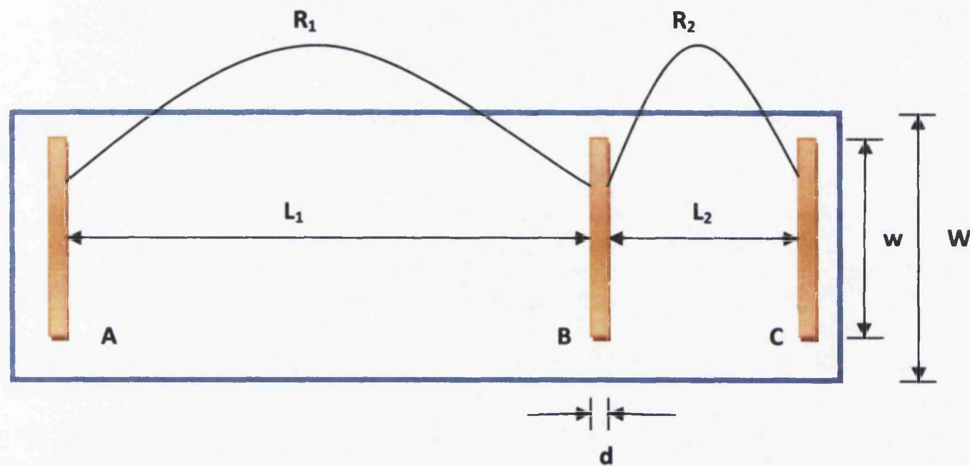

Figure 3.4: Origin and concept of contact resistance in metal semiconductor junction.

Consider a resistor having three equal contacts A, B and C arranged in different distances $l_1$and l_2 (Figure 3.4), it exhibits different resistances between A and B (R_1) and B and C (R_2). If l is the length between contacts A and B and W the width of the resistor, the resistance between contacts A and B (R_{AB}) is given by

$$R_{AB} = R_s \frac{l}{W} + 2R_c$$

Where R_c is the contact resistance, by applying above equation to R_1 and R_2 and solving for R_c results in

$$R_c = \frac{R_2 l_1 - R_1 l_2}{2(l_1 - l_2)} \qquad 3.7$$

.3.3.4. Spreading resistance (R_{SR})

The spreading resistance of contact (generally a round) on a semiconductor is an important quantity in many semiconductor device measurements and device design [9]. The current is concentrated at the probe tip and it spreads out radially from the tip. Figure 3.5 shows a schematic representation of probe touching the contact pad and spreading resistance.

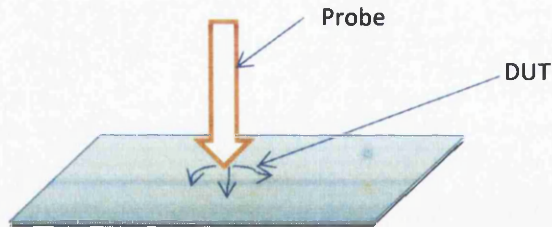

Figure 3.5: Concept of spreading resistance.

The commonly used formula for estimating the spreading resistance (R_{SR}) is given by following expression

$$R_{SR} = \frac{\rho}{2\pi a} \tan^{-1}\left(\frac{2b}{a}\right) \qquad 3.8$$

Where, b is the thickness and a is the contact radius of the probe.

Above expression is a well-known approximation derived from salt water tank measurements [11]. An attempted to find out an analytic expression for R_{SR} [12]; however, it was found out that in their paper they have made error while applying the boundary conditions.

These issues were overcome and not only an analytic expression for R_{SR} of very thin substrates but also a more general numerical solution. In brief the equation 3.5 is inaccurate for the range of the ratio of substrate thickness to contact radius 0.5 < b/a < 3 [17].

The thermal spreading resistance of a round heat conducting contact has the same mathematical form as the electrical problem. In a review of that work [18], the results are also limited to approximate analytic formula and numerical calculations.

3.5. Four point probe resistance measurement arrangement

To derive the four-point probe resistivity expression, we start with the sample geometry in Figure 3.7 (a). Consider a point P on a film of having infinite length. Let r be the distance of point P from the probe. The electric field E is related to the current density(J), the resistivity(ρ), and the voltage (V) through the relationship

$$E = J\rho = \frac{-dV}{dr} \qquad 3.9$$

Also

$$J = \frac{I}{2\pi r^2} \qquad 3.10$$

The voltage at point P at a distance r from the probe, is then

$$\int_0^v V = -\frac{I\rho}{2\pi}\int_0^r \frac{dr}{r^2} \tag{3.11}$$

$$V = \frac{I\rho}{2\pi r} \tag{3.12}$$

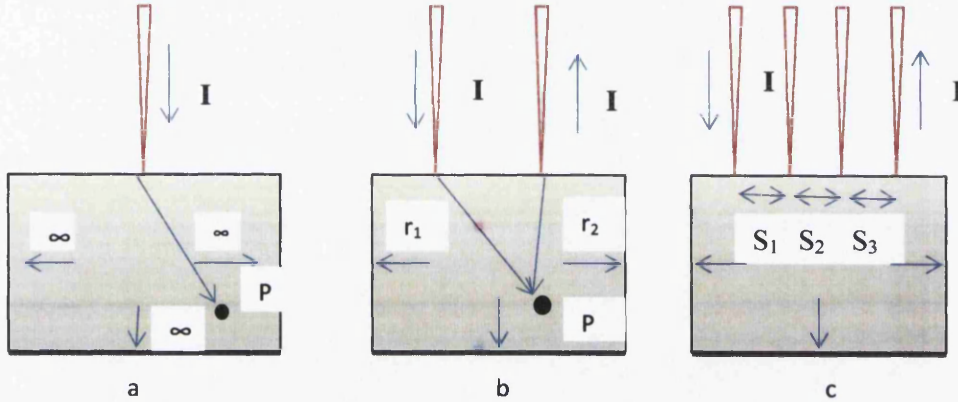

Figure 3.7: Mechanism current flow in (a) one-point probe, (b) two-point, and (c) collinear four-point probe.

For the configuration in Figure 3.7(b), the voltage is

$$V = \frac{I\rho}{2\pi r_1} - \frac{I\rho}{2\pi r_2} = \frac{I\rho}{2\pi}\left(\frac{1}{r_1} - \frac{1}{r_2}\right) \tag{3.13}$$

Where, r1 and r2 are the distances from probes 1 and 2, respectively. The minus sign accounts for current leaving through probe 2. For probe spacing's s1, s2, and s3, as in Figure 3.7 (c), the voltage at probe 2 is

$$V_2 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3}\right) \{\because here\ r_1 = s_1\ and\ r_2 = s_2 + s_3\} \tag{3.14}$$

and at probe 3 it is

$$V_3 = \frac{I\rho}{2\pi}\left(\frac{1}{s_1 + s_2} - \frac{1}{s_3}\right) \{\because here\ r_1 = s_1 + s_2\ and\ r_2 = s_3\} \tag{3.15}$$

The total measured voltage $V = V_2 - V_3$becomes

$$V = \frac{I\rho}{2\pi}\left(\frac{1}{s_1} - \frac{1}{s_2 + s_3} - \frac{1}{s_1 + s_2} + \frac{1}{s_3}\right) \tag{3.16}$$

The resistivity ρ is given by

$$\rho = \frac{2\pi}{(1/s_1 - 1/(s_1 + s_2) - 1/(s_2 + s_3) + 1/s_3)} \frac{V}{I} \qquad 3.17$$

$$s_1 = s_2 = s_3 = s \qquad 3.18$$

Usually, ρ *is* expressed in units of ohm cm with V measured in volts I in amperes and s in cm. Now if during the four-point probes the probe measurements spacing between the different probes is kept equal (i.e. s = s1 = s2 = s3), Equation (3.12) reduces to

$$\rho = 2\pi s \frac{V}{I} \qquad 3.19$$

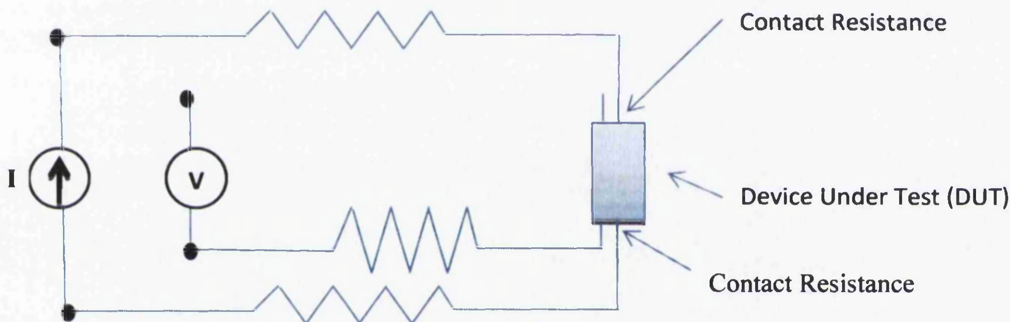

Figure 3.6: Equivalent circuit of four point probe resistance measurement arrangement.

Semiconductor wafers are not semi-infinite in extent in either the lateral or the vertical dimension and Equation (3.13) must be corrected for finite geometries. For an arbitrarily shaped sample the resistivity is given by

$$\rho = 2\pi s F \frac{V}{I} \qquad 3.20$$

Where, F corrects for probe location near sample edges, for sample thickness, sample diameter, probe placement, and sample temperature. It is usually a product of several independent correction factors. For samples thicker than the probe spacing, the simple, independent correction factors contained in F of Equation (3.14) are no longer adequate due to interactions between thickness and edge effects. Fortunately the samples are generally thinner than the probe spacing, and the correction factors can be independently calculated.

3.6. Correction factors

The Correction factor F in equation 3.19 is further subdivided into 3 independent correction factorsF_1, F_2 *and* F_3 .

$$F = F_1F_2F_3$$

Correction factor F_1accounts for the thickness of the sample, F_2 is for lateral dimensions of the sample and the final correction factor F_3 is introduced to account for the placement of probes on sample relative to the sample edges. Correction factor F_3 can be assumed as unity if the four point probe is performed by placing the probes near to the 10% region of centre. If probe spacing (s) is very small compared to the sample thickness(t), the correction factor (F) for thin film is given by [9],

$$F = \frac{t/s}{2\ln(2)}$$

Substituting this value of F in equation 3.20, the ρ can be expressed as

$$\rho = \frac{\pi}{\ln(2)} t \frac{V}{I}$$

For nanowires, if A is the area of cross-section and L is the length of nanowire

$$F = \frac{A}{L}$$

$$\rho = \frac{AR}{L}$$

3.7. Mutual trans-conductance (g_m), carrier mobility (μ) and carrier concentration (n) measurements

g_m, n *and* μ are most important parameters of an semiconductor. The device fabrication is directly dependent upon them. These factors can be indirectly controlled by extent of doping. Following equations represents their relations to fundamental quantities.

$$\mu = \frac{g_m L^2}{C V_{ds}} \quad 3.21$$

Where, g_m is the maximum transconductance that can be obtained from the slope of dI_D/dV_G of the I_D versus V_G plot, L is the length of the nanowire, C is the capacitance given by

$$C = \varepsilon_o \varepsilon_r \frac{A}{d} \quad 3.22$$

Where, $\varepsilon_o = 8.854 \times 10^{-12}$ Fm^{-1} is the vacuum permittivity and $\varepsilon_r = 8.91$ the permittivity of the ZnO nanowire, A is the area and d is the width of nanowire.

$$n = \frac{CV_{th}}{2\pi r^2 L} \qquad 3.23$$

Here V_{th} is the threshold voltage.

3.8. Scanning Electron Microscopy (SEM)

Unlike other electron microscopies SEM can be used to image and analysis of bulk specimens which made it suitable choice for use in the experiment for ensuring the integrity of the fabricated device. Electrons from a thermionic or field emission cathode are accelerated through a voltage difference between cathode and anode which can be easily controlled as desired in the wide range of 0.1-50KeV. Essential components of all SEMs include the following: Electron Source/Gun , Electron Lenses, Sample Stage, Detectors for all signals of interest, Display / Data output devices

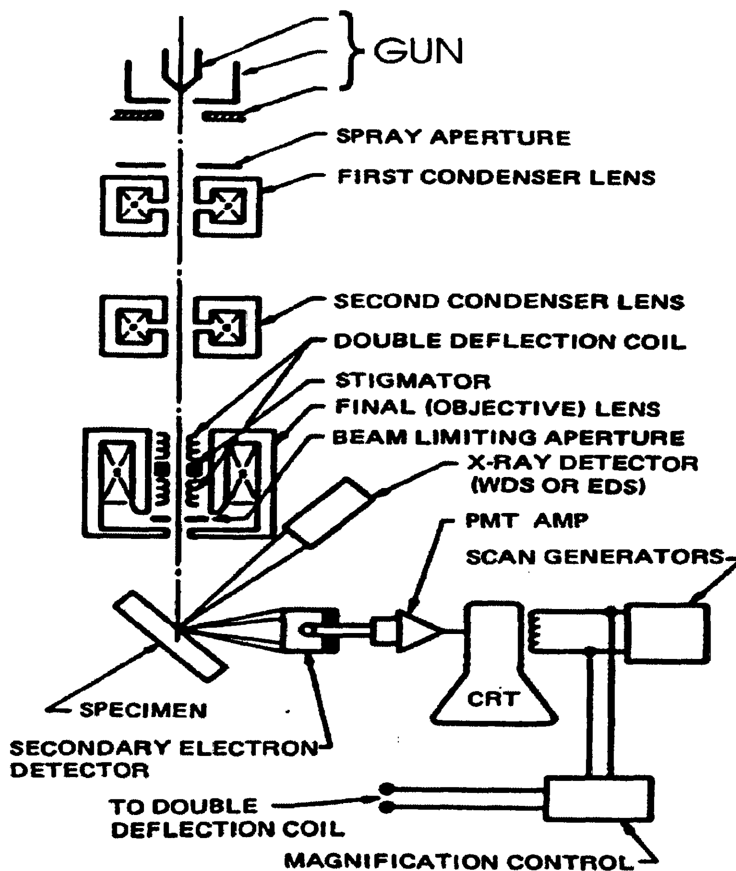

Figure 3.8: Schematic drawing of the electron and x ray optics of a combined SEM

3.9. Summary

From the above discussion following equation are summarized as they will be applied in Chapter 5.

Resistivity of thin film	$\rho = \frac{\pi}{\ln(2)} t \frac{V}{I} = 4.5323 t \frac{V}{I}$	3.24
Resistivity of nanowire	$\rho = \frac{AR}{L}$	3.25
Carrier mobility	$\mu = \frac{g_m L^2}{C V_{ds}}$	3.21
Carrier concentration	$n = \frac{C V_{th}}{2\pi r^2 L}$	3.23

3.10. References

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Chapter 4. EXPERIMENTAL SETUP

4.1. Introduction

In this chapter the details of the various experiments preformed will be discussed. First the sample preparation/fabrication of Cu doped thin films is discussed followed by their electrical measurements arrangement. ZnO nanowires growth and fabrication of four point contacts to the nanowire on a silicon wafer is discussed next. Then the four point probe measurements and trans-conductance characterisation process for the nanowires is presented in detail towards the end of the chapter.

4.2. Cu doped ZnO thin films deposition

Thin films are classified as two dimensional (2-D) nano structured devices based upon existence of electron confinement in them due to their shape and size [2]. The size of these nanowires is comparable to the order of mean free path of electrons in them, which gives rise to the quantum size effect and makes them exhibits different behaviour from the devices of same materials in their bulk/macroscopic sizes [3]. Thin film deposition is as extremely delicate process. Thin films used in these experiments were deposited using Filtered Cathodic Vacuum Arc (FCVA) technique [4, 5]. The whole process of thin film deposition is briefly presented in the following section.

4.2.1. Sample preparation - ZnO:Cu thin film deposition

The samples used for this study of electrical transport were prepared by a well-established technique of Filtered Cathodic Vacuum Arc [4, 5]. A schematic diagram of a FCVA is shown in Figure 4.1. During deposition/operation, a plasma beam with macro-particles and neutral atoms is emitted from the cathodic arc spot by a cathodic vacuum arc process. Unwanted macro-particles and neutrals are then be filtered out by a cross-magnetic and electric field. Only ions within a well-defined energy range are allowed to reach the substrate. Harder, denser and cleaner films can be produced by this technique which satisfies the general requirement for all applications - that the deposited films adhere well on a substrate and have good optical, chemical, electrical and mechanical properties that are predictable and reproducible.

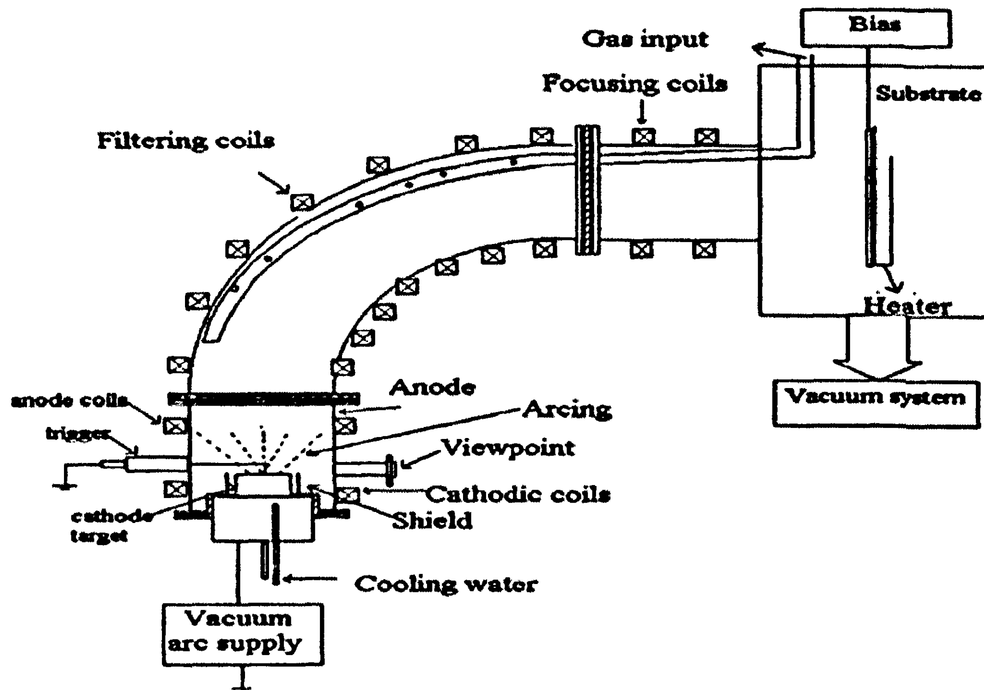


Figure 4.1: Schematic diagram of the Filtered Cathodic Vacuum Arc (FCVA) system for depositing thin films [1].

Heavily doped silicon was used as a substrate to deposit the thin films. A total of eight samples were prepared for the analysis. Five samples were prepared by using 1% Cu and three with 0.5 % Cu. Among the five samples that were prepared with 1% Cu three samples have uniform thin film thickness of 295nm and the remaining two have 177nm thick film.

Sample Number	Cu Target Used (%)	Film Thickness (nm)
S88-1	1%	295
S88-2	1%	295
S88-3	1%	295
S88-4	1%	177
S91-1	3%	270
S92-1	0.5%	178
S92-2	0.5%	100
S92-3	0.5%	100

Table 4.1: ZnO thin film samples, Cu % target used and film thickness.

The thin film thickness of 3 samples grown with 0.5% of Cu was 178 nm, 101 and 100nm. All samples were logically named for systematic study. Table 4.1 contains the summary of all thin film samples.

4.2.2 Post growth treatment of thin films

Sample S88-2 and S88-3 were both annealed at 400°C in the presence of oxygen and N_2O gas respectively. During the preparation of sample S92-2 N_2O gas was introduced. Sample S92-3 was annealed at 400°C in the presence of N_2O gas.

Sample Number	Film Thickness (nm)	Cu Target Used (%)	Special Treatment
S88-1	295	1%	As-grown
S88-2	295	1%	O_2 annealing at 400°C
S88-3	295	1%	N_2O annealing at 400°C
S88-4	177	1%	As-grown
S91-1	177	3%	As-grown
S92-1	178	0.5%	As-grown
S92-2	100	0.5%	Grown in N_2O environment
S92-3	100	0.5%	N_2O annealing at 400°C

Table 4.2: Special treatment performed on thin film samples.

4.2.2. Four point probe arrangement for thin films

As discussed in the Chapter 3 the probe positioning is important in order to accurately measure the resistivity of the film. The fabricated thin film sample was carefully placed on probe station, with the help of microscope mounted on the probe station probes were carefully lowered to touch the DUT. A schematic layout of the arrangement has been shown in Figure 4.2. After lowering the four probes precisely onto the desired locations on the thin film one by one, four point probe measurements were taken and this process is repeated for three times on three different areas on the thin film. Data is saved for further analysis and this process was repeated for all the eight thin film samples initially prepared.

An attempt was also made to carry out the trans-conductance measurements for thin films using back gate configuration, but very thin oxide layer between silicon wafer and ZnO thin film does not allow that because of too low breakdown voltage.

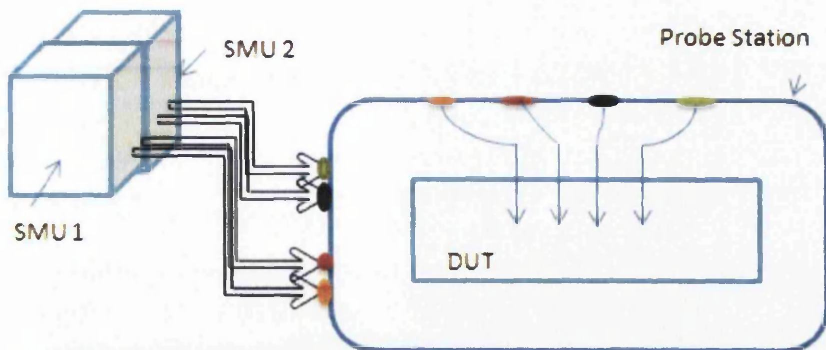


Figure 4.2: Schematic diagram for four point probe measurement arrangement for thin films (not drawn to scale).

4.3. ZnO nanowires growth and sample preparation for four point probe

Nanowires are basically one dimensional nanostructures fabricated/synthesized from their respective bulk state by either bottom up or top down approach. Inorganic nanowires are nanostructures fabricated from inorganic materials and their typical growth methods are thermal, hydride vapor phase epitaxy, metal organic vapor phase epitaxy and chemical vapor deposition, and growth mechanisms vapor-liquid-solid (VLS) and vapor solid (VS) methods [6]. Thin films are classified as one dimensional (1-D) [5] nano structured devices based upon existence of electron confinement in them due to their shape and size [2]. Their novice properties due electron confinement make them very important for research. A controlled growth of ZnO can be achieved by chemical deposition method (Figure 4.3). The growth process is highly sensitive to temperature and moisture content in the furnace, the furnace was turned on 30 minutes before the start of experiment to get rid of the any impurities present in the furnace. 0.3g of ZnO and C (graphite)[1] each were mixed together and transferred to an aluminium container open from the top, three 1cm^2 GaN wafers coated with 6nm of Au on were taken and marked as Sample A, B and C and placed in another aluminium container open from the top in way that each sample is 1cm apart from each other. First the aluminium container filled with ZnO and C mixture is placed in the furnace consulting the temperature chart of the furnace. Then the second aluminium container holding substrate is carefully placed in the furnace at exactly 7cm from the first container. Flushing[2] was performed at 200°C twice to remove the any impurities left in the furnace. Furnace was then filled

[1] Carbon is mixed with Zinc to lower its melting point. It is acting as a catalyst to lower the temperature.
[2] Flushing is the process followed to remove the any impurities present in the furnace by first creating a vacuum

with 98% Ar and 2% O_2 flowing at constant rate and temperature of the furnace is increased to 1000°C and kept there for 30 minutes and then allowed it to cool back to room temperature.

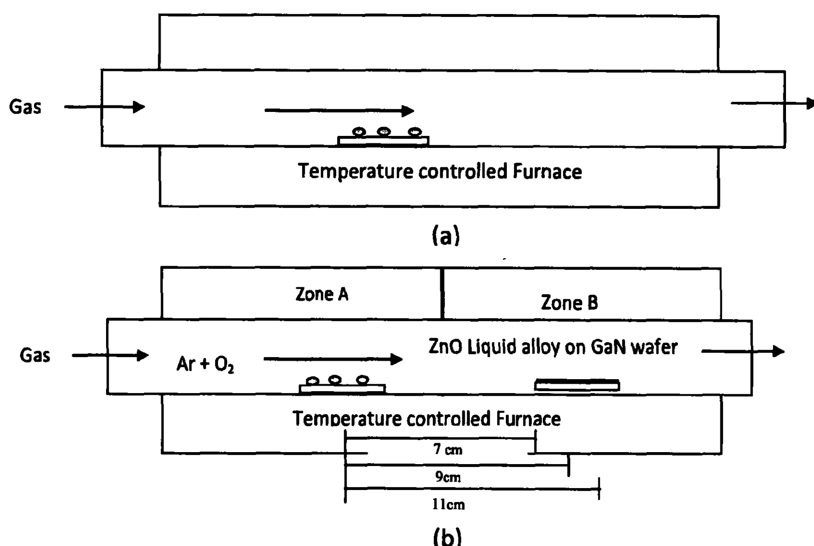


Figure 4.3 (a): Chemical Vapor Deposition (CVD) setup.
(b) Arrangement of samples and substrate in the experiment.

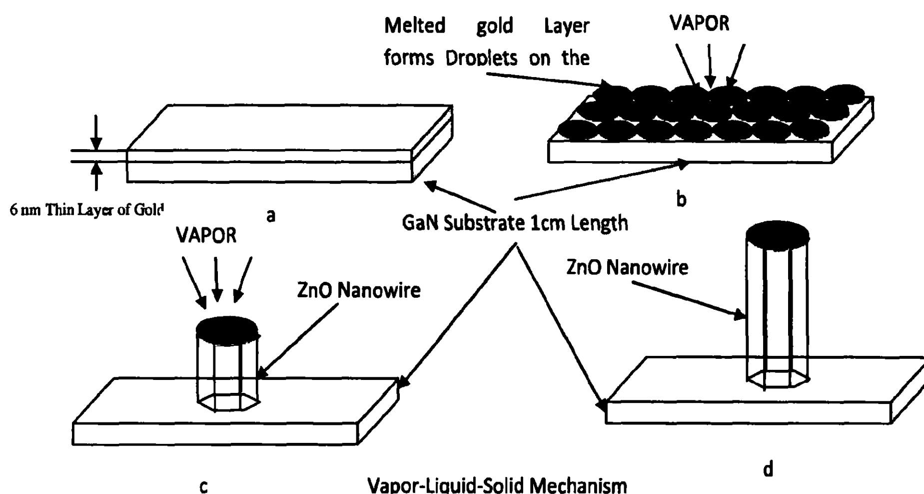
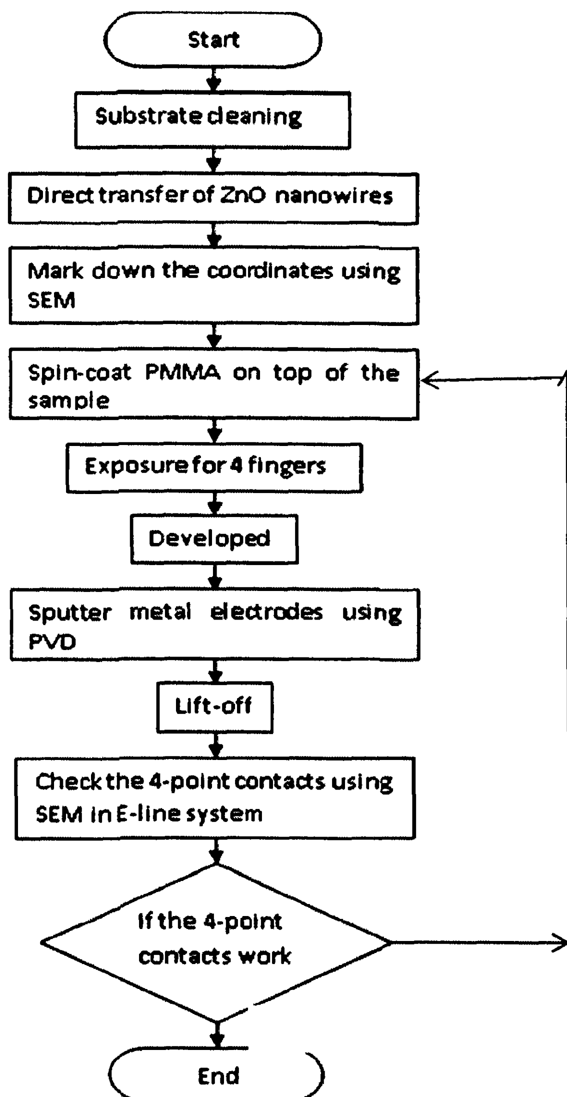


Figure 4.4 (a) GaN Substrate with 6 nm of thin gold layer at its surface, (b) As the temperature inside the furnace increases the top gold layer melts, forming small droplets on the surface of GaN (c) With time gold droplets acts as catalyst and speedup the process of ZnO settling onto the GaN (d) A grown ZnO nanowire.

Process of making contacts to the nanowire on the substrate starts with substrate cleaning using solvent cleaning technique of ultrasonic bath for 15 minutes in three

different solvents 1,1,1-Trichloroethane (TCA), acetone and Isopropanol (IPA). Substrate is then dried with nitrogen gas. ZnO nanowires are transferred direct on to the substrate after this.



Using the SEM in smaller aperture (10-20 μm) coordinates of desired nanowires are marked. Sample was then heated to 200°C for 1 minute followed by spin coating Polymethyl methacrylate (PMMA) at 2500 RPM for 30 seconds on the top of the sample. Exposure for the 4 finger contact to nanowire is then made with the help of scanning electron microscope (SEM) operating in small aperture mode. Samples

were dried before subjecting them to further PVD treatment for 5 minutes to sputter

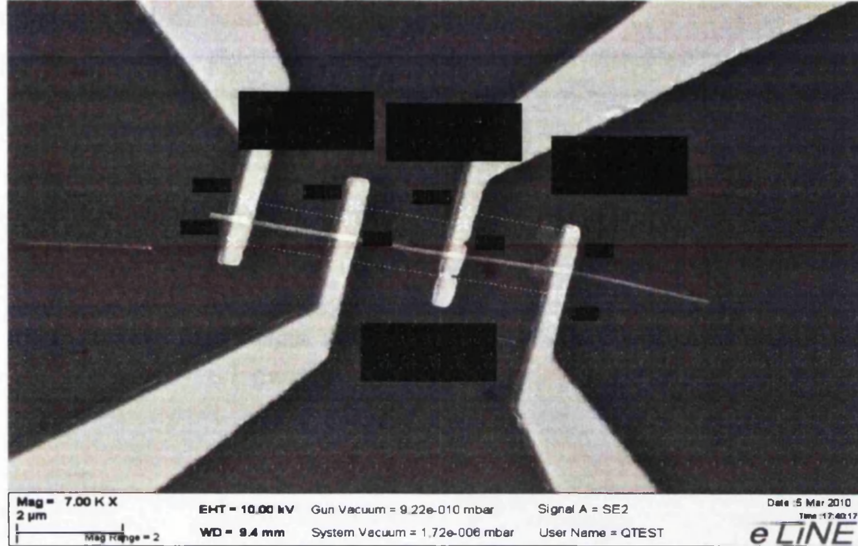


Figure 4.5: SEM Image of finalized device.

Au electrodes in the exposed area, which will result in formation of ohmic contact to the nanowire. Samples were then washed with acetone for 30 minutes or more till the patterns come out. Integrity checks for the device were performed next using SEM to make sure a reliable four point contact is established with the nanowire electrical measurements. A finalized device is shown in Figure 4.5.

4.4. Resistivity measurement arrangement for ZnO nanowires

As discussed in Chapter 3 a current is forced through the outer electrodes and voltage drop is measured at the inner electrodes of nanowire. A schematic sketch of four point probe resistivity measurement of a nanowire is shown in Figure 4.6.

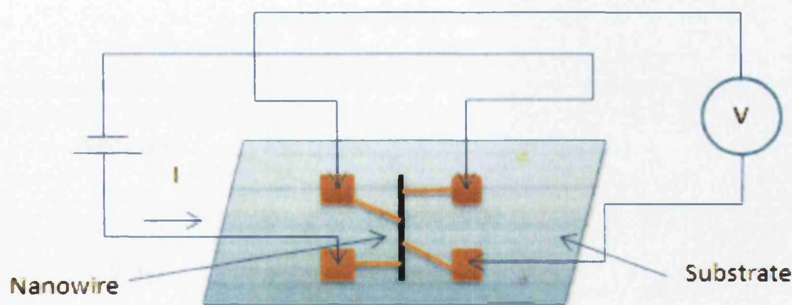
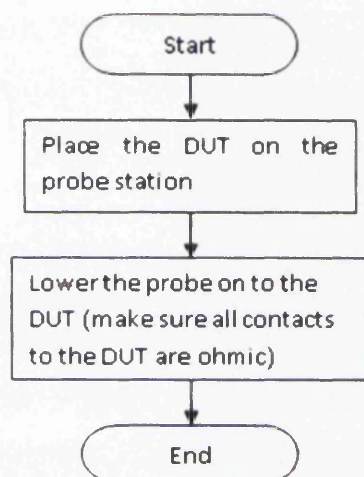


Figure 4.6: Four point probe arrangement for nanowires

It has already been proven in Chapter 3 that the resistance obtained by four point probe is very accurate and actual resistance of the nanowire channel, without any parasitic resistances. Flow chart 4.2 states the procedure followed during the resistivity measurement of nanowire.



4.5. Trans-conductance measurement arrangement for ZnO nanowires

Trans-conductance measurement is slightly more complicated than the above described method of four point probe for resistivity measure. The only difference here some gate bias (V_g) is applied. The schematic sketch of this arrangement is shown in Figure 2.7. Further V_g is varied and device characteristic were recorded and analysed. Detailed analysis is given in section Chapter 5.

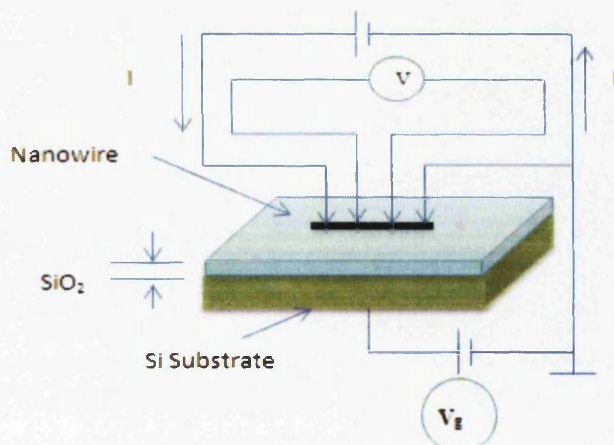


Figure 4.7: Trans-conductance measurement arrangement for nanowires

4.6. Summary

In this chapter the practical aspects of the project were presented. Precautions and good practice methods of performing the experiment were set and were followed throughout the experiment. While Cu doped thin films are easier to characterize when compared to resistivity measurement of nanowire. A lot of effort is required to first make the ohmic contacts to the nanowire and then extra care is to be taken while performing four point probe because a slight change can damage the device. In next chapter result obtained from these measurements are analysed.

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Chapter 5. RESULT AND DISCUSSION

5.1 Introduction

As discussed in Chapter 4, thin film samples used in this experiment had been fabricated using FCVA technique, so as to carry out systematic study of the electron transport properties of Cu-doped ZnO thin films. All the electrical transport measurements had been carried out at room temperature. The results of electrical transport properties of thin films will be presented first, followed by the discussion on improvement of transport properties and film stability by special post growth treatment of the thin films. Dependence of resistivity on film thickness, post growth treatment and Cu percentage will be discussed. Results obtained from resistivity and trans-conductance measurements of ZnO nanowires are presented and discussed in latter half of the chapter.

5.2 Electron transport study of ZnO:Cu thin films

As discussed in Chapter 4, eight different thin film samples were prepared for electrical measurements. The details of the samples and their post growth special treatment are summarised in Table 5.1. Each one of the eight thin film sample prepared for analysis were put to test one by one in the four point probe resistance masurement arrangement for thin films as described in Chapter 4.

Sample Number	Cu Target Used (%)	Film Thickness (nm)	Special Treatment
S88-1	1%	295	As-grown
S88-2	1%	295	O_2 annealing at 400°C
S88-3	1%	295	N_2O annealing at 400°C
S88-4	1%	177	As-grown
S91-1	3%	270	As-grown
S92-1	0.5%	178	As-grown
S92-2	0.5%	100	Grown in N_2O environment
S92-3	0.5%	100	N_2O annealing at 400°C

Table 5.1: ZnO thin film samples Cu % target used, film thickness and special treatment given to sample.

Figure 5.1 -5.8 shows the I-Vcurves plotted between the average of three measurements taken at three difrrenet points for each sample using four point probe measurement. Resistane was calculated form these plots by taking the average of all the measurements. Selective sampling was used while taking the average of resistance for sample S88-2 and S92-1 by not including values with noise in the average. Percentage uceratianty was calculated for eaach sample separetly usingthe expression

$$\text{Percentage uceratianty} = \frac{\textit{Stanadard Devivation}}{\textit{Average}} * 100$$

Uncertainity is found out to be under 2% for all the thinfilm samples except 14 % for S88-2 and 8% for S92-1. Using the measured resistance and percentage uncertainty, resistivity is calculated using the equation 3.24. The summary of resistivity calculated for all samples is presented in Table 5.2. Comparsion are drawn with respect to film thickness, special post growth treatment given to the sample and percentage of Cu target used during the growth of the thin film.

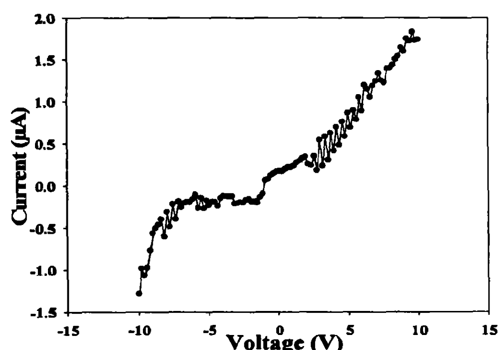

Figure 5.1. Electron transport measurement of sample S88-1(Cu doped ZnO as-grown thin film of thickness 295 nm).

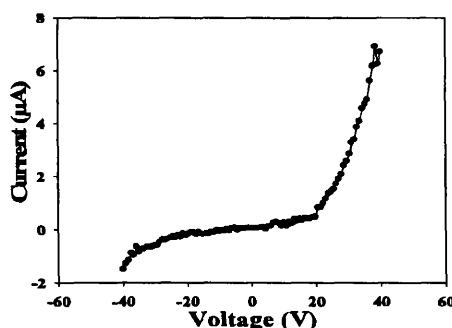

Figure 5.2: Electron transport measurement of sample S88-2 (Cu doped ZnO thin film annealed in O_2 at 400°C and of thickness 295 nm).

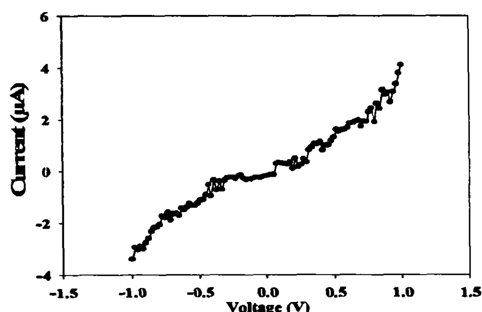

Figure 5.3. Electron transport measurement of sample S88-3 (Cu doped ZnO thin film annealed in N_2O environment annealed at 400°C and of thickness 295 nm).

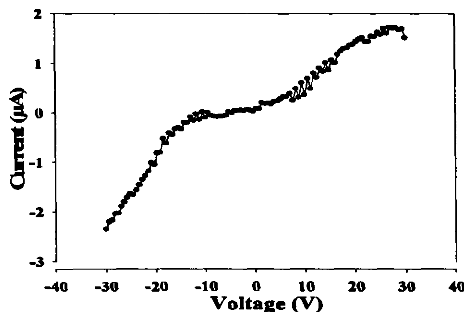

Figure 5.4: Electron transport measurement of sample S88-4 (Cu doped ZnO thin film of thickness 177nm).

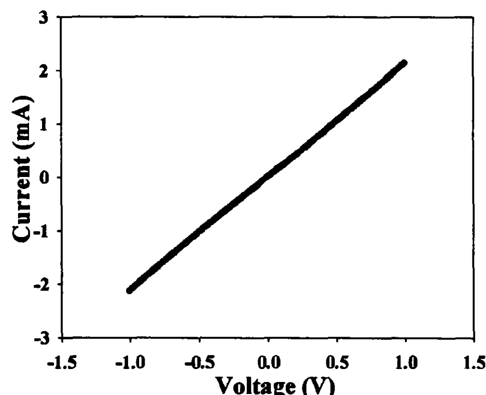

Figure 5.5: Electron transport measurement of sample S91-1 (Cu doped ZnO as-grown thin film of thickness 295 nm).

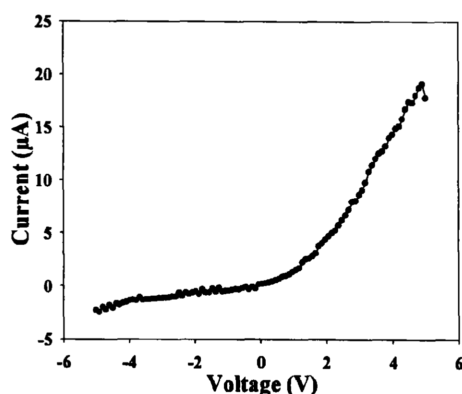

Figure 5.6: Electron transport measurement of sample S92-1 (Cu doped ZnO as-grown thin film with thickness 100nm).

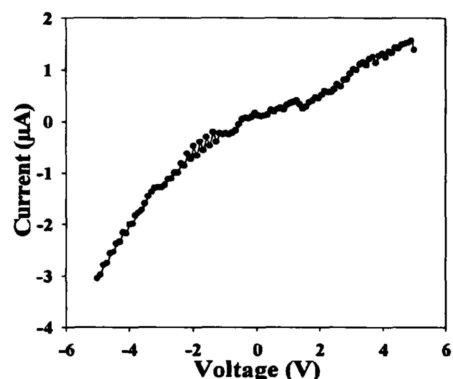

Figure 5.7: Electron transport measurement of sample S92-2 (Cu doped ZnO thin film of thickness 101nm grown in the presence of N_2O).

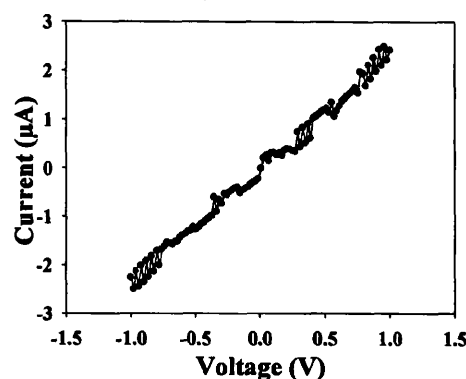

Figure 5.8: Electron transport measurement of sample S92-3 (Cu doped ZnO thin film of thickness 100nm grown in the presence of N_2O gas and annealed at 400°C).

Sample Number	Cu Target Used (%)	Film Thickness (nm)	Resistance (Ohm)	Resistivity Ohm cm
S88-1	1%	295	1.24×10^7	1.05×10^3
S88-2	1%	295	3.32×10^7	3.38×10^3
S88-3	1%	295	4.20×10^5	5.22×10^1
S88-4	1%	177	1.43×10^7	1.15×10^3
S91-1	3%	177	4.77×10^3	3.83×10^{-1}
S92-1	0.5%	178	1.52×10^6	8.25×10^3
S92-2	0.5%	100	2.96×10^6	1.35×10^2
S92-3	0.5%	100	4.47×10^5	2.02×10^1

Table 5.2: Summary of measured resistivity of all thin film samples.

5.2.1. Effect of the post growth treatment on the thin film resistivity

For post growth treatment studies lets first consider samples S88-1, S88-2 and S88-3.

Sample Number	Cu Target Used (%)	Film Thickness (nm)	Special Treatment	Resistivity Ohm cm
S88-1	1%	295	As-grown	1.05×10^3
S88-2	1%	295	O_2 annealing at 400°C	3.38×10^3
S88-3	1%	295	N_2O annealing at 400°C	5.22×10^1

Table 5.3. Resistivity of the samples S88-1, S88-2 and S88-3

For all these samples 1 % Cu target was used during the film deposition and all three samples have same film thickness of 295nm. First sample S88-1 is without any post growth treatment (Figure 5.1), the resistivity of the thin film comes out to be 1.05 $K\Omega cm$. For sample S88-2 which was anealed in the presence of O_2 at 400°C. The resistivity of the thin film measured to be 3.379 $K\Omega cm$, which increases three times in magnitude to that of as-grown sample S88-1. Sample S88-3 was annealed in the presence of N_2O enviornment at 400°C . The resistvity of this sample (Figure 5.3) is found out to be 52.15 Ωcm, which is decreased 100 times in magnitude to that of as-grown S88-1 sample. In Figure 5.9 resistivities of samples S88-1, S88-2 and S88-3 are plotted.

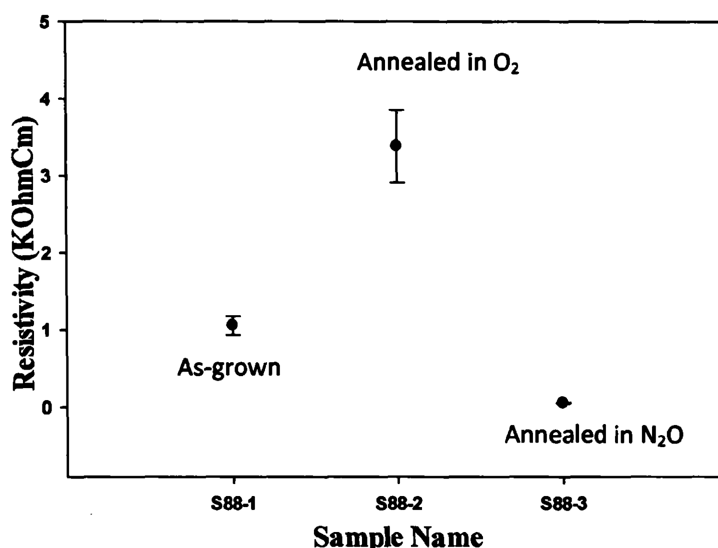

Figure 5.9: Resistivity of the as-grown, annealed in the presence of O_2 and annealed in the presence of N_2O thin films.

The resistivity of thin film after annealing in the presence of O_2 increase due to the chemisorption of O_2 in the interstitial sites and conversion of mono and trioxide to more stable dioxide state. This increase the percentage of O_2 in the thin film which is an electron acceptor and hence results in increased resistivity of the thin film. Annealing in the presence of N_2O enhanced the film stability considerably. The resistivity after the treatment process was found out to be approximately 100 times lesser than the resistivity of as-grown thin film of same thickness. But as discussed earlier annealing in the presence of O_2 alone resulted in threefold increase in the resistivity. This confirms that the decrease in thin film resistivity in the case of annealing in the presence of N_2O was perhaps due to N-Zn bonding, as the bond length on N-Zn bond is more than that of Zn-O bond [1, 2]. Similar trend is also observed in another set of samples S92-2 and S92-3 (Table 5.4) both having same film thickness (100nm) and Cu % of 0.5.

Sample Number	Cu Target Used (%)	Thickness (nm)	Special Treatment	Resistivity Ohm cm
S92-2	0.5%	100	N_2O environment	1.35×10^2
S92-3	0.5%	100	N_2O annealing at 400°C	2.02×10^1

Table 5.4: Resistvity of the samples S92-2 and S92-3

5.2.2. Effect of the film thickness on the thin film resistivity

For the study film thickness on resistivity two samples S88-1 and S88-4 both having 1% Cu were considered. Following table summerizes the charactestic of both samples to be compared.

Sample Number	Cu Target Used (%)	Thickness (nm)	Special Treatment	Resistance (Ohm)	Resistivity Ohm cm
S88-1	1%	295	As-grown	1.24×10^7	1.05×10^3
S88-4	1%	177	As-grown	1.43×10^7	1.15×10^3

Table 5.5: Resistvity of the samples S88-1 and S88-4

The resistivity of the sample S88-4 is 1.05 $K\Omega cm$, comparing to sample S88-1 the resistivity of the film as predicticted by previous theoratical and experimental studies increased to 1.15 $K\Omega cm$ with the decrease in film thickness. Figure 5.10 presents the resistvity of both samples with respect to their thickness. This trend is observed in all measured samples. If we study the I-V curve (Figure 5.4) for the sample S88-4 it can be seen that the curve can be divided into two regions for applied potential less then

15 volt the film offers more resistance but beyond that an ohmic behaviour is observed.

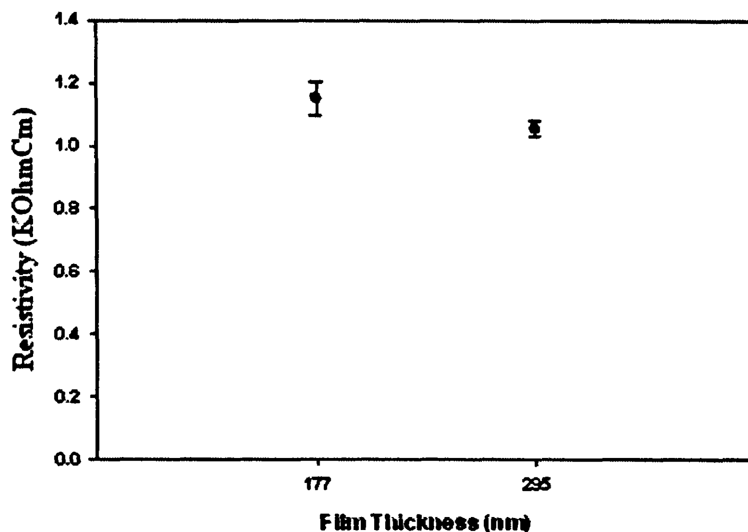

Figure 5.10: Resistivity vs thickness of ZnO thin films.

5.2.3 Effect of the Cu doping percentage on the resistivity of thin films

As discussed samples having 3 different percentages (0.5, 1 and 3%) of Cu target used during the film deposition were prepared. For the effect of Cu percentage on resistivity of thin film sample three samples S88-4, S91-1 and S92-1 having almost similar film thickness of 177 nm and all of these samples were not given any post growth treatment are considered. The measured resistivity of these samples is summarised in the following table for analysis.

Sample Number	Cu Target Used (%)	Film Thickness (nm)	Special Treatment	Resistivity Ohm cm
S92-1	0.5%	178	As-grown	
S88-4	1%	177	As-grown	
S91-1	3%	177	As-grown	

Table 5.6: Resistivity of the samples S92-1, S88-4 and S91-1.

From the measured data (Figure 5.11) it can be observed that the resistivity decreases exponentially with increase in Cu percentage. Cu has a work function of φ= 4.5 eV [10] and ZnO has a work function of φ = 5.4 eV [11], this results in lowering the fermi level of the system and hence conduction increases with that. Also increased percentage copper resulted in extra carriers available for the transport. The

exponetinal nature of the curve implies that resistivity of Cu doped thin films is very sensitive to the percentage of Cu present in them.

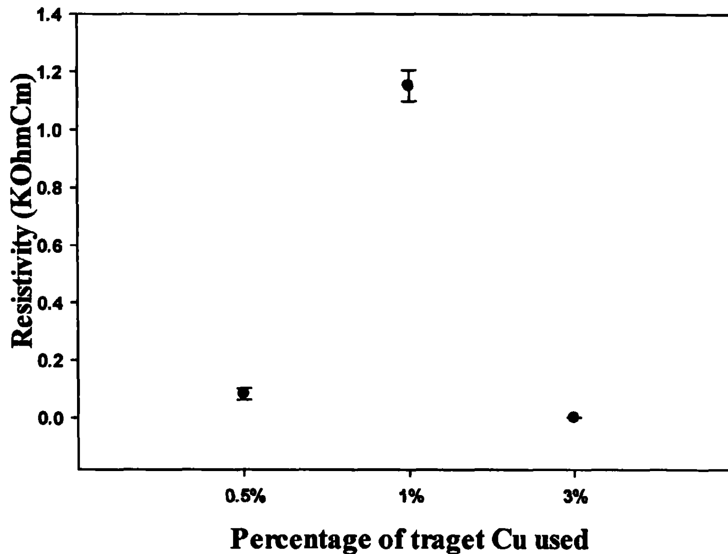

Figure 5.11: Resistivity vs percentage of target Cu used.

5.3 Electronic Transport Characterisation of ZnO Nanowires

For the systematic electron transport study of ZnO nanowires, eight devices of different nanowire length and width were fabricated in the process described in Chapter 4. SEM is performed on each of them to check the integrity of the device and measurement of length and width of nanowires.

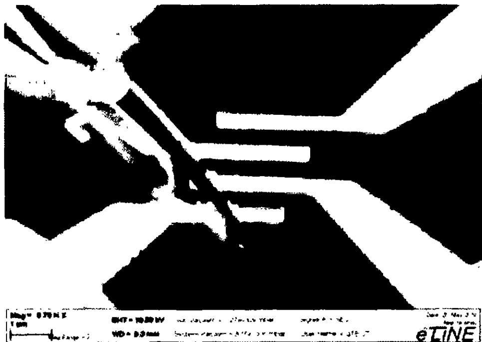

Figure 5.12: SEM image of the fabricated device using ZnO nanowire 1 (NW1)

Figure 5.13. SEM image of device fabricated with another nanowire 2 (NW2).

Figure 5.14: SEM image of the fabricated device using ZnO nanowire 3 (NW3).

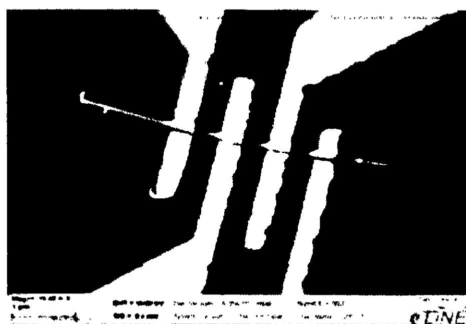

Figure 5.15: SEM image of the fabricated device using ZnO nanowire 4 (NW4).

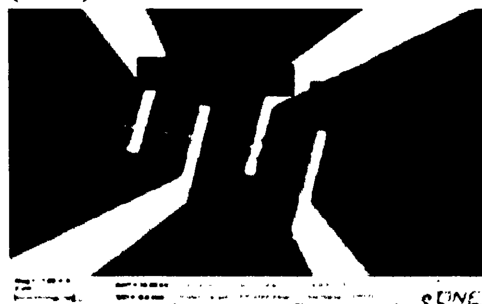

Figure 5.16: SEM image of the fabricated device using ZnO nanowire 5 (NW5).

Figure 5.17: SEM image of the fabricated device using ZnO nanowire 6 (NW6).

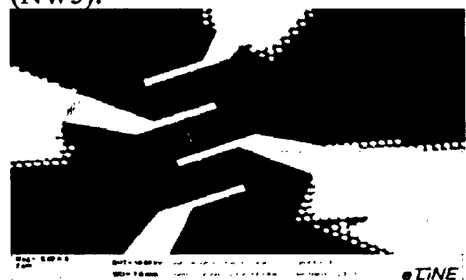

Figure 5.18: SEM image of the fabricated device using ZnO nanowire 7 (NW7).

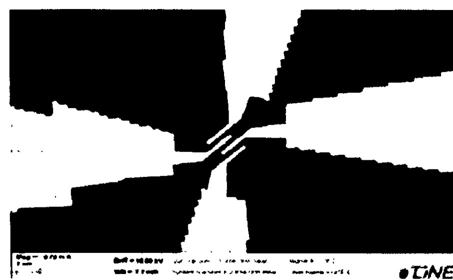

Figure 5.19: SEM image of the fabricated device using ZnO nanowire 8 (NW8).

From the SEM images of each sample and with the help of image processing software, the length and width of nanowires were measured and are summarized in Table 5.7. ZnO have hexagonal cross-sectional area (A). A schematic view of cross-sectional area of ZnO nanowire is shown in Figure 5.20. Cross-sectional area (A) can be calculated from the width (D) of the nanowire with the help of following equation,

$$A = \frac{3\sqrt{3}a^2}{2} = \frac{3\sqrt{3}D^2}{8} \qquad \left[\because a = \frac{D}{2}\right] \tag{5.1}$$

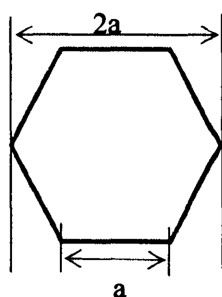

Figure 5.20: Schematic view of hexagonal cross-sectional area of ZnO nanowire.

By using equation 5.1 cross-sectional area of all nanowire samples were calculated and are summarised in following table:

Sample Number	Length (μm)	Width D (nm)	Cross-section area A (cm^2)
NW 1	0.3537	71.4	3.31×10^{-11}
NW 2	7.7010	133	1.15×10^{-10}
NW 3	3.0230	71.17	3.29×10^{-11}
NW4	0.3301	177.42	3.89×10^{-11}
NW 5	1.6143	85.45	4.74×10^{-11}
NW 6	0.8727	117.50	8.97×10^{-11}
NW 7	0.3569	91.29	5.41×10^{-11}
NW 8	1.9757	116.77	8.86×10^{-11}

Table 5.7: Summary of the cross-sectional area of nanowire samples

5.3.1. Resistivity measurements

Four point probe measurements were performed on each nanowire sample one by one in an arrangement described in Chapter 4. Four point probe data is collected and I-V curves are plotted (Figure 5.21-5.28). Resistance of each nanowire is obtained by taking average of all measured values and is for calculating the resistivity of each sample. Percentage uncertainty in measured resistance is under 1% for all samples.

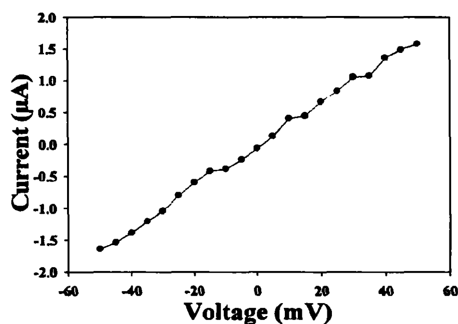

Figure 5.21: Electron transport measurement plot of ZnO nanowire

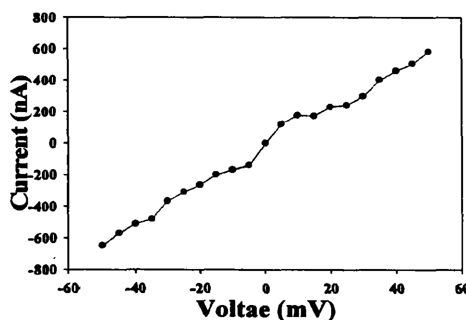

Figure 5.22: Electron transport measurement plot of ZnO nanowire

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(NW1) having length 35.37 µm and width 71.4 nm.

(NW2) having length 7.70 µm and width 133 nm.

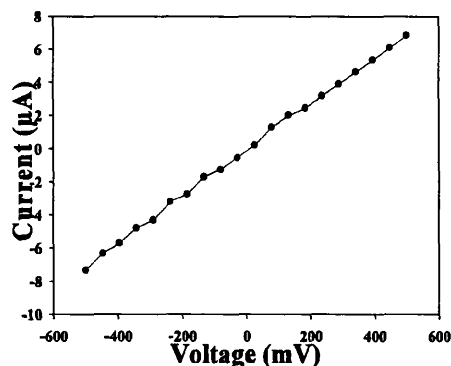

Figure 5.23: Electron transport measurement plot of ZnO nanowire (NW3) having length 3.02 µm and width 71.17 nm.

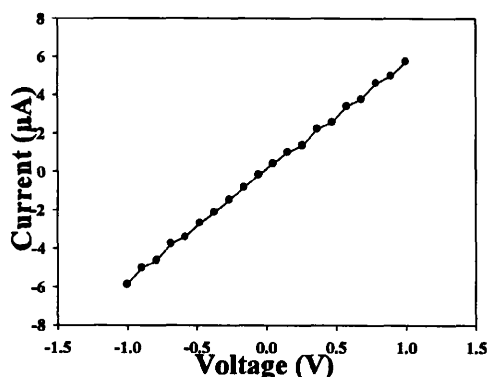

Figure 5.24: Electron transport measurement plot of ZnO nanowire (NW4) having length 0.3301 µm and width 177.42 nm.

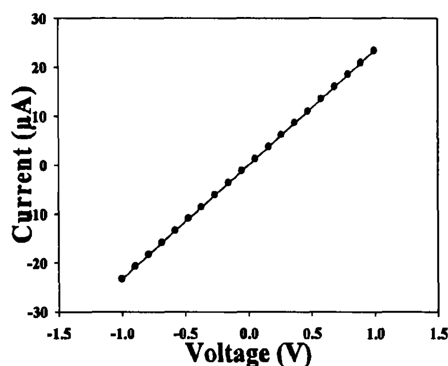

Figure 5.25: Electron transport measurement plot of ZnO nanowire (NW5) having length 1.61 µm and width 85.46 nm.

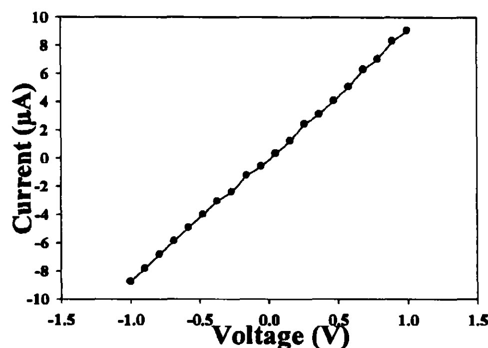

Figure 5.26: Electron transport measurement plot of ZnO nanowire (NW6) having length 0.8727 µm and width 117.5 nm.

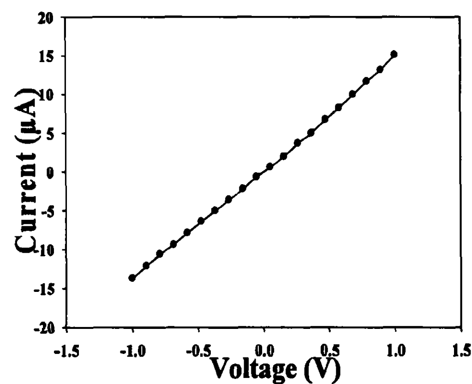

Figure 5.27: Electron transport measurement plot of ZnO nanowire

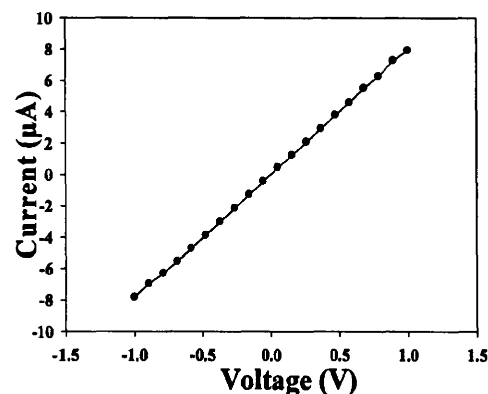

Figure 5.28: Electron transport measurement plot of ZnO nanowire

(NW7) having length 35.69 μm and width 91.29 nm.

(NW8) having length 1.97 μm and width 116.77 nm.

Resistivity (ρ) of a nanowire can be calculated with the help of equation 3.25

$$\rho = \frac{AR}{L}\Omega\text{m}$$

For first nanowires sample named NW1

$$\rho = \frac{3.311 \times 10^{-11} \times 30.8 \times 10^{3}}{0.3537 \times 10^{-4}} \cong 2.83 \times 10^{-4}\,\Omega\text{cm}$$

Also, conductivity (σ) is given by

$$\sigma = \frac{1}{\rho} \cong 6.2613 \times 10^{4}\mho m^{-1}$$

Similarly resistivity for the rest of the nanowire sample was also calculated and is presented in following table.

Sample Number	Length (μm)	Width (nm)	R ($K\Omega$)	ρ (Ωcm)
NW 1	0.3537	71.4	30.1	2.83×10^{-2}
NW 2	7.7010	133	82.4	1.23×10^{-2}
NW 3	3.0230	71.17	38.98	4.24×10^{-2}
NW4	0.3301	177.42	175.62	2.07×10^{-1}
NW 5	1.6143	85.45	42.92	1.13×10^{-2}
NW 6	0.8727	117.50	115.97	1.19×10^{-1}
NW 7	0.3569	91.29	72.59	1.10×10^{-1}
NW 8	1.9757	116.77	124.37	5.58×10^{-2}

Table 5.8: Summary of the resistance and resistivity of nanowire samples.

Resistivity measured here will be used in determining the other key parameters such as carrier concentration and carrier mobility in the following section of trans-conductance measurements.

5.3.2 Trans-conductance measurements

Trans-conductance measurements were performed for six samples NW3-NW8. Each of the six devices was placed in trans-conductance measurement arrangement as described in Chapter 4 one by one and data is collected for analysis.

Carrier concentration n can be calculated using the equation 3.23 from Chapter 3.

Figure 5.29 shows the trans-conductance plot for nanowire 1. From the tans-conductance plot n-type nature of ZnO is observed and the value of V_{th} can be determined and hence the carrier concentration(n).

$$n = \frac{CV_{th}}{2\pi r^2 L}$$

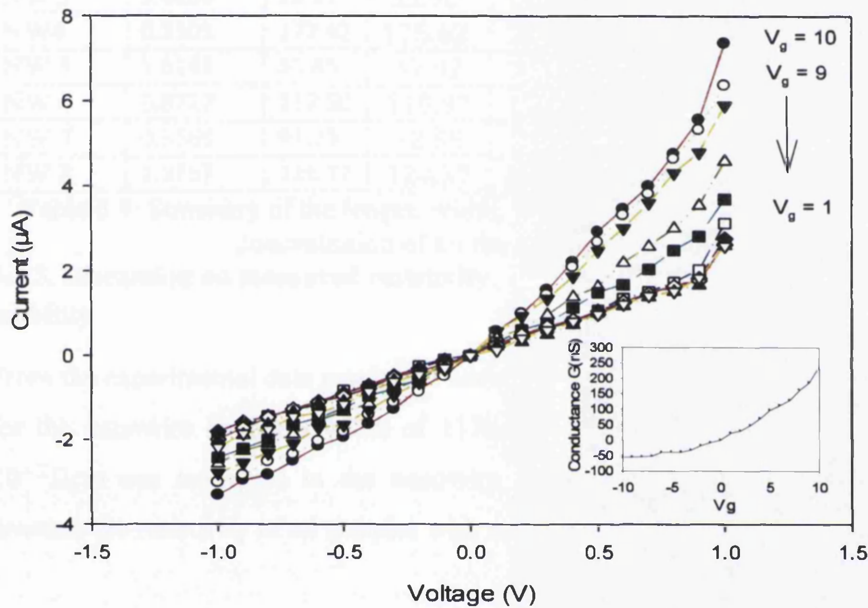

Figure 5.29: Electron transport measurement of a single ZnO nanowire (NW1). (a) I-V curves taken at different gate voltages, Vg. The most conductive I-V curve was from Vg =10. Each curve below is taken at different gate voltage with 1V interval. Inset: Conductance (G) vs V_g plot for the same device.

Similarly, as discussed in Chapter 3 carrier mobility (μ) can be calculated from equation 3.21

$$\mu = \frac{g_m L^2}{CV_{ds}}$$

Where, g_m is the maximum transconductance can be obtained from the slope (dI_d/dV_g) of the $I_d$versus V_g plot, L is the length of the nanowire, C is the capacitance given by

$$C = \frac{2\pi\varepsilon_o\varepsilon_r L}{ln(2h/r)}$$

Where, $\varepsilon_0 = 8.854 \times 10^{-10}$ Fcm^{-1} is the vacuum permittivity and $\varepsilon_r = 8.91$ the permittivity of the ZnO nanowire.

The calculated values of μ and n for all the samples are presented in the following table

Sample Number	Length (µm)	Width (nm)	R ($K\Omega$)	ρ (Ωcm)	n (cm^{-3})	μ (cm^2/V s)
NW 1	0.3537	71.4	30.1	2.83×10^{-2}	-	-
NW 2	7.7010	133	82.4	1.23×10^{-2}	-	-
NW 3	3.0230	71.17	38.98	4.24×10^{-2}	7.49×10^{18}	19.7
NW4	0.3301	177.42	175.62	2.07×10^{-1}	3.77×10^{19}	8.01
NW 5	1.6143	85.45	42.92	1.13×10^{-2}	4.13×10^{18}	13.4
NW 6	0.8727	117.50	115.97	1.19×10^{-1}	8.28×10^{17}	63.4
NW 7	0.3569	91.29	72.59	1.10×10^{-1}	5.66×10^{17}	100
NW 8	1.9757	116.77	124.37	5.58×10^{-2}	1.93×10^{18}	58

Table 5.9: Summary of the length, width, resistivity, carrier mobility and carrier concentration of all the nanowires samples.

5.3.3. Discussion on measured resistivity, carrier concentration and carrier mobility

From the experimental data maximum resistivity of $1.19 \times 10^{-1}\Omega cm$ was observed for the nanowire having a width of 117nm while minimum resistivity of $1.13 \times 10^{-2}\Omega cm$ was measured in the nanowire having a width of 85nm. Figure 5.30 presents the resistivity of all samples with respect to their width.

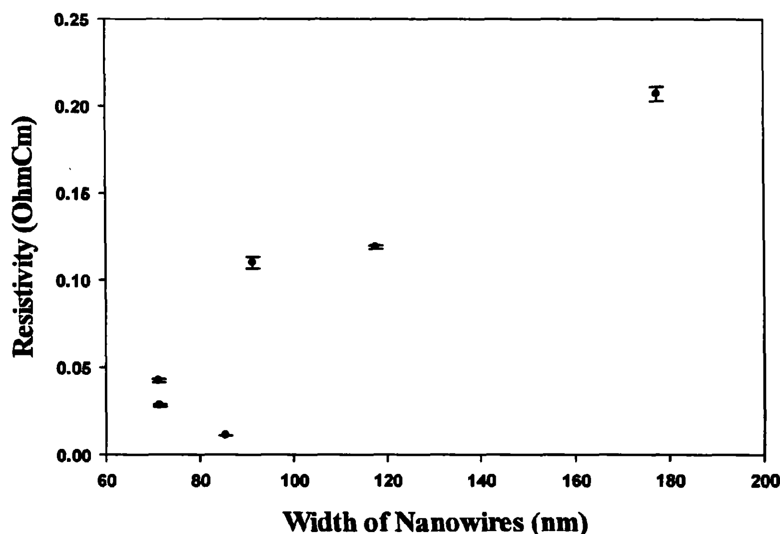

Figure 5.30: Resistivity versus width of nanowire.

Among all the nanowires studied of different width in the range of 70 to 180 nm it was observed that 90-100nm is the critical width, above or below which the behaviour of ZnO nanowires changes significantly. Nanowires with width less than 90 nm have lower resistivity than the ones with width more than 90 nm. Some researchers considered that the electric conduction mechanism in the ZnO nanowires is dominated by the defects at the surface of the single ZnO nanowire [3-5]. With decrease in the width of nanowire below 90nm the surface vacancies reduces, which results in reduced inelastic scattering events and this increases the electron mean free path. This decreases the resistivity of the ZnO nanowires. From the conductance versus gate voltage (V_g) plot, n-type nature of ZnO nanowires is observed. The carrier mobility for the ZnO nanowires was found out to be between 8 and 100 cm^2/Vs and the carrier concentration is in the range of $5.66 \times 10^{17}$to $3.77 \times 10^{19} cm^{-3}$. This is in good agreement with other results reported in this area of research [9].

5.4 Summary

The electron transport measurements were successfully performed on sixteen different samples, eight of which were thin film samples and remaining eight were nanowire based samples. It was observed that resistivity of the ZnO thin films can be reduced by heat treatment in the presence of N_2O. Also it was concluded that this change in resistivity is due to N-Zn bonds as the heat treatment of thin film in the presence of O_2 alone resulted in increase in resistivity. The resistivity of thin films was observed to be inversely proportional to the film thickness as with decrease in film thickness the resistivity increased. Resistivity of thin films was found exponential dependent on the percentage of Cu used during the film deposition. Resistivity and trans-conductance measurements were performed on a total eight different nanowire fabricated devices. Maximum resistivity of $1.19 \times 10^{-1} \Omega cm$ was measured for the nanowire having a width of 117nm while minimum resistivity of $1.13 \times 10^{-2} \Omega cm$ was found to be in the nanowire having a width of 85 nm. The carrier mobility for the ZnO nanowires was found out to be between $8\ to\ 100\ cm^2/Vs$ and carrier concentration in the range of $5.66 \times 10^{17} to\ 3.77 \times 10^{19}\ cm^{-3}$.

5.5. References

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Chapter 6. Summary and Conclusions

6.1. Introduction

A systematic study of electrical properties was carried out for both thin films and nanowires of ZnO and results were interpreted in the previous chapters. In this chapter the conclusions of this work are drawn and a future scope in this area is also discussed at the end.

6.2. Cu doped ZnO thin films study

Resistivity of the as grown Cu doped ZnO thin films was found out to be of the order of $10^3\ \Omega cm$ with $1.15\ K\Omega cm$ as the maximum value. It was also observed that the resistivity of thin films is inversely proportional to the film thickness.

6.2.1. Resistivity dependence on post growth treatment of thin films

The resistivity after the post growth treatment in the presence of N_2O was found out to be $5.22 \times 10^1\ \Omega cm$ which is approximately 100 times lesser than the resistivity of as grown thin film of same thickness. Further annealing in the presence of O_2 alone increased the resistivity to double the measured value of as grown film resistivity of same thickness. This is because O_2 is an electron acceptor and higher percentage of O_2 results in lesser number of free carriers available or transport and hence increased resistivity of the thin film. This confirms that the increase of film stability in case of annealing in the presence of N_2O was because of N-Zn bonding and not because of O_2 as the treatment of thin films in the presence of O_2 alone results in increase in resistivity.

6.2.2. Resistivity dependence on thickness of thin films

For the Cu doped thin films of different thickness in the range of 100-300 nm it was observed that the resistivity of ZnO thin films is inversely proportional to the film thickness (Figure 5.9). The resistivity of the sample S88-4 is $1.05\ K\Omega cm$, comparing to sample S88-1 the resistivity of the film as predicticted by previous theoratical and experimental studies increased to $1.15\ K\Omega cm$ with the decrease in film thickness. This trend is observed in all measured samples. Minimum value of $2.02 \times$

$10^1 ohm\ cm$ for the film off 100 nm thickness and maximum value of 5.22×10^1 ohm cm for the film of 300 nm thickness was measured.

6.2.3. Resistivity dependence on percentage of copper used during deposition

As discussed samples having 3 different percentages (0.5, 1 and 3%) of Cu target used during the film deposition were prepared and analysed. An exponential dependence on Cu percentage was observed. As the resistivity of Cu doped ZnO thin films is very sensitive to the presence of Cu content in them, this can be used to effectively control the resistivity of the thin films.

6.3. ZnO nanowires study

Ohmic contact to a single nanowire was successfully made and four point probe measurements were performed to measure their resistivity. To draw comparison nanowires of different width were used in different devices, from the experimental data maximum resistivity of $1.19 \times 10^{-1}\Omega cm$ was observed for the nanowire having a width of 117nm while minimum resistivity of $1.13 \times 10^{-2}\Omega cm$ was found to be in the nanowire having a width of 85nm. It was observed that with decrease in the width of nanowire beyond 90nm, the resistivity decreases because of the decrease in surface vacancies, which result in reduced inelastic scattering due events and electron mean free path increases. From the conductance versus V_g plot, n-type nature of ZnO nanowires is observed. The maximum carrier concentration for the ZnO nanowires was found out to be $3.77 \times 10^{19}\ cm^{-3}$ and a maximum carrier mobility of $100\ cm^2/Vs$ was determined, which are in good agreement with results reported by other researchers.

6.4. Future work

The results presented in this work shows a trend that ZnO based nanostructures will exhibit. ZnO nanostructures applications can find application in both information and healthcare.