Investigation of wafer processing technologies for the production of low-cost, improved efficiency Si PV cells.

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Investigation of wafer processing technologies for the production of low-cost, improved efficiency Si PV cells

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Abstract

Over the last five years, a dramatic expansion of renewable energy from Photovoltaic (PV) solar cells has been witnessed. This expansion is due in part to wafer based silicon solar cells. Crystalline silicon solar cells currently dominate the PV market because of their low cost per watt of electricity production. In order for silicon solar cells to continue to govern the market, efficiency improvements and cost reductions must be made.

This work focuses on both cost reduction and efficiency improvements, for wafer based silicon solar cells. The main aim of the work was to produce a thin monocrystalline wafer based silicon solar cell. A large proportion of the cost of conventional monocrystalline solar cells is related to the use of high purity silicon substrates. By producing a cell that uses less silicon, significant cost savings can be made. Conventional wafering techniques used in industry are reaching their limit for thin wafer production. The method adopted in this work uses a simple silicon exfoliation technique capable of producing ultrathin silicon foils. A fully operational solar cell was fabricated from a 40μm exfoliated silicon foil. The thin wafer based silicon solar cell was more than four times thinner than a commercially produced equivalent. The work investigated a variety of principles related to the exfoliation and the suitability of the technique for thin photovoltaic devices.

By using a thin exfoliated substrate, conventional anti-reflective (AR) suppressing processes could prove problematic. Experiments were conducted into finding an alternative technique to match the performance of the conventional AR process. The formation of porous silicon (PSi) on the surface of a silicon substrate was found not only to match the commercial process, but to exceed it. With a porous silicon layer, reflectivity was suppressed to just 6.68%. The technique could be applied to both thin silicon solar cells and conventional thicker wafer based cells. The reflectivity suppressive layer could be fabricated in a single simple processing step.

Investigation was also focused upon the top contact for silicon solar cells. As the top of the cell is responsible for current collection and light absorption, large electrical contacts shade the cell resulting in a decrease in efficiency. Silver nanowires (AgNWs) were successfully analysed and deposited onto standard silicon solar cell top contacts as an enhancement coating. Such a coating was found to improve the collection ability of the top contact without causing a significant increase in shading loss. The use of an optimised AgNW coating can increase cell efficiency by as much as 37%.

DECLARATION

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

Signed .... (candidate)

Date ..... 04/06/14 .....

STATEMENT 1

This thesis is the result of my own investigations, except where otherwise stated.
Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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STATEMENT 2

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List of Abbreviations

AC	Alternating Current
ARC	Anti Reflective Coating
a-Si	Amorphous Silicon
BJ	Back Junction
BSF	Back Surface Field
Cds	Cadmium Sulphide
CdTe	Cadmium Telluride
CIGS	Copper Indium Gallium Selenide
CPV	Concentrated Photovoltaics
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DLD	Dynamic Liquid Drop
DSSC	Dye-Sensitised Solar Cells
EBL	Electron Beam Lithography
EDX	Energy-Dispersive X-ray
ELTRAN	Epitaxial Layer TRANsfer
EWT	Emitter Wrap Through
FiT	Feed in Tariff
HIT	Heterojunction with Intrinsic Thin layer
ITO	Indium Tin Oxide
LGBG	Laser Grooved Buried Grid
LPCVD	Low Pressures Chemical Vapour Deposition
MAE	Metal Assisted Etching
MWT	Metal Wrap Through
NIL	Nanoimprint Lithography
OPV	Organic Photovoltaics
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapour Deposition
PERC	Passivated Emitter and Rear Cell
PERL	Passivated Emitter Rear Locally-diffused
PESC	Passivated Emitter Solar Cell
PSi	Porous Silicon
PV	Photovoltaic
PVD	Physical Vapour Deposition
SCIL	Substrate Conformal Imprint Lithography
SEM	Scanning Electron Microscopy
SLIM	Stress induced Liftoff Method
SOM	Silicon On Metal
SRH	Shockley-Read-Hall
TCE	Transparent Conducting Electrodes
TF	Thin Film
TIPT	Thermal-stress Induced Pattern Transfer
VEST	Via hole Etching for the Separation of Thin films

List of Symbols

FF	Fill Factor
G	Generation rate
I_{MP}	Current at the measured maximum power
I_{sc}	Short Circuit Current
L_n	Electron diffusion length
L_p	Hole diffusion length
η	Efficiency
V_{MP}	Voltage at the measured maximum power
V_{oc}	Open Circuit Voltage
I_L	Light generated current
I_o	Saturation current
J_L	Light generated current density
J_o	Saturation current density
Pin	Power input
$Pmax$	Maximum power
n	Refractive index
n_{ARC}	Refractive index of the ARC layer
q	Absolute value of electron charge

Chapter 1: Introduction to Photovoltaics

1.1 Introduction

This chapter discusses the essential need for renewable energy sources in order to start replacing conventional fossil fuelled and nuclear power stations. Renewable energy technologies will be briefly reviewed and advantages given for the use of photovoltaic (PV) solar cells. In particular the different generations of solar cell technology will also be reviewed in relation to their corresponding efficiencies. A brief overview of the PV market has also been included. Silicon solar cells will be shown to dominate this market and the reasons for such domination are discussed. PV research is closely related to market trends and as well as improved efficiency, cost and manufacturing issues must be considered as part of any research and development strategy. Finally, the aim of the research in this work will be outlined along with justifications of the importance of the experimental study.

1.2 World Energy Consumption

Since the widespread use of electricity, mankind's dependence upon it has grown exponentially. In 2010, the world produced over 20.2 trillion kilowatt-hours of electricity, and this figure is predicted to grow to 39.0 trillion kilowatt-hours by 2040 [1]. Electrical consumption is almost certainly set to rise year on year, but the methods by which this power is produced is far from certain. Over the recent decades, several issues have arisen which has changed our perception of electricity. The most important issues are concerned with the environment and depleted fuel reserves.

The emission of greenhouse gases has found to be directly related to global warming, causing the earth to heat up. Fig.1.1 plots the steady increase of temperature over the last one hundred years or so and also shows a prediction of how temperatures will rise, dependent on what we as the human race do next. To simply stop using fossil fuels for electricity and transportation is implausible, but if we reduce the amount of fuel we burn we can at least suppress the effects of global warming. If we do not reduce our emissions, we could see a potential temperature increase of as much as 3.3°C (6°F).

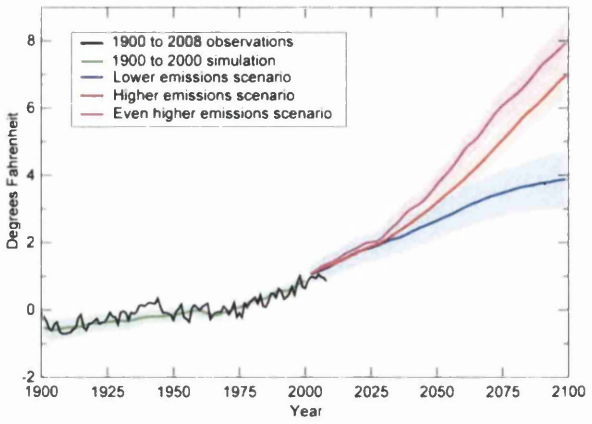


Figure 1.1: Predicted temperature increase due to emissions [2]

The second and perhaps more immediate concern with fossil fuels is their long term supply. Put simply, we have an ever increasing demand for energy but a limited amount of fossil fuels from which we can produce this energy. Fig.1.2 shows the remaining amount of three commonly used fossil fuels. If we do not find alternative energy sources, in a little over 50 years from now we will exhaust our natural gas and crude oil supplies that are currently known to exist.

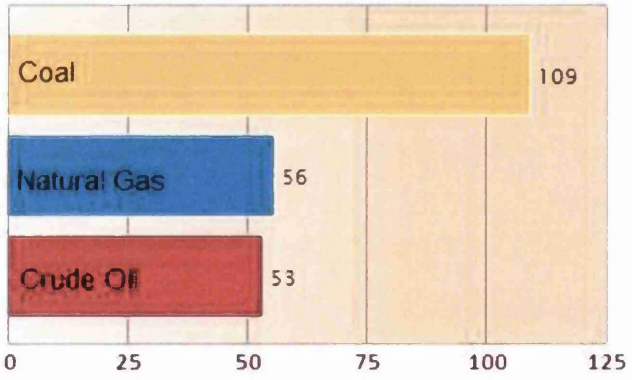


Figure 1.2: Fossil Fuels, years of extraction remaining [3]

The lower our reserves of fossil fuels become, the higher fossil fuel generated electricity prices will get. Presently, electricity in one form or another (being off-grid or on-grid) is accessible to 75% of mankind [4]. If we continue to rely upon the use of fossil fuels as our primary energy source, electricity prices will continue to rise until the poor can no longer afford it. The result would be millions of people and entire countries, particularly emerging economies, falling into energy poverty. Electricity provides the energy needed for manufacturing equipment, refrigeration for medical supplies, and energy for water treatment. It is therefore essential that alternative energy generation sources are found.

1.3 Renewable Energy

The alternative to fossil fuels is renewable or nuclear energy. Renewables are a source of energy that is replenishable and therefore everlasting. Worldwide directives have begun to emerge putting pressure on individual governments to reduce their dependency on fossil fuels, thereby reducing carbon emissions. Taking the United Kingdom as an example, the 2009 Renewable Energy Directive set a target for the UK to achieve 15% of its energy consumption from renewable sources by 2020 [5]. If the targets are not met there could well be financial sanctions imposed by other directive members. In recent years there has been a worldwide boom in renewable energy which is demonstrated in fig.1.3. The figure also displays future predictions of energy usage by fuel type, indicating that we are only just entering the era of renewable energy, which is set to substantially increase by 2040. It is important to note that nuclear energy is often included as a renewable energy source as it does not produce carbon emissions. Strictly speaking however, nuclear energy is not truly renewable as uranium is required, and estimated uranium reserves will only last for another 80 years at the current usage rate [6]. Despite this, the use of nuclear energy is predicted to increase as shown in fig.1.3. Safety issues that have recently come to light (with the Fukushima nuclear disaster) could affect this prediction as public concerns over the technology escalate.

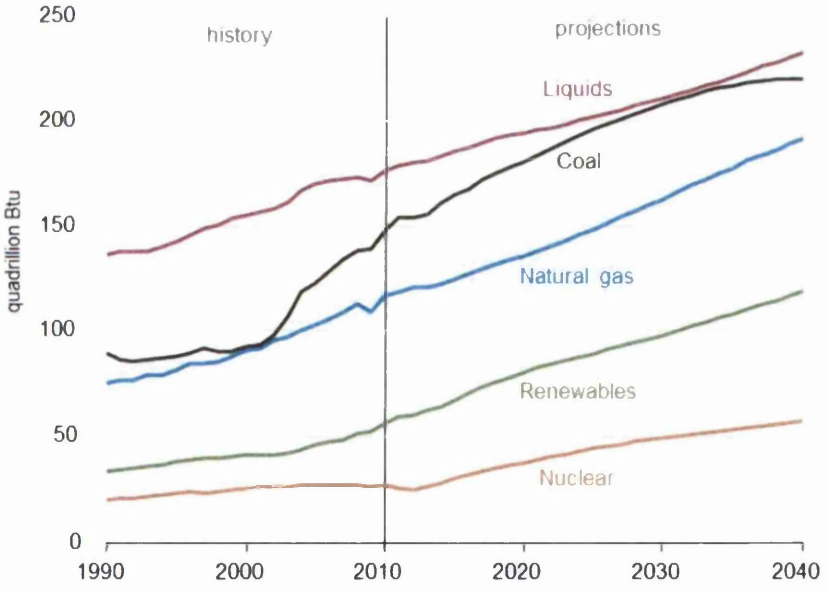


Figure 1.3: World energy consumption by fuel type 1990-2040 [1]

Types of truly renewable energy include those that produce electricity directly and those that need to be burnt to release energy. The main technologies are:

1. Direct electricity production
    - Wind: Wind turbines harvest kinetic energy from the wind and convert this energy into electricity.
    - Hydro: Hydro generators harvest kinetic energy from the movement of water and like wind turbines, convert this energy into electricity.
    - Solar Photovoltaics: Solar cells convert the energy from sunlight into DC electricity.
    - Ocean
        - Tidal: Tidal generators can take various forms but all rely upon harnessing energy from the movement of water.
        - Wave: Wave generators convert the up and down movement of waves into electrical energy.
2. Heat production
    - Anaerobic digestion: The process of anaerobic digestion releases methane gas which can be burnt to provide heat.
    - Bio energy
        - Wood: Felled trees can be burnt to provide heat.
        - Biomass: Vegetation can be burnt to provide heat.
        - Biofuel: Fuels such as ethanol can be produced from crops of corn.
    - Solar thermal: Different to solar PV, solar thermal uses energy from sunlight to heat water or other liquids.
    - Geothermal: Harnesses the earth's geothermal energy by digging deep into the ground.

From the above list, some renewable technologies provide an alternative fuel source which must be burnt in order to release its energy. The burning of a fuel (even if it is renewable) releases carbon which pollutes the atmosphere. For zero emission energy production, harnessing energy from the earth is critical. Solar, wind, hydro, geothermal, tidal and wave are all zero carbon energy techniques that can provide our energy without contributing to global warming. Table.1.1 shows the current and a predicted future use of such renewable sources. From the table, hydroelectric and wind are predicted to continue to produce most of the renewable energy, but solar has the largest annual percent change of 9.1%.

Region	2010	2015	2020	2025	2030	2035	2040	Average annual percent change, 2010-2040
World								
Hydroelectric	3,402	3,805	4,452	4,762	5,177	5,692	6,232	2.0
Wind	342	767	1,136	1,383	1,544	1,694	1,839	5.8
Geothermal	66	112	133	146	171	195	220	4.1
Solar	34	157	240	288	327	394	452	9.1
Other	332	427	549	643	729	800	858	3.2
Total World	**4,175**	**5,267**	**6,509**	**7,222**	**7,948**	**8,775**	**9,601**	**2.8**

Table 1.1: Renewable electricity generation (billion kilowatt-hours) by energy source [1]

1.4 Solar Energy

Solar renewable energy is typically split into two classifications, generation of heat and generation of electricity; technically referred to as solar thermal and solar photovoltaics respectively. This work will focus upon the use of solar photovoltaics for direct production of electricity.

In 1839, Edmund Becquerel discovered the photovoltaic effect [7] which is the basic principle by which solar photovoltaic cells operate. A solar cell converts energy from sunlight into electricity. The electricity produced by the solar cell is in the form of direct current (DC). Direct DC electricity production is unique to solar cells, with other renewable technologies such as wind and hydro power generating alternating current (AC).

A single solar cell typically produces a very low voltage and therefore it is common for many solar cells to be connected together in series to provide a more useful, higher voltage. When cells are connected together to form a larger array, the product is known as a solar module or panel. Solar cells also produce direct current which for some applications is ideal, although most domestic appliances use alternating current. To convert the direct current produced by solar cells into an alternating current an electrical device called an inverter is used. An array of panels connected to an inverter forms the basics of a solar PV system, which is typically what is installed in domestic applications. More details on the system element of this technology can be found in the Appendix B of this work.

The use of solar photovoltaic renewable energy has grown exponentially over the last ten years as can be observed in fig.1.4.

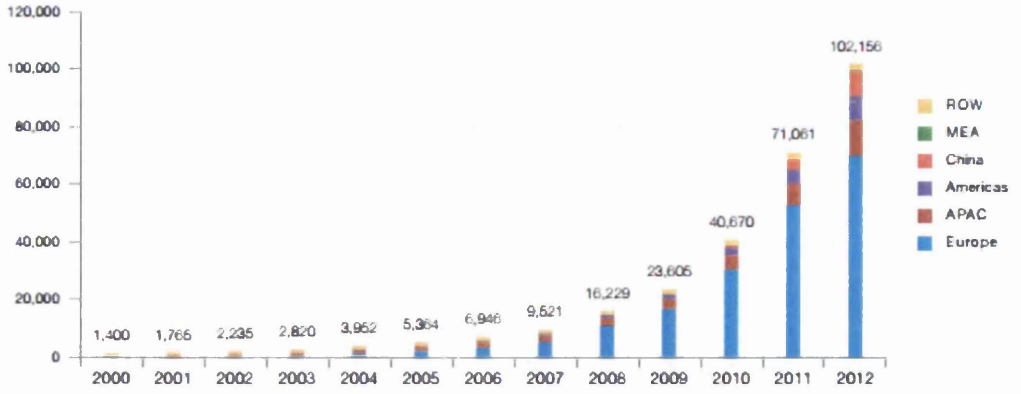


Figure 1.4: Evolution of global PV cumulative installed capacity 2000-2012 (MW) [8]

The growth of the industry is due largely to two factors. Firstly the advantages of solar photovoltaics over other renewable technologies and secondly financial incentives offered by governments.

1. Advantages of solar photovoltaics over other renewable technologies:

- Zero carbon emissions
- Can work anywhere exposed to sunlight
- Not as obtrusive as wind turbines
- Virtually maintenance free as there are no moving parts
- Modular solar panels are used which allow for easy assembly of various size systems from Watts to Mega Watts.
- Ease of building integration due to the various sizes, colours and flexibility of cells available.
- Direct current (DC) generation allowing for simple battery storage systems.

2. Financial incentives. To boost the market for renewable technology, incentives have been offered for the installation of not only solar but also other renewable technologies. Focusing on the case of solar in the United Kingdom gives a good description of the incentives that have been offered. In 2010, the UK government introduced the Feed-In Tariff (FiT) to promote the installation of small scale renewable energy systems. As renewable technologies were seen by most as an unknown, the FiT provided a financial incentive for people to install them. The tariff is scaled depending on the size of such a system and guaranteed for between 20 and 25 years. Table.1.2 shows the first tariff incentives for solar electricity production (2010).

Description	2010 Tariff (p/kWh)
<4kW new build	37.8
<4kW existing building	43.3
4kW - 10kW	37.8
10kW - 50kW	32.9

Table 1.2: 2010 UK solar feed in tariff [9]

The introduction of the tariff scheme saw a huge boost in solar PV installations in the UK. The downside to this was that the government had underestimated global PV system costs, which began to decrease rapidly. The financial incentive of the FiT had fast become a way for consumers of installed systems to make large profits. The typical payback time for a system was as low as five years meaning that the next 15 years of FiT payments were pure profit. On April 1st 2012, the UK government slashed the feed in tariff rates by 50% to prevent such profit making. The UK FiT for a <4kW PV system on an existing building (at the time of writing this thesis) is 14.9p/kWh.

1.5 Solar Cell Generations

Since the first silicon solar cell was produced at Bell Laboratories in the 1950's [10], there have been three generations of photovoltaic technologies. Fig.1.5 shows the most recent efficiency chart for all the different generations of solar cells.

1. First generation solar cells include the one fabricated at Bell Laboratories. These are wafer based silicon solar cells. Despite being the first generation of cells, they are the most commonly used type of silicon solar cell making up over 80% of the total PV market [11]. First generation cells can be further classified by the quality of the silicon they are fabricated from. There are two main categories namely monocrystalline and multicrystalline wafers. Monocrystalline cells are fabricated from high quality single crystal wafers, whereas multicrystalline cells are fabricated from wafers with multiple crystal domains. Due to the higher quality of monocrystalline cells, they have a higher efficiency than cells produced from multicrystalline substrates. Unfortunately such purity of monocrystalline cells comes at a cost and despite multicrystalline cells having lower efficiencies; they are more commonly used due to their lower production cost. From fig.1.5 wafer based silicon solar cells have achieved up to 25% efficiency (without concentration).

2. Second generation solar cells are known as thin film cells due to their thin solar active layers. Such cells include amorphous silicon (a-Si), Cadmium Telluride/Cadmium Sulfide (CdTe/CdS), Copper Indium Selenide and Copper Indium Gallium Selenide (CIGS) solar cells. Thin film second generation cells have lower efficiencies to that of first generation wafer based cells, but can be fabricated at low cost. Due to the materials and substrates used for such devices, solar cell production can take place over far larger areas than that of a typical wafer based cell. From fig.1.5, the highest performing technology in this generation are Copper Indium Gallium Selenide cells with 20.8% efficiency (without concentration).
3. Third generation solar cells typically do not rely on p-n junctions and can be of varied constructions. Third generation cells include nanostructured cells, organic PV OPV), dye-sensitised solar cells (DSSC), tandem/multijunction cells and concentrator cells. This wide ranging category offers cells that are cheap to produce with very low efficiencies, all way up to expensive cells offing very high efficiency such as the record efficiency three junction cell with 38.8% (without concentration) and 44.4% (under concentration at 302 suns) efficiencies. Concentrator cells use focused (concentrated) sunlight up to 1000x normal intensity.

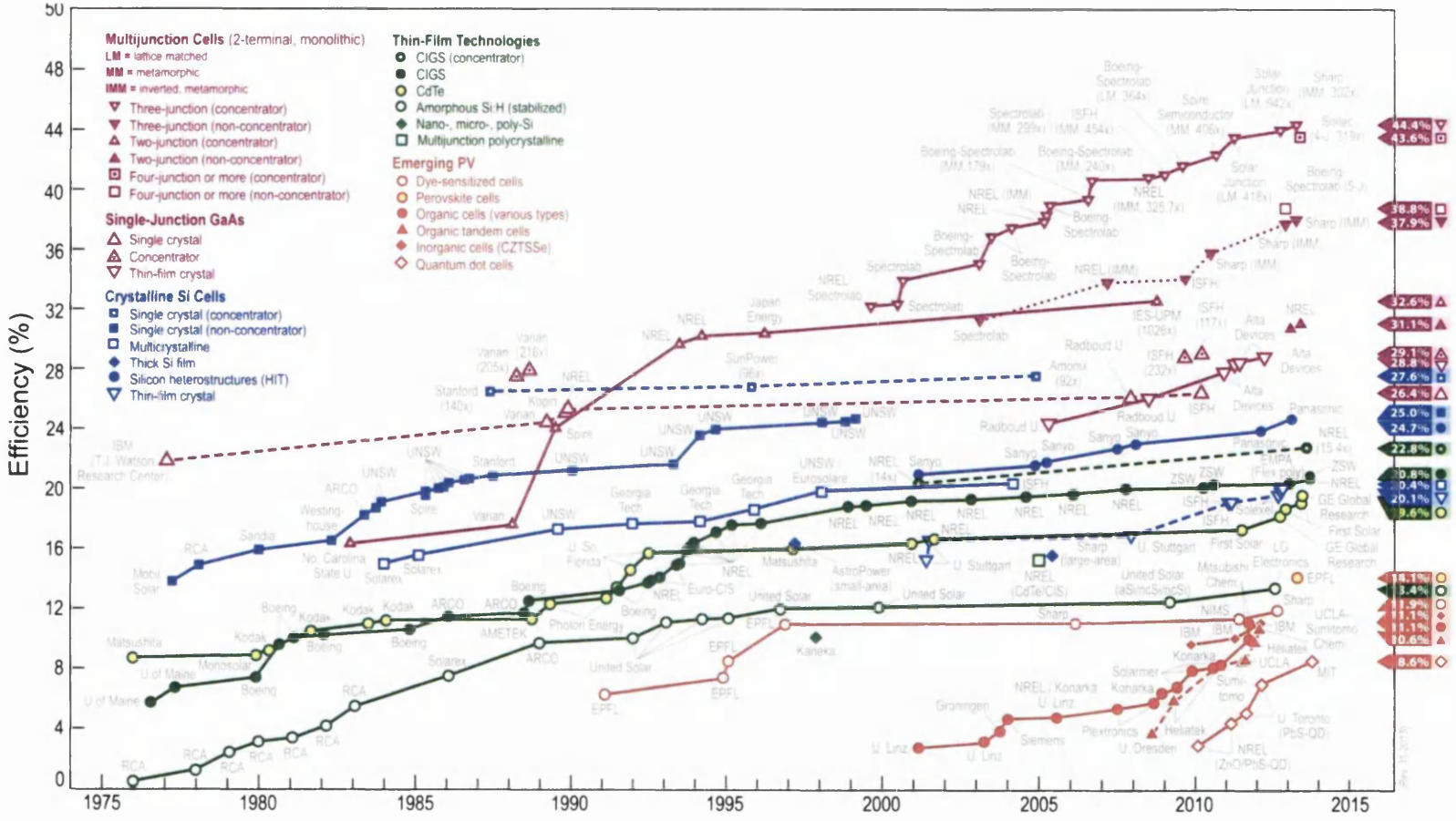


Figure 1.5: Best research cell efficiencies as of November 2013 [12]

1.6 The Future of Photovoltaic Solar Cells

Wafer based silicon photovoltaics have dominated the photovoltaic industry since the very beginning of the solar cell market in the 1950's [13]. Other than wafer based crystalline cells, the rest of the terrestrial PV market is made up of thin film cells such as amorphous silicon (a-Si), cadmium-telluride (CdTe) and copper indium gallium selenide (CIGS) [14].

Despite the current market conditions, other cell technologies are predicted to gain a larger market share. Fig.1.6 shows some of the emerging technologies and their long-term predicted efficiencies.

	2010	2015-2020	2030-
CPV			
Effic.(lab-effic),%	20-25 (40)	36 (45)	>45
Major R&D areas and targets	lifetime; optical efficiency (85%), sun-tracking, high concentration, up-scaling;		
Inorganic TF (spherical cells, poly c-Si cells)			
Effic.(lab-effic),%	(10.5)	12-14 (15)	16-18
Major R&D areas and targets	deposition, interconnection, ultra-thin films; up-scaling, light tailoring		
Organic cells (OPV, DSSC)			
Effic.(lab-effic),%	4 (6-12)	10 (15)	na
Major R&D areas and targets	Lifetime (>15 yr), industrial up-scaling		
Novel active layers			
Effic.(lab-effic),%	na	(>25)	40
Major R&D areas and targets	Materials, deposition techniques, understanding quantum effects, up-scaling from lab production		
Up/down converters			
Module effic., %	+10% over ref material		
Major R&D areas and targets	(nano) materials, physical stability, up-scaling		

Figure 1.6: Performance and targets for emerging PV options [14]

Concentrated photovoltaics (CPV) have existed for many years although they have still not broken into the mainstream solar cell industry, mainly because of high costs associated with the technology. Their primary application therefore has been in high value markets such as power generation for space applications [11]. Wafer based silicon solar cells have shown promise at relatively low concentration ratios, but the heat generated by high concentrator systems begins to degrade cell performance (as much as -0.5% relative per °C [11]). The materials of choice for high concentrator system are III-V semiconductors which can be tailored to produce a wide range of optical band gaps. Multijunction cells fabricated from various III-V materials can further utilise the whole solar spectrum. As previously described above, triple junction (GaInP/GaInAs/Ge) cells have produced record breaking efficiencies of 44.4% at 302x light concentration. Cost reductions relating to cell

manufacture and optical tracking for concentrator lenses, could see the technology commercially used.

Inorganic thin film (TF) solar cells such as a-Si, CIS, CIGS and CdTe already have a 20% market share [14], but their relatively low cell efficiencies are limiting mainstream use relative to crystalline silicon cells. It is important to note however that there has been a large amount of interest in recent years regarding thin film cells. Many analysts predicted that the price per watt of thin film technologies would by now be far less than that of wafer based silicon cells. However, the recent market trend for wafer based cells (which is discussed in more detail in 1.7) has seen the opposite effect as can be observed in fig.1.7.

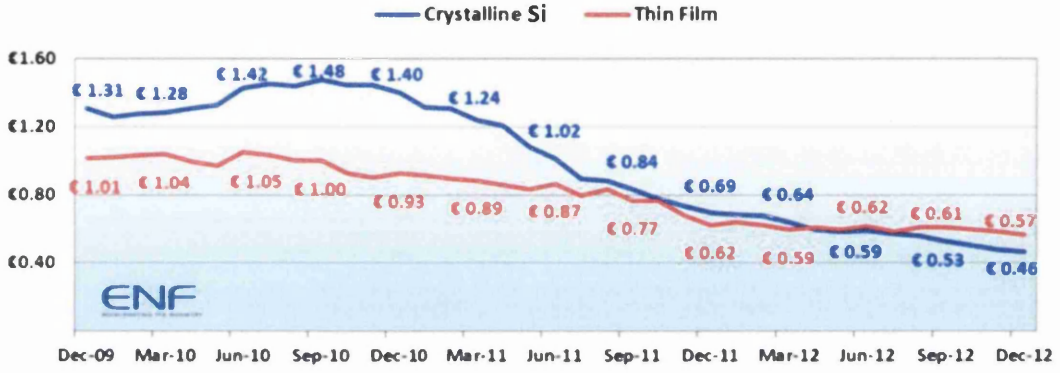


Figure 1.7: Chinese manufacturer average panel price for thin film and crystalline silicon [15]

From fig.1.7 it is apparent that until the middle of 2011, thin film solar cells were significantly cheaper than crystalline silicon based modules. It is quite possible that in the future, cost reductions and efficiency improvements will continue to be made in thin film technology at a faster rate than that of crystalline silicon equivalents.

Thin film cells such as dye sensitised and organic PV (OPV) cells can feasibly achieve a cost per watt of below $0.50 (USD) once scaling of processes is applied [14]. Issues around relatively low efficiency (11% academic record) and lifetime issues related to dye sensitised solar cells (DSSCs) are currently holding back the technology, although advancements through extensive research are continually being made. If lifetime and commercial efficiencies can be raised, organic cells, due to their inherent low cost and large scale application could have a large impact on the solar industry, although there are still significant obstacles to overcome.

There are many novel solar cell technologies constantly being developed and analysed. The interest in nanotechnology has seen a wide range of different structures and materials than can have excellent absorption capabilities as well as theoretical efficiency limits as high as 60% [14]. Another significant recent breakthrough has been the use of

perovskite for cell production, which stemmed from research into DSSCs. Perovskites are the name given for any materials that have the same crystal structure as calcium titanate, hence they are abundant materials [16].The technology has seen research investigations in the last year with cells rapidly reaching conversion efficiencies in excess of 15% [17]. Such cells although still firmly in the research and development phase are predicted to be capable of reaching efficiencies as high as 20-25% and cost only $0.10 to $0.20 (USD) per watt [18].

Despite the research and development of several different solar cell technologies, it is safe to say that for the foreseeable future, crystalline silicon solar cells will continue to dominate the market as they have done for over 50 years. A significant amount of research still revolves around efficiency enhancement and cost reduction of wafer based silicon solar cells. Recent research into up and down converters for example aims for photon absorption and re-emission at a different wavelength which could improve the efficiency of silicon solar cells by up to 10% (by expanding the spectral range of absorption) [14]. Laboratory developed silicon solar cells are now reaching in excess of 25% and moving ever closer to the theoretical silicon solar cell efficiency limit of 29.8% [19].

Of all PV technologies, perovskite sensitised solar cells have the greatest potential for replacing silicon wafer based cells, provided that predictions of cost and efficiency prove to be correct. The shear abundance of the material and simple processing technology (low cost), coupled with efficiencies as high as 25% could revolutionise the industry and help photovoltaic generated electricity to contend financially with fossil fuel technologies.

1.7 Cost Vs Efficiency

The commercial success of a solar cell technology not only relies upon efficiency but also the cost of producing the cell. Wafer based silicon solar cells dominate the market despite only being around 18-20% efficient. The reason they are so successful is that they provide reasonable electrical power at low cost. These parameters are critical for commercial installations of PV where people are competing directly against the cost of other renewable and fossil fuel technologies. For niche applications where cost is not as significant, high efficiency cells can be used for their higher electrical output, for example III-V solar cells for satellite applications. Fig.1.8 shows the typical efficiency and cost implications of each of the solar cell generations.

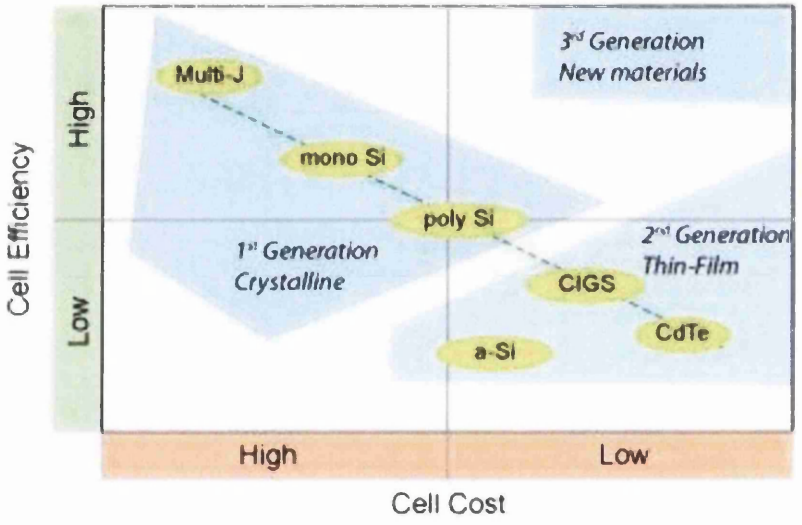


Figure 1.8: Efficiency Cost Profile for different solar generations [20]

Despite the low efficiency of wafer based crystalline silicon cells compared to multijunction cells that can exhibit efficiencies in excess of 40%, silicon cells dominate the market place. Fig.1.9 shows the current and predicted market share of photovoltaics by each technology type. The market share of silicon is predicted to remain constant at around 80% until 2017 at least. The reason for the great success of silicon is due to its abundance of raw materials, reliability, ease of construction, and wealth of knowledge in the area taken from the semiconductor industry. Industrial equipment specifically designed for silicon solar cell production has long been used and adopted by many countries that are now able to produce vast quantities of cells at low cost. The production of silicon specifically for solar cell production also greatly enhanced mass production capability resulting in huge cost reductions.

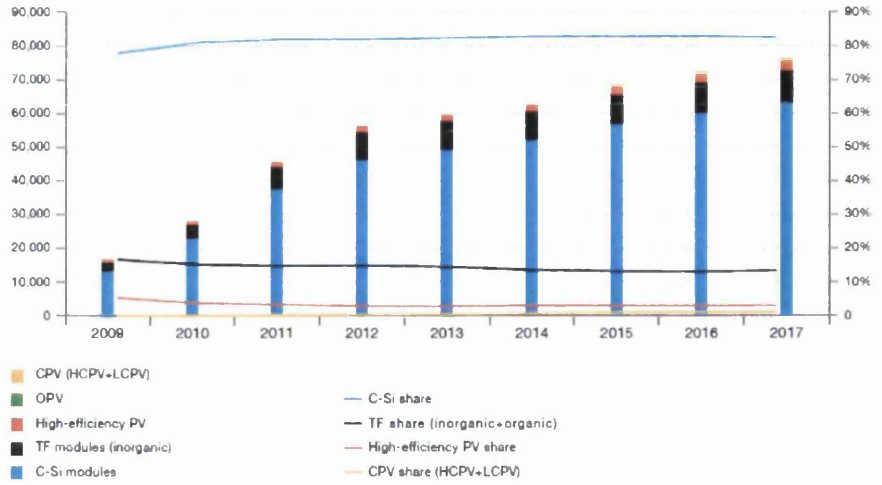


Figure 1.9: Market share of photovoltaics by each technology type [8]

Such large scale manufacturing of solar cells and panels particularly in China, has in recent years, led to a huge fall in the cost of silicon wafer based solar cells. The extent of the dramatic fall in panel costs is shown in fig.1.10, with a cost per watt of $1.81 in the first quarter of 2010 which reduced significantly to just $0.70 at the beginning of 2013.

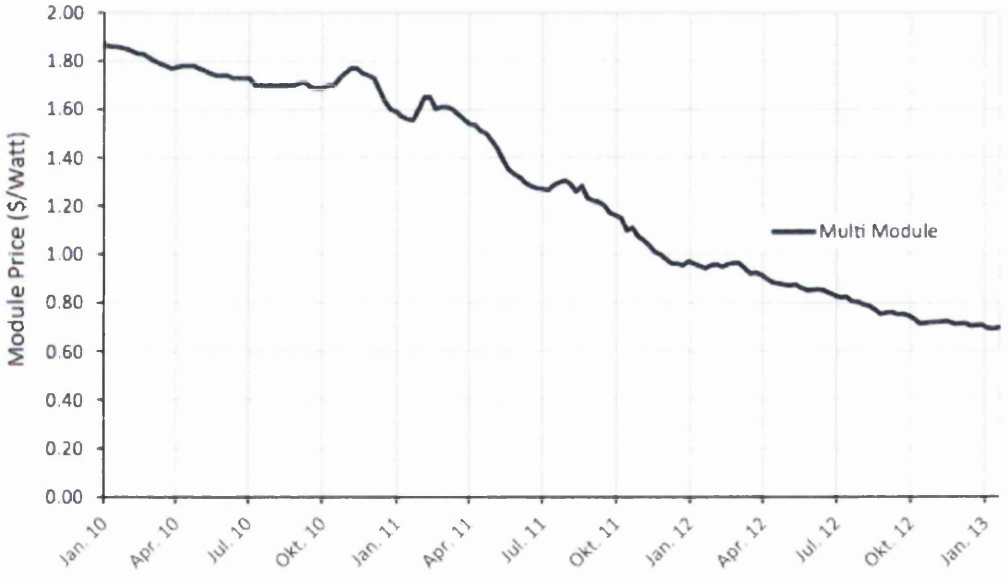


Figure 1.10: Silicon solar cell module cost reductions ($USD/Watt) [21]

It is important to note that these price reductions do not entirely translate into streamlining of the industry. Chinese cell manufacturers have been reported to be producing and selling solar cells and modules below cost [22]. This is mainly due to oversupply issues in the Chinese solar industry with production of cells exceeding demand. Recently due to the adverse effect of such 'dumping' of below cost modules, the European

Union imposed a series of measures on Chinese imported cells and modules. The measures included limiting EU imports to 7GW annually and also setting a minimum price of €0.56 per watt for silicon based modules [23]. Despite the minimum pricing, the majority of European solar module manufacturers have said that the pricing is still far too low and actual cost of solar production in China [24].

The turbulence in the industry has put a larger emphasis on cost reduction than ever before. Put simply, without substantial cost reductions or further government intervention, European solar cell manufacturers will continue to find it very hard to compete in the market. Recently here in the United Kingdom Sharp has announced the closure of its solar panel assembly plant because it is unable to compete in the current market [25].The UK industry now has to develop intellectual property and niche PV products (high value) to survive in the current market.

The focus of solar photovoltaics has always been strongly influenced by efficiency and cost. In order for the industry to continue to impact upon the renewable energy market, cell efficiency will need to rise or costs will need to reduce or preferably a combination of both. Unfortunately however, a trade-off currently exists between these two factors.

1.8 Outline of Thesis

Wafer based silicon solar cells dominate the market due to their reasonably high efficiencies and low cost processing conditions. In order for wafer based silicon solar cells to continue to dominate the market, they must continue to increase in efficiency whilst reducing in cost. As the efficiency of lab based silicon cells are approaching the fundamental limit for such devices, cost factors are becoming more important.

The primary aim of this work is to target the material usage for cell production. It will be shown that current wafer based silicon solar cells are using far more silicon material than is actually required for high efficiency cells. The cost of conventional monocrystalline solar cells is relatively high because of the high purity of the silicon wafer substrate from which the cell is produced. By producing a cell that uses less silicon material, significant cost savings can be made. Conventional techniques used in industry to produce cells are limited by the thickness of which a substrate can be cut. The method adopted and investigated in this work uses exfoliation principles to produce silicon substrates only 40μm thick. Such thin silicon foils are more than four times thinner than that currently used to fabricate commercial solar cells. The work investigated a variety of principles related to the process, in order to optimise and understand the mechanisms involved. From the experimental research, a novel process was developed in order to fabricate a fully operational solar cell from the40μm thick silicon foil.

One significant issue that arose from the use of such a thin exfoliated silicon substrate was the difficulty of using conventional anti-reflective texturing techniques. Such microscale texturing could significantly weaken the structure of a thin (40μm) silicon substrate. Issues relating to the surface quality of exfoliated Si substrates could also potentially disrupt effectiveness of conventional anisotropic texturing techniques. Research was conducted into finding an alternative technique to match the performance of commercially used anti reflective processes. Experiments into the formation of porous silicon on the surface of a silicon substrate were found not only to match the commercial process, but to exceed the antireflective performance of conventional ARCs. The technique was deemed to be suitable for both thick crystalline and thin crystalline silicon wafer based substrates. The PSi layer was also found to have the potential to reduce costs associated with front surface reflectivity suppression, by using a single etching process. Using such a simple technique to provide reflectivity suppression could be more economical compared to the two step conventional technique commercially adopted.

Experimental investigation also focused upon the top contact for wafer based silicon solar cells. As the top of the cell must allow for light absorption and the formation of electrical contacts, a trade off exists between shading losses and resistance of the front metallisation. A method was adopted to increase the electrical performance of standard front contact topologies without significantly increasing shading loss. Silver nanowires were successfully deposited and analysed on standard silicon solar cell top contacts as an electrical enhancement contact. Such a coating can improve the collection ability of the top contact but due to their nanoscale diameters, shading losses are not dramatically increased by the silver nanowires. The coating resulted in a substantial increase in cell efficiency when the optimum nanowire coating density layer was applied. The silver nanowire contact scheme is not compatible with traditional micro textured anti reflective surface. However, it can be integrated with the porous silicon anti reflective method developed in this work.

As my work was part funding by a solar cell fabrication company, product development was also undertaken. Although this work was not strictly academically based, it provided me with a commercial insight into the integration of photovoltaics with our environment. Two silicon solar cell based products that I helped to develop in conjunction with the company, have been briefly outlined in the Appendices Chapter of this work.

[1] Energy Information Administration, International Energy Outlook 2013, EIA, 2013
[2] Epa.gov. 2013. Future Climate Change | Climate Change | US EPA. [online] Available at: http://www.epa.gov/climatechange/science/future.html [Accessed: 4 Dec 2013]
[3] Knoema. 2013. World Reserves of Fossil Fuels - knoema.com. [online] Available at: http://knoema.com/smsfgud/world-reserves-of-fossil-fuels [Accessed: 4 Dec 2013]
[4] International Energy Agency, World Energy Outlook 2009, IEA, 2009
[5] Gov.uk. 2012. Increasing the use of low-carbon technologies - Policy - GOV.UK. [online] Available at: https://www.gov.uk/government/policies/increasing-the-use-of-low-carbon-technologies [Accessed: 4 Dec 2013]
[6] Royalsociety.org. 1999. Nuclear energy - the future climate | Royal Society. [online] Available at: http://royalsociety.org/policy/publications/1999/nuclear-energy/ [Accessed: 9 Aug 2013].
[7] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, John Wiley & Sons, 3 -312, 2003
[8] European Photovoltaic Industry Association, Global Market Outlook for Photovoltaics, 2013-2017, EPIA, 2013
[9] Ofgem.gov.uk. 2013. Feed-in Tariff Table 1 August 2011 | Ofgem. [online] Available at: https://www.ofgem.gov.uk/publications-and-updates/feed-tariff-table-1-august-2011 [Accessed: 2 Nov 2013].
[10] D.M. Chapin, C.S. Fuller and G.L. Pearson, A new p-n junction photocell for converting solar radiation into electrical power, J. Applied Phys. Vol 25, 1954, pp.: 676-677, 1954
[11] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, Second Edition, John Wiley & Sons, 265-313, 2011
[12] National Renewable energy Laboratory, Efficiency Chart, NREL, Rev 12-04-2013
[13] Comprehensive Renewable Energy, Ali Sayigh, Oxford Elsevier, 2012
[14] IEA-ETSAP and IRENA© Technology Brief E11 – January 2013
[15] CleanTechnica. 2013. panel_price_en. [online] Available at: http://cleantechnica.com/2013/01/13/small-chinese-solar-manufacturers-were-decimated-in-2012/panel_price_en/ [Accessed: 22 Nov 2013].
[16] Henry J. Snaith, Perovskites: The Emergence of a New Era for Low-Cost, High-Efficiency Solar Cells, The Journal of Physical Chemistry Letters, 4 (21), 3623-3630, 2013
[17] Docampo, Pablo *et al*, Efficient organometal trihalide perovskite planar-heterojunction solar cells on flexible polymer substrates, Nature Communications 4, 2761, 2013
[18] MIT Technology Review. 2013. A Material That Could Make Solar Power "Dirt Cheap" | MIT Technology Review. [online] Available at: http://www.technologyreview.com/news/517811/a-material-that-could-make-solar-power-dirt-cheap/ [Accessed: 22 Dec 2013].
[19] Tiedje, T.; Yablonovitch, E.; Cody, G.D.; Brooks, B.G., "Limiting efficiency of silicon solar cells," Electron Devices, IEEE Transactions, vol.31, no.5, pp.711-716, 1984
[20] Greenrhinoenergy.com, (2014). PV Cells & Modules, Photovoltaics | Solar Power. [online] Available at: http://www.greenrhinoenergy.com/solar/technologies/pv_modules.php [Accessed 19 May. 2014].
[21] Contributor, G. (2014). Solar PV Costs Will Fall By Half By 2020, But Prices Won't. [online] CleanTechnica. Available at: http://cleantechnica.com/2013/05/26/solar-pv-costs-will-fall-by-half-by-2020-but-prices-wont/ [Accessed 19 May. 2014].

[22] Europa.eu. 2013. EUROPA - PRESS RELEASES - Press release - EU imposes definitive measures on Chinese solar panels, confirms undertaking with Chinese solar panel exporters. [online] Available at: http://europa.eu/rapid/press-release_IP-13-1190_en.htm [Accessed: 20 Nov 2013].

[23] Pv-tech.org. 2013. EU governments approve China solar trade spat solution - PV-Tech. [online] Available at: http://www.pv-tech.org/news/eu_governments_approve_solar_trade_spat_solution [Accessed: 6 Dec 2013].

[24] Renewable Energy World. 2013. Chinese Solar Panels under EU anti-dumping custom duty. [online] Available at: http://www.renewableenergyworld.com/rea/blog/post/print/2013/12/chinese-solar-panels-under-eu-anti-dumping-custom-duty [Accessed: 26 Dec 2013].

[25] Pv-tech.org. 2013. Sharp closing uncompetitive UK solar module assembly plant - PV-Tech. [online] Available at: http://www.pv-tech.org/news/sharp_closing_uncompetitive_uk_solar_module_assembly_plant [Accessed: 26 Dec 2013].

Chapter 2: Solar Cell Operation

2.1 The P-N Junction

Semiconductor solar cells rely upon the structure of a p-n junction. Due to the importance of the p-n junction, a brief description will be given. Since this work is related with silicon photovoltaics, examples will be given which refer to Si p-n junctions.

Semiconductor materials used for solar cell fabrication such as silicon are often pure crystalline materials. Silicon for example has four valence electrons which are shared with four neighbouring atoms forming covalent bonds. All the electrons are being utilised in covalent bonds and the material is at equilibrium, i.e. no excess electrons or holes. The material is referred to as an intrinsic semiconductor and contains no impurities or dopants. Semiconducting materials are called such as they are able to conduct electricity above absolute zero. If the thermal energy is enough to overcome the band gap, an electron is promoted from the valence band to the conduction band (Ec) where it is free to participate in conduction. The vacancy left by the electron is referred to as a hole which is positively charged. Both the electron and hole are able to participate in conduction and they are often referred to as electron hole pairs or carriers (as they carry charge). The larger the band gap of the material the harder it is for an electron to be thermally excited to the conduction band. Therefore the higher the band gap the more insulating a material becomes and the lower the band gap the more conducting it is. A semiconductor material is in between these two conductivities. It is very important to note that in an intrinsic semiconductor, few electrons are thermally excited and the material is only partially conductive. Elevating the temperature however can increase the number of electrons excited and therefore increase conduction in the semiconductor. At 25 °C the intrinsic carrier concentration of silicon is $8.3 \times 10^{9} cm^{-3}$ whilst at 50°C it is $5.836 \times 10^{10} cm^{-3}$ [1].

To produce a solar cell and utilize the photovoltaic effect, two differently charged semiconducting regions are required to form a p-n junction. This essentially involves creating a junction where one side has an increased amount of electrons available (n-type as electrons have negative charge) and the other has an excess of holes available (p-type as holes have positive charge). In an n-type material there are more electrons than holes and therefore the majority carriers are the electrons and the minority carriers are the holes. In p-type, holes are majority carriers and electrons minority carriers.

In order to make an intrinsic semiconducting material n or p-type, another element must be added which has atoms with excess electrons or excess holes. The addition of such a material is referred to as 'doping', where impurities are added to disrupt the intrinsic qualities of the semiconductor. Once again using silicon as an example, a material containing an excess electron is required to produce n-type silicon. From Table 2.1, a group V material is required for n-type doping, such as Phosphorous. Similarly to produce p-type silicon a group III material is required, such as Boron.

III	IV	V
boron 5 **B** 10.811	carbon 6 **C** 12.011	nitrogen 7 **N** 14.007
aluminium 13 **Al** 26.982	silicon 14 **Si** 28.086	phosphorus 15 **P** 30.974
gallium 31 **Ga** 69.723	germanium 32 **Ge** 72.61	arsenic 33 **As** 74.922

Table 2.1: Group III to V of the periodic table

Doping of a semiconductor such as silicon is typically carried out by diffusing a dopant into the material at high temperature. The material is first doped p or n-type during the silicon growth process, followed by a diffusion doping procedure to add in the other dopant layer. The doping concentration, i.e. the number of atoms introduced with free holes or electrons, strongly affects the number of majority and minority carriers. Alternative doping processes such as ion implantation can be used, but diffusion doping is the most commonly used method for silicon PV cells [2].

Now that a p-n junction has been created, the photovoltaic effect can be exploited. Fig.2.1 below shows a typical schematic of the cross section of a silicon solar cell.

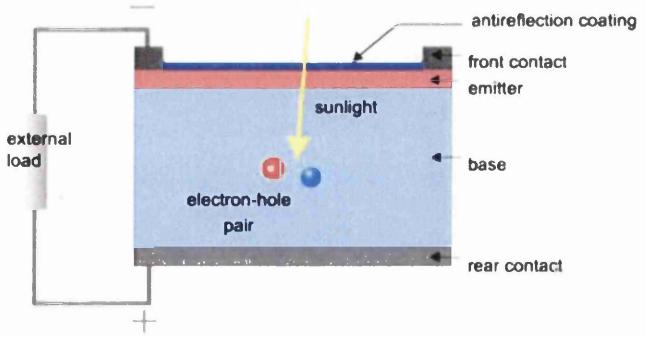


Figure 2.1: Cross section of a silicon solar cell [2]

Fig.2.1 is shows a p-n junction, with a metal contact to the top n-type silicon (called the emitter), and an electrical contact to the bottom p-type material (called the base). Since photons of energy from the sun must enter the cell, the front contact is made up of a series

of gridlines/fingers which allow a proportion of the light to enter the cell whilst still making an electrical contact to the silicon. An antireflective layer is deposited onto the surface of the cell to reduce reflectivity by enhancing light capture.

When a photon of energy from the sun is incident on the cell, if the energy of the photon is greater than or equal to that of the band gap of the semiconductor material, it is absorbed. For silicon that has a band gap of around 1.12eV, only photons with energy equal to 1.12eV or above will be utilized by the cell. Photons with energy less than the band gap will pass through the semiconductor without being absorbed. Photons with higher energy than that of the band gap can lose any energy higher than the band gap as heat and end up in the same position in the band gap as electrons excited by photons equal to the band gap.

When the photon energy is high enough and is absorbed, an electron is promoted from the valence band into the conduction band. The promotion creates a minority and majority carrier depending on the doping of the semiconductor. For a standard n-type emitter silicon solar cell, the minority carrier in the n-type emitter would be a hole. Minority carriers can only exist for a short amount of time before they naturally recombine (energy wasted and not utilized by cell). The job of the p-n junction is to keep them apart prohibiting recombination (using an electric field) as shown in fig.2.2. If the minority carrier (hole) makes it to the junction, the electric field created at the p-n junction transports it across the junction (to p-type silicon) where it is now a majority carrier and can contribute to current flow. The electron in the emitter is now free to move out of the cell through the top electrical contact, dissipate its energy through the external load before re-entering the cell through the back contact where it can recombine with the hole. Unfortunately not all minority carriers make it across the junction due to recombination mechanisms that exist in the bulk and at the surface of the cell. Any carriers that recombine are lost and no current can be generated from them. Thus to maximise the efficiency of a cell, carriers should be generated in the vicinity of the p-n junction.

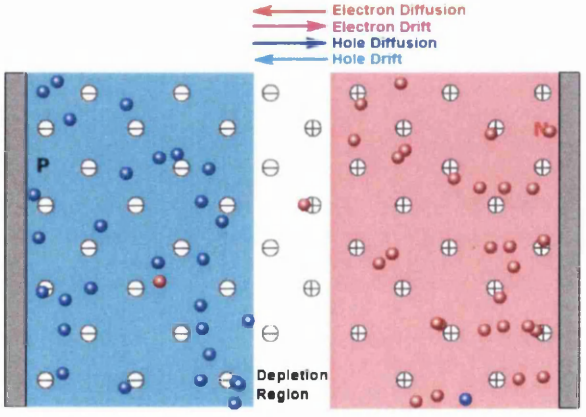


Figure 2.2: Schematic of a silicon solar cell p-n junction [3]

2.2 Important solar cell parameters

In a solar cell the electrical performance of the device is calculated from electrical measurements. The most important parameter is the efficiency of a device which is given as:

$$\eta = \frac{Pmax}{Pin} \quad (2.1)$$

where: $Pmax$ is the maximum power

Pin is the power of the incident photons on the cell

Since:

$$Pmax = V_{oc} \times I_{sc} \times FF \quad (2.2)$$

where: V_{oc} is the open circuit voltage

I_{sc} is the short circuit current

FF is the fill factor

Therefore:

$$\eta = \frac{(Voc)(Isc)(FF)}{Pin} \quad (2.3)$$

From the efficiency equation, it is advantageous for solar cell devices to have a high open circuit voltage, high short circuit current and high fill factor. Such parameters are therefore very important in rating the performance of a photovoltaic device. Each parameter will be fully discussed along with full explanations of where and how each value originates.

2.2.1 Short Circuit Current (Isc)

The short circuit current (I_{sc}) of a solar cell is the highest current value observed for the cell at 0V (fig.2.3) as it is not connected to a load but is instead short circuited (i.e. positive and negative contacts connected together). The short circuit current of a cell is a typical measurement made during efficiency calculations to determine the performance of the cell, without any effects from external circuitry and loads etc.

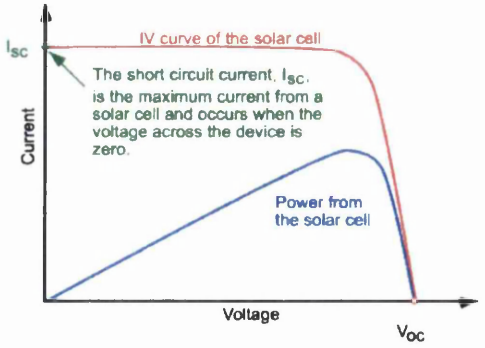


Figure 2.3: Short circuit current of a solar cell [4]

The short circuit current of a solar cell relies upon two factors, the electron-hole pair generation rate and the collection probability (successfully collecting light generated carriers).

1. The amount of light generated carriers is in turn dependent on several aspects. Major aspects include:
    - Band-gap of the solar cell: Only photons entering the cell with a higher energy than that of the band gap will contribute towards current generation. Photons must have enough energy to be able to excite an electron from the valence to the conduction band (electron-hole pair generated). For example, a silicon solar cell with a band gap of 1.12eV requires wavelengths shorter than 1100nm. Therefore the spectrum of light incident on a cell is of high importance.
    - Light intensity: A higher light intensity would mean a higher Isc as there is more irradiative power per unit area. In measuring a standard solar cell for ground use a standard illumination at AM1.5 is used. The standard adopted, mimics the solar spectrum that we observe on the surface of the earth as shown in fig.2.7. Due to the constantly changing solar spectrum during daytime, using standard spectra allows for consistent solar cell performance analysis to be made. This also means that if one cell is found to have a higher efficiency than another, this is due to the cell and not because more light is incident. The AM1.5 standard also known as the '1 sun standard' translates into a light intensity of 1000 W/m^2 at 25 °C perpendicular to the cell plane [5].
    - Reflectivity of the solar cell material: If the surface of the material has a high reflectivity, photons can be reflected away and not utilized. The lower the reflectivity the more light enters the cell, rather than being lost by reflection.
    - Absorption coefficient of the cell material: Essentially a measurement of how good a material is at absorbing a photon. Some wavelengths get absorbed at the surface of a cell material and others deeper into it. A high absorption coefficient is advantageous. Different semiconductors have different coefficients.
    - Thickness of cell: As previously mentioned different wavelengths get absorbed (utilized for current generation) at different depths in a semiconducting material. If the material is too thin, photons can pass through it without being absorbed.

2. The collection probability is the likelihood that a light generated carrier will make it to the p-n junction and therefore be utilized for current generation. Unfortunately due to recombination mechanisms and other losses, not every carrier generated will contribute to power generation. Collection probability relies upon:
    - Recombination mechanisms: If a carrier recombines before it makes it to the depletion region it no longer contributes to power generation as it loses its energy usually as heat. For indirect materials such as silicon, recombination is typically caused by defects at the surface or within the material. Different recombination mechanisms exist for the surface of the material than that of the bulk.
    - The distance away from the depletion region a carrier is generated: If a carrier is generated within the region then the probability of it being collected will be 100%. The region where carriers can be collected successfully is roughly within a diffusion length of the p-n junction. The diffusion length for a wafer based silicon solar cell is around 100-300μm [6]. Further away from the region, the probability decreases as the distance carriers must travel is larger. Therefore the probability of recombination is higher.

From the factors that affect short circuit current mentioned above, it is surmised that Isc is the same as that of the current produced by light generation. Unfortunately further losses occur due to the collection of light generated carriers by the electrical contacts to the solar cell (resistive loss mechanisms).

From the two main factors that make up the Isc, the simplified equation (neglecting recombination and assuming uniform generation) for a solar cell short circuit current is:

$$Isc = qG(Ln + Lp + W) \quad (2.4)$$

Where: G is the generation rate
L_n is the electron diffusion length
L_p is the hole diffusion length
W is the width of the depletion region
q is the absolute value of electron charge

2.2.2 Open Circuit Voltage (Voc)

Without a voltage a solar cell would not produce any power, the Open Circuit Voltage is the highest voltage measurement of a cell when the cell is open circuit, i.e. no current flow (fig.2.4). Voltage in a solar cell is created by the photovoltaic effect.

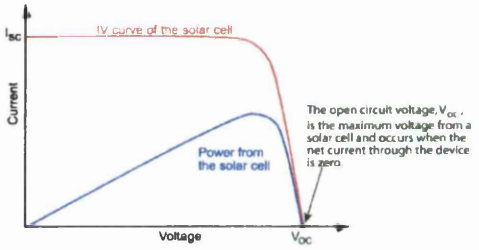


Figure 2.4: Open circuit voltage of a solar cell [7]

The photovoltaic effect relies upon the creation of a potential difference across the p-n junction of a semiconductor material in relation to light input into the material. As discussed previously, light generated carriers only contribute to current generation if they make it to the depletion region of the cell. When the cell is short circuited, carriers can freely leave the device as a current. Under open circuit conditions however no current can flow as the terminals of the cell are isolated from one another. Since carriers are now unable to leave the device, a charge builds up as electrons and holes begin to accumulate (electrons in n-type and holes in p-type side of junction) as carriers are still being generated by the incident light. The Voc of a cell is essentially the voltage value at which the current generated by incident light and the diffusion current are balanced, i.e. no current flow. Therefore the Voc corresponds to the forward bias voltage, at which the dark current (current measured from cell without illumination) compensates the photo-current [8]. The equation for Voc relates to this action:

$$Voc = \frac{nkT}{q} \ln\left(\frac{I_L}{I_o} + 1\right) \tag{2.5}$$

Where: I_L = Light generated current (current measured from cell under illumination)

I_o = Saturation current (current flow caused by the drift of minority carriers across the junction)

Similar to the Isc, as the current is dependent upon the area of the cell it is common to express the current as a density, therefore the equation becomes:

$$Voc = \frac{nkT}{q} \ln\left(\frac{J_L}{J_o} + 1\right) \quad (2.6)$$

Where: J_L = Light generated current density

J_o = Saturation current density

The saturation current I_o relates to the amount of recombination in a cell since as I_o increases, the current of the cell drops:

$$I = I_L - I_0 \left[\exp\left(\frac{qV}{nkT}\right)\right] \quad (2.7)$$

The open circuit voltage is thus an indicator to the amount of recombination in the cell. A material with a large band gap has a lower minority carrier concentration and therefore the chances of recombination are lower. Therefore a cell with a larger band gap will have a larger open circuit voltage. This is demonstrated in fig.2.5. From the plot in fig.2.5 silicon (Eg of 1.12eV) has a maximum Voc of 0.7V. Such a high open circuit voltage would be found using high purity silicon substrates.

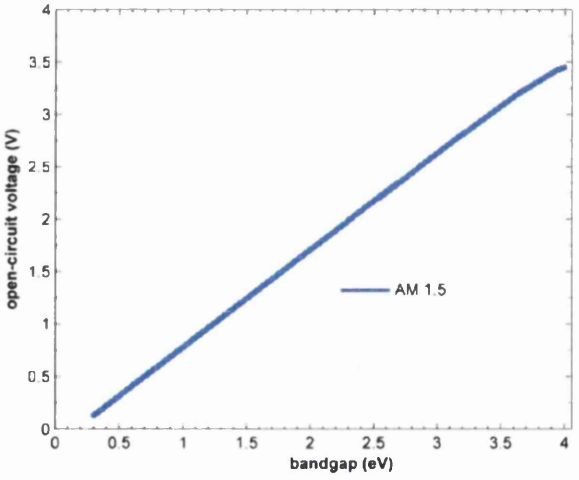


Figure 2.5: Open circuit voltage with respect to band gap energy

2.2.3 Fill Factor (FF)

The fill factor is a ratio of the power that can actually be obtained from a cell in relation to the maximum power derived from the Isc multiplied by the Voc. The closer the FF is to unity the better performing a solar cell will be.

Therefore the equation for FF is typically derived as:

$$FF = \frac{(I_{MP})(V_{MP})}{(I_{SC})(V_{OC})} \tag{2.8}$$

Where: V_{MP} is the voltage at the measured maximum power

I_{MP} is the current at the measured maximum power

The fill factor of a solar cell is strongly affected by recombination and ohmic resistances [9].The fill factor of a cell can be determined graphically by plotting the $I_{sc}V_{oc}$ and $I_{MP}V_{MP}$ and then finding the ratio of the area under each trace (fig.2.6)

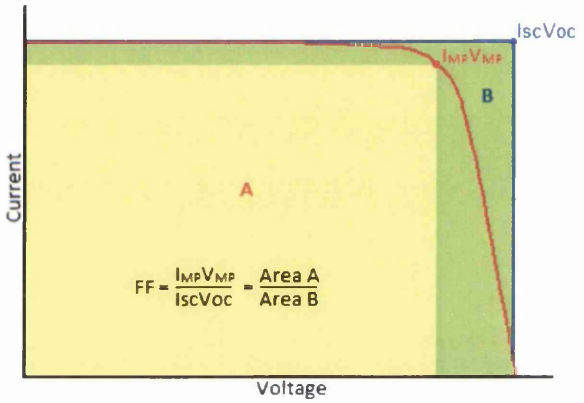


Figure 2.6: Graphical plot of finding the fill factor of a solar cell

From analysing the parameters that make up the efficiency equation, the importance of each can be seen on the efficiency of a cell.

Looking again at the equation for efficiency:

$$\eta = \frac{(Voc)(Isc)(FF)}{Pin} \tag{2.9}$$

An increase in the Voc, Isc or FF will relate to an increased efficiency. Each of the three parameters is affected by a different set of conditions related to the cell. Recombination and other loss mechanisms resulting from optical and ohmic issues ultimately reduce these parameters and hence efficiency. For simplicity, the loss mechanisms have not been fully described in this chapter. Loss mechanisms will be fully analysed in the relevant sections of the following chapter (Chapter 3).

2.3 Silicon for Solar Cell Applications

2.3.1 Properties of silicon

Silicon has long been widely used and favoured for solar cell fabrication. The reason for this is not because it is the best material for such an application, but rather it is a material of which we have great knowledge due to its extensive use in the semiconductor industry. Manufacturing of silicon through to cell processing has been done so on the back of the wealth of information that has come from the microelectronics industry. Silicon is a semiconductor material that has the following interesting properties:

- Silicon is abundant, making up over a quarter of the Earth's crust by mass
- Intrinsic high quality pure semiconductor
- Has a melting point of 1414^{o}C
- Is an indirect band gap material
- Has a band gap of 1.12eV (absorbs in the visible spectrum)

Two important properties listed above for silicon in relation to solar cells include the band gap of the material and the indirect band gap nature of the material. From fig.2.7, as silicon has a band gap of around 1.12eV, this translates into a silicon solar cell only being able to absorb wavelengths shorter than 1100nm. When comparing the Si absorption spectrum to that of what is available, it is easy to see that silicon absorbs over a relatively small area compared to what is available from the sun. The fact that silicon is also an indirect band gap material limits the material as an ideal candidate for solar cells. In such an indirect band gap material, the absorption co-efficient is relatively small (compared to direct band gap materials) hence light must penetrate deeper into the material before it can be absorbed [10].

Despite the drawbacks of silicon as an ideal photovoltaic material, it's simple processing and low cost production, continues to make it the number one commercially adopted technology. Industrial cells are now capable of an efficiency of more than 20% [11] with laboratory produced cells edging ever closer to the theoretical efficiency limit of 29.8% [12].

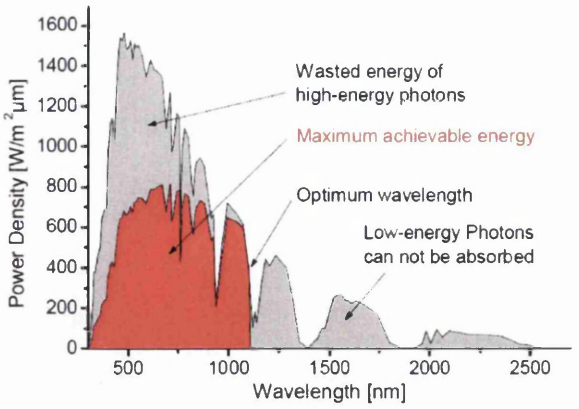


Figure 2.7: Absorption of a silicon solar cell compared to the solar spectrum [13]

2.3.2 Types of Silicon Wafer

Silicon solar cells require high purity substrates for efficient cells. Production often begins with the reduction of silicon oxide and carbon in an arc furnace to produce metallurgical grade silicon (99.0wt% Si) [14]. The metallurgical silicon is still not pure enough and must be further purified to create polysilicon. Polycrystalline silicon can be thought of as semi-crystalline silicon which is next turned into mono-crystalline ingots (by Czochralski crystal growth) or into larger multi-crystalline ingots (by directional solidification) [15]. The result is either the formation of monocrystalline silicon or multi-crystalline silicon which together account for nearly all the silicon solar cells produced. The difference between the two silicon materials differs in quality and therefore cost.

Fig.2.8 shows the difference in the structure of monocrystalline and multicrystalline silicon. Monocrystalline silicon has an ordered single crystal structure, with each atom ideally lying in a pre-ordained position [16]. Multicrystalline silicon on the other hand has regions of crystalline silicon separated by grain boundaries [16]. Because of the grain boundaries that exist in multicrystalline silicon, solar cells produced from such a material exhibit lower efficiencies to that of a cell made from a monocrystalline silicon substrate.

Although not strictly wafer based, other forms of silicon exist such as amorphous silicon (a-Si). Amorphous silicon has an irregular arrangement of atoms unlike the substrates mentioned above, and typically produces lower efficiency solar cells.

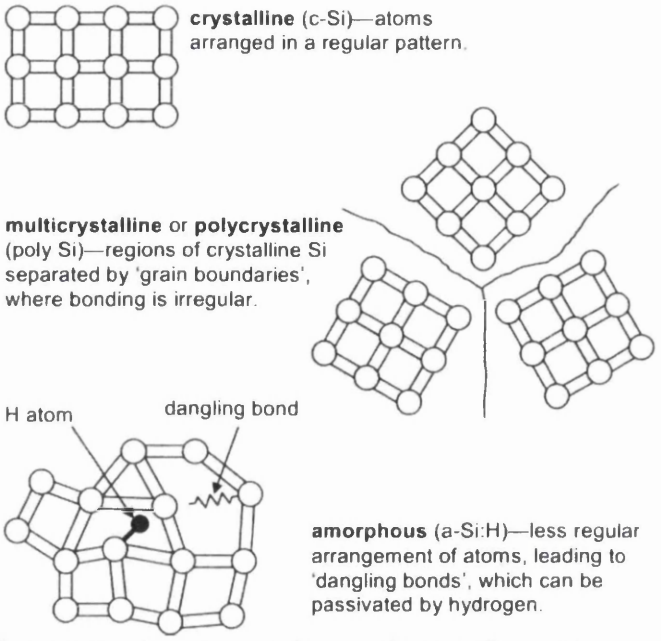


Figure 2.8: Crystal structure of monocrystalline, multicrystalline and amorphous silicon [16]

2.4 Wafer Based Silicon Solar Cell Topologies

Commercially available wafer based crystalline silicon solar cells typically adopt the form of the schematic in fig.2.9. This is referred to throughout this work as a conventional silicon solar cell due its overwhelming popularity. The popularity of the cell is mainly due to cost versus efficiency criteria. Such cells can offer efficiencies close to 19% [17] with a cost per watt of just $0.39 (USD) [18], due to the relatively simple processing steps required for such topographies.

A conventional solar cell structure (fig.2.9) is created by a number of difference processes. Full details on the construction and material choice for a conventional silicon solar cell will be given in the forthcoming chapters (Chapters 3 and 4). In brief, the main areas of a conventional cell include:

- P-N junction: The p-n junction of a silicon solar cell is produced using a p-type base substrate into which an n-type emitter layer is diffused. As previously discussed in this chapter the p-n junction is responsible for the photovoltaic effect.
- Anti reflective top surface: Silicon typically is highly reflective which would normally reflect the light away from the cell. To minimise reflection, the surface of the cell is textured onto which an anti reflective coating (ARC) is applied. The ARC layer used for conventional solar cells is almost exclusively silicon nitride (SiN). This ARC layer is also used to minimise the surface recombination of the emitter layer [19], hence this type of cell can also be known as a Passivated Emitter Solar Cell (PESC).
- Front Contact: The front contact of a cell is typically formed in a grid type pattern to keep shading losses to a minimum. Silver is used due to its good electrical properties and contact to the n-type emitter layer. The front contact has two roles. The first is to collect carriers from the cell to be delivered out to an external circuit. The second is to allow for external connections to be applied in order to connect the cells to one another or directly to a load. Tabbing wire is typically used to provide these external connections, which is simply a flat tinned wire than can easily be soldered onto the front silver contact. To allow for soldering of the front tabbing wire, conventional cells have slightly thicker 'busbar' front contacts to cope with the high temperature (250°C) of the soldering process.
- Rear Contact: The back contact of a cell has three functions, to provide an electrical contact out of the cell, to allow for external connection and to provide a back surface field (BSF). As light is not incident on the rear of the cell, the back contact can be a large scale block contact. The contact provides a back surface field (BSF) which essentially provides a higher doped region at the rear of the cell that

minimises rear surface recombination. The BSF repels carriers away from the rear cell surface where they could otherwise recombine.

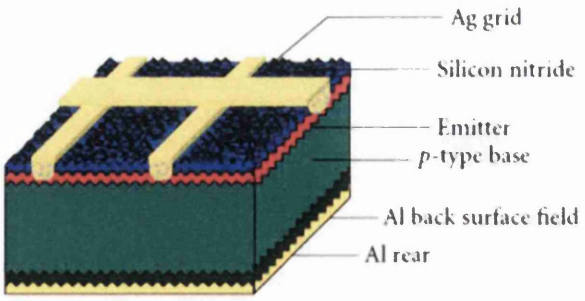


Figure 2.9: Schematic of a conventional silicon solar cell [20]

Several crystalline silicon solar cell topographies exist other than the conventional design previously described. The main drawback of these other technologies is that they often require more advanced processing conditions which increase the cell cost. The advantage of higher efficiency however, means that in some limited applications, higher powered cells are required even if they cost more per watt. A real world example is for domestic installations where one is limited by roof space on a property. For this application, higher efficiency cells allow for a larger installation on the same area of roof space.

Below are some of the main alternative silicon wafer based cell topologies that are currently under investigation, two of which (HIT and BJ) [21] are currently in commercial production.

2.4.1 PERC (Passivated Emitter and Rear Cell)

The passivated emitter and rear cell design is shown in fig.2.10. The topography is very similar to that of a conventional solar cell but uses a dedicated rear passivation layer, patterned to allow for point contact of the rear aluminium electrical contact to the silicon base material. The addition of a rear passivation layer reduces rear surface recombination more than a BSF alone, and the layer also acts as an ARC thereby causing high internal reflection if the cell is sufficiently thin [22]. The enhancements that the cell topography creates allow for efficiencies higher than that of a conventional cell at around 19.3% [17].

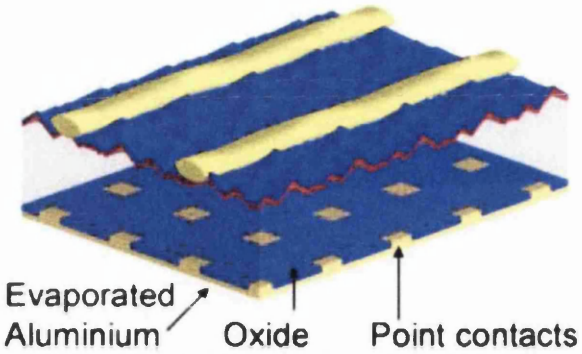


Figure 2.10: Schematic of a PERC (Passivated Emitter and Rear Cell) silicon solar cell [17]

2.4.2 PERL (Passivated Emitter Rear Locally-diffused) silicon solar cell

A passivated emitter rear locally-diffused silicon solar cell is designed to improve on the capability of a PERC cell previously described. A schematic of the cell structure is shown in fig.2.11. The cell topography differs only slightly to that of a PERC cell by the creation of rear local diffused p+ regions where the aluminium contacts the cell. In the PERC cell, the areas where the evaporated aluminium contacted the cell had no passivation layer, but the addition of a BSF in these areas, as in a PERL cell, overcomes the passivation issue [23]. The PERL cell essentially enhances the rear passivation of both a conventional cell and a PERC cell in order to minimise rear surface recombination in a silicon solar cell. Such developments have led to recent PERL cells being 25% efficient [11].

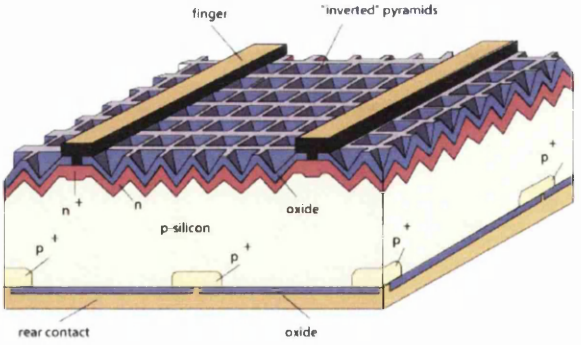


Figure 2.11: Schematic of a PERL (Passivated Emitter Rear Locally-diffused) silicon solar cell [24]

2.4.3 Back contact solar cells

As the PERC and PERL cells have been optimised for rear cell surface enhancements, back contact solar cells are focused upon improving the front of a silicon solar cell. Back contact cells typically demonstrate efficiencies around 20% [25]. Solar cells that fall into this category are grouped into three areas:

1. MWT (Metal Wrap Through)
2. EWT (Emitter Wrap Through)
3. BJ (Back Junction)

2.4.3.1 MWT (Metal Wrap Through) Solar Cell

The metal wrap through solar cell is shown schematically in fig.2.12. It has largely the appearance of a conventional solar cell, although there is one big difference which is that the front and rear electrical contact points are on the rear of the cell. In a practical application, a conventional cell is connected to, at both the front and rear of the cell using tabbing wire. The connection to the rear contact is not an issue, but the external connection to the front contact most certainly is. This is because a sufficiently large front contact busbar is required to solder the tabbing wire onto. If the contact is too thin and narrow, the thermal stresses caused during the soldering process will ruin the contact [26]. Making the contact large enough to cope with such stresses, unavoidably shades the cell which in turn reduces the efficiency. The structure of the metal wrap through cell is designed to relieve the issue of having front busbars on the cell. Instead a series of holes is laser drilled through the cell which allows for the front electrical contact to be accessed on the back of the cell. Since the rear of the cell does not have any constraints in regard to shading losses (as light is only incident on the front), large electrical busbars can be fabricated.

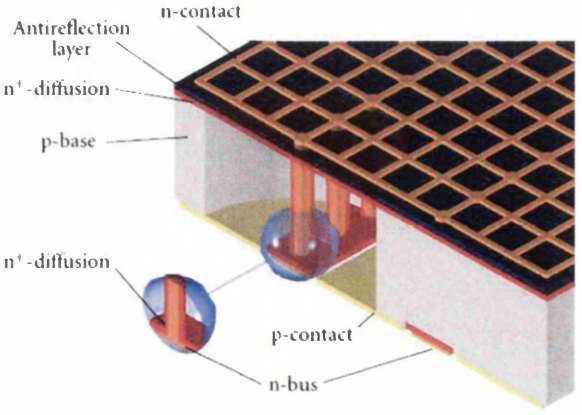


Figure 2.12: Schematic of a MWT (Metal-Wrap-Through) Solar Cell [27]

2.4.3.2 EWT (Emitter Wrap Through) Solar Cell

The emitter wrap through solar cell is shown schematically in fig.2.13. The structure addresses the same issues that the MWT cell was designed to improve. This time however instead of only moving the front electrical busbars to the rear of the cell (as in the MWT), the entire front contact including the silver gridlines are moved to the back. Having no front contact on the surface of a cell improves the area of the cell to which light can enter compared to a conventional cell that can have shading losses as high as 10 to 15% [28]. The cell still employs the use of a top n-type emitter, but it is attached to the bottom by a series of small pathways that run through the cell. By this mechanism, the EWT cell performance is over a wide range nearly independent of the cell thickness to diffusion length ratio [26].

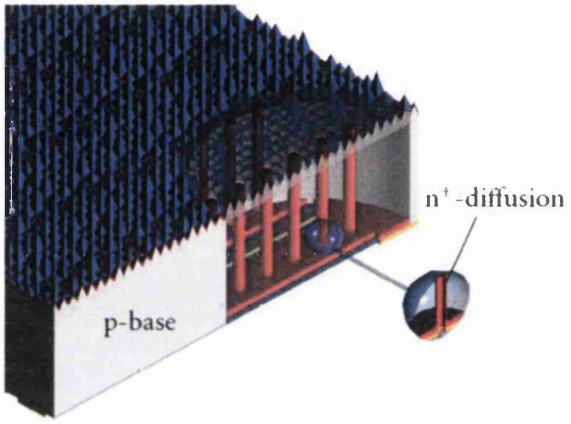


Figure 2.13: Schematic of a EWT (Emitter-Wrap-Through) Solar Cell [27]

2.4.3.3 BJ (Back Junction) Solar Cell

Back junction solar cells as shown in fig.2.14, not only have both sets of contacts at the rear of the cell, but also have the emitter base junction located there also. By having the junction at the rear of the cell, electron–hole pairs are generated in a high-lifetime bulk region within the bulk silicon near the rear of the cell, and are collected at interdigitated diffused junctions on the rear side of the cell [26]. The absence of metallisation from the front of the cell as in EWT cells, allows for more light to enter the cell. The biggest advantage of this topography is that there is no need to conduct the current along the emitter as with front-contacted cells, hence there is no trade-off between series resistance and grid shading and the rear junction can be optimised in terms of the lowest saturation current only [26].

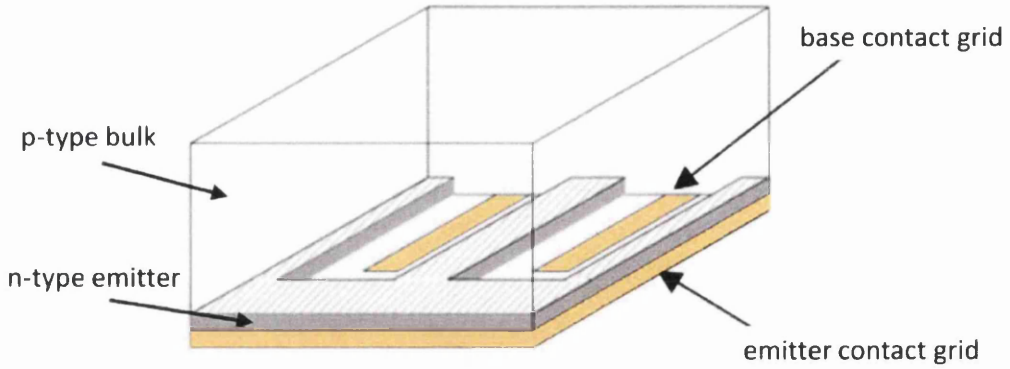


Figure 2.14: Schematic of a BJ (Back Junction) Solar Cell [26]

2.4.4 LGBG (Laser Grooved Buried Grid) Solar Cell

From the previous rear contact cell designs, the main focus was to reduce the front contact area of the cell without degrading efficiency or creating additional problems related to cell interconnection. Another quite different approach to reducing metallisation shading losses is incorporated in the design of a laser grooved buried contact cell as shown in fig.2.15. In the design of such a cell, the metal gridlines are buried inside the substrate by creating laser grooves (contacts lie flush with the top of silicon surface whilst retaining a large contact area). A selective emitter is also produced following the contour of the groove. The burying of the contacts allows for a larger area of contact to be used so that contact resistance is reduced without increasing shading loss [21]. In fact the structure actually allows for a shading loss reduction from 10 to 15% in a conventional cell to only 2 to 3% in a LGBG device [28]. Such cells have achieved an efficiency of 17.5% under standard AM1.5 conditions but have achieved over 19% when used with 50x concentration of light [29]. Because of the increased contact despite lower shading effects, LGBG solar cells are often used with light concentration to further enhance their electrical power output.

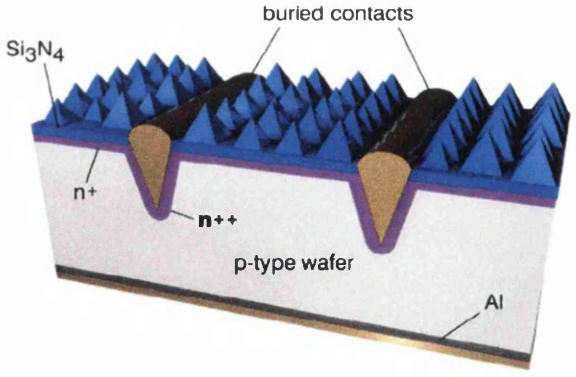


Figure 2.15: Schematic of a Laser grooved buried grid (LGBG) silicon solar cell [30]

2.4.5 HIT Solar Cell

The heterojunction with intrinsic thin layer solar cell originally developed by Sanyo is not strictly a typical wafer based silicon solar cell, but is included here due to its ever increasing popularity due to attractive efficiencies of 24.7% [11]. The HIT cell schematic (fig.2.16) is different in several ways to that of a conventional wafer based silicon solar cell. The use of an amorphous silicon (a-Si) emitter layer and additional intrinsic a-Si junction are the main differences along with a transparent conducting oxide film on the top of the cell. By inserting the high-quality passivation intrinsic a-Si layer, the defects on the c-Si surface can be effectively passivated, and a higher Voc can be obtained [31]. The a-Si layer also enhances the absorption capabilities of the cell due to the different band gap it possesses. Being able to effectively absorb over a greater wavelength range ultimately relates to a higher possible efficiency.

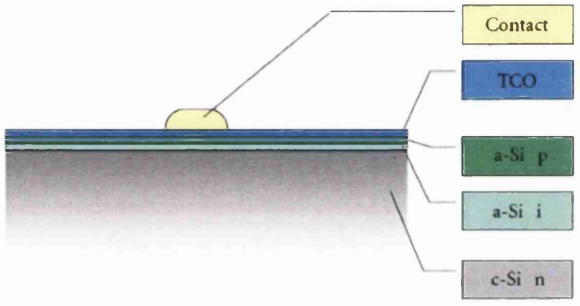


Figure 2.16: Schematic of a HIT (Heterojunction with Intrinsic Thin layer) Solar Cell [27]

[1] Pveducation.org. 2013. Intrinsic Carrier Concentration | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/pn-junction/intrinsic-carrier-concentration [Accessed: 4 Sep 2013

[2] Pveducation.org. 2013. Solar Cell Structure | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/solar-cell-operation/solar-cell-structure [Accessed: 6 Sep 2013]

[3] Pveducation.org. 2013. The photovoltaic effect | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/solar-cell-operation/photovoltaic-effect [Accessed: 6 Sep 2013]

[4] Pveducation.org. 2013. Short-Circuit Current | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/solar-cell-operation/short-circuit-current [Accessed: 6 Sep 2013]

[5] J.F. Randall, J. Jacot, Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra, Renewable Energy, Vol.28, Issue 12, P1851-1864, 2003

[6] Keller, S.; Spiegel, M.; Fath, P.; Willeke, Gerhard P.; Bucher, E., "A critical evaluation of the effective diffusion length determination in crystalline silicon solar cells from an extended spectral analysis," Electron Devices, IEEE Transactions on , vol.45, no.7, pp.1569, 1574, 1998

[7] Pveducation.org. 2013. Open-Circuit Voltage | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/solar-cell-operation/open-circuit-voltage [Accessed: 6 Sep 2013]

[8] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, Second Edition, John Wiley & Sons, 265-313, 2011].

[9] Khanna, A.; Mueller, T.; Stangl, R.A.; Hoex, B.; Basu, P.K.; Aberle, A.G., "A Fill Factor Loss Analysis Method for Silicon Wafer Solar Cells," Photovoltaics, IEEE Journal of , vol.3, no.4, pp.1170,1177, Oct. 2013

[10] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, John Wiley & Sons, 61-112, 2003

[11] Green, M. A., Emery, K., Hishikawa, Y., Warta, W. and Dunlop, E. D, Solar cell efficiency tables (version 43),Prog. Photovolt: Res. Appl., 22: 1–9, 2014

[12] Tiedje, T.; Yablonovitch, E.; Cody, G.D.; Brooks, B.G., "Limiting efficiency of silicon solar cells," Electron Devices, IEEE Transactions, vol.31, no.5, pp.711-716, 1984

[13] Comprehensive Renewable Energy, Ali Sayigh, Oxford Elsevier, 2012

[14] Jafar Safarian, Gabriella Tranell, Merete Tangstad, Processes for Upgrading Metallurgical Grade Silicon to Solar Grade Silicon, Energy Procedia, Vol.20, 88-97, 2012

[15] Green MA. Silicon solar cells: state of the art. Phil. Trans. R. Soc. A 371, 2013

[16] Stuart R. Wenham, Martin A. Green, Muriel E, Applied Photovoltaics, 3rd Edition Routledge, p32, 2012

[17] Schultz, O., Mette, A., Hermle, M. and Glunz, S. W., Thermal oxidation for crystalline silicon solar cells exceeding 19% efficiency applying industrially feasible process technology. Prog. Photovolt: Res. Appl., 16: 317–324, 2008

[18] Pv.energytrend.com. 2013. Price Quotes_EnergyTrend PV. [online] Available at: http://pv.energytrend.com/pricequotes.html [Accessed: 23 Dec 2013

[19] Cuevas, A.; Kerr, M.J.; Schmidt, J., "Passivation of crystalline silicon using silicon nitride," Photovoltaic Energy Conversion, 2003. Proceedings of 3rd World Conference on, vol.1, no., pp.913,918 Vol.1, 18-18, 2003

[20] Dirk-Holger Neuhaus and Adolf Münzer, "Industrial Silicon Wafer Solar Cells," Advances in OptoElectronics, vol. 2007

[21] Schultz, O. *et al*, High-efficiency solar cells with laser-grooved buried contact front and laser-fired rear for industrial production, Proc. 21st EU PV Solar Energy Conf, 826-829, 2006

[22] Myungsu Kim, Sungchan Park, Dongseop Kim, Highly efficient PERC cells fabricated using the low cost laser ablation process, Solar Energy Materials and Solar Cells, Vol.117, 126-131, 2013

[23] Zhao, J.; Wang, A.; Green, M.A., 24% efficient PERL structure silicon solar cells, Photovoltaic Specialists Conference, 1990., Conference Record of the Twenty First IEEE , vol.1, 21-25, 333-335 1990

[24] Pveducation.org. 2013. High Efficiency Solar Cells | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/manufacturing/high-efficiency [Accessed: 6 Jul 2013]

[25] Hendrichs, M. Cost-optimized metallization layout for metal wrap through (mwt) solar cells and modules, 28th European PV Energy Conference, 2013

[26] Kerschaver, E. V. and Beaucarne, G., Back-contact solar cells: a review. Prog. Photovolt: Res. Appl., 14: 107–123, 2006

[27] S. W. Glunz, "High-Efficiency Crystalline Silicon Solar Cells," Advances in OptoElectronics, vol. 2007

[28] Pveducation.org. 2013. Buried Contact Solar Cells | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/manufacturing/buried-contract [Accessed: 6 Jul 2013].

[29] Cole, A., *et al*, Silicon Based Photovoltaic Cells For Concentration-Research And Development Progress In Laser Grooved Buried Contact Cell Technology, AIP Conference Proceedings;, Vol. 1407, Issue 1, p46, 2011

[30] Cole, A., *et al*, Technological and financial aspects of laser grooved buried contact silicon solar cell based concentrator systems, 2nd International Workshop on Concentrating Photovoltaic Optics and Power, 2009

[31] Yasufumi Tsunomura. 2013. [online] Available at: http://us.sanyo.com/dynamic/LinkListingItems/Files/solarPower_22_3_Cell_Efficiency_White_Paper_Dec_07-1.pdf [Accessed: 6 Jun 2013].

Chapter 3: Literature Review

3.1 Thin Crystalline Silicon

In order for photovoltaic (PV) generated electricity to compete against the cost of conventional fossil fuelled energy, substantial cost reductions are still required despite the recent drop in solar cell prices. Currently, silicon PV cells dominate the solar electricity systems market with a 90% share [1]. The cost of the silicon starting material for such devices totals 50% of the cost of the entire cell [2]. It is imperative therefore that the amount of silicon be kept to a bare minimum in order to produce efficient low cost solar cells. A minimum silicon substrate thickness of 40μm is required in order to obtain the maximum theoretical possible efficiency from a cell [3]. This is because most of the optical absorption in a silicon solar cell takes place within the first 30μm of the substrate [4], which can be seen from fig.3.10 in 3.2.1.2. It is important to note however, that decreasing the thickness of a cell reduces the optical path length of the light (distance light can travel inside the cell) and therefore light trapping methods are very important. In theory by having ideal Lambertian light trapping, the optical path length can be increased by 50 times leading to efficiencies of 26% from a 1-μm-thick cell [5]. In fact by optimising light trapping, Chutinan *et al* [6] produced a 20 μm thick c-Si with an efficiency of 21.3% which without trapping would be significantly lower. Having thin cells not only reduces cell cost but a thin cell leads to reduced bulk recombination, hence a higher possible Voc, FF and efficiency.

Commercially, crystalline silicon wafers are cut from solid ingots almost exclusively using wire sawing technology. Wire sawing processes create a lot of waste material from the cutting of silicon. Such waste is often referred to as kerf-loss, and can be as much as 50% of the material consumption (cut one wafer, lose another as waste scenario). Since the mainstream arrival of silicon wire sawing in the mid 1980's [4], the thickness of wafers produced have continued to fall, these days wafers around 180μm are common [5]. Despite continued developments in thinner wire and state of the art abrasives, alternative techniques have emerged to produces thinner silicon substrates that wire sawing alone, would be unable to produce. Such methods include:

- Deposition of silicon onto a substrate
- Wafer layer transfer processes
- Silicon wafer etching
- Cleaving away a layer of the silicon wafer

As this work focuses around wafer based silicon solar cells, further investigation will be focused around thin c-Si wafer based techniques.

3.1.1 Layer transfer processes

Layer transfer processes typically involve epitaxial deposition/growth of polycrystalline silicon on a monocrystalline silicon substrate. Simply growing the layer on the surface of a standard wafer would prove difficult for subsequent detachment of the layer after growth. Novel processes have been developed to create boundary layers which can aid in the removal and will be covered here. Layer transfer processes developed include:

- VEST (via hole etching for the separation of thin films): The VEST structure is shown schematically in fig.3.1. Epitaxial growth of silicon is performed onto the surface of an oxidised silicon wafer. Holes through the epitaxial layer allow for subsequent etching of the SiO_2 layer thereby detaching the silicon film [7].

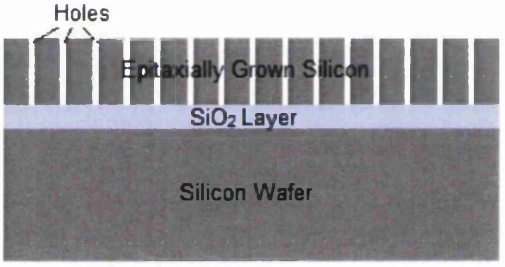


Figure 3.1: Schematic of VEST structure

- Porous Silicon weakening layers: A porous silicon layer is formed on a wafer which essentially is a weak silicon layer due to empty voids. Depositing a silicon layer on top of such a weak substrate enables the PSi layer to be removed, detaching the deposited silicon layer. Issues around epitaxial growth on such a porous layer have been overcome by novel approaches such as the ELTRAN (epitaxial layer transfer) process [8]. In the process (shown if fig.3.2), the top of c-Si surface (10μm) is converted into porous silicon (PSi). Oxidisation inside the pores allows for only the top surface of the PSi layer to close up during a high temperature annealing step. Epitaxial growth is then performed on the closed up PSi top surface. In the next step, the back of the wafer is ground down up to the porous silicon layer. Etching is then performed which removes the porous silicon layer quicker than the epitaxial grown layer. The result is a thin film epitaxial wafer.

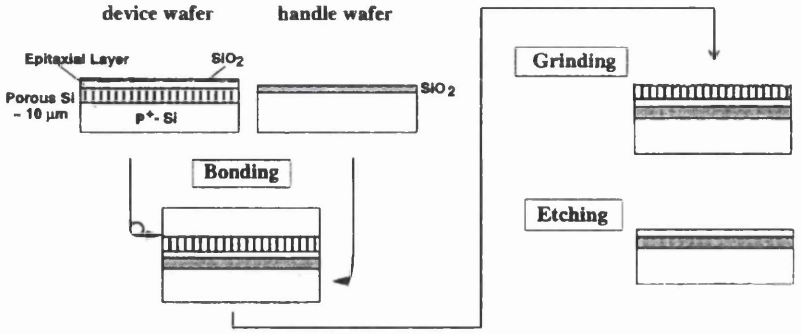


Figure 3.2: Schematic process flow of ELTRAN [8]

- TIPT (thermal-stress induced pattern transfer): This technique enables an epitaxial grown silicon layer to be removed from the substrate using a metallic layer [9] as shown in fig.3.3. The difference in thermal expansion co-efficient between a metallic paste and the substrate onto which the layer was grown, allows for detachment of the layer after a heating cycle. Essentially during the annealing cycle, the metallic layer bonds to the epitaxially grown silicon. Upon cooling the difference in thermal expansion between the metallic layer and the substrate wafer, causes the metallic layer (bonded to epitaxial silicon) to detach from the substrate.

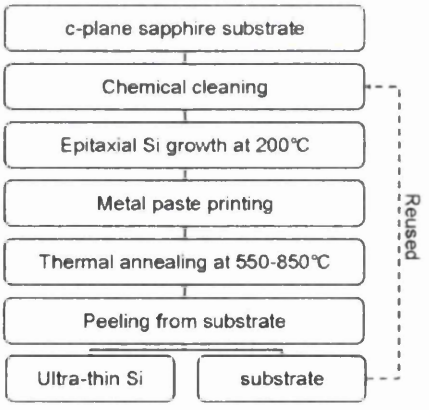


Figure 3.3: Schematic process flow of TIPT [9]

3.1.2 Etching

Etching techniques have long been investigated to create thin silicon substrates, although etching uniformity and duration have proved troublesome. Some techniques have emerged however that can overcome these barriers.

- Sliver cell concept: The sliver cell concept makes use of the alkaline etch selectivity for (100) surfaces to form deep narrow grooves in suitably masked wafers oriented such that a (111) plane is perpendicular to the wafer surface [10]. The result is the fabrication of thin silicon strips as shown in fig.3.4.

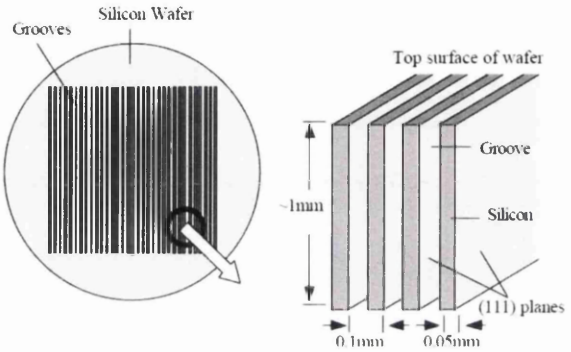


Figure 3.4: Schematic of the Sliver cell process [10]

- Silicon millefeuille: Meaning one thousand layers of silicon, is a process similar to that of the Sliver cell concept but instead porous silicon structures are created using a lithography mask. Subsequent high temperature annealing creates the millefeuille structure as shown in fig.3.5 [11].

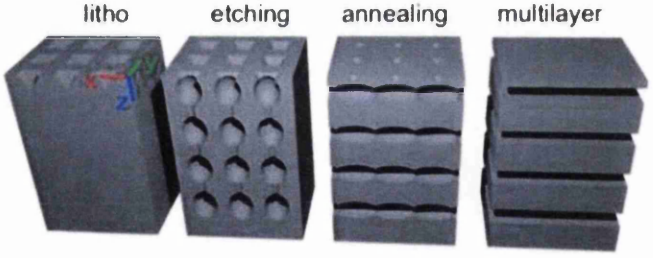


Figure 3.5: Schematic of the silicon millefeuille process [11]

- Magnetically guided etching: The process of magnetically guided etching works on the principle of metal assisted etching. This technique however uses magnetic layers in between the noble metallic layers so that etching under the noble metal layer can be steered by moving a magnet [12]. The schematic of the process is shown in fig.3.6.

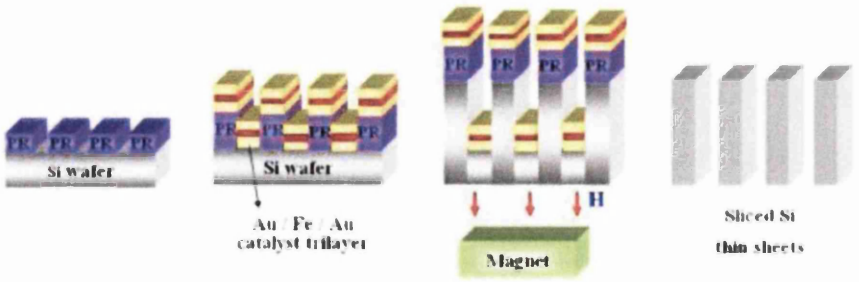


Figure 3.6: Schematic of the magnetically guided etching process [12]

3.1.3 Silicon Cleaving

Silicon cleaving processes potentially allow for a standard 600μm thick silicon wafer to produce several solar cells. Essentially the techniques adopted, allow for detachment of thin silicon foils from a wafer. Despite its excellent potential for low cost solar cell substrates, few methods exist which are simple and cost effective.

- SC (Smart cut): Ions are implanted into a c-Si wafer at a specified depth. High temperature annealing processes causes voids created by ion implantation, thereby cleaving the wafer to the desired thickness [13].
- PSi (Porous silicon) weakening layer: Similar to the method for epitaxial layer removal, a PSi layer can be etched into a silicon wafer by chemical etching techniques. As the layer is weak it can be detached from the substrate by methods such as bonding it to another substrate and simply pulling it away [14].
- Exfoliation: Silicon exfoliation is a very promising technique recently developed, that allows for thin c-Si foils to be exfoliated from a parent wafer using simple processing equipment. There are two main techniques being researched which are quite similar to one another:
    - Slim-Cut (**S**tress induced **l**iftoff **m**ethod): The slim cut process is another kerf loss free process of producing thin silicon substrates. Originally developed by IMEC, it is similar to the TIPT method in that a screen printable metallic paste is used. Instead of using the thermal mismatch to pull away an epitaxial grown layer, the slim-cut method uses the stress induced to exfoliate a layer from a monocrystalline silicon substrate [15-17]]. The schematic of the Slim-cut process is shown in fig.3.7. The process adopts simple screen printing and firing techniques that already exist as part of standard silicon solar cell production. Solar cells processed from 50μm thick cells with no additional processing have already achieved 10% conversion efficiency [15].

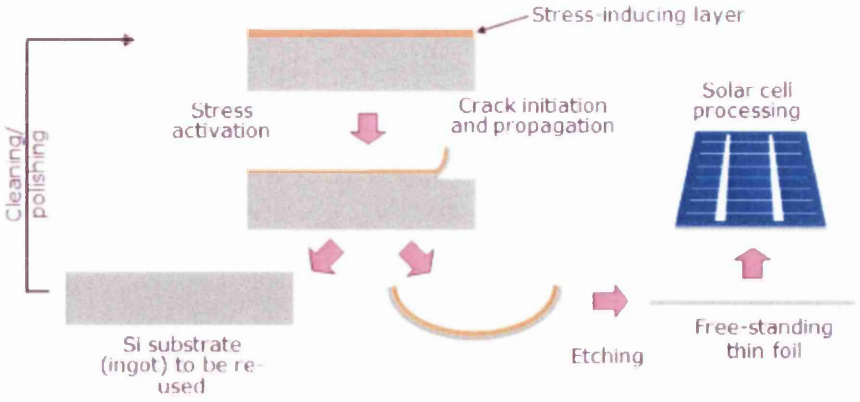


Figure 3.7: Schematic of the Slim-Cut Process [16]

- SOM (Silicon on metal): The SOM method is very similar to that of Slim-Cut but relies upon the electrochemical deposition of a metallic foil as well as the incorporation of hydrogen into the silicon during plating [18]. Once again the thermal expansion mismatch between the materials is used to create thermal stress during a heating and cooling step to exfoliate a silicon layer [19]. A schematic of the process is shown in fig.3.8. Un-optimised silicon heterojunction cells processed using 25µm substrates achieved 13.5% efficiency [20]. Little detail is given in the literature concerning the effect of the hydrogen incorporation during the plating process. It is most likely used as an implantation layer to aid in the cleaving process.

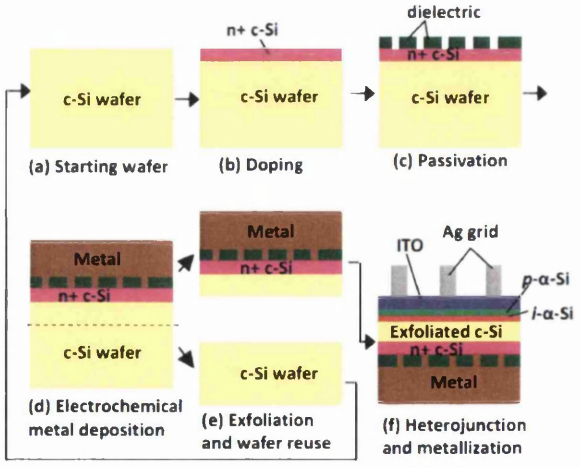


Figure 3.8: Schematic of the SOM Process [20]

3.1.4 Summary

From the review into methods of producing thin wafer based crystalline silicon substrates, several techniques have been analysed. The reduction of silicon material used for cell production can bring about significant cost savings, due the cost of the starting substrate. Multi-wire sawing is commercially used to produce silicon solar cell substrates around 180μm thick. Due to the 'cut one, lose one' kerf loss issue, much of the material is being wasted by the process. The diameter of the wire ultimately dictates the kerf loss and this technique is struggling to produce wafers thinner than those currently produced (180μm).

Several methods have been developed to produce thin silicon substrates using alternative techniques to that of conventional wire sawing. Processes that deposit epitaxial silicon have emerged, although expensive equipment is often required as well as the additional expense of modified carrier wafers. Various etching techniques have been researched and developed to produce thin c-Si foils. The photolithography masks that are often needed, coupled with slow etching rates, once again limits such technology. Cleaving of silicon wafers by ion-implantation involves additional equipment and hence increased costs.

Of all the thin wafer based processes evaluated, the exfoliation of silicon was found to have the best real world potential. The Slim-cut method developed by IMEC uses simple equipment, common to the industry, to produce thin silicon foils. By the simple application of a screen printed metallic layer followed by a high temperature step, thermal stress is induced during cooling which can exfoliate thin foils. Experimental studies developing these wafer exfoliating techniques are reported in Chapter 5.

3.2 Solar Cell Optical Loss

3.2.1 Optical Losses

Optical losses in the area of photovoltaics are an important loss mechanism since cells rely on the absorption of photons and subsequent conversion of this energy into electrical energy. Any light that is not successfully captured by the cell does not contribute to current generation. Since the efficiency of a cell is dependent upon the amount of light energy incident on the cell in relation to energy out, optical losses inherently reduce the efficiency. The three mechanisms for optical losses are related to:

1. Shading by front electrical contacts
2. Reflectivity of the surface of the cell
3. Inefficient or ineffective absorption of photons within the cell

3.2.1.1 Solar Cell shading

The shading effect of the solar cell front contact is a necessary loss which is kept at a minimum. A good electrically performing contact is required which inevitably will cause shading by taking up useful active area of the cell. The contact must be narrow enough to minimise shading losses but wide enough to minimise series losses. The solution is for tall, narrow contacts of very low resistivity to be formed on the cell surface.

3.2.1.2 Solar Cell Reflectivity

The reflectivity of the surface of the cell dictates how much light will be able to enter the cell and have a chance of contributing to light generated current. If the surface of the cell acts as an ideal reflector, the entire incident light will simply be reflected and no current generated. In contrast if the cell is perfectly non-reflective, all the light will pass through into the cell where it has a chance of being harnessed (subject to the band gap of the material used etc). The ideal reflectivity of a cell would be as low as possible over the range of wavelengths a cell can efficiently absorb for electron hole generation. Unfortunately, this is the ideal case; in practise suppression of reflectivity is wavelength dependent.

Reflectivity of the surface of a cell is the largest contributor to reflective losses. Silicon wafers used by the semiconductor industry have a mirror-like polished flat surface which is depicted in fig.3.9. As in a conventional reflective mirror, a large proportion of visible light is reflected. As silicon solar cells are specifically developed to harness energy in the visible

range, such a reflectivity is detrimental to the efficiency of the PV device. Making the surface more matt-like in appearance reduces reflection considerably. For crystalline silicon cells, this is primarily achieved by two methods often used together to further enhance anti-reflective properties:

1. Surface texturing of the silicon substrate
2. Deposition of an Anti Reflective Coating

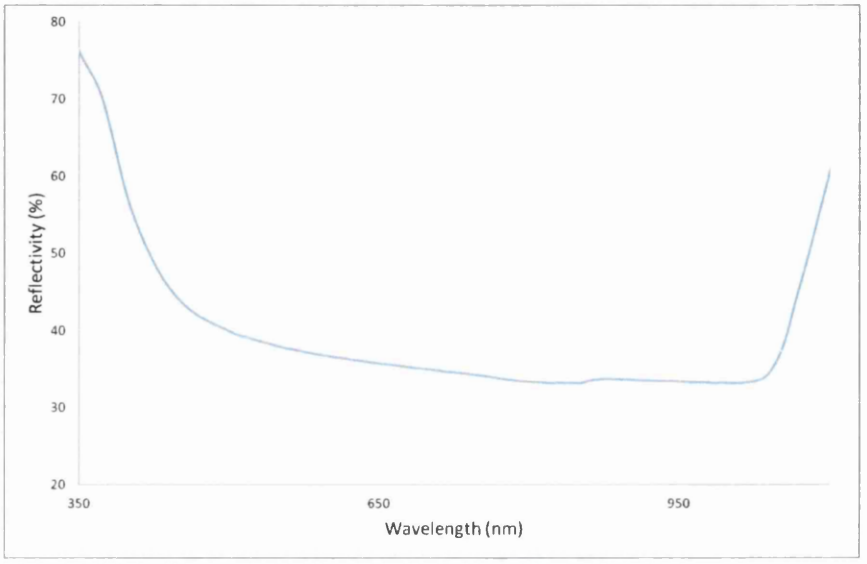


Figure 3.9: Reflectivity of a polished flat silicon substrate

3.2.1.3 Solar Cell Absorption

Absorption in a solar cell is important as it dictates how much of the light that is not reflected from the surface of the cell will actually be absorbed by the cell creating electron hole pairs. The absorption in a cell is dependent upon:

1. The material used to produce the cell
2. The thickness of the solar cell

The material of the solar cell is a spectrally selective absorber meaning that the material used for the cell dictates the photon wavelengths that can be absorbed. The band gap of the material used for the cell is responsible for this. Photons will only be absorbed if their energy is more than or equal to the band gap energy.

The thickness of material is also important for absorption. This is because each wavelength interacts differently with silicon. Some wavelengths penetrate deeper into the material than others before they are absorbed. The depth at which a wavelength will be absorbed by the material is called the absorption co-efficient (denoted by the Greek letter α) and once again is material dependent. Therefore if the cell is too thin some longer wavelengths can pass through the cell without being absorbed. The actual absorption

depth of a specific wavelength can be found by taking the inverse of the absorption co-efficient. Since the absorption depth changes for each wavelength, the depth for a material is stated as the distance into the material at which the light drops to about 36% of its original intensity [21]. The absorption depth of wavelengths for a silicon substrate is shown in Fig.3.10.

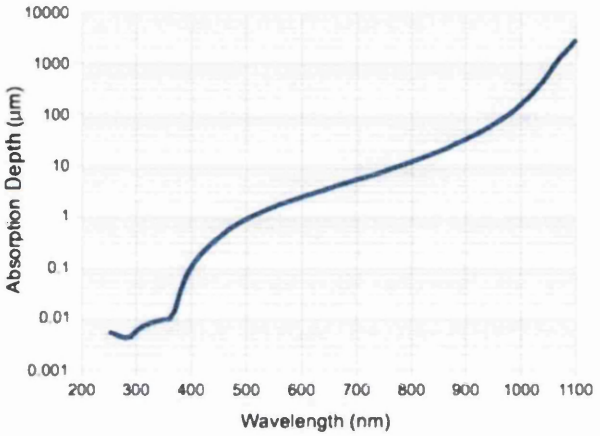


Figure 3.10: Absorption depth for silicon [22]

From fig.3.10 it is apparent that in order to absorb all photons with energy above the band gap (1100nm wavelength and below), the cell would have to be over 1mm thick. Such a thickness is impractical for two reasons:

1. Crystalline silicon is an expensive semiconductor material and using a thick substrate would increase the cost of cells dramatically. The cost of silicon in a typical c-Si solar cell (180µm) can account for up to 50% of the entire cell [23].
2. A light generated carrier is only guaranteed to be absorbed within one diffusion length of the depletion region (p-n junction). Further away from the region the collection probability decreases. Therefore carriers generated deep into the silicon stand little chance of being collected and typically recombine. In fact the minimum required thickness of a c-Si solar cell from theoretical calculations was estimated to be only 40-60µm [24].

Absorption is mostly material related it and ways to theoretically increase the thickness of a cell will be analysed further in relation to anti-reflective techniques. Back reflector techniques can be adopted in a cell to enhance the theoretical thickness of the cell by reflecting light back through the cell off the rear contact, essentially doubling the apparent thickness of the cell.

3.2.2 Reflectivity Suppression

As previously mentioned, the reflectivity of a silicon solar cell is detrimental to its efficiency. Reducing the surface reflectivity is essential to maximise the performance of the cell and suitable methods and materials must be adopted to suppress reflectivity over the spectrum of which the cell can perform. Two methods are commonly used for crystalline silicon solar cells, the application of an anti-reflective coating (ARC) and surface texturing of the substrate. This section will focus upon the theory around both of these techniques in lowering cell reflectivity.

3.2.3.1 Anti Reflective Coatings

An anti-reflective coating is a transparent thin layer of non-absorbing material with a lower refractive index (than that of silicon) on top of the cell that is designed to suppress reflection by deconstructive interference effects [25]. Deconstructive interference occurs when the wave reflected from the ARC is out of phase with the wave reflected from the surface of the silicon substrate as demonstrated in fig.3.11. As the name of the principle suggests, deconstructive interferences results in the waves cancelling each other out, so no reflection occurs.

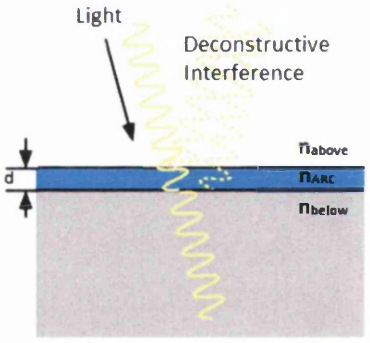


Figure 3.11: ARC deconstructive interference effects

The thickness of an ARC layer is very important in achieving deconstructive interference and the layer must be one quarter of the wavelength of the incident light. The result is that the wave reflected from the silicon substrate travels half a wavelength more than that reflected from the ARC layer so they meet deconstructively. The thickness/depth of the ARC is therefore defined as:

$$d = \frac{\lambda}{4n_{ARC}} \tag{3.1}$$

Where n_{ARC} is the refractive index of the ARC layer

The refractive index of the material must be chosen so that both the waves perfectly cancel each other out. This is determined from the geometric mean of the refractive indices of the materials at both sides of the ARC and therefore defined as:

$$n_{ARC} = \sqrt{n_{above} \times n_{below}} \quad (3.2)$$

Where: n_{above} is the refractive index of the material above the ARC
n_{below} is the refractive index of the material below the ARC

As the above equation returns exact values for the refractive index required, materials should be chosen with a refractive index as close as possible to the one calculated. It is also important to note that as the wavelengths of light changes, so will the thickness calculation for the ARC layer. It is thus impossible to have a perfect ARC for each incident wavelength and in practice it is common to use a wavelength of 600nm for the calculations because this wavelength is close to the peak power of the solar spectrum [25]. As an example, for a crystalline silicon solar cell using a single quarter wave ARC, the required refractive index for the ARC (assuming a cell to air arrangement) would be:

$$n_{ARC} = \sqrt{n_{above} \times n_{below}} = \sqrt{n_{Air} \times n_{Si}} = \sqrt{1 \times 3.5} = 1.87$$

Therefore with an ARC of n_{ARC} = 1.87, the optimum thickness of the ARC using for a wavelength of 600nm would be:

$$d = \frac{\lambda}{4n_{ARC}} = \frac{600}{4 \times 1.87} \approx 80\text{nm}$$

Therefore for the silicon to air interface at 600nm wavelength, the ARC should have a refractive index as close to 1.87 with a depth 80nm. It is important to mention however that solar cells are often mounted into panels so that the silicon no longer has an air interface but now a glass one instead. Repeating the above calculations for a Si to Glass ($n_{glass} \approx 1.5$) interface, an ARC should have a refractive index of 2.29 at a thickness of 66nm, to completely suppress reflectivity at a 600nm wavelength. These values closely match that of a SiN ARC, hence it's widespread use. Fig.3.12 lists the refractive index for several commonly used ARCs. More than one ARC layer can also be used for suppression of reflectivity, however process costs must be considered with respect to enhanced performance.

ARCs	n_{arc}	d_{arc} (nm)
SiO_2	1.4	116
Si_3N_4	2	81
ZnS	2.25	72
ZnO	2	81
MgF_2	1.4	116
TiO_2	2.5	65
SnO_2	1.9	86
SiN_x:H	1.9-2.4	68-86
Por.Si	(1.2-2.2)*	74-135

* For porosity from 52% to 80%

Figure 3.12: Refractive index and related depth of common ARC coatings [26]

3.2.3.2 Light Trapping - Surface Texturing

Deposition of an ARC has been found to be an effective method of suppressing reflectivity. Another method commonly used in silicon photovoltaics is surface texturing. Surface texturing physically makes the surface rougher so there is an increased chance of reflected rays bouncing back onto the surface [27] as shown in fig.3.13. Texturing can also change the path of the light through a cell. Light entering a textured substrate is tilted with respect to the cell normal allowing for photo-generation to take place closer to the p-n junction, leading to enhanced collection efficiency [25].

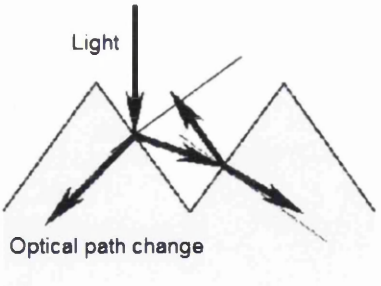


Figure 3.13: Optical effects of surface texturing [25]

The angle at which light is refracted into the cell can be found by rearranging Snell's Law:

$$\theta_2 = \sin^{-1}\left(\frac{n_2}{n_1}\sin\theta_1\right) \quad (3.3)$$

Where: n_1 and n_2 are the refractive indexes of the first and second materials respectively

θ_1 is the angle of incident

For monocrystalline silicon solar cells, the crystallographic planes exposed after KOH etching make the angle of incident 54.7° due to the pyramidal structures that are etched [28]. A typical textured monocrystalline silicon surface is shown in Fig.3.14.

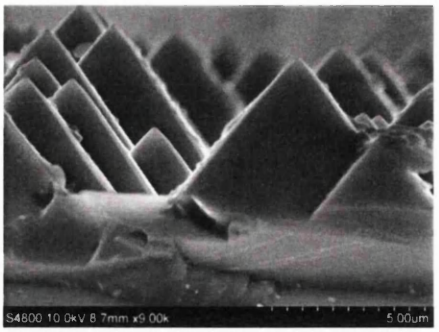


Figure 3.14: SEM of the surface of textured monocrystalline silicon with exposed Si pyramids

Such a structure is formed during isotropic etching of (100) silicon which is used as an industry standard process. Such etching exposes the {111} planes on which the etching rate is lowest [25].The anisotropic etching profile for a (100) silicon wafer is shown in fig.3.15.

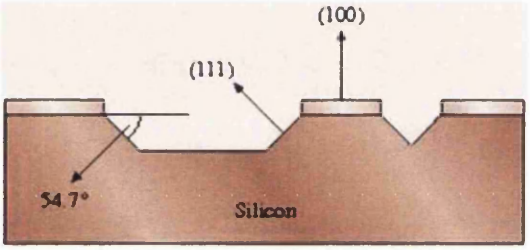


Figure 3.15: Anisotropic etch profile for (100) silicon wafer [29]

Unfortunately the process of texturing increases the likelihood of surface recombination due to the disruption of the silicon lattice and resulting dangling bonds. Fortunately as texturing is often used in conjunction with an ARC, the addition of the ARC layer can help passivated these dangling bonds, especially hydrogen rich nitrides. An ARC can be tailored to serve as not only an anti-reflective coating but also as a passivation layer. The ARC layer essentially ties up all the dangling bonds and reduces surface recombination losses that would have been increased by the texturing process. Some ARC layers are also hydrogen rich and a high temperature anneal after ARC deposition can reduce bulk recombination in the cell as well as surface recombination through hydrogen passivation of defects.

Eli Yablonovitch found that the increase in absorption in a solar cell due to a standard textured surface had a limit [30]. He stated that the absorption could only be increase by a factor of $4n^2$ [30], where n is the refractive index of the semiconductor material. It is important to note that this theory is not applicable with nanoscale structures [31]. Fig.3.16 shows the reflectivity suppression capability of both texturing and the deposition of a silicon nitride ARC, on a silicon substrate. Reflectivity can be suppressed from 30% (polished silicon substrate) to below 5% for a textured silicon substrate applied with a SiN ARC layer.

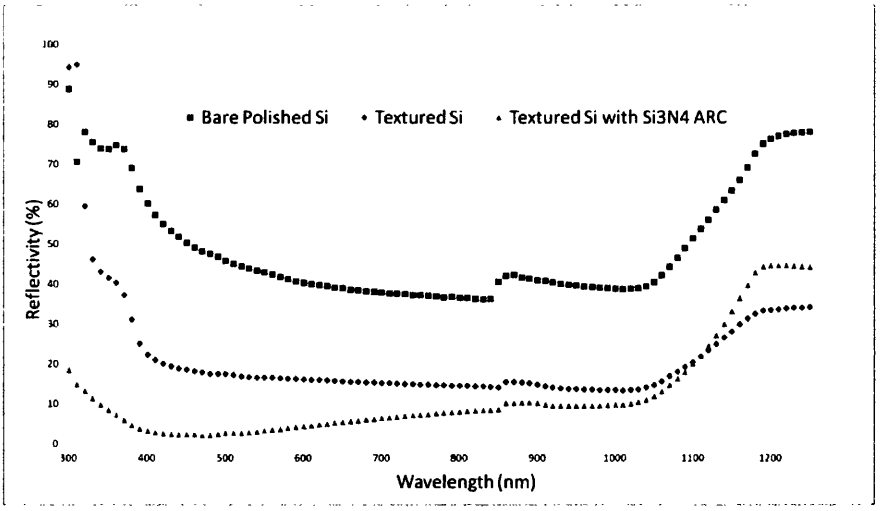


Figure 3.16: Reflectivity suppression of texturing and ARC techniques

3.2.3 Review of Anti-Reflective Technologies

Reflectivity suppression in photovoltaics is a vast research field that continues to grow. As with other reviews conducted for this thesis, the main focus will be around reflectivity suppression for wafer based crystalline silicon solar cells. Despite commercial manufacturers of c-Si cells adopting relativity simplistic anti-reflective techniques, research has provided a wealth of other processes which are often able to reduce reflectivity further. As with all other parameters relating to cell manufacturing, the improvement in cell efficiency must outweigh the extra cost associated with the process.

The review into reflectivity suppression will be separated into two distinct categories: anti-reflective coatings (ARC) and light trapping texturing of silicon. Between the two categories there are cross over technologies, although ARC will include methods that have a strictly deposited layer onto the surface of the cell. The light trapping investigation will deal with techniques that physically modify the surface of the silicon.

3.2.3.1 Anti-Reflective Coatings

Anti Reflective Coatings applicable to crystalline silicon cells range from quarter wavelength coatings (typically used in industry) all the way through to coatings that apply novel nanoscale particles and wires. The main types of ARC coatings are detailed below:

- **Commercially applied coatings**

  Commercially applied anti-reflective coatings for c-Si cells typically employ quarter wavelength technologies. Therefore coatings used have a refractive index as close to 1.87 (for Air to Si) or 3.27 (for Glass to Silicon) as possible. The main coatings adopted are:

- TiO_2/SiO_2: Titanium dioxide ARC layers were among the first used in screen printed cells [32]. As TiO_2 has a band gap close to 2, it is a good material for an anti-reflective coating for silicon solar cells [33]. However, TiO_2 has no surface or bulk passivation properties so it can only be used specifically as an ARC. [32]. Silicon Dioxide on the other hand has proven to be a good passivation layer for silicon [34]. Due to the good ARC properties of TiO_2 and surface passivation of SiO_2, double layer ARCs adopting titanium dioxide coupled with a silicon dioxide passivation layer have been used [35-38].
- SiN_x: Silicon Nitride is by far the most commonly used ARC for crystalline silicon solar cells. This is particularly due to its refractive index of 1.98 which is very close to the optimal index at a 600nm wavelength. Silicon Nitride also offers good passivation [39] of silicon making it a good all round coating, hence its widespread use [40- 42]. Recent work by a colleague [43] demonstrated that the refractive index of a SiN ARC could be tailored to better match that required for an ideal coating at 600nm (previously calculated to be n=1.87). Using plasma enhanced chemical vapour deposition (PECVD) equipment, varying the ratio of ammonia (NH_3) and silane(SiH_4) process gases led to the production of a silicon nitride coating with a refractive index of 1.8652, very similar to the ideal (for a 600nm wavelength) [43]. Fabricating textured silicon cells that were applied with this SiN ARC layer yielded enhancements in short circuit current, open circuit voltage, max output power, and fi p factor of 7.16%, 4.17%, 30.1% and 15.6% respectively, compared to a textured silicon cell deposited with a conventional SiN ARC layer [43].
- Al_2O_3: Aluminium oxide is typically used more as a passivation layer than an ARC. Deposition techniques for the material are similar to that used for SiN, such as PECVD. Al_2O_3 has gained recent interest because it provides very good surface passivation on p-type emitters, as good as that of a SiO_2 layer [44]. As many n-type silicon solar cell topographies have continued to grow in popularity, good surface passivation is required for p-type emitters and Al_2O_3 is able to satisfy the need, where SiN is unable to due to increased surface recombination effects. The main reason why Al_2O_3 is especially beneficial for the passivation of p-type silicon is because it has a

high fixed negative charge density, which is useful for p-type Si passivation where the minority carriers (the electrons) are effectively shielded from the c-Si surface [45].

- **Nanoparticle coatings**

  Nanoparticle coatings are different to most other ARCs as they use different mechanisms for suppressing reflectivity. By tailoring the size, shape, and environment of a metal nanostructure, light can be manipulated in many unique ways [46]. An excellent overview of plasmonic particles for solar cell reflectivity enhancement can be found in a review article by Mathew Rycenga *et al* [46]. Although the main research around plasmonic particles has been aimed at thin film devices [47, 48], some attention has been paid to using such particles for c-Si cells. Due to the relatively effective ARC and texturing for monocrystalline silicon cells, plasmonic particles are typically investigated on microcrystalline substrates where larger anti-reflective gains can be made [49]. Limited success has been achieved in the use of plasmonic particles for c-Si cells due to issues around the underlying ARC which reduce the effectiveness of the particles [50]. The issues are mainly due to the ARC layer interfering with the light scattered from the particles. Another issue is related to parasitic absorption of nanoparticles which affect the performance of the technique by reducing light capture into the cell [51]. Despite this, several publications have been presented around the use of metal nanoparticles for c-Si use [52-54]. Fahim *et al* found that a 6.3% increase in photocurrent could be made by embedding gold nanoparticles inside the SiN_x ARC of a textured mc-Si solar cell [50].

- **Nanowire coatings:**

  Another way of reducing reflectivity is by depositing vertically orientated nanowires. Nanowire coatings can be developed to have different refractive indices which can provide a gradual medium between the air and the semiconductor. Also, as the nanowires are fabricated in dense arrays, light trapping mechanisms exist reflecting light into the cell. Zinc oxide for instance has a refractive index of around 2 which is very close to the optimal index for a 600nm wavelength, so depositing ZnO nanowires can decrease the reflectivity of a cell even further [55].

3.2.3.2 Light Trapping

Light trapping regimes in c-Si cells typically employ etching of the silicon surface to create structures that refract light, increasing the optical path length. Texturing in commercial cells is typically on the microscale often creating pyramid type structures. New techniques have and are currently being developed to create nanostructures with better anti-reflective properties:

- Conventional Wet-Texturing

  Texturing is the method of choice in the majority of industrially produced c-Si solar cells. Wet chemical texturing is a relatively simple technique of creating anti-reflective structures on the surface of silicon substrates. The main categories are:

  - Anisotropic Etching: As discussed previously, texturing is very dependent on the crystallographic planes of silicon. Alkaline etching of 100 orientation monocrystalline silicon wafers produces textured pyramids on the surface, each of which with angle of incidence 54.7°. This etching mechanism is known as Anisotropic Etching and is common place with the use of mono-crystalline silicon solar cells. Common etchants for anisotropic etching include potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) [32]. The main difference between the two chemicals is that TMAH solution has higher undercut rate and lower (100) plane etch rate than KOH solution, and the (111)/(100) etch rate ratio of TMAH is two to three times that of KOH solution [56].
  - Isotropic Etching: Micro-crystalline silicon substrates differ to those of mono-crystalline as the crystal planes are random in nature. Using the same etchants as that of mono-crystalline wafers would result in randomly formed pyramids that would not perform as well. Acid etching on the other hand is an isotropic process so does not rely upon crystallographic planes. This is often the method of choice for microcrystalline silicon cells and the saw damage caused from the wafering process (wire sawing) is utilised in the etching process to provide a rough layer. A common etchant for isotropic etching include a solution of Hydrofluoric Acid (HF) and nitric acid (HNO3) [32].
  - Masking: By masking areas of the surface of the silicon wafer, custom etch structures can be produced with both anisotropic and isotropic etching. Masking is accomplished using photolithography by which a photoresist

layer is deposited and subsequently exposed through a mask to produce selective windows, through which the material can be etched. Due to the chemical resistance of the photoresist layer, areas covered by resist are not etched. Inverted pyramid type structures can be produced using 100 oriented silicon substrates using such a technique, which have better antireflective properties than simple anisotropic etching of conventional pyramid structures. Unfortunately the cost of the lithography process limits the use of the masked etching processes in the solar cell industry.

- Nanostructures:

Aside from conventional micro textured silicon surfaces, research into the modification of the surface to create nanoscale features has gown immensely in the last decade. The excellent light trapping capabilities of nanostructured surfaces have been utilised in a wide range of solar cell technologies including c-Si cells. New equipment and processes have allowed for endless configurations and some of the main developments are shown below:

  - Porous Silicon: Porous Silicon (PSi) is essentially a layer of silicon with a multitude of small holes causing the porosity. By tailoring the porosity of such holes, the layer of material can be tuned to a different refractive index. From fig.3.12 a PSi layer has a refractive index range of 1.2-3.2 and therefore could almost perfectly satisfy the ARC index parameter of 1.87 (for Air to Si) or 3.27 (for Glass to Silicon). PSi also allows for light trapping in the pores so can also perform the role of a textured surface, essentially replacing the two stage commercial process (ARC and Texturing) with one. The band gap of porous silicon can also be varied once again with porosity to values of between 1.1 and 1.9eV [26]. Having such a material at the surface of the cell possessing a different band gap, can expand the spectral properties of a cell. If a photon has energy higher than that of the band gap it will be lost, usually as heat. For conventional c-Si this means that energy over 1.12eV will be lost. Having the addition of a PSi layer however means energy up to 1.9eV can potentially be converted. One of the largest drawbacks of a PSi layer on a cell is the increased surface recombination effect due to the high surface area of the PSi layer [57], leading to more dangling bonds which require passivation. Conventional passivation layers

such as SiO_2 and SiN can however be used. Porous silicon can be produced in a number of ways including:

- Chemical etching: Formation of porous silicon by etching in hydrofluoric acid and nitric acid (very slow process).
- Metal assisted chemical etching (MAE): The etching process uses metal particles as a catalyst to assist in the chemical etching of silicon in hydrofluoric acid and hydrogen peroxide.
- Electrochemical etching: Formation of porous silicon in hydrofluoric acid by using dc electricity.

Of the methods listed above, electrochemical etching and metal assisted etching are commonly used. The use of electrochemical etching has been demonstrated to provide a 15.5% silicon solar cell using a porous silicon anti reflective layer [58].

Recently there has been a lot of research around metal assisted etching due to direct effect on silicon pore properties that the metallic catalyst particles have. Fig.3.17 shows a schematic of a typical metal assisted etching process, in this case using silver as the catalyst. The process essentially consists of:

- Metal particles or clusters are deposited onto the surface of the silicon substrate.
- The substrate is then transferred into a solution of hydrofluoric acid and hydrogen peroxide.
- Silicon that is in contact with silver is oxidised by the presence of hydrogen peroxide and becomes SiO_2.
- The silicon dioxide is subsequently dissolved by the hydrofluoric acid solution and the process repeated.
- The result is the formation of pits under the metal clusters.

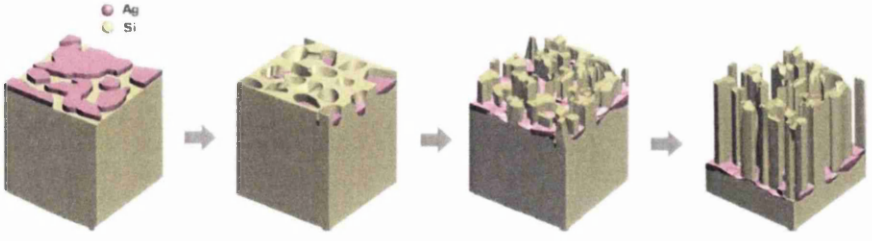


Figure 3.17: Silver metal assisted etching process for the formation of PSi [59]

- Fabricating ordered nanostructures

  Being able to fabricate silicon structures of specific size, depth and shape can be very beneficial in creating anti-reflective structures. This is because tailoring the structures can allow for tuning of the diffracted light off the structures into the solar cell. Designing and fabricating each nanostructure often requires complex electron beam lithography (EBL) equipment, which over the size of standard silicon solar cell (156x156mm) would take a substantial amount of write time (as EBL is a direct write technique). The introduction of techniques such as Nanoimprint Lithography (NIL) has allowed for replication of nanostructures in a matter of minutes. With equipment aimed at commercial nanoimprinting continuing to evolve, so has the research into the structures. Structures that have been investigated in the literature include moth eye structures [60 - 62], nanowires [63, 64], nanopillars [65], nanopyramids [66], nanocones [67, 68] and nanospikes [69, 70]. Moth eye structures have particularly shown to have excellent anti-reflective properties, taking inspiration from the topography of a moth's eye in nature. Boden *et al* [62] demonstrated an array of silicon moth eye structures that only performed 5.1% less than an ideal anti-reflective coating. Put into perspective a single layer SiN coating was found to perform 13.9% less than the ideal [62].

3.2.4 Summary

From this literature review into anti-reflective technologies applicable to crystalline silicon solar cells, it is quite apparent that reflectivity suppression is a very important research area. In industry, c-Si solar cells use two separate processes. The first is chemical texturing of the silicon surface for light trapping, and the second is the deposition of an ARC which suppresses reflectivity by using deconstructive interference effects from quarter wavelength coatings. Texturing is often performed using KOH for monocrystalline (100) orientated wafers; whilst an acid etch of HF/HNO_3 is used for multicrystalline substrates. The refractive index of SiN_x closely matches that of the ideal at a 600nm wavelength, hence it is commonly used as an ARC on both mono and multi-crystalline cells. SiN_x also provides surface and bulk passivation during an annealing process.

Monocrystalline silicon cells that are textured and coated with an ARC have very good reflectivity suppression, better than that of multicrystalline equivalents due to the lattice structure for mono substrates. Due to this, most reflectivity suppression technologies in the area of c-Si focus upon mc-Si cells. Exciting research in plasmonic structures for ARC enhancement has been demonstrated but the use of conventional anti reflective coatings with the particles have been found to be challenging.

Alternatives to the standard texturing processes for silicon surfaces have shown great promise. Highly ordered arrays of Si nano pillars and moth eye structures have shown the ability to manipulate light incident upon a cell. Replicating such structures across large area solar cell substrates is still an issue, although nanoimprint lithography has dramatically reduced the amount of time nanostructures take to be replicated. The use of porous silicon is an extremely promising technique once issues around increased recombination have been addressed. A single PSi layer can remove the need for a separate ARC layer which will inevitably save time and cost. PSi can be fabricated using simple chemical etching techniques which can be easily adopted by cell fabrication lines.

From researching the area in depth it is my belief that as current anti-reflectivity methods are achieving relatively good results for cell manufacturers, changing the tried and tested techniques will be quite difficult to implement. It is very important to note however that as the amount of silicon for a cell continues to be reduced, alternative anti-reflective techniques might be required. Obtaining thin c-Si substrates from an exfoliation process for example could potentially disrupt the crystal lattice structure of the next potential cell. For (100) orientated wafers for example alkaline etching would no longer produce the required textured surface. Even for mc-Si substrates, having micro-textured surfaces might prove too large in comparison to the overall cell thickness which could be as thin as 40μm. In this case other light trapping techniques will be adopted not only to match the performance of standard textured surfaces but to exceed it.

3.3 Solar Cell Metallisation

The main efficiency losses in a solar cell are related to reflection, recombination and electrical resistance (from metal contacts and bulk semiconductor resistances). Temperature also has a big effect upon cell efficiency. Here the effects tend to be material related and dependent on the temperature dependent carrier mobility and the thermal conductivity.

In this section, resistive losses will be investigated.

Resistive losses incurred by a cell are typically grouped as shunt and series resistances.

- Shunt resistance. A low shunt resistance is typically called a 'shunt' which can affect the electrical properties of a cell. A shunt is a local increase in the dark forward current of a cell which is typically caused by material defects or processing conditions [71].
- Series resistance in a solar cell is a parasitic, power consuming parameter that decreases the maximum achievable output of a cell [72].

3.3.1 Shunt Resistance

A comprehensive analysis of shunt resistance in crystalline silicon solar cells was undertaken by Breitenstein *et al* [73]. The study identified the main types of shunts separated into process and material induced shunts.

- Process-induced shunts
    1. Edge shunts: An edge shunt is caused when the emitter of the cell has not been fully removed from the edges of the wafer after the diffusion process. An alternative path is therefore provided by the shunt from the front to the back of the cell. This pathway allows for unwanted recombination for which energy is wasted.
    2. Cracks and holes: Cracks and holes in a silicon wafer can allow subsequent diffusion of the emitter region to contact the back of the cell. In this scenario a similar effect to an edge shunt is observed with carriers recombining and releasing their energy as unwanted heat.
    3. Schottky-type shunts: These shunts occur when there is a direct contact between the front metallic contact and the base region of the cell. In a well processed cell the thin emitter layer prevents this occurrence. A non uniform diffusion layer or over firing of the front electrical contact can lead to a punch

through of the emitter region. Once again unwanted recombination occurs because of such contact.

4. Scratches: Scratches on the surface of a cell generate local recombination centres by disturbing the p-n junction of a cell. As the emitter region is typically only several hundred nanometers, a relatively insignificant scratch can disturb the depletion region leading to recombination.
5. Aluminium particles: Due to the use of aluminium as a back contact and back surface field for silicon solar cells, it is quite possible that the front of the cell could become contaminated with aluminium accidentally. Because of its very nature of creating a p^+ back surface field on the rear of solar cells, annealing aluminium into an n-type emitter region would reduce its effectiveness. This p^+region may be in ohmic contact with the base, but it also makes a tunnel contact to the emitter, thus producing a shunt [73].

- Material-induced shunts

6. Strongly recombinative crystal defects: Impurities and poor crystal quality during cell manufacture can lead to Shockley-Read-Hall (SRH) recombination where an energy state in a forbidden region is created trapping carriers. If both electron and hole move to the same energy state, they simply recombine.
7. Macroscopic Si_3N_4 inclusions: Sometimes during the crystallisation process of multicrystalline silicon ingots, Si_3N_4 are unintentionally grown and the recombination activity of interface states between Si and this Si_3N_4material are responsible for this type of shunting [73].

3.3.2 Series Resistance

The series resistance in a typical p-n junction silicon solar cell is influenced by the following [72] (which can be seen in fig.3.18):

The Front Contact

1. Front busbars
2. Front gridlines
3. Interface between front contact metal and silicon

The Substrate

4. Emitter sheet
5. Bulk substrate

The Back Contact

6. Back metal
7. Back busbars

Series resistance in a cell is very important and it can decrease the fill factor by 2.5% for each 0.1Ω increase in resistance [74]. Of all the series resistance losses caused by metallic contacts, the top contact is most significant after sheet resistance. The top contact is used to collect minority carriers and due to their low density, collection can be problematic [75], in part due to the limited contact area that the front metallisation can have in relation to shading loss. The rear contact is used to collect majority carriers. Coupled with full metal coverage of the entire area of the back of the wafer and low base resistivity, the contribution of the back contact to the series resistance is minimal [76]. Fig.3.18 shows a schematic of a typical silicon solar cell depicting the main series resistive losses:

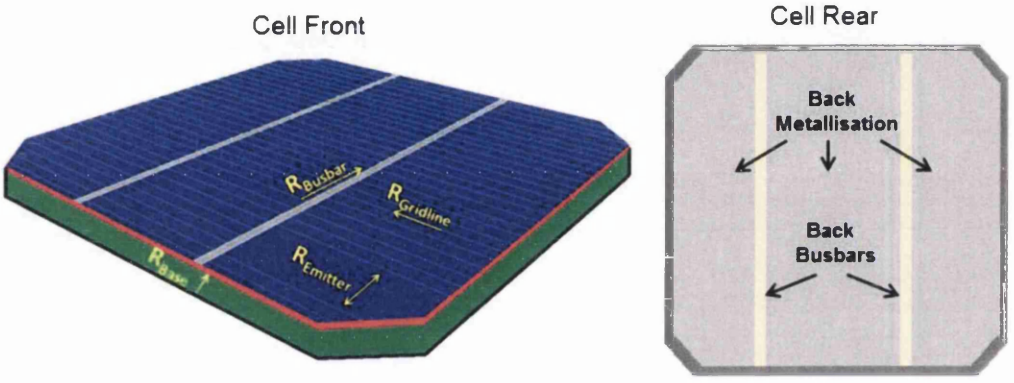


Figure 3.18: Schematic of the main series resistive components in a silicon solar cell

Determining an accurate value of the series resistance can be difficult although a range of techniques have been demonstrated [77]. Typical electrical instrumentation utilised by solar simulator equipment, use the method of a comparison between one IV curve to that another plotted at a different intensity [78].

The front contact of a standard silicon solar cell is of upmost importance as it is responsible for extracting minority carriers from the cell. Unfortunately, design of the front contact is not as simple as that of the rear. A trade-off between shading losses and series resistance exists. To allow as much light to enter a cell, the contact dimensions ideally would be very small to avoid shading. To have a low resistance however, the contact dimensions would be as large as possible and completely cover the top of the cell. Considering the two very different requirements, a specifically designed front contact is required on standard solar cells. One such design is illustrated in fig.3.19.

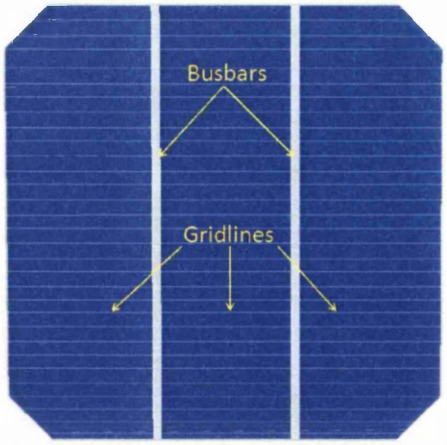


Figure 3.19: Typical silicon solar cell with two busbar top contact arrangement

The front contact demonstrated in fig.3.19 has a series of metallic lines printed onto the surface of the cell. The lines are composed of 3 vertical busbars and 65 thinner horizontally printed gridlines. The role of the thicker busbars is to collect the current from the finer gridlines to be transferred out of the device. The contact design allows for photons to enter the cell through the regions between the gridlines. Such a front contact design is often referred to as an 'H' contact due to its layout. The front contact (gridlines and busbars) typically shade around 10-15% of the front surface [79].

To minimise shading yet maximise contact current carrying abilities, high aspect ratio contacts are printed. The resistance of the contact line is proportionate to its volume. Such tall yet narrow contact lines are depicted in fig.3.20.

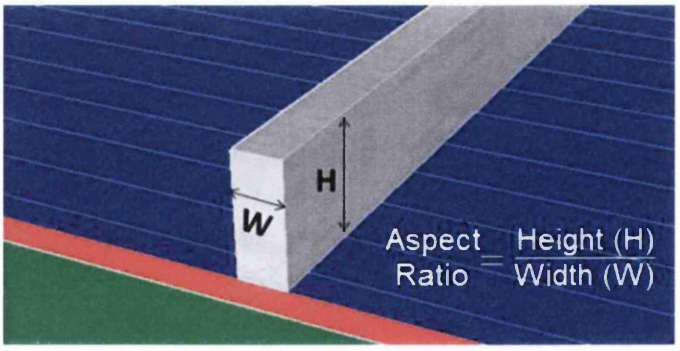


Figure 3.20: High aspect ratio front contact

Contact topologies such as the one demonstrated in fig.3.19 tend to dominate the crystalline silicon (c-Si) solar cell market. Such dominance is due to two reasons. The first is that it is technologically easier to produce rear and top contact silicon cells than other topologies such as back junction and buried contact cells. The second is that simple printing procedures can be adopted to print the contacts. Despite the widespread industrial use of standard printing processes, a number of advancements especially in front contact

technologies have been made. This review will show that worldwide research has been conducted around areas such as:

- Silicon solar cell topographies (Back contact cells, Laser buried contacts, Selective emitters).
- Materials used for contacts (Silver, Copper, Nickel, Metallic Nanowires).
- Deposition methods for fabricating contacts (Screen Printing, PVD, Plating, Aerosol Jet).

Front contacts in current use as well as novel front contacts will be reviewed for conventional cell topography in the following section.

3.3.3 Conventional Metallisation

Before analysing different materials and deposition methods for front contact formation on silicon solar cells, it is important to review the current methods adopted to produce commercial cells. In industry, screen printing of front and rear contacts is the method of choice. The rear contact, as previously mentioned, does not significantly contribute to resistive losses, so the focus of this discussion will be the front contact.

Screen printing is a simple printing technique which essentially applies ink through a series of holes in a mesh onto the substrate below. Areas where ink is not required to be deposited are masked so that no ink will pass through. Further details on the process can be found in Chapter 4. In commercially produced cells, the ink chosen to print the front contact is predominantly silver. Silver is typically chosen as it provides excellent conductivity (the best conductor of all the metals) and can easily be soldered to. Solder ability of a front contact is crucial as solar cells are often connected in series to provide a higher voltage solar panel. Conductive tabbing wire is used to electrically attach one cell to another. Being able to reliably solder this tabbing wire to a cell is very important. Fig.3.21 shows the connection of one silicon cell to another:

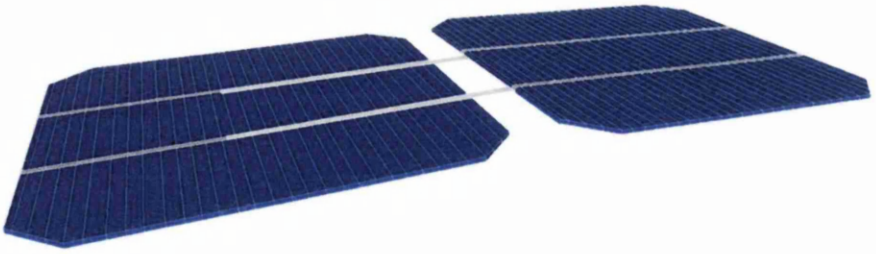


Figure 3.21: Solder tabbing wire connection between solar cells

Other than the qualities mentioned above, the front contact must also satisfy the following:

- Low resistance contact formed between the silicon substrate and metallisation.
- Contact must not penetrate through emitter junction (short circuiting the cell).
- Contact must adhere to the silicon substrate (not delaminate).
- Must be able to electrically contact silicon through the insulating native oxide and silicon nitride ARC coating.
- Must have good current carrying capability.

All the above parameters are successfully achieved by developing a customised metallisation paste for top contact formation. Simply using silver particles suspended in a solution would not achieve the required result. Other materials are required in the paste in order to satisfy each requirement of the contact.

A typical silver paste for front contact metallisation on silicon cells consists of [80]:

(i) Silver powder (70 to 80wt%).

(ii) Lead borosilicate glass frit PbO-B_2O_3-SiO_2 (1 to 10wt%).

(iii) Organic components (15 to 30wt%).

The silver powder provides the conductive metallisation and requires high temperature firing to sinter the particles together to form a conductive pathway. A representative firing profile for a silver screen printable photovoltaic paste is provided from a paste manufacturer's datasheet [81] and shown in fig.3.22.

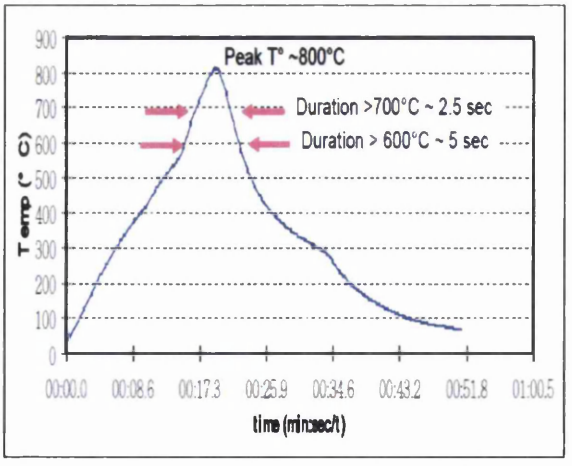


Figure 3.22:Typical firing profile for screen printable silver paste [81]

The organic components of the paste are mainly for printability enhancement for high aspect ratio contacts. The most important part of the paste is the glass frit. The glass frit is responsible for opening a window through the SiN ARC and adhering the contact to the silicon substrate [82]. The contact resistance of a front solar metallisation is strongly

influenced by the interface between silicon and silver. With the glass frit playing a key role during this contact structure, much research has formed around what actually goes on during the contact formation [83-86]. A relatively recent review backed up by experimentation was reported in the book 'Silicon Wafer-Based Technologies' [87] and describes the contact formation as follows:

- During the firing of the contact to the substrate, silver and silicon are both dissolved in the glass frit during the firing process. Mild etching of Si-bulk by the Ag supersaturated glassy-phase can occur.
- The amorphous SiN ARC is incorporated into the already-existing glass phase. A higher density ARC (deposited at 850°C through low-pressure) is more difficult to merge in the glass phase.
- The generated lead (from the glass frit) then alloys with the silver forming silver crystallites from the liquid Ag-Pb phase.
- Ag particles do not sinter into a very compact structure and a porous Ag-bulk is formed, resulting in a complex contact structure. From the study, at least three different microstructures were found.
- The combination effects of glassy-phase and the dissolved metal atoms have a crucial influence on Ag-bulk/Si-emitter structures, and consequently, the current transport across the interface.
- On cooling down, silver precipitates and re-crystallize on the silicon surface as well as in the glassy phase. There is direct contact between isolated Ag crystallites and the Si.
- Ag bulk is prevented from contacting the Si by a very thin glass layer (<5nm). Only Ag crystallites contact the silicon
- If there was no glass layer in between, the Ag would diffuse at least 5µm deep during the firing cycle and it would shunt the p-n junction

A High-resolution transmission electron microscopy (HR TEM) image of the thin glassy layer is shown in fig.3.23.

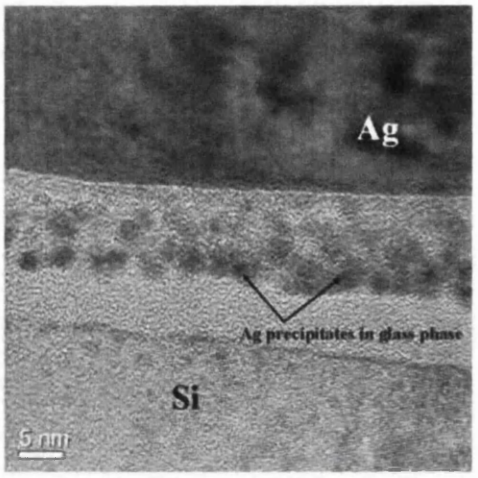


Figure 3.23: HR TEM Image of contact interface between silicon and silver [87]

The path through which current flows from the silicon to silver contact has again received much attention. Two main theories have been suggested and debated, the first presented by Schubert *et al* [88] and the second by Ballif *et al* [89]. Schubert *et al* suggest that the current transport mechanism is through the thin leaded glass layer between the bulk silver and silicon substrate. Ballif *et al* believes however that the current transport is through the silver crystallites between the bulk silver and silicon.

The most recent debate over the current transport mechanism took place at the 4th Workshop on Metallization for Crystalline Silicon Solar Cells [90]. The result from the workshop was inconclusive despite new research aimed exactly at determining the mechanism [91]. It was concluded that both crystallites as Ag nano colloids can be found in screen printed contacts, and that a continuous leaded glass layer correlates with a low contact resistance [90].

The current commercial process for front contact formation on crystalline silicon solar cells is not the only method available for contacts. In the last few years different printing processes and paste formations have been developed, some of which are beginning to enter industry. A comprehensive review has been undertaken here in order to highlight some of the advancements. As with most research areas in photovoltaics, two primary areas have been focused upon. The first aimed at improving efficiency and the second tasked with cost reduction. Due to the extensive breadth of research, techniques closer to meeting commercial demands will be discussed in more depth.

By far the two largest areas concerned with front contact research is the choice of metal to use and the process to apply it to the cell.

3.3.4 Materials for Metallisation

The choice of a metal largely depends on its ability to perform the functions of a front contact. The main qualities required of the metal are to have good conductivity, form a strong yet low resistance contact to the silicon substrate and to have good solder ability. Silver has long been used for such a purpose and the contact qualities are relatively well understood. It is also important to note that silver does not oxidise during the firing procedure, which could drastically increase contact resistance. Unfortunately the cost of silver has increased substantially over the last few years [92], so the hunt for a replacement material is of interest. Below are metals investigated for replacing silver as a contact.

3.3.4.1 Nickel

Nickel is a very promising metal for front metallisation of silicon solar cells. The primary reason for such promise is that a lower contact resistance than that of silver is measured between the nickel electrode and silicon substrate [93]. This is due to the difficulty of forming an ideal ohmic contact between phosphorous doped n-type silicon and silver. Nickel contacts have been investigated as interface layers between silicon and that of a standard silver contact. The schematic of a typical process is demonstrated by Baomin *et al* [94] and shown in fig.3.24.

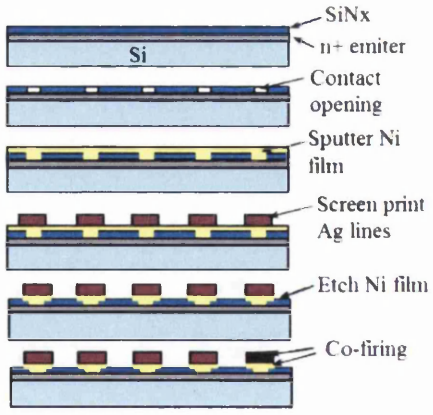


Figure 3.24: Schematic of a front contact process using a thin nickel layer [94]

In fig.3.24 the nickel has been sputtered onto the silicon substrate. Another method typically used, is electroplating of the Ni layer [95]. One disadvantage of sputtering and plating of metallic layers is that higher processing time and cost is incurred compared to conventional screen printing of contacts. It has also been suggested by Butler *et al* [96] that some of the nickel silicides that can form during firing of the Ni contact to silicon (at 200-

700°C) are not suitable for contact use, although others were found to have lower contact resistance at different temperatures.

3.3.4.2 Copper

The use of copper as an alternative to a silver electrode is an obvious choice due to the similar electrical characteristics copper possesses. Copper is the second best conductor of electricity (the first being silver). Unfortunately unlike silver, Cu oxidizes easily in an atmospheric environment at temperatures of ≥200°C [97]. Such oxidisation restricts the temperature at which a copper contact can be subjected to, limiting printing conditions to expensive deposition and plating techniques. One research group [98] has developed a paste consisting of a copper–phosphorus (Cu–P) alloy which can withstand firing over 200°C, to produce a low resistive contact. Unfortunately they found that when applying a copper contact directly to silicon, the inter-diffusion of the Cu and Si causes the formation of Cu silicide (Cu_3 Si) that degrades the cell performance significantly due to diffusion of copper into the p-n junction causing shunting [98]. Other groups [99-101] have used plated copper successfully as a front contact by using nickel to form a silicide as a barrier layer to prevent direct contact of the copper with silicon.

3.3.4.3 Magnesium

Another useful metal for the interface layer, to decrease the contact resistance between silicon and silver, is magnesium. The decreased contact resistance is attributed to the low work function difference between Si and evaporated Mg [102]. Using this technique a silicon solar cell with 17.75% efficiency was obtained [102].

3.3.4.3 Transparent Conductive Contacts

Transparent conductive contacts have long been used for thin film solar cells. Recently they have attracted attention for crystalline silicon cells.

- Indium Tin Oxide (ITO)

  ITO is a commonly used transparent conductor in many applications from touch screens to thin film solar cells. In comparison little research into the use of ITO as a contact for crystalline silicon substrates has been conducted. The main reason is firstly due to the excellent performance of metal gridline structures on silicon and secondly due to cost and structural issues (cracking of the layer) arising from ITO contacts. Despite the problems, research has found that the addition of an ITO

layer on c-Si can serve as a good ARC, whilst achieving a similar series resistance to that of a silver contact [103]. Kim *et al* [103] found that a substantial reduction of Ag grid area (by less than one quarter) could be made using an ITO layer. This enhances the available area of silicon that can be illuminated, yielding an increase in current of 10.3% [103].

- Metallic Nanowires

  Like ITO, the investigation of the use of metallic nanowires for c-Si applications has been limited. Silver nanowires are the natural first choice due to the well known electrical properties for the metal. One article published in 2013 suggested that the application of a silver nanowire contact directly on a crystalline silicon substrate had previously not been demonstrated [104]. The work found that such a silver nanowire mesh processed cell (depicted in fig.3.25) resulted in a cell efficiency of 5.32% [104]. No apparent depositions were made on a textured cell nor were comparisons made to other front contact topologies. Gao *et al* [105] demonstrated that a series of silver nanoparticles (deposited at the base of the pyramids only) sintered together on a textured silicon substrate can have the effect of a highly conductive nanowire contact. Silver nanowire contacts are further investigated in Chapter 7.

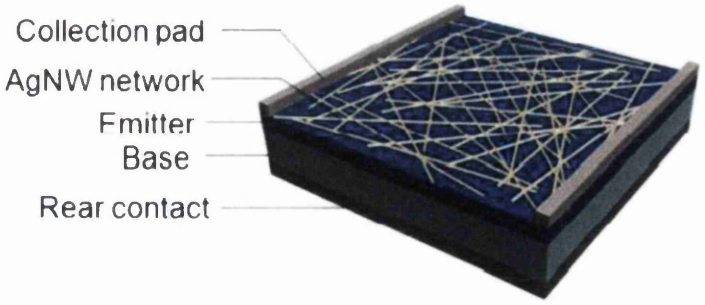


Figure 3.25: Silver nanowire mesh top contact for silicon solar cell [104]

3.3.5 Formation of Metallisation

The choice of equipment used to fabricate a contact is largely dependent upon the thickness, width (aspect ratio) and material to be deposited. With high aspect ratio features desirable, using low cost metals, various techniques have been developed and modified.

3.3.5.1 Plating

From the review of metals used for front contact formation, plating is an exciting area in solar cell metallisation. Plating is typically used to deposit interface layers, but can also be used to build up contacts with the same material or that of another. Plating has a large potential especially in c-Si and there are now commercially produced industrial plating tools for solar cell metallization [90]. There are several plating techniques developed:

- Electro-plating: An electrolysis technique used to deposit metal onto a conducting substrate (or in this case a semiconducting substrate). Any area of the material in electrical contact with the plating solution will get covered in a metal coating.
- Masked plating [106]: Masked plating is similar to that of electro-plating only a mask shields areas where no deposition is required. Masking materials can by any insulating layer such a photoresist and even dielectric ARCs. For photoresist masks, standard photolithography methods are used whilst for patterning an ARC, Laser ablation is used to open up windows in the ARC for subsequent metal plating.
- Light-induced plating [107, 108]: Exploits the photovoltaic properties of solar cells to produce a current to plate its own contact grid, as metallic cations in a plating bath have positive charge and the p-type illuminated cell accumulates a negative charge on the front surface [108]. As in masked plating, a dielectric ARC is used for mask purposes.
- Electro-less plating [99]: Electro-less plating involves the use of a chemical technique (auto-catalytic reaction) by which the solution provides the electrons (current for the process). As in other plating processes a mask material is required for selective contacts to be created.

3.3.5.2 Localized electro chemical deposition

The technique allows for selective plating without the requirement for masks which are often applied using expensive and time consuming photolithography techniques (photoresist patterning by mask alignment etc). A promising technique for selective plating is the Dynamic Liquid Drop (DLD) process [109]. In the recently developed Dynamic Liquid Drop technique, a chemical solution used for plating is confined to a specific area of the sample, allowing for localised plating without the need for

additional masks [110]. A schematic of the DLD technique is shown in fig.3.26. The key to the success of the process is the suspension of the plating solution (in a dynamic liquid meniscus) whilst recirculation of the fluid is implemented to allow for continuous plating.

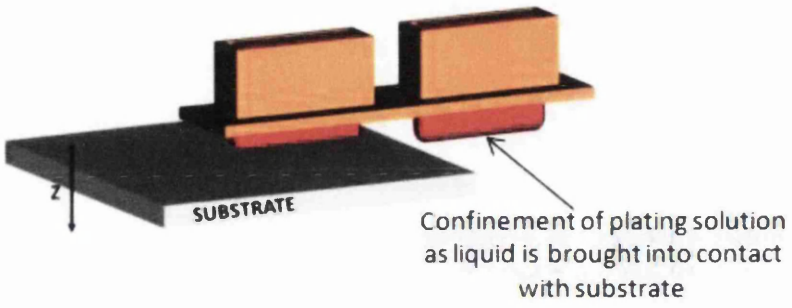


Figure 3.26: Mechanism of DLM formation as substrate approaches the DLD [110]

3.3.5.3 Evaporated and Sputtered contacts

The use of such equipment for silicon solar cells is very much confined to the research and development stage and is not cost effective due to low deposition rates and complex and expensive equipment required.

3.3.6 Printing Techniques

Screen printing is not the only technique that has been used to print front metal contacts on c-Si. The following printing methods are typically used to print seed/ interface layers rather than the entire contact. This is primarily due to the issues around the printed thickness of contacts the techniques are capable of printing.

- Pad printing: A contact printing technique where a rubber pad is used to transfer an inked design from a stamp to the substrate material using a pressure contact.
- Flexography printing: A contact printing technique where a rotating patterned stamp on a drum is first inked before the substrate is brought into contact with stamp, transferring the ink from stamp to substrate.
- Ink jet printing: A non contact printing technique in which droplets of ink are ejected through a small nozzle which moves back and forth across the sample, depositing ink where required (drop on demand). Piezoelectric materials are often used for ink ejection by momentarily squeezing the ink, forcing it out of the nozzle in the form of a droplet.

- Aerosol-jet printing: A non contact technique, similar to that of the ink-jet process only instead of a droplet, an aerosol jet of the ink is formed.

Of the four techniques listed above, aerosol-jet printing of metallic seed layers was found by Peraiah *et al* [111] to produce better electrical performing contacts, with finger/gridline widths as narrow as 14μm. Non contact techniques are often favoured for metallisation applications as a thicker layer of ink can ultimately be deposited. Contact techniques use pressure to transfer ink from a stamp or pad onto the substrate which compresses the ink and thereby reduces the aspect ratio of contacts. Aerosol-jet printing can allow for even thicker metallisation that ink jet printing as it is capable of using far higher viscosity inks due to the force (compressed gas) that can be applied to eject the ink. Also a sheathing gas is used in aerosol-jet printing to define a narrow jet of ink, which is ideal for producing narrow gridline contacts.

- Spray Coating: A very simple technique that uses a compressed gas to spray a medium onto the surface. Spray coating has been used in the deposition of silver nanowires [112, 113] using a very small nozzle to confine and direct the material.

In order for a front contact to be successful on a silicon solar cell, the metal must have physical contact with the silicon through the ARC. Some methods such as evaporating and sputtering (physical vapour deposition techniques) are limited to only applying the metal and no other components (which aid in the transition through the ARC coating). Plating a contact typically requires a conductive substrate, so an insulting layer such as an ARC will prohibit such a technique from being used. As previously mentioned, silver pastes typically used for contact formation contain glass frits and other materials to aid with the contact formation process. To overcome the obstacle of the ARC layer, methods have developed around patterning windows through the layer. This allows any subsequent metal deposition to contact the silicon directly. Opening of selected ARC windows can be achieved by:

- Application of a mask followed by wet etching
- Selective laser ablation
- Printing of wet etching chemicals
- Mechanical removal techniques

The last two years has seen a great change in the PV market as described in Chapter 3. The unprecedented low cost of Chinese c-Si solar panels has had a drastic affect upon the industry. To compete against the cost reductions, savings on materials and processing must be made. The silver quantity used for cell production is an obvious target. Research conducted on front contacts has changed course to address the issue. This is indicated by

the shear amount of publications related to the minimisation of silver use, especially during 2013. Published proceedings from the 4th Workshop on Metallization for Crystalline Silicon Solar Cells, held in May 2013 [90] reinforced this by stating that screen printing of Ag is progressing more than the alternative processes.

3.3.7 Reducing Metallisation

The reduction of silver material used to print the contacts has been separated into four distinct areas.

1. **Interconnects**

   The solder ability of a cell is important for interconnections. The front contact busbars therefore have to be suitably large and thick enough to carry the current whilst enabling soldered tabbing wires to be attached. A wide, thick contact inevitably translates to a higher quantity of silver paste. Removing the need for busbars is therefore advantageous. Some alternative methods are listed below:

   - Attachment of interconnects by conductive adhesives/films. Using a conductive adhesive can reduce Ag consumption by up to 40% by allowing for narrower busbars [114].
   - Multi bus bar concepts. Attaching several narrow tabbing wires from one cell to another can remove the need for separate thick additional busbars [115].

   Unfortunately, issues around the adhesion of such contacts [116] have been highlighted. As most solar panels come with a 25 year warranty, more research is required before commercialisation. The addition of a conductive film or additional wire interconnects can often outweigh the cost savings of busbars free designs.

2. **Screen Printing Improvements**

   One of the limiting effects upon achieving a high aspect ratio contact is related to the screen printing process. Typical solar gridlines have a minimum screen printed width of around 100µm. Recent studies have led to a reduction in the width by investigating and modifying important parameters in the process, some of which include:

   - Speed and pressure of process
   - Emulsion thickness
   - Ultra fine screen mesh: The reduction of the size of the mesh holes has lead to a significant decrease in the line width achieved for screen printed gridlines. With finer mesh screens, narrower lines below 50µm in width can be printed

[117], although discontinuous lines can be an issue. Simply printing over the line a second time can resolve the issue although material consumption is increased.

It is important to note however that a trade-off will eventually exists between fine gridline contacts and series losses, due to contact resistance and current carrying capabilities of fine structures.

3. **Grid Optimisation**

With the possibility of printing finer gridlines, the classic front H bar contact arrangement can be improved.

- Greulich *et al* [118] demonstrated that by varying finger width from 50 to 130μm, the optimum quantity of fingers changed from 100 to 60 respectively. I.e. 100x 50μm fingers can be used to replace 60x 130μm fingers. This shows that if we can print 50μm wide gridlines, we can save silver material without compromising the electrical properties of the contact.

4. **Ag Paste Modification**

Despite the various research concerned with the use of nickel and copper for front contact metallisation, the use of conventional silver paste is still being investigated and improved. With the current investigation ongoing into current transport mechanisms through the silver to silicon substrate, branches of research have fanned out. Some of the major parameters under investigation include:

- Viscosity of pastes: With finer meshes for screen printing and different printing techniques, comes the need for less viscous silver paste. One group at the Fraunhofer institute [119] modified paste compositions to print gridlines <40μm in width. They identified that both silver content and glass frit composition and size was important for fine-line printing.
- Glass frits: As the glass frit is important for low contact resistance formation between the silver paste and silicon substrate, varying frit composition and size has been investigated in the literature. By coating the glass frit in silver an improvement of conductivity of that over the standard frit was found to be about 15% [120]. The particle size of the glass frits was found to strongly affect the contact resistance. A silver contact with nanosized glass frit was found to have lower contact resistance than that of mircosized particles [121].

- Silver particle size: The size of silver particles is important, as if a contact is too porous, the conductivity will decrease. Adding silver nanoparticles to a paste composed of microsize silver was found to help to the sintering process and improve PV performance [122].
- Environmentally friendly pastes: Although not related directly to cost savings, the environmental impact of silver paste is an important topic especially with pastes containing lead glass frit. The most promising lead substitute is the use of Bi-based (Bi_2O_3–B_2O_3–SiO_2) glass frits [123].

3.3.8 Summary

From reviewing literature specifically aimed at crystalline silicon solar cell front contacts, it is clear that screen printing of silver is still by far the most commercially adopted method. Despite some very exiting alternatives being investigated, the market is still the driving force behind research. During the last year a move back to improving silver screen printed metallisation was observed. This is largely due to the challenges manufacturers outside of the Chinese market are facing. To compete with costs, every aspect of the cell must be optimised and the silver front contact is one area well and truly under the spotlight. Silver as a metallisation is well suited to function as a top contact for silicon solar cells. The contact formations are reasonably well understood although there is still some debate around current transport mechanisms. Continued research in the near future will almost certainly put an end to any speculation.

Other metals have been put forward to replace silver and some such as nickel have shown real promise. The main issue is the mechanism required to make contacts out of the metals. Plating and evaporation have been widely used to fabricate good electrical contacts. Unfortunately, plating requires additional equipment and processing of the cell, whilst evaporation requires complex equipment and has slow deposition rates. The use of interface layers may however bridge the gap between screen printing and more complex deposition techniques. If a thin seed layer is deposited and then plated/printed on top of with copper for example, a large enough saving on materials can offset the cost of the more complex processing method.

I believe from reviewing the area in depth, that screen printing of silver will for now remain the industry standard. The main reason for this is due to the tough market conditions where companies are less likely to take risks on new processes (unless significant savings can be demonstrated). Improvements to silver paste composition and

finer screen printed gridlines have made good progress, and will hopefully make it into commercial operations. The largest cost in silver paste is the silver itself and reducing the amount in the paste will affect its electrical performance. Screen printing has also begun to reach its limit in printing narrower gridlines. Due to the limitations of current methods, there will come a time when new deposition methods and materials take over. Plating is predicted to take over from screen printing with copper being the metal of choice for plating onto seed layers. With this, techniques to open contact windows will also advance. Commercial plating in silicon solar cell fabrication lines is on the horizon, but at the moment waiting for researchers to industrialise the process further.

[1] Van Swaaij *et al.* Thin-film silicon technology for highly-efficient solar cells, Bipolar/BiCMOS Circuits and Technology Meeting, IEEE , pp.1,7, 2012

[2] Saga T. Advances in crystalline silicon solar cell technology for industrial mass production. NPG Asia Materials, 96–102, 2010

[3] Dross F. *et al.*, Stress-Induced Lift-Off Method for kerf-loss-free wafering of ultra-thin (~50 μm) crystalline Si wafers. PVSC '08. 33rd IEEE, vol., no., pp.1,5, 2008

[4] Alex Masolin, Payo Maria Recaman, Method for fabricating thin photovoltaic cells, WO2012/034993A1, 2012

[5] R. Brendel: Crystalline thin-film silicon solar cells from layer-transfer processes: a review: *Ext. Abstr. 10th Workshop on Crystalline Silicon Solar Cell Materials and Processes,* p. 117, *2000*

[6] Alongkarn Chutinan *et al*, Wave-optical studies of light trapping in submicrometre-textured ultra-thin crystalline silicon solar cells, J. Phys. D: Appl. Phys. 44 262001, 2011

[7] Deguchi, M *et al.*, Prospect of the high efficiency for the VEST (via-hole etching for the separation of thin films) cell, Photovoltaic Energy Conversion, IEEE First World Conference , vol.2, no., pp.1287,1290 vol.2, 5-9, 1994

[8] Sato, N.; Sakaguchi, K.; Yamagata, K.; Atoji, T.; Fujiyama, Y.; Nakayama, J.; Yonehara, T., "High-quality epitaxial layer transfer (ELTRAN) by bond and etch-back of porous Si," SOI Conference, 1995. Proceedings., 1995 IEEE International , vol., no., pp.176,177, 1995

[9] Teng-Yu Wang; Chien-Hsun Chen; Chen-Hsun Du; Chung-Yuan Kung, "Fabrication of an ultra-thin silicon wafer with honeycomb structure by Thermal-Stress Induced Pattern Transfer (TIPT) method," Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE , vol., no., pp.002731,002734, 2012

[10] Stocks, M.J.; Weber, K.J.; BLAKERS, A.W.; Babaei, J.; Everett, V.; Neuendorf, A.; Kerr, M.J.; Verlinden, P.J., "65-micron thin monocrystalline silicon solar cell technology allowing 12-fold reduction in silicon usage," Photovoltaic Energy Conversion , vol.1, pp.184-187 Vol.1, 2003

[11] Hernandez, David; Trifonov, Trifon; Garin, Moises; Alcubilla, Ramon, ""Silicon millefeuille": From a silicon wafer to multiple thin crystalline films in a single step," Applied Physics Letters, vol.102, no.17, pp172102-4, 2013

[12] Young Oh, *et al*, Magnetically Guided Nano–Micro Shaping and Slicing of Silicon, Nano Letters,12 (4), 2045-2050, 2012

[13] Michel Bruel, Separation of silicon wafers by the smart-cut method, Material Research Innovations, Vol 3, 1, pp 9-13, 1999

[14] Ernst, M.; Brendel, R., "Large area macroporous silicon layers for monocrystalline thin-film solar cells," Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE , pp.003122,003124, 2010

[15] Dross *et al.*, "Slim-cut: A kerf-loss-free method for wafering 50 um-thick crystalline Si wafers based on stress-induced lift-off," 23rd European Photovoltaic Solar Energy Conf. and Exb., pp. 1278-1281, 2008.

[16] Masolin, A.; Vaes, J.; Dross, F.; Poortmans, Jef; Mertens, Robert, "Thermal curing of crystallographic defects on a slim-cut silicon foil," Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE , pp.002180,002183, 2010

[17] Jan Vaes ; Alex Masolin ; Amaia Pesquera and Frédéric Dross, "SLiM-cut thin silicon wafering with enhanced crack and stress control", Proc. SPIE 7772, Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, 777212, 2010

[18] Leo Mathew, Dharmesh Jawarani: Method of forming an electronic device using a separation technique, US20120045866A1, 2012

[19] Fossum, J.G.; Sarkar, D.; Mathew, L.; Rao, R.; Jawarani, D.; Law, M.E., "Back-contact solar cells in thin crystalline silicon," *Photovoltaic Specialists Conference (PVSC)*, pp.003131,003136, 2010

[20] Rao, R. A. *et al*, "A novel low cost 25μm thin exfoliated monocrystalline Si solar cell technology," Photovoltaic Specialists Conference (PVSC), pp.001504,001507, 19-24 2011

[21] Jiri Vanek, Kristyna Jandova, Solar Cells - Silicon Wafer-Based Technologies, InTech, 112-124, 2011

[22] Green, M.A. and Keevers, M. "Optical properties of intrinsic silicon at 300 K ", Progress in Photovoltaics, p.189-92, vol.3, no.3; (1995)

[23] Saga T. Advances in crystalline silicon solar cell technology for industrial mass production. NPG Asia Materials, 96–102, 2010

[24] Dross F. *et al.*, Stress-Induced Lift-Off Method for kerf-loss-free wafering of ultra-thin (~50 μm) crystalline Si wafers, Photovoltaic Specialists Conference, PVSC '08. 33rd IEEE , vol., no., pp.1,5, 2008

[25] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, Second Edition, John Wiley & Sons, 265-313, 2011].

[26] Tayyar Dzhafarov (2013). Silicon Solar Cells with Nanoporous Silicon Layer, Solar Cells - Research and Application Perspectives, Prof. Arturo Morales-Acevedo (Ed.), 2013

[27] Chetan Singh Solanki, Solar Photovoltaics: Fundamentals, Technologies and Applications, Prentice-Hall, 2011

[28] Hylton J. D., Burgers A. R., Sinke W. C., Alkaline Etching for Reflectance Reduction in Multicrystalline Silicon Solar Cells, J. Electrochem. Soc., 151, 6, G408-427, 2004

[29] Ziaie, B., *et al*. Introduction to Micro-/Nanofabrication. Springer Handbook of Nanotechnology. B. Bhushan, Springer: 231-269, 2010

[30] Yablonovitch, E. Statistical ray optics. J. Opt. Soc. Am. 72 (7), 899–907, 1982

[31] Yu, Z., *et al*. "Fundamental limit of nanophotonic light trapping in solar cells." Proceedings of the National Academy of Sciences, 2010

[32] Dirk-Holger Neuhaus and Adolf Münzer, "Industrial Silicon Wafer Solar Cells," Advances in OptoElectronics, vol. 2007

[33] G. San Vicente, A. Morales, M.T. Gutierrez, Preparation and characterization of sol–gel TiO2 antireflective coatings for silicon, Thin Solid Films, Vol 391, Issue 1,2, P133-137, 2001

[34] Surface passivation of crystalline silicon solar cells: a review. Prog. Photovolt: Res. Appl., 8: 473–487, 2000

[35] Martinet, C., Deposition of SiO2 and TiO2 thin films by plasma enhanced chemical vapor deposition for antireflection coating, Journal of Non-Crystalline Solids, vol. 216, pp. 77-82, 1997

[36] M. Mazur, *et al*, TiO2/SiO2 multilayer as an antireflective and protective coating deposited by microwave assisted magnetron sputtering, Opto-Electronics Review,Vol 21, Issue 2, pp 233-238, 2013

[37] S. Kh. Suleimanov, *et al*, Effective antireflection coating based on TiO2-SiO2 mixture for solar cells, Technical Physics Letters, Vol.39, Issue 3, pp 305-307, 2013

[38] Ali Ibrahim, A.A. El-Amin, Etching, Evaporated Contacts and Antireflection Coating on Multicrystalline Silicon Solar Cell, IJRER, Vol 2, No 3, 2012

[39] Bhushan Sopori, Silicon nitride coatings for Si solar cells: control of optical reflection and surface/bulk passivation, Dielectrics in Emerging Technologies: Proceedings of the International Symposium, p186-200, 2003

[40] Soppe, W., Rieffe, H. and Weeber, A., Bulk and surface passivation of silicon solar cells accomplished by silicon nitride deposited on industrial scale by microwave PECVD. Prog. Photovolt: Res. Appl., 13: 551–569, 2005

[41] Kyung Dong Lee, *et al*, Influence of SiNx:H film properties according to gas mixture ratios for Crystalline Silicon Solar Cells, , Current Applied Physics 13, 241-245, 2013
[42] Jinsu Yoo, S.K. Dhungel, J. Yi, Properties of plasma enhanced chemical vapor deposited silicon nitride for the application in multicrystalline silicon solar cells, Thin Solid Films, Vol 515, Issue 12, 23, Pages 5000-5003, 2007
[43] Yufei Liu, Owen James Guy, Jash Patel, Huma Ashraf, Nick Knight, Refractive index graded anti-reflection coating for solar cells based on low cost reclaimed silicon, Microelectronic Engineering, Vol 110, 418-421, 2013
[44] Dingemans, Gijs; Kessels, E., "Status and prospects of Al2O3-based surface passivation schemes for silicon solar cells," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films , vol.30, no.4, p040802-27, 2012
[45] Hoex, B.; Schmidt, J.; Van de Sanden, M. C M; Kessels, W. M M, Crystalline silicon surface passivation by the negative-charge-dielectric Al2O3, PVSC '08. 33rd IEEE , vol., no., pp.1,4, 11-16, 2008
[46] Rycenga, M., *et al.* "Controlling the Synthesis and Assembly of Silver Nanostructures for Plasmonic Applications." Chemical Reviews 111(6): 3669-3712, 2011
[47] K.R. Catchpole, Plasmonic solar cells, OPTICS EXPRESS 2008, Vol. 16, No. 26, 21793, 2008
[48] Tan, H., *et al.* "Plasmonic Light Trapping in Thin-film Silicon Solar Cells with Improved Self-Assembled Silver Nanoparticles." Nano Letters 12(8): 4070-4076, 2012
[49] Y. Zhang, *et al*, "Improved multicrystalline Si solar cells by light trapping from Al nanoparticle enhanced antireflection coating," Opt. Mater. Express 3, 489-495, 2013
[50] Fahim, Narges F, *et al*, "Enhanced photocurrent in crystalline silicon solar cells by hybrid plasmonic antireflection coatings," Applied Physics Letters , vol.101, no.26, pp.261102,261102-5, 2012
[51] Xi Chen, *et al*, Exceeding the limit of plasmonic light trapping in textured screen-printed solar cells using Al nanoparticles and wrinkle-like graphene sheets, Light: Science & Applications, 2, 2013
[52] Zhang, Yinan; Ouyang, Zi; Stokes, Nicholas; Jia, Baohua; Shi, Zhengrong; Gu, Min, "Low cost and high performance Al nanoparticles for broadband light trapping in Si wafer solar cells," Applied Physics Letters , vol.100, no.15, pp 151101-4, 2012
[53] H. Dai, M. Li, Y. Li, H. Yu, F. Bai, and X. Ren, "Effective light trapping enhancement by plasmonic Ag nanoparticles on silicon pyramid surface," Opt. Express 20, A502-A509, 2012
[54] N. Fahim, B. Jia, Z. Shi, and M. Gu, "Simultaneous broadband light trapping and fill factor enhancement in crystalline silicon solar cells induced by Ag nanoparticles and nanoshells," Opt. Express 20, A694-A705, 2012
[55] Yufei Liu; Blayney, G.J.; Guy, O.J., "Rapid microwave growth of ZnO nanowires for low cost photovoltaics cells using reclaimed silicon substrates," Electron Devices and Solid State Circuit (EDSSC), 2012 IEEE International Conference on , pp.1,3, 3-5 Dec. 2012
[56] Yu X, Wang D, Lei D, Li G, Yang D. Efficiency improvement of silicon solar cells enabled by ZnO nanowhisker array coating, Nanoscale Res Lett, 7(1):306, 2012
[57] Yujie Fan, Peide Han, Peng Liang, Yupeng Xing, Zhou Ye, Shaoxu Hu, Differences in etching characteristics of TMAH and KOH on preparing inverted pyramids for silicon solar cells, Applied Surface Science, Vol 264, 2013

[58] Salman, Khaldun A.; Hassan, Z.; Omar, Khalid, Effect of Silicon Porosity on Solar Cell Efficiency, International Journal of Electrochemical Science, Vol. 7 Issue 1, p376-386. 11p, 2012

[59] Hui Fang *et al*, Silver catalysis in the fabrication of silicon nanowire arrays, Nanotechnology, Vol 17, 3768, 2006

[60] Stuart A. Boden ; Darren M. Bagnall; Nanostructured biomimetic moth-eye arrays in silicon by nanoimprint lithography. Proc. SPIE 7401, Biomimetics and Bioinspiration, 74010J, 2009

[61] Noboru Yamada, *et al*, Characterization of antireflection moth-eye film on crystalline silicon photovoltaic module, OPTICS EXPRESS, Vol. 19, No. S2, 2011

[62] Boden, S. A. and Bagnall, D. M., Optimization of moth-eye antireflection schemes for silicon solar cells. Prog. Photovolt: Res. Appl., 18: 195–203, 2010

[63] Erik Garnett, *et al*, Light Trapping in Silicon Nanowire Solar Cells, Nano Letters, 10 (3), 1082-1087, 2010

[64] Peng, K., Xu, Y., Wu, Y., Yan, Y., Lee, S.-T. and Zhu, J., Aligned Single-Crystalline Si Nanowire Arrays for Photovoltaic Applications. Small, 1: 1062–1067, 2005

[65] Brian, K., *et al.* "Multifunctional porous silicon nanopillar arrays: antireflection, superhydrophobicity, photoluminescence, and surface-enhanced Raman scattering." Nanotechnology 24(24): 245704, 2013

[66] Daif, O. E., Trompoukis, C., Niesen, B., Yaala, M. B., Sharma, P. P., Depauw, V. and Gordon, I. 2013. Inverted random nanopyramids patterning for crystalline silicon photovoltaics. [online] Available at: http://arxiv.org/abs/1305.6207 [Accessed: 9 Nov 2013].

[67] Z. Xu, J. Jiang, and G. Liu, "Lithography-free sub-100 nm nanocone array antireflection layer for low-cost silicon solar cell," Appl. Opt. 51, 4430-4435, 2012

[68] Qiaoyin Yang *et al*, Antireflection effects at nanostructured material interfaces and the suppression of thin-film interference, Nanotechnology, vol 24, 23, 2013

[69] Hirai, Y., *et al.* "Biomimetic bi-functional silicon nanospike-array structures prepared by using self-organized honeycomb templates and reactive ion etching." Journal of Materials Chemistry 20(48): 10804-10808, 2010

[70] Y. Hung, S. Lee, and L. Coldren, "Deep and tapered silicon photonic crystals for achieving anti-reflection and enhanced absorption," Opt. Express 18, 6841-6852, (2010)

[71] S. A. Correia *et al.*, "Eliminating Shunts from Industrial Silicon Solar Cells by Spatially Resolved Analysis", 19th EPVSEC, p. 1297, 2004

[72] Meena Dadu, A. Kapoor, K.N. Tripathi, Effect of operating current dependent series resistance on the fill factor of a solar cell, Solar Energy Materials and Solar Cells, Volume 71, Issue 2, Pages 213-218, 2002

[73] O. Breitenstein, J. P. Rakotoniaina, M.H. Al Rifai, M. Werner, Shunt Types in Crystalline Silicon Solar Cells, Progress in Photovoltaics: Research and Applications, Vol. 12, pp. 529-538, 2004

[74] J. Lindmayer and J. F. Allsion, The violet cell an improved siliocn cell. COSMAT Tech. Rev. 3, 1, 1973

[75] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, Second Edition, John Wiley & Sons, 265-313, 2011

[76] Bowden, S. ; Rohatgi, Ajeet, Rapid and Accurate Determination of Series Resistance and Fill Factor Losses in Industrial Silicon Solar Cells, Proceedings of 17th European Photovoltaic Solar Energy Conference and Exhibition, 2001

[77] D. Pysch, A. Mette, S.W. Glunz, A review and comparison of different methods to determine the series resistance of solar cells, Solar Energy Materials and Solar Cells, Volume 91, Issue 18, 6 November 2007, Pages 1698-1706

[78] Keithley Application Note: Making I-V and C-V Measurements on Solar/Photovoltaic Cells Using the Model 4200-SCS Semiconductor Characterization System

[79] Pveducation.org. 2013. Buried Contact Solar Cells | PVEducation. [online] Available at: http://pveducation.org/pvcdrom/manufacturing/buried-contract [Accessed: 9 Sep 2013].

[80] Dirk-Holger Neuhaus and Adolf Münzer, "Industrial Silicon Wafer Solar Cells," Advances in OptoElectronics, 2007

[81] DuPont™ Solamet® PV17A, Photovoltaic Metallization, Technical Data Sheet, 2012

[82] Konno Takuya, Paste For Solar Cell Electrodes, Method For The Manufacture Of Solar Cell Electrodes, And The Solar Cell , US 2010/0175754A1, 2010

[83] Horteis M, T. Gutberlet, A. Reller, and S.W. Glunz . High-temperature contact formation on n-type silicon: basic reactions and contact model for seed-layer contacts, Advanced Functional Mateials, Vol. 20, pp. 476-484, 2010

[84] Schubert G., F. Huster, and P. Fath. Physical understanding of printed thick-film front contacts of crystalline Si solar cells—Review of existing models and recent developments, Solar Energy Materials & Solar Cells, Vol. 90, pp. 3399-3406, 2006

[85] C. Ballif, D. M. Hulji´c, A. Hessler-Wysser, and G. Willeke, "Nature of the Ag-Si interface in screen-printed contacts: a detailed transmission electron microscopy study of crosssectional structures," in Proceedings of the 29th IEEE Photovoltaic Specialists Conference (PVSC '02), pp. 360–363, 2003.

[86] C Khadilkar, S Kim, T Pham, A Shaikh, S Sridharan, Characterization of silver front contact in a silicon solar cell, Solar Energy Materials and Solar Cells 2005, DOI:10.1016/j.solmat.2005.09.015

[87] Ching-Hsi Lin, Shih-Peng Hsu and Wei-Chih Hsu. Silicon Solar Cells: Structural Properties of Ag-Contacts/Si-Substrate, Solar Cells - Silicon Wafer-Based Technologies, Prof. Leonid A. Kosyachenko (Ed.), 2011

[88] Schubert G, Huster F, Fath P, Current transport mechanism in printed Ag thick film contacts to an n type emitter of a crystalline siliconsolar cell. Proceedings 19th EUPVSEC; 813–816, 2004

[89] Ballif C, Huljic DM, Willeke G, Hessler-Wyser A, Silver thick-film contacts on highly doped n-type silicon emitters: Structural and electronic properties, Applied Physics Letters; 82 : 1878–80, 2003

[90] Guy Beaucarne, Gunnar Schubert, Jaap Hoornstra, Summary of the 4th Workshop on Metallization for Crystalline Silicon Solar Cells, Energy Procedia, Vol 43, P2-11, 2013

[91] Hoenig R, Duerrschnabel M, van Mierlo W, Aabdin Z, Bernhard J, Biskupek J, Eibl O, Kaiser U, Clement F, Biro D, Investigating the nature of screen printed front side silver contacts - Aims and Results of the Research ProjectMikroSol, Proceedings of 4th Workshop on Metallization for Crystalline Silicon Solar Cells, 2013

[92] Martin A. Green, Ag requirements for silicon wafer-based solar cells Progress in Photovoltaics: Research and Applications, Volume 19, Issue 8, pages 911–916, 2011

[93] Li, Tao; Wang, Wenjing; Zhou, Chunlan; Liu, Zhengang; Zhao, Lei; Li, Hailing; Diao, Hongwei, Influence of Nickel Silicide Thin Film on Series Resistance of Silicon Solar Cells, Current Nanoscience, vol. 8, issue 4, pp. 628-631, 2012

[94] Baomin Xu; Limb, S.; Rodkin, A.; Shrader, E.; Garner, S., "Formation of very low resistance contact for silicon photovoltaic cells," Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE , vol., no., pp.003354,003358, 2012

[95] Cheolmin Park, Taeyoung Kwon, Bonggi Kim, Jonghwan Lee, Shihyun Ahn, Minkyu Ju, Nagarajan Balaji, Hoongjoo Lee, Junsin Yi, Front-side metal electrode optimization using fine line double screen printing and nickel plating for large area crystalline silicon solar cells, Materials Research Bulletin, Volume 47, Issue 10, Pages 3027-3031, 2012

[96] Butler, K. T. and Harding, J.H., A computational investigation of nickel (silicides) as potential contact layers for silicon photovoltaic cells. Journal of Physics-Condensed Matter, 25 (39), 395003, 2013

[97] Kato, T.; Adachi, S.; Aoyagi, T.; Naito, T.; Yamamoto, H.; Nojiri, T.; Yoshida, M., "A Crystalline Metallic Copper Network Application Film Produced by High-Temperature Atmospheric Sintering," Photovoltaics, IEEE Journal of , vol.2, no.4, pp.499,505, 2012

[98] Adachi, S.; Kato, T.; Aoyagi, T.; Naito, T.; Yamamoto, H.; Nojiri, T.; Kurata, Y.; Kurihara, Y.; Yoshida, M., "Development of Innovative Application Films for Silicon Solar Cells Using a Copper–Phosphorus Alloy by an Atmospheric Sintering Process," Photovoltaics, IEEE Journal of , vol.3, no.4, pp.1178,1183, 2013

[99] Janušonis, Julius; Galdikas, Algirdas; Juzumas, Valdemaras; Jaraminė, Lina; Lukštaraupis, Tomas; Andrijauskas, Darius; Janušonienė, Vida; Janušonis, Darius; Ulbikas, Juras, Electroless copper contacts for low concentration silicon solar cells,CPV-8. AIP Conference Proceedings, Volume 1477, pp. 53-56, 2012

[100] Jae Doo Lee, Hyuk Yong Kwon, Soo Hong Lee, Analysis of front metal contact for plated Ni/Cu silicon solar cell, Electronic Materials Letters, Volume 7, Issue 4, pp 349-352, 2011

[101] Dong Ho Kim, Soo Hong Lee, Investigation on plated Ni/Cu contact for mono-crystalline silicon solar cells, Electronic Materials Letters, Volume 9, Issue 5, pp 677-681, 2013

[102] Jonghwan Lee, Youn-Jung Lee, Minkyu Ju, Kyungyul Ryu, Bonggi Kim, Junsin Yi, A novel method for crystalline silicon solar cells with low contact resistance and antireflection coating by an oxidized Mg layer, Nanoscale Research Letters, 7:32, 2012

[103] Mingeon Kim, Joondong Kim, Hyunyub Kim, Jaewoo Choi, Jinjoo Park, Min Cheol Ahn, Junsin Yi, Optimization of transparent conductor-embedding front electrodes for efficient light management, Current Applied Physics, Volume 13, Issue 5, Pages 808-813, 2013

[104] S. Xie, Z. Ouyang, B. Jia, and M. Gu, "Large-size, high-uniformity, random silver nanowire networks as transparent electrodes for crystalline silicon wafer solar cells," Opt. Express, Vol 21, A355-A362, 2013

[105] Gao, Jinwei; Pei, Ke; Sun, Tianyi; Wang, Yaohui; Zhang, Linghai; Peng, Weijin; Lin, Qinggeng; Giersig, Michael; Kempa, Krzysztof; Ren, Zhifeng; Wang, Yang, Transparent Nanowire Network Electrode for Textured Semiconductors, Small, vol. 9, issue 5, p. 733-737, 2013

[106] Geissbühler J, De Wolf S, Faes A, Badel N, Demaurex B, Seif J, Tomasi A, Barraud L, Descoeudres A, Martin de Nicolas S, Paviet- Salomon B, Holovsky J, Despeisse M, Holman ZC, Papet P, Ballif C, Electrodeposited copper front metallization for High-efficiency silicon heterojunction solar cells, Presentation at 4th Workshop on Metallization for Crystalline Silicon Solar Cells, Konstanz, Germany, 2013

[107] P. Narayanan Vinod, The electrical and microstructural properties of electroplated screen-printed Ag metal contacts in crystalline silicon solar cells, RSC Adv.,3, 14106-14113, 2013

[108] S. Tutashkonko, A. Kaminski-Cachopo, C.Boulord, R. Arès, V. Aimez and M. Lemiti, Light induced silver and copper plating on silver screen-printed contacts of silicon solar cells Opto-Electronics Review Vol 19, no. 3, pp. 301-306, 2011

[109] Balucani M, Kholostov K, Nenzi P, Crescenzi R, Serenelli L, Izzi M, Tucci M, Bernardi D, Ciarniello D, New selective processing technique for solar cell, Presentation at 4th Workshop on Metallization for Crystalline Silicon Solar Cells, Konstanz, Germany, 2013

[110] Balucani, M.; Ciarniello, D.; Nenzi, P.; Bernardi, D.; Crescenzi, R.; Kholostov, K., "New selective wet processing," Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, pp.247-254, 2013

[111] Peraiah Sastry Aakella, S. Saravanan, Suhas S. Joshi, Chetan Singh Solanki, Pre-metallization processes for c-Si solar cells, Solar Energy, Volume 97, Pages 388-397, 2013

[112] Tahmina Akter and Woo Soo Kim, Reversibly Stretchable Transparent Conductive Coatings of Spray-Deposited Silver Nanowires, ACS Applied Materials & Interfaces, 4 (4), 1855-1859, 2012

[113] Madaria, AR. *et al*, "Large scale, highly conductive and patterned transparent films of silver nanowires on arbitrary substrates and their application in touch screens" Nanotechnology, Vol 22, Number 24, 2011

[114] Andreas Schneider, Rudolf Harney, Severin Aulehla, Engelbert Lemp, Simon Koch, Progress in Interconnection of Busbar-less Solar Cells by Means of Conductive Gluing, Energy Procedia, Volume 38, P387-394, 2013

[115] Schneider, A.; Rubin, L.; Rubin, G., "Solar Cell Efficiency Improvement by New Metallization Techniques - the Day4 Electrode Concept," Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference on , vol.1, no., pp.1095,1098, 7-12 May 2006

[116] Schneider A, Harney R, Aulehla S, Hummel S, Lemp E, Koch S, Schröder K. Conductive gluing as interconnection technique towards solar cells without front busbars and rear pads, Proceedings of the 27th EU PVSEC, p. 335-339, 2012

[117] Masashi Nakayama, *et al*, Lead-free Silver-paste for Fine-line Printing with Ultra-fine Mesh Screen. Presentation at 4th Workshop on Metallization for Crystalline Silicon Solar Cells, Konstanz, Germany, 2013

[118] Greulich, J.; Fellmeth, T.; Glatthaar, M.; Biro, D.; Rein, S., "Comparison of Analytical and Numerical Models for the Optimization of c-Si Solar Cells' Front Metallization," Photovoltaics, IEEE Journal of , vol.2, no.4, pp.588,591, 2012

[119] S. Olweya, A. Kalio, A. Kraft, E. Deront, A. Filipovic, J. Bartsch, M. Glatthaar, Fine-line Silver Pastes for Seed Layer Screen Printing with Varied Glass Content, Energy Procedia, Volume 43, P37-43, 2013

[120] Yu-Chou Shih; Yue Shao; Yeong-Her Lin; Shi, F.G., "Nano-sized glass frits with surface treatment for silicon solar cells," Advanced Packaging Materials (APM), 2013 IEEE International Symposium on , vol., no., pp.290,296, 2013

[121] Yu-Chou Shih, Yeong-Her Lin, Jiun-Pyng You, Frank G. Shi, Screen-Printable Silver Pastes with Nanosized Glass Frits for Silicon Solar Cells, Journal of Electronic Materials,Volume 42, Issue 3, pp 410-416, 2013

[122] Quande Che, Hongxing Yang, Lin Lu, Yuanhao Wang, Nanoparticles-aided silver front contact paste for crystalline silicon solar cells, Materials in Electronics,Volume 24, Issue 2, pp 524-528, 2013

[123] Quande Che, Hongxing Yang, Lin Lu, Yuanhao Wang, A new environmental friendly silver front contact paste for crystalline silicon solar cells, Journal of Alloys and Compounds, Volume 549, Pages 221-225, 2013

Chapter 4: Experimental Methods

In this chapter both fabrication and characterisation equipment used for the work in this thesis will be described. Due to the wide range of equipment used, only a brief explanation of the principle behind each major technique will be given. Where appropriate, referrals to comprehensive resources are given. The final section in this chapter will deal with the full process of fabricating a reclaimed silicon solar cell.

4.1 Fabrication Equipment

4.1.1 Physical Vapour Deposition

The term Physical Vapour Deposition (PVD) covers two main techniques, (i) Evaporation and (ii) Sputtering of a source material onto the required substrate. In this work, physical vapour deposition in the form of sputtering equipment was used to deposit a thin film of metal onto silicon substrates. A Kurt J Lesker PVD 75 sputter system equipped with three Torus Magnetron Sputtering sources was used. The process of sputtering involves vaporisation of atoms from the source material onto the substrate by bombarding it with energetic atomic-sized particles [1]. The energetic particles are usually ions from a gas accelerated in an electric field [1]. In the equipment used for the work, the source material was pure Silver (99.99% Ag supplied by Lesker) and Argon (99.9995% supplied by BOC) was used as the ionising gas. Before deposition the chamber of the equipment was evacuated down to a base pressure of 10^{-6} Torr. A high voltage is applied between the source material (Ag) and a substrate (Si), then electrons emanating from the surface of the source cause cascade ionisation in the gas (Ar), forming plasma, from which positive ions are attracted to the source. These ions eject atoms from the source that subsequently deposit on the substrate surface [2].

4.1.2 Chemical Vapour Deposition

Chemical Vapour Deposition (CVD) is similar in some respects to PVD sputtering but instead of the source material being a solid, in CVD the source material is in a gaseous form. CVD covers many different forms from Low Pressures Chemical Vapour Deposition (LPCVD) to Plasma Enhanced Chemical Vapour Deposition (PECVD). In this work, PECVD equipment (Oxford PlasmaLab80) was used to deposit a thin film of SiN onto silicon substrates. Fig. 4.1 shows the schematic of a PECVD chamber. Standard CVD consists of thermally activated gas-phase and surface reactions that produce a solid product at the surface [3]. In PECVD

however, the thermal activation step is replaced by electron impact of the source gas or gases, which enables a lower temperature deposition process [3]. Source gases used for SiN formation consisted of NH_3 and $5\%SiH_4+95\%N_2$.

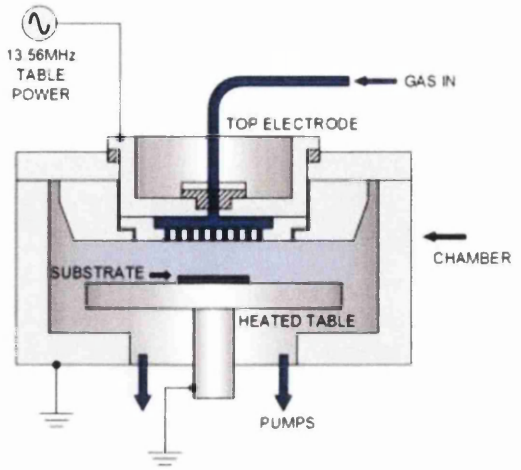


Figure 4.1: PECVD equipment schematic [4]

4.1.3 Annealing Furnaces

Three different furnaces were used in this work namely a single zone electric furnace, a 4 zone IR belt furnace and a POCL furnace:

- Single zone electric furnace: The single zone electric furnace in this work was used for several silicon exfoliation experiments. The electric furnace (Carbolite CSF1100) used simple heating coils/elements to achieve a maximum temperature of 1000°C at atmospheric pressure.
- 4 zone IR belt furnace: The 4 zone belt furnace in this work (Centrotherm 1090) was used during the high temperature annealing/firing of metallic contacts. The belt furnace had four separate zones allowing for a range of temperatures up to 1100°C. Heating was achieved by the use of infra red radiation.
- POCL furnace: The POCL furnace (Hitech furnaces) was used to dope an n-type emitter region of a silicon wafer. A POCL furnace is essentially an adapted piece of annealing equipment that allows for $POCl_3$ (Phosphoryl chloride) liquid to enter the furnace via an inert carrier gas such as nitrogen. The $POCl_3$ solution (from CVD Selectipur) is used as a phosphorous source in the diffusion process to obtain an n-type emitter layer (as phosphorous atoms have 5 valence electrons).The high temperature diffuses the dopant into the silicon forming the required n-type silicon emitter layer. More on the diffusion of the emitter region is covered later in this chapter (4.3.5).

4.1.4 Screen Printing

Screen printing is a simple technique that uses a woven mesh screen on top of which an emulsion mask is applied. When an ink is applied to the screen, only the areas where no emulsion is present can the ink pass through onto the underlying substrate. Due to the structure of the woven mesh, the ink passes through the screen and forms ink droplets on the substrate underneath. Fig.4.2 shows a schematic of the process:

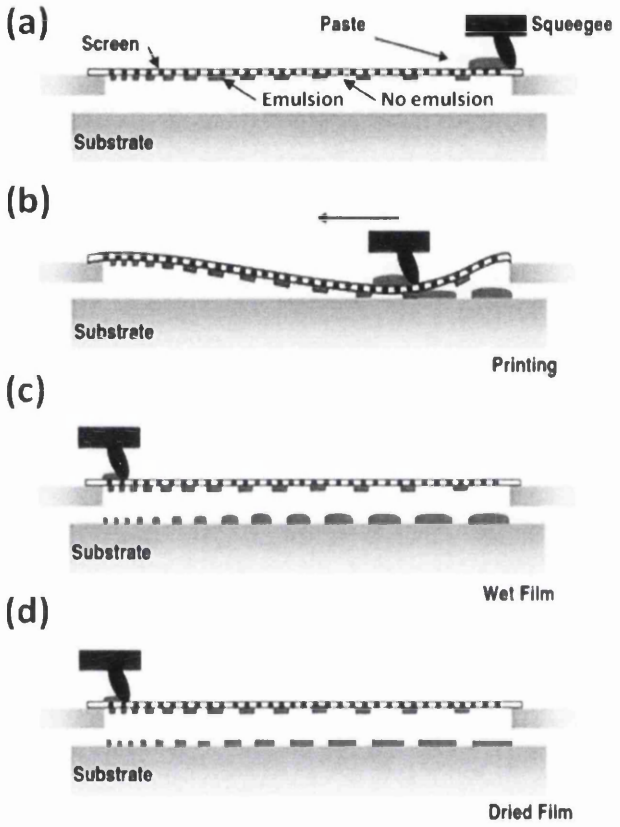


Figure 4.2: Schematic of screen printing process, adapted from [5]:

(a) Paste/Ink applied to screen
(b) Rubber squeegee draws the ink across the screen and forces it through areas in the screen where no emulsion mask is present.
(c) The result is a printed wet ink design on the underlying substrate
(d) Ink is allowed to dry

4.2 Characterisation Equipment

4.2.1 Solar Simulator/I-V measurements

A solar simulator was used in this work to provide electrical measurements of a cell under the standard AM1.5 spectrum (defined in Chapter 2 as 1000 W/m^2 at 25 °C [6]). The equipment provides valuable parameters such as I_{sc}, V_{oc}, FF and the overall efficiency of the cell. The equipment used was a Newport Oriel Sol3A Class AAA Solar Simulator equipped with a Keithley 2400 source meter with 2x2" output beam size. The simulator uses a Xenon arc lamp to provide illumination approximating that of sunlight. The source meter is then connected to the front and rear of the cell (to existing tabbing wire or directly onto busbars using electrical probes) and used for electrical I-V measurements of the cell under illumination.

4.2.2 UV-VIS-NIR Spectrophotometer

A spectrophotometer was used in this work to measure the reflectivity and reflectance of different substrates. The equipment used was a Perkin Elmer Lambda 750S equipped with a 60mm integrating sphere capable of transmittance and reflectance measurements over a range of 200-2500nm. Fig.4.3 below shows a schematic of how both transmission and reflectivity measurements are made (from the transmission schematic, Spectralon is brand of material with nearly 100% diffuse reflectance). Essentially for both transmission and reflectivity measurements a spectrometer uses a light source which is divided into spectral components and the interaction with the sample is measured using detectors (a photomultiplier for the visible range and an InGaAs detector for the NIR) [7].

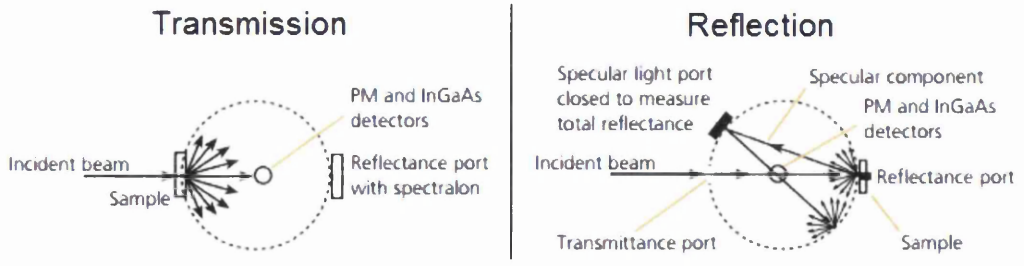


Figure 4.3: Spectrophotometer schematic of transmission and reflection measurements [8].

4.2.3 White Light Interferometry

White light interferometry was used in this work for surface topography realisation as well as surface roughness measurements. For the work a Veeco Wyko NT2000 white light optical profiler was used. Fig.4.4 depicts the schematic of a typical white light interferometer. Such equipment relies upon the interaction between a reference beam and refracted light from the sample. A white light source is firstly passed through a beam splitter to create two beams, one of which is used as a reference the second of which reflects off the sample being profiled. The beams then recombine and are imaged by a detector. The way the beams interact with one another (relating to their optical path lengths) creates fringes which reflect the topography of the sample.

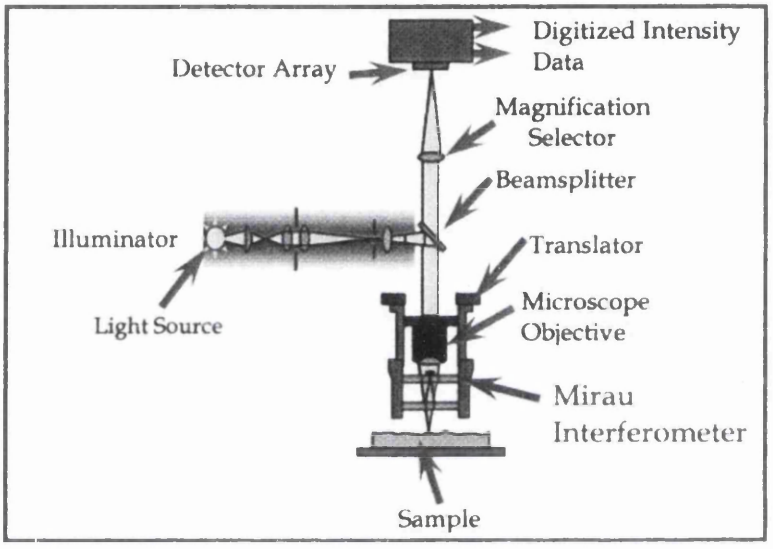


Figure 4.4: Schematic of white light interferometer setup [9]

4.2.4 Scanning Electron Microscopy (SEM) with Energy-Dispersive X-ray (EDX)

Scanning Electron Microscopy is a very important imaging technique used to image and measure at the nanoscale. SEM was used throughout the work to characterise structures and depositions alike. For the work a Hitachi S4800 Ultra-High Resolution FE-SEM equipped with EDX was used. The basic operational principle of SEM is the interaction of the sample with electrons. Fig.4.5 illustrates a schematic of such a system. An electron beam is accelerated through a high voltage (kV range) through a series of apertures and electromagnetic lenses in order to produce a narrow beam of electrons. The response of the sample to the beam causes different effects depending upon the sample. Typically the sample emits secondary electrons which are collected by a detector inside the chamber. From this data the topography of the surface is generated.

Energy-Dispersive X-ray Spectroscopy is used to provide elemental analysis of samples. EDX can be performed by the addition of a suitable detector on a standard SEM system. X-rays emitted by the sample during exposure to the electron beam, are collected by the detector. These X-rays hold valuable information about the elemental composition of the sample.

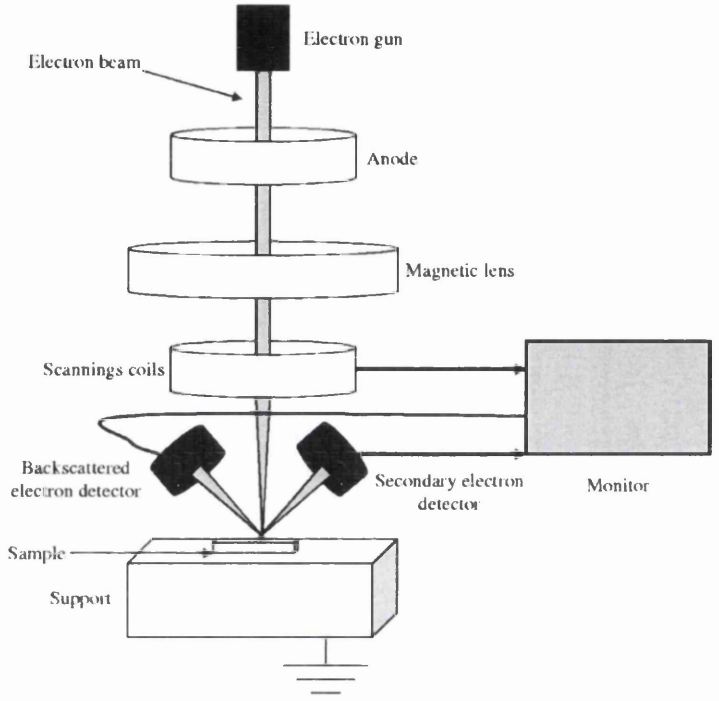


Figure 4.5: Schematic of Scanning Electron Microscopy equipment [10]

4.3 Solar Cell Fabrication

This section describes how silicon solar cells used in this work are processed. The sequences used here are the same as that used in industry but on a lower volume scale. In this work however, reclaimed silicon substrates are used because of their green credentials (as described below). Due to this, extra processing steps have been added to address the use of such substrates. The basic fabrication process consists of:

- Starting wafer from semiconductor industry
- Wafer Reclaim
- Wafer Grinding/Thinning
- Surface Texturing
- Doping of emitter junction
- Phosphorous glass removal, backside grinding and edge isolation
- Cutting/Dicing (Circular wafer to Pseudo Square)
- ARC deposition
- Screen Printing of electrical contacts
- Firing of electrical contacts
- Cell Testing

4.3.1 Starting Wafer

The semiconductor industry typically uses high purity 200mm diameter crystalline silicon wafers for semiconductor device fabrication. Before such complex devices can be manufactured, every aspect of the device fabrication process must be thoroughly tested. Processes often include thin film deposition as well as diffusion of different materials. Due to the vigorous testing procedures, large numbers of test wafers are commissioned. The test wafers must be of the same purity as those that will finally be used for device fabrication. Once verification of the process is made on the test wafer, the test wafer is no longer required. Simply disposing of the wafer at this point would have significant cost implications to the industry. The wafer is still perfectly usable, although the test film/structures must be removed. The wafer reclamation process is concerned with such a task.

4.3.2 Wafer Reclamation

The process of wafer reclamation is to take the used test wafers and reclaim them back to their starting condition so they can be reused once more. The basic process adopted for semiconductor wafer reclamation is [11]:

1. Removal of deposited films of foreign material from the front and back surfaces as well as the edges of the wafer.
2. Removal of a layer from one surface of the wafer substrate, to remove any doped and diffused regions.
3. Polishing the surface of the wafer to obtain the required surface properties and flatness.
4. Cleaning of the wafer to yield a silicon surface suitable for processing in a semiconductor production line.

Once the test wafer has had any deposited films removed from its surface and has been re-polished, it can then be returned back to the semiconductor company. The test wafer can then be used once again for process testing. After the test has performed its function a second time it is then sent for reclamation and the process repeated. Unfortunately after several reclamation cycles the test wafer becomes too thin for use by the semiconductor company. This is primarily due to the insufficient thickness of the wafer. During each reclamation cycle, a layer of the silicon is physically removed. Therefore after several cycles the wafer is much thinner than it started out as. The risk of breakage of the wafer during test depositions by the semiconductor company is too high so the wafer finally becomes redundant.

The company sponsor for my PhD is Purewafer Plc, a worldwide leader in wafer reclamation with facilities in both the UK and USA. Purewafer reclaim silicon wafers for some of the largest semiconductor companies in the world. Pure Wafer realised that once the test wafers became too thin they could potentially be used for silicon solar cell production instead of being scraped as was often the case. In 2009 they collaborated with Swansea University to produce the first silicon solar cell from reclaimed silicon wafers. Such a cell offers a far lower energy payback time than any other crystalline silicon solar cell. This is because other c-Si cells are purposely made, with a large amount of energy being required to produce the silicon starting material (Si melt at upwards of 1400°C). As the material for reclaimed wafers essentially is a waste material, the energy required to first produce the substrate can be neglected as it was originally designed for semiconductor

industry use. Cells made from reclaimed wafers can offer significant cost savings over other solar cells due to the utilisation of a scrap silicon material.

All silicon substrates used in this work are reclaimed materials, kindly provided by Purewafer Plc. The reclaimed wafers are p-type (100) monocrystalline silicon with resistivity of 10-30 Ωcm^{-1}. Although not ideal resistivity's for PV applications, the cost and energy savings outweigh the shortfalls in material suitability.

4.3.3 Wafer Grinding/Thinning

After the reclamation process the wafers are ground from a starting thickness of 600μm down to a common industrially used thickness of 180μm in order to reduce the series resistance of the bulk wafer. Thinning of the wafer is achieved by mechanically grinding down the back surface of the wafer which grinds away the silicon using a rotating abrasive pad. Fig.4.6 shows an image of the robotic mechanical grinding equipment used.

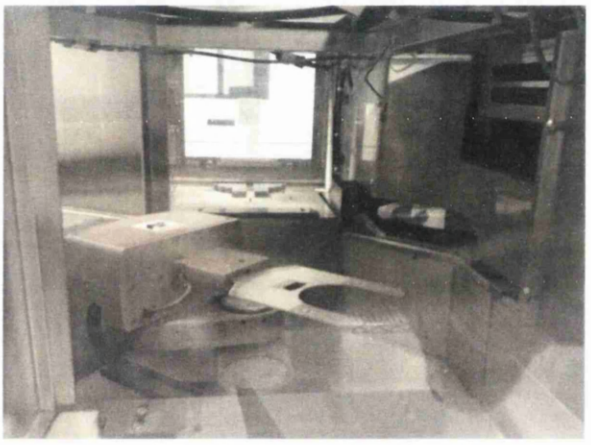


Figure 4.6: Mechanical grinding equipment for wafer thinning

4.3.4 Surface Texturing

After the wafer had been ground to the required thickness, the surface is etched to produce micro-pyramid textured features for light trapping. This is achieved by geometrical texturing of the surface by anisotropic etching using potassium hydroxide (KOH). Before etching, wafers were cleaned for 10 minutes with a solution of de-ionised water, hydrogen peroxide and ammonia hydroxide (SC1 clean). The native oxide of the wafer was then removed in 49% Hydrofluoric acid (HF) for 1 min at 70°C followed by rinsing in de-ionised water. The anisotropic etch consisted of 10.7% isopropyl alcohol (IPA), 3.2wt % KOH, and 86.1% de-ionised water. The wafers were processed in the solution for 28 minutes at a temperature of 80°C. The result from the etching process was the creation of a matt finish

that consisted of microscale square based pyramids which can be seen in the SEM image of fig.4.7. More information on the anti reflectivity properties of a textured surface can be found in Chapter 3 and 4 of this thesis.

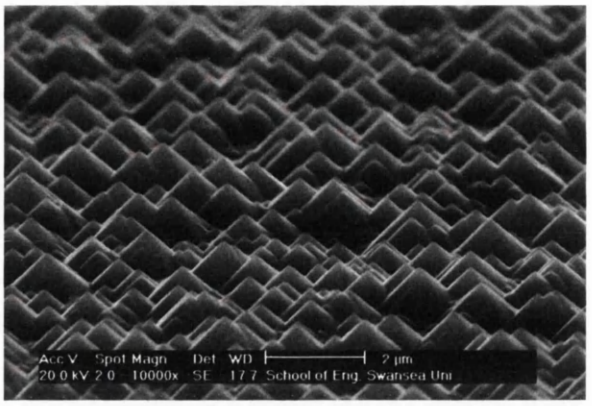


Figure 4.7: SEM of textured silicon by KOH etching

4.3.5 Doping of n-type emitter junction

The next step of cell production was doping of the n-type emitter junction to create the necessary p-n junction. The doping was achieved by $POCl_3$ deposition and diffusion. An emitter depth of 800nm with a sheet resistance of 50-60Ω/□ was targeted). $POCl_3$ doping was achieved using a specially designed diffusion furnace as shown in fig.4.8. $POCl_3$ doping was conducted at 840°C for 35 minutes followed by a drive in/anneal cycle of 840°C for 45 minutes.

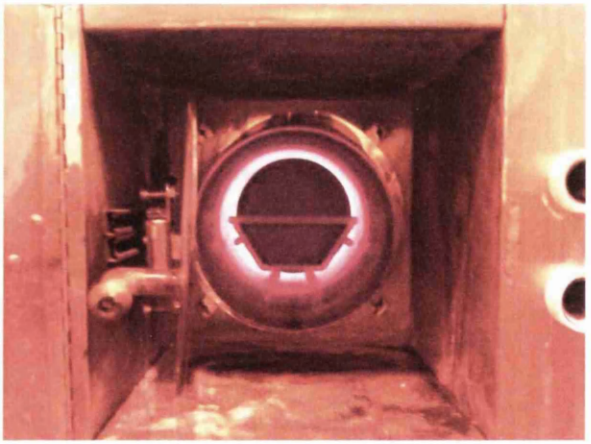


Figure 4.8: N-type emitter doping using POCl furnace

4.3.6 Phosphorous glass removal, backside grinding and edge isolation

The diffusion process leaves a phosphorous glass layer on the surface of the silicon wafer consisting of phosphorous silicate. This layer is simply removed by etching in HF for two minutes. During the doping process, an n-type region is not just formed at the front surface

of the wafer but on the back and the sides of the wafer also. After removal of the glass using HF, the edges of the wafer are finished by an abrasion process to remove the junction. The rear n-type layer is removed using back-side grinding to remove 10μm of material. The final result is an n-type emitter only at the surface of the silicon wafer.

4.3.7 Cutting/Dicing

At this stage, all cell processing steps have been performed on a 200mm diameter wafer. Unfortunately circular wafers cannot be arranged space efficiently in an assembled solar module. Large spaces are left between the round cells therefore minimising the power output of a standard sized module. The solution is to cut the round wafer into a pseudo square cell, roughly 156mm x 156mm. The straight edges of the cells allow for a tighter packing density than possible for round cells. The circular wafers are cut into the square shape using a dicing saw, incorporating a diamond edged cutting disc revolving tens of thousands times a minute. The cutting of a circular wafer into a pseudo square is shown in fig.4.9a and b respectively.

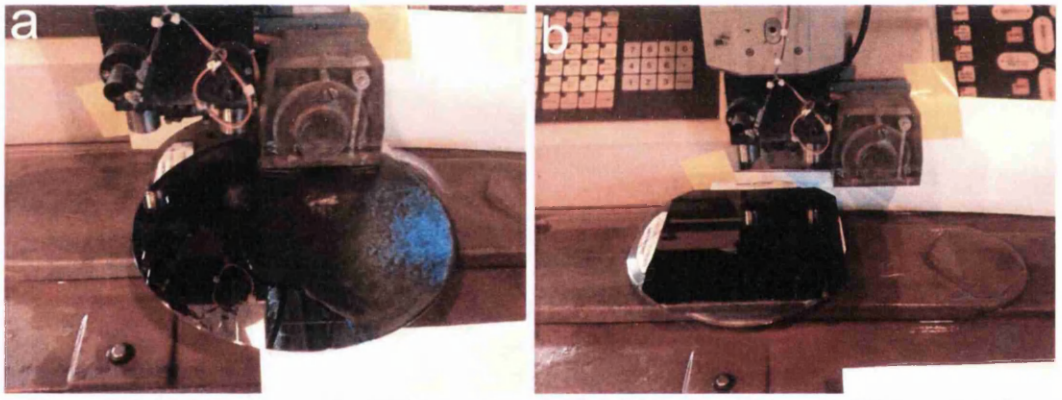


Figure 4.9: Dicing of a circular 200mm silicon wafer (a), into a 156mm x 156mm pseudo square (b)

4.3.8 ARC deposition

For enhancement of the anti-reflective properties of the solar cell, a silicon nitride ARC layer was deposited on the textured, doped wafer. The coating was produced using plasma enhanced chemical vapour deposition (PECVD). An optimum coating with a refractive index close to 1.87 and 80nm in depth was deposited. The process conditions used for such an ARC are:

- Process gases: NH_3 and $5\%SiH_4+95\%N_2$
- Flow rate: NH_3 = 50sccm and $5\%SiH_4+95\%N_2$ = 100sccm

- Chamber Pressure: 1000mTorr
- RF Power: 20W
- Stage Temperature: 250°C
- Duration of deposition: 360seconds

After the deposition, the surface of the silicon wafer had a dark blue appearance as can be seen in fig.4.10.

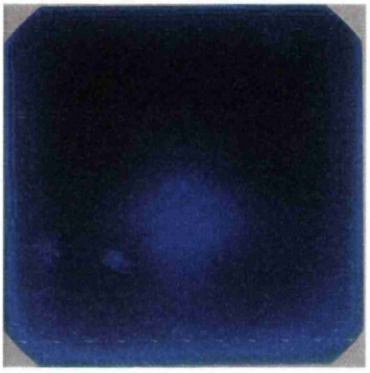


Figure 4.10: SiN ARC coating on textured Si substrate

4.3.9 Screen Printing of electrical contacts

Now that the cell had been completed, electrical contacts were printed onto the cell. Screen printing was the method of choice for contact formation onto the silicon cell. The front contact received a standard H-bridge type contact consisted of silver gridlines and busbars. Before printing of the rear contact, the silver paste was dried at 50°C for 10 minutes. The rear contact consisted of aluminium block pads with a silver/aluminium interconnect. Once again after printing the contacts were dried. Fig.4.11 shows the front and rear of the cell after screen printing of the electrical contacts.

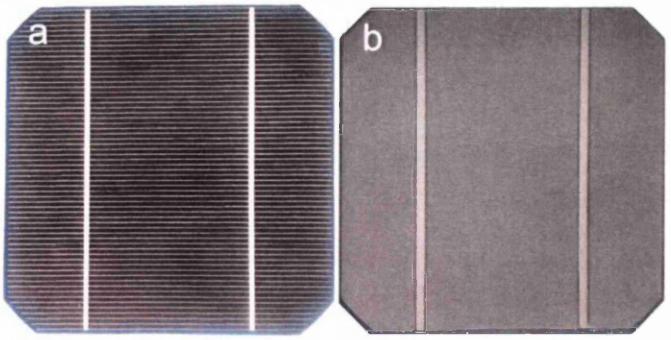


Figure 4.11: Electrical Contacts a) Front surface b) Rear Surface

4.3.10 Firing of electrical contacts

In order for a sufficient electrical contact to be made with the silicon, a high temperature firing step was used to co-fire the front and rear contacts. The high temperature process was conducted using a four zone IR belt furnace. The firing profile recommended by the paste manufacturer (DuPont) is shown in fig.4.12a. The different zones are required to evaporate the solvents from the contact paste at lower temperature before entering the high temperature zone that sinters the contacts and punches through the ARC to obtain a contact directly to the silicon substrate. The four zone furnace used is shown in fig.4.12b.

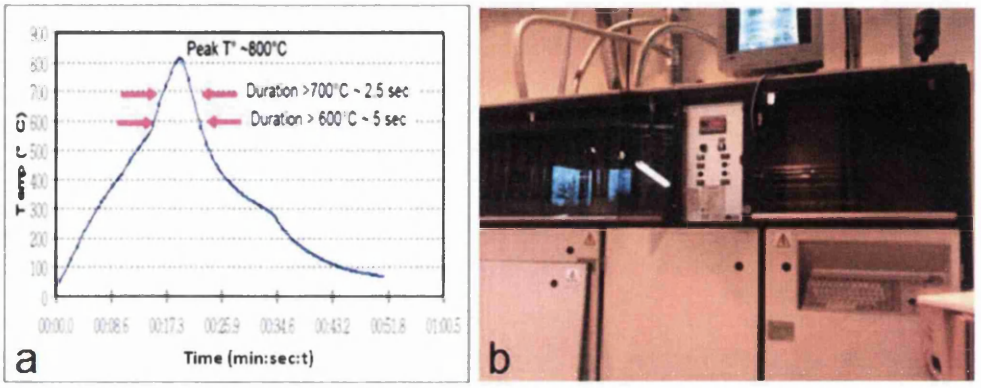


Figure 4.12: a) Contact firing profile [12], b) 4 Zone firiing furnace

4.3.11 Cell Testing

Now that a functioning solar cell had been produced, electrical measurements were performed on the devices to make sure they were operating correctly. A solar tester was used (fig.4.13) to give important electrical parameters such as; V_{oc}, I_{sc}, J_{sc}, I_{max}, V_{max}, Fill Factor, and efficiency of the cell. Detailed explanation of these parameters is given in Chapter 2 of this work.

Figure 4.13: Oriel solar tester equipment used to measure cell performance

[1] Handbook of Physical Vapor Deposition (PVD) Processing, Second Edition, Donald M. Mattox, Elsevier, 2010
[2] Lesker.com. 2014. Kurt J. Lesker Company | R&D Magnetron Sputtering Sources Overview | Vacuum Science is our Business. [online] Available at: http://www.lesker.com/newweb/Deposition_Sources/TechNotes_Sputtering.cfm [Accessed: 3 Dec 2013]
[3] M. A. Lieberman, A.J. Lichtenberg, Principles of Plasma Discharges and Materials Processing, Second Edition, John Wiley and Sons, 2005
[4] Oxford-instruments.com. PECVD - Oxford Instruments. [online] Available at: http://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition/pecvd [Accessed: 3 Dec 2013].
[5] Gonzalez-Macia, L., *et al.* Advanced printing and deposition methodologies for the fabrication of biosensors and biodevices. Analyst 135(5): 845-867, 2010
[6] J.F. Randall, J. Jacot, Is AM1.5 applicable in practice? Modelling eight photovoltaic materials with respect to light intensity and two spectra, Renewable Energy, Vol.28, Issue 12, P1851-1864, 2003
[7] Björn, L. The Amateur Scientist's Spectrophotometer. Photobiology. L. Björn, Springer: 647-658, 2008
[8] Tams, C. Perkin Elmer Application Note, The Use of UV/Vis/NIR Spectroscopy in the Development of Photovoltaic Cells, 008954_01, 2009
[9] James C. Wyant; White light interferometry. Proc. SPIE 4737, Holography: A Tribute to Yuri Denisyuk and Emmett Leith, 98, 2002
[10] Gagnadre, C., *et al.* Electron microscopy pictures, mathematical model and approximate solution of the surface potential. Kybernetes 38(5): 780-788, 2009
[11] Lewis, David John, Process for reclaiming Si wafers, EP1205968A2, 2002
[12] Guide for DuPont Solamet Photovoltaic Metallization Materials, L-13909, 09/07

Chapter 5: Ultra-thin Wafer Based Crystalline Silicon

5.1 Introduction

For high efficiency silicon photovoltaic devices, the substrate quality is extremely important and heavily influences the efficiency of a cell. Despite many recent developments in material enhancement, mono-crystalline silicon still offers the highest quality of all the silicon types. Producing such high grade material comes at a cost and therefore using as little material as possible is paramount.

In the ever increasing market for silicon solar cells, customers expect high quality products at reasonable prices. Silicon solar cells are fabricated using a wafer obtained from a silicon ingot. The thickness of each wafer ultimately dictates the amount of silicon that is used for a single cell. In the last decade there has been a large leap forward in techniques developed to obtain a wafer that is economically viable for energy production. Since almost 50% [1] of the entire cost of a mono-crystalline solar cell panel is related to the silicon wafer, reducing material consumption ultimately leads to a cost reduction. (Cell and module processing account for the other 20% and 30% of panel cost respectively [1])

There have been several innovative processes developed to produce wafers ranging from conventional sawing, to grinding and chemical etching techniques. Currently, the most commonly used method is multi-wire saw wafering. The method outlined in fig.5.1 uses a series of wires in abrasive slurry to cut through the silicon ingots, producing thin wafers. The diameter of the wire is of critical importance as this amount of material is essentially lost each time a cut is made. The diameter of the wire is often as thick as the wafers produced. The material lost during wafering is often referred to as the kerf-loss and is kept at a minimum during the process, although 50% of the silicon material can be lost as waste. Typical wafer thickness is now around 180µm, compared to in the 1990's where it was as thick as 350µm [2].

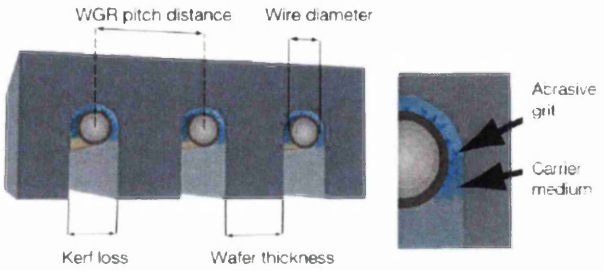


Figure 5.1: Multi-wire saw wafering schematic [3].

Despite the drive for ever decreasing material use for silicon photovoltaics, the minimum wafer thickness to preserve cell efficiency must also be considered. From literature, the minimum cell thickness (where there is no detrimental loss in the theoretical efficiency limit) is around 40μm [4]. The limit therefore means that 140um of silicon in a modern commercially produced silicon solar is not required. Such excess material usage is prohibiting further cost reductions in the silicon substrate for photovoltaics.

Recently there has been a lot of research around kerf-loss free methods where no material is wasted. One article alone identified over 18 kerf-free wafering methods [5]. More information on these processes can be found in Chapter 3. Despite the various processes, currently none are being commercially used in industry, mainly due to the complex equipment and processing required. One method of particular interest relies upon simple processing conditions that already existing in a photovoltaic manufacturing facility. The method is called silicon exfoliation and relies upon mechanical stress to cleave several wafers from a single parent wafer substrate [6, 7]. The process involves simple procedures to apply a metallic layer onto a silicon wafer followed by a thermal cycle. Rapid heating and cooling causes the metallic layer to peel from the parent wafer with a thin layer of silicon attached to the contact. The method is not only kerf-loss free but can also produce ultra-thin silicon wafers. Ultra-thin wafers are typically less than 40μm thick, whilst thin wafers are deemed less than 100μm [2]. Silicon exfoliation is able to produce wafers perfectly suited to photovoltaic devices being 40μm thick.

The exfoliation of an ultra-thin layer of silicon relies heavily on the thermal expansion co-efficient of the metallic layer deposited onto the parent wafer. The whole process is depicted in fig.5.2. Once the metallic layer has been applied and dried at low temperature, the wafer is 'fired' (at several hundred degrees) which is essentially a high temperature processing step. This procedure is typically used in conventional solar cell fabrication to create a uniform electrically conducting contact. However, in the exfoliation processes the same firing cycle is used to create the necessary expansion of the contact. If there is a large coefficient of thermal expansion (CTE) mismatch between the metallic layer and the Si substrate, when the wafer exits the furnace into the cooling zone, the rapid temperature difference induces thermo-mechanical stress between the metallic layer and the silicon semiconductor substrate. The thermal mismatch creates tensile stress parallel to the metallic layer surface which can be used to 'peel' away a thin layer of silicon that is attached to the metallic layer (fig.5.3).

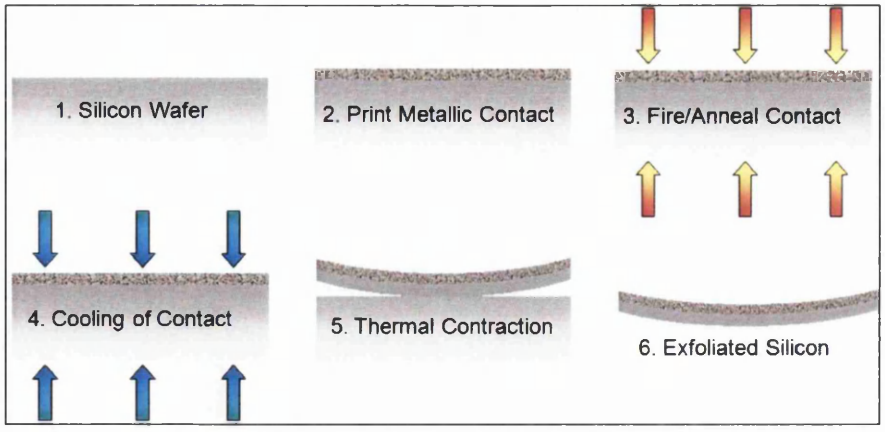


Figure 5.2: Silicon Exfoliation Process

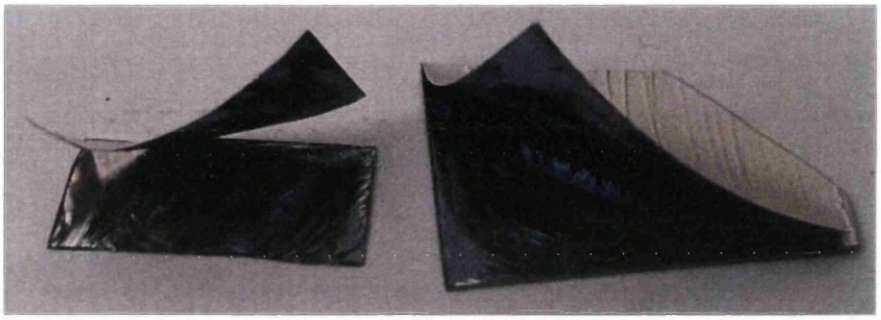


Figure 5.3: Silicon foil and corresponding metallic layer (after exfoliation) partially attached to parent substrate

Despite the research already conducted in the area of exfoliation by induced cleaving, there are many factors unexplored. The purpose of the experimentation undertaken in this study is to focus upon key aspects in relation to the silicon exfoliation process. Factors investigated include metallic layer thickness and composition, printing methods, annealing temperatures and the effects of substrate surface on the process. After investigating the critical parameters listed above, a repeatable recipe could be formed to produce ultra-thin silicon foils around 40um in thickness. Investigations were concluded by producing a fully functioning silicon solar cell from an exfoliated ultrathin substrate. This work is the first reported in depth analysis on the processing conditions for the exfoliation technique.

5.2 Experimental Procedure

Recipe conditions constantly evolved during the progression of the work, so a general procedure will be highlighted upon which parameters were varied one at a time.

Reclaimed polished and textured silicon wafers, supplied by Pure Wafer Plc, were cut into 5cm x 5cm samples. As every wafer undergoes a rigorous cleaning procedure at the factory (complying with the requirements of the microelectronics industry) additional cleaning was not required. Where textured substrates were used, texturing was produced at the factory using KOH wet etching.

Each sample was either screen printed or stencil coated with DuPont™ Solamet® metallic paste (information on the printing processes as well as paste composition are given in the experimental work). Such pastes are used for front and rear contact formation on silicon solar cells. After application, the metallic layers were dried at 150°C for 10 minutes before annealing/firing. Firing was conducted either in a single zone electrical furnace or a four zone infrared belt furnace. Firing temperatures ranged from 450 to 975°C.

After silicon exfoliation, measurements and surface characterisation was performed with a Hitachi S4800 Scanning electron Microscope. For additional surface topographical information, white light Interferometry was conducted with a Veeco NT-2000 Interferometer. For electrical efficiency measurements, a Newport Oriel® I-V Test Station was used at standard AM1.5 solar spectrum.

5.3 Experimentation Results

5.3.1 Firing Temperature

The first series of experiments relating to exfoliation were to assess annealing/firing temperatures. The temperature at which the contact is fired can be critical. In normal use the metallic ink has a strict firing regime that is specifically designed for the best electrical contact to silicon, whilst having sufficient diffusion into and adhesion to the substrate. Metallic layers specifically used for silicon exfoliation, have different objectives to those the ink was designed around.

In exfoliation, a substantial temperature difference is required in order for the contact to expand then contract again during cooling. A crucial parameter during the process is that the metallic layer remains in contact with the silicon. If the layer expands and contracts independently of the silicon, it will simply detach itself without any exfoliation of the substrate. Experiments were conducted in order to observe the effects of temperature on the exfoliation process using three commercially produced DuPont pastes. The pastes chosen were silver (DuPont PV149), aluminium (PV381) and a silver/aluminium mixture (PV202).

For the work, 300µm thick, single side textured silicon substrates were used (which are typical anti-reflective substrate for silicon solar cells). The pastes were applied to each sample using screen printing as demonstrated in fig.5.4 (further details on the process are given in Chapter 4). After application of the metallic pastes, a drying cycle was adopted (oven drying at 150°C for 10 minutes) as recommended by the ink manufacturer [8]. Subsequent annealing/firing of the samples took place in a single zone electric furnace (fig.5.5) at temperatures ranging from 600-1000°C. After the samples were fired, they were removed from the furnace and left to rapidly cool at room temperature (22.7°C).

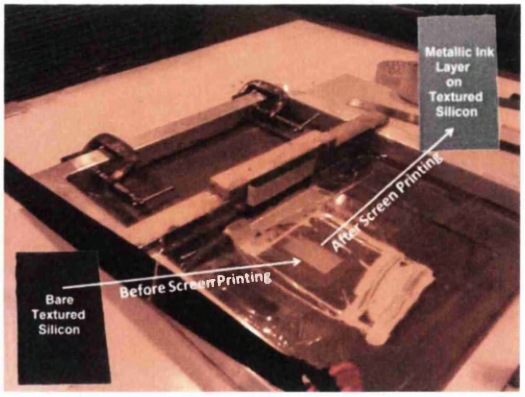


Figure 5.4: Image of screen printing apparatus

Figure 5.5: Single zone electric furnace

After each sample had cooled (in order to be handled safely), each was visually assessed to observe the final adhesion of the metallic contact to silicon. A sharp pointed tool was used to verify adhesion by scratching the contact. Results from the experimentation are shown in Table 5.1.

Sample Number	Metallic Paste Used	Firing Temp of Single Zone Furnace (°C)	Time at Firing Temp (s)	Quality of Contact Adhesion
1	Aluminium	640	25	Poor
2	Aluminium	780	25	Poor
3	Aluminium	880	25	Excellent
4	Aluminium	980	25	Excellent
5	Aluminium	980	60	Excellent
6	Silver Aluminium Mix	640	25	Poor
7	Silver Aluminium Mix	780	25	Average
8	Silver Aluminium Mix	880	25	Good
9	Silver Aluminium Mix	980	25	Excellent
10	Silver Aluminium Mix	980	60	Excellent
11	Silver	640	25	Poor
12	Silver	780	25	Good
13	Silver	880	25	Excellent
14	Silver	980	25	Excellent
15	Silver	980	60	Excellent

Table 5.1: Firing temperature in relation to contact adhesion

The samples that were screen printed with aluminium paste (Samples 1-5, Table 5.1), reacted very differently to firing temperatures. At 640 and 780°C the aluminium appeared light grey in colour with a powdery textured. Adhesion to silicon was poor, such that the metallic layer could be scratched away from the substrate with relative ease. At higher temperatures, a physical/permanent contact was made between the two materials. Samples fired at 880°C and 980°C exhibited excellent adhesion with a dark grey

appearance. Firing at 980°C for an extended time (60s) once more created an excellent contact, with the metallic layer more dark brown in colour. Consulting the metallic paste guide, supplied by the manufacturer [8] aluminium contacts light grey in appearance are indicative of under-firing, with dark brown indicative of over-firing. The ideal contact colour is mid grey for an optimal firing process. The colour description relates well to the experimental results. Light grey under-fired samples (fig.5.6a) were observed at 640 and 780°C, well fired dark grey samples (fig.5.6b) occurred from 25s at 880 and 980°C whilst samples annealed for a longer period of time at 980°C came out over-fired and dark brown (fig.5.6c).

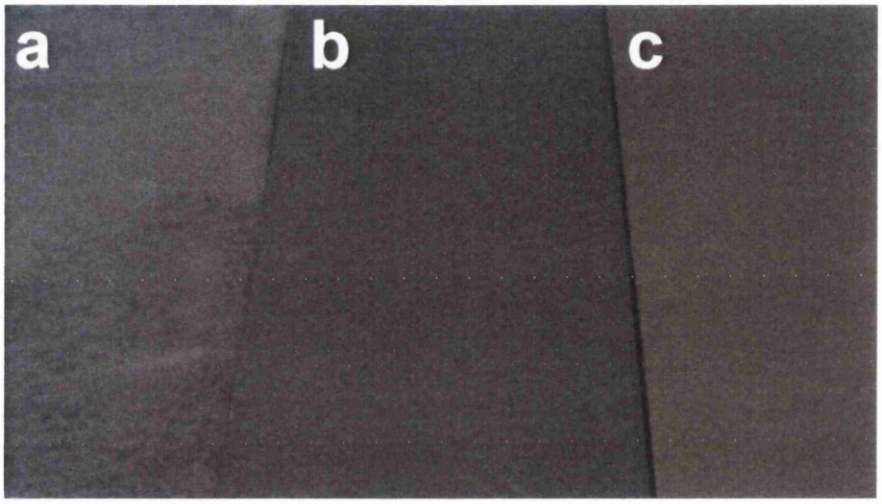


Figure 5.6: Aluminium contacts after firing (a) Under-fired, (b) Optimally fired, (c) Over-fired

The next batch of samples fired (samples 6-10, Table 5.1) were screen printed with an aluminium/silver paste mix. At 640 and 780°C the metallic layer appeared light yellow/cream in colour. The adhesion of the sample fired at 640°C was poor and the contact easily removed. At 780°C the layer had bonded better to the silicon substrate, but some areas around the edge of the sample could still be scratched away. At 880 and 980°C the aluminium/silver contact showed greater adhesion, with the contact able to resist scratching and prying from the substrate. The contact remained a light cream colour. Firing at 980°C for an extended time (60s) did not change the adhesive qualities of the contact, although a very small colour change (darker in appearance) was observed. Unfortunately the slight colour change was not apparent from photographs.

The final silicon substrates were printed with silver paste (samples 11-15, Table 5.1). At all temperatures, the paste remained a yellow/cream colour very similar to that of

the aluminium/silver contacts. At 640°C adhesion to silicon was poor, such that the metallic layer could be scratched away from the substrate with relative ease. At 780°C adhesion increased to form a good contact, resistant to scratching across most of the sample. Samples fired at 880°C and 980°C exhibited the best adhesion. Firing at 980°C for an extended time (60s) also proved to create an excellent contact with no significant change in colour.

From the firing trials conducted, it was apparent that temperature affected the adhesion and properties of the contacts. For aluminium paste, firing at temperatures below 780°C resulted in the aluminium not forming a complete contact. Such a formed layer unsurprisingly had very poor adhesion to silicon. Firing at an elevated temperate of 880-980°C provided the required heat to form a complete contact with excellent adhesion. Silver aluminium paste also required higher temperatures to form good contacts. A temperature of 980°C was found to give a very good result. Reduced temperatures led to small areas of the metallic layer having poor adhesion to silicon. For silver paste, a trait very similar to that of aluminium and aluminium/silver was observed. Once again firing at a temperate of 880-980°C provided an excellent metallic contact. It is important to note that no silicon exfoliation took place during the annealing process.

5.3.2 Contact Thickness

From previous work focused around firing of metallic pastes, none of the single screen printed samples exhibited signs of exfoliation. As the exfoliation process relies upon mechanical forces from the thermal mismatch of materials, it was therefore apparent that the thickness of such materials could have a significant effect on the process. Trials were conducted to ascertain if the thickness of the metallic layer would indeed influence the silicon exfoliation process.

Single side textured silicon substrates were again chosen, along with screen printing for the metallic layers. For the trials, three silicon samples were dedicated for each metallic paste. On each of these three substrates a different thickness of paste was printed. The first received a single screen printed layer, the second two screen printed layers and the third three layers. After each layer was screen printed the standard drying cycle was implemented. Following the final dry cycle, firing was performed in an electric furnace (as used previously). For simplicity, the samples were fired at 980°C for 25 seconds. The temperature and duration was chosen as previous trials showed that such parameters created well adhered contacts for all three paste compositions.

The single layer of screen printed metallic ink behaved as previously trialled, with excellent well adhered contacts being made to the silicon substrate with no de-lamination. Whilst firing the second batch of samples (screen printed with two layers of ink) the silver printed sample underwent partial silicon exfoliation (fig.5.7). However, samples printed with 2 layers of aluminium and aluminium/silver did not exhibit any exfoliation (fig.5.8).

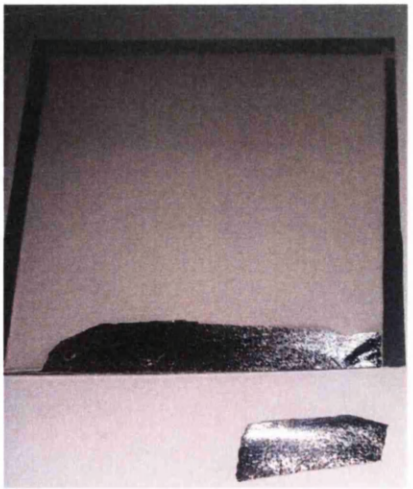


Figure 5.7: Sample with two screen printed layers of silver paste, resulting in exfoliation of a small area of the sample

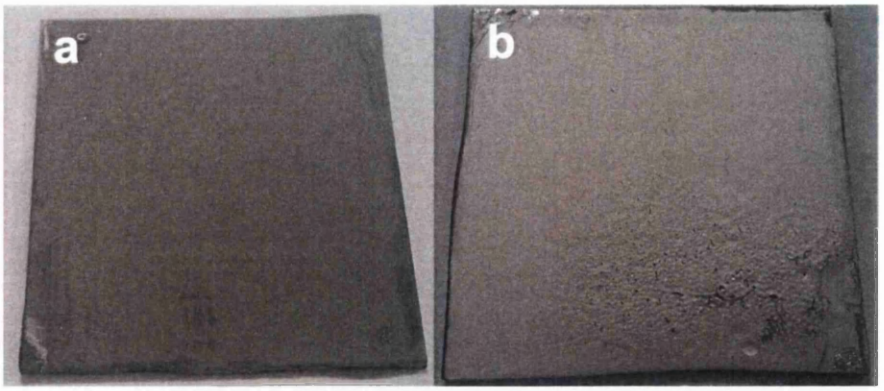


Figure 5.8: Sample with two screen printed layers of: a) aluminium paste, b) aluminium silver paste

From Fig.5.7 it can be seen that a small area of the silver contact has de-laminated from the edge of the sample. Silicon has been exfoliated from the substrate by the metallic contact peeling away. The result is a separate metallic layer attached to a thin silicon foil. Metallic paste samples printed with three layers of paste exhibited similar traits as those printed with two. Both aluminium and aluminium silver mix samples did not show any signs of exfoliation. Silver paste samples did however exfoliate. With the three layers of paste, exfoliation of the sample was far more pronounced (fig.5.9).

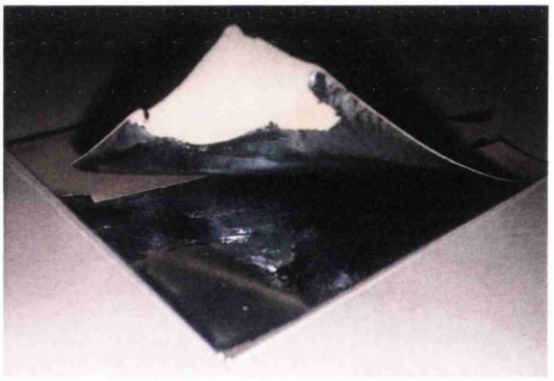


Figure 5.9: Sample with three screen printed layers of silver paste

From investigating metallic paste thickness, it became apparent that only one of the three screen printable pastes (formulated for silicon solar cell applications) worked for the exfoliation process. Aluminium and aluminium/silver mix pastes were unable to cause any exfoliation in the trials. As both the pastes are formulated for rear contact use on a silicon solar cell, they have different additives to that of pastes manufactured for top contacts. From the literature [9] silicon solar cell silver front contact pastes have the addition of a glass frit. The glass frit softens at a relatively low temperature of 450-550°C [10] and alloys with the silicon surface. Unlike the other pastes, when the silver paste is

fired in the furnace, the glass frit softens at the silicon silver junction and essentially fuses the two different materials at the junction into one conglomerate layer. Upon cooling a permanent contact is formed. When the silver layer is sufficiently thick enough, a high tensile force is created due to the thermal mismatch between the two materials (silicon and silver), and the silver contact peels away from the substrate. Because the silver and silicon are bonded together, a thin layer of silicon is exfoliated from the substrate during the process. From the trials, the minimum thickness of silver was found to be two screen printed layers.

Once the minimum silver contact thickness had been established, White Light Interferometry was performed in order to accurately measure the fired thickness of the 2 layer screen printed contact.

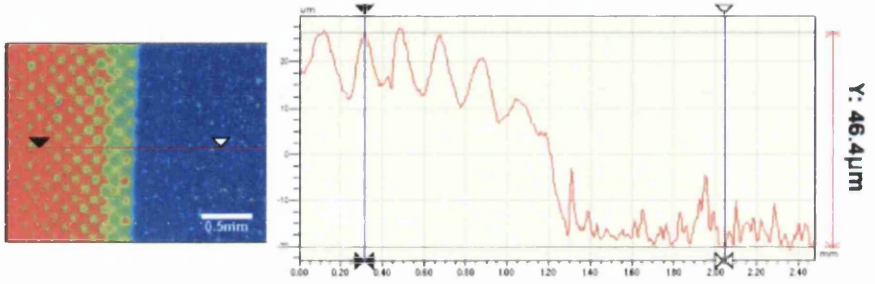


Figure 5.10: Thickness measurement for double screen printed silver contact using white light interferometry

From fig.5.10 it is apparent that the double printed fired contact (that had facilitated exfoliation) was around 46µm thick. In conclusion, for any exfoliation to reliably occur on a textured silicon substrate, a silver metallic contact thicker than 46µm is required.

5.3.3 Printing Methods

Silicon exfoliation was found to require a silver contact thicker than 46µm (2 layers of screen printed paste) to successfully take place. Screen printing several layers of the metallic ink becomes time and labour intensive due to drying cycles that must be adopted in between printing of each layer. Screen printing in the area of photovoltaics is inherently designed for depositing layers of around 20µm onto substrates. Other printing and coating techniques can be used to yield thicker metallic layers in one deposition. One of the simplest techniques is stencil coating, where a squeegee is used to deposit an ink or paste through an open mask/stencil. The thickness of the stencil material ultimately dictates the thickness of the printed contact. Stencil coating was analysed as a viable alternative for printing the silver contacts for silicon exfoliation. Stencil coating was performed on textured silicon substrates, which were subsequently dried and fired using the same conditions as for screen printed samples (980°C for 25s). The stencil was constructed from a 50µm thick PET sheet with a window removed, through which the contact was printed and dried at 150°C.

Upon firing and subsequent cooling, the stencil coated contact partially peeled away from the substrate, exfoliating a layer of silicon along with it.

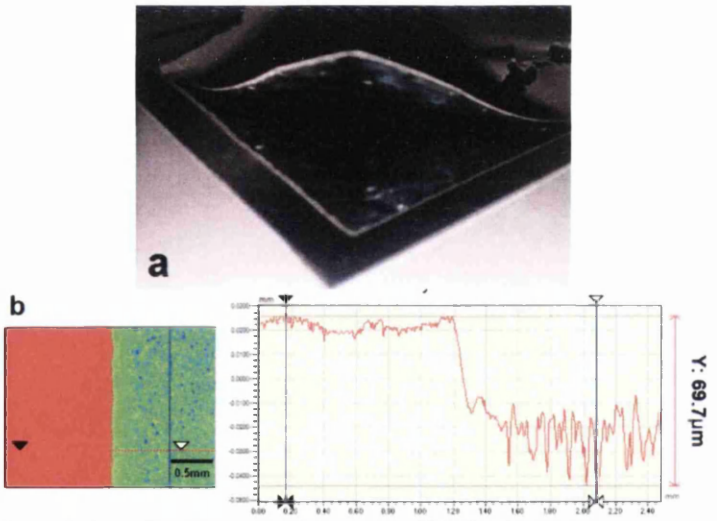


Figure 5.11: (a) Partially exfoliated stencil contact, (b) Thickness measurement of contact.

Fig. 5.11(a) shows the sample after removal from the furnace and (b) White Light Interferometer data used to determine the fired contact thickness (70µm). The sample showed good exfoliation, with 40% of the sample yielding a silicon foil. From experimentation it was concluded that stencil coated silver metallic contacts could be

successfully used in the exfoliation process. Such a technique would reduce labour and processing times compared to screen printing.

5.3.4 Exfoliation uniformity in relation to printing method

During printing investigations (outlined previously), it was observed that after the silicon foil had been peeled away from the parent substrate, differences in surface uniformity of the foil were apparent, depending on which printing method was used. Interferometry was used to analyse surface roughness of a foil obtained from a two layer screen printed and single layer stencil coated sample (fig.5.12a and 5.12b respectively).

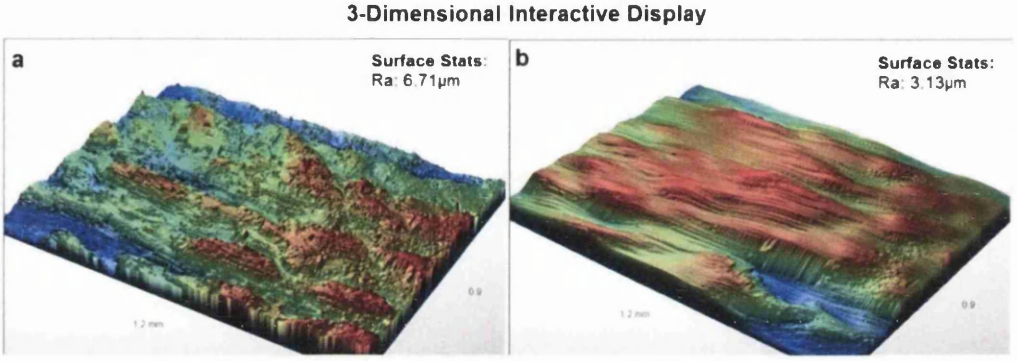


Figure 5.12 3D topography of (a) Screen printed foil, (b) Stencil coated foil

From the three dimensional topography image of fig.5.12, it is visually apparent that the surface of the foil obtained from screen printing is rougher than that obtained by stencil coating. The surface roughness (Ra) measurements also reinforce the visual observation. The screen printed foil had a substantially higher surface roughness of 6.7µm, compared to only 3.1µm for the foil obtained from stencil coating.

The differences in surface roughness were attributed to the printing procedure. Screen printing essentially applies the metallic paste through small holes in a mesh onto the substrate. Stencil coating however, draws the ink over a mask with an open window. Ink is allowed to contact the substrate through the window, with the excess being drawn away. A screen printed and stencil coated silver contact were analysed to observe the difference in surface topography in relation to the printing processes (fig.5.13).

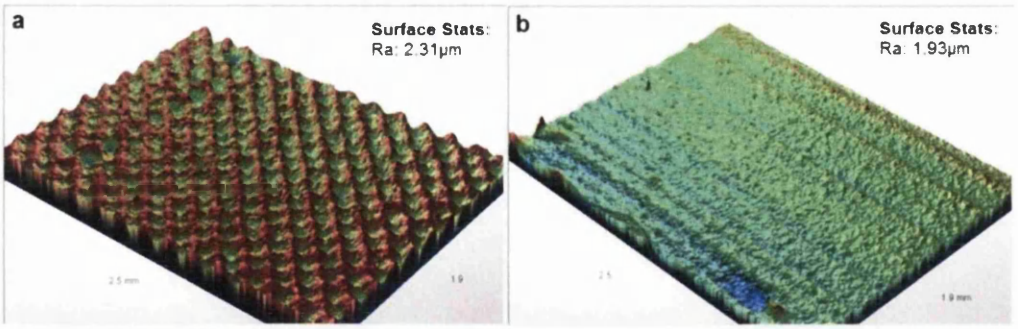


Figure 5.13 3D topography of (a) Screen printed contact, (b) Stencil coated contact

From the 3D topography of the screen printed silver contact in fig.5.13a, it is evident that the printing process yields a dimpled non uniform surface on the contact. The stencil coated silver contact of fig.5.13b yields a more even, smoother surface. The screen printed contact had a measured Ra of 2.31µm compared to 1.93µm for the stencil coated equivalent.

The dimpled effect of the screen printed surface can be attributed to the screen through which the paste was applied. Essentially, drops of paste pass through the screen onto the sample to build up the contact. The stencil coated surface topography displays more lateral deviations in the surface, caused by drawing of the ink across the stencil. From the analysis of the contact surfaces, the printing process by which an exfoliated sample is produced directly relates to the surface topology of the final silicon foil. During the firing process the surface structure of the metallic layer is transferred into the silicon. If the metallic contact has enough mechanical strength during thermal expansion and contraction, a foil resembling the surface of the contact is obtained.

5.3.5 Substrate Type

The exfoliation process relies upon the metallic layer fusing to the silicon, creating a sufficient tensile force to cleave/peel away a layer of silicon from the substrate. The metal to silicon interface and hence the silicon surface, play critical roles in achieving the necessary splitting force. Textured silicon substrates had previously been used for all experiments, due to their inherent increased surface area and adhesion. Fig.5.14 shows the difference of a textured silicon surface compared to a polished flat wafer.

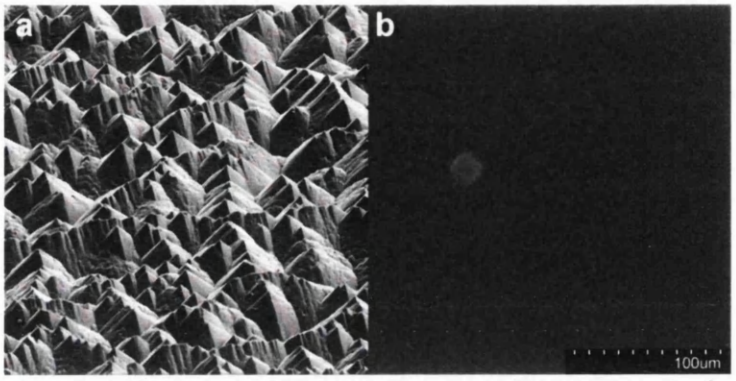


Figure 5.14: (a) Textured Silicon Surface, (b) Polished Silicon Surface

From the comparison of the two surfaces, it is suggested that the micro-pyramid topography (fig.5.14a) would give greater adhesion for a metallic contact than a flat mirror-finish surface (fig.5.14b). To reinforce the hypothesis that textured silicon was more suitable for the exfoliation process; silver metallic layers were coated on both textured and polished substrates, in order to observe the affect on exfoliation.

Silicon samples, each with textured or polished surfaces were processed. A stencil coated layer of silver paste was applied to each sample. After drying and firing using the aforementioned conditions, comparisons were made (fig.5.15).

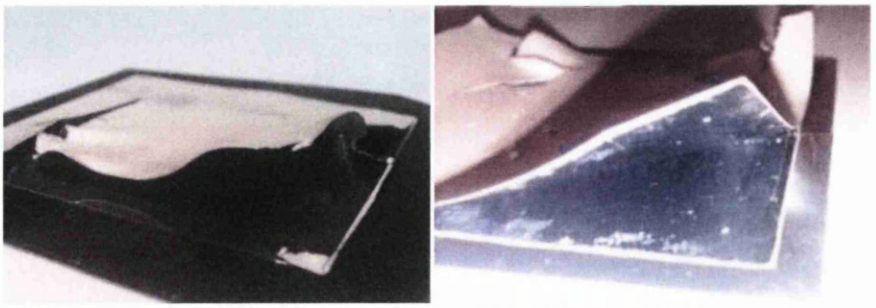


Figure 5.15: (a) Polished wafer after firing process, (b) Textured wafer after firing process

From fig.5.15a it is observed that the polished silicon substrate coated with metallic ink has not undergone any significant exfoliation. The metallic layer mainly peeled away from the

substrate without affecting the silicon surface. Unlike polished silicon, the textured sample underwent significant exfoliation. The contact peeled away from the substrate taking with it a thin layer of silicon. The extent of exfoliation of the polished wafer was significantly less than for the textured silicon.

The result of the trial reinforced the hypothesis that the micro pyramid texturing of the silicon surface, allows for greater silicon contact area for the metallic ink to sinter to. The micro pyramids also facilitate greater adhesion between the metal and silicon during the contraction and cooling of the metal layer. The result is an improved exfoliation process with larger area silicon foils being produced. In contrast, the contact on the polished silicon sample did not have sufficient contact area hence adhesion to produce any significant exfoliation.

5.3.6 Silver Ink Composition

From extensive research it was found that only the silver paste trialled produced repeatable silicon exfoliation. Aluminium and silver/aluminium mix pastes were not suitable. DuPont Solamet PV149 silver paste was found to produce consistent exfoliation when fired for 25 seconds at a temperature of 980°C. The PV149 paste was brought to market in around 2008 [11] and unfortunately DuPont no longer manufacture it. The current alternative offered by DuPont for silicon front metallization is Solamet PV17A. Textured silicon samples were stencil coated with a single layer of the new paste to observe if exfoliation occurred.

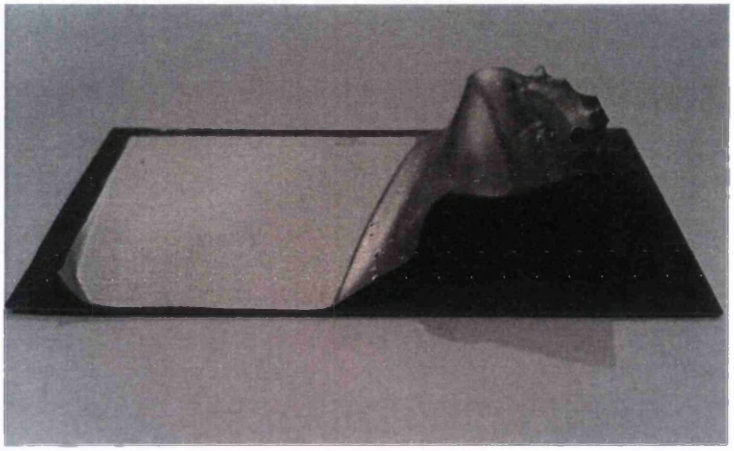


Figure 5.16: Stencil coated PV17A silver contact on textured silicon after firing

Samples coated with the new PV17A silver paste and processed using standard conditions, exhibited no exfoliation. From fig.5.16 it is seen that after the firing process the silver contact has distorted and peeled from the textured silicon substrate.

To ensure that no difference in process and firing conditions existed compared to previous experiments, another textured silicon substrate was coated with two separate metallic contacts. One contact was produced by coating the new PV17A paste, while the other was made up of PV149. Drying and firing cycles remained as previously outlined.

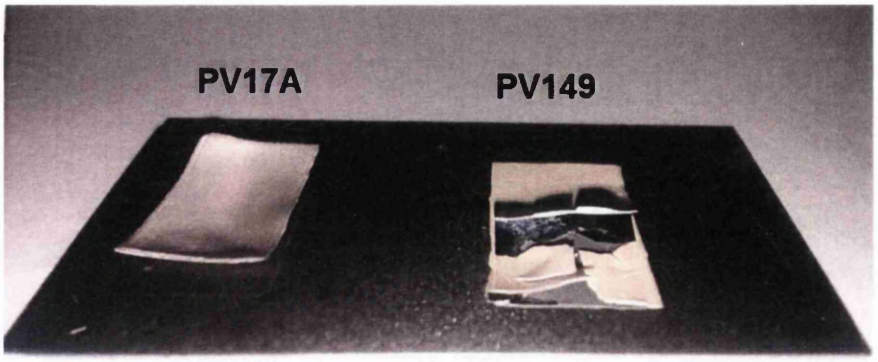


Figure 5.17: Stencil coated PV17A and PV149 silver contacts on textured silicon substrate after firing

From fig.5.17 the affect of the different metallic pastes on the exfoliation process is quite apparent. The PV17A contact once again peeled from the substrate without exfoliating any silicon. The PV149 contact underwent exfoliation producing a thin layer of silicon from the parent substrate. The colour of each contact is also different, with the PV17A silver metallic layer being lighter in colour compared to cream/yellow colour of the PV149. From the sample it is clear that the new DuPont Solamet PV17A paste is not suitable for silicon exfoliation.

In order to understand why such a difference occurred between two pastes developed for the same application, each paste composition was studied. From documentation provided by DuPont [12, 13] the main differences between the two pastes were the inclusion of lead in the PV149 paste and a lower content of silver in PV17A. The PV17A paste was lead free which has an effect on many paste parameters including the contact mechanism [13]. The reduced content of silver could also lead to less force being created during the firing cycle, as the thermal expansion co-efficient would be slightly less than that of the PV149 (which has a higher silver content). The lead borosilicate glass frit plays an important role during the firing of the ink, helping the contact to adhere to the silicon substrate [14]. Without a leaded glass frit, adhesion is reduced between the contact and silicon which was observed during the firing of the PV17A paste. It is therefore suggested that the superior performance of the DuPont Solamet PV149 silver metallic paste for exfoliation, is due to the inclusion of the lead based frit and a higher silver concentration.

5.3.7 Refinement of silicon exfoliation process

Now that the process conditions for silicon exfoliation had been identified. The next step was to analyse if the process could be applied in a typical solar cell manufacturing environment. The paste and screen printing procedure are already widely used in the industry, therefore processing of the metallic layer for the exfoliation process would not be an issue. In cell manufacturing however, multiple zone four belt furnaces are usually used to fire contacts. The different zones help to achieve solar cell contacts with excellent electrical properties. Work was carried out at a manufacturing facility using a four zone infrared belt furnace to exfoliate silicon, using the newly developed process. For the trials, textured silicon samples stencil coated with a single layer of DuPont PV149 silver paste were used.

The main adjustable parameters for the belt furnace were the zone temperatures and belt speed. Experimentation was conducted in order to find the best parameters for reliable exfoliation to occur. Fig.5.18 depicts the furnace program best suited for silicon exfoliation.

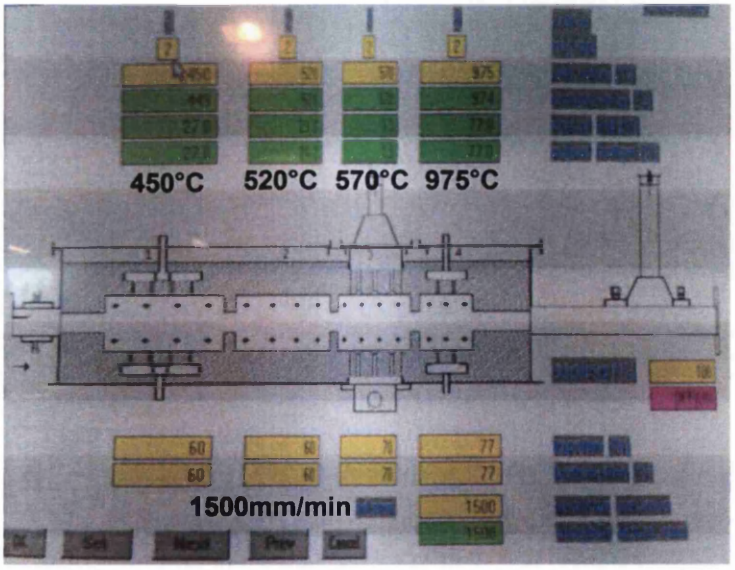


Figure 5.18: Four zone belt furnace firing parameters for silicon exfoliation

The firing profile most suited for exfoliation consisted of four temperature zones at 450, 520, 570 and 975°C respectively (fig.5.18). The coated samples entered the first zone at 450°C whilst moving through the furnace at a belt speed of 1500mm/min. After exiting the final zone (975°C) the samples passed through a cooling area (forced cooling at 25°C) before being collected from the belt. Silver stencil coated textured silicon samples fired with the profile, exhibited good exfoliation.

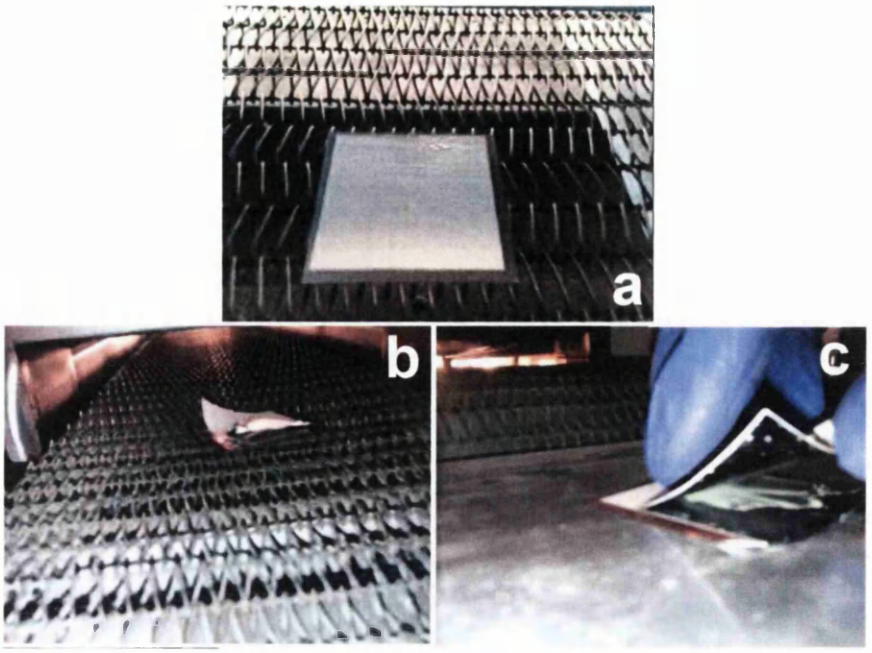


Figure 5.19: Silver coated sample (a) Entering furnace, (b) Exiting furnace, (c) After firing

Fig 5.19 shows the transition of the sample from entering to exiting the furnace. It can be clearly observed from fig.5.19c that the process successfully exfoliated silicon. From the trial, a four zone infrared belt furnace was found to successfully produce the firing profile required for silicon exfoliation to occur. Zone temperatures ranging from 450-975°C, with a belt speed of 1500mm/min yielded the optimum firing conditions.

5.3.8 Cell Processing

Previously detailed trials led to a very good understanding of the process and parameters required to produce thin silicon foils. The ultimate aim of the research was the use of such foils for silicon solar cell applications.

Once the thin silicon had been successfully detached from the parent substrate it was left with a relatively thick silver metallic layer at the top of the cell where sunlight would normally be incident. Since the contact is solid, no photons are able to pass through such a thick metallic contact and therefore it must be removed completely or partially.

5.3.8.1 Etching Trials

Experiments were conducted into removing the silver contact without damaging the fragile layer of silicon (as thin as 40μm). Such a thin layer is mechanically fragile and delicate handling is required. A wet chemical etching process was chosen to etch away the thick contact. From the literature, a suitable silver wet etchant was found to be an ammonia/hydrogen peroxide solution (two to three mols of hydrogen peroxide per four mols of ammonia are particularly preferred) [15].

To analyse the etchant suitability for contact removal, small ($10mm^2$) detached silicon foils (40μm silicon attached to 45μm silver) were used. The samples were etched until only the silicon foil remained. A solution of Ammonia (29.5%)/Hydrogen Peroxide (30%) was prepared and the sample introduced into the etchant, cradled in a stainless steel basket to help with foil retrieval after etching. Upon immersion in the etchant, the silver contact on the sample reacted vigorously with the etchant causing the sample to move around the basket (fig.5.20). After several minutes it was apparent that as the metal contact became thinner, the violent motion of the sample in the beaker caused the thin fragile silicon foil to break apart. After 4 hours the silver contact appeared to be totally removed with the textured silicon surface once more visible.

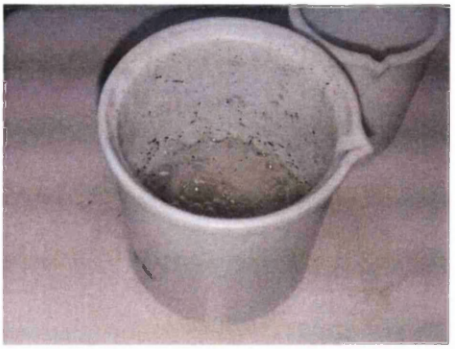


Figure 5.20: Silver Metallic contact removal in Ammonia/Hydrogen Peroxide/Water etchant

Due to the damage that occurred to the fragile foil, a weaker solution of the etchant was prepared (by adding water) and the experiment repeated. When the sample was introduced, far less activity was observed with the sample remaining stationary at the bottom of the basket. After 6 hours (two hours more than the previous etch), the textured silicon surface became visible, indicating that the top silver contact had been successfully removed. The basket was retrieved from the solution and dipped consecutively into a beaker of de-ionised water in order to remove any leftover etchant. To aid with the removal of the thin fragile silicon foil from the basket, the sample was air dried. Once dried, various delicate attempts were made to remove the silicon from the basket. Unfortunately due to the nature of the thin silicon, it broke apart extremely easily with the slightest touch of a tweezer. A small piece of the silicon foil that was retrieved is shown in fig.5.21. From the foil it is apparent that the textured surface of the silicon is once more visible, indicating the successful removal of silver. Since the foil would need to undergo further processing, including printing of front and rear contacts, it was clear that an alternative method was required in order to handle the wafer without it breaking. A technique to remove the metallic contact whilst supporting the substrate would be preferable.

Figure 5.21: Textured silicon foil after metallic contact removal

5.3.8.2 Patterning of Gridlines

In a silicon solar cell, the front contact typically consists of screen printed silver gridlines. Since the exfoliated silicon already had a front silver contact, albeit a block contact, it would be advantageous to open up windows in the contact rather than completely removing it. Such a method would result in the silicon having silver gridlines which due to their thickness (45um) would provide additional support during further processing (printing of rear contacts etc). A silicon exfoliated foil with metallic contact attached, underwent a lithography process in order to provide gridline structures from a material resistant to the

etching process. The silver surface not covered by the photoresist material would be subjected to the etchant and consequently etched.

A positive lithography photoresist (AZ ECI 3027) was spin coated onto the silicon substrate using a recipe relevant for a sufficient resist thickness of 3μm [16]. The recipe consisted of applying the photoresist solution onto the substrate, followed immediately by spinning at 3000rpm for 60s (with an acceleration value of 500). Following the coating procedure a 'soft-bake' was undertaken heating the coated substrate to 90°C for 60 seconds. After the baking cycle, the sample was loaded into mask alignment equipment with a mask consisting of several gridlines. The mask aligner was used to UV expose the unmasked resist. After exposure the sample was 'post-baked' (110°s for 60s) before submerging in the resist developing chemical 'AZ 726 MIF'. The sample was left in the solution until only gridlines of photoresist remained. Due to the slight curvature of the small exfoliated samples, there was an inconsistency of gridline width across the sample. Despite this, well formed gridlines of resist were apparent on the surface.

The next step was to etch away the unprotected silver. The less reactive mixture of Ammonia/Hydrogen Peroxide was used as in the last etching trial. Previous experimentation found that after 6 hours the silver had been removed using the etchant. Unfortunately after 6 hours with the photoresist gridline samples, the resist layer was removed before complete silver etching occurred.

Due to the thickness of the silver contact (45um) it was not possible to vertically etch in between the resist gridlines without compromising the resist pattern. Coupled with the problem of non-uniform exfoliated samples to begin with, lithography patterning of the gridlines was not feasible.

5.3.8.3 Support structure

From the mixed success of previous experiments, it was established that removing the entire silver contact was possible, but transporting and further processing the foil without breakage was not. Partially etching away the contact to leave a gridline structure had proven to be very difficult, due to the curvature of the foils and issues around etching. It was imperative that an additional material was found to support the thin silicon foil during the removal of the silver contact, and for further processing. As silicon photovoltaic cells have both front and rear contacts, attention was drawn to the possibility of applying the rear contact before removal of the front block contact. Typical back contacts in silicon solar cells consisted of large aluminium block contacts with aluminium/silver busbars (primarily

for soldering external connections). If an aluminium rear contact could be implemented prior to etching, it would undoubtedly give greater support to the fragile exfoliated silicon foil.

The addition of an aluminium contact as a support structure would be very useful, but a method of totally removing the silver contact layer without corrupting the integrity of the aluminium contact was crucial. Brief experimentation found that the conventional use of the silver etchant (Ammonia/Hydrogen Peroxide) used previously, also etched aluminium at a similar rate. Further investigation indicated that commercially available chromium etchant (ceric ammonium nitrate/perchloric acid) could possibly provide the necessary etching selectivity [17].

After the process of silicon exfoliation to achieve a silicon foil bonded to a silver contact, standard back contact aluminium ink DuPont PV381, was applied to the rear of sample (silicon face). The paste was applied by brush, taking care not to paint over the edges of the silicon which could result in an electrical short circuit. After application the paste was dried and fired in a four zone belt furnace using the conventional recipe previously used (zone temperatures ranging from 450-975°C, with a belt speed of 1500mm/min). Before removal of the silver contact, SEM imaging was implemented to observe the cross section of the sample (fig.5.22).

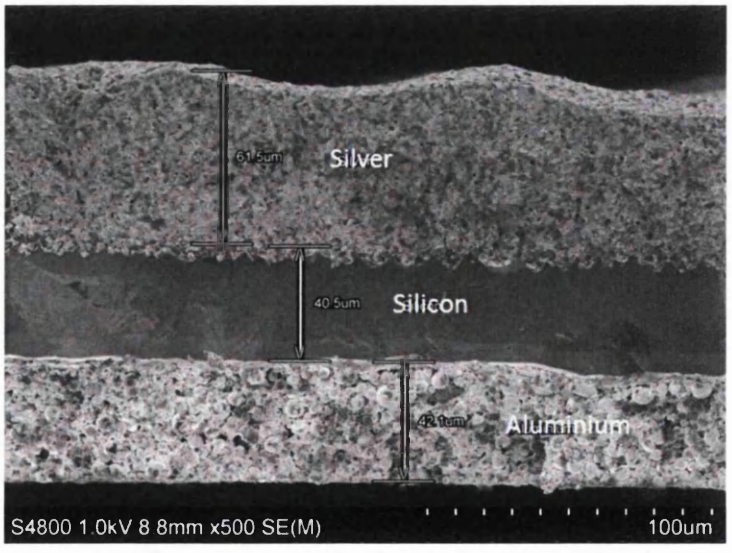


Figure 5.22: SEM imaging of cross section of exfoliated sample with aluminium rear contact

From fig.5.22 the silicon is sandwiched between a 61.5um silver and 42.1um aluminium contact respectively. The exfoliated silicon itself is around 40um thick. Following the

addition of the aluminium back contact, the sample underwent a wet etching process in order to remove the silver front contact. For the etching, standard chromium etchant was used due to its selectivity to etch silver faster than aluminium. The sample was introduced to the etchant and remained for 30 minutes when it was visually observed that the front contact had been removed. It was noted that long before the silver contact was completely etched away, it would detach from the silicon. Fig.5.23 shows an SEM image of the silver contact detachment from the textured silicon foil mid way through the process.

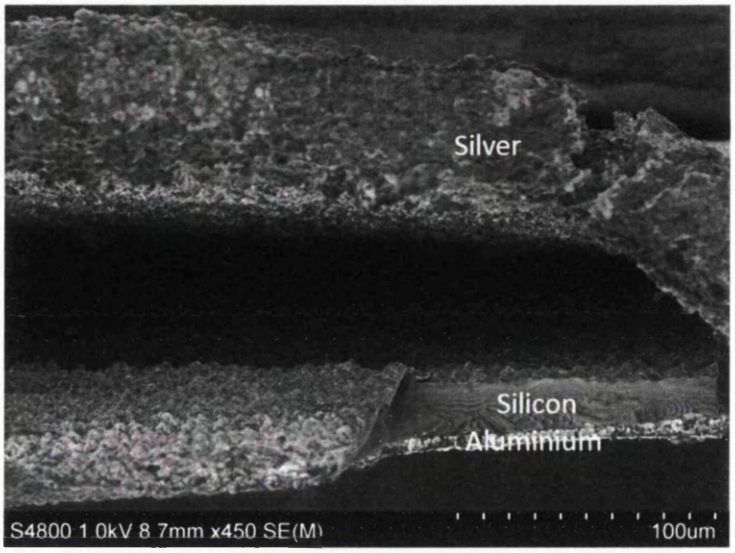


Figure 5.23: Silver contact detachment from silicon foil substrate

From fig.5.23 it is observed that the silver front contact detaches from the silicon foil in the presence of the chromium etchant solution. It is suggested that one reason for this is that a different material composition is formed at the interface of silver and silicon. The chromium etchant is able to remove such material far quicker than silver alone. The removal of the interface layer by which the silver and silicon is bonded together, results in the two materials detaching from one another.

Once the reaction had resulted in full detachment of the silver from the foil, imaging of the surface of the silicon foil was performed. Assessment of the surface of the silicon was important to observe if the micro-pyramid texturing remained.

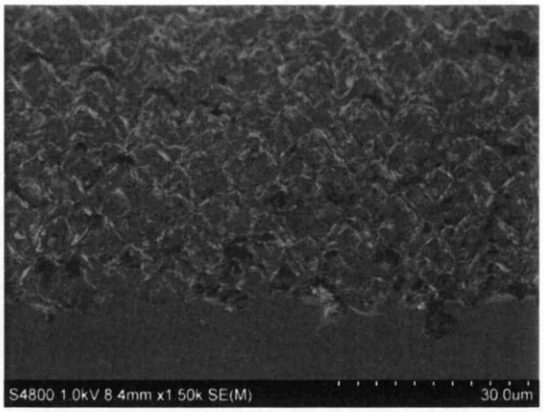


Figure 5.24: SEM image of silicon surface after silver contact removal

The textured surface of the silicon foil was still observed after the etching process (fig. 5.24). When comparing the topography of the foil to one of a surface before starting the experiment (fig.5.14a), differences are quite apparent. The micro-pyramids have lost definition, with a more rounded uneven profile. The variation in topography is associated with the bonding of the metallic contact and its subsequent etching. As previously described, a glassy layer is formed in between the silver and silicon substrates essentially creating a very thin layer of alloyed materials at the interface. Removal of the silver contact reveals the silicon pyramids.

The removal of the silver contact also had the added benefit of dramatically reducing the curvature of the sample. Fig.5.25 shows the silicon foil and the subsequent metallic layer (now detached). The foil can be seen to be relatively flat compared to the removed silver layer which remains curled. The returning of the silicon foil to a flatter profile shows that the silver metallic layer caused the initial curvature, due to the thermal expansion and contraction it underwent during firing and subsequent cooling. Removal of the metallic layer also removed the mechanical stress from the Si foil.

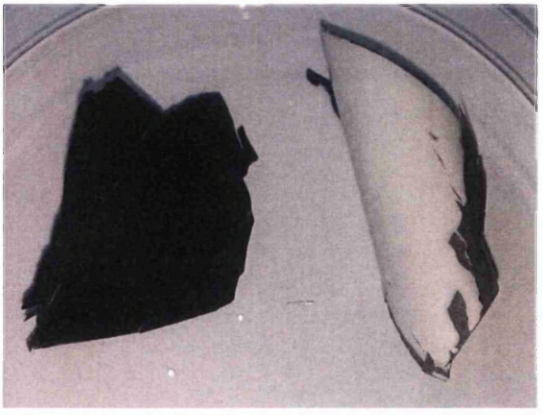


Figure 5.25: Silicon foil and metallic contact after separation

Despite the removal of the thick silver layer, the silicon foil remained supported by the aluminium contact previously applied to the rear. SEM imaging concluded that the aluminium back contact had remained intact during the etching of the silver front contact.

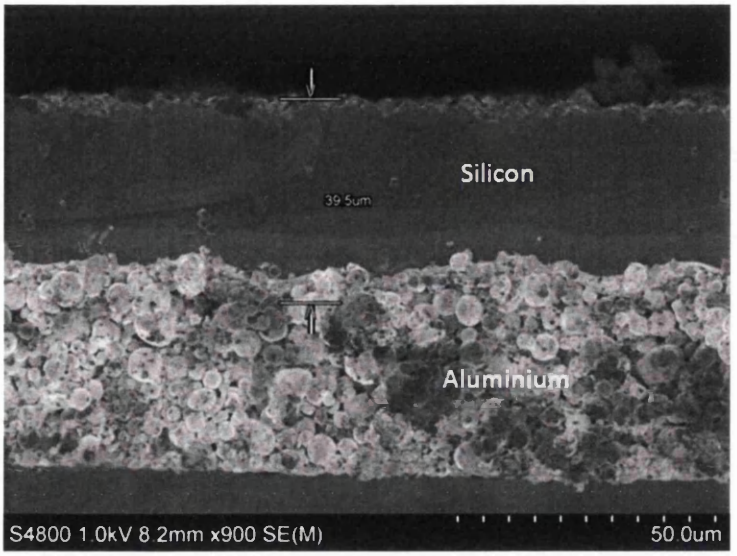


Figure 5.26: SEM image of silicon foil after silver front contact removal

From fig.5.26 the silicon foil now has no front contact which would otherwise restrict light from entering the semiconductor material. The aluminium back contact has however been maintained, providing a rear electrical contact as well as a vital mechanical support for the thin foil.

Now that the silver contact had been removed, a new gridline front electrical contact could be fabricated. Typically, gridlines are applied to the top of a silicon solar cell via screen printing. Despite the aluminium providing support for the substrate, the method of screen printing a thick ink requires a flat surface with reasonable strength. Since the sample even with the aluminium contact was still only around 80um, screen printing was not suitable due to non-uniformity and fragility issues. Instead a 1µm silver layer was deposited onto the sample by physical vapour deposition. To avoid total sample coverage, a shadow mask was produced so that only thin gridlines would be deposited on the surface of the cell.

To ensure that the fully processed solar cell would not be damaged during electrical measurements, two extended front and rear contacts were attached. The contacts were electrically connected to the cell using a silver conductive ink (Electrolube SCP). After application, the sample was placed on a hotplate at 150°C for 120 seconds to

enhance adhesion of the ink. To further protect the cell, the sample was bonded to a glass slide for greater mechanical support (fig.5.27).

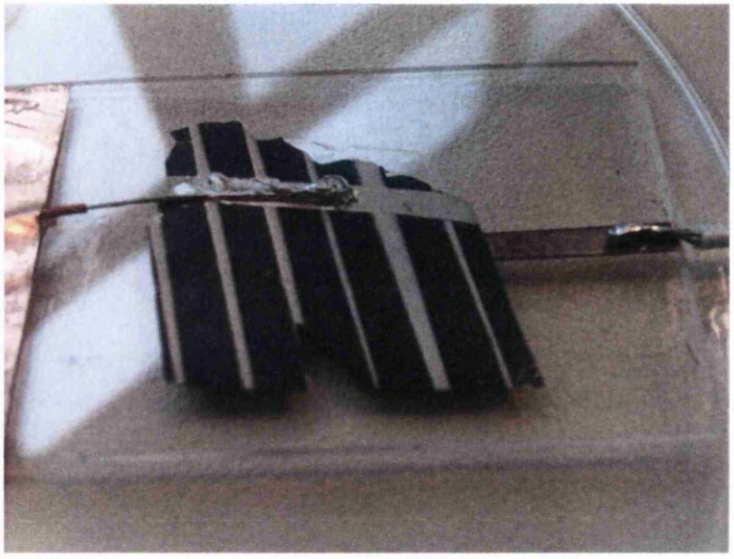


Figure 5.27: Fully processed 40μm thin silicon solar cell with textured surface (2.5cm^2)

5.3.8.4 Efficiency measurements

Efficiency measurements of the cell were finally conducted in order to observe the electrical characteristics of the ultra-thin silicon solar cell. From table 5.2 the efficiency of the measured cell was found to be 1.08%. Although this efficiency is quite low, it is important to note that the cell produced was far from optimal. It is therefore suggested that significant efficiency gains could be made by enhancing the electrical contacts and anti-reflective properties of the cell. A solar cell produced using a similar exfoliation technique exhibited an efficiency of 10% although process conditions are unclear [6].

For the work, the front contact was sputtered with silver, producing a contact thickness of only 1μm. Electroplating on top of the existing sputtered contact would create a thicker and better electrically performing contact. Although the front surface of the exfoliated foil was already textured using conventional KOH etching, no ARC was deposited onto the cell. By depositing a coating and opening windows prior to metal deposition, the anti reflective properties of the cell would increase. The ARC coating would also allow for surface passivation of the cell. Process induced shunts in the cell from micro cracks formed during silicon exfoliated could also have a negative effect upon the efficiency of the cell, although due to the nature of the exfoliation process, preventing such shunting would be

very difficult. Despite possible shunting, improving the electrical contact and anti reflective properties of the cell, are expected to improve the cell efficiency significantly.

Voc V	Isc A	Jsc mA/cm2	Imax A	Vmax V
0.26003141	0.03240213	16.20106602	0.01629624	0.13195466

Fill Factor	Efficiency	R at Voc	R at Isc	Power W
25.5219	1.0752	7.572116	8.334	0.00427262

Table 5.2: Efficiency measurement for 40μm thick exfoliated silicon solar cell

5.4 Summary

In this chapter the process of silicon exfoliation was investigated in order to produce ultra-thin silicon substrates for photovoltaic applications. Such substrates have great potential for reducing material consumption and therefore cost. Experimentation was carried out on various parameters relating to firing temperature, contact thickness, printing methods, substrate type, and ink compositions. Scanning Electron Microscopy and White Light Interferometry were used to analyse samples.

A critical parameter for reliable exfoliation was found to be the firing temperature of the contact. A period of 25 seconds at 980°C was found to be suitable for exfoliation. Despite testing a range of metallic pastes suitable for silicon solar cell production, only one paste (DuPont Solamet Silver PV149) was found to work successfully. A sufficiently thick metallic layer was required to provide enough mechanical force for exfoliation to occur. This related to a minimum contact height (after firing) of 46µm. Such a contact required two screen printed layers or one stencil coated layer of the silver paste. Using a thicker contact than 46µm was found to produce a more effective exfoliation. Textured silicon substrates normally used for silicon solar cell fabrication were found to be useful for exfoliation. The micro pyramid texturing on the surface of the substrates, allowed for excellent adhesion of the metallic contact during expansion and contraction from the firing cycle.

The extensive trials allowed for repeatable exfoliation to occur, producing ultra thin silicon foils. A novel processing structure was formulated to convert the silicon foils into fully operational solar cells. Initial cells measured around 1% efficient, but it is envisaged that great efficiency gains could be achieved with better electrical contacts and optimisation of the techniques. The silicon exfoliation process developed was successfully tested in a commercial silicon solar cell manufacturing facility.

[1] Saga, Tatsuo, Advances in crystalline silicon solar cell technology for industrial mass production, NPG Asia Materials, vol.2, no.96, pp. 96–102, 2010
[2] Hernández, David *et al*, "Silicon millefeuille": From a silicon wafer to multiple thin crystalline films in a single step, Applied Physics Letters, 102, 172102, 2013
[3] Beesley, J. G., and Schönholzer, U. Slicing 80 micrometer wafers — process parameters in the lower dimensions. In Proceedings of the 22nd European Photovoltaic Solar Energy Conference and Exhibition, 2007
[4] Kerr, M.J.; Campbell, P.; Cuevas, A., "Lifetime and efficiency limits of crystalline silicon solar cells," *Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE* , pp.438,441, 2002
[5] Henley, F.J., "Kerf-free wafering: Technology overview and challenges for thin PV manufacturing," Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE, vol., no., pp.001184,001192, 2010
[6] Dross F *et al*. SLIM-cut: a kerf-loss-free method for Wafering 50-µm-Thick Crystalline Si Wafers Based on Stress-Induced Lift-Off, 23rd European Photovoltaic Solar Conference and Exhibition (Valencia, Spain), pp 1278-81, 2008
[7] Rao, R. A. *et al*. A novel low cost 25µm thin exfoliated monocrystalline Si solar cell technology, *Photovoltaic Specialists Conference (PVSC), 37th IEEE*, vol., no., pp.001504,001507, 2011
[8] Guide for DuPont Solamet Photovoltaic Metallization Materials, L-13909, 09/07
[9] Luque, A.; Hegedus, S., Handbook of Photovoltaic Science and Engineering, Second Edition, John Wiley & Sons, 265-313, 2011
[10] Takuya Konno, Paste for solar cell electrodes, method for the manufacture of solar cell electrodes, and the solar cell, EP1801891A1, 2007
[11] DuPont™ Solamet®, The Science of PV Cell Efficiency, 2011
[12] DuPont™ Solamet® PV17A, Photovoltaic Metallization, Technical Data Sheet, 2012
[13] Giovanna Laudisio *et al*, A view of the design challenges involved in the development of advanced n-type contacts using lead-free chemistries. 2nd Workshop on Metallization for Crystalline Silicon Solar Cells, 2010
[14] Gunnar Schubert, Formation and nature of Ag thick film front contacts on crystalline silicon solar cells, PV in Europe, 2002
[15] Fumio Okamoto, Etching Solution for Silver, US Patent 3860423, 1975
[16] AZ ECI 3027 Product Datasheet
[17] Williams, K.R.; Gupta, K.; Wasilik, M., "Etch rates for micromachining processing-Part II", Journal of Microelectromechanical Systems, vol.12, no.6, pp.761, 778, Dec. 2003

Chapter 6: Reflectivity Suppression

6.1 Introduction

Maximising the amount of light entering a solar cell is extremely important. A silicon wafer has a polished surface acting almost like a mirror. Such a high reflectivity means that a large proportion of light is simply reflected away and thus wasted. Such light could have potentially contributed to current generation instead. Reducing the reflectivity of the wafer surface is therefore essential. An in depth review of properties affecting reflectivity and current research areas were covered in Chapter 3. In industry two methods of reflectivity suppression are typically adopted for crystalline silicon solar cells. The first is a chemical etch to roughen the surface of the silicon. The second is the application of an Anti Reflective Coating (ARC).

The texturing technique currently used for monocrystalline substrates is popular mainly due to the crystal lattice arrangement of (100) monocrystalline silicon substrates, (which yields a microscale pyramid textured structure when anisotropically etched). With the ever increasing demand for thinner silicon substrates such a texturing process may no longer be suitable. One method for producing thin silicon substrates is by using an exfoliation technique. From experimentation conducted in this work, 40μm thin silicon solar cells were produced. Despite the starting material for the thin substrates being (100) monocrystalline silicon, only the upper most exfoliated foil can use standard anisotropic etching with success. Because the exfoliation process disrupts the surface of the next foil, such etching might not create well formed pyramidal structures as would a prime wafer. The micro pyramid structures of conventional texturing can be several microns in height and the structured surface would mechanically weaken the thin silicon substrate. Alternative methods are therefore required to texture the thin silicon solar cell substrates of the future.

Other methods exist for roughening the surface of a silicon wafer. One such method has the ability to produce a rough anti-reflective surface using low cost processing techniques. The method is porous silicon formation, which essentially creates nanoscale pores in the surface of a silicon wafer. Investigations into the suitability of porous silicon as an anti-reflective surface were conducted on reclaimed polished silicon wafers. Several methods of creating such structures were assessed including metal assisted etching, nanoimprint lithography and electrochemical etching. SEM and UV-VIS-NIR spectrophotometery were used to analyse the porous silicon surfaces.

6.2 Experimental Procedure

For the investigation of porous silicon, the following procedure was implemented. For this work, reclaimed polished monocrystalline silicon substrates were used. The silicon wafers were first doped with an n-type phosphorous emitter junction as described in Chapter 4.

Two ways of producing porous silicon were investigated. The first by using a metal assisted etching (MAE) technique and the second by electrochemical etching of the surface. For metal assisted etching, metal nanoparticles required for the technique were sputtered onto the Si surface using physical vapour deposition. Due to sample size constraints with deposition and characterization equipment, emitter doped silicon wafers were cut into 30mmx30mm samples. To achieve the deposition, a DC power of 8W was used with 30sccm Ar corresponding to a deposition rate of 0.5Å/s, using a Kurt J Lesker PVD 75 with a Torus magnetron source.

Following the deposition of metal nanoparticles onto the surface of the silicon substrates, wet chemical etching was performed. The etch solution consisted of HF (50% concentration), Hydrogen Peroxide (30% concentration) and De-ionised Water with the ratio 5:2:15 respectively. The samples were etched in the solution for 60 seconds before being thoroughly rinsed with de-ionised water and blow dried with compressed nitrogen gas.

The process of creating PSi via electrochemical etching was conducted differently to that used by the MAE technique. P-type reclaimed polished silicon substrates were cut into 30mmx30mm pieces before being loaded into a specially designed etch vessel constructed of Polytetrafluoroethylene (PTFE). Two electrodes were used in an electrolyte solution of HF (50% concentration). One electrode was attached to the bottom of the silicon substrate (this electrode being insulated from the solution) whilst the other was suspended above the silicon (10mm) in the HF solution. A power supply provided the necessary potential required for the process. Initial experiments used a fixed voltage of 1.5VDC transpiring to a current of 15.4mA.

After the etching of substrates to create a porous silicon surface, SEM and WLI were used to assess the surface topography. A UV-VIS-NIR spectrophotometer was used to measure the reflectivity of the silicon samples before and after various etching procedures.

6.3 Experimental Results

6.3.1 Porous Silicon – Metal Assisted Chemical Etching

6.3.1.1 Metal Deposition

Metal assisted etching of porous silicon for reflectivity suppression was first analyzed on reclaimed polished silicon substrates. Since the process to create pores in the substrate is heavily dependent on the metallic particles deposited. Experimentation first focused around the choice of material for deposition.

From the literature silver metallic nanoparticles were found to produce a good PSi anti-reflective structure on silicon after etching [1]. Physical vapor deposition (via sputtering) of silver nanoparticles was chosen due to the simplicity and reproducibility of the deposition method. Sputtering is typically used to deposit a thin film of a material onto a substrate. Since the porous silicon would require nanoparticles to create the pore structures, experimentation was carried out to observe deposited silver particle dimensions.

Reclaimed polished silicon samples were sputtered with silver particles. A crystal monitor (essentially a quartz crystal whose frequency changes in respect to the amount of material deposited onto it) was used to give an estimation of the thickness of the layer deposited. Following the deposition, SEM imaging was used to visualize and measure the particle size. Three different deposition thicknesses were performed, estimated to be 2nm, 5nm and 10nm by the crystal monitor.

The first step was to observe the surface of the silicon after deposition. SEM enabled a high resolution image to be taken of each of the sample surface (fig.6.1). SEM also allowed for accurate measurements of the particle diameters. It is apparent that the particle diameters vary over the surface of silicon. Due to the variance, an average particle size was determined by measuring several particles and taking an average (over an area of 200nmx200nm). As the particle size differed across each of the three samples analysed, an average was found for each using the same method as above. The 2nm (fig.6.1a) and 5nm (fig.6.1b) samples revealed average particle diameters of 13nm and 16nm respectively. The 10nm sample was more of a series of interconnected particles with diameters of around 30nm in diameter. For the 2nm and 5nm depositions, instead of a film forming relating to the thickness indicated, isolated particles with diameters 13nm and 16nm were produced. The results from the deposition trials revealed that sputtering equipment was capable of producing isolated nanoparticles without any additional annealing processes.

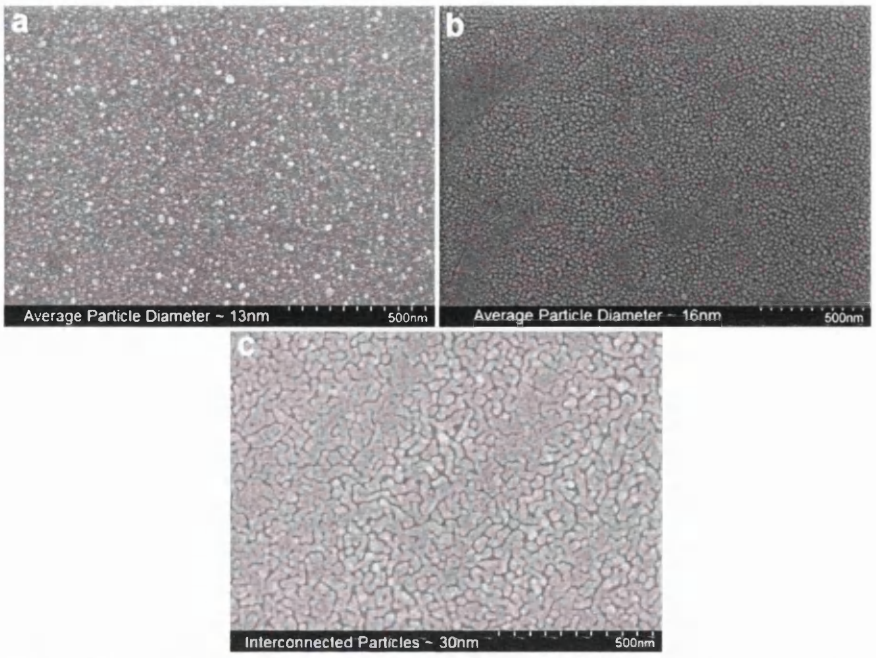


Figure 6.1: SEM Image of Si with deposition of a) 2nm Ag, b) 5nm Ag and c) 10nm Ag

6.3.1.2 Chemical Etching

Following the successful nanoparticle deposition process, the samples were chemically etched for 60s in a solution of hydrofluoric acid, hydrogen peroxide and de-ionized water. Care was taken to place and remove the samples into the solution quickly as a rapid reflectivity change was observed, as shown in fig.6.2.

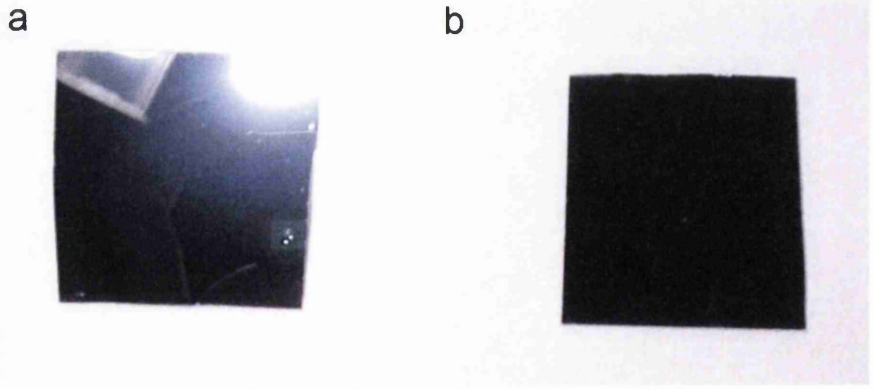


Figure 6.2: 2nm Ag deposition a) Before etching, b) After 60s etch. Before etching the camera flash is reflected by the sample

After 60s the samples were immediately introduced into a beaker of de-ionised water to stop the chemical reaction. After blow drying of the samples, the samples were reimaged using SEM.

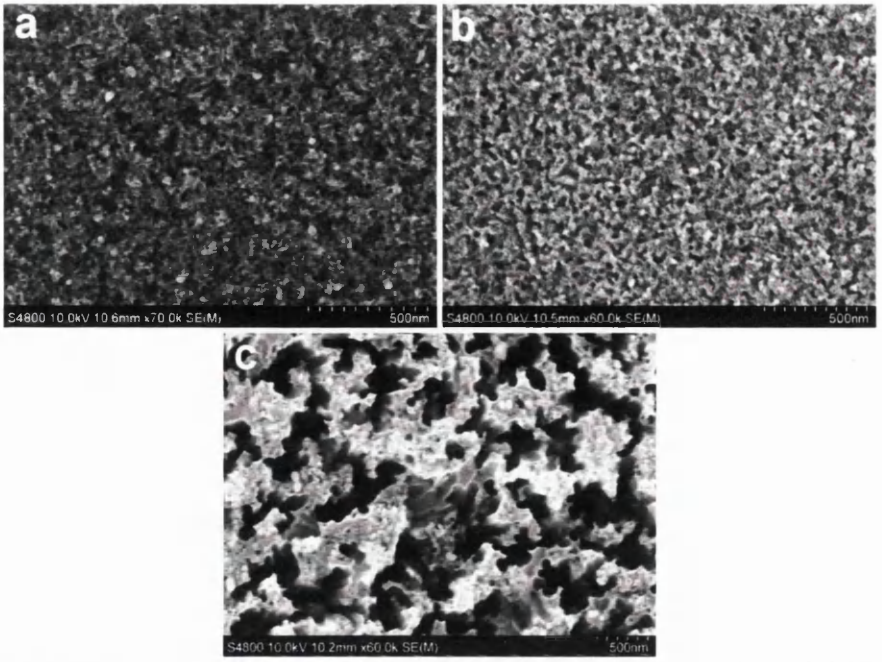


Figure 6.3: SEM Image of PSi formed deposition of a) 2nm Ag, b) 5nm Ag and c) 10nm Ag from chemical etching in HF/H_2O_2

From SEM images obtained of the newly formed PSi layer (fig.6.3) it is evident that the surface of the polished silicon has changed significantly. The silver particles that were once on the silicon surface have burrowed into the silicon and created pores. From inspection of the SEM images, the diameter of the pores relate to the diameter of the deposited metal nanoparticles. Fig.6.3a/b exhibit isolated pores, whereas the sample surface of fig.6.3c has interconnecting pores much larger in diameter than those of the other samples. The distribution of metallic nanoparticles directly relates to the distribution of pores after the etching procedure. The larger the particle size the larger the diameter of pores created.

From the literature [2], a pore depth of 200-300nm was found to be sufficient for silicon photovoltaics, due to the cut-off in reflectivity gain for pores any deeper than this. In order to assess the depth of the pores, the samples were cleaved in order to expose the cross-section of the porous silicon (fig. 6.4).

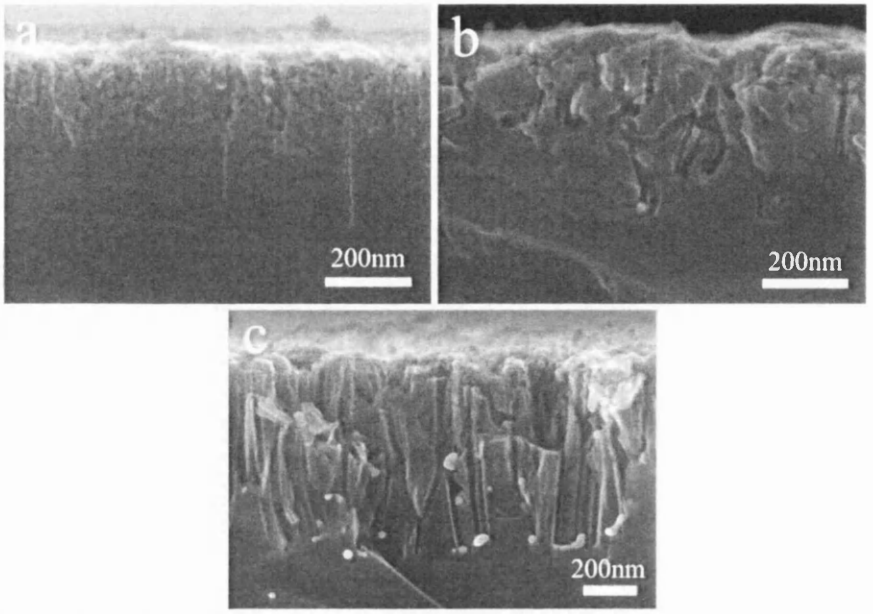


Figure 6.4: Cross-section of PSi from deposition of a) 2nm Ag, b) 5nm Ag and c) 10nm Ag

From the SEM images of fig.6.4, it was found that a 60 second etch of the 2nm and 5nm samples, resulted in pores around 300nm deep. For the 10nm sample, etched under the same conditions, pores as deep as 600nm were observed. A possible explanation for this difference is that the 10nm particles were far larger than those deposited for the 2nm and 5nm samples. The larger particles have greater mass and will etch deeper into the silicon under the same etching conditions due to the effect of gravity.

6.3.1.3 Anti-reflective Properties

Following analysis of the PSi layers, despite a visual change in reflectivity of the silicon surface, accurate reflectivity measurements were needed in order to compare the anti-reflective properties of the PSi against commercial anti reflective processes. The three different samples reflectivities were measured along with that of a bare polished substrate as a reference. As silicon solar cells require photons with energy equal to or higher than the band gap for silicon (1.12eV), reflectivity over a specific spectral range was desirable. To find the spectral range required, the threshold wavelength was required.

Since wavelength λ can be determined using:

$$\lambda = \frac{hc}{E} \tag{6.1}$$

As a silicon cell is being used as well as a PSi layer, taking the lowest band gap of the two materials will give the longest wavelength that can be absorbed; therefore Eg of silicon (1.1eV) will give:

$\lambda = 1.13 \times 10^{-6}\text{m} \approx 1100\text{ nm}$

Therefore, for silicon solar cells (with a PSi layer) only wavelengths below 1100nm can contribute to current generation. Reflectivity of the PSi samples was measured between 300-1100nm using a spectrophotometer.

From the reflectivity data obtained in fig.6.5, polished silicon without any treatment had an average reflectivity of 45.86% over the wavelengths of 300-1100nm. The porous silicon samples showed significant reduction in reflectivity. In fact the 2nm and 5nm samples showed an average reflectivity of 7.30% and 7.15% respectively. The lowest reflectivity of porous silicon was from using a 10nm deposition of silver, which had an average of 6.68%.

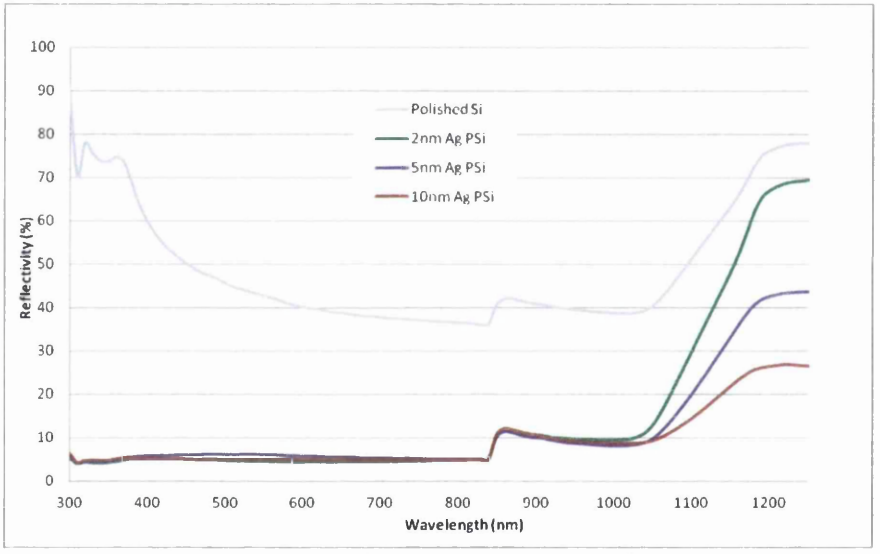


Figure 6.5: Reflectivity suppression of PSi

Creating a PSi surface drastically decreased the reflectivity of the polished silicon starting substrate. For the technique to be fairly evaluated, the samples were next compared to commercially used reflectivity suppression methods, namely textured silicon and textured silicon with an additional silicon nitride ARC.

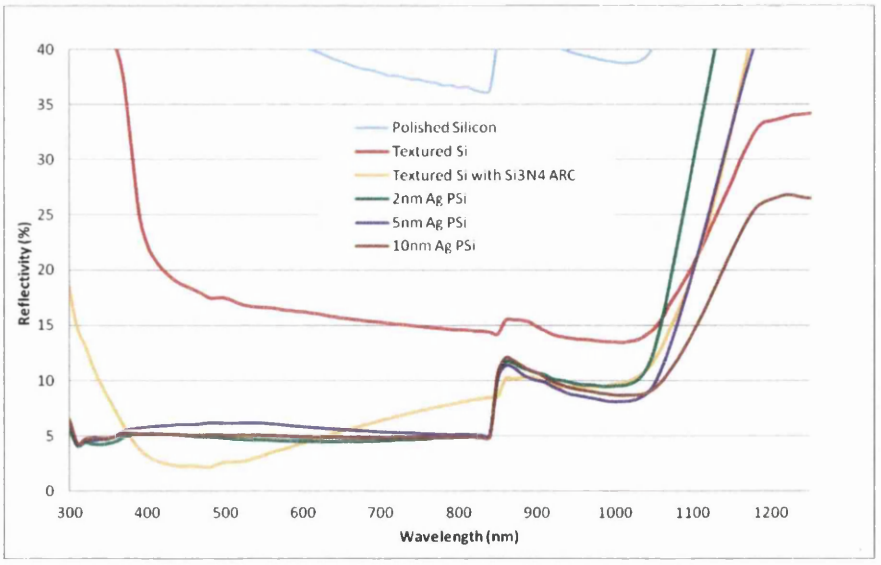


Figure 6.6: Reflectivity of PSi compared to commercial process

From the reflectivity comparison in fig.6.6, it can be seen that a polished silicon surface that undergoes a standard KOH texturing process has its average reflectivity reduced from 45.86% to just 20.24% (red plot). Commercial silicon cells not only adopt micro-texturing of silicon but also an additional ARC coating, typically silicon nitride. From the reflectivity data, an average reflectivity of 7.56% can be achieved by the addition of such an ARC. The porous silicon samples were found to far outperform standard textured silicon alone and have similar ability to that of textured silicon with an additional silicon nitride coating. The 10nm deposition of silver had an average reflectivity of just 6.68%, which is actually lower than the commercial anti-reflective suppression technique of textured silicon plus an ARC. This low average reflectivity is very exciting as it had the greatest reflectivity suppression of all the samples tested. The porous silicon layer in question can be produced in a single process unlike the commercially adopted method of having a textured surface plus a separately applied ARC. It must be noted however that the approach undertaken in this work uses sputter equipment which is quite complex and expensive. The next area of investigation was how to produce porous silicon features using a more economic means. Two very different approaches were taken, the first by Nanoimprint lithography and the second by electrochemical etching of the silicon surface.

6.3.2 Porous Silicon – Substrate Conformal Imprint Lithography

To overcome the issues of having to sputter metal nanoparticles as part of the porous silicon process, a relatively new technique was investigated. Substrate Conformal Imprint Lithography (SCIL) is a form of Nanoimprint Lithography (NIL) with the ability of reproducing nanoscale features onto a photo curable resist through a simple imprinting action. The nanoscale features are first prepared on a silicon master wafer as shown in fig.6.7(1), before a 'soft stamp' is created as in fig.6.7(2-6). The soft stamp is made from a more suitable flexible material which can be used to imprint the features in a resist. A wafer is coated with a photo curable resist and then the replicated stamp is used to imprint the features from stamp to resist. Ultraviolet light is then used to cure the resist so that the features are set permanently. The stamp is retracted leaving the cured, patterned resist on the Si surface. The resist acts as a barrier layer during etching so that the features set into the resist are physically etched into the substrate whilst the resist protects other areas from being etched. The overall result is that the finished wafer mimics the features created on the master wafer, without using any complex equipment.

The first part of the process was to create the master wafer and make a replicated stamp.

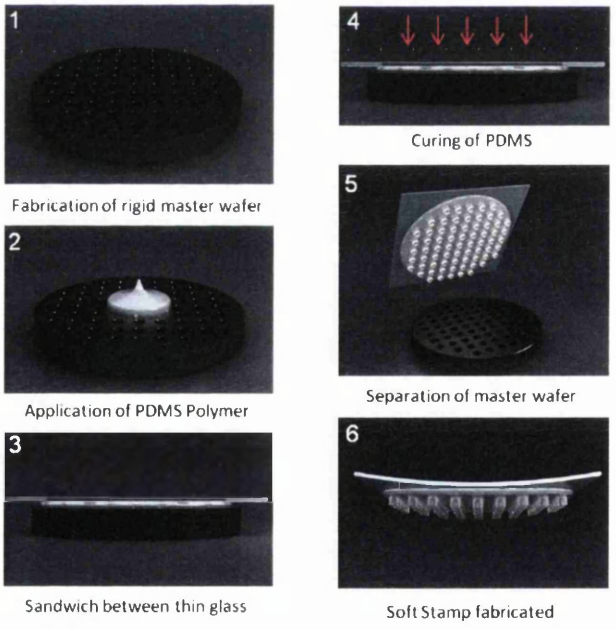


Figure 6.7: SCIL Stamp Replication Process Schematic.
(1) Si master wafer with fabricated PSi layer
(2) Coating of flexible soft stamp polymer material (PDMS) on master wafer
(3) Flexible glass substrate applied on top of stamp polymer material
(4) Heat curing of stamp polymer material (at 50°C)
(5) Separation of glass/polymer stamp from Si master wafer
(6) Completed soft polymer stamp

The first step in investigating the suitability for SCIL reproduction of PSi was to create the master wafer. As this wafer would be a one off, from which many more could be created, it was fabricated using the metal assisted etching process previously described. As PSi produced from a 10nm Ag deposition had the lowest reflectivity, this process was chosen to produce a 4" (10cm) silicon master wafer. Fig.6.8 shows a picture of the wafer before (left image) and after PSi formation (right image). The only change made to the process was the etching time was reduced from 60s to 30s to create shallower (300nm) pores.

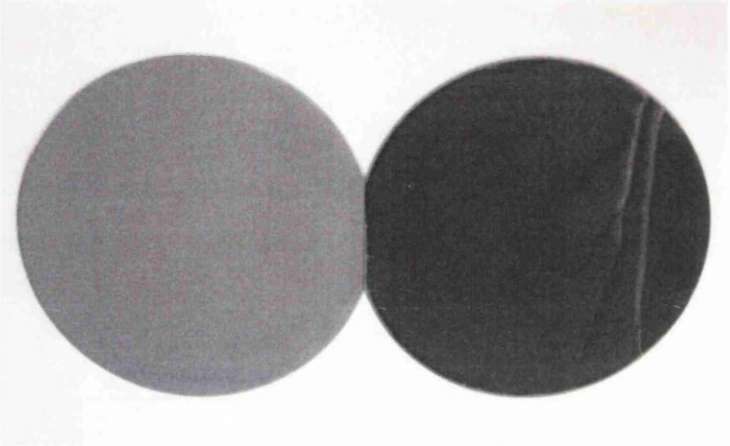


Figure 6.8: Image of Silicon wafer before and after PSi formation

Several smaller silicon pieces of a similar wafer were also processed in conjunction with the master, so that information (topography and hydrophobic nature) could be obtained without damage of the master. One such piece was imaged using SEM to check the pore sizes of the PSi surface (fig.6.9).

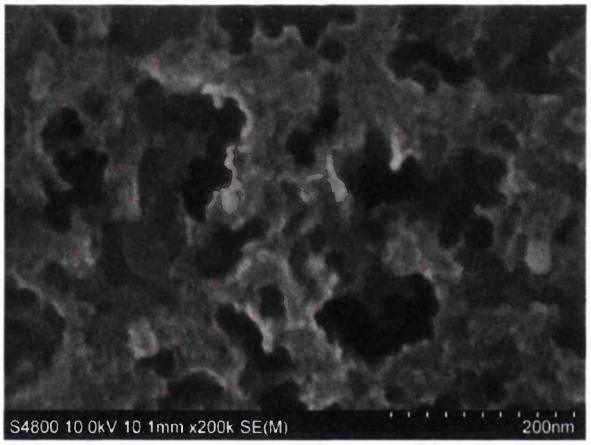


Figure 6.9: SEM conformation of PSi formation

After verifying the formation of PSi, the next step in the process was to replicate a stamp from the master wafer. The replication process consisted of applying a layer of Polydimethylsiloxane (PDMS) to the PSi surface, followed by a thin (200μm) glass sheet.

After curing, the PDMS/glass layer would be detached from the master thereby generating the replicated soft stamp. Before replication was attempted, an anti-sticking layer was deposited onto the PSi master surface. The layer was required to aid in the separation of the master from the stamp after curing. A suitable anti-sticking layer was found to be FDTS (1H,1H,2H,2H perfluorodecyltrichlorosilane) [3]. The FDTS solution was evaporated onto the wafer at 50°C for 8 hours in a vacuum oven. A quick test to verify the efficiency of the anti-sticking layer was then performed. Fig.6.10 shows the result of the test after water droplets were pipetted onto an untreated (left of image) and treated (right of image) wafer.

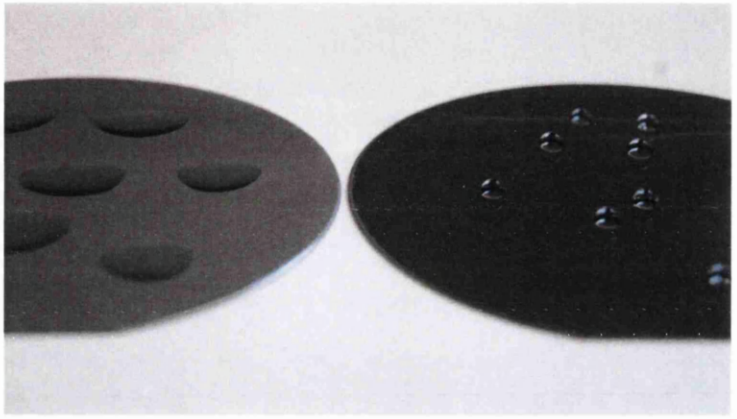


Figure 6.10: Silicon wafer before and after FDTS treatment

When water was dropped onto a wafer without FDTS treatment wetting of the surface occurs, hence it is hydrophilic in nature. Once an anti-sticking layer of FDTS is evaporated the surface becomes hydrophobic and wetting does not occur, indicated by the more spherical shape of the water droplets. For a more accurate analysis of the layer, contact angle measurements were taken. From fig.6.11 it is apparent that the measurement returned a contact angle of 130.7° indicating the PSi surface was indeed highly hydrophobic.

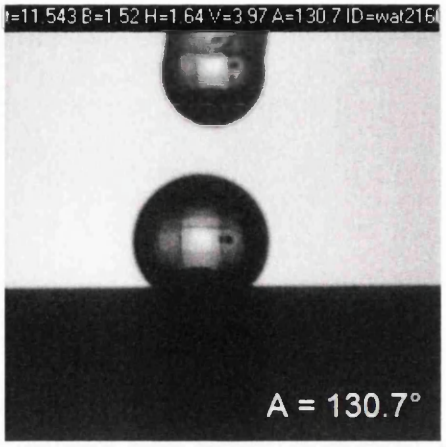


Figure 6.11: Contact Angle of PSi wafer surface after FDTS layer

Following the successful evaporation of an anti-sticking layer, the surface was reimaged in order to verify that the FDTS layer was sufficiently thin enough to avoid blocking of the silicon pores. Once more a smaller sample was imaged that had undergone exactly the same processing conditions as the master wafer.

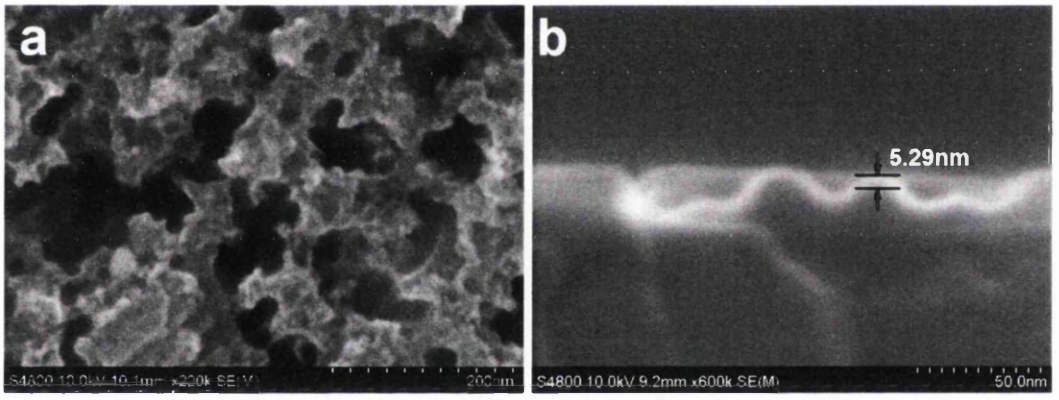


Figure 6.12: SEM of FDTS layer a) Surface, b) Cross section

From fig.6.12a it is observed that despite the evaporation of the anti-sticking layer, the pores of the PSi remain largely unaffected. From observing the cross section of the sample (fig.6.12b) the FDTS layer was measured as being only 5.29nm (from the difference in contrast from SEM imaging), although it is quite possible that the layer is indeed thinner due to the quality of the image.

Once the anti-sticking layer had been assessed and found to be suitable, replication of the master PSi surface onto a stamp was attempted. The master wafer was placed onto one side of the master replication tool (MRT) followed by a thin 200mm^2 glass wafer on the other. The master replication tool is used for soft stamp production by using two heated vacuum chucks. The glass wafer had been treated previously with an adhesion promoter. Both substrates were held in place by vacuum. 10grams of PDMS was then degasses

thoroughly and poured onto the surface of the master wafer. The tool was then closed, applying the glass wafer on top of the PDMS layer creating a Si wafer/PDMS/Glass wafer stack. A picture of the stack in the master replication tool is shown in fig.6.13.

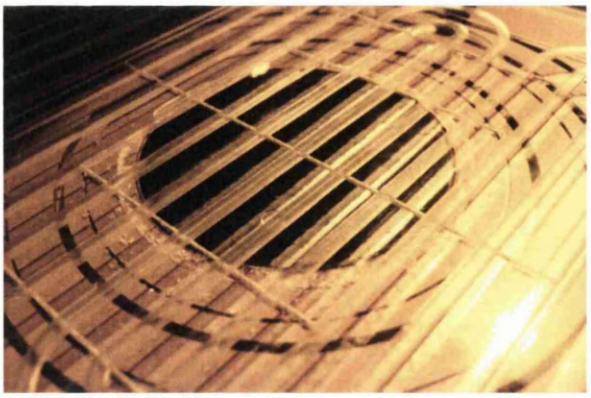


Figure 6.13: SCIL Stamp replication of PSi features using master replication tool

Following a 2 day cure in the MRT to harden the PDMS, the stack was removed and loaded into the separation tool (fig.6.14). The tooling essentially used two plates, one to vacuum contact the master wafer and the second to vacuum contact the glass substrate. The two plates were then slowly separated to remove the stamp (PDMS with glass substrate) from the master wafer.

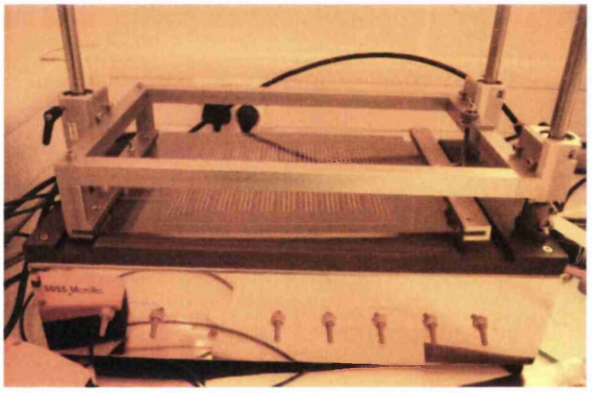


Figure 6.14: SCIL Stamp separation tool

Unfortunately it was extremely difficult to separate the master wafer from the stamp. Full separation was not possible and during the process the glass substrate broke. To observe what was going on at the interface between the master and PDMS, the stack was cut into several pieces and SEM performed on the cross section of the samples. To aid with SEM analysis, the samples were sputtered with a thin 8nm gold layer so they became electrically conducting. From investigation of the contact interface between the PDMS and PSi surface, two issues were observed.

The first problem was related to the separation itself. From fig.6.15 it can actually be seen that in various areas of the PDMS/PSi interface, during the separation the PDMS

delaminated the PSi layer from the Si base. The adhesion between the PDMS and PSi layer must have been strong enough that the porous layer can be physically broken away from the base material. Such adhesion over such a large area as a 4" wafer would result in an enormous force required to pull away the layer of PSi. Due to this adhesion, large scale separation was unsuccessful. It is suggested that as the FDTS coating was shown previously to be an effective anti-sticking layer, the very nature of the porous silicon was to blame. When first applied the PDMS was liquid and able to flow into the pores of the silicon surface. Some of the pores are not perfectly vertical in nature and deviate from the normal. PDMS that had made it into such pores upon curing became solid. The force required to pull the PDMS from the deviated pores was so large that the surrounding PSi detached from the wafer. It is also surmised that an even coating of the anti-sticking layer in such pores could be compromised leading to sidewall adhesion. Height aspect ratio of pores could therefore be unsuitable for the SCIL process.

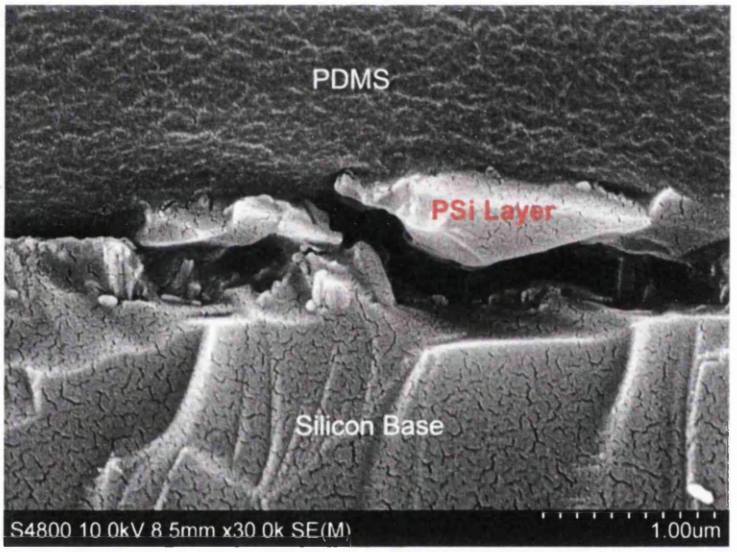


Figure 6.15: PSi detachment from Si base

The second issue exposed was related to the coverage of the PDMS layer. From the SEM image of fig.6.16a, it is clear that in some areas large cavities exist between the PDMS and PSi surface. The higher magnification image (fig.6.16b) shows a series of silicon pores that are completely empty. It is suggested that the small diameters of the pores restrict the flow of the viscous PDMS during stamp replication. One reason for this is that as the PDMS flows across the top of the PSi, air can be trapped inside some of the pores. Since there is no way of the air escaping, the PDMS is unable to penetrate into the pores.

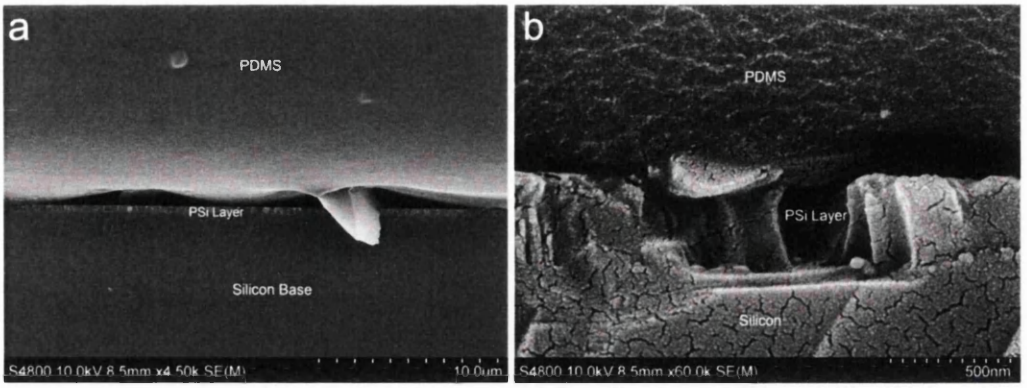


Figure 6.16: Cavities between PDMS and PSI

From investigating the use of SCIL for PSi replication, several problems were encountered. Despite the successful application of an anti-stick layer, separation of the master wafer from the stamp was unsuccessful. Further investigation was performed which found that some areas of the PSi layer had been torn away from the silicon base substrate. Other areas revealed the opposite effect, where no PDMS had entered the silicon pores. Overall the use of SCIL for PSi replication has proven to be quite difficult due to the high aspect ratio structures that PSi is comprised of. Enhanced anti-sticking layers, PDMS viscosity modification and conducting the replication in a vacuum could potentially solve the issues encountered. Unfortunately such enhancements would inevitably add to the complexity of technique and could prevent its mainstream use.

6.3.3 Porous Silicon – Electrochemical etching

Electrochemical etching is a well established technique of producing porous silicon. The main issue with its use for mass production is the need to isolate the rear surface of the silicon substrate and the rear electrode from the electrolyte solution. The purpose of the experiment was to design, fabricate and test an electrochemical etching cell/chamber that could successfully insulate the rear silicon surface and contact from the solution. As the electrolyte in electrochemical etching of porous silicon is often HF [4], components of the chamber had to be HF resistant. Due to severe health risk associated with the acid, the chamber was also designed to allow for secondary containment of the acid if a leak should occur. Fig.6.17 shows the design of the electrochemical chamber.

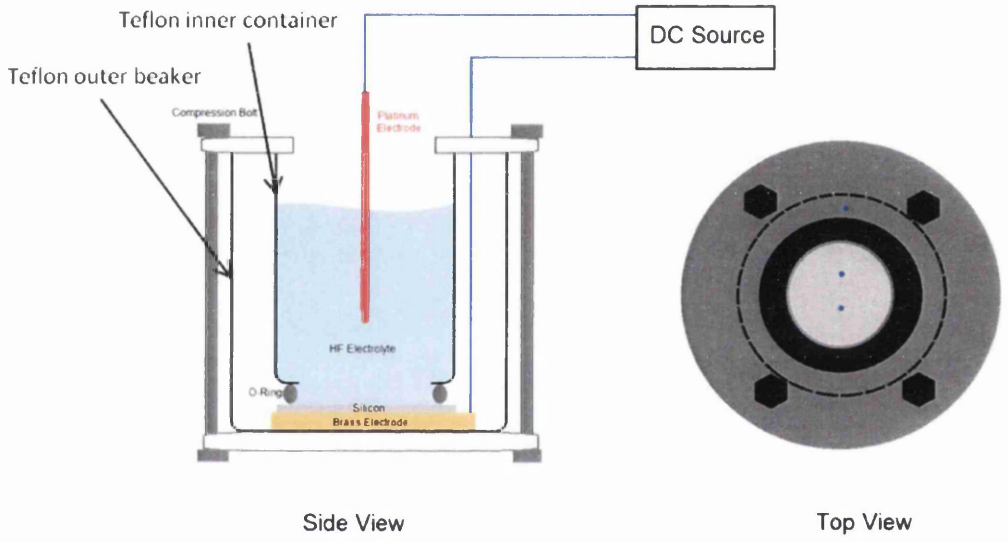


Figure 6.17: Design of chamber for electrochemical etching of PSi

The design of the chamber allowed for a brass electrode to be seated in a large outer beaker onto which the silicon substrate would be placed. A second smaller beaker with the bottom removed and a sealing o-ring could then be lowered onto the silicon substrate. Compressing the inner and outer beakers together would deform the o-ring thereby creating a watertight seal. The electrolyte solution could then be added into the inner beaker, in turn contacting the front surface of the silicon substrate only. As the rear electrode was situated in the outer beaker, it was insulated from the etching solution. The chamber was also designed so that if a leak through the o-ring did occur, the solution would exit into the outer containment beaker, where it could be safely removed.

It was important that materials were used to construct the chamber to resist the acid electrolyte (HF). Polytetrafluoroethylene (PTFE) beakers were used as the inner and

outer containment vessels. One of the most important components in the design was the use of an o-ring to contain the solution in the inner most beaker only. Standard nitrile o-rings were found to seriously degrade in HF. Fluorocarbon polymer o-rings (Viton®) were selected instead due to their excellent chemical resistance. The components of the chamber are shown in fig.6.18a along with the assembled chamber fig.6.18b.

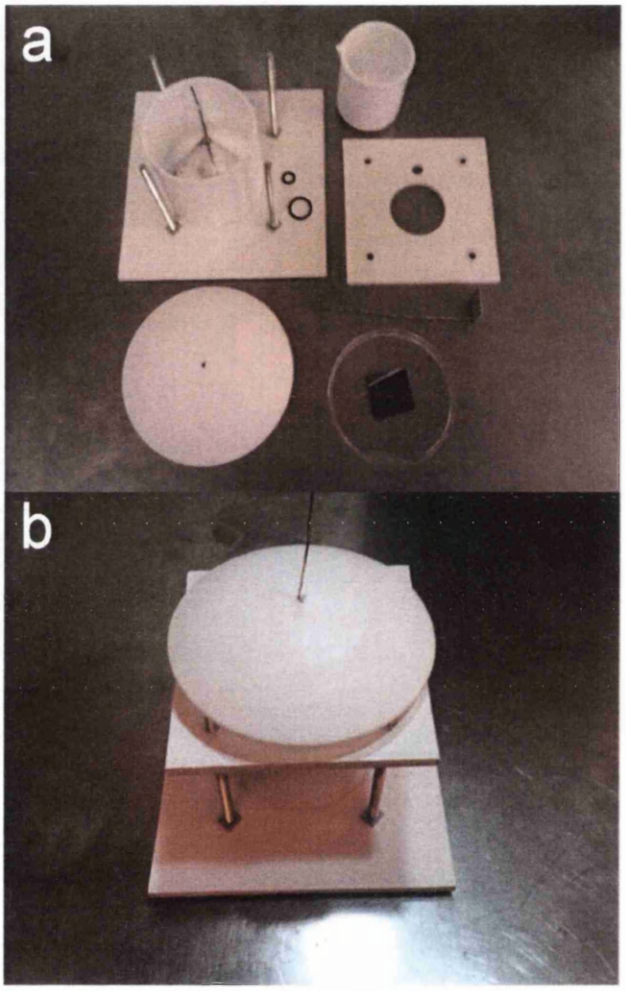


Figure 6.18: a) Chamber components and b) Fully assembled chamber

Following construction of the chamber, an initial etch was performed to evaluate its performance. From the literature [4] a suitable constant voltage of 1.5V was identified and used with an electrolyte solution of 50% HF. The voltage transpired to a current of 15.4mA over the area to be etched, measured as 0.6cm^2. After two minutes, etching was stopped and the chamber emptied. Upon removal of the silicon sample it was apparent that the area exposed to electrochemical etching had reduced reflectivity (fig.6.19).

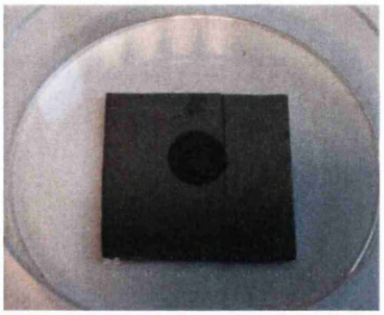


Figure 6.19: Si substrate after etch at 1.5V, 15.4mA for 2minutes

SEM was performed on the region in order to observe the effect of the etching process. From fig.6.20 the silicon surface has pores from the etching process; hence a PSi layer was formed. From further magnification of the surface the pores are uniform across the sample with measured diameters of around 5nm. The presence of a PSi layer confirmed that the etching chamber was capable of producing porous silicon.

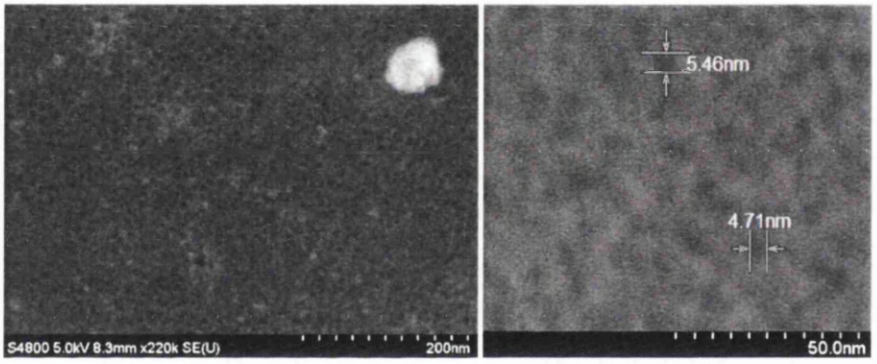


Figure 6.20: SEM of Si substrate after etch at 1.5V, 15.4mA for 2minutes

Although electrochemical etching of silicon was confined to a small area during this experiment, this was due to the size of the chamber constructed. By scaling up the chamber, full wafers could be etched using this simple technique. If a PSi layer could be electrochemically produced, mimicking the anti-reflective properties of previous investigations, the technique could replace standard industrial anti-reflective processes. Although the area of PSi obtained from using the electrochemical etching chamber was too small for reflectivity measurements, electrochemical etching has been shown to produce an effective anti reflective layer, yielding 15.5% efficient silicon solar cells [5]. It is important to mention however that further work is required to assess the surface passivation capability of such a PSi layer.

6.3.4 Zinc Oxide (ZnO) nanowires

Alternative anti-reflective processes to enhance existing anti reflecting surfaces were also investigated. One such technique was the use of ZnO nanowires to enhance the anti-reflective properties of commercially used textured silicon cells deposited with a SiN_x ARC.

The experiments into ZnO nanowire enhanced ARCs were conducted along with a fellow member of our research group at the university, Dr Yufei Lui. My role in the work was to assist in the fabrication and measurement of the cells.

For these experiments, 5cm x 5cm (100) p-n doped (200μm thick) reclaimed textured silicon substrates were used. Texturing was performed using the standard KOH recipe outlined in Chapter 4. The next step was to spin coat a solution of zinc acetate on the textured samples. The zinc acetate was deposited as the seed layer for ZnO growth. Spin coating of the zinc acetate solution onto the samples was performed at 3000rpm for 40 seconds, followed by a post bake at 160°C for 7 minutes. The samples were next submerged in a growth solution of hexamethylentramine and nitrate hexyhydrate, dissolved in de-ionised water. The samples in the solution were placed into an 800W microwave for 2 minutes to promote growth of the ZnO nanowires. After microwaving, the samples were removed from the solution and blown dry with low pressure nitrogen gas as not to damage the newly formed nanowires. More information on the microwave assisted synthesis process of ZnO nanowires growth can be found in the work by Unalan *et al* [6]

A SiN_x ARC layer was then deposited onto the ZnO nanowire surface using plasma enhanced chemical vapour deposition equipment (Oxford Plasmalab80 PECVD). The PECVD process consisted of two process gases, NH_3 and $5\%SiH_4+95\%N_2$, with flow rates of 50sccm and 100sccm respectively. A chamber pressure of 1000mTorr was used along with an RF power of 20W. The samples were placed on a heated platen (250°C) within the equipment and nitride deposited using the above conditions for 6 minute duration.

After deposition of the ARC, SEM imaging was performed on the surface. Fig.6.21a depicts a micro-textured pyramid after the growth of ZnO nanowires and the subsequent deposition of SiN. ZnO nanowires are clearly present crating a uniform coating on the pyramid. A sample was also cleaved so that the cross-section of the layer could be analysed. From fig.6.21b, the cross-section image reveals the textured Si/ZnO nanowire/SiN ARC structure. The images of ZnO nanowires show that the process was successful in fabricating the Si/ZnO/Nitride structure.

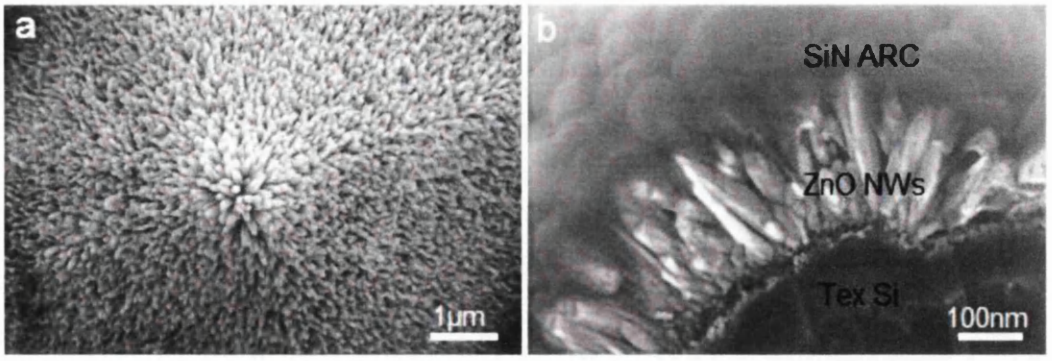


Figure 6.21: ZnO nanowires on textured Si, a) Top view, b) Cross-sectional view

Reflectivity measurements were subsequently conducted in order to measure the effectiveness of the enhanced ZnO ARC coating. In order to compare the process, standard textured substrates and ones coated with a SiN ARC were measured. Fig.6.22 shows the reflectance of each sample.

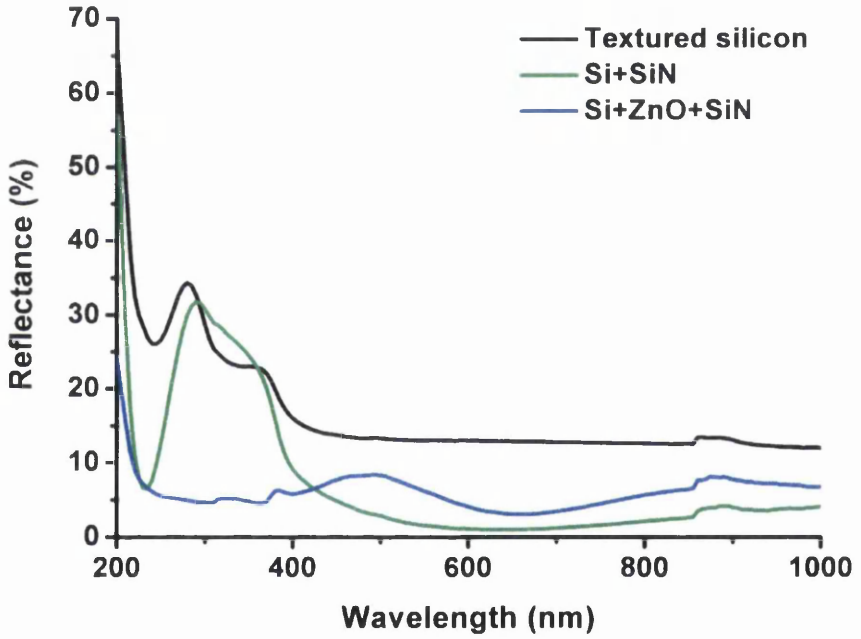


Figure 6.22: Reflectivity measurement of textured silicon surface with SiN and ZnO+SiN

From fig.6.22, the results show that the anti-reflective properties of bare textured Si were enhanced by 54.25% with deposition of a SiN_x ARC. By the addition of a ZnO/SiN onto bare textured Si the enhancement is increased to 63.68%. Therefore the ZnO-SiN combined ARC layer reduced the reflectance from 16.86% to 6.12% in comparison with the textured silicon substrate. Even compared to a textured Si sample with an additional SiN ARC, the addition of ZnO nanowires still related to an enhancement of 1.59% across the effective absorption range.

Finally, textured silicon samples were processed into functioning silicon solar cells. Front and rear contacts were screen printed onto the cell and fired in the standard four zone IR belt furnace. Fig.6.23 shows the finished solar cell. As in the reflectivity comparison, other textured cells were produced and subsequently coated with a SiN ARC layer in order to compare against the ZnO enhanced cells.

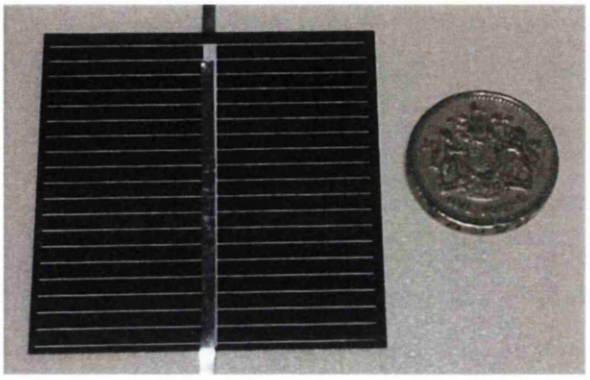


Figure 6.23: Fully fabricated reclaimed silicon solar cell with the ZnO and SiN combined ARC

The electrical efficiency of fabricated cells was measured using an Oriel® I-V solar tester (Newport Corporation). Based on the AM1.5 solar spectrum, the test showed that the photoelectric conversion efficiency of the cells with the ZnO-SiN combined ARCs was increased from 17% to 17.3%, compared to the efficiency of the cells with a SiN ARC only (fig.6.24). It should be noted that doping and carrier mobility in the reclaimed silicon wafers was not optimised, thus limiting cell performance. Nevertheless, it is clear that cells using the ZnO-SiN combined ARCs perform better than those using a standard SiN ARC.

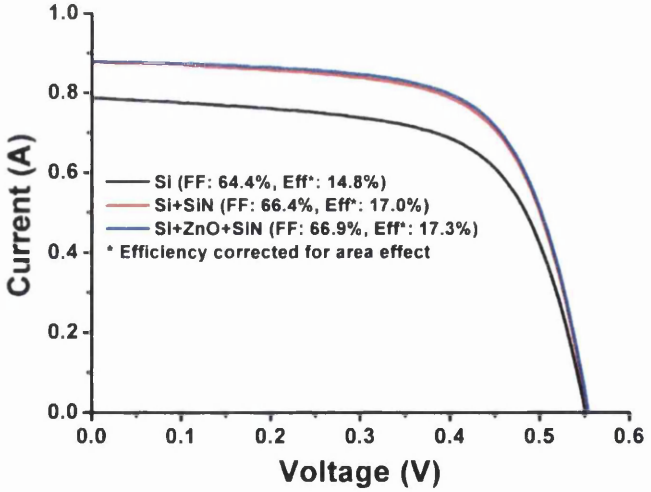


Figure 6.24: I-V performance of the solar cells with SiN and ZnO+SiN ARC

From experimentation, a novel microwave based rapid growth of ZnO nanowires was successfully implemented and applied to low cost silicon solar substrates. ZnO-SiN combined ARCs were developed and studied for the application of enhancing the light

capture properties of low-cost solar cells, based on reclaimed silicon substrates. The results show that the solar light capture property of the ZnO-SiN combined ARCs was increased by 1.59%, resulting in an efficiency improvement of 0.3%, in comparison with the conventional monocrystalline textured silicon solar cells with just a standard SiN ARC.

6.4 Summary

The majority of this chapter focused upon the use of porous silicon as a viable alternative to texturing. From previous work in Chapter 5, thin silicon solar cells were produced from (100) monocrystalline silicon substrates by an exfoliation method. As exfoliation disrupts the surface structure of the silicon substrate, conventional alkaline etching to produce textured silicon pyramids could prove difficult. PSi was identified as an alternative anti-reflective structure which uses acid based etching mechanisms which are not orientation dependent.

Experimentation into the formation of porous silicon via metal assisted etching (MAE) was implemented first. Sputtering equipment was used to deposit silver nanoparticles onto polished reclaimed silicon substrates. Subsequent etching underneath the particles resulted in pore creation. From deposition and etching a series of interconnected silver particles with average diameters of around 30nm, and a very low reflectivity of 6.68% was measured. Such a reflectivity was not only lower than standard KOH textured substrates, but also lower than that of commercially used textured Si with an additional SiN ARC layer. Since the PSi had such excellent anti-reflective properties, it could potentially replace not only the texturing process but also the additional ARC coating also. Therefore solar cell reflectivity suppression could be achieved in a single step. However silver deposition by sputtering is a costly step, so alternative low cost methods of PSi formation were investigated.

Substrate conformal imprint lithography was assessed as such a technique. Unfortunately due to the high aspect ratio of the PSi surface, issues were encountered during stamp replication.

Another potentially low cost method was electrochemical etching of PSi. A special chamber was constructed in order to trial the process. From initial experimentation it was found that PSi could be successfully produced using simple equipment. Although the area of PSi obtained from using the electrochemical etching chamber was too small for reflectivity measurements, electrochemical etching has been shown in literature to produce an effective anti reflective layer, yielding 15.5% efficient silicon solar cells [5]. It is therefore suggested that the electrochemical etching setup could potentially be adopted by industry for anti-reflective PSi formation.

Although this chapter dealt mainly with porous silicon structures, an enhanced ARC was also investigated. ZnO nanowires were used to reduce reflectivity of a commercially adopted process even further. By using ZnO nanowires grown on textured Si substrates and

deposited with a SiN ARC, reflectivity was found to decrease even further. The process of growing the nanowires used a rapid microwave growth technique. Full silicon solar cells manufactured using the process exhibited an efficiency improvement of 0.3% in comparison with conventionally produced textured silicon solar cells with just a standard SiN ARC.

[1] Hui Fang *et al*, Silver catalysis in the fabrication of silicon nanowire arrays, Nanotechnology, 17, 3768, 2006
[2] Svetoslav Koynov *et al*, Black nonreflecting silicon surfaces for solar cells, Appl. Phys. Lett. 88, 203107, 2006
[3] Weimin Zhou *et al*, Nanoimprint lithography: a processing technique for nanofabrication advancement, Nano-Micro Letters, (2), 135-140, 2011
[4] Michael J. Sailor, Porous Silicon in Practice: Preparation, Characterization and Applications, First Edition. Wiley, 2012
[5] Salman, Khaldun A.; Hassan, Z.; Omar, Khalid, Effect of Silicon Porosity on Solar Cell Efficiency, International Journal of Electrochemical Science, Vol. 7 Issue 1, p376-386. 11p, 2012
[6] Husnu, Emrah U., *et al*, Rapid synthesis of aligned zinc oxide nanowires, Nanotechnology, Vol 19, 25, 2008

Chapter 7: Silver Nanowire Solar Cell Enhanced Contacts

7.1 Introduction

The importance of reducing the reflectivity of a cell has been shown in Chapter 7. More light capture essentially translates to more current generated by a cell. Ensuring that this extra current is not wasted requires efficient metallic contacts to be made to the semiconductor substrate. The front metallization of a typical crystalline silicon solar cell is responsible for collecting the current generated. It is therefore essential to the efficiency of a cell that there is a sufficiently large top contact to collect as much current as possible. Satisfying these criteria in most semiconductor devices is relatively straight forward, by applying a block contact. However a solar cell requires photons of sunlight to be able to enter the cell through the very same surface on which the contact is situated. Applying a standard block contact would therefore render the device inoperable, as no light would enter the cell so the photovoltaic effect would not take place. On the other hand, applying a small contact would allow lots of light to enter the cell but current collection would be very poor. For silicon photovoltaic devices there is thus a trade-off between contact area and shading. If contacts are spaced too far apart then resistive losses become large (carriers must travel a larger distance to the contacts therefore increasing the probability of recombination before reaching the contacts), too close and shading losses become a problem. Front contacts are therefore designed as a compromise of the two loss mechanisms. Figure 7.1 shows a crystalline silicon solar cell with a typical front contact structure.

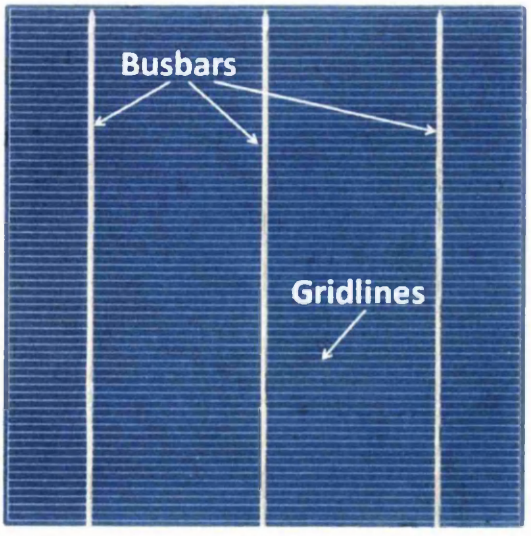


Figure 7.1: Typical silicon solar cell with three busbar top contact arrangement

In fig.7.1, the cell contact consists of three busbars and a large number of smaller gridlines. Since screen printing is commonly used, limitations of gridline widths are around 100µm. Various alternative metallization techniques can be used to produces smaller gridlines for silicon photovoltaics such as sputtering [1] and plating [2]. Having thinner gridlines (<100µm) is advantageous but more complex and expensive equipment is required, ultimately adding to the processing cost of a cell. The added efficiency benefit in relation to an increased price is deemed not to be cost effective.

Screen printing metallization for silicon solar cell front contacts is well established and relatively cheap with a high throughput also. Enhancing the electrical performance of a conventional screen printed contact without adding significantly to shading loss would be highly advantageous. The use of transparent conducting electrodes (TCE) has fulfilled such a requirement. Unfortunately ITO has several issues related to it. The main issue is that indium as a material is in short supply and therefore expensive [3].

In recent years, several investigations have focused upon the use of conducting nanowires as transparent conducting electrodes (discussed in more detail in Chapter 3 of this thesis). Silver nanowire contacts have been shown to have excellent electrical performance, while maintaining good optical transparency (fig.7.2).

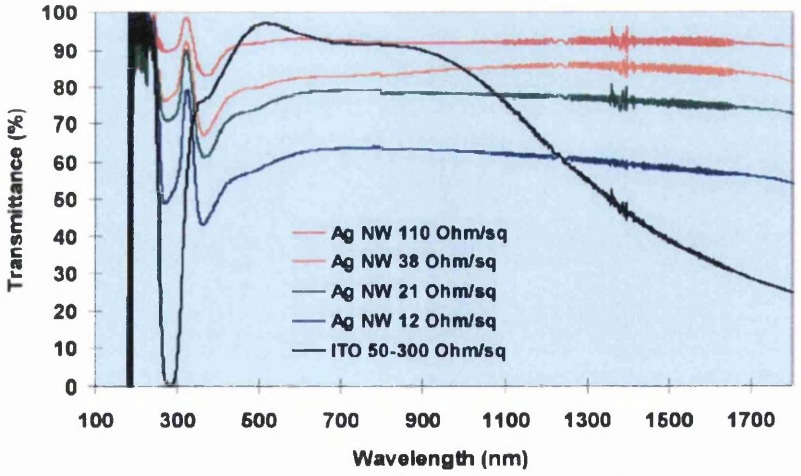


Figure 7.2: Optical transmittance of transparent Ag NW electrodes [4]. Nanowire density decreases resistivity but also decreases transmittance

The vast majority of applications using silver nanowires have been related to its use as a replacement for ITO. Little research has been conducted around the use of silver nanowires to enhancement the electrical performance of standard screen printed silicon solar cell

contacts. Only one article was found analysing the affects of silver nanowire deposition contacts for crystalline silicon solar cells, and this article stated that such an application had not been previously demonstrated [5]. The publication did not use nanowires to enhance a standard top contact (as will be presented in this work) but instead as a standalone transparent conducting top contact. Work by J. W. Gao *et al* [6] studied the effects of a nanowire contact on textured silicon, however the nanowires were not deposited but made up from a series of silver nanoparticles sintered together.

The fundamental purpose of this experimental study is to analyse the affect of applying silicon nanowires to a conventionally produced silicon solar cell front contact. Factors investigated include nanowire deposition methods, conductivity trials and the suitability of various silicon surfaces for the contact process. After investigation of such parameters, a repeatable fabrication process was developed to produce silver nanowire enhanced silicon solar cell devices.

7.2 Experimental Procedure

Reclaimed polished and textured silicon wafers, supplied by Pure Wafer Plc, were cut into various sizes dependent on the experimental process. As every wafer undergoes a rigorous cleaning procedure at the factory (complying with the requirements of the microelectronics industry) additional cleaning was not required. Where textured substrates were used, texturing was performed at the Pure Wafer factory using KOH wet etching. Additional information on the cleaning and texturing procedures implemented at Pure Wafer can be found in Chapter 4. Silicon solar cells were processed using the standard conditions also outlined in Chapter 4.

Solar cell samples were either Meyer rod or spray coated with 115nm diameter (35μm in length) silver nanowires supplied from Seashell Technology.

After nanowire deposition, dimensional measurements and surface characterisation was performed with a Hitachi S4800 Scanning electron Microscope. For electrical efficiency measurements, a Newport Oriel® I-V Test Station was used at standard AM1.5 solar spectrum.

7.3 Experimentation Results

7.3.1 Deposition Trials

Depositing silver nanowires onto an existing silicon solar cell structure could allow for enhanced current collection with minimal increases in shading losses. Before experimentation could be carried out to determine the effect of such an application of nanowires, a viable deposition method had to be determined. An in depth literature review revealed two suitable deposition techniques; rod coating and spray coating.

To assess the suitability of the two methods for the PV cell application, silver nanowires were rod and spray coated onto polished silicon samples. 20mm x 20mm single side polished (600µm thick) silicon samples were cleaved from a 200mm parent wafer using a diamond scribe. Silver nanowires with diameter 115nm and 35um in length were purchased from Seashell Technology. The nanowires were supplied in a solution of Isopropanol (IPA) at an estimated 1wt%. For deposition trials, the nanowire solution was diluted further with IPA at a ratio of 1:10. The final solution gave an equivalent of 1000ppm of nanowires in IPA. 25µL of the solution was applied to the silicon samples by either rod or spray coating.

Rod coating of the silver nanowire solution was completed using a 10# (number 10) Meyer Rod (wire wound rod that meters the deposition medium). The solution was first pipetted onto the edge of the silicon substrate before being drawn across the sample using the rod. Fig.7.3 depicts the Rod Coating experimental setup used.

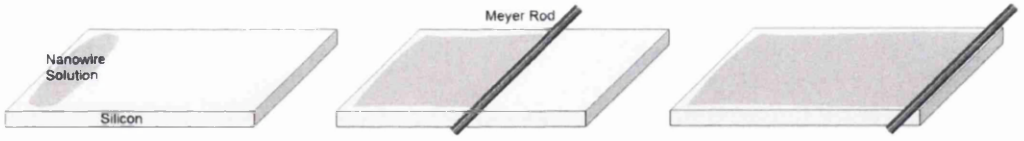


Figure 7.3: Silver nanowire rod coating procedure

Spray coating of the silver nanowire solution was completed using an Iwata HP-AR airbrush. The solution was pipetted into the internal tank of the airbrush before being sprayed over the sample using a constant back and forth movement. For uniform deposition, the spray gun was kept at a distance of 5cm above the sample. To avoid contamination, nitrogen gas at a pressure of 1bar was used as the propellant for the airbrush. At such pressure, the rate of deposition was calculated to be 97.8µL/s. Fig.7.4 details the Spray Coating experimental setup used.

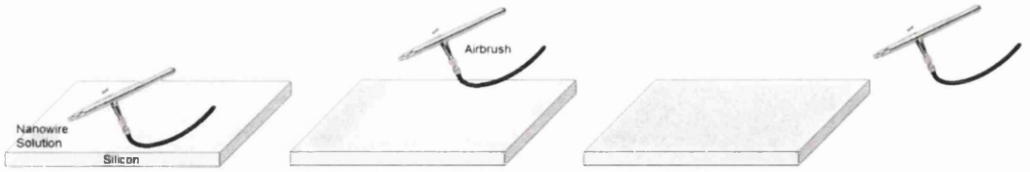


Figure 7.4: Silver nanowire spray coating procedure

After the nanowire solution was applied using both methods, SEM (Hitachi S4800) was used to characterise the uniformity of the two deposition techniques. White light Interferometry was also performed on samples (Veeco NT-2000) in order to measure topographical changes.

From Fig.7.5 it is apparent that the rod coated silver nanowires have been uniformly spread across the polished silicon surface. The wires are relatively straight and range from just a few microns to tens of microns in length. The nanowires are arranged in a largely random fashion with some overlapping one another, forming a mesh type structure. The mesh is not entirely continuous due to the presence of isolated wires. The discontinuity suggests that more nanowires are needed for a complete mesh to be formed.

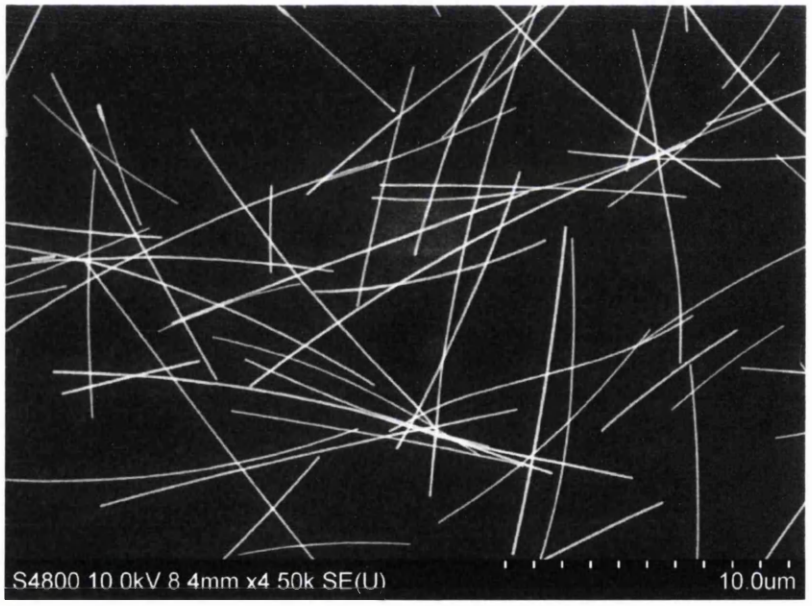


Figure 7.5: Rod Coated AgNW's on Polished Si Substrate

Nanowires deposited by spray coating (fig.7.6) exhibit traits similar to that of the rod coated samples. Such shared qualities include; uniformity, variable length of wires and the inconsistency of a complete mesh. The main difference of spray coating is that the nanowires are not as straight. It can be clearly seen in the SEM image of fig.7.6 that several

of the wires have significant curvature, with one forming a complete circle. An explanation for the difference can be attributed to the very high aspect ratio of the wires (micros in length but nanometers in diameter). When ejected from the airbrush, drag on the very thin wires causes them to curl up in mid air. Since the nanowires are inelastic they land on the silicon surface with the same curvature.

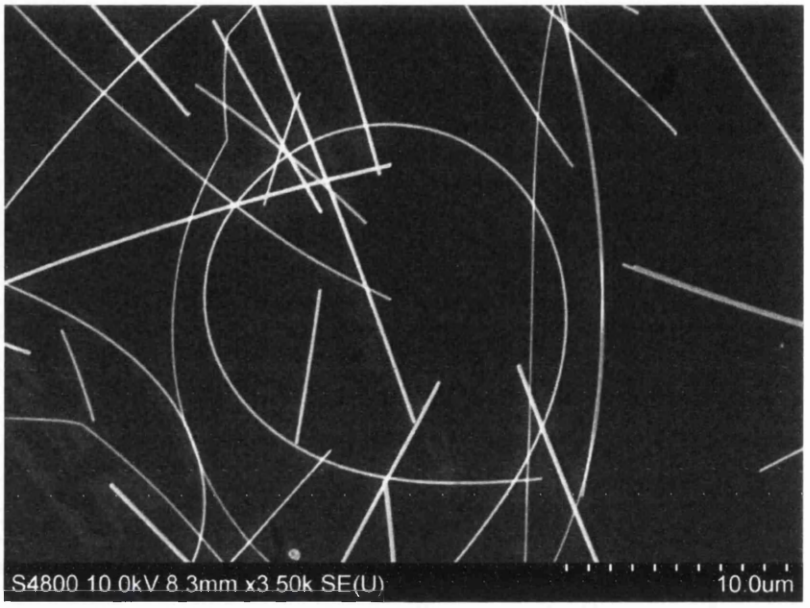


Figure 7.6: Spray Coated AgNW's on Polished Si Substrate

After analysing the deposition methods, it was found that both succeeded in depositing uniform silver nanowire layers on a polished silicon substrate. Before the deposition methods could be applied to silicon solar cells, the structure of the cell was investigated for suitability of rod and spray coating. Primary analysis was conducted using SEM imaging to visualise the surface topography of a typical silicon solar cell, on to which silver nanowires would be coated. From the study, two significant observations were made that ruled out rod coating as a suitable candidate for nanowire deposition.

The first issue (visualised in the SEM image of fig. 7.7) shows the random pyramidal micro-texturing of the surface of a silicon solar cell. It is apparent that the surface is very rough with good anti-reflective properties (as it was designed to be) but is not suitable for rod coating applications. Rod coating is effective only with relatively flat surfaces. Such a rough surface as textured silicon with sharp pyramids could damage the fragile silver nanowires as they are drawn across the sample.

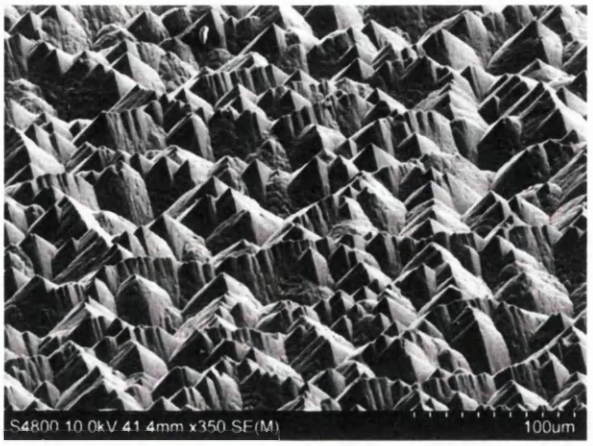


Figure 7.7: SEM image of pyramidal micro-texted surface of a typical silicon solar cell

The second issue involves the front contact topography of a conventional silicon solar cell. As rod coating works best on flat surfaces, any topographical changes could cause the road to deviate and deposit uneven areas of the nanowire solution. Fig.7.8 shows the front surface of a silicon solar cell. Front contacts are applied by arranging a series of narrow gridlines connected by a central busbar. Such gridlines are typically screen printed and have a width around 170µm. It is apparent from the image that the silver front contact is protruding from the surface of the cell and white light interferometry was used to measure the step change. From the Interferometer data (fig.7.9), the front contact gridline height was measured to be around 30µm.

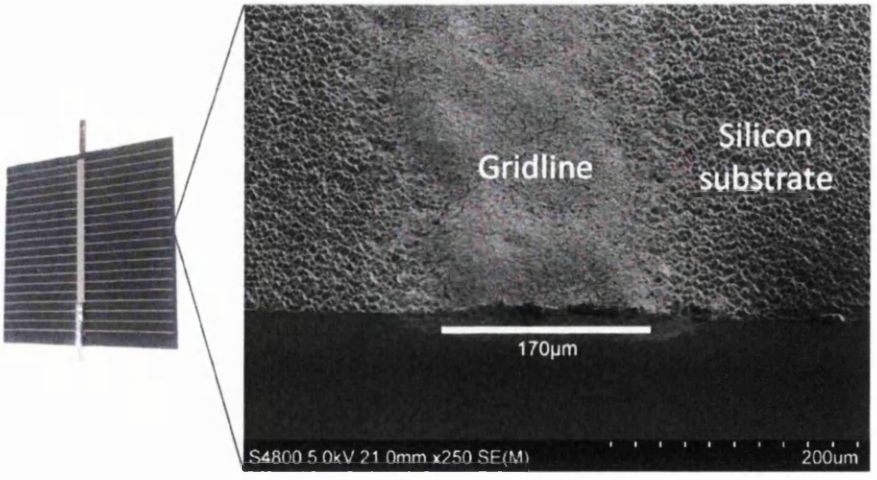


Figure 7.8: SEM image of a silicon solar cell front contact gridline

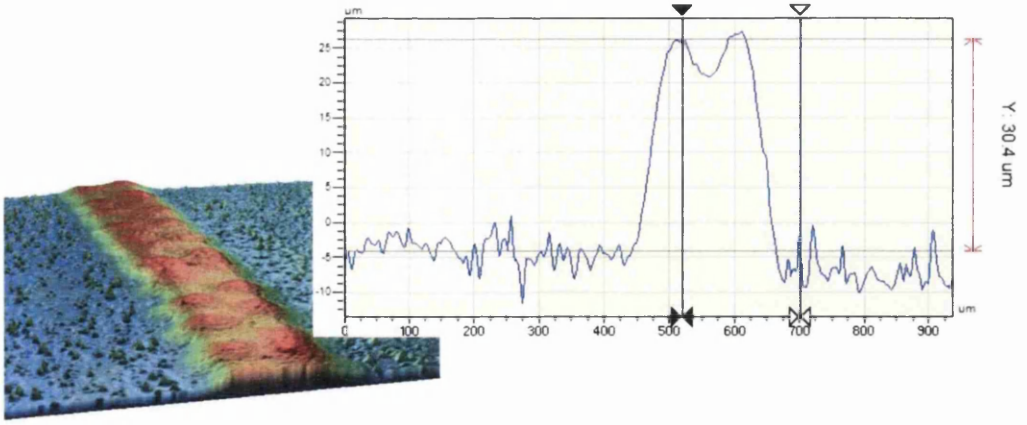


Figure 7.9: Interferometry (3D and line profile) of front contact gridline step height change relative to the silicon substrate

Using the data obtained for a typical silver front contact gridline of a solar cell, the rod coating process for nanowire deposition becomes problematic. The method essentially draws the nanowire solution across the silicon sample. When faced with a sharp gradient change such as a protruding gridline contact, the rod would unavoidably deviate upwards, as illustrated in fig.7.10. Such a movement would leave an unregulated gap underneath the rod where nanowires could collect.

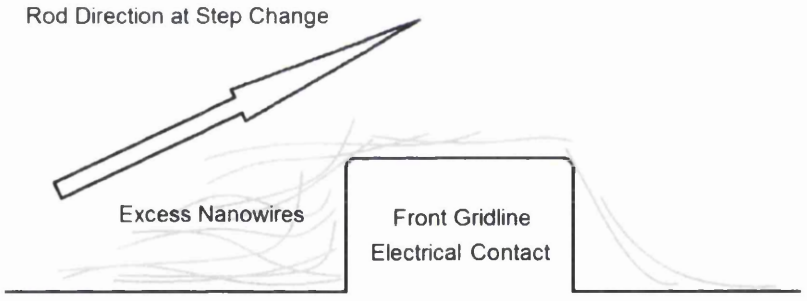


Figure 7.10: Depiction of step change on rod coating silver nanowires

Spray deposition is not as susceptible to step changes as rod coating, due to the non-contact elevation of the airbrush. As the solution is being deposited above the sample surface, collection around step changes is not such an issue, as illustrated in fig 7.11.

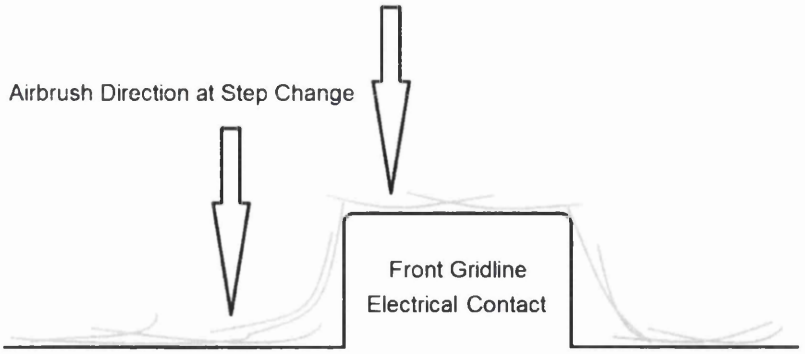


Figure 7.11: Depiction of step change on spray coating silver nanowires

After extensive investigations, it was concluded that for silver nanowire deposition onto textured silicon solar cells, spray coating is the preferred method. Due to the rough surface from silicon texturing and the significant changes in step height across the wafer surface (contact gridlines), rod coating was ruled out as a viable deposition method. Such surface roughness and variable topography would not only damage the fragile nanowires, but cause them to collect at the base of existing contact gridlines. Spray coating is not affected by such roughness and topographical changes. Thus spray coating is suited most for applying nanowires to an existing silicon solar cell.

After a suitable deposition method had been found, the next challenge was to assess the transmittance and conductivity of a spray coated silver nanowire mesh.

7.3.2 Conductivity Trials

Before applying silver nanowires to actual solar cells, importance was placed on finding the minimum amount of solution required for a conducting nanowire mesh to be formed. Any isolated regions of nanowires would not contribute to contact enhancement. In fact the areas would shade active cell area with no additional efficiency benefits.

A copper printed circuit board (PCB) was designed and fabricated (fig.7.12) in order to assess the conductivity of a silver nanowire mesh between spaced apart contacts. The copper track contacts were spaced 1mm apart to simulate the distance between two front contact gridlines of a silicon solar cell. The size of the circuit board was designed to be 5cm x 5cm to simulate the size of a small scale silicon solar cell which would ultimately be fabricated once conductivity trials had concluded.

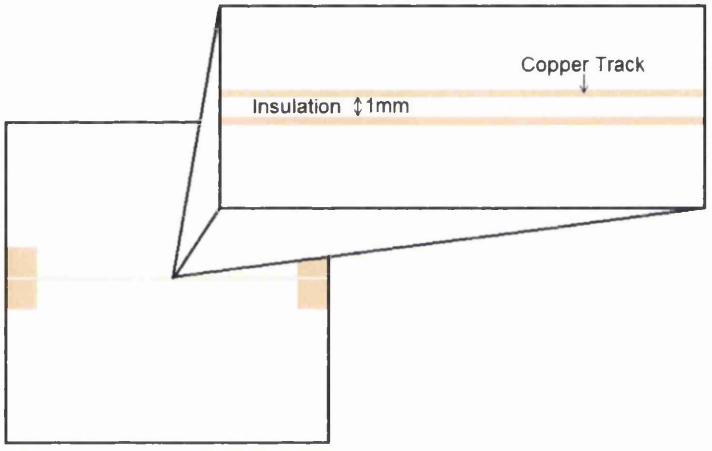


Figure 7.12: PCB layout of copper tracks on insulating substrate for silver nanowire conductivity trials

A ratio of 1:10 AgNW solution to IPA was used. Each applied spray coated layer used 104µL of the prepared solution. The same Iwata HP-AR airbrush was used with nitrogen gas at a pressure of 1bar, corresponding to a deposition rate of 97.8µL/s. Since the contacts were electrically isolated from one another, a mesh of nanowires formed across the contacts should result in a change in conductivity. To find the minimum silver nanowire concentration required for an effective conducting mesh, the solution was spray coated across the whole sample. I-V measurements were then performed between the two PCB contacts using an electrical analyser and probe station. If no conduction was observed, another layer was applied and the procedure repeated, until conductivity was recorded (indicating the presence of a continuous mesh).

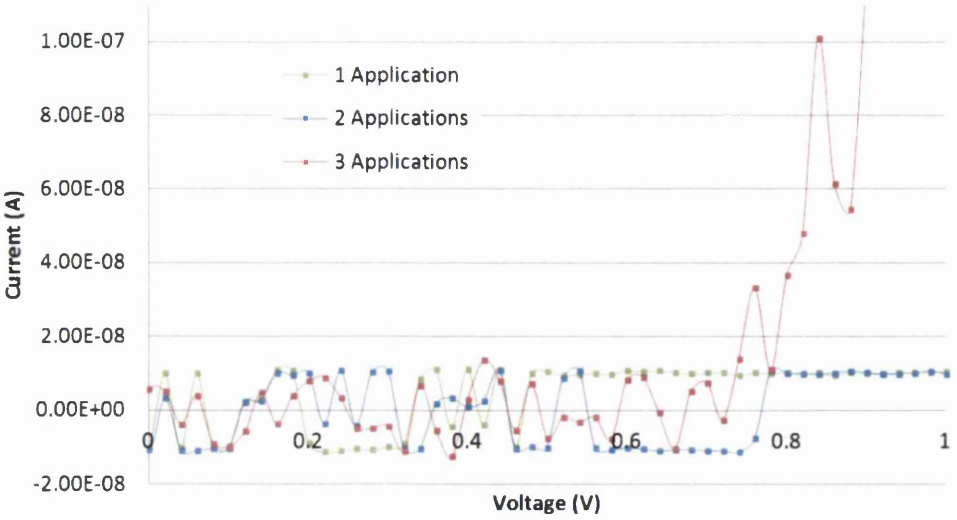


Figure 7.13: Electrical measurement across 1mm gap (between the Cu tracks) after application of nanowire layers

After one application (104µL) of the nanowire solution, no conductivity was observed (Green IV trace fig.7.13). The current was essentially zero indicating an open circuit between the two PCB contacts. A second application of the solution was made and the sample re-measured. The sample, now with two layers, still did not exhibit any conduction; once more indicating an open circuit between the contacts. After the third application the sample began to show signs of possible conduction, albeit with very low current. It can be seen from the third application plot that the current begins to slightly increase at a voltage range of 0.8V-1V. Despite the increase the current remains in the micro to nano amp range (MΩ resistance).

After a forth application, the sample had been subjected to a total of 416µL of the silver nanowire solution (before evaporation of the IPA). When IV measurements were performed between the PCB contacts, the sample showed conductivity (fig.7.14). Averaging the current and voltage readings resulted in an average resistance of 652Ω.

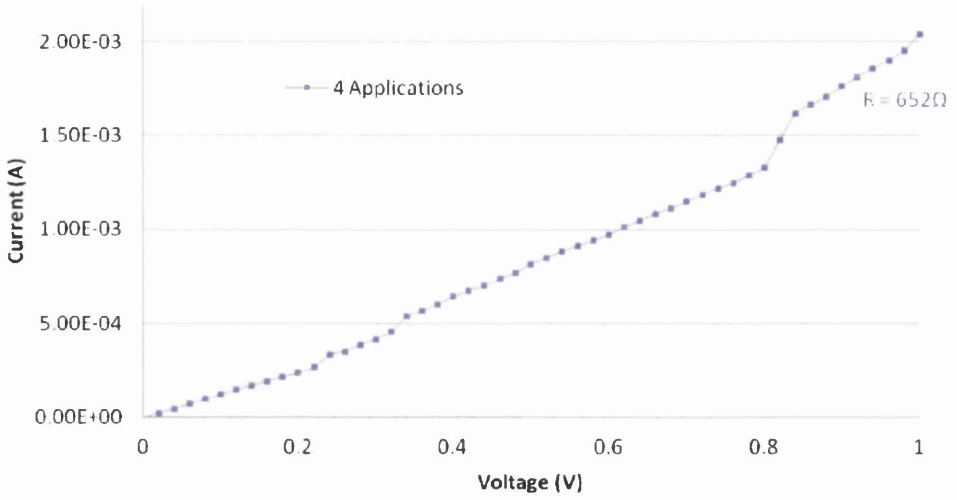


Figure 7.14: Electrical measurement across 1mm gap after application of 4th nanowire layer

Following the successful conductivity trials, the nanowire layers were characterised using SEM imaging.

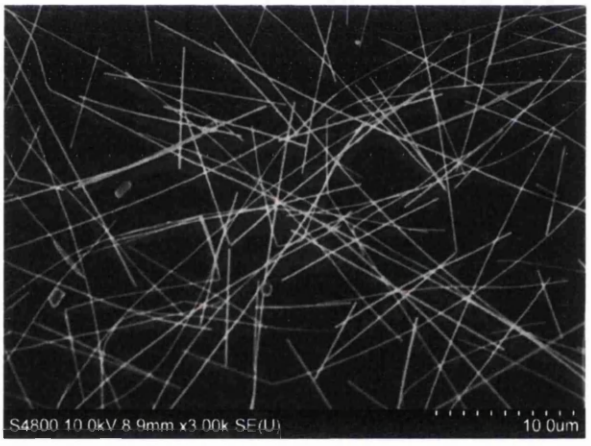


Figure 7.15: SEM of 4 layers of silver nanowires

Since most nanowires in the mesh were now in contact with one another, current was able to flow. Thus, from experiments it was found that 4 applications (416 µL) of AgNW solution was required to construct a conducting mesh across a gap of 1mm. The average resistance of the silver nanowire mesh across the 1mm gap was found to be 652Ω. Fewer than four layers rendered the network incomplete and non-conductive.

7.3.3 Nanowire Conductivity Enhancement

Despite four layers of silver nanowire solution being conductive, it would be advantageous to further improve the electrical characteristics of the mesh. Reducing the resistance from 652Ω would be preferable over adding further nanowire layers, which would increase shading. From the literature, various schemes for improving the contact between silver nanowire junctions have been investigated. Two such techniques are compression [7] and thermal annealing [3]. Using compression to ensure that intersecting wires are electrically in contact with one another is not a suitable method for use with a solar cell substrate such as silicon. Commercially produced silicon solar cells are only around 180μm thick so any compression force could fracture the cell, with significant performance issues arising.

Thermal annealing of nanowires is more suitable for silicon photovoltaics, but repeatable annealing results are difficult to obtain due to the random deposition nature of the nanowires. In many cases, nanowires begin to fuse and simply break apart as shown in fig. 7.16.

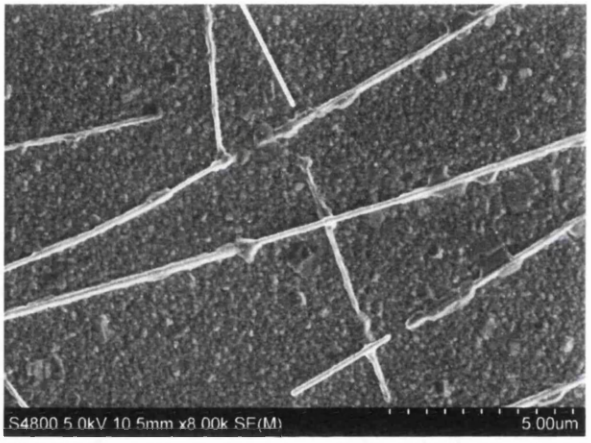


Figure 7.16: Silver nanowires annealed at 180°C for 10minutes

Difficulty with the annealing process has been encountered previously in the literature. Annealing for 60s in a N_2 environment at 400°C was found to be suitable [5]. Unfortunately such an annealing cycle adds complexity and cost to the process due to the requirement of a nitrogen environment and increased thermal budget.

Whilst performing electrical measurements on nanowire samples, an interesting discovery was made. From the conductivity trials previously described, re-measuring the samples yielded some very exciting observations. Once a sufficiently thick layer of nanowires had been deposited (creating a conducting mesh), performing further electrical measurements led to an improvement in conductivity.

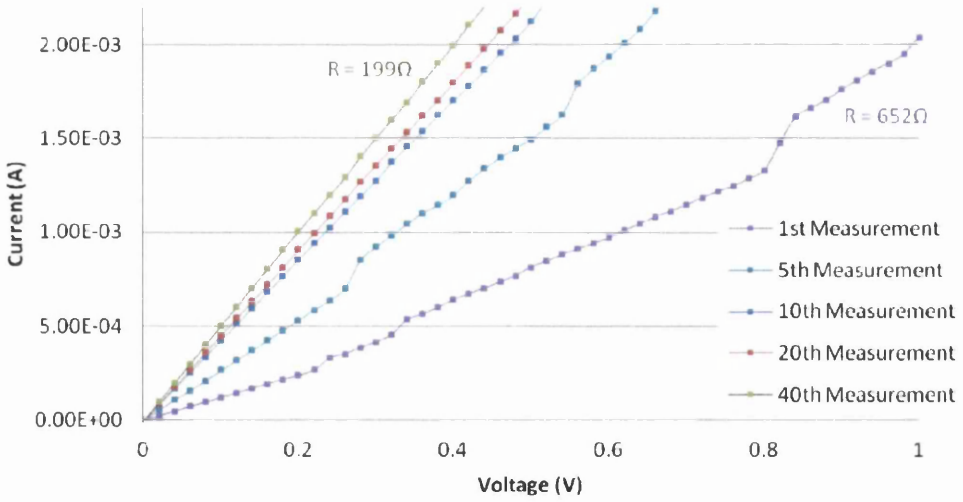


Figure 7.17: Repeated I-V measurements across 1mm gap decreased the electrical resistance of AgNW mesh (after 4 layers)

Such improvements are shown in fig.7.17 where the first measurement performed yielded an average resistance of 652Ω. Just ten measurements later the resistance had dropped to only 290Ω. After forty measurements (in total), the resistance reached its lowest value of just 199Ω. The result is that the resistance after forty measurements is almost four times lower than to begin with. It was also observed that any more measurements after the 40th no longer change the resistance significantly. Re-measuring the sample after several minutes still has no significant affect on the reduction of resistance indicating stability has been achieved in terms of electrical conductivity.

Such large decrease in resistance to a constant value suggests a permanent change has been made to the nanowire mesh. Imaging the intersection of individual nanowires before and after electrical measurements could yield important information.

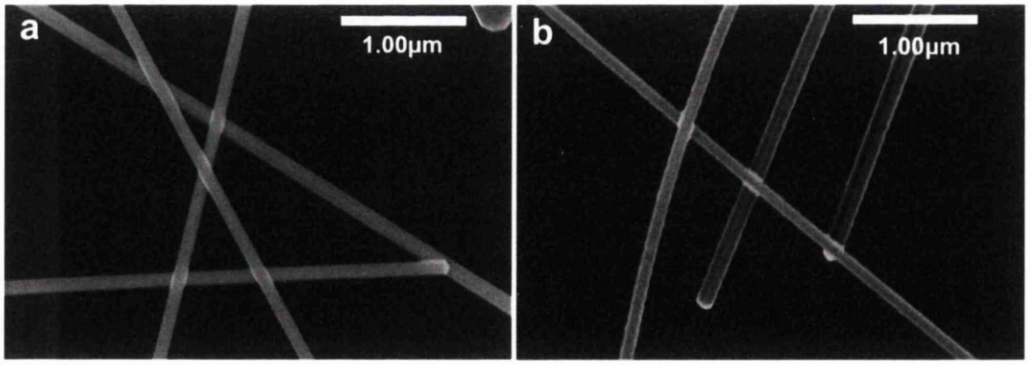


Figure 7.18 SEM images of nanowire junction: (a) Before electrical measurements (b) After 50 electrical measurements

From the SEM images, nanowires after repeated electrical measurements (fig.7.18b) look largely similar to nanowires that had not been measured (fig.7.18a). The only slight difference is the intersections of the nanowires. After multiple electrical measurements, the nanowires are clearly fused together at each point of intersection, whereas before any electrical measurement, the nanowires appear to simply overlay one another. It is therefore suggested that the nanowires that underwent multiple electrical measurements, are better electrically attached to one another (lower junction resistance of the fused intersections). Any further measurements no longer have effect because they are optimally attached. One hypothesis why the resistance falls during electrical measurement is due to the current passed along the wires that connect from one PCB contact to another. The current along such a small wire causes localised heating which in turn fuses it to the next wire in the mesh. The electrical annealing effect could remove the need for any additional treatments to reduce the resistivity of the mesh. As silicon solar cells generate current, it is anticipated that such an electrical annealing effect would be observed.

7.3.4 Optical Analysis

The transparency of a silver nanowire mesh for solar cell applications is critical, as if shading losses caused by the nanowire mesh become too large, any increase in electrical performance will be lost.

Nanowire layers were deposited onto glass sheets in order to measure the transmittance loss for varying densities of nanowires. The glass sheets were cut into $5cm^2$ pieces in order to simulate the size of a small scale silicon solar cell, which would ultimately be fabricated. As in previous experiments, a ratio of 1:10 AgNW solution to IPA was used. Each applied layer used 104μL of the prepared solution. The Iwata HP-AR airbrush was again used with nitrogen gas at a pressure of 1bar corresponding to a deposition rate of 97.8μL/s.

Glass samples sprayed with 4, 6 and 10 layers of the solution were measured using a spectrophotometer in order to assess the transmittance over the useable spectrum for silicon solar cells. A glass sample that had not been deposited with nanowires was measured as a reference.

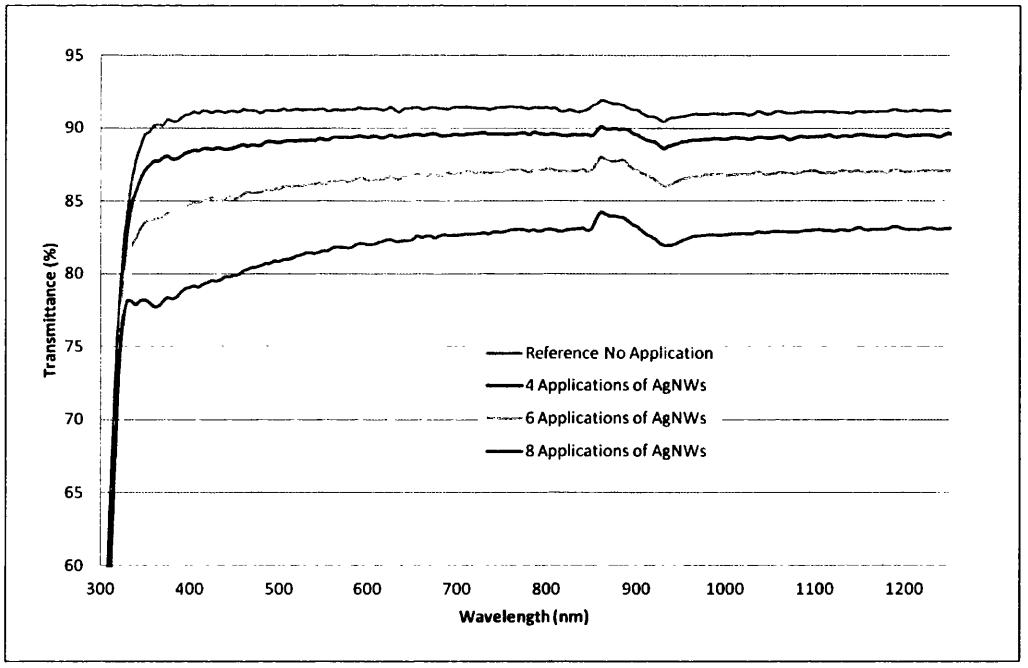


Figure 7.19: Transmittance of glass substrate after AgNW applications

From the spectrometer data of fig.7.19, it is observed that increasing the number of applications of the nanowire solution onto the glass decreased the transmittance. The reference sample had a transmittance from 400-1200nm of around 91%. After 4

applications of the nanowire solution (4x104μL), the transmittance fell to around 89%. 6 and 8 applications of the solution onto glass substrates resulted in a transmittance measurements of 87% and 83% respectively. Despite the 115nm diameters of the silver nanowires, as the density increases, more light is prevented from travelling through the sample. The enhancement of the electrical properties that silver nanowires can bring must be carefully balanced with the shading losses they inadvertently incur.

7.3.5 Full Textured Silicon Solar Cell Trials

After the coating and conductivity trials had been concluded, silver nanowires were ready to be applied to a fully operational silicon solar cell. It was previously found that 4 applications (4 x 104μL) of 1:10 nanowire/IPA solution was required for conduction to occur across the gap of a typical front contact gridline arrangement. Using the result, experiments were designed to produce 4 groups of nanowire deposited cells. Group one would receive 4 applications of the solution, group two → 6, group three → 8, and the forth group would receive 10 applications. The experiments would provide valuable data by observing the change in cell efficiency in relation to the amount of silver nanowire solution applied. For each group of samples, 3 textured solar cells were measured so that an average efficiency could be measured (improving result accuracy).

Several $5cm^2$ (300μm thick) textured silicon solar cells were fabricated ready for the nanowire applications. A full description of the solar cell fabrication process has been previously covered in Chapter 5. To avoid repetition, only the major production steps are highlighted below:

- Silicon wafer (200mm, 100 orientation) texturing using Potassium Hydroxide (KOH)
- Emitter junction 'doping' by thermally diffusing Phosphorylchlorid Phosphoryl Chloride.
- Backside wafer grinding
- Dicing of wafer into $5cm^2$ squares
- Front and rear electrical contact printing
- Firing of electrical contacts
- Tabbing of cell connections

Once the solar cells had been fabricated (fig.7.19), each cell was tested using a Newport Oriel Sol3A solar simulator. Measurements allowed for an efficiency to be recorded for each cell before the deposition of nanowires. Any change in efficiency after deposition would therefore be attributed to the nanowire coating. Four groups of three solar cells were measured. Table 7.1 lists the average efficiencies of each group of textured silicon solar cells before any nanowire deposition.

Sample Group Number	Average efficiency (%) before nanowire application
1	7.67
2	7.93
3	9.68
4	9.33

Table 7.1: Silicon Solar Cell Average Efficiencies before nanowire deposition

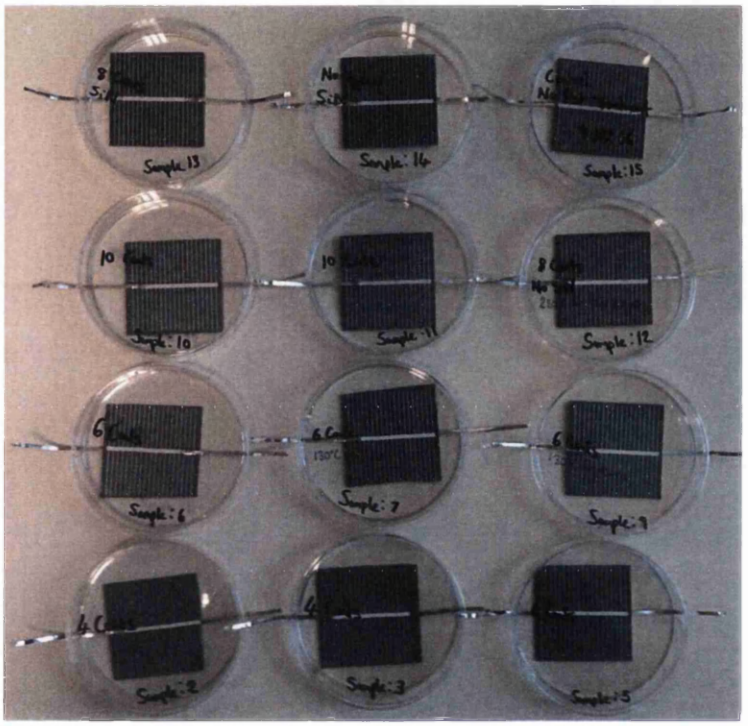


Figure 7.20: Fabricated textured silicon solar cells

Now that an efficiency baseline had been calculated for each solar cell, the silver nanowire solution could be spray coated onto the surface. As previously described, each group received different applications of the nanowire solution as listed in table 7.2.

Sample Group Number	Applications of nanowire solution received per cell	Amount of solution received per cell (µL)
1	4	416
2	6	624
3	8	832
4	10	1040

Table 7.2: Applications of nanowire solution received for each sample group

Following the application of the silver nanowires, each sample was re-measured using the solar simulator in order to observe the affect of the nanowires on efficiency (table 7.3).

Applications of nanowire solution	Average efficiency (%) before nanowire applications	Average efficiency (%) after nanowire applications
4	7.67	7.69
6	7.93	8.06
8	9.68	9.16
10	9.33	8.49

Table 7.3: Silicon solar cell average efficiencies before and after nanowire depositions

In order to assess the performance of the silver nanowire deposition process, the average efficiency results of cells before the deposition and after were compared. From fig.7.21 it is apparent that for 4 applications of the nanowire solution, the efficiency remained relatively unchanged with only a slight increase of 0.03%. The data suggests that the 4 nanowire depositions did not substantially increase the efficiency of the cell nor did it decrease it. Therefore the increase in current collection must be equal to that of the shading losses incurred by the nanowire mesh. For the cells that received six applications, a small efficiency gain of 0.13% was recorded. The efficiency gain implies that the increase in current collection by the nanowire mesh was greater than the shading losses incurred. For the cells that received eight applications, a large efficiency loss of 0.52% was recorded. The efficiency decrease suggests that the increase in shading by the nanowire mesh was larger than the enhancement of current collection. For cells receiving ten applications, a substantial efficiency loss of 0.84% was recorded. The efficiency decrease is attributed to the increase in shading by the nanowire mesh far outweighing the enhancement of current collection. It is important to note that despite each cell being measured several times in order for an average efficiency value to be obtained, significant changes in efficiency were not found indicating the absence of the electrical annealing affect. It is hypothesised that during I-V measurements of nanowires deposited between two contacts, current is forced along the mesh from one contact pad to another. Once a nanowire mesh is deposited onto an existing solar cell front contact structure, current is distributed throughout the gridline contacts as well as the nanowire mesh. This distribution prevents heating of the nanowire mesh which was attributed to the reduced resistance in the conductivity trials.

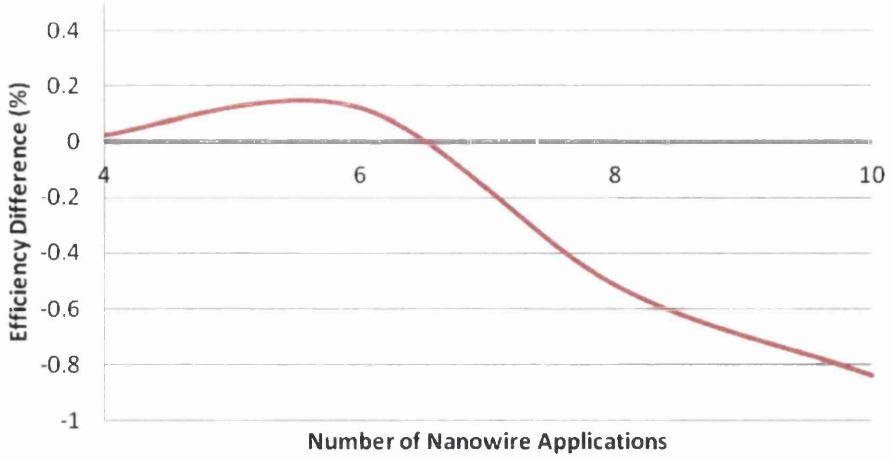


Figure 7.21: Solar cell efficiencies before and after nanowire depositions

From analysing the data obtained in fig.7.21 it is apparent that the amount of nanowires applied to the surface of a textured solar cell has a strong influence on the efficiency of the cell. Six nanowire applications (corresponding to a total solution volume of624μL) is the optimum amount of silver nanowires for efficiency enhancement to occur. Less than this amount has no affect on the cell efficiency, whilst any more starts to degrade cell performance. In fact depositing a volume of 1040μL of the nanowire/IPA solution degrades the cell performance from 9.33% to 8.49%

Even when the optimum amount of solution was sprayed onto the cells, the efficiency only increased from 7.93% to 8.06% (0.13% enhancement). To further understand why such as small efficiency gain was measured, SEM was performed on a textured silicon sample that had received 6 applications of the nanowire solution (fig.7.22).

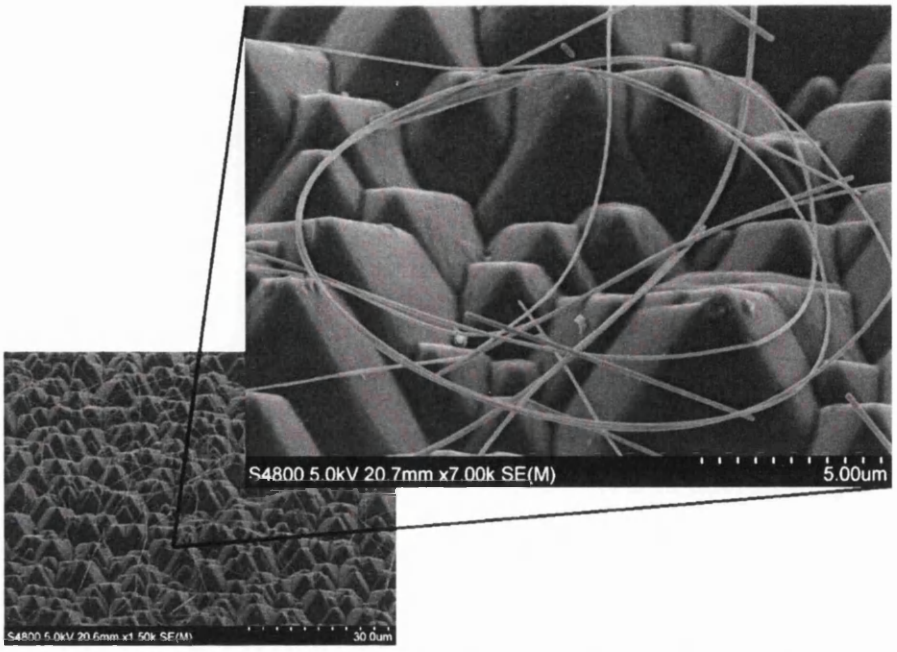


Figure 7.22: Textured silicon solar cell after 6 nanowire applications

From the SEM image it can be seen that the nanowires despite resting on the surface of the silicon have very little contact area with the silicon cell. The small contact area is due to the surface texturing of the silicon. As micro-pyramids have been etched into the silicon (as an anti-reflective treatment), when the nanowires are applied, they sit on the side or tips of the pyramids as shown in fig.7.23. As the nanowires are quite rigid they cannot contour to the pyramids. Only areas where the nanowires physically contact the silicon will collect electrons. The small efficiency gains measured for the cells are due to this small contact area between the silicon and silver nanowires. If the nanowires were able to contact the silicon over a greater area, current collection would be enhanced and therefore larger efficiency gains measured.

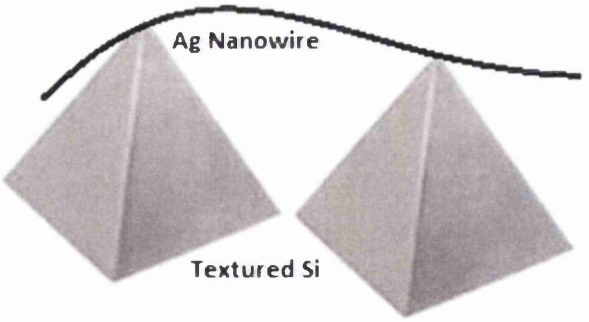


Figure 7.23: Illustration of nanowire contact points between textured silicon pyramids

7.3.6 Full Polished Silicon Solar Cell Trials

Analysing the behaviour of the nanowire interaction with a textured silicon surface led to the identification of contact area issues. Two ways to overcome such issues would be to either modify the nanowires to form around the silicon pyramids, or use a flatter silicon surface. To contour the nanowires around such an intricate shape as a pyramid would be very difficult due to the random textured surface of a silicon cell. A far easier method would be to use a polished flat silicon substrate.

To assess the effect of depositing silver nanowires onto a flat silicon surface, multiple polished silicon solar cells were fabricated. The experimental procedure was kept the same as that of the previous experiment (where textured cells were fabricated and AgNWs deposited on top of the cells). The only difference with the new work was that polished silicon (600µm thick) was used as the starting substrate (i.e. the KOH texturing step was omitted). Please see previous work above for experimental details.

Once the solar cells had been fabricated (fig.7.24), each was tested using a solar simulator. Four groups of three solar cells were measured. Table 7.4 lists the average efficiencies of each group of polished silicon solar cells before any nanowire deposition.

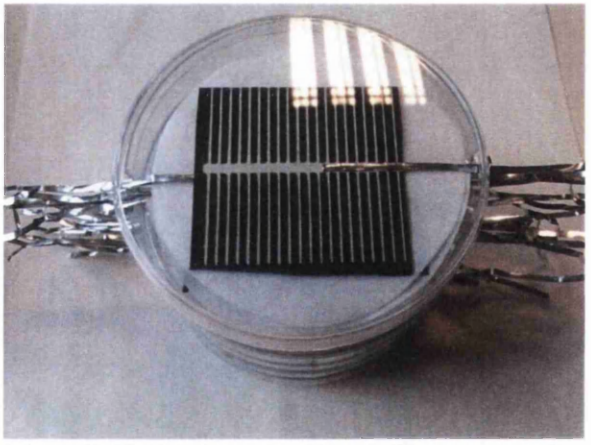


Figure 7.24: Fabricated polished silicon solar cells

Sample Group Number	Average efficiency (%) before nanowire application
1	3.34
2	2.98
3	3.22
4	3.77

Table 7.4: Silicon Solar Cell Average Efficiencies before nanowire deposition

Now that an efficiency baseline had been calculated for each solar cell, the silver nanowire solution could be spray coated onto the surface of the cells. As previously described, each group received different applications of the nanowire solution (table 7. 5)

Sample Group Number	Applications of nanowire solution received per cell	Amount of solution received per cell (µL)
1	4	416
2	6	624
3	8	832
4	10	1040

Table 7.5: Applications of nanowire solution received for each sample group

After nanowire deposition onto polished cells, it was noticed that a visual difference existed between the samples applied with different layers of the solution. From fig.7.26, the surface reflection of a cell applied with 4 layers and that of a cell applied with 10 is compared. A camera flash was used to exhibit the difference. The polished cell that received 4 applications (fig.7.25a) has a greater reflectivity than that of the cell applied with 10 layers of the solution (fig.7.25b). Such a change in apparent reflectivity relates well to the transmittance data obtained for the different applications previously described in the work. The more applications of the nanowire solution, the lower the transmittance became due to shading effects.

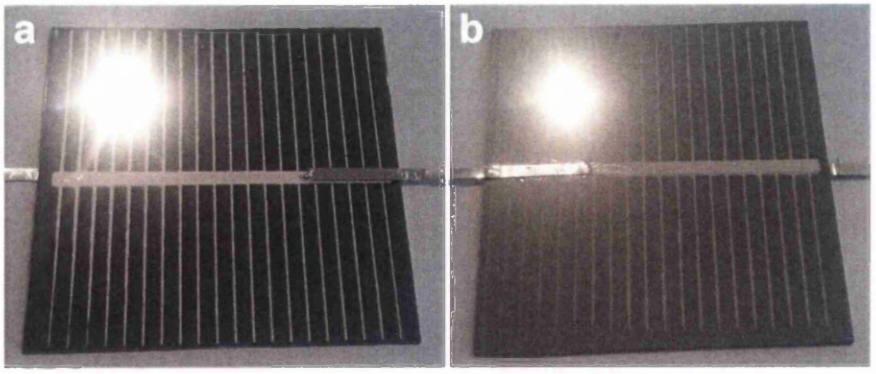


Figure 7.25 Polished silicon solar cells with (a) 4 AgNW Applications, (b) 10 AgNW Applications

Following the application of the silver nanowires, each sample was re-measured using the solar simulator (table 7.6).

Applications of nanowire solution	Average efficiency (%) before nanowire applications	Average efficiency (%) after nanowire applications
4	3.34	3.88
6	2.98	4.07
8	3.22	2.51
10	3.77	3.03

Table 7.6: Silicon solar cell average efficiencies before and after nanowire depositions

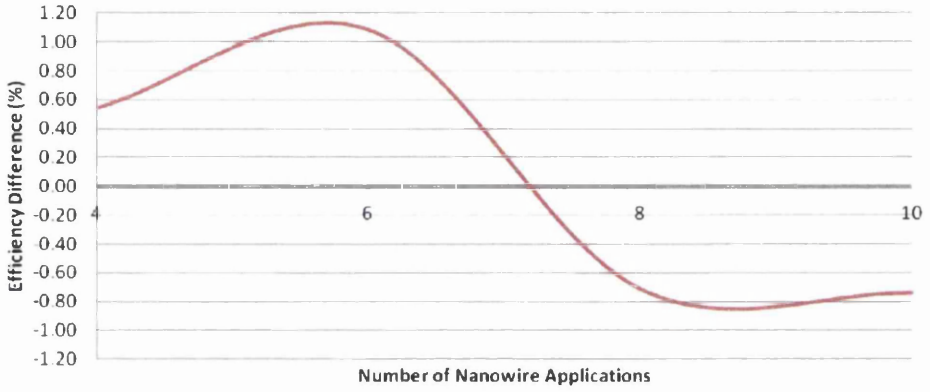


Figure 7.26: Polished silicon solar cell efficiency modification after nanowire depositions

In order to assess the performance of the silver nanowire deposition process, the average efficiency results of cells before the deposition and after were compared graphically (fig.7.26). From fig.7.26 an increase in efficiency was found with polished silicon cells that received 4 and 6 applications of the nanowire solution. Conversely cells applied with 8 and 10 applications saw a decrease in efficiency. With the cells that received 4 applications an average increase in efficiency of 0.54% was measured. Cells that had 6 applications had an average increase in efficiency of 1.09%. Cells deposited with 8 and 10 layers of the solution displayed average loss in efficiency of 0.71% and 0.74% respectively. The increase measured for cells with 4 and 6 applications, suggests that benefits of current collection outweighed shading effects. From analysing the electrical data obtained during efficiency measurements, the hypothesis of increased current collection could be reinforced. Comparing the electrical data in table 7.7 for a polished cell before and after application of 6 layers of nanowire solution yields some interesting discoveries.

	Voc V	Isc A	Jsc mA/cm2	Imax A	Vmax V
Before	0.53	0.44	17.56	0.24	0.28
After	0.52	0.52	20.51	0.33	0.35
Difference	*1% Decrease*	*17% Increase*	*17% Increase*	*34% Increase*	*26% Increase*
	Fill Factor	Efficiency	R at Voc	R at Isc	Power W
Before	28.82	2.68	0.93	1.92	0.13
After	42.03	4.52	0.35	2.43	0.19
Difference	*46% Increase*	*69% Increase*	*63% Decrease*	*27% Increase*	*43% Increase*

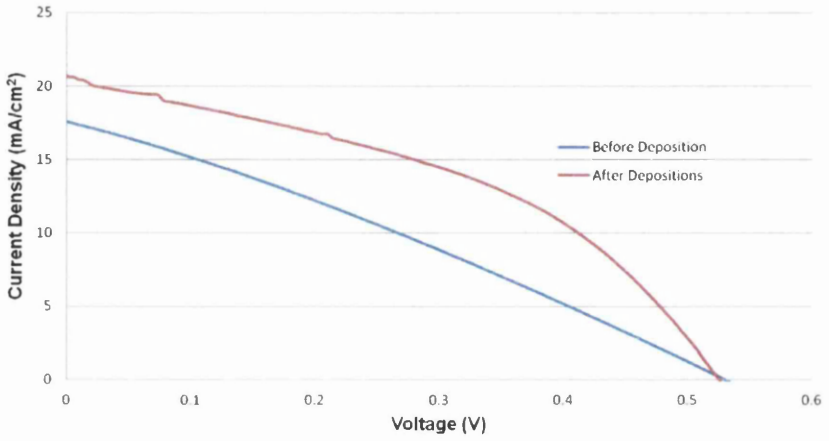


Table 7.7: Electrical efficiency measurement of polished cell with 6 nanowire applications

From the data, a significant increase of 46% in the fill factor was observed. Recalling the simplified equation for the fill factor of a solar cell:

$$FF = \frac{(I_{MP})(V_{MP})}{(I_{SC})(V_{OC})} \tag{7.1}$$

We can see that since the fill factor of the cell was dramatically increased, the product of $(I_{MP})(V_{MP})$ must have increased or the product of the $(I_{SC})(V_{OC})$ decreased. From the electrical measurements (table 7.7), it is apparent that the measured maximum current and voltage increased by 34% and 26% respectively. The fill factor of a solar cell is strongly affected by recombination and ohmic resistances. As the Voc of a cell is a good indication of the amount of recombination, a change of 1% as observed in the measurement of the cell ruled out any significant change in recombination. The other main contributions to the fill factor are ohmic losses. It is therefore suggested that a decrease in ohmic losses was the primary cause of the efficiency increases due the enhancement of contact area by the silver nanowire network. It is also worth noting that since a polished silicon substrate was used, it is also possible that the nanowires also reduced the reflectivity of the cell, although most of the enhancement is attributed to decreased ohmic losses. Work has previously been carried out on the literature of silver nanowires acting as such [8, 9]. The primary cause for

efficiency enhancement however is from series resistance reduction through the silver nanowire enhanced emitter contact.

The good increase in efficiency of the 4 and 6 layer nanowire cells also reinforces the hypothesis made earlier in the work that a polished flat substrate would enable the silver nanowire mesh to collect more carriers from the emitter surface than using a micro-textured surface. From previous trials conducted with cells fabricated on textured silicon, a relatively small efficiency increase of 0.03% and 0.13% was recorded for cells applied with 4 and 6 layers of solution respectively. The small efficiency increases were attributed to the small contact area between the nanowires and the textured silicon micro-pyramids on the surface of the cell. From the SEM image in fig.7.27 of silver nanowires applied to a polished silicon cell, it can be seen that the nanowires have a much larger contact area with the flat silicon substrate. The large increase in efficiency of the cells deposited with 4 and 6 layers of the solution is mainly attributed to the solar cell front contact enhancement.

For polished silicon cells applied with 8 and 10 layers an efficiency loss was measured. Such a loss suggests that the shading losses far outweighed the increase in current collection at the emitter of the cell. Any increase in current collection is then irrelevant due to the restriction of photons entering the cell caused by the nanowire applications. Once again the electrical measurements were analysed, this time for a polished silicon cell applied with 10 nanowire layers.

	Voc V	Isc A	Jsc mA/cm2	Imax A	Vmax V
Before	0.48	0.51	20.87	0.28	0.29
After	0.45	0.45	18.53	0.24	0.26
Difference	*6% Decrease*	*11% Decrease*	*11% Decrease*	*13% Decrease*	*10% Decrease*
	Fill Factor	Efficiency	R at Voc	R at Isc	Power W
Before	31.96	3.22	0.45	1.36	0.15
After	29.92	2.52	0.56	1.31	0.12
Difference	*6% Decrease*	*22% Decrease*	*24% Increase*	*4% Decrease*	*20% Decrease*

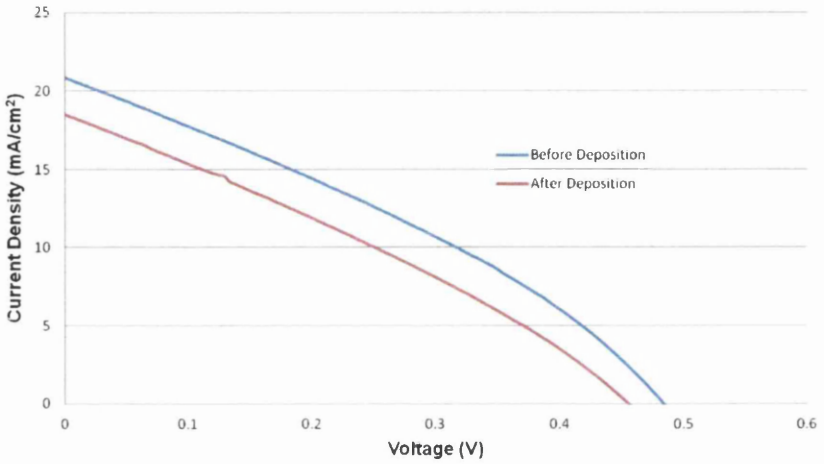


Table 7.8: Electrical efficiency measurement of polished cell with 10 nanowire applications

From the data it is observed that the Voc and FF both reduced by 6% after nanowire application. As the silver nanowires were applied to existing screen printed gridline top contacts, the resistive loss of the contact would not be increased by the addition of a conductive mesh. The Isc of the cell fell by 11% which suggested that photons of were being restricted from entering the cell. The restriction of photons is due to the shading effect by the nanowire contact.

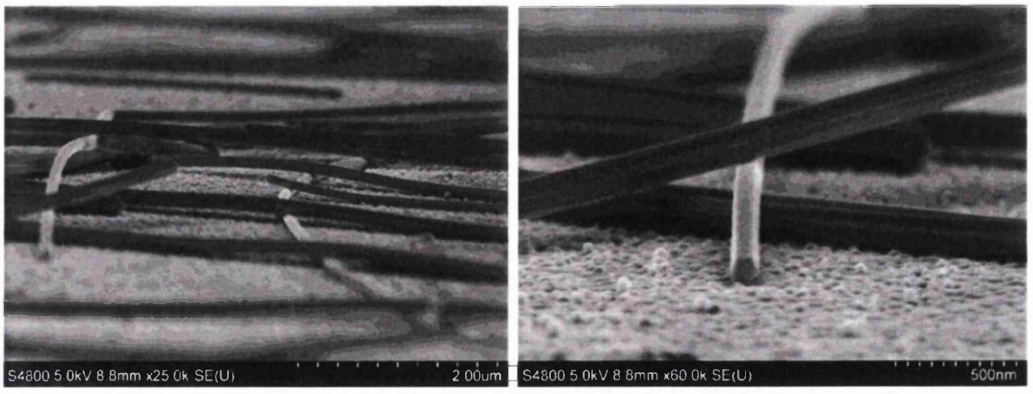


Figure 7.27: Silver nanowires on surface of polished silicon solar cell

During the efficiency measurements of the polished silicon solar cells, some cells exhibited irregular electrical values affecting the efficiency of the cells. Cells that followed the same trend were analysed and compared to the cells exhibiting spurious results. It is important to note that the cells exhibiting irregular results were by far in the minority, but further investigation and understanding was performed on these cells.

As a control, one of each of the different nanowire application cells that exhibited consistent measurements were imaged (fig.7.28).

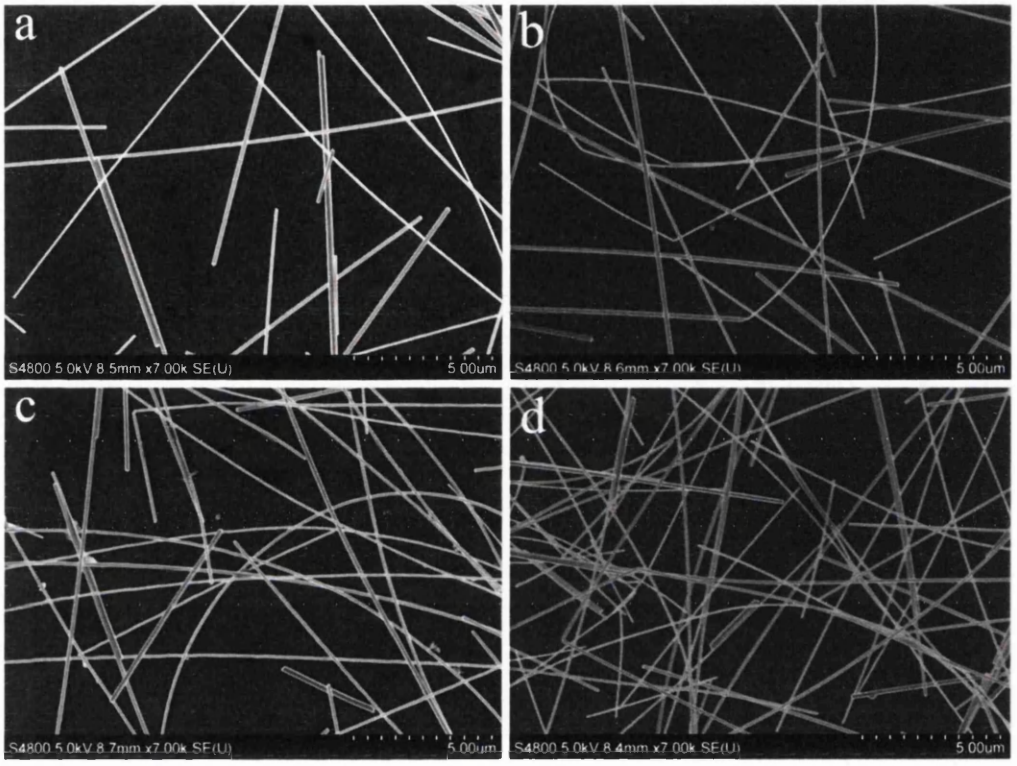


Figure 7.28: SEM image of polished cells with a) 4 nanowire applications, b) 6 nanowire applications, c) 8 nanowire applications and d) 10 nanowire applications

Fig.7.28 validates that the density of nanowires increases with the number of applications. Taking the image of fig.7.28a (surface of a 4 application polished cell) and comparing it to that of the surface of one which received 6 applications (fig.7.28b), the amount/density of nanowires slightly increases. The trend continues when comparing the 6 application cell to the 8 and so forth. The increase in density between the samples indicates that a uniform spray deposition has been achieved.

Now a control image had been established, a polished cell spray coated with 6 nanowire applications that exhibited a loss in efficiency was analysed. Other cells deposited in the same manner exhibited an increase so understanding why the cell exhibited such different behaviour was of interest.

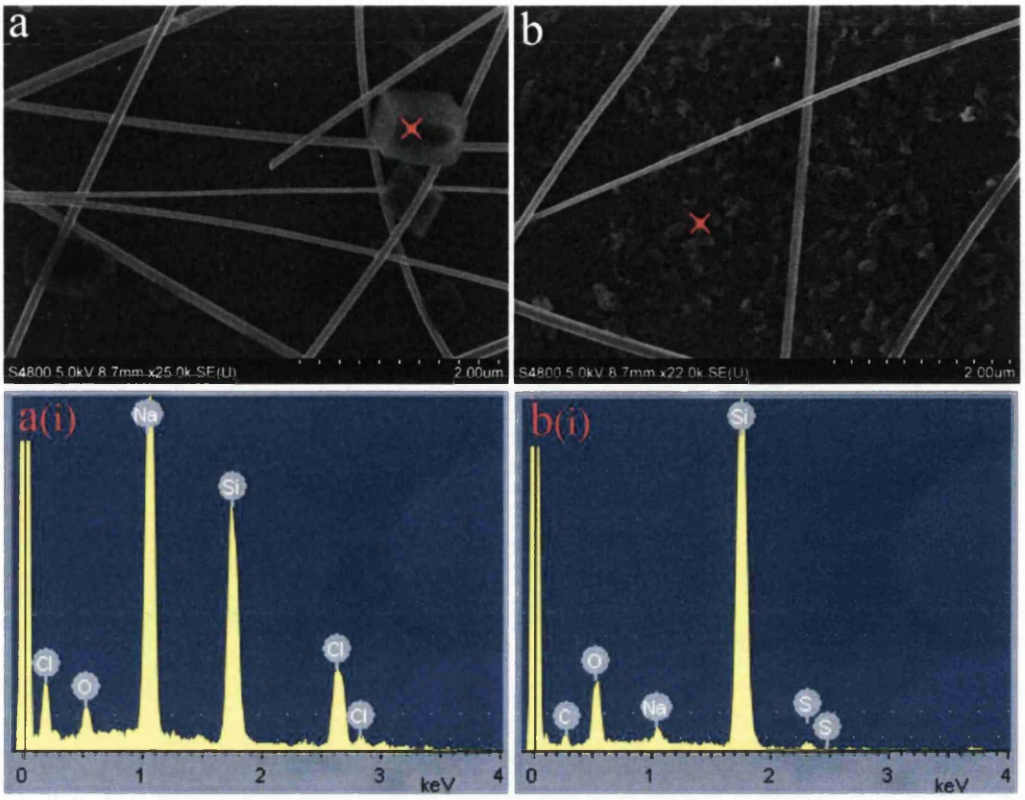


Figure 7.29: SEM and EDX analysis of irregular polished cell with 6 nanowire applications

SEM imaging conducted on the sample revealed two distinct features which were not observed on the surface of other cells. The two irregular features are depicted in fig.7.29a/b. The first interesting observation was of cube type structures amongst the silver nanowires. Some of the structures were as large as 1µm in width and were situated across the surface of the cell. Such structures due to their relatively large nature could significantly increase the shading of the cell. To better understand what the structures were composed of, Energy Dispersive X-ray (EDX) spectroscopy was performed on one of the features. The technique provided elemental composition data about the feature (fig.7.29ai). From the data obtained from EDX spectroscopy, it was suggested that the feature possibly contained sodium and chlorine i.e. sodium chloride. Other particle contaminants observed on fig.7.29b were analysed using EDX spectroscopy and also revealed the presence of sodium and also sulphur.

Sodium chloride is typically used to assist in the synthesis of silver nanowires [10], but usually the after synthesis the silver nanowires are separated from the solution by a centrifuge. It is apparent in the case of the spectroscopy data above that some of the

sodium chloride made it through into the final nanowire solution. A reason why only one sample showed the containment and no others were that the solution sprayed onto the sample was at the bottom of the container. Despite vigorous shaking (as recommended by the manufacturer) because the solution quantity was running low (less that 2mL left of the concentrated AgNW solution) the sodium chloride was concentrated within the remaining solution. The presence of sulphur as indicated by fig.7.29b(i) is related to silver sulphide. From the literature [11] silver nanostructures are prone to corrosion once outside the solution, where a layer of silver sulphide nanocrystals can form around the nanowires. As explained above, since the solution used for the sample was the residual contents of the container, it is quite possible that residual nanowires on the container walls were mixed in when shaking it. As the nanowires on the container wall had been exposed to atmosphere, corrosion could have occurred explaining the presence of sulphur detected using EDX.

7.4 Summary

A silver nanowire mesh was chosen to investigate the effects upon cell performance. Due to their nanoscale diameters, silver nanowires yield both a conductive and transparent mesh. Such properties make them ideal candidates for contact enhancement where shading losses are as important as the electrical contact improvement itself. Experiments were carried out on the deposition of nanowires as well as the conductivity and optical properties of the nanowire mesh. SEM, photospectrometer and I-V equipment was used to characterise the mesh.

The ultimate aim of the chapter was to observe the effect of a silver nanowire mesh deposited on the surface of standard monocrystalline silicon solar cell. Rod and spray coating deposition methods were analysed for the suitability of applying a nanowire mesh onto such a device. Consideration of the surface topography of the raised front contact of a solar cell identified spray coating as the most suitable deposition technique.

Once a suitable deposition method had been found, conductivity trials were carried out to determine the minimum quantity of nanowire solution required for a conducting mesh to be formed across a standard silicon solar cell front contact. Experimentation found that 4 applications or 416µL of silver nanowire solution was found to create a conducting mesh across a 1mm spaced contact. Whilst performing I-V measurements of the nanowire mesh, an electrical annealing effect was observed. Repeated measurements of the nanowires led to a resistance decrease from 652 to 199Ω.

Spray depositions of different quantities of silver nanowire solution were applied to textured and polished silicon solar cells processed using standard conditions. For textured silicon solar cells applied with 624µL of solution, an efficiency increase from 7.93% to 8.06% (0.13% increase) was observed. For quantities of solution below 624µL little change in efficiency was observed. Samples processed with more than 624µL led to reduced efficiency. For polished silicon solar cells deposited with the nanowire solution, a largely similar pattern was observed. The optimum quantity of solution was once again found to be 624µL, this time leading to a substantial increase in efficiency from 2.98 to 4.07% (1.09% increase). As with the textured cells, samples processed with more than 624µL led to reduced efficiency. Differences in the efficiency enhancement between textured and polished cells deposited with the same amount of silver nanowire solution were attributed to the contact area between the NWs and the silicon at the surface of the cell. A polished flat substrate enables the silver nanowire mesh to collect more carriers from the emitter

surface than using a textured surface, where nanowires only contact at specific points along the micro-textured pyramids.

Unfortunately polished silicon solar cells reflect a large amount of light which seriously affects their efficiency performance. By using a PSi anti reflective layer previously developed in this work, the reflectivity of such a cell could be dramatically reduced. Due to the nanoscale topography of a PSi layer, it is envisaged that such a surface would be ideally suited for nanowire deposition due to its relative flatness. It is also important to note that during repeated efficiency measurements of silver nanowire textured and polished cells, the electrical annealing effect that was discovered during previous deposition trials was not observed during cell measurements. It is hypothesised that during I-V measurements of nanowires deposited between two contacts, current is forced along the mesh from one contact pad to another. Once a nanowire mesh is deposited onto an existing solar cell front contact structure, current is distributed throughout the gridline contacts as well as the nanowire mesh. This distribution prevents heating of the nanowire mesh which was attributed to the reduced resistance in the conductivity trials. In conclusion the work demonstrated that a silver nanowire mesh has the capability to enhance standard solar cell front contacts on both textured and polished silicon substrates. Silicon solar cells processed from polished flat substrates could see their efficiency improved by as much as 37% by applying a silver nanowire mesh.

[1] Eidelloth, S.; Heinemeyer, F.; Münster, D.; Brendel, R., "Aluminum Evaporation and Etching for the Front-Side Metallization of Solar Cells," Photovoltaics, IEEE Journal of , vol.3, no.2, pp.702,708, April 2013

[2] Kim, DH.; Lee, SH., "Investigation on plated Ni/Cu contact for mono-crystalline silicon solar cells" Electronic Materials Letters, Vol 9, Issue 5, pp 677-681, September 2013

[3] Madaria, AR. *et al*, "Large scale, highly conductive and patterned transparent films of silver nanowires on arbitrary substrates and their application in touch screens" Nanotechnology, Vol 22, Number 24, 2011

[4] Hu L, Kim HS, Lee JY, Peumans P, Cui Y, "Scalable coating and properties of transparent, flexible, silver nanowire electrodes". *ACS Nano* , Vol 4, Number 5, pp 2955–2963, 2010

[5] S. Xie, Z. Ouyang, B. Jia, and M. Gu, "Large-size, high-uniformity, random silver nanowire networks as transparent electrodes for crystalline silicon wafer solar cells," Opt. Express, Vol 21, A355-A362, 2013

[6] Gao, Jinwei; Pei, Ke; Sun, Tianyi; Wang, Yaohui; Zhang, Linghai; Peng, Weijin; Lin, Qinggeng; Giersig, Michael; Kempa, Krzysztof; Ren, Zhifeng; Wang, Yang, Transparent Nanowire Network Electrode for Textured Semiconductors, Small, vol. 9, issue 5, p. 733-737, 2013.

[7] Takehiro Tokuno, Masaya Nogi, Makoto Karakawa, Jinting Jiu, Thi Thi Nge, Yoshio Aso, and Katsuaki Suganuma, "Fabrication of silver nanowire transparent electrodes at room temperature," *Nano Research.* 2011.

[8] Ting Xu ; Myung-Gyu Kang ; Hui-Joon Park ; L. Jay Guo; Enhanced efficiency of organic solar cells with silver nanowire electrodes. Proc. SPIE 7933, Physics and Simulation of Optoelectronic Devices XIX, 793329, 2011

[9] Liu CH, Yu X. Silver nanowire-based transparent, flexible, and conductive thin film. Nanoscale Res Lett, 8, 1–8, 2011

[10] Zhong Chun Li; Tong Ming Shang; Quan Fa Zhou; Ke Feng, "Sodium chloride assisted synthesis of silver nanowires," Micro & Nano Letters, IET, vol.6, no.2, pp.90,93, 2011

[11] Jose Luis Elechiguerra, Leticia Larios-Lopez, Cui Liu, Domingo Garcia-Gutierrez, Alejandra Camacho-Bragado, Miguel Jose Yacaman, Corrosion at the Nanoscale: The Case of Silver Nanowires and Nanoparticles, Chemistry of Materials 17 (24), 6042-6052, 2005

Chapter 8: Conclusion

The main objective of this work has been related to both reducing the cost of silicon wafer solar cells and improving the efficiency of such PV devices, using techniques applicable to commercial cell production. Cost reductions were investigated by the use of thinner silicon cell substrates thereby reducing material usage. Efficiency improvements were studied in the form of front contact enhancements whilst taking into account for the extra cost associated with additional processing. From experimentation into thin silicon wafer substrates, conventional front surface anti-reflective suppression techniques were found to potentially cause issues when using a substrate only tens of microns thick. An alternative anti reflective process was studied, suitable for both thick and thin wafer based substrates. Such a process was later deemed suitable for enhanced contact use by conclusions obtained from contact enhancement trials.

A review was conducted in each area of which subsequent experimentation was performed. The three areas studied in depth were related to thin wafer based substrates, reduction of optical losses through anti-reflective processes, and solar cell electrical contact metallisation. The production of thin wafer based silicon substrates was found to be limited by using commercially adopted wire sawing processes. Such equipment was also found to have large material loss during wafering often referred to as kerf loss. Various techniques and processes that were able to produce thin silicon wafers have been evaluated in terms of suitability for photovoltaic use, where cost is a major factor. Most techniques involved layer transfer processes where silicon was grown onto a substrate and subsequently removed. The cost implication of growing materials and then removing them from the substrate is too high for low cost photovoltaic applications. A silicon exfoliation technique using a metallic layer was found to be suitable for thin silicon substrate production. The technique was originally developed by IMEC although a limited number of publications had been focused around the process, leaving many unknowns.

Theoretical understanding and reviews into anti reflectivity suppression techniques for silicon solar cells, uncovered an extensive research area. Conventional cells adopting a textured surface, onto which a separate anti reflective coating was applied, were found to suppress reflectivity very well although room for improvement was apparent. Techniques involving nanoscale structures were found to be very popular and efficient at suppressing the reflectivity of a cell even further. One nanoscale texturing process, namely the formation of porous silicon, was found to be able to create nanopores in the silicon surface which offered excellent light trapping ability.

The final review of front contact metallisation techniques to allow as much light as possible in, whilst allowing for carriers to be collected by the electrical contacts, looked at different metallisation method. The use of conventional screen printing was found to be the main limiting factor in the producing of fine gridline top contact structures. Various other deposition techniques, as well as different metallic materials, have been put forward as replacements for screen printing of silver. Electroplating of copper and nickel were found to be promising technologies, but require more complex processes to pattern and plate the contacts. The application of silver nanowires was found to provide good electrical contacts on thin film solar cells and touch screen devices. Their use for wafer based silicon solar cells was extremely limited and just one publication on the use of nanowires for such an application was found.

Silicon exfoliation has been used in order to produce ultra-thin silicon substrates for photovoltaic applications. Such substrates have excellent potential for reducing material consumption and therefore cost. Experimentation was carried out on various parameters relating to firing temperature, contact thickness, printing methods, substrate type, and ink compositions. Scanning electron microscopy (SEM) and white light interferometry were used to analyse samples. The process involved coating a textured silicon wafer with a silver paste (more than 46μm thick), then heating at 980°C followed by rapid cooling. This caused a thermo mechanical stress capable of cleaving a Ag/Si layer (40μm) from the substrate. A critical parameter for reliable exfoliation was found to be the firing temperature of the contact. A period of 25 seconds at 980°C was found to be suitable for exfoliation. Despite testing a range of metallic pastes suitable for silicon solar cell production, only one paste (DuPont Solamet Silver PV149) was found to work successfully. A sufficiently thick metallic layer was required to provide enough mechanical force for exfoliation to occur. This related to a minimum contact height (after firing) of 46μm. Textured silicon substrates normally used for silicon solar cell fabrication were found to be essential for effective exfoliation. The micro pyramid texturing on the surface of the substrates, allowed for excellent adhesion of the metallic contact during expansion and contraction from the firing cycle. The extensive trials allowed for repeatable, large area, exfoliation to occur, producing ultra thin silicon foils. A novel processing structure was formulated to convert the silicon foils into fully operational solar cells. Initial cells measured around 1% efficient, but it is envisaged that great efficiency gains could be achieved with better electrical contacts, ARCs, and optimisation of the techniques. The silicon exfoliation

process developed was successfully tested in a commercial silicon solar cell manufacturing facility, however handling of delicate foils presents challenges.

Porous silicon has been developed as a viable alternative to conventional texturing and ARC coatings. From previous work, it was found that the exfoliation of silicon disrupts the surface structure of the silicon substrate. Such disruption could have an effect on conventional alkaline etching used to produce textured silicon pyramids. PSi was identified as an alternative anti-reflective structure which uses acid based etching mechanisms which are not orientation dependent. Experiments into the formation of porous silicon via metal assisted etching (MAE) were implemented. Sputtering equipment was used to deposit silver nanoparticles onto polished reclaimed silicon substrates. Subsequent etching underneath the particles resulted in pore creation. From deposition and subsequent etching of a series of interconnected silver particles with average diameters of around 30nm, a very low reflectivity of 6.68% was achieved. Such a reflectivity was not only lower than standard KOH textured substrates, but also lower than the commercially used textured Si incorporating an additional SiN ARC layer. Since the PSi had such excellent anti-reflective properties, it could potentially replace not only the texturing process but also the additional ARC coating. Therefore solar cell reflectivity suppression could be achieved in a single step. However, silver deposition using sputtering equipment is a costly step and alternative low cost methods of PSi formation were investigated. Substrate conformal imprint lithography was assessed as such a technique. Unfortunately due to the high aspect ratio of the PSi surface, issues were encountered during stamp replication. Strong adhesion between the stamp and substrate prevented separation. Another potentially low cost method for PSi production was electrochemical etching. A special chamber was constructed in order to trial the process. From initial experiments it was found that PSi could be successfully produced using a simple HF electrochemical etch. It is therefore suggested that the electrochemical etching setup could potentially be adopted by industry for anti-reflective PSi formation. Although this chapter dealt mainly with porous silicon structures, an enhanced ARC was also investigated as. ZnO nanowires were used to reduce reflectivity of a commercially adopted nitride ARC process even further. By using ZnO nanowires grown on textured Si substrates and depositing a SiN ARC on top, reflectivity was found to decrease even further to 6.12%. The process of growing the nanowires used a rapid microwave growth technique. Full silicon solar cells manufactured using the process exhibited an efficiency improvement of 1.02% over conventionally produced textured silicon solar cells with just a standard SiN ARC.

The final aspect of this work focused around the enhancement of existing silicon solar cell front contacts. A silver nanowire mesh was chosen to investigate the effects upon cell performance. Experiments were carried out on the deposition of nanowires as well as the conductivity and optical properties of the nanowire mesh. SEM, spectrophotometer and I-V equipment was used to characterise the mesh. Rod and spray coating deposition methods were analysed for the suitability of applying a nanowire mesh onto such a device. The surface topography of the raised front contact of a solar cell identified spray coating as the most suitable deposition technique. Conductivity trials determined the minimum quantity of nanowire solution required for a conducting mesh to be formed across a standard silicon solar cell front contact. 4 applications or 416µL of silver nanowire solution was found to create a conducting mesh across a 1mm spaced contact. Whilst performing I-V measurements of the nanowire mesh, an electrical annealing effect was observed. Repeated measurements of the nanowires led to a resistance decrease from 652 to 199Ω. Spray depositions of different quantities of silver nanowire solution were applied to textured and polished silicon solar cells processed using standard conditions. For textured silicon solar cells applied with 624µL of solution, an efficiency increase from 7.93% to 7.06% (0.13% increase) was observed. For quantities of solution below 624µL, little change in efficiency was observed. Samples processed with more than 624µL led to reduced efficiencies. For polished silicon solar cells deposited with the nanowire solution, a largely similar pattern was observed. The optimum quantity of solution was once again found to be 624µL, this time leading to a more substantial increase in efficiency from 2.98 to 4.07% (1.09% increase). As with the textured cells, samples processed with more than 624µL led to reduced efficiency. Differences in the efficiency enhancement between textured and polished cells deposited with the same amount of silver nanowire solution were attributed to the contact area between the NWs and the silicon at the surface of the cell. Unfortunately polished silicon solar cells reflect a large amount of light which seriously affects their efficiency performance. By using a PSi anti reflective layer previously developed in this work, the reflectivity of such a cell could be dramatically reduced. Due to the nanoscale topography of a PSi layer, it is envisaged that such a surface would be ideally suited for nanowire deposition due to its relative flatness. It is also important to note that during repeated efficiency measurements of silver nanowire textured and polished cells, the electrical annealing effect that was discovered during previous deposition trials was not observed during cell measurements. In conclusion the work demonstrated that a silver nanowire mesh has the capability to enhance standard solar cell front contacts on both

textured and polished silicon substrates. Silicon solar cells processed from polished flat substrates could see their overall efficiency improved by as much as 37% by applying a silver nanowire mesh.

Publications

Conference Publications

- Yufei Liu; **Blayney, G.J.**; Guy, O.J., "Rapid microwave growth of ZnO nanowires for low cost photovoltaics cells using reclaimed silicon substrates,", *2012 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)*, pp.1-3, Dec 2012
- **G.J. Blayney**, C. Zaradzki, Y. Liu, M.A. Mohd-Azmi, O.J. Guy, Anti-reflective porous silicon features by substrate conformal imprint lithography for silicon photovoltaic applications, Proceedings of HeteroSiC-WASMPE 13, June 2013

Conference Papers

- **Gareth J Blayney**, Yufei Liu, Owen J Guy, Analysis of Reclaimed Crystalline Silicon Substrates for the Production of Thin-Foil Solar Cells, *Photovoltaic Science Applications and Technology (PVSAT) 9*, 2012. Proceedings available at http://www.pvsat.org.uk/PVSAT-9_Proceedings-FINAL.pdf [last accessed 30/12/13]

Patents

- Yufei Liu, Owen J Guy and **Gareth J Blayney**, A novel Rapid Microwave Growth of ZnO Nanowires for Low Cost Photovoltaics solar Cells, UK Patent (application reference: GB1222023.2)

Appendix A

Lightweight composite panels

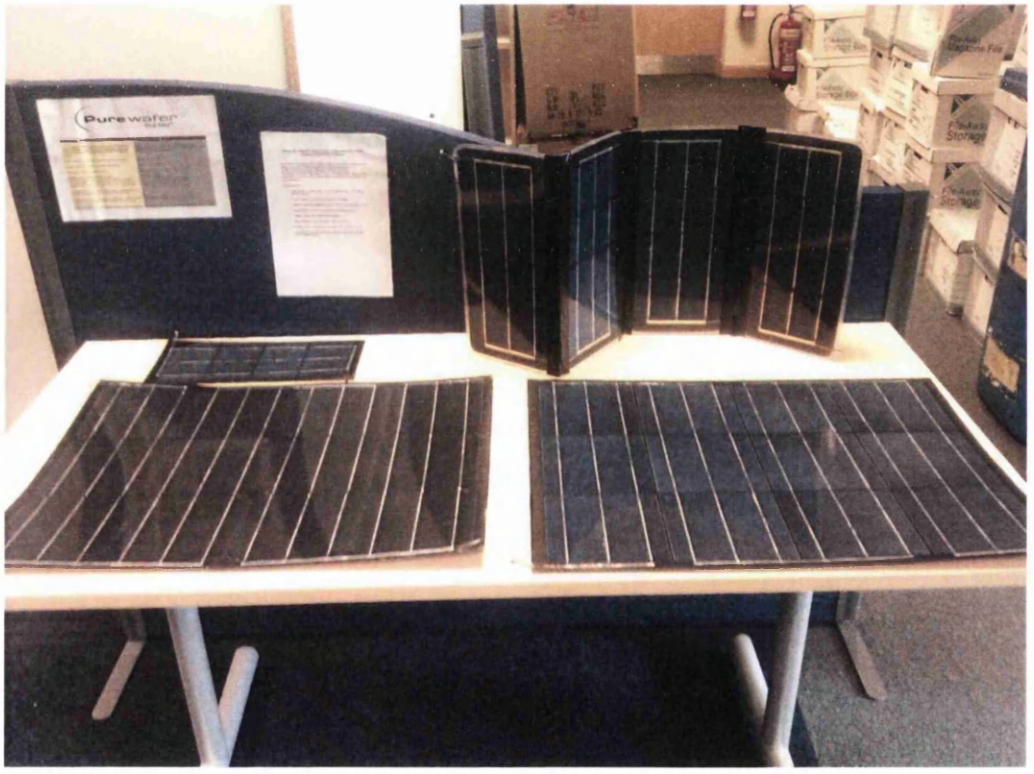
The requirement for lightweight yet durable portable photovoltaic panels has continued to increase with our ever increasing reliance on portable technology. An excellent demonstration of this is mobile phone technology. Over the last decade they have evolved into smart phones incorporating several advanced features such as GPS and internet. All these features have quite substantial power requirements compared to mobile phones from several years ago. Device designers want phones and other electrical portable devices to be sleek and stylish, with non intrusive batteries. As dependency on these devices has increased, running out of battery power can be of great concern. Portable solar charging equipment although still in its relative infancy has started to boom.

Current mainstream manufactured portable PV panels are typically constructed from several thin film photovoltaic cells laminated together. Simple power regulation circuitry is also adopted to create a lightweight charging device that can be folded up and placed inside a rucksack etc. Manufacturers have also produced rucksacks with integrated solar panels and there has recently been a drive for clothing that incorporates the same principles. Thin film portable solar panels are suitable for small devices such as a mobile phone with most thin film portable panels capable of around 500mA at 5V.

For larger portable electronic equipment such as laptops, thin film solar panels struggle to provide the required charging capability, whilst remaining lightweight, compact and of relatively low cost. Silicon photovoltaics are ideally suited to satisfy the requirements for larger portable electronic devices. Silicon solar cells offer lightweight, excellent electrical performance at low cost. The biggest drawback of using portable panels constructed from silicon is that silicon is inherently very brittle. In commercial solar panel construction, silicon solar cells are laminated to a relatively thick sheet of glass (around 4mm) to provide the stability and protection they require. Such panels are usually fixed into place, be it on a roof or a ground mounted array and typically weigh around 25kg each. Such a heavy and cumbersome silicon panel is not suited for portable power applications.

The use of carbon fibre as a rigid support structure for standard silicon solar cells was investigated. Carbon fibre sheets pre-impregnated with resin were purchased and experiments performed to analyse how the material could be effectively used to prevent damage to the brittle silicon solar cells. A heated vacuum press (used for solar panel manufacturing) was found to be a very good tool for curing the pre-impregnated carbon.

By varying the thickness of carbon fibre layers the rigidity of the cured sheet could be controlled. For the application of small portable silicon solar cell cells, the carbon fibre support structure was required to be as rigid as possible to protect the wafers. Unfortunately carbon fibre is a relatively expensive material so finding the minimum carbon fibre thickness suitable for the application was investigated. From the experiment an optimal cured layer was found to be around 2-3 layers of a 215g density woven mesh. The rigidity required by the supporting sheet ultimately depends upon the environment to which the panel would be subject to. A general purpose panel used during hiking etc was estimated to require only 3 layers of carbon fibre. For more challenging environments (military use), the panel would require a more substantial rigid support structure of 4-5 layers. The picture below showcases some of our early development carbon fibre support silicon modules. Some modules were connected in an array allowing the panel to be stacked neatly into a self contained power pack.



Appendix B

PV Battery Storage System

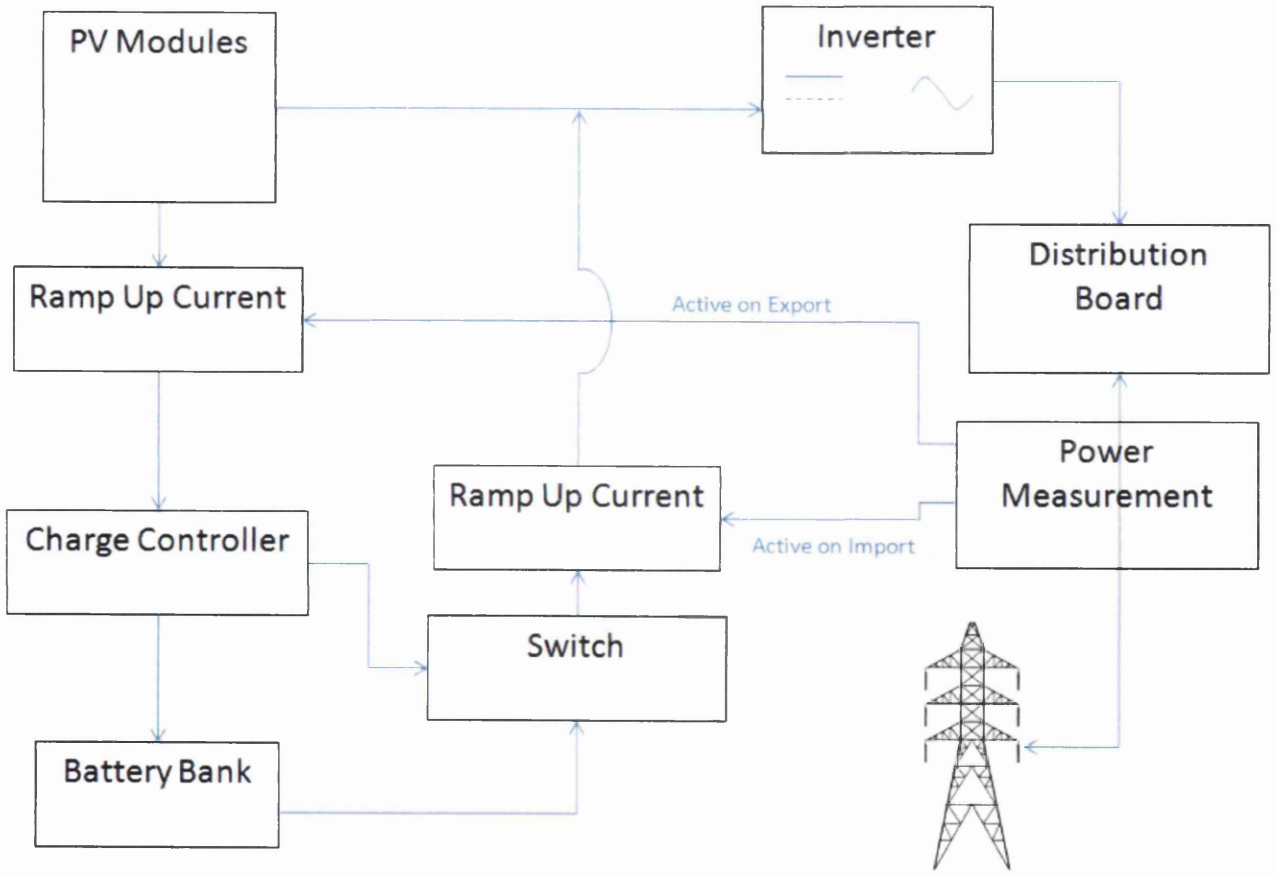
Over the last decade, the exponential growth of photovoltaic installations has paved the way for worldwide governments to get closer to meeting renewable generation pledges. Unfortunately over the last few years, the vast number of installs has started to put stress on the current grid networks. Taking the United Kingdom as an example, the grid network was essentially built as a one way system to transfer electricity from a power station to the end users. Grid management systems were designed around this idea. These days however, even a typical domestic solar installation of 4kW/h is effectively a miniaturised power station. The grid has therefore been heavily modified with the addition of thousands of these mini power stations. Many of which are often situated in close proximity to one another. The issue that the grid management companies have is that these solar installations provide electrical output during daytime hours, which is generally when grid consumption is at its lowest. In the UK for domestic systems, the Feed in Tariff assumes that you export 50% of the available power from a solar installation back into the grid. During evening hours when there is a large demand for electricity, solar installations provide little or no power. In these hours, conventional power stations are required to meet our demands. The need to store electrical energy is therefore essential if photovoltaic energy is to continue to see such a growth and challenge the large fossil fuelled power stations.

A system which could be fitted to a photovoltaic installation to enable battery storage would be very beneficial. Instead of installations exporting excess electricity into the grid, it could be used to charge a bank of batteries instead. During daytime hours, a PV installation could not only provide power for any domestic loads, but if there is excess electricity produced it would store this in batteries. The stored energy could then be used in the evening when the installation is not operational.

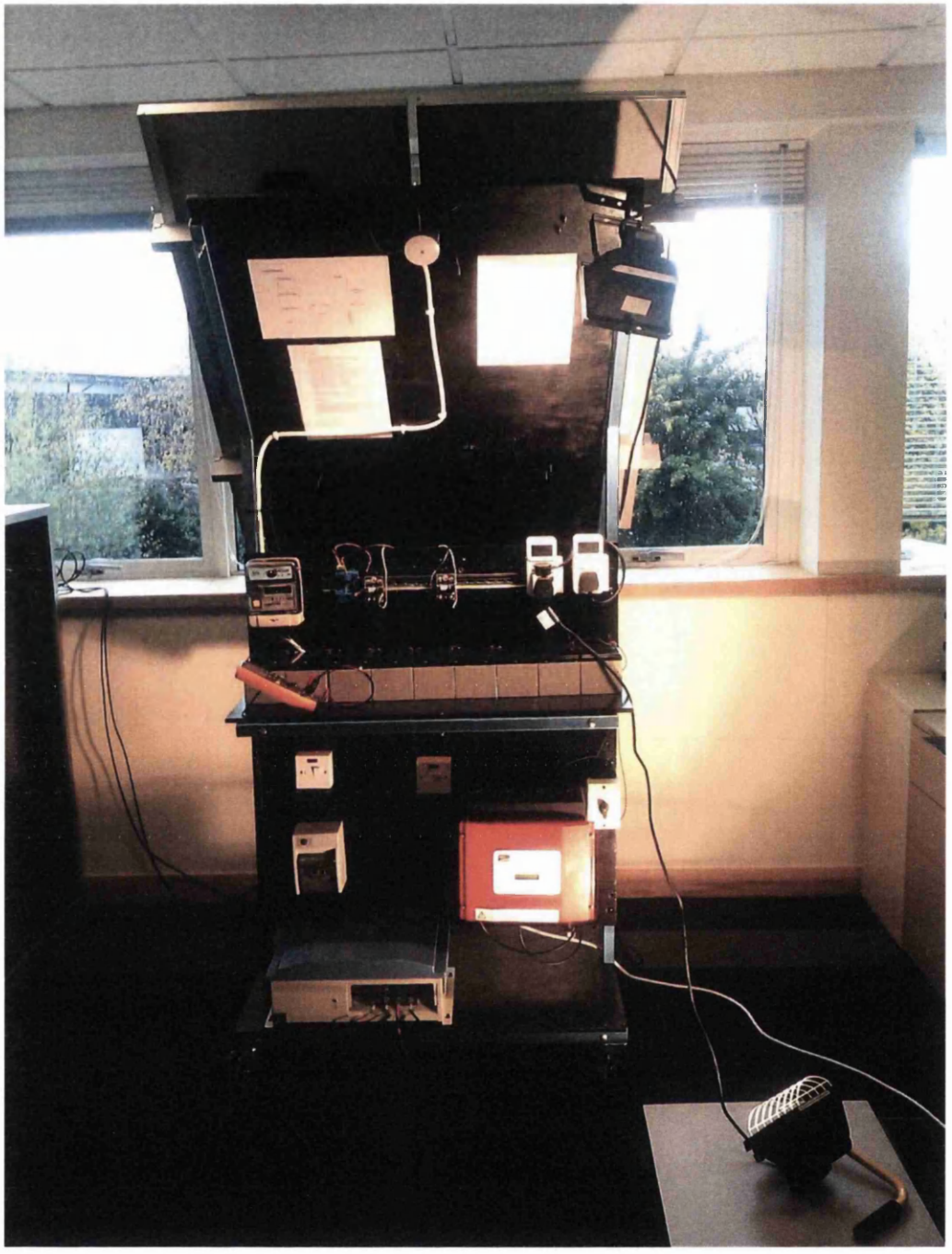
A simple PV storage system was designed to perform such a task. The system consisted of 5 devices:

1. PV Modules
2. Grid-tied Inverter
3. Charge controller
4. Battery Bank
5. Power Management

PV Storage System Schematic



Prototype PV Storage System



Modes of operation

Operation during daytime:

- PV Panels are generating electricity.
- Electricity converted by inverter to provide domestic AC.
- If electricity generated from PV system is more than that required by domestic consumption, the excess is exported into the grid.
- In this instance, a power measurement device fitted near to the existing electricity meter measures the amount of electricity being exported.
- It realises that energy is being exported which could be better used to charge the battery bank instead.
- The measurement device sends a signal to a DC current controller located between the battery bank and PV array. The signal is analogous and is dependent upon the level of electricity being exported. For example if 5A was measured, an external output of 3V would occur. Similarly if 10A was measured, this would correspond to a 6V output.
- The voltage output is received by the DC current controller which in turn diverts a portion of the PV generated electricity, to charge the battery bank.
- Therefore the amount of electricity that was being exported is now being diverted to charge the battery bank. Zero electricity is essentially being exported.
- The energy diverted by the controller from panels to battery bank is not direct. A charge controller is installed before the bank to allow for optimum battery performance and lifetime.
- As the batteries begin to charge, less current is drawn by the charge controller. If the output from the PV system is still greater than that required to charge the batteries, and to provide for domestic consumption, the excess electricity will be exported as normal.
- The storage system reacts constantly to changing light conditions and domestic consumption with no refresh rates etc. For example; if there is excess energy being diverted to the battery bank and suddenly light intensity levels decrease rapidly (thick clouds etc). The power measurement device will detect insufficient PV output to maintain the current charging conditions. The voltage output it sends will decrease accordingly, therefore restricting charge current and diverting a larger proportion of PV generated power for domestic consumption. It does this to avoid importing from the grid as a conventional system would operate.

Operation during nigh-time:

- PV Panels are no longer generating electricity.
- Grid tied inverter has effectively shut down and household is using imported electricity.
- In this instance, the power measurement device fitted near to the existing electricity meter measures the amount of electricity being imported.
- It realises that energy is being imported (at 13p/kW) which instead could be provided from the battery bank (essentially free).
- The measurement device sends a signal to a DC current controller located between the PV array and inverter. The signal is analogous and is dependent upon the level of electricity being imported. For example if 5A was measured, an external output of 3V would occur. Similarly if 10A was measured, this would correspond to a 6V output.
- The voltage output is received by the DC current controller which in turn, diverts a portion of the electricity stored in the battery bank to fulfil the domestic consumption.
- Therefore the amount of electricity that was being imported is now being provided for by the battery bank.
- The energy diverted by the controller from the batteries to inverter is not direct. A charge controller is installed before the bank to allow for optimum battery performance and lifetime.
- As the batteries begin to discharge, less current is allowed to be taken from the bank by the charge controller. If the domestic consumption requirement is larger than that allowed from the battery bank, additional electricity will be imported as usual.
- The storage system reacts constantly to battery power available and domestic consumption with no refresh rates etc. For example; if there is a sudden increase in domestic consumption (Computer, television switched on etc). The power measurement device will detect insufficient battery output to provide for the loads. The voltage output it sends will increase accordingly, therefore diverting a larger proportion of stored battery power for domestic consumption. It does this to avoid importing from the grid as a conventional system would operate. It must be noted that when large electrical consuming appliances are used (cookers, showers etc), the domestic load will increase substantially. In this instant the power

controller will try to provide for the consumption using the battery bank. The charge controller will only allow a specific amount of power from the batteries to avoid damaging them. In this instance the excess needed will be imported from the grid as standard.