Intelligent charging/processing of nickel-cadmium batteries via complex-impedance measurements.

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INTELLIGENT CHARGING/PROCESSING OF NICKEL-CADMIUM BATTERIES VIA COMPLEX-IMPEDANCE MEASUREMENTS

by

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SUMMARY

The work presented in the thesis investigates the use of impedance-component measurements upon conventional sealed Nickel-Cadmium cells and multi-cell batteries for purposes of controlled cell/battery charging and the determination of cell/battery charge state and other aspects of serviceability.

The thesis includes the following parts:-

(a) A review of research into non-conventional methods, including methods involving impedance-component measurements, for the analysis and controlled charging of cells/batteries.

(b) A description of a computer-controlled research test rig designed and constructed for the purposes of performing controlled charge-discharge cycling of cells/batteries and of performing impedance-component measurements at frequencies in the range $^1/_{12}$ Hertz to 128 Hertz upon those batteries.

(c) A discussion of experiments done using the aforementioned research test rig and of associated conclusions. It is discovered that cells/batteries from different sources may have surprisingly different impedance characteristics. The use of measurements of the imaginary component of Nickel-Cadmium cell/battery impedance at frequencies between about $^1/_2$ Hertz and about 32Hz are found to be of practical value for purposes of determination of safe end-of-charge points during the charging of batteries at high charge rates. The use of impedance-component measurements is found to be of limited practical value for purposes of determination of cell/battery state-of-charge except, possibly, where calibration curves can be stored and utilised for individual batteries.

(d) A description of a practical microprocessor-controlled stand-alone charger, based on research results, designed and constructed for "intelligent" charging and testing of PYE P.F.X. radio communications handset batteries. The charger is optimised for use in an 8-hour shift-work system, such as that used by the British Police Force, and has some potential as a marketable product.

STATEMENT

The studies upon which this thesis is based have been carried out entirely by the candidate.
Chapters 1, 2, 3 and 4 should be considered as reviews by the Author of relevant work performed by other persons and authorities.
Material contained within other Chapters should be regarded as being original in content except where acknowledgement is made to other persons or authorities.

.....

(Candidate)

(Director of Studies)

DECLARATION

I declare that the work presented in this thesis has not already been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

J. P. Bain.

(Candidate)

ACKNOWLEDGEMENTS

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AN EXPLANATION OF THE DOCUMENT INDEXES

This document is provided with three indexes, namely a "(General) Index", a "Chapter Index" and a "Graph Index".

The General Index immediately follows this explanatory page and lists the main component parts of the document. It does not list individual sections contained within Chapters and it provides only minimal information relating to the Graphs section.

The Chapter Index follows the General Index and provides a listing of Chapter titles and of titles of individual sections within Chapters where appropriate. Wherever the subject, significance or level of detail contained within a Chapter or Chapter section is not sufficiently apparent from the title the Chapter Index includes a description as guidance for the reader.

The Graph Index immediately precedes the Graphs section of this document. It contains important notes on graph format and gives guidance to the reader for matters of inspecting and interpreting the results presented in graph form.

GENERAL INDEX OF CONTENTS

INTRODUCTION

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DIAGRAMS

(Diagrams relating to the Research Cell/Battery Test Rig follow) ...

GRAPH INDEX AND NOTES ON GRAPHS

GRAPHS - (See Graph Index for more information)

APPENDICES

CHAPTER INDEX

This Chapter covers a range of topics associated with the research programme including justifications, basic requirements, choice of methods and outlines of hardware and software. These subjects are dealt with in a relatively broad and non-detailed form and the sections dealing with hardware and software may be regarded as introductions to the more detailed and technical Chapters 6,7 and 8 which follow.

CHAPTER 6 - "The Research Cell/Battery Test Rig Hardware".

This Chapter contains a wealth of information on the research cell/battery test rig hardware. Most of the titled sections commence with a simple description but some contain highly technical information which is not of immediate value from the point of view of pure battery study but which illustrates the specialised nature and thoroughness of the hardware design.

This Chapter contains a wealth of information on the research cell/battery test rig software excluding programs written in BASIC. Some simple information is given but much of the discussions are quite technical and relate to memory-map and assembly code software listings. Most information included is not of immediate value from the point of view of pure battery study but illustrates the structured use of computer memory and describes an important suite of machine-code routines accessible from BASIC. An especially lengthy description is given of an implementation of a phase-sensitive detection process implemented in software (commencing at page 7 - 15).

This Chapter describes, with reference to program listings contained in this document, the functional parts of two BASIC programs given as examples for purposes of research cell/battery test rig control. Other programs associated with the test rig are outlined. A reader of this Chapter will generally benefit from prior knowledge of B.B.C. BASIC since the programs are somewhat complex and intricate; However, the more casual reader can still glean useful information on program structuring and flow from this Chapter.

This Chapter gives details, justifications and discussions of policies of experimentation, of types of experimentation done and of general problems afflicting experimentation. Some experimental observations and conclusions which influenced the progress of experimentation are outlined.

This Chapter contains much technical information and is written in a highly organised style. A selection of experiments is described and discussed which illustrates important experimental methods, progressions and discoveries. For each titled experiment section the intended purpose of the experiment/experiment-group is described under a sub-section entitled "Purpose" and the observations and conclusions from the experiment/experiment-group are contained in a sub-section entitled "Conclusions". For some experiments the conclusions amount to simple observations; for other experiments a lengthy discussion of the significance and value of observations is given. Some experimental details are included with the list of titled sections as follows.

These experiments involve second-harmonic response studies. Problems encountered and the usefulness of second harmonic methods compared to fundamental-component methods are discussed.

CHAPTER 11 - "Conclusions of the Research as Applicable to State-of-Charge and End-of-Charge Determination for Contemporary Commercial Ni-Cd Cells and Batteries".

This Chapter lists and describes the most important conclusions arising from the experimental programme based upon the research cell/battery test rig. The Chapter also describes three provisional algorithms, based upon experimental observations, for purposes of end-of-charge termination for sealed Ni-Cd cells and batteries.

CHAPTER 12 - "Development of the J.P.B./U.C.S. Charger for PYE P.F.X. Radio Communications Handset Batteries".

This Chapter describes the conception, creation and broad details of the "J.P.B./U.C.S" stand-alone charger for P.F.X. batteries (not to be confused with the research cell/battery test rig!). With reference to the J.P.B./U.C.S. Charger User Manual, contained within this document, the general charging strategies, provisional charging algorithms, user-

This Chapter describes a few experiments done with the J.P.B./U.C.S. charger and includes an early appraisal of its performance. An interesting observation is discussed which appears to be associated with a form of battery internal fault.

CHAPTER 15 - "Late Developments and Discoveries and Overall Conclusions".

This Chapter covers various developments and discoveries made during the late stages of the research programme and includes a discussion of important observations made with batteries obtained via Motorola which suggest possibilities of viability for end-of-charge detection with this type of battery. The Chapter concludes with a section summarising the overall achievements of the Author's programme of work.

INTRODUCTION (IN TWO PARTS)

PART (A) A Philosophical Introduction to the Ni-Cd Battery Processor Project : A Latter-Day Holy Grail?

The research project at the University College of Swansea concerning study of the a.c. impedance parameters of Ni-Cd batteries, with the hope of developing an efficient battery processor, has now reached its conclusion as far as the Author is concerned. It was in some ways a rather ambitious project since it involved the construction of a large customised research test rig prior to any work that could be considered as true research, yet it was always borne in mind that the intended goals might prove to be unattainable in a practical manner. The Author must admit to being something of a perfectionist and, being aware of poorly-supported conclusions made by some previous researchers in the field of battery charging and analysis, saw a necessity for taking a considerable time over the investigation rather than for aiming at a speedy conclusion of doubtful reliability. Indeed, the very nature of the experiments undertaken dictated that progress would be slow. The Author is not entirely satisfied with results achieved since he considers that too much time was spent on matters of hardware and software development rather than on fundamental experimentation; in retrospect, having acquired greater knowledge of techniques and instruments of electronics and computing, he might have tackled some tasks rather differently.

The research project depended upon determination of at least an end-of-charge detector and preferably a state-of-charge detector for sealed Nickel-Cadmium cells and batteries; the reader might care to consider the description of the latter concept by one professional battery engineer, with whom the Author once engaged in conversation, as "the Holy

Grail of Battery Charging": this highlights a quite realistic view of the difficulty of the task embarked upon.

PART (B) An Introduction to the Objectives of the Research

The objectives of the research undertaken were to carry out as far as possible the following tasks:-

(a) Engagement upon a thorough initial search of published literature for information on and results of past research into battery charging and battery electrochemistry. Particular attention would be paid to information relating to the sealed Ni-Cd battery system and to the use of impedance-related techniques in battery analysis. Information would also be sought from battery manufacturers and the Patent Office.

(b) Design and construction of a versatile instrument as a research tool for performing fast, repeatable measurements of terminal voltage and of impedance components upon Nickel-Cadmium cells and batteries at low audio and sub-audio frequencies. The measurement instrument might, if convenient, be provided with additional capabilities.

(c) Design and construction of a charge-discharge rig for research purposes with a capability for cycling up to 48 cells or batteries in a programmed manner. The rig could be used, if desired, to simulate conditions of real-world battery usage and would allow programmed coupling at any time of any selected cell or battery under investigation to a remote measurement instrument.

(d) Use of the special measurement instrument combined with the

charge-discharge rig to perform tests on Ni-Cd cells and batteries as required to determine, as far as possible, an end-of-charge and state-of-charge indicator or algorithm for those batteries. The capability of the test rig to take up to 48 cells or batteries would enable larger numbers of cells/batteries to be studied than by previous researchers and would allow some statistical analysis of results in order to obtain a measure of the effectiveness and reliability of any end/state-of-charge method found.

(e) Optionally, construction and evaluation of a prototype microprocessor-controlled "intelligent" Ni-Cd battery charger/"processor" incorporating the most effective end/state-of-charge detection method or algorithm found. The battery processor might be capable of recognising and dealing selectively with individual cells/batteries if feasible but should, most importantly, be a practical instrument of sufficient robustness and reliability to be usable in expected field conditions.

(f) Optionally, instigation or supervision of field tests on the prototype battery processor in order to determine its practical effectiveness and serviceability.

Some deviations in research objectives were expected and the above list should not be considered as a summary of actual work done. However, most of the original objectives, including optional parts (e),(f), were achieved to a reasonable degree of satisfaction and are discussed later in this thesis.

CHAPTER 1 (IN TWO PARTS)

PART (A): An Introduction to Sealed Nickel-Cadmium Cells and Batteries : Their History and Characteristics

For more information than is given in this Chapter, the following items of literature may be valuable. For general information on batteries and their usage it is suggested that the reader consults references such as (1-4) and for information specifically on sealed Ni-Cd systems also Refs. (5-9). For information on the general electrochemistry of battery electrolyte/electrode systems Refs. (10-14) are suggested.

General History

The first patent for a nickel-cadmium storage cell was granted in 1899 to W. Jungner of Sweden and was soon followed, in 1901, by a patent to Thomas A. Edison of America for the closely related Nickel-Iron system. The earliest Ni-Cd cells were vented and non-pressurised, had bulky "pocket" electrodes and in physical construction were rather like the automotive lead-acid accumulators of today. Many refinements in electrode and electrolyte composition followed which improved battery life and performance. In the 1910's such batteries were mass-produced and fundamentally similar ones are still in use today, primarily for traction or large emergency power installations. In 1928 experiments were done with electrodes based on porous sintered nickel and a few years later the sealed cell incorporating gas recombination emerged. Mass production of the new cell types was started after the Second World War in about 1950.

General Cell Types and Characteristics

Ni-Cd cells have a nominal terminal voltage of 1.25V and a specific energy of 20-40 Wh/kg. Sealed cells are manufactured with capacities commonly from 0.02 to 20Ah and can usually be operated in any orientation. Expected lifetime depends on the nature of the application but is generally between 250 and 10,000 charge-discharge cycles, which may amount to a period of use of as long as ten years. There are three main types of sealed Ni-Cd cells, namely the "button cell", the "cylindrical cell" and the "rectangular cell". All cells contain a negative and a positive electrode separated by a porous non-conducting "separator" which retains an alkaline electrolyte by capillary action. These components are housed in a strong sealed case incorporating electrical terminals. All modern cells incorporate a safety feature to guard against excessive pressure buildup which might arise via improper use or excessive charging.

Button cells have capacities in the range 0.02-0.5Ah and generally have "pressed-plate" (also called "mass-plate" or "bonded-plate") electrodes which provide low self-discharge rate (about 5-8% per month). These cells are designed so that excessive internal pressure causes the button-shaped case to distort. This will either rupture the gas seal or break internal electrical connections in a safe manner; the fail-safe method is thus likely to be fatal to a cell.

Cylindrical cells have capacities in the range 0.1-10Ah and generally have "sintered" electrodes which provide low internal resistance, high current-delivering capability, generally longer life than pressed-plate types and better operation at temperatures below -20°C. However, sintered cells suffer from an increased self-discharge rate (about 10-15% per month) and tend to suffer an effect known as the "memory effect" which involves a reversible loss of capacity (discussed in a later

Chapter). Cylindrical cells incorporate a safety vent, which may be resealable, which can release excessive internal gas pressure. Repeated venting should be avoided since it causes loss of electrolyte and will rapidly degrade cell performance.

Rectangular sealed cells have capacities in the range 11-20Ah, or sometimes greater, and normally employ pressed-plate electrodes. They can deliver quite high currents, have low self-discharge rate and employ safety vents.

Fundamental Chemistry of Sealed Ni-Cd cells

In its discharged state, regardless of the exact nature of the electrodes, the active material of the positive electrode is nickel hydroxide and that of the negative electrode is cadmium hydroxide. The electrolyte is a solution of potassium hydroxide in water; the potassium hydroxide does not participate in the main (generally quoted) cell reaction. During charge, nickel hydroxide is converted to a higher valence oxide:-

$$Ni(OH)_2 + OH^- \longrightarrow NiOOH + H_2O + e^-$$

At the negative electrode, cadmium hydroxide is reduced to cadmium:-

$$Cd(OH)_2 + 2e^- \longrightarrow Cd + 2OH^-$$

The overall reaction is reversible and can be expressed as follows:-

$$2Ni(OH)_2 + Cd(OH)_2 \underset{\text{discharge}}{\overset{\text{charge}}{\rightleftharpoons}} 2NiOOH + Cd + 2H_2O$$

Although undergoing chemical oxidation and reduction during cell

operation, the active materials undergo only minor changes in their physical states. All of the above nickel and cadmium compounds are virtually insoluble in the highly alkaline electrolyte and remain as solids. Hence, apart from a small change in the total water content of a cell (water being consumed during charging) there is little change in the electrolyte concentration during charge or discharge. This results in the Ni-Cd cell having a very flat voltage profile during discharge.

With open, vented Ni-Cd cells, if charging is continued past the point at which most of the active materials have been converted to their charged states then oxygen gas is evolved at the positive plate and hydrogen is produced at the negative plate. The onset of gassing at the negative is accompanied by a pronounced rise in terminal voltage of about 0.2V. With sealed cells, however, such a large rise is not observed since hydrogen production is suppressed by careful design. Sealed cells are manufactured with negative electrodes having an effective capacity in excess to that of the positive electrodes. This calculated excess, sometimes called "charge reserve", ensures that the positive will always commence gassing well before the negative. The oxygen gas generated cannot escape from the sealed cell under normal conditions and a gas pressure of 10-60 p.s.i. may be developed. The cell is designed so that the oxygen can diffuse with reasonable ease from the positive to the negative plate. The great virtue of the sealed cell is its ability to "recombine" the oxygen gas at the negative plate where the following reaction occurs:-

$$2Cd + O_2 + 2H_2O \longrightarrow 2Cd(OH)_2$$

This reaction is exothermic (generates heat), consumes the excess oxygen and ensures that the negative electrode never reaches a fully-charged condition and never evolves significant quantities of hydrogen.

Chemistry of Cell Reversal and Reversal Protection

If a Ni-Cd cell without special protection is discharged, by an externally supplied e.m.f., beyond the point at which all active materials have been converted into their discharged states then the terminal voltage of the cell will reverse and gassing will occur. Oxygen will be evolved at the cadmium-based electrode (now positive) and hydrogen at the nickel-based electrode (now negative) which is most undesirable since gas recombination cannot occur and the cell may eventually vent to relieve the excess pressure. To reduce the harmful effect of "cell reversal" a small amount of negative active material, often called "antipolar mass", can be added to the positive electrode. In normal cell operation this material is electrochemically redundant. Upon reversal of cell voltage, however, the cadmium hydroxide in the antipolar mass begins to be reduced to cadmium. Simultaneously, the cadmium in the antipolar mass is available to combine with oxygen generated at the cadmium-based electrode. Oxygen recombination thus takes place on overdischarge and, as during overcharge, hydrogen evolution is suppressed. This protection mechanism, called "reversal protection", normally operates well at C/10-rate discharge currents but at higher currents its effectiveness at preventing irreversible hydrogen generation during overdischarge decreases.

Electrode, Separator and Electrolyte Types and Finer Details of Chemical Constitution

Sealed Ni-Cd cells incorporate either sintered or pressed-plate electrodes or occasionally one of each, depending on the intended application; the performance characteristics have already been discussed.

Pressed-plate electrodes are produced by a technique in which appropriate active materials {i.e. $Ni(OH_2)$ or $Cd(OH)_2$} in powder form are mixed with conductivity enhancers, binders and other additives and compressed under pressures of about 35-60MPa either into tablets or onto a steel mesh support. The active materials can be prepared by a variety of chemical or electrochemical processes. The nickel-based positives often contain about 20% of flaky graphite to improve conductivity and may include barium hydroxide or cobalt hydroxide to improve performance; antipolar mass may be included. The cadmium-based negatives may include additives such as magnetic iron oxide (Fe_3O_4) and organic oils.

Sintered electrodes are based on plates of sintered nickel having high electrical conductivity. These plates have high porosity of 80-85% with pore size of 5-20μm and thickness 0.5-2mm and are impregnated with the active materials. In practice the base plates are usually manufactured by sintering nickel powder onto a nickel-plated steel mesh, steel being used to reduce usage of costly nickel. Impregnation of the positives with $Ni(OH)_2$ is achieved by chemical precipitation methods followed by careful washing to remove harmful reagents and finally electrical "forming". The cadmium-based negatives may be impregnated either by purely chemical means or by an electrodeposition process followed by further processing.

The material used to separate the electrodes in modern cells is usually a non-woven nylon fabric that is chemically stable in the electrolyte and resistant to oxidation at normal cell operating temperatures. The separator is highly absorbent to electrolyte and permeable to the oxygen gas generated during overcharge. Cells optimised for operation at elevated temperatures often have separators of the more stable material polypropylene, though this reduces gas permeability and cell conductivity.

The electrolyte used in sealed Ni-Cd cells is normally a solution

of potassium hydroxide of concentration 25-30% though lithium hydroxide may sometimes be added in order to improve cell capacity and cycle life. As the oxygen recombination reaction can take place at an appreciable rate only if active materials, electrolyte and gas exist in mutual contact, a sealed cell is not fully saturated with electrolyte. Instead, the degree of electrolyte fill is carefully controlled so that the porous electrodes contain an appreciable percentage of gas space; such electrodes are described as "starved" or "non-flooded".

Further Chemical Considerations

The chemistry of Ni-Cd cells is complicated by the facts that reactions other than the main ones occur, that chemical additives may be used, and that certain cell constituents change or deteriorate with use.

The positive electrode has a particularly complex chemistry. On charge, higher oxides of nickel than NiOOH are formed and have general formula $NiO_x \cdot yH_2O$ where x can vary between 1.6 and 1.8. These higher oxides are unstable and decompose over a period of days or weeks after a fresh charge which results in an increased rate of cell self-discharge during this initial period. Another consequence of the formation of higher oxides is that cell open circuit voltage just after charge may be as high as 1.45-1.7 Volts and takes time to drop to the normal value of 1.3-1.34V. The potassium hydroxide from the electrolyte plays an important role in the formation of higher oxides and potassium ions may become incorporated into the oxide lattices. Sintered cells suffer an increased rate of discharge relative to pressed-plate types since the higher oxides can react with the nickel electrode base to form $Ni(OH_2)$.

The reaction at the negative, cadmium-based electrode is not so variable although iron, if incorporated (deliberately) into the electrode,

may participate to a limited degree in charge/discharge reactions.

Additives are generally used to improve the physical structure of electrode deposits during charging or discharging but inevitably have some effect on cell chemistry. Manganese, copper, chromium, nitrates, carbonates, chlorides and many organic compounds are detrimental to cell performance and iron can poison the nickel-based electrode causing severe capacity loss. As a cell ages additional "foreign" substances may be introduced into the system. These include carbonates from deterioration of nylon separators. Iron compounds may arise via migration of iron from negative electrodes or from the cell case and current-carrying grids which are usually made from nickel-plated steel for reasons of cost.

Factors Affecting Cell Performance and Lifetime (Excluding Charging and the Memory Effect)

The main external factors upon which performance of Ni-Cd devices depend are the rate of discharge and the ambient temperature. Due to internal resistances (including electrochemical polarisations), the average on-load terminal voltage of a Ni-Cd cell decreases with increasing discharge current. Consequently, for any given cutoff voltage, the effective capacity of a cell decreases with increasing discharge rate. For example, for a (rather low) cutoff of 0.4V, the capacity at the 4C discharge rate may be only about 70% of that at C/10 (Ref. 5).

Ni-Cd cells can work over a temperature range of -40 to +50°C but operate best between -20 and +30°C. Below -20°C much performance is lost due to an increased internal resistance. Above +30°C cell voltage is reduced due to a negative temperature coefficient of e.m.f. and the self-discharge rate increases. For best performance at low temperatures or high discharge rates the internal resistance of cells should be kept as low as

possible which requires careful design of the geometry of electrodes, separators and bulk internal electrical conductors.

As mentioned previously, the expected lifetime of a Ni-Cd cell or battery depends on the regime under which it is used. Capacity inevitably degrades as the number of charge/discharge cycles which a cell has undergone increases; there are many causes. Electrolyte is gradually lost by evaporation through cell seals, since these are made of nylon which has some permeability to water; this reduces the electrode area wetted by electrolyte. Also, with cycling, the physical structure of active materials in the electrodes changes. Crystals may aggregate (or "sinter") and lose surface area or may lose electrical contact from the bulk electrical conductors or even be physically shed from the active mass. On discharge of the nickel-based electrode, Nickel hydroxide is formed in the form β-$Ni(OH)_2$ which has a disordered crystal lattice, this being beneficial to electrochemical operation. Normally, charging converts this to β-NiOOH but with high charge rates the form γ-NiOOH can be generated which has a high specific volume. Higher oxides of nickel also tend to have high specific volumes with the result that the volume of the positive electrode increases upon charge. Such volume changes set up mechanical stresses which can cause damage, particularly in pressed-plate electrodes.

Failures may occur in a more sudden manner by development of internal shorts, especially since cadmium metal tends to plate in an irregular manner onto the negative electrode. Cadmium often forms dendritic crystals and sometimes "whiskers" (See Refs. 33,39,40) which can penetrate the separator and make contact with positive plate active materials. Such shorts may be of high resistance, which results in a high cell self-discharge rate, or low resistance, which prevents a cell from accepting charge.

In general, the greater the depth-of-discharge ("d.o.d.") of a Ni-

Cd device, the shorter its service life since increased discharge depth involves greater physical restructuring of active materials. Cells which are maintained on trickle charge for standby or emergency power have effectively zero d.o.d. and usually last five or more years, whereas for 100% d.o.d. a life of 500 cycles is expected for sintered cells and perhaps only 200 for mass-plate types.

Ni-Cd cell life decreases with increasing temperature of operation, whether average or peak. Higher temperatures lead to an increased rate of evaporation of electrolyte through seals and an increased rate of oxidation of separators; separator degradation increases the risk of internal shorts. Special "high temperature" cells incorporate polypropylene separators which can withstand temperatures up to 70°C without excessive oxidation. Internal temperature of cells rises with increasing discharge current due to energy dissipation in internal resistance but, in practice, cells often experience their highest temperatures during charging processes (To be discussed later).

Very excessive temperatures allied with internal pressures arising from poorly controlled overcharging or cell-reversal often result in operation of over-pressure safety mechanisms. Button cells may be rendered useless by a single excursion to high pressure because of the crude protection method adopted. Larger cells, if equipped with non-resealing safety vents (simply a diaphragm which bulges and punctures itself on a metal spike) are rendered permanently leaky such that oxygen will escape with ease during future overcharges. Cells incorporating self-resealing safety vents will fare better but will lose more electrolyte and hence capacity every time that venting occurs.

Cells can fail in a catastrophic manner through improper use; for example external shorting causes intense internal heating which can quickly melt separators and insulators or boil off the electrolyte.

PART (B): **Considerations of Theoretical and Practical Cell Electrochemistry and Cell Electrical Modelling with Particular Reference to the Ni-Cd System**

For more information than is given in this Chapter, references (10,11,12,37) are suggested.

D.c. Considerations

The open-circuit voltage ("o.c.v") of any electrochemical cell is normally equal to the difference between the "electrode potentials" of the materials from which the electrodes are constituted but may deviate from the thermodynamically calculated value if electrode processes other than the nominal reaction occur. For a reversible cell, such as a Ni-Cd type, where a mixture of substances may be present at the electrodes the o.c.v is determined primarily by the materials which are characteristic of the "charged" state. Since electrode potentials vary with type and concentration of electrolyte in a cell, the o.c.v. of a cell depends on the nature of its electrolyte. As has been mentioned already, the electrolyte concentration of the Ni-Cd system remains virtually constant during operation which leads to a very flat discharge profile. Electrode potentials vary with temperature; the consequence of this for Ni-Cd cells is a significant, negative temperature coefficient of terminal voltage of about -4mV/^{o}C.

When a current is passed through an electrolytic cell the terminal voltage changes from its open-circuit value. This is in part due to ohmic resistance of electrical conductors and electrolyte. It should be noted that in electrochemical experimentation the equipment used is normally carefully structured so as to minimise ohmic effects but with practical

electrochemical cells for power storage the ohmic resistance will always be significant. Electrolyte conductivity depends on type and density (virtually fixed for Ni-Cd cells) and very much on temperature. Conductivity generally increases with temperature since ionic mobility increases. Ni-Cd cells performance on discharge falls off at sub-zero temperatures since the aqueous KOH electrolyte becomes viscous (note that the potassium hydroxide acts as an "anti-freeze" agent).

The cell electrolyte is not simply an electrical link between electrodes but is a source of ions for the electrode reactions. On discharge of the Ni-Cd-KOH system, OH^- ions are formed at the positive (nickel-based) plate, migrate through the electrolyte due to an electric field, and are reacted at the negative plate. In practice, though, some K^+ ions also migrate, but in the opposite direction and without being involved in the continuous cell reaction. The consequence of OH^- production at and K^+ migration to the positive plate is that the electrolyte concentration at its surface tends to increase. Conversely, the electrolyte concentration at the negative plate tends to decrease. After a d.c. discharge current has been applied for some time, a steady-state concentration gradient develops in which ion migration is balanced exactly by ion diffusion processes. A similar, though opposite, concentration gradient is developed during charging of a cell. It should be noted that processes of bulk convection can occur in a free liquid electrolyte which tend to suppress concentration gradients; however, in a "matrix electrolyte" which is restrained, for example by being in a gel form, convection is eliminated. A sealed Ni-Cd cell has an electrolyte which is largely restrained due to being held by capillary action within pores of the separator and electrodes.

Electrolyte concentration changes, as described above, at cell electrodes arising from external current flow cause changes in the

electrode potentials, a process which is known as "diffusion polarisation" (or "concentration polarisation"). The resulting change in cell terminal voltage is described as a "diffusion polarisation overvoltage" and appears externally as a non-linear resistance in series with other components of cell internal resistance. When a steady current through a cell is halted, ion migration ceases and diffusion processes level off electrolyte concentration in a characteristic time of the order of a second (c.f. pulse Ni-Cd testing methods described in the next two Chapters).

A second important source of overvoltage is "charge-transfer polarisation" (or "activation polarisation"). An electrode reaction, even if thermodynamically feasible, may occur at a low rate due to having a high activation energy. The presence of an activation energy barrier requires that excess energy be applied externally in order to intensify a reaction. In the case of an electrochemical cell this energy is supplied by an excess voltage. At sufficiently low electrode current densities the activation polarisation is proportional to the current, wheras at high current densities it may be a linear function of the logarithm of current. Hence, in a d.c. situation a charge-transfer polarisation appears externally as an additional non-linear resistance in series with diffusion polarisation resistance. Experiments have shown that activation polarisation in Ni-Cd cells is small compared to diffusion polarisation.

A third source of overvoltage, though of little importance in Ni-Cd cells, is "crystallization polarisation" which results from an activation energy for nucleation of crystals of active electrode materials.

A.c. Considerations at Audio Frequencies

When an alternating current is applied though a cell the situation

observed is rather more complicated, though internal resistance and polarisations still exist. At audio frequencies aqueous ionic electrolytes such as KOH will exhibit a constant resistive impedance equal to that of the d.c. case. Charge-transfer effects will remain dependent on current only and can still be represented as a non-linear resistance.

Diffusion polarisation is very frequency dependent since concentration gradients stabilize and dissipate with a characteristic relaxation time. With a.c. currents applied through a cell the net migration of any particular ion integrated over time is zero so the limiting concentration gradient of the d.c. case is never reached. It can be calculated that diffusion effects give rise to a complex impedance known as the "Warburg" impedance which has form ...

$$\frac{W}{\omega^{0.5}} - j\frac{W}{\omega^{0.5}}$$

where ω represents excitation/measurement angular frequency and W can may be described as a "Warburg Coefficient". This coefficient is a function of frequency in itself and depends on many factors including electrode geometry (See Ref. 37 for a more detailed case).

A further and an important factor which influences a.c. behaviour of electrochemical cells is the "double-layer capacitance" at the electrodes. In an electrochemical cell under conditions of zero external current and high electrolyte conductivity there is virtually zero electric field in the bulk electrolyte. The positively charged electrode tends to attract negative solution ions which form a layer at the electrode surface (it as assumed here that the ions in question do not engage in a chemical reaction with the electrode material). In a similar manner, the negative electrode acquires a layer of positive ions. The ions immediately adjacent to an electrode are held most tightly and are described as the "Helmholtz

layer". Beyond the Helmholtz layer the excess concentration of the attracted ions falls off with distance forming the "Gouy diffuse layer" (for the concentrated electrolytes found in most battery systems the diffuse layer is of the order of 10^{-9}m). The local ordering of ions at an electrode is called a "double-layer" and has the properties of a capacitor whose capacitance per unit electrode area is in the region of 10-100$\mu F/cm^2$ (Note that "wet double-layer" capacitors are now available, for electronic memory backup purposes, with capacitances of the order of 1 Farad). The capacitance of an ionic double layer is normally independent of frequency at audio frequencies but changes with potential. If, however, certain electrolyte ions can be "specifically adsorbed" (a chemical reaction of sorts) at an electrode surface then a relaxation process may occur which causes the effective double-layer capacitance to increase at sufficiently low frequencies. The extra capacitive contribution, known as "adsorption pseudocapacitance", may be an order of magnitude greater than simple double-layer capacitance and often has a relaxation time of the order of ten seconds. The negative electrode of the Ni-Cd system is known to have the ability to adsorb OH^- ions (This will be discussed later as "passivation").

A problem remains in representing and combining the effects discussed above so as to arrive at an effective model of electrochemical cell behaviour as a two-terminal passive electrical network. A complete cell has a pair of electrodes, both of which must be considered, and will inevitably have some internal inductance will largely depend on the geometry of bulk conductors. Fig. 1(i) is a comprehensive electrical equivalent circuit for such a cell; the circuit is qualitatively valid for a multicell battery also. It should be noted that each Warburg impedance includes a resistive part and a capacitively reactive part which are equal in magnitude and highly dependent on frequency. The value and behaviour of

the Warburg impedance can be calculated by considering factors involved in diffusion processes. The result for plane electrodes is known but analysis of porous electrodes, such as those found in Ni-Cd cells, requires the application of complicated transmission-line theory.

In practice, when considering a cell/battery such as a Ni-Cd type, it is often convenient to ignore inductive effects and to lump electrode responses together so as to arrive at a circuit of the "Randles" type shown in Fig. 1(ii). The Warburg impedance is highly frequency dependent and the effective double-layer capacitance may also be so if it contains a contribution from specific ion adsorption. The net impedance formed from the Warburg impedance in series with the charge-transfer resistance is often called a "Faradaic" impedance whilst double-layer capacitive effects are termed "Nonfaradaic".

Passivation of electrodes

Passivation is a process which causes electrodes in electrochemical cells to lose activity. General passivation may result from restructuring of electrode deposits or from buildup of thick insulating oxide layers on electrodes but is sometimes the result of far more subtle effects. Passivation of electrodes can be particularly severe at low temperatures and may develop in a cell after a long period of disuse. In the Ni-Cd cell the cadmium metal of the negative electrode has a tendency to adsorb OH^- ions which form thin resistive films. Both the negative and positive electrodes may suffer structural changes to their active materials which degrade performance (This will be discussed later in Chapter 4).

CHAPTER 2

A Literature Search into Battery Technology with a Particular Interest in State-of-Charge Determination Methods for Ni-Cd batteries and in Applications of Impedance Measurement Methods to Cells and Batteries

An extensive literature search, primarily during the first year of the research, uncovered a fairly large amount of information on battery technology. Much of the information was inevitably technical data of a general nature. Information concerning other battery systems, such as Lead-Acid, was studied for comparison since certain characteristics and problems are shared between battery types.

The report which provoked the Author's research was (Ref. 15) that of Norman Latner in 1968, for the United States Atomic Energy Commission, into determination of a state-of-charge indicator for Ni-Cd batteries. Latner tried out various contemporary methods; these included uncompensated open and closed-circuit voltage measurements, impedance measurements (at unspecified frequencies), terminal-voltage settling time on sudden application of a load; and a coulometer for integration of battery charging and load current. Latner decided that none of these methods was effective in a practical situation. He concluded that "a new inexpensive, simple and rapid method of measuring state of charge was needed" and proceeded to claim that such a method had been found in the measurement of "Farad capacitance" of the Nickel-Cadmium battery. It should noted that Latner's terminology of "Farad capacitance" is rather ambiguous since the science of electrochemistry defines quantities called "Faradaic" and "Nonfaradaic" capacitances, both of which contribute towards terminal capacitance of a storage battery. Perhaps Latner simply

uses the term "Farad" since Ni-Cd batteries often display effective capacitances of the order of (electrical unit) Farads. He does, though, use more rigorous terminology in the technical section of his report.

After encountering problems when trying to use a 1000Hz General Radio Type 1650A Impedance Bridge, Latner found a more suitable instrument for his measurements, namely a Wayne-Kerr B522, four-lead, transformer-ratio-arm bridge. This machine could measure series capacitance of batteries accurately despite contact and battery internal resistances though its measurement frequency was set permanently to 60Hz. The majority of measurements were done on 14 Gould-National 500mAh 6-Volt batteries although nine Eveready (Not Ever Ready which is a different manufacturer) 500mAh button cells were also studied. Latner's general procedure was to first fully charge a cell/battery and then discharge it at the C/5 rate (See Appendix 1(a)) whilst taking measurements of series capacitance or other parameters at timed intervals so that measured parameters could be related to cell/battery state-of-charge.

Each type of cell or battery tested produced a characteristic curve of series capacitance versus state-of-charge although Latner points out that some devices exhibited rather unhelpful "anomalous" behaviour which he attributed to varied histories of use. For the majority of cells/batteries series capacitances were found to decrease in a fairly linear manner during discharge. Absolute values of capacitance depended, as expected, on nominal capacity and number of cells in a battery. Capacitance variation between fully-charged and zero-charged states was a factor of about ten. For single cells, the reproducibility of results was found to be better than 5% and for the 'well-behaved' cells the states-of-charge could be predicted from a standard empirically-determined curve to an accuracy of 7-8%. For 6-cell batteries the state-of-charge predictions were accurate to about 15-16% of the full charge. Latner talks of the need

for a standard reference curve against which measurements on individual batteries must be compared in order to ascertain state-of-charge. His "anomalous" cells, though, could not be expected to perform properly with such a curve and he mentions that cells within three hours or so of having been freshly charged exhibit a further systematic anomaly in response.

Using the rather basic instrumentation available to him and working with a single 500mAh cell, Latner also took measurements of impedance magnitude and components versus state-of-charge and versus measurement frequency from 1Hz to 10kHz. He discovered that both the effective series capacitance and the series resistance of Ni-Cd devices were non-linear functions of frequency. Latner concluded that his hopes for developing a very simple series-capacitance-measuring meter without resorting to bridge techniques could not be realised (or at least, not using electronic techniques available at the time).

It should be noted that Latner's results are not directly useful for application to an "intelligent" battery charger since his measurements were taken solely during battery discharging (in a highly controlled manner) and not during battery charging.

The earliest example that the Author has found of published interest in battery impedance is that (Ref. 27) of Willihnganz and Rohner in about 1959 who tested Lead-Acid storage batteries using a Wheatstone bridge. The extraordinary magnitude of the effective series capacitance of such batteries was commented on but the research did not seem to have been performed with any particular goal in mind.

An example of early work done with Ni-Cd cells/batteries using impedance-related techniques is that (Ref. 28) of Lurie, Seiger and Shair in the U.S.A. in about 1963. The researchers used large sealed cells and tried four types of measurement.

In the first experiment a number of cells were excited with a one-

Ampere sinusoidal current and the phase of the alternating voltage component developed across the cell terminals was measured using a phase meter. A frequency of about 40Hz was found to produce the greatest phase shifts. The phase shift was found to vary with battery state-of-charge in a systematic manner and also with temperature. The method was found to give state-of-charge predictions of up to 10% accuracy under certain controlled conditions.

In a second experiment the apparent "ohmic" (i.e. d.c.) resistance of cells was measured by momentarily shorting cells with very low resistance loads so as to cause discharge currents of 75C or greater. Although promising results were obtained, the method involved serious technical difficulties and was potentially detrimental to the cells.

In a third experiment the researchers attempted to measure the double-layer capacitance of Ni-Cd cells using transient techniques but found that results varied too much between individual cells and between different charge/discharge cycles on any given cell to be of any use.

In a fourth type of test, the magnitude of the impedance of cells was measured at audio frequencies. Impedance magnitude was found to vary little with state of charge except near complete discharge, where a rise was observed; it was noted that this had also found by a previous researcher in 1955.

At the conclusion of their report, Lurie, Seiger and Shair mention a proposition to investigate the components of an equivalent circuit of a Ni-Cd cell using a bridge method in order to see if component variations with state-of-charge provide a usable indicator of state-of-charge. The Author did not manage to find any results of this programme.

Other methods of cell/battery state-of-charge determination that have been tried with batteries, including Ni-Cd types, have generally involved modifying the cell/battery or its associated circuitry. For

example, possibilities exist of optical methods for monitoring electrode state and possibilities exist involving extra sensing electrodes, which are known to have been tried with Lead-acid batteries. Coulometers (See Ref. 29) have been tried in conjunction with battery units in specific applications to record charge flow in and out. However, with sealed Ni-Cd cells/batteries in most applications these methods are inappropriate either because they are ineffective or for reasons of cost and complexity.

Ramasubbalaksmi and Rao (Ref. 17) of India published a review in 1972 of state-of-charge determination methods for Ni-Cd batteries and concluded that the work of Norman Latner, of which they were aware, seemed to be the most promising, or at least promising for the particular Ni-Cd devices used. Several years later, in 1978, Sathyanarayana, Venugopalan and Gopikanth (Ref. 18), also of India made investigations into nondestructive (i.e. nondestructive of charge-state) determination of the state-of-charge of nickel-cadmium cells using a.c. impedance methods. They tried to relate their results to the equivalent electrical network which can be used to represent the Ni-Cd cell.

Using a Wien bridge with a phase-locked detector amplifier the researchers measured effective parallel capacitance and resistance, effective series capacitance and resistance and phase shift. Three nominally 4Ah sealed cells were used and were selected from a batch, after three "conditioning" charge/discharge cycles, so as to have true capacities within 5% of the mean. It was claimed that at measurement frequencies of 40Hz or greater the inductive reactance of the cell, due to its content of ferromagnetic nickel and paramagnetic nickel hydroxide, became dominant over capacitive effects and consequently frequencies above 30Hz were not used. The Author considers, though, that the effect might well have been due to a systematic error introduced by the measurement apparatus; Sathyanarayana et. al. found series-capacitance above 15-25Hz

to increase with increasing test frequency in contradiction to the systematic decrease shown by Latner's and the Author's results. The lowest measurement frequency used was 10Hz due to bridge limitations. The sensitivity of the amplifier was such that the the excitation frequency across a test cell could be kept as low as 1 millivolt which would avoid upsetting the electrochemistry within the cell. It should be noted that cells were brought into various states of charge in a very carefully regulated manner in that predetermined amounts of charge were removed from cells at the C/10 rate and then a ten-hour rest period given before taking measurements. Introduction of charge at constant current was also apparently used though the report does not make clear whether partial charges were used between any measurements in a sequence, which would be problematic due to the non-unity charge-acceptance factor of the cells. The purpose of the rest period was to let certain aspects of cell behaviour, including terminal voltage, to stabilise.

Sathyanarayana et. al. concluded in a general way that the a.c. phase shift and the equivalent series or parallel capacitances of the Ni-Cd cell vary in a useful way with state-of-charge for prediction of charge state. They decided that the impedance of the Ni-Cd cell at 5-30Hz is controlled mainly by diffusion in the electrolyte and subsequently discussed the electrochemistry and equivalent circuit of the cell assuming the porous electrode structures to behave in the manner of electrical transmission lines. The work was later extended to Lead-Acid batteries (Ref. 19).

In 1980 Zimmerman, Martinelli and Badcock (Ref. 20) of the Aerospace Corporation, U.S.A., studied nickel-cadmium cells using impedance measurements in the extensive range of 0.01mHz to 10kHz. Cells of capacity 10Ah were brought into various states of charge using a controlled sequence of charges and partial discharges. This amounted to a

form of pre-conditioning although, unlike Sathyanarayana et. al., it would appear that no particular care was taken to let cells rest for a fixed period before taking measurements. For test frequencies of 10Hz and greater an a.c. impedance measurement system involving sinusoidal excitation was used but for measurements below 10Hz a pulse-excitation method was tried in order to minimise measurement time. In this method an effectively open-circuit cell was subjected to a 1 milliampere current step with the terminal voltage response to this event being recorded over a long period. The Laplace transformations of current and voltage were then used to calculate cell impedance as a function of frequency.

Zimmerman et. al. found that cell impedance became inductive above several hundred Hertz (unlike the 40Hz of Sathyanarayana et. al.) and came to the conclusion, upon analysis of results, that the capacitive impedance observed below 10Hz resulted mainly from diffusion-controlled processes. It was found that the diffusion resistance was inversely proportional to the current applied through the test cell. Attempts were made to formulate a model that involved two consecutive diffusion-controlled charge-transfer processes so as to be consistent with observed results. Experiments indicated that the diffusion coefficients involved decreased by nearly an order of magnitude as a cell was discharged. The diffusion characteristics were thus apparently found to depend on cell state-of-charge. It was suggested that buildup of reaction products {i.e. $Cd(OH)_2$ and NiOH} in the pores of the sintered electrodes could be responsible since these inactive materials could be expected to impede mass transport within the electrodes. A decrease in the general rate of diffusion transport was also found to be associated with occurrence of the "memory effect" (to be discussed in a later Chapter).

In a period up to 1984 Ron Haak, Cameron Ogden, Dennis Teach and Sal di Stefano. in the U.S.A. (Ref. 32) attempted to use impedance

measurements for monitoring Ni-Cd cell degradation and managed to extend the work of previous researchers. A large number of 12Ah sealed cells were used and the tests apparently took place over a considerable period of time since cells were put through several thousand charge/discharge cycles. Attempts to use excitation frequencies of above 10Hz for charged cells gave an inductive response, which the researchers realised was caused by deficiencies in their measurement hardware. The main conclusion was that certain types of cell failure, due to internal shorting (to be discussed later) could be predicted in advance by monitoring the impedance of discharged cells at frequencies of less than 1Hz. The graphs contained within the report indicate that frequencies in the very low range 1-10mHz are required to give the appropriate information. Haak et. al. also tested the usefulness of impedance plots for 5-500mHz as a method of determining state-of-charge and found a parameter which varied in a consistent way for each individual cell but varied in absolute value between cells.

The most recent example of published work of direct relevance to the Author's project is that undertaken by several researchers including N.A. Hampson at the University of Technology, Loughborough, U.K. in the early 1980's (Refs. 21-26). These researchers combined electrochemical studies, using standard electrochemical instrumentation and a Fast-Fourier analyser, with an effort to develop a microprocessor controlled state-of-charge meter. Part of the work, though, involved batteries other than Ni-Cd types.

The first tests with Ni-Cd devices appears to have been with SAFT type "VR", "RR"-size cells of nominal 1.2Ah capacity. The conclusion from initial tests was that cell impedance (It would appear that impedance components are referred to by this expression) varies little with charge state except possibly at frequencies less than 50mHz. The Author, though, suspects that significant variations did occur at higher frequencies but

were rendered hard to detect due to limitations of the electrochemical interface hardware; the hardware was not optimised for test cells of such low impedance. In the report Ref. 21 it is suggested, seemingly rather prematurely, that a practical test for Ni-Cd cells cannot be based on simple a.c. signal injection. Consequently, the work which followed involved the application of pulse techniques with Fast-Fourier analysis methods, though a simpler analysis method was eventually adopted.

A simple pulse test developed involved withdrawing a current from a cell at the 1C rate and noting the terminal voltage after a period of several seconds. It is pointed out that such a current pulse is equivalent to applying a wide range of test frequencies simultaneously. It is not made clear whether voltage change or absolute voltage is the parameter under study; if the method relies on an absolute voltage measurement then it would seem, in common with an on-load voltage test, to be rather sensitive to cell internal temperature unless some form of temperature compensation is involved. The researchers do not mention temperature considerations and perhaps have omitted to give them full consideration. The success of the test under selected cell discharge conditions led to the development of a residual-charge tester instrument incorporating an 8-bit analogue-to-digital converter to measure cell voltage and a Z80A microprocessor, running the high-level language FORTH, for control and data processing. Using a simple calculation algorithm and operating in a highly 'artificial' discharge regime with constant load and constant discharge intervals, which the researchers admit was "hardly typical of real-world conditions", the instrument was found to produce "believable" readings. A graph is included in the report Ref. 21 showing results for one particular 1.2Ah cell, for which true residual charge and indicated residual charge agreed to within 7% throughout discharge.

When using cells from 23Ah aircraft batteries (possibly not fully

sealed types) severe instrumentation problems were experienced arising from their extremely low impedances. With these cells it was determined that "the resistive component did not change as the cells were discharged"; that (in an early analysis, at least) impedance spectra above 49mHz could not be "sufficiently resolved for use as a residual charge indicator" and that impedance spectra at test frequencies below 49mHz were useless for state-of-charge prediction due to lack of reproducibility. As with previous researchers, test cells were brought into various states by means of partial discharges form the fully-charged state. Hampson et. al. had determined that impedance spectrum data for certain primary cell types could be processed so as to give an accurate indication of state-of-charge; the same methods were subsequently tried with the 23Ah Ni-Cd cells. Restricting their work to cells discharged at the 1C rate, it was found that the capacitive reactance at 0.39Hz could be used to predict state-of-charge using a standard linear relationship for six cells out of eight tested (See Ref. 22). The accuracy of the prediction is not specified but the published graph suggests a value somewhat worse than 15%. A frequency of 0.39Hz is claimed to be the optimum value within a possible useful range of 0.1Hz to 10Hz. The researchers comment that they had not determined if the test would be valid at other rates of discharge; this comment resulted from observations that the impedance spectra of the cells depended significantly on rate of discharge, a fact which was attributed to the formation of "variable resistive films" of $Cd(OH)_2$ on the cadmium electrode (i.e. passivation films).

CHAPTER 3 (IN TWO PARTS)

PART (A) Charging Requirements of Ni-Cd Batteries ; Associated Problems and Contemporary Methods

Voltage Profile on Charge

It has already been pointed out in an earlier Chapter that the discharge profile of a sealed Ni-Cd cell (or battery) is very flat due to the virtually constant electrolyte concentration. The voltage profile on charge is also rather flat, compared to other common rechargeable battery types, not only because of the characteristics of the electrolyte but because of the oxygen recombination mechanism which suppresses voltage rise upon overcharge. The behaviour of terminal voltage during overcharge is determined by competing effects. Near overcharge, the formation of higher oxides of nickel at the positive plate tends to increase terminal voltage. However, the oxygen recombination reaction which occurs upon overcharge generates heat which tends to cause terminal voltage to fall because of the negative temperature coefficient of the Ni-Cd system. It should be noted that the rate of rise of internal temperature of a cell during overcharge is determined by the reaction rate and the thermal inertia of the cell. In practice, on charge at rates above C/10 the terminal voltage of a cell increases to a peak near the onset of overcharge and then decreases, gradually approaching a steady value. The exact profile depends on many factors including ambient temperature and cell internal construction. Fig. 2(a) shows the typical profile of terminal voltage for a sealed Ni-Cd cell on charge at two charge rates.

Temperature and Internal Pressure on Charge

Restrictions on internal temperature and pressure are the factors which determine the maximum rate and degree of charging of Ni-Cd cells and batteries. Fig. 2(b) shows typical profiles of internal temperature and internal pressure for a sealed Ni-Cd cell on charge at two charge rates.

During the early part of the charging process some internal heating of a cell occurs due to internal resistance, though this is partly offset by the endothermic (consuming heat) nature of the charging reaction. The oxygen recombination reaction, however, is exothermic. Oxygen evolution begins when a cell is about 75% charged and once the positive plate active material is fully converted to the charged state then all electrical input goes into oxygen production. Provided that charge rates are not very high then the oxygen recombination reaction lags only slightly behind the rate of production. Consequently, cell internal temperature shows a well-defined rise at or prior to true overcharge. The exact profile is dependent greatly on the charge rate.

In most charging situations the case temperature of a cell will be lower than the internal temperature because of cooling by thermal convection, conduction or radiation. Furthermore, as cell components have considerable thermal inertia then internal rises in temperature will take time to manifest themselves as an increased case temperature. Battery packs comprising multiple cells packed into a compact structure can be rather susceptible to internal overheating arising from excessive charging.

Cell internal pressure is related to the difference between rates of oxygen production and consumption and follows a profile roughly similar to that of temperature. At high charge rates the internal pressure of a sealed cell increases dramatically upon evolution of oxygen and can lead

to cell venting if the charging process is not properly controlled. Charging at low temperatures must be done with great caution to avoid excessive pressure rises since the oxygen recombination rate decreases with decreasing temperature.

D.c. Charging Methods Without Parameter Sensing

Constant-voltage charging, as used commonly for lead-acid batteries, is quite inappropriate for sealed Ni-Cd cells devices because the temperature coefficient of voltage of the sealed Ni-Cd system is negative and can lead to disastrous thermal runaway.

The "standard" method for charging Ni-Cd devices is by application of a constant current at the C/10 rate for 14-16 hours. Partly because of the nature of the kinetics of the cell reaction and partly because of wastage of charging current through oxygen production, a Ni-Cd cell/battery needs at least 40% charge in excess of its nominal capacity in order to become fully charged. The excess charge requirement is often defined in terms of an "overcharge factor", this being about 140% for Ni-Cd devices. The great advantage of charging at the C/10 rate is that virtually all cells/batteries can withstand an overcharge at room temperature at the C/10 rate for many hours without damage. Some manufacturers even claim that indefinite charging at this rate will have no serious effect. A cell/battery may thus be charged fully and safely with a "standard" charge regardless of its initial state-of-charge, which is very convenient for the user. The great disadvantage of the standard charge is that it takes an appreciable period of time which may cause problems for certain types of user. Furthermore, the user has no way of knowing when any particular cell/battery, perhaps having been put on charge from a part-charged state, is ready for use. Some sources (See

Refs. 9,39(June),40) suggest that charging at C/10 rates encourages growth of cadmium dendrites and whiskers and that extensive overcharge at this rate should thus be avoided.

Faster charging may be achieved by a process known as "dump-charging" in which a cell or battery is first discharged rapidly, perhaps at the C/2 rate, to a predetermined cutoff voltage and then charged at a rate greater than C/10 for a fixed time. The initial discharge ensures that a cell/battery is in a fully exhausted state before charging so that the degree of overcharge received is determined only by the properties of the charger. Charge rates using this method may be as great as several C. However, oxygen evolution occurs within cells well prior to overcharge proper with rates of pressure rise being greater at higher charge rates; consequently, charging at high rates must be terminated before the fully charged state is reached. For example, charging at the 1C rate must normally be terminated when a cell has been given a charge equal to about 80% of its true capacity. Some chargers transfer a cell/battery to a C/10 charge on completion of a fast charge phase in order to top-up remaining uncharged capacity at a safe rate.

D.c. Charging Methods With Parameter Sensing

By sensing or monitoring certain aspects of cell/battery behaviour during charge it is sometimes possible to sense the point at which a Ni-Cd device becomes fully charged. A viable end-of-charge determination method allows cells/batteries to be charged from unknown initial states at rates greater than C/10 without harm.

The ideal parameter that could be sensed is cell internal pressure; pressure sensors, though, tend to be complicated and expensive devices. A possible alternative is an oxygen partial pressure sensor (See

Ref. 29). Cell internal temperature would also be a valuable indicator, though temperature rise on overcharge at very high rates lags behind rise in pressure. Unfortunately, any type of monitoring of the internal climate of a cell requires special cell construction which is far too expensive for use in all but the most demanding applications. A second-best parameter is cell case temperature, measurable by a thermistor or other device in contact with the exterior of a cell. In battery packs where several cells are potted into a case a temperature sensor may be included at the central point of the cell cluster. During charging, case temperature can be monitored and overcharge can be considered to be achieved when either the cell/battery temperature exceeds a certain threshold or when the rate of rise of temperature exceeds a predetermined value.

The on-charge terminal voltage profile, although generally rather flat, does display a rise upon overcharge that can be sufficiently sharp and repeatable for end-of-charge detection provided that the charge rate is about 1C or more. It is sometimes possible to monitor absolute terminal voltage, on charge or open circuit, as a charge-state indicator for lower charge rates provided that the cell/battery is provided with an accurate temperature sensor for purposes of temperature compensation.

Asymmetrical-a.c. Charging Methods

Methods of charging using asymmetrical a.c. currents, in which the average current is in the charging direction and constant, or reasonably so, have been tried with various battery systems. For example, methods of partly recharging zinc-carbon primary cells have been described in which an asymmetrical a.c. current produces a more uniform redeposition of zinc on the negative electrode. The a.c. charging method arises in part

from experiences with industrial electroplating. A.c. currents will in theory influence the degree of diffusional polarization at electrodes but the effect that this will have on charging efficiency of cells such as Ni-Cd units seems arguable, though some experiments (See Refs. 8,30) indicate improvements of 10-15% over constant-current charging for vented Ni-Cd batteries. One more specific claim for a.c. charging with Ni-Cd cells is that formation of dendrites or whiskers of cadmium is suppressed (See Ref. 39). Theory and experiment suggest that discharge currents may preferentially dissolve cadmium metal from such structures rather than from bulk electrode material; hence, periodic reversals of a charging current may prevent dendrite growth.

Methods of charging with structured a.c. waveforms have been used in which the waveform is used to measure selected aspects of electrical behaviour of Ni-Cd cells or batteries. Some examples of such methods will be discussed in the next Chapter.

PART (B) A Review of Contemporary Charging Systems for Sealed Ni-Cd Devices ; How Effective Are They?

"Constant-Current" Chargers

The vast majority of Ni-Cd cell/battery charging units sold for domestic and general use are simple, inexpensive nominally constant-current units utilising C/10 or lower charge rates. The most basic "constant-current" chargers, in fact, generate unsmoothed, rectified a.c. derived from a mains supply via a transformer, in which case the average current is maintained reasonably constant either by a resistance in series with the battery or by a capacitor in series with the transformer primary. Users of constant-current chargers often leave cells and batteries on virtually permanent charge when not in use. Although nearly all Ni-Cd devices will tolerate continuous C/10 rate currents, their performances will generally be degraded over long periods of time.

Medium-scale users of Ni-Cd batteries, such as organisations operating portable radio communications equipment, may use C/10 rate multi-battery chargers in which any battery receives a constant C/10 charge whenever it is in position in a battery holder. With this type of charger the user may have to follow a special routine for keeping a check on how long each battery has been on charge. It will generally be necessary to maintain an appreciable number of spare batteries on charge in order to ensure continuity of availability of charged units. It is inevitable that some battery units will spend much of their time idling on overcharge.

"Dump-Charge" Chargers

For some commercial users, such as those operating radio communications handsets in shift systems, a 16-hour charging period may be unacceptably long. The simplest solution is the use of a "batch charger" based on the "dump-charge" principle. Examples of these are a range of chargers manufactured by Stoneleigh Electronics (U.K.). The most recent versions from Stoneleigh incorporate solid-state electronic timing and control and can charge a battery in 8 hours using a discharge to a preset voltage cutoff, at about the C/2 rate, followed by a timed six-hour charge at about the C/4 rate. Due to the nature of the electronics in batch chargers, the charging process must start on all batteries simultaneously; a battery could be damaged by insertion into a machine when part way through its cycle. Batch chargers give a clear indication to the user of when the charging cycle has ended.

The dump-charge method, although neat and capable of giving guaranteed full, or near-full, charging has a major disadvantage in that it forces every cell or battery to undergo 100% depth-of-discharge. Consequently, only the minimum rated lifetime should be expected from any Ni-Cd unit regardless of the average degree of discharge resulting from use in powered equipment. A further drawback is that damaging cell reversal may occur during discharge phases when the method is used with many-cell batteries (To be discussed in the next Chapter).

"Intelligent" Chargers

In order to improve charging performance it is necessary to involve some control of charging/discharging currents based on sensing of one or more parameters of a cell/battery. Four examples of chargers

incorporating control feedback loops or electronic "intelligence" are discussed below.

The "TSL" system of VARTA Batteries Limited (See Ref. 8) uses terminal voltage sensing with temperature compensation. Charging is done with unsmoothed, full-wave-rectified current at an effective rate of about 1C until cell terminal voltage exceeds a predetermined limit, whereupon current is reduced to a trickle-charge level. Terminal voltage is sensed during the troughs of the charging waveform, so as to eliminate effects of contact and other resistances. The reference voltage is given a temperature coefficient equal to that of the Ni-Cd system in order to eliminate the interfering effect of ambient temperature variations although a cell or battery being charged needs to be in an ambient temperature within 10°C of that of the charger. The method is apparently viable with batteries of up to 10 cells and the initial fast-charge phase ceases when about 80% nominal capacity has been reached. It is claimed that the "TSL" method is especially valuable when charging batteries at high ambient temperatures, whereupon battery charge acceptance and expected life are increased in comparison to situations where "conventional" charging is used. Similar methods have apparently been tried by various manufacturers of batteries and equipment although specific information on performance of the method is hard to obtain.

A rather more exotic charger for specialised applications is the "ReFLEX-20" (Ref. 31) manufactured by the Christie Electric Corporation (U.S.A.) for which it is claimed that batteries of any initial state-of-charge can be fully charged within 20 minutes and that battery lifetimes can extended up to tenfold relative to more common methods of charging. The ReFLEX-20 uses a 4C average charge rate for a primary charge phase. The charging waveform comprises alternate positive-going (charging) pulses and sharp, negative-going pulses. It would appear that the positive

"pulses" are derived from an unsmoothed full-wave-rectified a.c. waveform. Battery terminal voltage is measured during zero-current periods and is used to check the state of the battery. The negative going pulses, which the author of the above reference likens to the "burping" of a baby, are claimed to eliminate battery polarisation losses and to produce charging efficiencies of 90-97% with minimal battery heating. The energy of the negative pulses is not constant but is increased as the battery state-of-charge is sensed to increase. Some very grand claims are made but it should be noted that the ReFLEX-20 is intended for use with proprietary battery packs containing extremely high grade cells and an array of thermistors, thermal switches and fuses necessary for temperature compensation and protection. Cells are sorted, using many precise tests, into an astonishing 484 charge/discharge performance groups in order to obtain supermatched sets for the batteries. The overall scheme obviously involves a great deal of expense and is intended for use by customers for whom reliability has a far higher priority than financial cost, such as military and medical concerns and the television/film industries.

Provided that a charger instrument can be given electronic memory facilities, it may be possible to control charging through keeping track of cell/battery voltage profile whilst on charge. Black & Decker Inc. have taken out a patent (Ref. 40) for such an instrument. Interfering effects of ambient or battery temperature and of varied battery history are claimed to be eliminated since the absolute value of terminal voltage is not of primary importance. Instead, a microcontroller within the instrument observes and records trends in voltage during the period in which a high-rate charging current is applied. When a predetermined sequence of events is observed, which may include regions of positive or negative slope or points of inflection, the charge current is reduced to about the C/10 rate for a limited period of time and then to an even lower

"maintenance" level. The charging algorithm, incorporated into control software, is claimed to be capable of recognising already-fully-charged batteries and certain types of defective battery.

A fourth and very recent example of an "intelligent" charger, of which the Author has had first-hand experience, is the Redif(fusi)on "BC21" "battery processor" for Pye "PFX" radio communications handset batteries. The Author first acquired information on this charger late in 1987. A British patent (Ref. 41) has been taken out on this machine and it would appear that marketing of the initial version is only in its early stages (and may now have been discontinued - see Chapter 15). The machine can accept up to 10 batteries at a time and uses a fast charging technique which is claimed to charge batteries fully in 20 minutes or less. The charger is unusual, though, in that the fast-charging phase of operation deals with batteries in a time-sequential manner rather than simultaneously; batteries inserted into the charger are sorted by software into a queue and are charged one at a time. The primary reason for this mode of operation appears to lie in the charge-current generator hardware which contains expensive and bulky components and requires a large power supply and heatsink for just one current generator. The sequential charging method, though, does have advantages for the user in certain applications.

The BC21 uses an a.c. current waveform of fixed and rather complex profile for charging. The waveform has a period of about 12 seconds and incorporates a discharge pulse lasting about a second. A BC21 unit which the Author had a chance to study was calibrated for 600mAh batteries and the average current delivered per wave-cycle was measured at 1.52A which corresponds to an effective charge rate of 2.53C. It is interesting to note that even assuming a 100% overcharge factor this charge rate would take 24, and certainly not just 20, minutes to charge batteries fully. An

end-of-charge detection method is employed which is based on analysis of terminal voltage variations arising from a change in current through a battery. A parameter is sensed which increases in magnitude on approach to full charge and decreases slightly as overcharge progresses. The measurement taken has some relation to a measurement of battery impedance using mixed frequencies though the "excitation" currents involved are much larger than for conventional instrumentation impedance methods and may modify battery response. As the end-of-charge detector is incapable of responding to an already-fully-charged battery, for which the measured parameter will be at or near its peak, it is necessary to discharge a battery by a predetermined amount before starting a fast-charge operation on it. The discharge is done at a high current of about -2.5C and lasts for a few minutes or until a preset voltage cutoff is reached. The BC21 puts each battery onto a C/10 charge after the initial fast-charge phase.

Apart from the normal "Fast Charge/Top Up" mode two other operational modes are provided. In a "Trickle Charge" mode all batteries are charged in parallel at a constant C/10 rate. In a "Rapid Charge/Analyse" mode the batteries, one at a time, are discharged to a preset cutoff voltage and then fast-charged; the working capacity of the battery is estimated from the time taken to reach apparent end-of-charge and if less than 70% of the nominal capacity a warning is signalled to the user.

The BC21 is controlled by a dedicated 8039 microprocessor provided with 4kbytes of R.A.M. and an attempt has been made to completely automate operation. The machine senses when a battery is inserted, by the user, into any of ten holders provided and places the battery into a queue for charging. Indicator l.e.d.'s inform the user of the state of progress of charging for any battery.

The Author has tested the operation of one BC21 and has found it

to perform in a sensible manner except when mains power fails and is reinstated, whereupon the machine forgets everything that it has previously done and begins a charging sequence all over again. Furthermore, momentary mains failures sometimes caused the machine to latch up into non-operating states. The Author's own simple tests of charging effectiveness indicate that the fast-charge phase of the BC21 is capable of charging new "PFX" batteries containing cells of SAFT manufacture to an average of 86% of their true capacities, with about 25 minutes taken per battery. The manufacturer's claims for charging thus seem somewhat inaccurate. In most situations of use, though, the C/10 charge which follows the true fast-charge phase will top up most batteries to their full capacities.

The Redif(fusi)on BC21 and the Christie ReFLEX-20 are both "reflex" chargers though have greatly differing waveforms. A comparison of constant current, positive pulse and reflex charging was done by Otto C. Wagner and Dorothy D. Williams in about 1984 (Ref 8,30) for the U.S. Army. Conclusions for charging vented Ni-Cd batteries at average currents of 2C were that the charge efficiencies of both the negative and positive plates of the Ni-Cd cell were slightly greater for positive pulse charging than for constant-current charging and 10-15% greater for reflex methods. The advantages of reflex charging were found to be reduced at temperatures above about 40°C. For constant frequency reflex waveforms the energy content of the negative pulse, rather than its shape or peak magnitude, was found to be the critical factor. For a five-cell 5.5Ah battery and 60Hz reflex charging the optimum negative pulse energy was claimed to be about 3 milliwatt-seconds. According to the discussion of the results by VARTA (Ref. 8) similar results were not achieved with otherwise equivalent Ni-Cd batteries of the sealed type.

CHAPTER 4

Problems Remaining with Ni-Cd Cells and Batteries and Thoughts upon Improvements for Management of Battery Charging

Apart from the need at charge rates above C/10 for cautious charging to avoid excessive overcharging (outlined in Chapter 3) other problems exist with Ni-Cd cells and batteries which are easily overlooked or ignored. These include phenomena involving temporary or reversible loss of useful capacity and also detrimental cell-reversal problems in multi-cell batteries. This Chapter discusses such matters and concludes with thoughts upon ways in which the management of charging of batteries could be improved.

Reversible Capacity-Loss Effects in Sintered Ni-Cd Cells Including the "Memory Effect"

Ni-Cd cells of the sintered-electrode type suffer from effects which manifest themselves in various ways involving a non-permanent loss of performance in charge acceptance and delivery. The effect is attributed to physical restructuring of the active materials of one or both electrodes.

New cells/batteries are normally supplied by manufacturers in an uncharged state and the user is often warned that cells/batteries will need to undergo two or three standard C/10 charges, each followed by a full discharge, before they will develop full working capacities. Such a process is required to "form" the electrode active materials into more effective physical states. This procedure is also advisable for any Ni-Cd

cell that has undergone a long period of disuse. However, it should be noted that temporary or "reversible" losses of cell performance can also result from certain regimes of apparently normal cell usage.

A cell or battery which undergoes a very long period of overcharge may develop a reduced capacity by a process involving recrystallisation of cadmium hydroxide at the negative (cadmium-based) electrode (See Refs. 30,34). The effect can appear not only as a reduction in capacity but as a depression of cell terminal voltage by up to 150mV over the latter part of any subsequent discharge. The effect is sometimes called "fadeout" and it can normally be cured by applying several standard charges, each followed by a full discharge. Usually, only batteries employed for standby power are affected by the phenomenon since the overcharge periods required are of the order of months. Otto C. Wagner and Dorothy D. Williams (Ref. 30) found that a pulse charging method could restore negative plate capacity in one cycle.

The true "memory" effect is more complex and seems to be related to effects at both the negative and positive (nickel-based) plates (See Refs. 34,35,38). There seems to be a fair degree of uncertainty, though, as to which electrode is most to blame and, noting that not all cells appear to be susceptible, the processes involved may be very sensitive to subtle differences in electrode composition. As an example of the memory effect, suppose that a good sintered cell undergoes a highly repetitive charge/discharge regime in which it is always discharged to exactly 50% d.o.d. After about 20-50 cycles it may be found that the cell, if called upon to deliver its full capacity, will have developed a depressed "second plateau" in its terminal voltage beyond the 50% d.o.d. point. The cell may still be capable of delivering its full coulombic charge but the terminal voltage during the second plateau may be too low to power equipment properly. However, the cure for the memory effect is simple: an afflicted

cell or battery can usually be restored to its normal state by giving it two or three standard charges, each followed by a full discharge.

The memory effect may or may not be a problem in real-world situations since conditions of battery usage vary. Not all battery applications involve highly repetitive partial discharges so the memory effect may never occur in an extreme form. Furthermore, in many situations of use batteries receive occasional full discharges which will reverse any memory that might be tending to develop.

Extra Problems Associated with Multi-cell Ni-Cd Batteries

Ni-Cd cells are often connected in series and assembled into cases so as to form discrete battery packs. Alternatively, battery assemblies may be semi-permanently installed into portable equipment. Unfortunately, multi-cell batteries suffer from additional problems during charging and discharging which tend to become more significant as the number of constituent cells increases.

Since cells are often closely packed into compact cases, the effective surface area per cell available for air convection cooling and radiation cooling is reduced. Hence, on overcharge or on high-rate discharge the central cells in a pack are likely to become quite hot. Furthermore, if cells within such a pack are allowed to vent then the battery case, if not well designed, may be fractured by the pressure of released gas.

A quite serious problem can occur if a multi-cell battery is discharged deeply. Cells for use in a given battery pack will usually be matched for true capacity to perhaps 5%. If the pack is given a full charge with overcharge and subsequently placed on discharge then some

cells will inevitably reach voltage cutoff before others. If the discharge current is maintained even after the first cell has undergone voltage reversal then that cell will be subjected to reverse charging, possibly at a rate considerably greater than the reasonably safe C/10 rate. Battery voltage sensing is incorporated into dump-chargers and into some powered equipment in order to prevent discharge of batteries below a preset voltage limit; the limit is often chosen as being the number of cells in the battery multiplied by a value in the range 0.9-1.0 Volt. Such a discharge limit is very valuable for few-cell batteries but is a poor method for preventing cell-voltage reversal in batteries of over six cells. Consider, for example, a seven-cell battery combined with a voltage cutoff of 7V: it is difficult to distinguish between a battery containing seven cells discharged to 1V and a battery containing six cells at 1.25V in series with one being reverse charged at -0.4V. Over the course of time the capacity match between batteries in a pack is likely to worsen which will render the occurrence of reverse charging more likely. Furthermore, since the cell in a pack which is most vulnerable to reverse charging, and hence damage, is the one with the lowest initial capacity then a vicious circle of degradation may ensue.

Possible Improvements for Battery Charging Management

In practice Ni-Cd cells and batteries are often subjected to charging regimes which are deleterious to good performance and long life, especially in situations where relatively fast and user-convenient charging is required. It is inevitable that, in order to increase charging rates and convenience without tradeoffs in cell/battery performance, the complexity of the charging process must be increased. For this purpose a

state-of-charge or end-of-charge determination method for Ni-Cd cells/batteries would be of enormous value. A practical battery charger/processor utilising complex monitoring and charging methods would probably need to utilise microprocessor control to such an extent that it would be deserving of the title of an "intelligent" instrument (in much the same manner by which a computer terminal is conventionally called "intelligent" as opposed to "dumb" if it incorporates a microprocessor and provides special interpretation or user functions rather than doing little more than converting key presses into unique electrical signals). It has been shown in previous Chapters of this document that matters of battery monitoring by electrical methods and controlled charging have been investigated in the past. However, previous examples of research had been limited in scope and the only known practical, contemporary battery charger for non-selected batteries, namely the PYE P.F.X. charger (see Chapter 3), utilised by design necessity a charging regime which could be described as highly aggressive.

Improvements in general technology often enable old problems to be reviewed and sometimes overcome substantially. The problems associated with Ni-Cd cells and batteries certainly fall into this category. The Author realised that opportunities for investigation existed, which have been partially tackled by his own efforts: namely a programme of research, pursued using purpose built test instrumentation, with the main object of study being impedance-component response during charging processes. The Author's efforts were eventually directed towards development of a practical "intelligent" battery charger/processor for a specific application; this charger, though certainly not an exhaustive or perfect solution is certainly capable of future development. Considering the increasing influence of microprocessors upon all aspects of life nowadays it is not inconceivable that ultra-intelligent battery processors/chargers

may eventually be introduced which are capable of recognising individual batteries, especially in situations where many batteries are associated with a user based at one site. Such chargers might use highly optimised and flexible charging regimes, might monitor battery performance over entire battery lifetimes, might be capable of recognising problems such as the memory effect and might advise of any necessity for battery conditioning or replacement. Work such as the Author's may well play a role in the development of such technologies.

CHAPTER 5

An Introduction to the Ni-Cd Battery Research Programme (excluding matters relating to research results and to the "J.P.B./U.C.S." Charger)

Justifications for the Research

The initial literature search in the early months of the project uncovered quite a wealth of information on battery technology. It appeared that no practical state-of-charge indicator had been found for sealed Ni-Cd batteries and that contemporary end-of-charge sensing methods could certainly be improved upon. It seemed that the use of advanced fast chargers (e.g. the "reflex" type) was very rare in the United Kingdom except, perhaps, within the military services and the television and film industries. Requests for information from U.S.A. battery manufacturers Gould and General Electric and from some European manufacturers met with no success though it seemed likely that such industrial concerns would have researched matters of advanced battery charging; it was impossible to tell in these cases whether information was being considered too proprietary to divulge or, perhaps, whether attempts at practical chargers had been embarrassingly unreliable. No evidence was ever found that impedance-related measurements were in use for purposes of practical battery monitoring and charging.

As for reports of relevant research published in the open literature, the conclusions of researchers varied; it seemed sensible, though, to give greater weighting to the more recent examples. In studies relating to a.c. impedance parameters of Ni-Cd batteries the test instrumentation used was often basic and sometimes suspect, one evident

major problem being that conventional measurement instruments designed for use in electronics or electrochemistry are not optimised for use with test devices in the extremely low impedance range (tens of milliohms) characteristic of Ni-Cd storage cells/batteries. The earliest examples of experimentation involved test frequencies rather higher than those considered suitable by later researchers, though this was largely a result of limitations of available test instrumentation. In most cases only single cells or small samples of cells/batteries were studied and little or no allowance was made in conclusions for the effects of production variations between individual cells. None of the investigations involved taking measurements of impedance parameters during cell/battery charging, as opposed to discharging from a known fully charged state; this is somewhat surprising considering that an advanced or "intelligent" battery charger having end-of-charge sensing will be required to operate primarily under the charging regime.

With the apparently promising results of Latner, of Hampson and of Sathyanarayana et. al. (Reviewed in Chapter 2) given particular consideration, it seemed that more extensive research was desirable using a purpose-built battery testing system and using samples of tens or hundreds of cells/batteries before the true usefulness of impedance methods in practical Ni-Cd battery analysis and processing could be determined. The Author consequently engaged upon a course of action involving construction of a specialised testing system (introduced in this Chapter), followed by use of that system for experimentation into cell/battery impedance parameters (introduced in Chapter 9), followed by the development of a stand-alone charger for a particular type of Ni-Cd battery (the "J.P.B./U.C.S. charger - introduced in Chapter 12): However, the Author always bore in mind that that impedance methods, including his own, might prove to be of limited practical value.

Basic Requirements for Tests and a Test System

It has been shown in Chapter 1 that the Ni-Cd cell can be electrically modelled in a number of ways. Equivalent circuits such as the Randles variety (See Fig. 1(ii)) may be of use to the electrochemist who can relate components in the network to physical and chemical processes but for an engineer investigating the external electrical properties of a battery such models can be somewhat cumbersome. A Ni-Cd cell can be regarded as a two-terminal network which, to a first approximation, is a series combination of a small resistance, a large capacitance and a small inductance, though at frequencies below about 100Hz the internal inductance of a typical sealed Ni-Cd is generally small enough to be ignored. The effective series capacitance and effective series resistance are known to be frequency-dependent and to be related to some extent to cell/battery charge state. In view of the complexity of the internal electrochemical and physical processes occurring within cells, of which only the most major seem to have been satisfactorily modelled, and in view of the fact that subtle differences in cell constitution and construction are likely to have dramatic effects on elements of the a.c. impedance response, it was decided for purposes of the Author's research that Ni-Cd cells and batteries would best be treated as simple R-C series combinations. The effective values of R and C at any frequency could be determined simply by measuring, respectively, the real and imaginary components of impedance; results would then be treated in a largely empirical manner. An impedance meter of some form was thus required for the research programme.

A separate requirement existed for subjecting Ni-Cd cells and batteries to controlled charge-discharge cycling in as flexible a manner as possible. It was considered desirable to perform charge-discharge

cycling and measurements on a large number of cells/batteries simultaneously in order to reduce experimentation time and to allow easy comparison and statistical-type analysis of cells/batteries.

In view of the above points, a fundamental decision made at an early stage was that a specialised test rig should be built having a capability to run about 50 sealed Ni-Cd cells or batteries simultaneously through preprogrammed cycles of charging and discharging by computer control. Impedance components of cells/batteries on test would be measured automatically at defined intervals using some form of impedance meter incorporated into the test rig and results would be printed onto paper or stored on magnetic media. The test rig would also have a capability for performing simple d.c. measurements to aid monitoring of cell/battery charge status. The test rig would be designed, within reasonable cost restraints, so as to be highly flexible and adaptable with its modes of operation largely determined by software. The test rig, by virtue of its computer control, would in theory be capable of decision-making and could thus be used as an intelligent tool in cell/battery analysis.

Charge-Discharge Hardware Requirements and Choices

A piece of electrical hardware was required, as part of the test rig, for the purpose of passing charge-direction and discharge direction currents through Ni-Cd cells and batteries in a highly programmable manner. The hardware was thought to be best constructed in a modular form for ease of assembly and maintenance. In practice, 48 identical "charge-discharge" printed-circuit-board modules were constructed, with one cell/battery being allocated to each module. The modules were mounted on a rack structure and were linked to other items of hardware, including a

measurement instrument and a controller computer, via various bus structures. The choice of about 50 modules was determined as being roughly the maximum acceptable considering system cost and complexity. The general hardware structure is shown in Figure 3. Each charge-discharge module contained a programmable constant-current generator utilising precision components so that currents were defined to good accuracy and stability; the high accuracy of the generators was beneficial to accuracy of results and the high stability removed any necessity for regular recalibration. Each module also contained a four-pole relay by which the cell/battery associated with the module could be connected to any remote measurement instrument for a four-terminal type measurement enabling high measurement accuracy. The constant-current generators were designed to have a very high output impedance so that the presence of a generator circuit in parallel with a cell/battery would not invalidate results of impedance measurements done on that battery; measurements could be taken whilst zero current, charge-direction d.c. currents or discharge-direction d.c. currents were being passed through a cell/battery. In practice a reed-relay was provided on each charge-discharge board which enabled the constant-current generator to optionally be completely isolated from its associated cell/battery. The design of the hardware was very thorough and many protection and safety features were included. The reader should consult Chapter 6 for more detailed information on the charge-discharge hardware.

Requirements and Choices Relating to Measurement Methods

An appraisal was made of various commercially available instruments for purposes of impedance component measurement. Instruments

employing Fast-Fourier transform methods were considered too expensive for purposes of the investigation and most had low frequency limits well above the region of interest. Available contemporary instruments employing sinewave excitation, which included bridges and transfer function analysers, also had inappropriate frequency ranges. A Hewlett-Packard 3575A "Gain/Phase Meter" was considered since, in conjunction with a sine source, this instrument is capable of measuring gain and phase response at frequencies down to 1Hz. However, the 3575A is a broadband detector and has settling times at low frequencies that are too long (20 seconds for 1-10Hz) for use in a highly multiplexed system such as was envisaged for the battery test rig.

A decision was consequently made that a customised impedance meter would be built which would be optimised for use with Ni-Cd cells and batteries. A cell or battery to be tested would be subjected to current-mode excitation, meaning that a precisely defined time-dependent current would be passed through it. The voltage perturbation developed across test devices would be detected and analysed by suitable hardware and software (The simple impedance theory associated with this method is outlined in Appendix 2). The excitation waveform was chosen to be a standard sinewave in precisely defined integer-number-of-cycle bursts.

The use of voltage excitation was considered impractical since Ni-Cd cells/batteries have a non-zero quiescent terminal voltage which, unless excitation hardware is made very complicated, demands that cells/batteries be capacitor-coupled to a voltage generator. Unfortunately, capacitor coupling introduces problematic time-constants for settling and is generally not viable for excitation frequencies in the sub-1-Hertz region. The use of sinewave bursts which amounted to single cycles at the lowest measurement frequencies, as opposed to "continuous" sinewave excitation, was required in order to minimise the time duration

of individual measurements. However, although giving results which are repeatable for an invariant test device and which should be meaningful, the burst excitation method does not necessarily deliver accurate impedance-component values (This point is mentioned again in Chapter 6 and is discussed in more detail in Appendix 3).

Of various sinewave generation methods considered for the sinewave generator a digital synthesis method involving an EPROM "lookup" table and a digital-to-analogue converter was chosen. This method is capable of giving virtually perfect phase definition and, by using small digital quantisation steps both for time and instantaneous-amplitude, a sinewave of high harmonic purity can be generated without a necessity for explicit filtering. The use of filters was considered undesirable since it would have added to the complexity of the design process and since filtering might lead to frequency-dependent phase and amplitude errors. The "sinewave" generation method adopted was flexible in that a large variety of symmetrical or asymmetrical waveforms could be produced if desired via appropriate EPROM programming.

The selection of frequency range for the customised impedance measurement instrument was not particularly difficult. Since many Ni-Cd cells and batteries begin to exhibit inductive behaviour above, very roughly, 100Hz and since inductive effects depend more on the geometrical considerations of cells/batteries than on electrochemical factors then there was little point in making special efforts to produce frequencies above this range. The lower sensible frequency limit was thought to be about 0.1 Hertz for hardware-related reasons. A measurement at 0.1 Hertz requires a theoretical minimum time duration of 10 seconds. It was realised that many-second measurements could easily be spoiled by drifts in the precision measurement hardware caused by temperature changes or by effects within Ni-Cd cells/batteries involving long time constants.

Furthermore, considering that the research cell/battery test rig was highly multiplexed, the cumulative result of many many-second measurements could be so long as to make sensible programming of the rig operations and sequencing difficult. In practice, a frequency range of $^1/_{12}$Hz to 128Hz was chosen which encompassed the desired frequency range and was fairly convenient from the point of view of ease of digital and analogue design.

For purposes of measuring cell/battery response to excitation an analogue-to-digital conversion method was used. The hardware developed included a preamplifier stage, a stage for nulling out the d.c. component of cell/battery terminal voltage, a final amplifier and a high resolution A-to-D converter. The d.c. voltage nulling was achieved by including in the signal amplification chain a true-differential amplifier having its spare input connected to the output of a programmable D-to-A converter. The measurement instrument outputted raw results in digital form for analysis by computer.

For purposes of analysing cell/battery response a phase-sensitive detection method was chosen, being implemented in a software form (The simple theory of the phase-sensitive detection method is outlined in Appendix 2). An alternative approach would have involved a Fourier transform technique, such as the calculation method known as the Fast-Fourier transform (F.F.T.) which is often applied in practical instrumentation. However, a F.F.T. method would have been vulnerable to noise problems unless large sample numbers had been used to eliminate aliasing of the lower noise frequencies. The sample number and resolution of measurements from the customised impedance meter were far too high for a complete F.F.T. algorithm to be applied to a full sample set without consuming an extremely excessive amount of computer time and memory; Such an algorithm would have wasted resources in producing a large amount of superfluous, worthless data relating to high-harmonic frequencies. A

software implementation of a phase-sensitive detection algorithm was eventually devised which utilised a full set of sample results, so as to maximise noise rejection, and was speedy and compact. The phase-sensitive detection method has an additional advantage over Fourier transform techniques in that it can be implemented easily in an analogue hardware form capable of giving very accurate results (This approach was used in the J.P.B./U.C.S. Charger - See Chapter 13).

The reader is referred to Chapter 6 for more details of the measurement hardware and to Chapter 7 for more details on the adopted phase-sensitive detection data analysis method.

Points Relating to Choice of a Test System Controller Computer

A B.B.C. Microcomputer, initially a Model "B", was chosen as a controller for the complete test rig for various reasons which are listed as follows. This machine is equipped with a variety of hardware interfaces including a near-direct interface with the microprocessor bus. The R.O.M.-resident language, B.B.C. BASIC, is reasonably powerful and well structured and provides easy access to a multitude of machine-specific hardware and software features, including a software clock. As B.B.C. BASIC is (primarily) an interpreted language, programs are easy to test, correct and modify. The interpreted nature of the language is most beneficial from the point of view of hardware control since it provides for "hands-on" control via the typing-in of commands and program lines for immediate interpretation (as opposed to instructions as part of a listable program). The language includes a 6502 machine code assembler and freely enables the use of machine-code routines within B.B.C. BASIC programs; it was realised that this facility could be used for speeding up the more

time-critical functions of the control software for a cell/battery test rig. Furthermore, it was noted that upgrades for the B.B.C. model "B" were available and could be used if the computing power of the basic machine proved to be inadequate.

Computers of the I.B.M.-"P.C." compatible type were given serious consideration as alternative controller computers which would have provided more memory and processing power. However, such machines available at the time in an acceptable price range tended to lack those resident hardware and software features, present within the B.B.C. microcomputer, that were most valuable for the Author's purposes.

General Software Requirements and Choices

It was realised that most, if not all, of the software for system control and data analysis would need to be custom written due to the unique nature of hardware and data formats required for research purposes.

The primary requirement for software was a customised program suite for control of the test rig hardware. It was envisaged that the programming system would be developed over the course of time and would involve a highly modular format. At the highest programming level a need existed for a program structure for control of non-measurement operations including charge-discharge current control; this structure was named the "RUN-control" structure/program. A second structure/program was required for control of measurements. Incorporated within a typical RUN-control structure would be a procedure monitoring and utilising a time-clock for operation timing; procedures controlling the timing and sequencing of charge-discharge operations and of other operations, including measurement requests; procedures performing updating of charge-discharge currents;

procedures enabling manual override of pre-programmed settings; and procedures, involving run-time decision-making, for monitoring and preventing cell/battery overvoltage and overdischarge. Incorporated within a typical measurement-control structure would be procedures for sequencing measurement hardware programming and relay operations; procedures for selection of measurement types and parameters, either from pre-programmed tables or via run-time calculations and decisions based on results from preceding measurements; procedures for results analysis; and procedures for outputting of results to media such as the computer V.D.U. and floppy disk. An additional and very important requirement existed within the hardware control software for an extensive system of error trapping which would allow automatic controlled hardware shutdown upon occurrence of serious program errors, program data errors and other run-time errors.

In practice, and largely due to computer memory restrictions the RUN-control and measurement-control structures were configured as separate programs which would load and run (CHAIN) each other alternately during test rig operation in order to perform the full range of necessary operations. A "RUN-control" program remained responsible for the system clock and its associated operation timings and control was passed temporarily to selected "measurement(-control)" programs at intervals.

The reader should note that the system software was written in a highly modular form but that many of the modules were selected and customised to suit particular experiments. Most software programs and modules were highly language-specific and made use of the advanced commands of the B.B.C. microcomputer. Consequently, no attempt is made in this document to describe the system software in a complete form. However, Sheets 3(a,b) contain flowcharts, respectively, for a RUN-control and a measurement program outlining entry and exit routes, typical main program parts and operation sequencing.

A secondary software requirement, associated with the research programme, existed for a collection of customised programs for such purposes as generation of programming data, testing of system operation and performance, plotting of results in graphical form and for analysis of results in a useful manner. A sizeable suite of programs was eventually developed for these purposes.

The reader can acquire more insight into specific program operations from the example program listings included in the Appendices and from the detailed software descriptions contained in Chapters 7 and 8.

Miscellaneous Problems Encountered Relating to Test Rig Development

Much custom support hardware and software had to be created for the research programme, which proved to be a lengthy and difficult task due to the physical size and complexity of the system. The reader should note that discussions of hardware and software that follow in later Chapters relate, except where stated, to final versions and that many modifications and upgrades were undertaken during the course of the research programme.

Frustrating problems were encountered with the test rig hardware involving intermittent glitch failures and interference. For construction of hardware to sufficiently exacting standards the departmental technical support facilities proved to be inadequate and the Author felt compelled to do much of the work involved. The system software was written with fairly comprehensive data-checking and error-handling procedures and was reviewed and upgraded from time to time. The choice of a B.B.C. Model "B" microcomputer for a system controller turned out to be a reasonable one although the hardware interface did not operate as smoothly as was

desired, in part due to doubtful bus timings in the computer. A BASIC/6502 machine-code program environment proved to be sufficiently flexible but problems were encountered with regard to computer memory size and some time was wasted in attempts to create workable unified test programs. Eventually, a method was adopted in which test programs were split into manageable smaller units involving the separation of measurement control functions from other control functions (as mentioned earlier). The acquisition of a B.B.C. "Master" microcomputer during the main stages of the research speeded up programming considerably due to its extended facilities; however, this machine proved to be inadequate for analysis of data from the test rig and, so as to maintain downward compatibility but to increase program speed at least tenfold, an innovative Acorn "Archimedes" microcomputer was later utilised.

Concerns Known to be Interested in the Research

Since the Author was pursuing a research programme which was aimed ultimately at the development of practical battery charging and analysis methods, efforts were made to identify potential users of end results. Two major organisations that were found to be interested in charging and monitoring methods for Ni-Cd batteries were the (U.K.) Home Office Directorate of Telecommunications and British Gas p.l.c., both of which had some involvement with the Author's study. The British Armed Forces were also known to have interests in this field and in early 1990 an enquiry was expressed by British Aerospace in connection with the use of Ni-Cd storage devices in satellites.

The Home Office Directorate of Telecommunications was once responsible for providing personal radio communications handsets and the Ni-Cd batteries that these require to the British Police Force; the

Directorate nowadays has more of an advisory role. The Police Force has several tens of thousands of radio handsets of various types in field use and, with observed battery lifetimes being of the order of one year, this results in over one hundred thousand batteries being purchased per annum. Considering that batteries cost £10-£30 per radio, dependent on type, the total cost to the British Police Force for batteries is of the order of £2,000,000 per year. A strong incentive obviously exists for improving the lifetimes of such batteries and it has been realised that the adoption of improved charging methods is very important in achieving battery longevity.

Many Police batteries are currently charged using timer-controlled dump-charge chargers, the most recent of which operate on an 8-hour cycle so as to fit in with the standard 8-hour shift-work system. It has been mentioned earlier (in Chapter 3) that dump-charging of multi-cell Ni-Cd batteries is potentially very detrimental to batteries as it is liable to cause reverse-charging of some cells. It is interesting to note that advice has been given to some regional Police forces to modify existing dump-chargers so as to bypass the "dump" phase. The British Police Force over recent years has been converting from radios manufactured by Burndept, which use batteries based on mass-plate cells, to radios manufactured by Storno, PYE and Motorola, which use batteries based on sintered cells. It was initially thought that batteries based on sintered cells could be expected to last considerably longer than mass-plate types but experience so far with PYE "P.F.X." 8-cell batteries has shown this not to be obviously the case; it seems possible that the common usage of dump-charging methods may be a contributory factor.

It should be noted that the Home Office does not have a general requirement for particularly fast charging of batteries since an 8-hour charging period is tolerable for standard Police shift-work situations. In

some working situations there may be a need for batteries to be charged more quickly but it should be borne in mind that faster charging generally results in shorter battery life. An interesting point is that the Home Office, in the past, has tested a battery charger claimed to utilise capacitance measurements and found it to be no more effective (The precise details are unknown to the Author) than conventional methods.

British Gas p.l.c. has a requirement for Ni-Cd battery packs in devices known as "P.I.G.'s" which are used to inspect gas mains for defects. A P.I.G. is a vehicle of cylindrical shape incorporating a flexible skirt which is inserted into a gas main at a convenient point and forced along the main by externally controlled gas pressure. A P.I.G. has no hard-wired interface to the external world and thus requires batteries to operate the electrical and electronic hardware which it contains. Current P.I.G.'s utilise battery packs in which several size "F", 7Ah SAFT cells are wired in series. British Gas considers that a state-of-charge measurement device would be very valuable for use with P.I.G. batteries. Since the number of P.I.G. battery packs in field use around the World is of the order of fifty, a state-of-charge indicator device could feasibly be installed permanently within each P.I.G.; furthermore, the concept of a battery charger/monitor capable of recognising individual batteries might be practical in this application. British Gas also has interests in the fast-charging and topping-up of battery packs for reasons of operational convenience; for this purpose a means for determining battery end-of-charge is desirable. Unlike the case of the Police Force, the interests of British Gas lie almost entirely in short-term considerations of usage convenience of Ni-Cd batteries rather than including long-term considerations relating to extension of battery lifetimes.

CHAPTER 6

The Research Cell/Battery Test Rig Hardware

The hardware for the research cell/battery test rig comprised three main parts, namely a charge-discharge (cycling) rig, a unit providing an interface with the B.B.C. microcomputer (plus additional important functions) and a cell/battery complex-impedance meter.

The Cell/Battery Charge-Discharge Cycling Rig and General Rig Busing Arrangements

The battery cycling rig took rather longer to set up than expected and was not fully assembled until May 1988 although experimental usage began, with 8 of the rig's intended 48 "Charge-Discharge" modules operational, in April 1987. Fig. 3 shows the general architecture of the whole test rig and Plate 1 is a photograph of the entire setup.

The rig contains 48 "Charge-Discharge" modules (or "boards") mounted on a timber rack. The modules are linked via a power bus to various power supplies; via the slow "Ch-D-Logic" bus to supervisory hardware and the controller B.B.C. microcomputer; and via the analogue "Cell-Access" bus to the impedance-measurement instrument. Each Charge-Discharge module is constructed on a 5 inch square, single-sided printed circuit board and contains a cell holder, with provision for connecting to external cells/batteries with flying leads; a programmable constant-current generator; a four-pole relay; and support circuitry. Each module can be individually programmed by the microcomputer for charge or discharge current over periods of hours or even days. The cell/battery to which any module is assigned can be linked, via the module's four-pole

relay, to the Cell-Access bus at programmed intervals so as to allow measurements to be taken on that cell/battery. The Cell-Access bus is a four-conductor bus comprising an "Excitation" bus and a "Response" bus which enables the use of a four-terminal measurement strategy to prevent errors arising from lead resistances and self-inductances.

Fig. 4 shows the general layout of a Charge-Discharge "Board-Carrier" which is designed for simplicity and reasonable ease of access. This diagram also shows positions of some parts associated with Board-Carriers and Ch-D modules. The most critical feature of the Board-Carriers is the Response bus which needs to be well balanced in terms of lead resistance; of low mutual inductance with the Excitation bus so as to minimise stray signal transfer; and of low mutual inductance with respect to power rails so as to minimise pickup of possible interference. The Excitation bus is required to carry alternating currents of up to a few hundred milliamps and had to be constructed so as to generate minimal external magnetic fields. A twisted pair of fairly heavy gauge wire was chosen for the Response and Excitation buses aboard the carriers. The power rails, although preferably kept in a close bundle to minimise lead inductances, had to be spread out to allow connections to be made reliably via solder joints.

Each Charge-Discharge Board-Carrier is provided with a supervisory printed circuit board containing an array of power rail fuses and a voltage reference unit. Each reference unit supplies a stable voltage of 1.35 Volts to a twisted-pair bus on its Board-Carrier. Fig. 5 shows the layout and circuit of a Fuse/V_{REF} board and Plate 2 shows a photograph of a board.

The circuit for a Charge-Discharge module, of which there were 48 in total, mounted 8 per Board-Carrier on each of six Carriers, is shown in Figs. 6(a,b). With reference to these diagrams the following notes are

given:-

- All logic devices are HCT-series CMOS for ease of interfacing.
- "α", "β" and "γ" symbols refer to "Power", "Logic" and "V_{REF}" grounds respectively. A comprehensive grounding scheme was employed to minimise interactions between power, logic and V_{REF} buses.
- "V_{REF}" is provided by the Board-Carrier 1.35 Volt reference bus.
- The '573 transparent latch is programmed with data from the Ch-D-Logic bus.
- The quasi-complementary-current output DAC (Precision Monolithics DAC-312FR) and the current amplifier stage (utilising OP-07CN operational amplifiers) constitute a precision bi-directional current generator having a high (voltage-) compliance output. With the current sensing resistors connected in series the output current range is -160 to +157.5mA. With a single resistor used the range is -320 to +315mA. With resistors connected in parallel the range is -640 to +630mA.
- The "100k" trimpot shown in Fig. 6(a) is for current generator f.s.d. adjust and the "20k" trimpot shown in Fig. 6(b) is for zero adjust.
- Note that the lowest values shown for certain supply voltages in Figs. 6(a,b) are correct for a test cell of nominal voltage 1.25V and that for testing batteries of higher voltage some of the positive-side voltages may need to be increased.
- The 12-bit DAC has differential nonlinearity of 1 LSB, integral nonlinearity of 0.05% f.s.d. and temperature coefficient of 40 p.p.m. maximum. The OP-07 operational amplifiers have input offset voltage drifts of less than about 2μV/°C. The precision resistors are of 0.1% tolerance and 15 p.p.m. maximum temperature coefficient. These specifications may seem excessive but, after a calibration at 25°C for full-scale and zero currents, the resulting accuracy for current generator output over a temperature range of 0°C to 50°C is theoretically about +/-3% worst-case

for currents of $^1/_{20}$th f.s.d., decreasing to about +/-0.5% for full-scale currents. The accuracy is such that the tolerances in individual charge-discharge modules can be safely ignored when performing precision charging and discharging of cells and batteries. Furthermore, the use of high grade components should ensure that the test rig will operate for periods of months or years without need for recalibration.

- The current generator as a whole operates as a bidirectional D-to-A converter with 7-bit 2's-complement binary control. A coding table is shown below:-

Input Code	Output Current
0111111	V_{FS+}-1LSB
0111110	V_{FS+}-2LSB
⋮	⋮
0000001	+1LSB
0000000	(ZERO OUTPUT)
1111111	-1LSB*
⋮	⋮
1000001	V_{FS-}+1LSB
1000000	V_{FS-}

(where "FS" = "full-scale" and "LSB" = least-significant-bit of generator output)

- Note*: In practice, binary code 1111111 results in zero generator output since it is detected by the 7-input NAND gate and leads to opening of the reed relay. Code 1111111 is used to isolate a cell/battery completely from the current generator, for example, to avoid the output leakage currents that may be present in the 0000000-code state.

- The four-pole relay has reliable gold-flashed contacts and is controlled by a (dual-NOR-gate) flip-flop. An individual relay is closed by application of a positive-going pulse via an appropriate logic bus line. A relay is opened by application of an extended positive pulse to

the "Reset" input. It should be noted, though, that all Charge-Discharge modules in the Ch-D rig share a single "Reset" line.

- In general, connections made to cells and batteries are in four-terminal format; this may be accomplished either via customised cell/battery holders or by flying leads.
- Each Charge-Discharge board is provided with two l.e.d. lamps which indicate the status of the relays. (the resulting "light show" of the operational rig makes it quite entertaining to the layman!)
- The resistor/capacitor/diode network surrounding the Reset input provides a local reset function upon +5V line failure or powerup and also provides some e.s.d. (electrostatic discharge) protection for the CMOS logic.
- The resistor network surrounding the latch Enable input slows down its response to bus control signals and provides some e.s.d. protection for the CMOS latch.
- The "Current-Sense" line is an important safety feature. The four-pole relays of all Charge-Discharge modules in an assembled rig sink currents to a common Current-Sense line. By sensing the current at the ground-return end of this line it is possible to determine the number of four-pole relays activated at any time. It is most important, though, that no more than one relay is ever closed at one time since this would result in simultaneous connection of more than one cell/battery to the Cell-Access bus which could lead to uncontrolled current flow. In order to preclude this possibility, which might occur (and indeed has done in practice) via upsetting of hardware logic by glitch/interference effects, a supervisory circuit (namely the "Relay-Overcurrent" sensor installed in the "Beeb-Interface-Box" - see later) triggers an immediate Reset pulse if more than one four-pole relay becomes activated at any time.

The Beeb-Interface-Box

The "Beeb-Interface-Box" is a unit serving as a buffer and interface between the controller B.B.C. Microcomputer and external hardware. It primarily contains logic circuitry and, as fairly conventional techniques have been used, only its major functions will be described here.

- One purpose of the Beeb-Interface-Box is that of providing basic hardware buffering for the 1MHz bus in order to avoid excessive loading of, and to give some degree of fault protection for, computer internal hardware. The impedance measurement hardware is connected to the 1MHz bus via this buffering.

- A second function of the Beeb-Interface-Box is that of providing the address and data lines of the Ch-D-Logic bus for Charge-Discharge modules. An address decoder is included which has 128 mutually exclusive outputs corresponding to addresses (in hexadecimal) FC80 to FCFF in the controller computer memory map. Address outputs FC90 to FCEF are used for Charge-Discharge module control (2 lines per module) and other outputs are available for other purposes. Initially, attempts were made to connect Charge-Discharge modules directly onto the buffered 1MHz data bus in order to program their '573 latches but the resulting system proved to be somewhat unreliable, especially as individual bus lengths exceeded two metres. After unsuccessful experimentation with different bus configurations and terminations it was decided that the Charge-Discharge bus between the Beeb-Interface-Box and the Charge-Discharge module array had to be slowed down. Consequently, a write-only bus driver system incorporating latches (See Figs. 7(a,b,c)) was installed in the Beeb-Interface-Box enabling data and address pulses to be extended considerably. In the eventual configuration the Charge-Discharge bus

timings were as follows: data-valid time = 60μs, (mutually-exclusive) address pulse time = 30μs.

- The Beeb-Interface-Box contains the "Reset" unit (See Fig. 8) which outputs a 1.5 millisecond positive-going pulse to the Charge-Discharge module Reset line whenever memory location (hexadecimal) FCFE (in computer mapped memory) is addressed. A "Reset" pulse is also generated when the 1MHz bus Not-Reset line goes low (as on computer power failure or manual reset via the "BREAK" key) or whenever the Relay-Overcurrent sensor is triggered.

- The Beeb-Interface-Box contains the Relay-Overcurrent sensor (outlined earlier - See Fig. 8) which is based upon an operational-amplifier and is linked to the Reset unit.

- The Beeb-Interface-Box also contains the "Power-Crash" protector (See Fig. 9), the primary function of which is to partially deactivate all Charge-Discharge modules upon the occurrence of certain power failures, whether momentary or extended. The protector behaves in a similar manner to "No-Volt-Release" systems used with industrial machine tools to prevent uncontrolled restarting upon reinstatement of power after a failure. It is conceivable that after certain power failures the Charge-Discharge module '573 latches may be programmed incorrectly or that the computer software may have lost control of the hardware. The protector also provides a partial emergency shutdown facility via the B.B.C. Microcomputer "BREAK" key. The Power-Crash protector manages a latched relay which delivers +12 Volt power, via the Power bus, to the Charge-Discharge modules. The relay is set closed only when the hardware Reset address (hexadecimal) FCFE is accessed by the controller computer. The relay is set open upon any of three possible fault conditions: namely failure of the +5 Volt power supply (which powers virtually every logic device in the hardware); failure of the B.B.C. Microcomputer power supply (which results in the

computer Not-Reset line going low); and pressing of the computer "BREAK" key (which also causes the Not-Reset line to go low). Note (!) that unless a +12 Volt supply with high current surge capability is used or the Power-Crash-Protector 12 Volt supply is well decoupled then the unit will need an independent +12 Volt power supply (since closing of the relay leads to a high initial current surge which can crowbar the +12 Volt rail sufficiently to stop the relay from holding closed - the relay then has a tendency to behave as a mechanical buzzer!).

The Ni-Cd Cell/Battery Complex-Impedance Meter (Sinegenerator - Detector Unit - Control Board)

Assuming the representation of a Ni-Cd cell/battery for d.c measurement purposes as a simple source of e.m.f. with internal resistance and for a.c. measurement purposes as a series combination of resistance and capacitance a highly stable resistance-capacitance measurement instrument was devised and built, largely during the second year of the research. The instrument was tailored to meet the specific requirements of Ni-Cd cells/batteries, unusual in that impedances in the range of tens of milliohms were common and in that d.c. terminal voltages of magnitude 1000 times that of a.c. perturbation voltages had to be coped with. The measurement instrument is fundamentally a complex-impedance meter using the phase-sensitive-detection technique. It includes a high-purity sinewave current source for purposes of excitation, and a response-voltage processor capable of nulling out battery d.c. voltages and having a 14-bit digital output (See Appendix 2 for a discussion of relevant aspects of the theory of the current-excitation complex-impedance meter). The system-controller B.B.C. microcomputer forms an integral part of the impedance meter and the measurement programming, autoranging and phase-sensitive-

detection functions are provided by purpose-written software. In order to take measurements in the shortest possible time, which is essential when an impedance-measuring instrument is multiplexed to a large number of test cells/batteries, the excitation sinewave is applied in controlled bursts. Mathematical purists might complain that the resulting measurement is not generally a pure single-frequency one (See Appendix 3 for a discussion of this) but the important point is that fast, reproducible results can be obtained. The instrument was designed so as to take four-terminal measurements on remote devices and has differential input and output coupling in order to reduce common-mode voltage problems.

The impedance meter hardware was constructed in three distinct parts, the "Sinegenerator" board, the "Detector" unit and the "Control" board which are described in the following sections:-

The Sinegenerator Board

Sheets 1(a,b) show the circuit for the sinewave excitation-current generator, the "Sinegenerator", which was built using the wirewrapping technique on a double-Eurocard size, g.r.p., square-pad prototyping board. It includes a digital, EPROM-based sine synthesiser; a programmable attenuator; and a complementary-current-mode power output stage. As it was thought that the Sinegenerator might be used in experiments involving measurements of harmonic-generation in test cells/batteries it was designed to produce very low sine distortion. The Sinegenerator is a self-contained unit and has the following specifications:-

Frequency - $^1/_8$Hz to 8Hz in binary-weighted sequence : one cycle of sinewave produced when triggered

- $^1/_{12}$Hz to $5^1/_3$Hz in binary-weighted sequence : one cycle of

sinewave produced when triggered

- 16Hz to 128Hz in binary-weighted sequence : 2,4,8,16 cycles respectively produced when triggered (sine burst thus lasts $^1/_8$ second)
- $10^2/_3$Hz to $85^1/_3$Hz in binary-weighted sequence : 2,4,8,16 cycles respectively produced when triggered (sine burst thus lasts $^3/_{16}$ second)

Amplitude - 8 output levels coded "0-7" in binary-weighted sequence : highest range ("7") has output current of 247.5mA r.m.s. (350mA peak) : lowest range ("0") has output of 1.933mA r.m.s.

Distortion - Very low : measured using a total-harmonic-distortion meter with various resistor and Ni-Cd cell loads as less than 0.02% for all excitation frequencies at amplitude levels "0-5"

With reference to Sheets 1(a,b) the following notes are given:-

- The Sinegenerator has a stable 2^{21}Hz crystal master oscillator which is divided down by a factor of 8 for frequencies in the sequence $^1/_8, ^1/_4, ..., 128$Hz and by a factor of 12 for frequencies in the sequence $^1/_{12}, ^1/_6, ..., 85^1/_3$Hz.
- The pre-divided master clock signal is fed into two binary divider chains. A 4-divider chain provides the "Not-Convert" signal which is used to clock external Detector unit hardware. A 10-divider chain plus logic gates forms a programmable binary-weighted frequency divider for frequency selection.
- The square wave output from the main frequency divider is fed into an 11-stage counter which acts primarily as a sequential address counter for the 2048-byte EPROM.
- The EPROM is pre-programmed with binary data describing one full cycle

of a sinewave. Circuitry associated with the EPROM is quite complex, requiring four latches with three clock signals ("2Clk","Clk","Not-Clk"), because sinewave data is stored as 12-bit words in the 8-bit EPROM by means of consecutive 2-byte blocks in {low-byte},{high-byte} format.

- As the address counter counts up from zero (00000000000) to its maximum count (11111111111) one whole cycle of sinewave is synthesised, after which the address count returns to zero. A chain of 5 dividers beyond the final address-counter divider combined with additional logic forces the Sinegenerator to cease sinewave production after an integer number of cycles. The number of cycles allowed is dependent on the measurement frequency and is selected automatically by the hardware.
- Due to a need for exactly repeatable excitation signal bursts, the Sinegenerator was designed so as always, when triggered, to produce a sinewave starting at a fixed phase angle in its cycle (relative to a true sine wave starting at the time origin) and to end at that same phase angle after an integer number of cycles.
- The start phase angle is determined by EPROM programming and was chosen as 0 degrees nominal as this is ideal for excitation of series R-C combinations (See Appendix 3). For zero start phase angle, the first word in the EPROM (held in address locations {00000000000},{00000000001} should nominally be the word representing the zero instantaneous-amplitude of the sinewave at the origin. However, the generation of a sinewave from such data in a stepwise fashion leads to an effective retardation by half of a sample time relative to the Not-Convert output and other synchronisation outputs. This problem can be eliminated by adjusting the effective phase of the sinewave data (or possibly by modifying the hardware, though this was considered undesirable). With a sinewave generated via 1024 samples the retardation amounts to a phase lag of -0.176° which is not particularly serious.

- In practice, as hardware systems involved in the whole measurement system were likely to introduce an effective phase lag error between sine synthesiser and detector, it seemed sensible to program the EPROM with sine data advanced by one sample from nominal zero-phase in order to achieve a degree of compensation (This was done since an appropriate data file was at hand at the time though, in retrospect, half-sample-advanced data might have been used for virtually perfect results). Address locations {00000000000},{00000000001} (binary) thus contained a word representing the first non-zero sinewave sample and locations {11111111110},{11111111111} (binary) contained a word representing the zero instantaneous value of the sinewave at the end of its cycle. The sinewave was thus synthesised with an initial phase lead of 0.176° (+0.0031 Radians). It was thought unlikely that Ni-Cd cells/batteries would produce phase shifts of less than 10° so that the resulting error in phase measurement would be less than 1.76%. This was considered good enough especially as compensations could be made in final calculations if necessary.

- The EPROM contains sinewave word data in sign-plus-11-bit-magnitude form (magnitude stored in D0-D11 and sign in D12). The digital output of the EPROM-latch arrangement is fed into a composite digital-to-analogue converter.

- The composite digital-to-analogue converter comprises a (Precision Monolithics) PM-562 DAC operated, with an OP-07 op-amp, as a unidirectional 11-bit voltage-output DAC followed by a switched-resistor attenuator and an analogue-switch bridge.

- The DAC-op-amp output is switchable via a reed-relay to two values mutually weighted by a factor of two. With the EPROM programmed for sinewave generation, the output waveform is in the form of a full-wave rectified sinewave.

- The switched-resistor attenuator, containing reed-relays and 0.1% tolerance resistors in a compact array, provides programmable voltage division by factors of 4 to 64 in a binary-weighted sequence.
- The analogue-switch bridge (using a Precision Monolithics SW-201 quad S.P.S.T. F.E.T. switch configured as a D.P.D.T. switch) conveys its input signal to one of two outputs in alternation at a rate determined by the "Sign" signal on line D12. For sinewave generation D12 carries a square-wave at the fundamental frequency and hence the two switch bridge outputs carry half-wave sine pulses in mutual alternation.
- The output from the analogue-switch bridge is fed into a power V-I converter arrangement. The converter requires true-differential inputs in order to realise a sinewave output. In practice, two identical V-I converter circuits were used since complementary outputs were desired; complementary operation was achieved with ease by connecting converter inputs in mutual antiphase to the switch bridge output.
- The AMP-01 differential input/output amplifier proved to be an ideal device for constructing the power V-I converters as at has high-current +/-50mA output drive capability and high linearity. Precision resistors were used throughout to ensure stability of performance over many months or years.
- The output stage has high (voltage-) compliance outputs. Note that the positive supply voltage shown may be raised as high as 18 Volts in order to deliver excitation currents into many-cell batteries.
- The purpose of generating closely matched but mutually inverse current outputs is to allow an excitation signal to be sent 'cleanly' down a few metres of coaxial or balanced line to a test cell/battery in a setup where the cell/battery shares an external (power) ground line with the Sinegenerator. The complementary drive constrains virtually all of the excitation current to flow within the intended cable; hence, magnetic

field generation and ground-loop effects are minimised. It is inevitable that some excitation current will be present in the external ground line due to inaccuracies in V-I converter matching; however, the residual current will normally be of a trivial magnitude.

- Note that the nominal "Sinegenerator" is very versatile in that, by fitting EPROMs with different programming, bursts of virtually any waveform of any phase relationship can be produced.

The Detector Unit

The Detector unit is a 222mm by 146mm by 106mm die-cast metal box containing a purpose-designed voltage processor system. The box provides overall screening and environmental protection and helps to maintain a stable ambient temperature for the precision electronics involved. The Detector unit is intended to be integrated with dedicated hardware and a microcontroller (in this case a B.B.C. microcomputer) since a sequence of programming operations is required in order for it to return sensible data.

In its "D.C." mode the Detector measures the terminal voltage of a cell/battery connected, in practice via the Response bus, to its input. In the "A.C." mode a voltage generator internal to the Detector is programmed so as to compensate for cell/battery d.c. terminal voltage; the gain of the Detector is then increased by a factor of 200 and perturbations in the d.c. terminal voltage can be measured. The Detector contains a 14-bit, digital output "Analogue-Data-Acquisition-Module" (A.D.A.M.) which in detector A.C. mode is run continuously at high speed with output samples being sent to (external) electronic memory. Voltage perturbations across a cell/battery are thus recorded in digital form over a period of time.

A major consideration for the Detector analogue circuitry as a

whole was that drifts in resistor values and in semiconductor offset voltages had to be kept to an absolute minimum since the Detector was being designed to cope with signals of amplitude of a few millivolts at frequencies down to $^1/_{12}$Hz. At $^1/_{12}$Hz, for example, an impedance measurement operation will take at least 12 seconds during which time a drift in Detector offsets may have occurred which could contribute an error term to final impedance results. Such errors are very hard to analyse and it was considered that careful circuit layout was required with special attention paid to thermal effects.

The Detector was constructed using two circuit boards (modified g.r.p., square-pad prototyping boards) by a hybrid of wirewrapping and hard-wiring techniques. The smaller of the two boards, which contained the bulk of the analogue components, was housed inside a sealed 114mm by 64mm by 55mm die-cast alloy box (within the larger box) in order to guarantee freedom from short-term temperature fluctuations, as might be caused by air draughts in the laboratory environment, without resorting to oven techniques.

The main specifications of the Detector unit hardware are as follows:-

d.c. measurement ranges - ("2-Volt" range) -2 to +2 Volts
- ("14-Volt" range) -14 to +14 Volts

d.c. nulling capability - ("2-Volt" range) -2 to +2 Volts
- ("14-Volt" range) -14 to +14 Volts

a.c. measurement input - ("2-Volt" range) max. 10mV pk. a.c.
- ("14-Volt" range) max. 70mV pk. a.c.

Figs. 10(a,b) show (most of) the circuitry contained within the Detector unit; with reference to these diagrams the following notes are given:-

- The Detector is connected to test cells/batteries via the Response bus

which is constructed from twisted-pair cable for low noise pickup. The Response bus resident on Ch-D Board-Carriers is plain twisted-pair but the wiring harness which connects the Detector with the Carriers comprises an individually-shielded (screened) twisted-pair arrangement in which the shields are actively driven from their respective signal lines. The bootstrapping of shields effectively eliminates the capacitance between the signal lines and the surrounding environment and removes problems of asymmetric signal pickup that might occur, even with a twisted-pair arrangement, if the cable, being flexible, came into close proximity with a conductor carrying a.c. voltages. (The normal justification for individual shield drivers, namely that of eliminating inter-conductor capacitances is not too important here due to the low frequencies involved and the very low impedances of Ni-Cd test cells/batteries. A system employing a twisted pair with an overall screen actively driven at the average of the input voltages could have been used. However, appropriate cable, of the type used in professional "balanced microphone" applications, was not available to the Author at the time of construction). The choice of OP-07 op-amps for shield drivers may seem strange but these devices are more suitably compensated and have a larger guaranteed output voltage swing than many common op-amps.

- The Response signal is fed initially into a Burr-Brown 3627BM true-differential input amplifier in order to eliminate ground-loop problems between test cells/batteries and the Detector, which are connected via long power ground lines to commoned power supplies. The 3627 contains a high grade op-amp and precision resistor network configured for unity voltage gain. The input impedance is rather low at 25kΩ but this is not too important considering that Ni-Cd cells to be tested generally have impedances of less than 1Ω. The resistor network of the 3627 is trimmed for 100dB common-mode rejection (at 25°C); a source imbalance of about

2.5Ω will reduce this to 80dB, which is tolerable in most situations envisaged. The 3627 has advantages over 3-op-amp configurations of introducing lower noise and being able to accept input voltages as high as 16 Volts (with 18 Volts placed on the appropriate supply rail) without suffering non-linearity.

- Note that the 3627 "-15V" power rail may be adjusted to as low as -18V if Ni-Cd batteries of more than about 7 cells are being tested.

- The output of the 3627 is taken to a switched-gain preamplifier providing gains of either 5 or $^5/_7$. A gain of 5 was optimum for single cells and a gain of $^5/_7$ was provided since it was thought in the first two years of the research that work would be required to be done with 7-cell batteries (7-cell Burndept radio handset batteries); work, however, was eventually done with 8-cell batteries but the hardware seemed to perform adequately. The resistors were 3 p.p.m. temperature-coefficient types and were cemented together onto a small heatsink in order to ensure the minimum possible drift of stage gain. It should be noted that during measurements of a.c. superimposed upon cell/battery d.c. a variation in gain over a period of time of the preamplifier will result in an apparent offset drift that could spoil phase-sensitive detection results. The switching relay, a 5-Volt-coil reed type, has mercury-wetted contacts for best possible stability of contact resistance. A further feature is a dummy load resistor, of resistance (nearly) equal to that of the relay coil, which is cemented to the relay body. When the relay is not activated a voltage of 5V is applied across the resistor. The heat dissipation of the relay-resistor combination is thus constant which aids temperature stability within the Detector.

- In Detector D.C. measurement mode the output of the preamplifier is connected to the input of the A.D.A.M. by closing analogue switch *"D"* (one of four in a Precision Monolithics SW-201) and setting the "A.C./D.C."

reed-relay to its "D.C." position. The "100R" resistor (plus analogue switch *"D"* resistance) and the "330n" capacitor provide a degree of low-pass filtering to reduce noise. During a d.c. measurement the switches *"A"* and *"B"* are held open.

- For an a.c. measurement a further amplifier stage is brought into use; this utilises a (Precision Monolithics) AMP-01 true-differential input amplifier. The voltage generator (See later) applies a stable voltage to the inverting (-) input of the AMP-01 that is equal, or nearly so, to the average d.c. voltage at the non-inverting (+) input. Analogue switch *"D"* is held open and the "A.C./D.C." relay is in its "A.C." position so that AMP-01 output is fed to the A.D.A.M. The AMP-01 is configured for a gain of 200 so that, provided that any residual d.c. potential difference across its inputs is less than about 50mV, it amplifies any perturbations in the voltage output from the preamplifier.

- A diode clamp is used across the AMP-01 inputs to protect this device from differential-mode voltages that could otherwise exceed 20 Volts.

- The Analogue-Data-Acquisition-Module (A.D.A.M.), an (Analogic Corporation ADAM-824) is a self-contained module comprising a sample-and-hold amplifier and 14-bit resolution A-to-D converter capable of operation up to frequencies of 20kHz. In the Detector unit the ADAM-824 is configured to operate linearly for inputs in the range -10V to +10V, for which it produces an digital output in 14-bit offset-binary form.

- Converter trigger signals and synchronisation functions are provided from an external Control board (to be discussed later). In Detector D.C. measurement mode the converter is requested to do a single measurement at a time (i.e. "one-shot" operation). In A.C. mode the converter is made to do a burst of 2048 measurements at a constant rate over a defined period of time. In practice, the 2048 measurements are done in simultaneity with application of a sinewave cycle/burst to a test cell/battery.

- The voltage generator is a composite sign-plus-12-bit-magnitude D-to-A converter based around a (Precision Monolithics) PM-562 DAC. Output polarity may be selected to be positive or negative through analogue switching (using three switches of four in a SW-201).
- The voltage generator, as a whole, operates as a D-to-A converter with offset-binary input coding. Positive outputs require the closing of analogue switch *"A"* only. For generation of negative outputs an op-amp inverter is included by closing analogue switch *"B"*, the data signals from D0-D11 are inverted (note that the logic i.c.'s used to do this are mounted on the Control board rather than in the Detector unit) and a necessary -1LSB output offset is added by closing analogue switch *"C"*.
- The voltage generator is designed for high stability and is supplied, via a buffer, with a 10 Volt reference voltage from the ADAM-824 module. High stability is required since reference drifts will interfere with a.c. measurements in a similar manner as will drifts in the preamplifier.
- Voltage accuracy and stability are worse for negative outputs than for positive outputs due to an extra inverter stage required. This, though, is not normally important since cells/batteries have fixed polarity in normal operation.
- The "3k3" resistor and the "330n" capacitor form a low pass filter of time constant about 1 millisecond which reduces voltage generator noise. The "3k3" resistor also serves an important function of limiting current flow if the potential difference between preamplifier and voltage generator outputs should exceed about 1 Volt when in A.C. mode.
- Note that the A.D.A.M. was later provided with a negative input voltage clamp comprising a zener diode, a diode and a current-limiting resistor; these are not shown in Figs. 10(a,b). The clamp was added several months after initial construction of the Detector since the ADAM-824 was found to generate a highly misleading output code for out-of-range input voltages

more negative than about -13V. The generation of such false outputs was undesirable since it made certain d.c.-null trimming and recovery operations impossible (See later Chapters).

The Control Board

The Control board is constructed on a double-Eurocard size, g.r.p., square-pad prototyping board using the wirewrapping technique and contains 42 logic i.c.'s, predominantly of the Low-power Schottky family, and two R.A.M. i.c.'s configured as 2048 bytes of 16-bit memory. The Control board acts as an interface between the buffered B.B.C. microcomputer 1MHz bus and the measurement hardware. Its primary function is that of supervision of the Detector unit, though the Sinegenerator is interfaced to the 1MHz bus via buffers and one latch residing on the Control board. Many of the fine details of gating and timing arrangements will not be described in this report as fairly conventional techniques have been employed. With reference to Figs. 11-15 which show the Control board electronics, and bearing in mind that a computer is required to operate the board, the following notes are given:-

- Fig. 11 shows the architecture of the Control board with buses shown and major component parts outlined.
- The interface with the external 1MHz bus (already buffered and having 8-bit data, 8-bit address and several control lines) is made via a controlled buffer/transceiver and a circuit which modifies "Read/Not-Write" line performance (See Figs. 13(i,iii)).
- The Control board has an internal 8-bit data bus from which four latches are programmed directly. The first is the "Frequency" latch which has an identical (computer memory-map) address to the programming latch of the Sinegenerator board. The second latch is the "Detector" latch which allows

programming of Detector unit 2V/14V status; A.C./D.C. status; A.D.A.M. status for d.c. measurements; and also, for reasons of hardware convenience, Sinegenerator output polarity. The third and fourth latches, "RAMlo" and "RAMhi" store low and high address bytes for interrogating the on-board R.A.M. when required.

- The Control board contains a 16-bit data bus which is interfaced to the internal 8-bit data bus via the bidirectional "Bus-Interface" unit (See Fig. 14). The 14-bit A.D.A.M.; the 13-bit voltage-nulling D-to-A converter (both in the Detector unit); and the on-board R.A.M. are connected to this bus and all have 3-state outputs. An open-collector gate is connected to D16 of this bus as a means of allowing the controlling computer to monitor an important hardware status line, "Not-Enab-Meas", during a.c. measurements (See later). Data lines D15 and D16 are otherwise redundant.

- During a d.c. measurement on a cell/battery the operation of the control board is very simple. Firstly, the Detector latch is programmed such that "A.C./Not-D.C." is low; "2V/Not-14V" is set appropriate to the cell/battery voltage and "Latchtrig" is set low (note that "Autotrig" is assumed to be high). The A.D.A.M. will then be in Sample (as in "sample-and-hold") mode. The Detector latch is then reprogrammed so that "Latchtrig" goes high, whereupon the A.D.A.M. will enter Hold mode and perform a conversion (in less than 44μs). The A.D.A.M. always holds its binary data until its next conversion and can be interrogated by the controller computer via the 8- and 16-bit buses in order to read a d.c. conversion result.

- For an a.c. measurement the system operation is rather more complex. It should be noted that during the progress of sinewave excitation the measurement system assumes temporary autonomy from the controller computer and the Control board is subservient to the Sinegenerator. Note that logic signals "Not-Inhibit"; "Not-Enab(le)-Meas(urement)"; and "Not-Convert"

originate from the Sinegenerator (See Sheets 1(a,b)).

- Prior to an a.c. measurement a d.c. nulling operation must have been performed. This simply involves performing a d.c. measurement and writing the result (after division by 2 by the computer) to the voltage-nulling D-to-A converter. The Detector latch must then be reprogrammed such that "Latchtrig" remains high; "A.C.-Not-D.C." is high and "Polarity" is as desired. The Sinegenerator and the Frequency latches, which share the same address line, must be programmed with valid data to select excitation signal frequency and amplitude. Once the measurement system has been correctly programmed then the Sinegenerator "Trigger" address can be accessed (with the data value and Read-Not-Write line status being unimportant). The Sinegenerator then takes control of the system by means of holding "Not-Enab-Meas" low for the duration of a measurement. By monitoring the state of the "Not-Enab-Meas" line via line D16 of the 16-bit data bus (See Fig. 13(iv)), a controller computer is able to tell when a measurement has terminated.

- The "Not-Enab-Meas" signal has various functions. Firstly, after slight modification (See Fig. 13(ii)), it is used to hold the "RAM-Address" counter in the Reset state when inactive (high). Secondly, when active (low), it connects R.A.M. address inputs to the RAM-Address counter by means of the "Data-Selector", rather than to latches RAMlo, RAMhi. Thirdly, when active, it selects the A.D.A.M. and the R.A.M. simultaneously via the "Addressing-Director" (See Fig. 15). Fourthly, the "Read-Not-Write" signal, originating from the controller computer is modified by "Not-Enab-Meas" via the "R/Not-W-Cleanup" unit (See Fig. 13(iii)) resulting in a signal "Read-Not-Write-X". "Read-Not-Write-X" mimics its parent signal except during a.c. measurements whereupon it is locked high to ensure that the A.D.A.M. output is constantly enabled and that the Bus-Interface unit is held in read mode. Fifthly, an active "Not-

Enab-Meas" state results in the R.A.M. outputs being kept disabled; this is important since, although "Read-Not-Write-X" is high, the R.A.M. is being required to accept, rather than deliver, data. "Not-Enab-Meas" is also involved in control of the 8-bit bus buffer/transceiver during measurements in order to allow read operations whilst avoiding possible contention of the external 1MHz data bus. (The B.B.C.-microcomputer external bus, unfortunately, seems to have various imperfections, one of which is that it is not permanently in the Read state when not in intentional use).

- During an a.c. measurement operation, whilst the Sinegenerator is producing an excitation waveform, the A.D.A.M. performs continuous conversions at a rate synchronised with the Sinegenerator internal clock by means of the Not-Convert signal. The Not-Convert signal is divided down by a programmable binary divider, which is programmed with sine-frequency data in parallel with the Sinegenerator latch, resulting in signal "Not-Var(iable)-Conv(ert)". "Not-Var-Conv" determines the A.D.A.M. trigger rate; this is always such that exactly 2048 conversions are performed during a measurement phase regardless of the excitation frequency and number of sinewave cycles involved.

- The "Not-Var-Conv" signal is fed into a 11-bit binary counter which provides sequential addresses, starting at 00000000000 for the 2kbytes of 16-bit on-board R.A.M. By means of address incrementing combined with appropriate chip enabling signals the 2048 14-bit A.D.A.M. conversion results are stored in consecutive memory locations in the R.A.M. Upon termination of a measurement the address counter is reset to zero. The address value is held at zero and the R.A.M. retains its data until the next measurement is performed. Detector a.c. output data is thus stored and made available for the controller computer to read at its leisure.

- Figs. 12(a,b) show the timing logic used for interface between the

Sinegenerator and the A.D.A.M./R.A.M.. Note that the A.D.A.M. is controlled by means of linked "Trigger" (negative-edge triggered) and "Sample-Hold" (sample when high) inputs and that the status of the A.D.A.M. is sensed by means of an (active-low) E(nd)-O(f)-C(onversion) output. The logic used to generate the signal "Autotrig" may seem overcomplex but results from attempts to identify and cure a persistent fault in circuit operation. It was eventually discovered that the fault lay within the A.D.A.M.; it had a nasty habit of occasionally sticking after powerup with its (active low) "EOC" output high and could be 'unstuck' only by setting the Trigger input low. The Not-Latchtrig line is required to be permanently high during measurements but due to the use of the logic gate marked "*" it provides a means of forcing a reset of the A.D.A.M. control bistable which serves to 'unstick' the A.D.A.M.. The latch generating the Not-Latchtrig signal is primarily intended for performing one-shot measurements, for example, as in d.c. measurements. The 3μs monostable produces a pulse on the "Not-Samplewrite" line upon termination of each conversion which requests the R.A.M. to read the A.D.A.M. output data resulting from that conversion.

- Fig. 14 shows the circuit of the Bus-Interface unit which is constructed from two 8-bit latches, two 8-bit buffers and control logic. For a read operation of a device installed on the 16-bit bus the operation is done in two stages. Firstly, the low byte of the data is read by addressing the low-byte latch/buffer pair and the read device simultaneously with the Read-Not-Write line high (the controller computer is responsible for providing the appropriate timings here). Then the high byte of the data may be read by a similar operation using the high-byte latch/buffer pair. For a write operation to a device on the 16-bit bus three stages are required. The latches of the low-byte and high-byte latch/buffer pair are first programmed individually with low-byte and high-byte data,

respectively, from the 8-bit bus and then the write device is addressed with the Read-Not-Write line low. Originally, transparent-type latches were utilised rather than D-type latches and pull-up resistors were found to be essential on the 16-bit bus, even though it is a three-state bus, otherwise uncontrollable bus oscillations often occurred which caused widespread system corruption. A peculiar feedback mechanism involving the Bus-Interface latch/buffer pairs was identified, though the instability was being allowed only because the B.B.C. microcomputer 1MHz bus timings were somewhat faulty. D-type latches are now in use in the Bus-Interface units which should remove the necessity for pull-up resistors.

- Note that the Bus-Interface unit was designed to allow write operations such that write-only latches on the 16-bit bus could have all bits programmed simultaneously; this is essential for the voltage-nulling D-to-A converter as it allows an analogue-output voltage to be changed without generating intermediate states. In hindsight, though, since no other write-only devices were ever installed on the 16-bit bus, the voltage-nulling D-to-A converter might better have been programmed from the 8-bit bus via a dedicated double-buffered latch.

- Fig. 15 shows the circuit of the local address decoder included on the Control board; the decoder has 16 mutually exclusive outputs of which 12 are used.

- Fig. 15 also shows the logic involved in the Addressing-Director which processes addressing signals plus the Not-Enab-Meas signal and allows certain pairs of Control board devices to be addressed simultaneously for purposes of internal communication.

CHAPTER 7

Non-BASIC Control Software for the Cell/Battery Test Rig

Apart from data analysis programs, the software programs associated with the research cell/battery test rig fall into three main categories: namely, BASIC "RUN-control" programs (incorporating charge-discharge control amongst other functions), BASIC "measurement(-control)" programs and invariant system routines written in machine code. Although the bulk of the rig control software was written in B.B.C. BASIC for convenience, certain system functions, including the reading-in of sinewave data from the internal R.A.M. of the measurement instrument, had to be accomplished by means of machine-code routines in order to maintain a reasonable program speed. Many other routines were written in machine code for convenience, compactness and security of storage.

Operation of the rig demanded a number of data tables for storage of programming and results data; however, the data storage facilities provided by B.B.C. BASIC were too inflexible for many purposes. Consequently, most system data was stored in specially reserved fixed memory locations so that it would be available to both BASIC and machine-code programs. The use of specially reserved memory had an additional advantage in that a large degree of protection was provided against data deletion and corruption.

The first half of this Chapter describes the use of specially reserved B.B.C. Microcomputer memory as an aid to understanding the programs and hardware interfacing which are discussed in this document. The second half of this Chapter describes a library of invariant machine-code routines which was made available to all high level programs,

generally written in BASIC, involved in the control of experiments. Many machine code routines served as convenient interfaces for hardware device programming but others provided more complex functions. The most important complex functions performed by machine code routines were those of battery d.c. terminal voltage nulling (described under "autonul%"), the reading-in and sorting of measurement data (described under sinread% and compact%) and the software implementation of phase-sensitive detection (described under "psdsoft%"). Note that Appendices 4 and 5 contain non-BASIC program listings and other (generally non-BASIC) information relevant to program usage during cell/battery testing.

Memory Usage of the B.B.C. Microcomputer for Purposes of Cell/Battery Test Runs

The B.B.C. microcomputer and B.B.C. BASIC allow space to be reserved in computer main memory for purposes other than BASIC program storage and workspace. This facility was used to provide an area for storage of machine-code routines, tables of system programming parameters and data from measurements. Devices on the B.B.C. Microcomputer "1MHz" external bus appear to the computer to lie within its main memory map. The research cell/battery test rig utilises about half of the "page FC" 1MHz bus address space.

Appendix 4(a) lists the utilisation of computer memory. The reader should note the following conventions used hereforth in this document relating to the cell/battery research test rig:-

- The computer memory map is divided into 256 "pages", each of 256 bytes.
- All absolute computer addresses and page numbers are given in hexadecimal.
- Computer address offsets are given in decimal unless stated otherwise.

- Bit positions within any 8-bit byte are numbered 0-7 starting at the lowest-order ("ones") bit.
- Generally, wherever data words are stored in multiple-byte form each word is held in the minimum number of contiguous memory locations required (e.g. a 16-bit word is held as two adjacent 8-bit bytes) with the lowest-order byte having the lowest address and the highest-order byte having the highest address (i.e. {low-byte, high-byte} or {low-byte, ..., high-byte} format). This format does not apply to the "Primary-Sinewave" table.
- Wherever a data word of bit length not an exact multiple of 8 is stored in multiple memory locations the word is held such that its lowest-order bit is occupying the least significant bit (BIT0) of the lowest-order memory location (i.e. a "right-justified" format). Superfluous high-order bits may or may not be arbitrary.

With reference to Appendix 4(a) and the above conventions the following notes are provided:-

- Locations 0070-0077, 0080-0084 and 0088-008B (which lie in a block 0070-008F reserved by B.B.C. BASIC II within "zero-page" memory for user purposes) are used as workspace by various machine-code routines. Locations 0076, 0077 and 0082-0084 are utilised in certain transfers of data from machine-code routines to BASIC. Note that no zero-page locations are reserved by any machine-code routine or by any RUN/measurement program for purposes of long-term storage of data; locations 0070-008F are thus generally available to external routines and programs.
- A B.B.C. Microcomputer being used as a controller computer must be operated in MODE 7 ("Teletext" mode) since this mode consumes the least memory (MODE 135 will work just as well with a "Master"-series computer). A block of memory is reserved above 62FF for special purposes by setting BASIC pseudovariable HIMEM to 62FF. If using a model "B" computer with a disk interface fitted this results, typically, in 18.5 kbytes of memory

being available for BASIC programs and workspace. A B.B.C. "Master" computer is preferred as it will give 21.25 kbytes of memory for BASIC programs and workspace under the same conditions.

- Locations 6300-69FF comprise a contiguous 1.75 kbyte block of memory available for machine-code routines.

- Locations 6A00-6AEF (240 bytes) are used for storing programming data for measurement programs. This section of memory is divided into tables which hold information on cell/battery types and data for measurement sequences. These tables are accessed only from BASIC programs and generally need to be set up correctly by the user prior to a system run or the performance of manually-controlled measurements (See the next Chapter for details of usage). Locations 6A00-6A5F comprise four "Frequency-Setting-Factor" ("FSF") tables. Elements of selected FSF tables are used to set excitation frequencies in automated a.c. measurement sequences. Locations 6A60-6ABF comprise four "Amplitude-Factor" ("AF") tables. Elements of selected AF tables are used in the determination of excitation amplitudes in automated a.c. measurement sequences. Locations 6AC0-6AEF comprise a "Cell-Type-Factor" (CTF) table which contains 48 bytes in sequence corresponding to the 48 Charge-Discharge modules. Each byte informs RUN and measurement programs of the type (single-cell or multi-cell) of battery present in its associated Charge-Discharge module and can be used to select between two alternative measurement sequences for each battery type.

- Locations 6AF0-6AFF (16 bytes) are not used by the Author's programs.

- Locations 6B00-6B5F (96 bytes) are used by RUN-control programs for storing information on cell/battery charge-discharge status. The contents of these tables are accessed for reading or update from BASIC programs only. Locations 6B00-6B2F comprise a "Cell-Programming-Byte" ("CPB") table which contains 48 bytes in sequence corresponding to the 48 Charge-

Discharge modules. The table is used to keep a record of the output-current status of Charge-Discharge modules. Locations 6B30-6B5F comprise a "Program-Change-Reminder" table which contains 48 bytes in sequence corresponding to the 48 Charge-Discharge modules. The table is used to record certain automatic modifications to charge-discharge programming which may occur when testing cells/batteries under computer control.

- Memory block 6B60-6BEF (144 bytes) is used as a table, the "Compacted-Sinewave" table, for storing partly processed measurement results as 48 contiguous samples in {low-byte, middle-byte, high-byte} format (Note that 6502 machine-code restrictions require that this table must not cross a page boundary).
- Locations 6BF0-6BFD (14 bytes) are used for various purposes both by machine-code routines and by BASIC. 6BF8 contains the "Sinegenerator-Programming" byte and 6BF9 contains the "Detector-Programming" byte (See later - "Notes on usage of 6BF8 and 6BF9").
- Locations 6BFE and 6BFF (2 bytes) are not used by the Author's programs.
- Memory block 6C00-73FF (2048 bytes) forms the "Low-Byte-Sinewave" table and block 7400-7BFF (2048 bytes) forms the "High-Byte-Sinewave" table. These tables together comprise the "Primary-Sinewave" table which is used to store 2048-byte sinewave data generated by the test-rig measurement hardware when operated in A.C. mode.

In page FC, which is associated with the B.B.C. Microcomputer 1MHz bus, memory was allocated as follows:-

- Locations FC00-FC8F (144 bytes) are not used.
- Locations FC90-FCEF (96 bytes) are used to control charge-discharge modules. Each of the 48 modules is allocated two addresses, one for programming its Charge-Discharge latch and one for activating its 4-pole relay. Note that, because of a peculiar configuration of the Charge-

Discharge hardware bus in the current version of the system, the addresses are not assigned in a simple sequential manner. However, the machine-code routines which are normally utilised for programming Charge-Discharge modules contain algorithms for calculating the required addresses (See later).

- Locations FCF0-FCFB (12 bytes) are used for communication between the B.B.C. Microcomputer and the measurement hardware (Fig. 11 shows the utilisation of addresses, given in decimal, within memory page FC).
- Locations FCFC and FCFD are not used by the Author's hardware.
- Location FCFE has a very important status as the reset address for Charge-Discharge hardware. Whenever this location is accessed the Charge-Discharge system reset mechanism is initiated and the Power-Crash-Protector is reset to its normal operational state.
- Location FCFF is not used by the Author's programs.

Notes on Usage of 6BF8 and 6BF9

Memory location 6BF8 holds the Sinegenerator-Programming byte. The Sinegenerator latch is generally programmed, whenever required, using the exact contents of this location. 6BF8 is thus used to keep a record of Sinegenerator latch status. In normal program operation there is a one-to-one correspondence between the 8 bits of the latch (See Sheet 1 and Appendix 5(a)) and the 8 bits of location 6BF8.

Memory location 6BF9 holds the Detector-Programming byte. 6BF9 is used when reprogramming the Detector latch and is a means of keeping a record of Detector latch status. With the exception of BIT5 there is a one-to-one correspondence between bits of the latch and bits of 6BF9 (See Fig. 15 and Appendix 5(a)). BIT5 of the Detector latch is used for A.D.A.M. triggering but BIT5 of 6BF9 is normally maintained high. Machine-

code routine "autonul%" (See later) always leaves BIT5 of 6BF9 high on exit. (!) Note that BIT5 must always be high on entry to routine "acprep%" (See later) else subsequent a.c. measurements using routine "acmeas%" (See later) will fail. (!) Note also that BIT4 of 6BF9, which is used for determining Sinegenerator output polarity, is not programmed by any machine-code routine and must be set as required from a BASIC program prior to performance of a.c. measurements.

The Charge-Discharge/Measurement Machine-Code Library Block

Appendix 4(b) shows a listing of the B.B.C. BASIC assembler source code for the 6502 machine-code routine library used by all charge-discharge and measurement programs. The object version of the code (1716 bytes), resulting from assembly, has been stored as a file named "U.CELCODE"; this code must be loaded into reserved computer memory prior to every test system run (preferably automatically by a "RUN-control" program) so as to be available to the programs involved in the run.

With reference to Appendix 4(b), the following notes are given, though note that Appendix 4(a) and Fig. 19 provide supporting information. Many references are made to system hardware devices which are primarily described in Chapter 6. Machine-code routines are dealt with in the order that they appear in the listing:-

- Lines 10-100 and 8710-8940 are connected with operations during code assembly by B.B.C. BASIC and have no direct significance to the final code.
- Lines 110-8700 comprise the machine code in mnemonic form with labels given as BASIC integer variables (Note that BASIC variable "os%" is an address offset involved during offset assembly and that occurrences of

"+os%" can be ignored when studying the machine code). Some labels indicate entry points to routines. Major routines are separated for clarity by double-"NOP" (null) commands. Single "NOP" commands are used to separate minor routines/subroutines. Machine code from line 100 to line 4150 concerns measurement system control, d.c. measurement operations and reading of a.c. measurement data. Code from line 1960 to 8200 concerns manipulation of a.c. measurement results. Code from line 8230 to 8700 concerns control of the charge-discharge hardware.

- "dcmeas%" is a routine which performs all operations necessary for a d.c. measurement. It first calls "autonul%" and then "oneshot%" (See the descriptions of the individual routines). Note that the entry requirement for oneshot% is automatically met in this situation.

- "oneshot%" is a routine which causes the Detector unit A.D.A.M. to perform a one-shot measurement. It does not alter the A.C./D.C. status of the Detector in any way and may thus be used to do a one-shot measurement whilst the Detector is in either mode. Note that oneshot% puts the Detector unit into either 2V or 14V mode depending on the state of BIT7 of 6BF9 upon entry. (!) However, oneshot% should never be used unless the Detector 2V/14V status is already correct on entry because the routine does not provide the time delays which are required for hardware settling during 2V/14V status changes.

ON ENTRY to oneshot% - memory location 6BF9 must contain a byte which has BIT7 set to the same state as BIT7 of the Detector latch.

ON EXIT from oneshot% - BIT5 of the Detector latch (signal "Latchtrig") is always set high and the 14-bit result from the measurement is present in memory locations {0076,0077}.

- "autonul%" is a routine which first puts the Detector unit into D.C. mode and does one d.c. measurement. The 14-bit offset-binary measurement result is then read in, divided by two to convert it into 13-bit offset-

binary form, and written to the Detector unit voltage-nulling D-to-A converter. On completion of this procedure the Detector is left in D.C. mode with its D-to-A converter generating a voltage nearly equal to the voltage (assumed steady) at the output of the preamplifier. Soon after entry, autonul% automatically sets the Detector unit to the voltage range (2V/14V) appropriate to the state of BIT7 of 6BF9 and a timing loop (timlopB%) is included to allow settling of the preamplifier reed-relay before continuing. A similar time delay is included after the voltage-nulling operation to allow settling of the composite D-to-A converter.

ON ENTRY to autonul% - 6BF9 must contain a byte which has BIT7 set appropriate to the voltage range (2V/14V) required for subsequent measurements.

ON EXIT from autonul% - the Detector unit is in D.C. mode and is set to the voltage range determined by 6BF9 on entry. BIT6 of 6BF9 is always set low. BIT5 of the Detector latch (signal "Latchtrig") is always set high. The result from the d.c. measurement involved is stored in {6BFC,6BFD} in 14-bit format. The result divided by two is stored in {6BFA,6BFB} in 13-bit format and is also programmed into the Detector voltage-nulling D-to-A converter. The voltage nulling hardware will have settled to near-perfect accuracy.

- "acprep%" is a routine, generally used after autonul%, which sets the Detector unit into A.C. mode and allows time for the Detector A.C./D.C. reed-relay to settle. Note that acprep% puts the Detector unit into either 2V or 14V mode depending on the state of BIT7 of 6BF9 upon entry. In practice, though, it is not sensible to use the routine for purposes of changing Detector voltage range.

ON ENTRY to acprep% - memory location 6BF9 should contain a byte which has BIT7 set to the same state as BIT7 of the Detector latch. BIT4 of 6BF9 should be set appropriate to the polarity of a.c. excitation required for

consequent a.c. measurements. (!) BIT5 of 6BF9 must be set high.

ON EXIT from acprep% - the Detector is in A.C. mode and is set to the voltage range determined by the contents of 6BF9 on entry. BIT6 of 6BF9 is always set high. The Detector system hardware will have settled.

- "trimdwn%" and "trimup" are subroutines used for purposes of fine trimming of voltage nulling. They are intended for use whilst the Detector Unit is in A.C. mode and are best invoked from a higher-order routine written in BASIC. The action of trimdwn% is to reduce the voltage at the output of the Detector unit voltage-nulling D-to-A converter by 1LSB. Conversely, the action of trimup% is to increase the voltage at the output of the converter by 1LSB. A time delay is included in each routine to allow hardware settling before exit.

ON ENTRY to trimdwn% - the Detector should be in A.C. mode and memory locations {6BFA,6BFB} should contain the data with which the voltage-nulling D-to-A converter is programmed at that time.

ON EXIT from trimdwn% - the contents of memory locations {6BFA,6BFB} will have been decremented by one. The voltage-nulling D-to-A converter will be programmed with the new contents and will have settled to near-perfect accuracy.

ON ENTRY to trimup% - (as for trimdwn%)

ON EXIT from trimup% - the contents of memory locations {6BFA,6BFB} will have been incremented by one. The voltage-nulling D-to-A converter will be programmed with the new contents and will have settled to near-perfect accuracy.

- "timlopA%" is a delay routine based on a software timing loop. When used with a 6502 (or compatible) microprocessor operating at a clock frequency of 2MHz a nominal delay of 100μs is produced. Note that machine interrupts (which occur regularly during normal operation of the B.B.C. microcomputer) may occasionally interfere with this routine and will

increase its effective delay. This routine is primarily intended for use with one-shot A.D.A.M. conversions in order to allow conversions to finish before attempting to read the resulting data (44μs maximum for an ADAM-824). Routine timlopA% has no effect on data in computer memory or on measurement hardware status.

- "timlopB%" is a delay routine based on a software timing loop. When used with a 6502 (or compatible) microprocessor operating at a clock frequency of 2MHz a nominal delay of 22ms is produced. As with timlopA%, machine interrupts may occasionally interfere with the routine and extend its effective delay. This routine is primarily intended for use in allowing measurement hardware systems (including reed-relays) to settle between settings/status changes and measurement operations. Routine timlopB% has no effect on data in computer memory or on measurement hardware status.

- "acmeas%" is a routine, generally used after acprep% (with possible subsequent null trimming) to request an a.c. measurement. Firstly, the routine programs the Sinegenerator (for frequency and amplitude) with the data held in memory location 6BF8. A delay follows to allow reed-relays to settle. The Sinegenerator is then triggered, whereupon the measurement hardware assumes temporary autonomy from the controller computer. After a delay of about 50ms the program enters a loop in which it repeatedly reads the state of the Not-Enab-Meas hardware signal line (via BIT7 of the Hi-byte Bus-Interface unit - see previous Chapter). Upon detection of a high state the loop terminates and the routine is exited.

ON ENTRY to acmeas% - the Detector unit should be set to the desired voltage range and should be in A.C. mode with a satisfactory d.c. voltage null in force. Location 6BF8 should contain a valid frequency/amplitude (FSF/AF) programming byte.

ON EXIT from acmeas% - the measurement hardware will have performed an

a.c. measurement but (apart from the updated contents of its R.A.M.) will be in the same configuration as upon entry. Routine acmeas% has no effect on the contents of any computer memory location.

- "sinread%", "St8%", "St16%", "St32%", "St64%" and "storehv%" constitute a suite of routines, for which sinread% provides the single entry point from BASIC, for purposes of transferring data from (external) measurement hardware R.A.M. into computer memory. A complex set of routines is required since the (two-byte) data is not always stored in computer memory in a simple sequential format. Selective data manipulation takes place during the reading process in order to put data into a form easily analysable by phase-sensitive detection methods whilst consuming the minimum possible processor time. The format of sinewave data held in computer memory in the Primary-Sinewave table has been described earlier and only the general details of the operation of the routine suite will be explained here.

Routine sinread% first initialises various zero-page memory locations for use as loop counters and then, by inspecting the Sinegenerator programming byte present in memory location 6BF8, jumps to one of St8%, St16%, St32%, or St64% depending on the frequency set for the preceding measurement.

Routines Stxx% provide counter incrementing and calls of storehv% in order to transfer and sort data as required. St8% is used to read in data from measurements involving a single cycle of sinewave. St16% is used to read in and sort data from measurements involving two cycles of sinewave. St32% is used for 4-cycle sinewave results. St64% is used for 8-cycle and 16-cycle sinewave results. Note that each pass of an inner loop "loopixx%" deals with 256 samples (which is the page size for the 6502).

Subroutine storehv% performs the immediate function of reading data bytes from external R.A.M. and writing them to locations in the computer

sinewave (low- and high-byte) data tables. It makes extensive use of 6502 Indirect,Y addressing and is directed by information provided via memory locations 0071, 0072, 0073, 0074, {0088,0089} and {008A,008B}. Routine storehv% has additional important functions, namely, those of finding the highest sample value occurring in a response waveform and of checking for the occurrence of the sample value 00000000000000 which is indicative of a Detector unit overload (or an ambiguous near-overload).

ON ENTRY to sinread% - the measurement hardware R.A.M. should contain data resulting from an a.c. measurement and 6BF8 should contain the Sinegenerator programming byte used for that measurement.

ON EXIT from sinread% - data from the measurement hardware R.A.M. will have been read, sorted and stored in composite single-cycle format (with the exception of results from $85^1/_3$Hz and 128Hz measurements which will be in two-cycle format) in the Primary-Sinewave data tables 6C00-73FF (low-byte) and 7400-7BFF (high-byte). The highest sample value found will be present in memory locations {0082,0083} in {low-byte, high-byte} form. If a sample of value zero (00000000000000) was present in the data then memory location 0084 will contain a value 1; if not then location 0084 will contain 0. Note that an operation of sinread% takes approximately 0.7 second.

- "compact%", "xcompct%", "clrcomp%", "pagcalc%", "adstor%", "csateA%", "csateB%" and "divSby3%" comprise a suite of routines for which compact% and xcompct% are the intended entry points from BASIC. These routines are for purposes of compressing 2048-sample, 2-byte sequential data, held in the Primary-Sinewave table into 48-sample, 3-byte sequential form. The process is accomplished simply by adding together the samples contained within 48 consecutive blocks. Output data is placed into the Compacted-Sinewave table (6B60-6BEF), the general layout of which has already been explained. Since, rather inconveniently, 48 does not divide exactly into

2048 the method used is not one of simple addition. Instead, output samples are constructed by adding groups, respectively, of 43,42,43,43,42,43,..... input samples with error compensations (using a simple proportional method) made for the 43rd, 44th, 85th, 86th, (128+43)th, (128+44)th, (128+85)th, (128+86)th, (256+43)rd, ... input samples; each output value is then effectively a sum of $42^2/_3$ contiguous input samples. Note that the data outputted to the Compacted-Sinewave table is in a peculiar {binary + (offset $2^{13}*42^2/_3$)} format and is in {low-byte, middle-byte, high byte} form. The compact% suite uses many techniques in common with the sinread% suite. On entry via compact% the Compacted-Sinewave table is first cleared (all locations being set to zero) using clrcomp% and then the data compaction routine is performed. It is possible to enter the suite via xcompct% in which case the routine clrcomp% is bypassed; this may be of value for obtaining averages from multiple measurements. Note that 256 input samples are dealt with for each pass of the loop "loopoc%".

Routine pagcalc% calculates page numbers of input data for use in Indirect,Y addressing.

Routine adstor% performs the immediate function of data transfer/addition; it makes use of 6502 Indirect,Y addressing and is directed by information provided via memory locations 0071, 0073, {0088,0089}, {008A,008B}.

Routines csateA% and csateB% are compensation routines which perform additions and subtractions of part-samples and which are called at appropriate times by compact%.

Routine divSby3% is a divide-by-3 routine required by csateA% and csateB%.

ON ENTRY to compact% - the Primary-Sinewave table should contain sensible data for compaction.

ON EXIT from compact% - the Compacted-Sinewave table will contain compacted data in special format (See earlier) relating to the input data. All other non-zero-page memory locations (including the Primary-Sinewave table) will be unaffected.

ON ENTRY via xcompct% - the Primary-Sinewave and Compacted-Sinewave tables should both contain sensible data.

ON EXIT from xcompct% - as for compact% except that the Compacted-Sinewave table will contain compacted new data added to its original contents.

- "average%" is a routine which adds together all 48 3-byte samples in the Compacted-Sinewave table, divides the total by 4 and places the result in {6BF0,6BF1,6BF2}. Due to the format of the input data and a special initialisation method, the output data will be in a peculiar {binary + (offset $2^{23}+2^{22}$)} format. This routine is intended, with an appropriate scaling factor applied, for calculating the average sample value in sinewave data. This routine makes use of subroutines which will be described in the next section.

ON ENTRY to average% - the Compacted-Sinewave table should contain sensible data.

ON EXIT from average% - memory locations {6BF0,6BF1,6BF2} will contain a value in special format (See earlier). Via division of the value by appropriate binary scaling factors a result is obtained which is equal to the average value of samples in Compacted or Primary sinewave data. Memory locations 6BF3, 6BF4, 6BF5 and 6BF6 will always contain 0 and location 6BF7 will always contain 2. All other non-zero-page memory locations will be unaffected.

- "psdsoft%", "divby4%", "tORfR%", "tORfI%", "addRorI%", "subRorI%" and "prepint%" comprise a suite of routines which act upon data in the Compacted-Sinewave table and for which psdsoft% is the single entry point from BASIC. These routines simulate a phase-sensitive detection process in

which an arbitrary (but assumed repetitive) input signal is multiplied by a square-wave function of precisely defined frequency and phase and the product integrated over a defined period. By multiplying sine data with a square wave of effectively the same frequency and phase as the excitation sine wave a value proportional to the Real part of test cell/battery impedance may be obtained; by multiplying sine data with a square wave in effective quadrature with the excitation sine wave a value proportional to the Imaginary part of test cell/battery impedance may be obtained. For sinewave data in single-cycle format (in a sine data table), the data represents an absolute phase span of 0-2π radians. In this case the multiplying square wave for Real-part analysis is a simple function having value +1 for angles from 0 inclusive to π and value -1 for angles from π inclusive to 2π; the corresponding square wave for Imaginary-part analysis is a function having value +1 for angles from π/2 inclusive to 3π/2 and value -1 otherwise. The multiplication of sampled binary data by factors of +1 and -1 whilst performing an integration of the product is accomplished very simply in the psdsoft% routine suite by means of selective additions of samples to and subtractions of samples from a running total. The routines perform analyses of Real and Imaginary response components simultaneously. By using square wave functions having repetition rates of integer multiples of the fundamental rate it is possible to obtain values proportional to Real and Imaginary components of second and higher harmonic elements which may be present in response waveforms. On entry to psdsoft% the contents of the output memory locations are preset to a special value using "prepint%" (See later) and then a series of program loops is entered. Note that sections "toPId2%", "toPI%", "to3PId2%", to2PI" relate to quadrants of a multiplying square wave cycle (of absolute phase through 0-2π radians). The number of passes through each of the above loops is determined by the value present in

memory location 0075 on entry to psdsoft%; this provides a means of selecting the response frequency harmonic to be analysed. In common with the hardware phase-sensitive-detection process, the software version produces results which are unaffected by any fixed offset in sample values. Apart from an inevitable offset in sample values due to imperfect d.c. nulling within the hardware there is an effective fixed offset in all samples in the Compacted-Sinewave table due to the nature of the {binary + offset} coding. Both types of offset are conveniently ignored by the p.s.d. process.

Routine divby4% divides the 4-byte contents of memory quadruplets {6BF0-6BF3}, {6BF4-6BF7} by four and is used, for reasons of convenience, at the end of psdsoft% (and at the end of average%) to ensure that the final output data words will have length no greater than 24 bits (3 bytes). The numerical accuracy lost during this process is trivial.

Routine tORfR% ("to-OR-from-Real") is used directly before addRorI% or subRorI% to direct an addition or subtraction to act upon the Real component running total in memory locations {6BF0-6BF3}. It simply sets the low byte of the quadruplet base address for purposes of Indirect,Y addressing.

Routine tORfI% ("to-OR-from-Imaginary") is used in a similar manner to tORfR% to direct an addition or subtraction to act upon the Imaginary component running total in memory locations {6BF4-6BF7}.

Routine addRorI% ("add-Real-or-Imaginary") performs an addition of a sample from the Compacted-Sinewave table to either the Real or Imaginary component running total. Both the input locations (using a base address in {0088,0089}) and the output locations (using a base address in {008A,008B}) are determined by 6502 Indirect,Y addressing.

Routine subRorI% ("subtract-R-or-I") acts in a similar manner to addRorI% but performs a subtraction of a sample rather than an addition.

Routine prepint% performs the functions of initialising memory locations {0088,0089} and 008B for use in Indirect,Y addressing and of initialising the contents of Real part memory quadruplet {6BF0-6BF3} and Imaginary part quadruplet {6BF4-6BF7}. Both output quadruplets are initialised not to zero but to 2^{25} which ensures that, regardless of the nature of the response data present in the Compacted-Sinewave table (assuming that the Compacted-Sinewave table has been constructed via compact% from data samples of size no greater than 14 bits), the final integration results of psdsoft% will always be positive (The same applies to the result of average%). It should be noted that the initialisation offset may have to be removed when results are further processed.

ON ENTRY to psdsoft% - the Compacted-Sinewave table should contain sensible data. (!) Memory location 0075 must contain one of the following values else the routine will fail to perform a useful function and may hang up:-

For sinewave results in single-cycle format .....

12 for Fundamental (1st. Harmonic) analysis

6 for 2nd. Harmonic analysis

4 for 3rd. Harmonic analysis

3 for 4th. Harmonic analysis

2 for 6th. Harmonic analysis

For results in double-cycle format (128Hz and $85^{1}/_{3}$Hz) .....

6 for Fundamental (1st. Harmonic) Analysis

3 for 2nd. Harmonic analysis

ON EXIT from psdsoft% - memory locations {6BF0,6BF1,6BF2} will contain a value in {binary + (offset 2^{23})} format proportional to the Real component of the response waveform at the selected harmonic. Memory locations {6BF4,6BF5,6BF6} will contain a value in {binary + (offset 2^{23})} format proportional to the Imaginary component of the response waveform at the

selected harmonic. Memory locations 6BF3 and 6BF7 will always contain 0. All other non-zero-page memory locations will be unaffected.

- busline% is a subroutine used by charge-discharge hardware control routines for calculating a special hardware address offset for a Charge-Discharge module (on the 1MHz B.B.C. Microcomputer bus) given its serial number. The routine calculates a value from the contents of memory location 0070 and places the result in 0071. busline% is primarily intended for use by machine-code routines but can be called from BASIC.

ON ENTRY to busline% - memory location 0070 should contain a Charge-Discharge module serial number (0-47).

ON Exit from busline% - memory location 0071 will contain a calculated value to be used as an offset from an appropriate base address for Charge-Discharge module control (note that the base addresses within memory page FC are decimal 144 for charge-discharge current programming and decimal 146 for four-pole relay activation). The contents of memory locations other than 0071 will be unaffected.

- "access%" is a routine for the purpose of closing a selected Charge-Discharge module four-pole relay. The routine makes use of busline% and a Charge-Discharge module serial number provided via memory location 0070; It performs an arbitrary write operation to the appropriate memory-mapped location (Note that a read would also work since an addressing pulse is all that is required).

ON ENTRY to access% - (!) memory location 0070 should contain a valid Charge-Discharge module serial number (0-47). (!) No Charge-Discharge module four-pole relay should be closed at the time (though no harm would result if the same relay were selected twice in succession).

ON EXIT from access% - the four-pole relay for the selected Charge-Discharge module will be closing. (!) Note that no time delay is included in this routine to allow full relay closing before exit (The delay

requirement must be handled by BASIC programs - the four-pole relays are slow in operation compared to reed types). Memory location 0071 will contain the full hardware address offset within memory page FC of the selected charge-discharge module.

- delatch% is a routine for the purpose of opening all charge-discharge module four-pole relays in one operation. It simply performs a write (though a read would also work) of an arbitrary byte to the memory-mapped 1MHz bus location FCFE which is used as a hardware reset address. Note that in accessing the reset address, delatch% also resets the hardware Power-Crash protector to the active state.

ON ENTRY to delatch% - (no special conditions required)

ON EXIT from delatch% - any previously closed Charge-Discharge module four-pole relay will be opening. (!) Note that no time delay is included in this routine to allow full relay opening before exit (The delay requirement must be handled by BASIC programs). The Power-Crash protector hardware will be reset to its normal operational state.

- "chdpro%" is a routine for the purpose of programming a selected Charge-Discharge module '573 latch. The routine makes use of busline% and a charge-discharge module serial number provided in memory location 0070; It performs a write operation of a byte, supplied via location 0075, to the appropriate memory-mapped location.

ON ENTRY to chdpro% - memory location 0070 should contain a valid Charge-Discharge module serial number (0-47) and location 0075 should contain a sensible Cell-Programming byte.

ON EXIT from chdpro% - the (output-current-determining) '573 latch for the selected Charge-Discharge module will have been programmed with the Cell-Programming byte supplied. Memory location 0071 will contain the full hardware address offset within memory page FC of the selected Charge-Discharge module.

CHAPTER 8

BASIC Software for Control of the Cell/Battery Test Rig and for Related Programming and Analysis Purposes

B.B.C. BASIC was found to be a useful language since it allows programs to be fairly well structured and because it incorporates an error handler which enables controlled hardware to be shut down in a predictable manner upon occurrence of serious run-time errors. As BASIC is (primarily) an interpreted language, programs could be modified and programming errors located with reasonable speed.

Due to memory limitations of the B.B.C. microcomputer, the programs for controlling cell/battery test runs had to be split into "RUN-control" and "measurement" programs which CHAINed (loaded and ran) each other alternately (Note that a B.B.C. "Master" computer can in theory be configured to hold fully-integrated programs but complications result, especially during program development). Each system run generally utilised a program doublet. The division of certain system functions into separate programs was advantageous in that program parts controlling measurements and program parts controlling other operations could be modified or replaced independently. However, a disadvantage existed in that measurements had to be done within discrete time-blocks rather than being done in a more time-efficient fully-time-staggered manner. A great amount of care was taken in order to make programs as powerful in the user-interface and as fault-tolerant as possible, though, at the expense of additional limitations on program timings and computer memory space.

During the course of the research, programs were modified and improved often and a large number of program variants were used. In general, programs had to be customised for particular system runs (or

groups of runs) and for purposes of this document a particular, often-used program doublet "dCELRUN"-"MAF" will be described. Appendix 6 contains the listings of "dCELRUN" (largely uncommented for reasons of limited computer memory) and "MAF". The program flowcharts contained in Sheets 3(a,b) provide guidance in understanding general program flow but are far from complete. The reader (who will probably be unfamiliar with B.B.C. BASIC) should note the following points:-

- Numbers prefixed with "&" are hexadecimal.
- Variables ending with "%" are integer variables.
- Variables ending with "$" are string variables.
- Numbers prefixed with "?" specify absolute memory locations.
- The command *FX3,8 enables a printer and *FX3,0 disables it.
- The command *FX15,1 flushes the computer input buffer (usually the keyboard buffer).
- The command "INKEY$(0)" results in an instantaneous test of the computer input buffer (usually the keyboard buffer).
- "VDU" commands are generally connected with monitor graphics output.
- Any "PROCxxx" is a procedure and any "FNxxx" is a function.

The RUN-control Program "dCELRUN"

With reference to the listing of "dCELRUN" in Appendix 6(a) and the above points, the following notes are provided:-

- The program "dCELRUN" (in common with all RUN-control programs) must usually be saved under the name "DUMMY" when used so that it can be re-entered successfully (via a CHAIN operation) on completion of any measurement program.
- "dCELRUN" obtains data for values/timings of charge-discharge currents and types/timings of measurement program requests primarily from the

"Automatic-RUN-Control" instruction table which is a BASIC DATA table at the program end. "dCELRUN", though also provides a method for manual programming of charge-discharge currents which can be of use for very simple tests and charge-discharge runs.

- (!) "dCELRUN" (in common with most RUN-control programs) requires that valid data be present in the Cell-Type-Factor (CTF) table in reserved computer memory (See previous Chapter). The data must be consistent with the cell/battery types present in the Charge-Discharge modules being controlled. Before "dCELRUN/DUMMY" is RUN valid data must have been entered by the user into the CTF table (often via a *load from a file).

- (!) "dCELRUN" (in common with most RUN-control programs) requires that a printer be attached to the computer since the program (and also many measurement programs) prints certain important items of information during a RUN onto paper as a permanent record. If an on-line printer is not attached then the program is liable to hang in a state which could damage cells/batteries.

- If "dCELRUN" is constructed so as to request measurements then any measurement program required must be available to the computer in an appropriate disk drive. In practice, measurement programs are generally placed on the same disk and in the same directory as the RUN-control program.

- Program lines 90-110 provide BASIC handles on machine-code routines and binary data tables (See previous Chapter).

- Line 130 prints a message on paper via printer. The message is printed both on initial entry to "dCELRUN/DUMMY" and whenever "dCELRUN/DUMMY" is re-entered via a CHAIN from a measurement program.

- Line 160 defines the number of Charge-Discharge modules (starting at module "0") to be controlled by the program.

- Line 200 defines maximum and minimum allowable-voltage thresholds for

1.25V (1 cell) and 9-10V (7-8 cell) batteries respectively (used in "PROCsafe" - see later).

- Line 240 loads the machine-code routine library into computer memory.
- Lines 260 and 290 load explanatory text to the computer monitor.
- Line 230 determines if the program is being entered for the first time (a manual start) or being re-entered automatically (e.g. by being CHAINed by a measurement program) and takes appropriate actions.
- Lines 240-370 constitute a startup/initialisation section of the program which (a) loads the machine-code routine library into reserved computer memory, (b) gives some on-screen information to the user, (c) allows the user to optionally set a manual RUN end-time value, and (d) allows the user to optionally start the run with manual data.
- Lines 390-590 constitute the main body of the program which operates the cell/battery test rig in "Normal/RUN" mode. In this mode the program performs various important operations in a regular cyclic manner. The operations include displaying the system clock on the computer monitor; comparing the system clock with an 'alarm' value which is used to note the time of the next reprogram or measurement-request or program-end operation; and applying procedure "PROCsafe" (See later) to all controlled cells/batteries in sequence once every 10 seconds or so. In Normal/RUN mode a menu of utility/mode options is displayed on monitor (readable from the program listing); the user may invoke any utility/mode by pressing an appropriate keyboard key. (!) It should be noted, though, that in system modes other than Normal/Run mode the program is unable to act upon its Automatic-RUN-Control instructions so that system utilities should be used by the user as sparingly and briefly as possible.
- "PROCtdisp" displays the value of the system clock on the computer monitor.
- "PROCc_clist" displays a listing of the most recent manual-reprogram

instruction sequence.

- "FN14BOB" converts a 14-bit offset-binary number to decimal.

- "FNerr(<string>)" tests if a character string is pure numeric.

- "PROCrhardw" resets the test rig hardware to a quiescent state in which all Charge-Discharge modules are programmed for zero current and all Charge-Discharge module relays are open.

- "PROCCBPclr" clears all Cell-Programming-Bytes (CPBs).

- "PROCPCRclr" clears all Program-Change-Reminder (PCR) bytes.

- "PROCsafe(<cell No.>)" is a very important procedure which tests the cell/battery pointed to for overvoltage (as might arise from excessively fast charging) or undervoltage (as might arise from overdischarge). The routine makes use of a brief d.c. test on the relevant cell/battery and utilises preset voltage thresholds (set at program line 200). On detection of a detrimental situation the Cell-Programming byte (CPB) for the relevant cell/battery is cleared (giving non-isolated zero-current) and the PCR for the battery is set to a value other than zero. As soon as the CPB for such a battery is found to be reprogrammed to a non-detrimental value then PROCsafe clears the relevant PCR and allows normal programming for the battery. Any incidence of clearing of a CPB by PROCsafe is recorded via a printer on paper. The main value of PROCsafe in practice is for recording the times of voltage cutoff of cells/batteries during discharge for purposes of charged-capacity determination.

- "PROCsuspend" suspends a system run with all Charge-Discharge modules in a quiescent state and with the system clock effectively frozen and provides a means by which the user can (a) resume operations, (b) manually CHAIN a measurement program or (c) abort the system run in a controlled (but nominally permanent) manner.

- "PROCsyntdescr(<switch>)" loads explanatory text (for "Manual-Reprogram" mode) to the computer monitor.

- "PROCinputlines" is used in Manual-Reprogram mode for interpreting manual instruction strings. The instruction syntax is checked for errors and valid instructions are placed into consecutive elements of array "order$()".
- "PROCwaittorep" provides a "Wait-to-Reprogram" mode which is intended to follow Manual-Reprogram mode. In this mode a list of options is displayed (readable from the program listing) which relates to the use of the most recent set of manual instructions; the user selects an option by pressing an appropriate keyboard key.
- "PROCdatatoCPBs" reprograms some or all CPBs according to the instructions contained within array "order$()".
- "PROCCPBstochds" reprograms all Charge-Discharge modules for charge-discharge current according to the CPB table in computer memory.
- "PROCendt" is intended to be called when the program end time (manual or automatic) is reached. It terminates the program leaving all Charge-Discharge modules in a quiescent state and displaying a message on the computer monitor.
- "PROCresettime" provides a route by which the user can manually modify the system clock value during a system run.
- "PROCsetendt" is intended to be used in the initialisation section of a system RUN. It enables the user to set a manual program-end time (which has equal priority to the automatic program-end time).
- "PROCresetendt" provides a route by which the user can modify the manual program end-time during a system RUN.
- "PROCCPBlist" generates a listing on the computer monitor of the CPBs active at the time of procedure entry for all Charge-Discharge modules being controlled.
- "PROCstartdata" is intended to be used in the initialisation section of a RUN. It interprets the first instruction contained within the Automatic-

RUN-Control instruction table held in DATA statements at the program end. If the instruction syntax is found to be in error then the program is terminated in a controlled manner. PROCstartdata has the function of optionally setting the program start time (in terms of the system clock value).

- "PROCusedata" checks and interprets instructions (excluding the first one) contained within the Automatic-RUN-Control instruction table held in DATA statements at the program end. On detection of a syntax error in any instruction the program is terminated in a controlled manner. The main functions of PROCusedata comprise reprogramming of CPBs, storage of an 'alarm' time for the next automatic-reprogram operation, requesting of measurements (indirectly) and requesting of program termination.
- "PROCreentry" provides a route by which "dCELRUN/DUMMY" can be re-entered correctly via a CHAIN upon termination of a measurement program which has been CHAINed by "dCELRUN/DUMMY". "PROCreentry" restores the program DATA pointer, the system clock and the manual end time.
- "PROCCHAINM(<program name>)" CHAINs the specified measurement program and saves the program DATA pointer, the system clock value and the manual program end-time value to the B.B.C. BASIC "resident integer variables" J%, K%, L%.
- "PROCERROR" is invoked if the BASIC interpreter encounters an error whilst the program is running or if the computer "Escape" key is pressed by the user. "PROCERROR" causes a termination of the program with all Charge-Discharge modules set to a quiescent state and displays the values of J%, K%, L% which are required to be set in order to restart the system RUN from the point at which the error occurred.
- The Automatic-RUN-Control instruction table held in DATA statements commences at program line 2730 and may be as large as the user requires subject to memory limitations of the computer chosen.

The Measurement Program "MAF"

With reference to the listing of "MAF" in Appendix 6(b) and the information points given earlier, the following notes are provided:-

- "MAF" is intended to be invoked from a RUN-control program such as "dCELRUN/DUMMY" and, whilst operational, takes sole control of the test system hardware.
- "MAF" obtains information on battery types and on measurements required on cells/batteries from the FSF/AF/CTF table in computer memory. "MAF" (in common with most measurement and RUN-control programs) requires that valid data be present in these tables; such data must have been entered by the user into the tables (often via a *load from a file) before the associated RUN-control program is RUN.
- Program lines 140-160 provide BASIC handles on machine-code routines and binary data tables (See previous Chapter).
- Lines 230-420 define various parameters and scaling factors for use by the program.
- Line 450 prints to paper, via printer, the measurement program name and the time of entry (in terms of the system clock).
- Lines 460-510 constitute the main program loop which calls selected routines. The loop utilises a cell/battery counter (BASIC variable C%) and executes once for every Charge-Discharge module being controlled, so that each cell/battery in turn has a complete measurement sequence done on it. At the start of the loop the Cell-Access relay for the relevant battery is closed and at the end of the loop the Cell-Access relay is closed (by closing all relays).
- It should be noted that on entry to "MAF" from "DUMMY" all Charge-Discharge modules are programmed for isolated-zero-current and that "MAF" (unlike some measurement programs that the Author has used) does no

reprogramming of Charge-Discharge currents. This procedure, though simple and having a high safety factor, has a disadvantage in that different batteries will suffer different rest-times between suspension of Ch-D currents and commencement of measurements.

- Line 540 terminates "MAF" by CHAINing a program named "DUMMY" which should be the RUN-control program for the RUN.
- "PROCmsqN" is an extensive procedure which intelligently requests a sequence of measurements on the cell/battery pointed to by the BASIC variable C%. The procedure performs a sequence of measurements the frequencies of which are determined directly by a sequence of Frequency-Setting-Factors (FSFs) in the FSF table in computer memory. When the routine finds an FSF of the special value 255 the measurement sequence is terminated. For every FSF there exists a corresponding Amplitude-Factor (AF) in the AF table in computer memory.

The initial measurement performed (lines 600-620) is for purposes of roughly gauging cell/battery impedance and its results are not analysed in depth. The excitation amplitude (programmed for the Sinegenerator) for the first measurement is set directly according to the value of the first AF in the Amplitude-Factor table. For purposes of "MAF" (and most other measurement programs) the first AF may thus be called an "Amplitude-Setting-Factor" (ASF).

Every measurement following the first has its excitation amplitude calculated by the procedure (lines 760-800) according to the response amplitude found in the previous measurement, the excitation amplitude used for the previous measurement and the value of the relevant AF. Every AF other than the first may thus be called an "Amplitude-Estimation-Factor" (AEF).

For every measurement done, the following parameters are calculated (lines 660-680): the highest A.D.A.M. code encountered (HIVAL%), the

average A.D.A.M. code (AV%) and the apparent response-waveform peak value (PKA%). For every measurement other than the first the procedure (within lines 860-960) obtains the real- and imaginary-component raw-data values and calculates various parameters relating to impedance response. For measurements other than the first the routine (within lines 980-1060) also obtains certain real- and imaginary-component raw-data values of response-waveform harmonic components.

The procedure displays virtually all frequency, amplitude and measurement-result parameters on the computer monitor as it progresses through measurements. Selected items of information and selected measurement results in raw-data format are sent to a file on floppy disk for analysis at a later time. The data is put to disk in binary form and is in a variable block-wise format (which includes results from d.c. measurements - see later).

- "FNREAL" performs a conversion to decimal of the number held in special format in memory locations {6BF0,6BF1,6BF2}.
- "FNIMAG" performs a conversion to decimal of the number held in special format in memory locations {6BF4,6BF5,6BF6}.
- "FNFREQ(<FSF>)" calculates measurement frequency in Hertz from the Frequency-Setting-Factor given.
- "FN14BOB" (defined as in "dCELRUN").
- "PROCatrim(<time-period value>)" trims, as accurately as is possible, the d.c.-voltage nulling of the Detector-Unit whilst in A.c. mode. The trimming mechanism repeats continuously for the time period given.
- "PROCacN" acts upon the cell/battery pointed to by the BASIC variable C%. It first performs a d.c. test and puts the result to the computer screen and to a floppy disk file (the same file as for a.c.-measurement results). The procedure then prepares the measurement hardware for a.c. measurements and calls procedure PROCmsqn to perform a.c. operations.

- "PROCERRORN" is invoked if the BASIC interpreter encounters an error whilst the program is running (note that the computer "Escape" key is disabled during most of program "MAF" and cannot cause a BASIC error). "PROCERRORN" causes a termination of the program with all Charge-Discharge modules set to a quiescent state and displays an important warning to the user on the computer monitor.
- "PROCrhardw" (defined as in "dCELRUN").

Other (BASIC) Software Associated with Usage of the Cell/Battery Test Rig including System Programming/Configuration and Results Analysis

Apart from RUN-control and measurement programs, the Author created many other BASIC programs/utilities for use in creating programming-data files for the research cell/battery test rig, for system testing and for interpretation and analysis of the results of tests. Some of these programs are outlined below.

A menu-driven program named "CTF/MSQ" was used for editing the contents of CTF/FSF/AF tables in computer memory and for generating binary files (of name "U.MEASxxx") which could be *load'ed directly into computer memory from floppy disk prior to system RUNs.

A program named "valDATA" was used for checking syntax of Automatic-RUN-control instruction sequences (held in blocks of BASIC DATA statements) before such instructions were used in RUN-control programs. A listing of "valDATA" is given in Appendix 6 (primarily since the program listing contains notes on instruction sequence syntax and usage).

A range of highly customised RUN-data manipulation and graph-printer programs was developed. Data analysis was complicated severely by the fact that the format of results on floppy disk resulting from test

system RUNs was variable. For any particular RUN the format and total size of a result file depended on (a) the number of cells/batteries tested in the RUN, (b) the number and type of measurements in a sequence and (c) the duration of the RUN. Furthermore, the printing of graphs of results onto paper with high resolution was a very time-consuming process. A suite of graph-printer utility programs was developed which could print a complicated set of results graphs automatically; some system RUNs required printing of over a hundred graphs, which took many hours. The graph-printer suite operated in a similar manner to the RUN-control/measurement-control program system in that a controller program and specialised graph-printer programs were used which CHAINed (loaded and ran) each other alternately. As an example case, programs "DC_C_K" and "GAMMA" from the suite "DC_C_K", "ALPHA", "GAMMA", "DELTA" are given in Appendix 6. It should be noted that "DC_C_K" is usually required to be saved under the name "DRIVER" when used. Program "ALPHA" prints a graph of cell/battery terminal voltage, "GAMMA" prints a graph of cell/battery Effective-Series-Capacitance and "DELTA" prints a graph of cell/battery Effective-Series-Conductance.

As well as raw-data-dependent graph-printer programs, some programs were developed for converting raw-data results into a simpler format for purposes such as result comparisons via displays on monitor and basic statistical analyses and interpretations.

CHAPTER 9

General Philosophies Policies and Problems of Experimentation ; An Outline of Experiments Done Using the Cell/Battery Test Rig and Associated Discoveries ; Rig Limitations and Infelicities

Construction of an Integrated Database - Viable or Not?

It was originally thought that that the cell/battery test rig might be used by the Author to accumulate a large formal database of information in a well-defined format for easy computer analysis. However, this idea proved to be unworkable for a combination of philosophical and technical reasons and in practice most results were put into printed-graph form with selected sets of results being analysed in more detail.

The philosophical reasons largely concerned the rather optimistic proposal of the research to lead to the development of a practical, adaptable, "intelligent" battery charger/processor. A large database of information on the limited number of sample cells/batteries available to the Author might have been of academic interest but from the point of view of utilising information for a useful end, much of the information eventually collected proved to be of very limited value.

During the course of the research, experimentation methods were refined continuously and the scope of experimentation often had to be narrowed, in a manner based on interpretation of preceding results, in order to concentrate attention on more promising areas. In view of the facts that the scope of experimental investigations changed during the period in which experiments were being done and that responses of

cells/batteries to experimental methods were found to vary between different cell/battery types/batches in a rather unexpected manner, the concept of creating a large, integrated database seemed an excessively cumbersome exercise. Consequently, attentions were focused upon representing results in an accurate printed-graph form which was amenable to analysis and comparison by pen-and-paper methods.

It should also be noted that conventional rigorous statistical analyses are not necessarily particularly valuable when applied to real-world situations; instead, non-intensive studies of worst-case situations may suffice. For example, to take a simple case, a battery charger capable of charging batteries to a statistically-calculated average of 85% capacity might sound reasonable but if some of the batteries were being charged to only 70% capacity, some or perhaps all of the time, then the charger would be unlikely to be considered as having acceptable specifications. If such a charger were modified so as to charge all batteries to 85% capacity worst-case then this would probably necessitate roughly half of the batteries receiving excess overcharging. One consequence of this, since the charging efficiency of batteries tends to zero during overcharge, is that the statistical distribution of charged capacities would then become highly asymmetrical (and, in particular, highly non-Gaussian) and not amenable to reasonably simple analysis by methods of probability and statistics.

The technical reasons for avoiding large-scale statistical interpretation of results in a database form are explainable as follows. Analysis of results was complicated by the fact that cell/battery test runs produced raw-data in a variable format dependent on the numbers of cells/batteries and certain details of measurement sequences involved in individual runs. For comparison of results, even from superficially similar system runs, the large number of variables involved often demanded

a large amount of file manipulation and manually-controlled 'unscrambling' to be done in order to achieve worthwhile conclusions.

Statistical interpretation of general results was also complicated by the occurrence of random or semi-random measurement failures of variable magnitude which, if uncorrected, could have grave effects on statistical analyses though could easily be ignored for purposes of visual study and interpretation. Consequently, large-scale mathematical analyses would have required prior manual inspection and intelligent modification (or some might say "fiddling") of anomalous results via a customised and rather complex display/editor program.

A further factor was the inescapable fact that no two cells/batteries have exactly the same capacity, for which selection of cells/batteries into capacity-groups is not a perfect solution since capacities are known to change with time. It was decided, for reasons of programming convenience, that during cell/battery test runs all cells/batteries would be cycled using charge-discharge currents specified in a rigid manner as follows: in order to perform a charge/discharge on a given cell/battery at a (nominal) rate of C/x the cell/battery should be supplied/drained with a current of magnitude <nominal-capacity>/x where <nominal-capacity> is the nominal capacity for the type of cell/battery in question and not the true measurable capacity for that particular cell/battery. An alternative method might have been chosen involving the tailoring of charge-discharge currents according to the true capacities as measured in prior tests such that, for example, a nominal "C/10-rate" charge/discharge on a nominal "500mAh" cell known to have a deliverable capacity of 531mAh would involve a current of magnitude 53.1mA. It should be noted, though, that the 7-bit resolution of the Charge-Discharge board current-generators is perhaps too coarse to make this method generally applicable to a worthwhile accuracy (An upgrade to 8-bit resolution is

technically possible with reworking of the Charge-Discharge boards and the Charge-Discharge bus).

The adoption of the alternative charge-current selection method (assuming the accuracy problem to be solved) would have meant that results from cells/batteries of differing true-capacities undergoing nominally similar charge-discharge cycles could be compared directly, for example, by graphical superposition or by point-by-point statistical comparison. However, it was decided that system runs would be programmed in as simple and standard a manner as possible partly since other aspects of run programming and system configuration were already time-consuming and complex and partly to minimise the possibility of irredeemable human errors. Consequently, to perform an accurate comparison of behaviour of several batteries during charge-discharge cycling, it was necessary to normalise results with respect to time in some manner. In practice, this generally required a customised program utilising interpolation methods to create files of normalised data for individual batteries. For test runs involving several phases of charge and/or discharge the situation became extremely complicated since each charge and discharge section generally required its results to be treated separately, rather than the results for the whole run being treated as a single block. A fairly simple normalisation program was written for this purpose but, partly to avoid serious deviation of the research into software matters, an integrated software package for data manipulation was never constructed by the Author.

Conflicts between Needs for Information on Behaviour of Cells/Batteries under Risky or Detrimental Charging Regimes and for the Preservation of such Cells/Batteries

A quite significant conflict of interests was involved in the choice of charge rates for cycling cells/batteries in the rig. At the start of the research programme it was thought that charging currents of, perhaps, as great as 1C might eventually be used to gain useful information on battery impedance and related behaviour. However, at such charge rates cells/batteries would be extremely susceptible to damage through small amounts of excess charging (and very vulnerable through programming error); therefore, attempts at 'intelligently'-controlled charging processes would be risky without a reliable end-of-charge indication method having been developed through experimentation under less vigorous charging regimes. It seemed sensible, though, to subject selected batteries on a few occasions to deliberate and potentially damaging overcharge to observe their behaviour under such conditions. However, and in part due to reservations expressed by potential users of a possible end-product based on the studies, the greatest charging rate used by the Author in practice was C/2.5; this eased the problems considerably.

It was decided that a cautious route be taken in which a wide variety of experiments would initially be done using the C/5 charge rate, which according to the manufacturer (SAFT) of the majority of the cells/batteries being used should not cause nominal damage to the devices even if extended over about twice the normal charging period. The results from such experiments would be studied and used to determine a reasonably effective state-of-charge indicator or, at least, an end-of-charge indicator for charging at the C/5 rate. By applying the charge status

indicator to experiments utilising higher charging currents, by gathering information and then by extending tests to successively higher currents it was hoped that a balance could be achieved between obtaining information and protecting cells/batteries from excessive degradation. In practice, though, the Author never used the cell/battery research rig for fully automated working tests of charge-control algorithms; instead, some such tests were done using a stand-alone charger machine (the "J.P.B./U.C.S." charger - see later Chapters) which was built at the end of the research programme.

Conflicts between the Need for Long-Term Tests on Sets of Cells/Batteries and the Need for a Variety of Tests on a Variety of Devices

A significant conflict of interests was involved in the choice of experiment type and duration. Ideally the battery test rig was required to be used in a variety of operating modes to perform a mixture of experiments and tests (with different charge/discharge rates, different test frequencies, different sequencing of operations, e.t.c.) and to perform tests on a wide variety of cells/batteries (from different manufacturers, of different ages and histories, from different batches, e.t.c.). However, a need also seemed to exist to perform long term charge/discharge cycling of a selected set of batteries over a period of a year or more, during which time the batteries would be analysed using a standardised set of measurements. This scheme would serve the purpose of determining whether the measurements being performed could give any indication of charge-capacity degradation or of possible imminent failure by gradual or catastrophic mechanisms of such batteries, with the view in mind of incorporating a cell/battery quality/condition predictor mechanism

into a possible future practical battery processor.

The two options for cell/battery test rig operation proved to be highly mutually exclusive since early experiments showed that the search for a particularly accurate and dependable state-of-charge indicator would not be an easy one. A considerable amount of time was consequently spent in performing a variety of experiments, sometimes involving only subtle differences in measurement type and strategy. This choice of policy, coupled with the difficulties of general file handling and result analysis and a certain degree of maintenance and improvement of the cell/battery test rig, meant that the Author never had a chance to dedicate an extended period of time for the purpose of performing long-term tests. In any case, a programme of long-term tests on one or two particular cell/battery types might well have proved to have been of little practical value since one of the conclusions of the research was that batteries of differing manufacture do behave in surprisingly different ways from the point of view of impedance-related measurements. The concept of performing long-term tests on a fixed set of batteries might have been more attractive if an early idea of developing an intelligent battery processor capable of recognising individual batteries had been pursued, which it was not.

Conflicts between Experiments for Determination of a State-of-Charge Indicator and for Determination of an End-of-Charge Indicator

It might be thought that experiments aimed at determining an end-of-charge detector for Ni-Cd cells/batteries would simply comprise a subset of the experiments involved in determining a general state-of-charge indicator. However, early experiments showed that measured impedance-related parameters could not be related in a one-to-one manner

to Ni-Cd cell/battery charge state, and showed in particular that cell/battery Effective-Series-Capacitance curves during charging and discharging processes were often very unlike. From a practical viewpoint, for batteries in service a state-of-charge indicator is likely to be of most value for batteries in the course of discharge and for batteries having undergone fairly recent discharge, the function of the indicator being that of determining degree of charge remaining and necessity/urgency for recharging. In contrast, a test for battery end-of-charge is required, virtually by definition, to be applied during a charging process (though a nominal charging process is not necessarily devoid of applications of discharge-direction currents). The Author made a decision to concentrate his attentions on cell/battery response to measurements during charging operations rather than during discharge; this was partly since an end-of-charge indicator was highly desirable for purposes of automation of experimentation and partly since the worth of early results for battery state-of-charge indication was doubtful.

Cell/Battery Conditioning, Storage and Cutoffs

The Author adopted a policy that virgin cells or batteries would always be given three "conditioning" cycles of (16hr charge at C/10)-followed-by-(discharge to cutoff at C/5) prior to experimentation proper in order that the cells/batteries would develop full chargeable capacities and would hopefully develop stable impedance characteristics also. Furthermore, if cells/batteries were ever left unused for a period of greater than a few weeks then they were subjected to at least one conditioning cycle before experimentation was resumed upon them.

In the earlier experiments on single cells a cutoff voltage of about -2.5mV was used although this may seem strange considering that

battery capacities are usually specified with a cutoff of 1 Volt or thereabouts. A cutoff of just under zero Volts has a distinct benefit in that during cell discharge cells can be removed, for example for visual inspection or during system testing, without the overdischarge protection mechanism (via "PROCsafe" - see previous Chapter) being invoked. Considering that the discharge currents used in the earlier experiments were not particularly high, the errors in determinations of cell capacities resulting from the non-standard cutoff would rarely amount to more than a few per cent. When experiments progressed to the stage where multi-cell batteries were being tested a zero-Volt cutoff became wholly inappropriate since this would have caused overdischarge of cells within such batteries. The 1 Volt-per-cell standard was adopted for multi-cell batteries and also for single cells when used for purposes of comparison.

In general, when cells/batteries were 'between runs' or otherwise in disuse they would be left in a discharged state in order to achieve a degree of experimental standardisation; cell/battery test runs were generally configured so as to commence with a charge period and to end with a discharge-to-cutoff. An additional advantage was that cells which had been discharged to zero-Volt cutoff were virtually immune to damage from accidental shorting and were not liable to damage other items with which they might happen to come into contact. Cells and batteries which had been discharged to a 1 Volt-per-cell cutoff required more careful handling.

An Outline of Experiments with Single Cells

A wide range of experiments was done with single Ni-Cd cells using the cell/battery test rig, though some of the initial experiments utilised only 8 Charge-Discharge modules as a result of the rig having not been

fully assembled.

As mentioned earlier, the first experiments done using the cell/battery test rig utilised low, cautious charge rates. Early experiments were also limited exclusively to single cells so that complications involved with multi-cell batteries could be avoided. A group of about 50 new 500mAh "AA" cells, nominally of SAFT manufacture, was bought from a supplier and some "AA" cells of other origins were collected, including some used devices. Some "AA" cells and slightly larger cells were extracted from new and used 8-cell radio handset batteries (See later). During the course of the research some larger cells of SAFT manufacture, including 7Ah "F" devices, were made available and were tested with the aid of a high-current (up to about 6 Amps) programmable current generator which was interfaced to the cell/battery test rig.

Overall, about 50 meaningful test runs were done by the Author using single cells. Early tests on the new SAFT "AA" cells indicated that a very effective end-of-charge indication method was possible for most by monitoring the Imaginary-part impedance at frequencies of about 2Hz. Some of the cells in the original batch, though, exhibited a less favourable response to measurements and were initially considered by the Author to be 'anomalous'. Unfortunately though, it was later realised that the cells which were behaving in a very useful manner were not cells of regular ("regular" being the Author's own term and not necessarily to be taken literally) SAFT manufacture but instead were apparently manufactured in Japan. Upon dissection of the two types of nominally SAFT cell it was found that there were differences in construction, with the Japanese version seeming mechanically inferior. The Japanese cells generally had lower capacities than the regular SAFT versions. A number of PYE P.F.X. battery packs, which seem to contain SAFT cells virtually exclusively,

were dismantled and were found to contain only the regular cell variety. The discovery of the differences between the cells of nominally similar manufacture was rather disappointing and provides a very good example of a major problem associated with the use of impedance-related measurements on Ni-Cd cells/batteries for battery charge control or battery analysis in real-world situations: namely, that cells/batteries may need to be specified specifically for a.c. impedance parameters and response during charging/discharging. This problem was highlighted again when cells (900mAh but of "AA"-cell diameter), were extracted from Motorola battery packs and tested; these cells, which the Author has been told were of National Panasonic (Japan) manufacture, exhibited impedance-component responses of a surprisingly different type to any SAFT cell studied. A certain consolation, though, was that a cell manufactured by VARTA (Germany), a manufacturer which is an official second source for cells used in PYE P.F.X. batteries, exhibited a reasonably similar response to regular SAFT cells.

The Author's early experiments involved the charging and discharging of cells in a simple manner with constant currents such that cells were driven both into overcharge and into full discharge. During such experiments d.c. and a.c. measurements were taken over a wide range of test frequencies with charge/discharge currents suspended during the period of measurement. The experiments which followed were generally tailored according to preceding results and were aimed at improving reliability of measurements and at finding optimum measurement strategies for determining cell/battery state- or end-of-charge. It was found, for example, at a fairly early stage that measurements at frequencies of lower than about 6Hz were likely to provide useful information on cell state-of-charge for cells approaching overcharge.

As well as the effect of variation of measurement frequency, the

influence of less obvious, but potentially significant, factors was studied. One such factor is the length of the rest period between suspension of charge/discharge currents and the commencement of measurements; this is important since a Ni-Cd cell is a complicated electrochemical system involving a wide range of time constants for reactions and diffusions. The existence of many-second or many-minute time constants is evident from the fact that after suspension of a charge or discharge current through a cell the d.c. terminal voltage of the cell takes a considerable time to reach a pseudo-equilibrium state. Another factor which was considered likely to be significant was the magnitude of d.c. current through a cell at the time of a.c. measurement. It was thought that certain d.c. currents might, via creation of electrochemical diffusion gradients within cells or via modification of electrode passivation films, influence impedance-related parameters of cells in a valuable manner; this idea had not been expressed in any positive or explicit manner by previous researchers known to the Author. A range of experiments was thus done in which constant currents were passed, in charge and discharge directions, through cells whilst a.c. measurements (using sinewave-current excitation) were in effect. For most of the SAFT "AA" cells and for some of the larger SAFT cells it was found that a current bias applied in the positive (charge) direction improved response to certain impedance-component measurements in such a way as to make an end-of-charge indicator very easy to implement. Unfortunately though, it was later realised that the "AA" cells which behaved favourably under the positive-bias conditions were the non-regular cells of Japanese origin.

As an intentional deviation from the main course of experiments, some test runs were done in which second-harmonic components of cell response were studied. These experiments, though, seemed to indicate that second-harmonic response was not likely to be worthwhile as a battery

state-of-charge or end-of-charge predictor since it provided no more information than fundamental response and involved additional measurement difficulties.

One point that should be noted concerning experiments done by the Author is that all were done in a standard laboratory environment in which the ambient temperature was not very closely controlled, though was generally in a range comfortable to humans. It had been hoped, originally, that experiments would be done in which cells would be charge/discharge cycled and subjected to measurements at ambient temperatures other than room temperature in order to simulate conditions likely to be encountered in field use of cells/batteries. It should also be noted that the experimentation was often hindered by faults in the test rig, which were gradually corrected during the course of the research; by limitations in the rig (Discussed later); and by inevitable operator errors.

It was realised during the research that Ni-Cd batteries were highly variable in many ways from the point of view of impedance-related measurements. Unlike the simple factors of terminal voltage and charge-holding-capacity which are used generally to specify Ni-Cd cells, the results of impedance-component measurements on such cells were found to be very dependent on aspects of cell internal construction with which the battery user normally needs not to concern himself. It was found that major differences exist in the manner in which cells from different manufacturers behave when subjected to similar impedance-component tests. Furthermore, it seemed likely that different production batches of batteries from a single manufacturer might exhibit significantly different impedance characteristics. In view of the nature of the variations and considering that the concept of a charger capable of recognising individual cells/batteries was unlikely to be realised by the Author, later experiments were aimed mainly at investigating cell response during

charging processes and especially during the approach-to-overcharge phase of charging. Attempts were made to find the measurement conditions which produced the most pronounced and reliable effects for use in end-of-charge determination. Cell charge rates were eventually increased to as high as C/2.5 with measurements being taken at those test frequencies which were considered to be both informative and convenient for practical purposes. It was at this stage that possible end-of-charge algorithms for a practical charger were first contemplated in detail.

As regards the testing of theoretical end-of-charge algorithms, this was never done by the Author using single cells; instead, the experimentation progressed to the use of multicell batteries.

An Outline of Experiments with Multi-cell (8-cell) Batteries

Experiments with multi-cell batteries utilised a maximum of 10 of the Charge-Discharge modules of the cell/battery test rig since a limited number of such batteries, being rather expensive, was available and also since the special 4-terminal contact assemblies that they required were difficult and costly to construct. PYE P.F.X. 500mAh, 600mAh and 800mAh batteries and Motorola (marked "NTN 5048A") 900mAh batteries were investigated, all being 8-cell, 10 Volt types for use in radio communications handsets. These batteries were provided by the Home Office Directorate of Telecommunications.

Experiments mainly comprised repeats of tests done with single cells. It was expected that multicell batteries would respond to impedance-component measurements in much the same manner as single cells, though with impedance components scaled according to the number of cells in series within the battery and with an averaging effect which tends to

mask differences in capacity between cells; this was found to be the case. However, it was thought that, especially at fairly high charge rates, the cells within battery packs would become considerably hotter than single cells during overcharge and that the increased temperature rise might have a significant effect on the trends in cell impedance in the overcharge region.

The Author had originally intended to use the cell/battery test rig to perform test runs which utilised working end-of-charge algorithms; a decision, though, had to be made to suspend this aspect of the research in order to pursue development of a practical stand-alone battery charger (namely the "J.P.B./U.C.S." charger - see later Chapters) for batteries such as PYE P.F.X. types. When completed, the stand-alone charger was used to develop end-of-charge algorithms; the most promising algorithm was eventually put into practice for trials. PYE P.F.X. batteries, which seem to always contain cells from SAFT and of the regular type, do exhibit certain aspects of response to impedance-component measurements during charging which are usable for determining battery end-of-charge to a useful accuracy; the Imaginary-part impedance response to measurements at test frequency of 2Hz is of particularly high value. Motorola NTN5048A batteries, which contain cells of National Panasonic manufacture, were found to exhibit an impedance-component response at 2Hz during charging of a type which makes a reliable end-of-charge algorithm based on 2Hz measurements difficult, if not impossible, to implement.

Infelicities and Limitations of the Research Cell/Battery Test Rig

As mentioned in the previous Chapter, the memory limitations of the B.B.C. Microcomputer combined with a cautious approach to programming

and a desire for a powerful user-interface led to limitations in the timing strategies possible for system runs. It is a simple and convenient matter to perform fast operations, such as modifications of charge-discharge currents, on multiple cells/batteries (pseudo-)simultaneously. Correspondingly, from the point of view of system timings, the most convenient strategy for performing measurements on multiple cells/batteries is one in which measurements are done at preset intervals on all cells/batteries simultaneously. In practice, though, if only one measurement instrument is available then this approach is impossible and measurements must be tackled in a time-sequential manner. A problem arises since multiple measurements and associated special operations consuming many seconds of time may be required on each cell/battery; consequently, when up to 48 cells/batteries are being tested a complete sequence of measurements may consume many minutes of program time. If measurements are done sequentially then the strategy producing the most accurate timings for charge-discharge control and measurement operations is one in which the control program treats cells/batteries in a cyclic manner, devoting equal time periods (or 'slots') to each in turn for the performance of necessary operations. This strategy, though, complicates and makes less convenient the manual control/modification of system operations since different cells/batteries will always be at different stages in any preprogrammed charge-discharge/measurement regime. Furthermore, a division of system-control programs into parts (as was required by the Author due to computer memory limitations) makes this strategy risky to implement if the constituent programs are required to be loaded from floppy disk, the reason being that the strategy forces program exchanges to be very frequent and the probability of 'fatal' hardware data-transfer errors is thus increased.

In practice, when the test rig was in use by the Author all

control programs for the cell/battery test rig were split into separate parts, one for charge-discharge control and one or more for measurement control (as described in earlier Chapters). For simplicity, the RUN-control programs, which dealt with charge-discharge control, utilised a single system clock and performed pseudo-simultaneous programming of all Charge-Discharge modules. The RUN-control programs requested measurement programs (generally at preset constant intervals) in much the same manner as for requests for charge-discharge reprogramming. For simplicity of timings, prior to a request for any measurement program every RUN-control program was made to effectively freeze the system clock and to save its value to a safe memory location. Upon automatic re-entry to any RUN-control program the program was made to reinstate the system clock from the saved value.

Measurement programs normally performed multiple-measurement sequences on cells/batteries and performed a sequence on each cell/battery under control in turn (i.e. a sequence of sequences). Where many cells/batteries are being studied with per-cell/battery measurement sequences which take more than a few seconds the consequent time errors resulting from time-staggering of measurement operations (noting that charge-discharge programming is virtually non-staggered) may become very significant. The degree of influence of timing discrepancies on results of measurements may depend greatly on the degree of complexity of charge or discharge waveforms. For true constant-current charging or discharging the timing inaccuracies may have little effect but for pulse or complex waveforms having cycle times of the order of a minute then problems may result (though this depends on the manner in which the waveform is generated). The problem is complicated by the fact that upon entering a measurement program the primary means of control of charge-discharge currents is lost. For simplicity and program safety, every RUN-control

program used by the Author was made to suspend all charge-discharge currents before requesting any measurement program. After such a request, the control of charge-discharge currents then became entirely the responsibility of the measurement program.

In practice, most measurement programs used by the Author were written so as to maintain zero charge-discharge currents. This was done since measurement programs were vulnerable to failures, involving hardware-related problems, of a type that would prevent the cell/battery test rig from being shut down in a properly controlled manner. However, a disadvantage is present in this method in that the rest period between suspension of charge-discharge currents and the taking of measurements increases for successive cells/batteries. The discrepancies between rest times of different batteries increase with increasing duration of per-cell/battery measurement sequences. It is possible for measurement programs to reinstate all charge-discharge currents on entry and to modify currents programmed for cells/batteries in an individual manner during the course of measurements; however, if this is done then an attempt should be made to ensure that all cells/batteries receive the same amount of charging/discharging during the period in which the measurement program is operative. Furthermore, since the system clock is formally frozen during measurement programs then prior to exit from a measurement program the saved system time value must be modified in such a manner as to compensate for any charging/discharging involved during measurement-program control. Reinstatement and modification of charge-discharge currents by measurement programs was utilised by the Author for some experiments but tended to make measurement program design and implementation somewhat complicated.

Three problems were encountered, with respect to a.c. measurements on cells/batteries, being due to an effect inherent in the cells/batteries which is rendered especially troublesome due to limitations of the a.c.

measurement hardware and the general measurement strategy. The problems are linked to the fact that (as mentioned earlier in this Chapter) a Ni-Cd cell/battery is a complicated electrochemical system which involves some time constants of the order of several seconds and minutes. When a charge-discharge current through a cell/battery is suspended or modified, the d.c. terminal voltage of the cell/battery will normally show some immediate change but may not reach a (pseudo-)steady-state value for many seconds or minutes. Most of the Author's measurement program strategies involved the changing of charge-discharge currents through cells/batteries prior to measurements (Often a current was temporarily suspended). However, in order to minimise measurement program time, long delays for d.c. settling of cells/batteries could generally not be explicitly included; measurements were thus often taken whilst cell/battery d.c. values were still settling.

The most drastic problem is that, for any particular cell/battery, if the d.c. settling rate is sufficiently high during the period in which a.c. measurements are performed (subsequent to a detector d.c. nulling operation) then the cell/battery terminal voltage may drift out of the linear input range of the Detector (which will be in the high-gain A.C. mode). This problem can be lessened by applying a d.c. null trimming operation immediately prior to every a.c. measurement in a sequence. In extreme cases, though, and especially at low measurement frequencies, excessive drifts can occur during the course of a single measurement.

The second but less drastic problem is that the 'd.c. drifting', which is effectively an a.c. effect involving a range of very low frequencies, interferes with a.c. measurements since the d.c. drift becomes superimposed upon the response voltage arising from sinewave excitation during any measurement. It is a simple matter to show that a linear terminal voltage drift will result in a systematic error component

in a Real-part phase-sensitive-detector result wheras it will not introduce an error into an Imaginary-part result; a non-linear terminal voltage drift, though, can introduce an error into both results. By considering the nature of the excitation/detection strategy used by the cell/battery complex-impedance meter (See Chapter 6), it can be seen that the magnitude of an error imparted to an a.c. result will tend to increase with decreasing measurement frequency. Also, by considering relative amplitudes, it can be seen that the magnitude of an error imparted to an a.c. result will tend to increase with decreasing excitation amplitude. In many experiments done by the Author the Real-part battery impedance result was recognised as being spoilt by drift effects but, fortunately, was considered to be a much less useful parameter for practical purposes than the Imaginary-part result. It appeared from experimental results that generally enough time was being allowed between modifications of charge-discharge currents and the taking of measurements such that nonlinearities in drifts were having only a small influence on Imaginary-part impedance results. As regards excitation sinewave amplitudes, these were deliberately kept as low as possible since it was desired that the "small-signal" a.c. characteristics of cells/batteries were to be studied (though the definition of "small-signal" in this case is not well defined). It is possible to introduce a degree of compensation for drift effects into measurements by performing every measurement twice in quick succession whilst reversing the phase of the excitation signal for the second measurement (and reversing the phase of the phase-sensitive detection process correspondingly). The errors induced into the two measurements should be nearly equal in magnitude but of opposite sign; the error term can thus be largely removed if results from the two measurements are averaged. Note though that, to complicate matters still further, it is quite possible that excitation waveforms may interact with d.c. settling

in a non-linear manner such that the phases of initial and subsequent excitation waveforms will influence results (and especially so for single-cycle sine-bursts!). It must be stressed here that few a.c. measurements done by the test rig in practical test or working situations are simple, 'accurate' measurements as might be done by an experimenter working with a few cells/batteries and conventional test equipment and for whom time is not at a severe premium.

A third problem exists which is fairly minor and is fundamentally a side-effect of the d.c. drift effect. The test rig hardware/software is able, via appropriate programming, to autorange its excitation signal amplitude in order to achieve optimum response voltages for individual measurements; for example, in most experiments done by the Author the autoranging mechanism was employed in order to minimise possibilities of Detector overloads. It has already been mentioned that errors caused by cell/battery terminal voltage drifting are dependent on excitation signal amplitude. One consequence is that if an error-cancellation method is not deliberately used (perhaps through the errors involved being small) then for a sequence of measurements, whether in close sequence or whether taken over the course of a test run, variations in excitation amplitudes between individual measurements will result in a degree of apparent 'jitter' in overall results. Another 'unfriendly' result of this effect is that in most test situations associated with practical cell charging or discharging, any attempt to deliberately vary measurement excitation amplitude in order to investigate the specific influence of the parameter will produce inaccurate or ambiguous results.

CHAPTER 10

Discussions of Selected Experiments and of Associated Factors and Conclusions

A large number of experiments was performed by the Author. Some of the experiments were planned repeats, some produced no information that was not already known, some produced results which were suspect or certainly invalid due to programming errors or system malfunctions, and some were connected largely with system testing. Considering that the large volume of numeric results obtained cannot be expressed in a reasonably compact form, no attempt will be made in this thesis to describe in detail all experiments done. Instead, examples of the more informative experiments and groups of experiments will be discussed, together with associated factors and conclusions.

Notes on Experimental Cell/Battery Test "RUNs" and Associated Graphs

Each experimental run done with the research cell/battery test rig was identified by means of a unique "RUN" serial number. Furthermore, experimental runs were categorised into separate series, namely a "zero" series, a "100" series, a "200" series, a "300" series, and so on. Within each series, the serial numbers of individual experiments indicate the chronological order in which those experiments were done.

In the following discussions reference will be made to various example graphs included in this thesis. For all example graphs relating to the research cell/battery test rig the X-axis represents time elapsed since the start of the relevant system run and points are plotted at time

intervals of 10 minutes (600 seconds). It should be noted that in most graphs the scaling of the X-axis is non-constant and is made to vary with charge-discharge rate to obtain a clearer plot; this may be observed by noting the X-separation of plotted points or by studying X-axis annotation. X axes are labelled in units of minutes. For multiple graphs relating to a particular RUN the X-axes of all graphs (which may relate to different cells/batteries or different measured parameters) are identical; this allows easy comparisons between graphs.

It should be noted that no attempt has been made to present a comprehensive set of result graphs in this thesis. The majority of details relating to the included example graphs will be given in discussions in this Chapter.

Each example graph is labelled in a simple manner (via a customised graph-printer program) with the relevant RUN number ("RUNXXX"), Charge-Discharge module number ("Ch-D MODULE XX"), Cell/Battery identification code (e.g. "S4"), a description of the Y-axis function being plotted, and numeric annotations of the X and Y axes. Any graph which contains multiple plots relating to different measurement frequencies has the order of plots indicated above the graph (See "Notes on Graphs 1(a)-13(i)" in the Graph Index for details).

RUNs 5/6/7/8 (See Graphs 1(a-k))

Devices (cells/batteries tested in the RUN) :-

8 of 500mAh SAFT "AA" cell (5 of regular SAFT and 3 of Japanese-SAFT though the distinction was not realised until long after the RUN).

Regime (charge-discharge regime) :-

RUNs 5/6/7:

Charge for 16 hours at C/10 ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current.

RUN8:

Charge for 22 hours at C/10 ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current.

Measurements (measurement sequence in time order) :-

64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz.

Purpose (basic aims of experiment(s)) :-

Early general multifrequency experiments used also to determine if order of cell testing (which affects pre-measurement rest periods) was important. RUN8 also tests the effects of extended overcharge.

Discussions:-

Voltage profiles were much as expected. During charge for all cells a gradual rise to a final plateau occurred and during discharge a gradual decrease occurred ending in a sudden drop. Note (with reference to all d.c. terminal voltage graphs in this document) that the drop to zero volts is not particularly clear in many d.c. terminal voltage graphs since it generally occurs between measurement points and because on termination of a discharge current upon cutoff the d.c. terminal voltage of a cell/battery 'recovers' to near-normal levels fairly rapidly.

Profiles of Effective Series Capacitance (E.S.C.) and Effective Series Conductance (E.S.Con.) were classifiable into two groups with some degree of variation within each group; The grouping was later found to be attributable to the existence of the two types (regular SAFT and Japanese-SAFT) of cell. "S4" is a fairly typical Japanese-SAFT cell and "S6" is a fairly typical regular SAFT cell. For both types of cell an E.S.C. and E.S.Con. is observed which generally increases during charge and generally decreases during discharge.

For Japanese-SAFT cells during charge the E.S.C. at measurement frequencies in the approximate range 2Hz to 32Hz first rises to a medium height plateau after possibly passing a slight peak; on approach to overcharge it rises again to a final plateau after which a gradual decline is observed. As measurement frequency increases the more striking (or 'interesting') aspects of E.S.C. behaviour become increasingly suppressed. E.S.C. profiles for higher measurement frequencies and E.S.Con. profiles for lower frequencies display a noticeable upward step simultaneous with the second 2Hz E.S.C. rapid-rise; it is possible that the E.S.Con. step may be partly attributable to the interactions between E.S.C. and E.S.Con. which are known to be inherent in the measurement method.

For regular SAFT cells during charge the rise-plateau-rise-plateau structure is almost absent though E.S.C. generally reaches a maximum value during extended overcharge. E.S.C. values are generally somewhat higher than for Japanese-SAFT cells.

For all the cells tested (and for all cells/batteries ever tested by the Author) E.S.C was found to decrease with increasing measurement frequency and E.S.Con. was found to increase with increasing frequency; these observations are consistent with an electrical-equivalent model of a cell/battery in which a multiplicity of relaxation effects are present. Furthermore, the more "interesting" features of E.S.C. and E.S.Con. curves, such as sections of rapid rise and peaking effects, become suppressed as measurement frequencies increase.

It is interesting to note that for Japanese-SAFT cells the rise to the final E.S.C. plateau for each cell, best observed at 2Hz, is centred fairly accurately upon the point at which the cell has received a charge equal to its true (individual) capacity; this could form the basis of an end-of-charge indicator.

An important observation is that the E.S.C behaviour of cells

during discharge is at best only a very approximate reversal of that during charge, with the greatest disparities occurring at lower measurement frequencies. During discharge the E.S.C. of all SAFT cells is normally observed to decrease monotonically and "interesting" features, such as peaking, are rare. On a few occasions, though, a limited increase in E.S.C. has been observed to precede the decrease, especially at the lower measurement frequencies.

It was evident during these RUNs that E.S.C. and E.S.Con. profiles for all cells were showing apparent systematic changes with repeated cycling. For the Japanese-SAFT cells the E.S.C. rise-plateau-rise-plateau structure during charge was becoming slightly more pronounced and more useful for purposes of end-of-charge indication. For all cells it appeared that E.S.Con. was generally decreasing with repeated cycling, with the greatest change occurring at the point during charge where cells had received about a 0.6C quantity charge.

In RUN7 (for which results are not included) the order of cell testing was reversed so that pre-measurement rest times for individual cells were different to those used in RUNs 6 and 8. The modified test conditions did have some influence on E.S.C. curves but except for the extreme cases of the first and last cells (in Ch-D modules "0" and "7") the perturbations involved appeared to be of no greater magnitude than the changes apparently occurring with repeated charge-discharge cycling. The slight effect that did exist suggested that for Japanese-SAFT cells a wait of a few seconds before measurements possibly improved the rise-plateau-rise-plateau E.S.C. profile for purposes of end-of-charge determination. Reversal of the test sequence also had a minor influence, as expected, on measured d.c. terminal voltages but the perturbations involved were so small as to be virtually unnoticeable in graph plots.

RUNs 9/10/11/12 (See Graphs 2(a-f))

Devices:-

8 of 500mAh SAFT "AA" cell (5 of regular SAFT and 3 of Japanese-SAFT though the distinction was not realised until long after the RUN).

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/2.5 to 0-Volt cutoff ...

THEN Rest at zero-current.

Measurements:-

32Hz, 16Hz, 8Hz, 4Hz, 2Hz, 1Hz.

Purpose:-

Early experiment using elevated Ch-D rates and multiple frequencies including 1Hz.

Discussions:-

Curves of d.c. terminal voltage, E.S.C. and E.S.Con. for 2,4,8,16 and 32Hz measurements were found to be of the same profile as for the C/10-charge-C/5-discharge case.

For every Japanese-SAFT cell the 1Hz E.S.C. measurements during charge produced an initial peak which almost reached the height of the final plateau. The first plateau, which normally precedes the initial peak, was replaced by a downward incline. Due to the presence of the high initial peak the 1Hz E.S.C. measurements did not appear to be particularly useful for purposes of an end-of-charge indicator based on single-frequency measurements.

For regular SAFT cells a significant E.S.C. initial peak was observed at 1Hz.

For some RUNs, including RUN11, graphs of the function ((E.S.C.)*(E.S.Con.)) were plotted. The resulting plots for Japanese-SAFT

cells at 1Hz and 2Hz are of a particularly pronounced rise-plateau-rise-plateau profile.

RUNs 13/14 (See Graphs 3(a-h))

Devices:-

8 of 500mAh SAFT "AA" cell (5 of regular SAFT and 3 of Japanese-SAFT though the distinction was not realised until long after the RUN).

Regime:-

Charge for 16 hours at C/10 ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current.

Measurements:-

32Hz, 16Hz, 8Hz, 4Hz, 2Hz, 1Hz.

Purpose:-

To check repeatability of RUN5/6/7/8 results and to try 1Hz measurements under the same charge-discharge regime.

Discussions:-

Compared to RUN5/6/7/8 results there existed changes in E.S.C. profiles for all cells tested.

For each Japanese-SAFT cell the average E.S.C. value during charge had changed little but generally the initial peaks had decreased in height slightly and the final plateaus had risen slightly.

For each regular SAFT cell during charge the average E.S.C. value had changed little but the E.S.C. curves had developed an approximate rise-(sloping-plateau)-rise structure. The plateau was preceded by a small peak at lower measurement frequencies and was terminated by a distinct sharp gradient increase prior to the onset of overcharge.

Compared to RUNs 5/6/7/8 there existed changes in E.S.Con.

profiles for all cells tested.

For each Japanese-SAFT cell the E.S.Con. values during most of the charge-discharge cycle were much the same. On the onset of overcharge, however, an obvious upward step in E.S.Con. was occurring even at the higher measurement frequencies and E.S.Con. values during overcharge were significantly higher.

For each regular SAFT cell the E.S.Con. values were much the same on average but the E.S.Con. curve during charge had developed a small upward step at a point corresponding to the E.S.C. gradient sharp increase.

RUN 18 (See Graphs 4(a-n))

Devices:-

8 of 500mAh SAFT "AA" cell (5 of regular SAFT and 3 of Japanese-SAFT though the distinction was not realised until long after the RUN).

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/2.5 to 0-Volt cutoff ...

THEN Rest at zero-current ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

2Hz, 2Hz, 2Hz*, 2Hz^{+}, 2Hz^{+}, 2Hz^{+}*, 2Hz^{-}, 2Hz^{-}, 2Hz^{-}*.

where ($^{+}$) = with +C/5 bias, ($^{-}$) = with -C/5 bias.

Purpose:-

To check effects of bias currents during measurements whilst attempting to observe and to avoid interfering effects of d.c. drifting.

Special note:-

Measurements were done in repeated triplets as a means of

observing the effects of differing degrees of d.c. terminal voltage settling prior to measurements. Each of Graphs 4(a-n) shows results for the third measurement in the relevant triplet (indicated in "Measurements" above by *).

Discussions:-

D.c. bias currents applied during measurements were found to significantly affect E.S.C. and E.S.Con. profiles of all cells during charge and discharge. For purposes of the following discussion it will be assumed that charge, discharge, and bias rates mentioned are as for RUN18.

For Japanese-SAFT cells during charge a +ve bias current depresses apparent E.S.C. and causes the height ratio between the final peak/plateau and the initial peak/plateau to decrease. The E.S.C. profile during charge is thus worsened for purposes of end-of-charge indication (Note that at one stage it was thought that +ve bias currents improved the rise-plateau-rise-plateau structure but this thought was based on results from a cell that was eventually identified as being anomalous and possibly faulty). For Japanese-SAFT cells during discharge a +ve bias current raises apparent E.S.C. and reduces its degree of variation with state-of-charge.

For Japanese-SAFT cells during charge a -ve bias current raises apparent E.S.C. considerably and and causes the height ratio between the final peak/plateau and initial peak/plateau to decrease severely. During discharge a -ve bias current raises apparent E.S.C. considerably but leaves its profile virtually unchanged.

For regular SAFT cells during charge a +ve bias current depresses apparent E.S.C., especially in the region where cells are approaching overcharge. The profile of E.S.C. during charge becomes quite like the rise-plateau-rise-plateau of Japanese-SAFT cells tested with zero-bias; however, a substantial initial peak is always present. For regular SAFT cells during discharge a +ve bias current generally raises apparent E.S.C.

but, instead of decreasing throughout discharge, E.S.C. initially rises to a broad peak and then decreases.

For regular SAFT cells during both charge and discharge a -ve bias current raises apparent E.S.C. considerably but E.S.C. profiles remain largely unchanged.

For Japanese-SAFT cells a +ve bias current depresses apparent E.S.Con. during the first half of charge and raises it during the second half. In the early overcharge region the apparent E.S.Con. may be observed to rise dramatically forming a sharp peak which can overload the measurement-hardware response detector and produce anomalous unprintable results; this occurred in the case of RUN18. This peak is evidently due to d.c. terminal voltage settling effects which become especially pronounced in this region of charging. The height of the peak is very dependent on the time allowed between imposition of the bias current and taking of the measurement.

For Japanese-SAFT cells a -ve bias current depresses apparent E.S.Con. significantly during the first half of charge and during discharge. The depression during charge is evidently largely due to d.c. terminal voltage drift effects and may interact with the autoranging mechanism used in the measurement hardware in such a manner as to produce highly discontinuous profile plots (Graph 4(n) provides a good example of this - the E.S.Con. curve should be pieced-together mentally to obtain a more accurate view - the apparent sudden drop in E.S.Con. is merely an artefact generated by side-effects of the measurement method).

For regular SAFT cells a +ve bias current depresses apparent E.S.Con. during the first half of charge and raises it during the second half. In the early overcharge region the apparent E.S.Con. may be observed to rise dramatically forming a sharp peak. The peak is due to d.c. terminal voltage settling effects, as for Japanese-SAFT cells (See

earlier). During discharge a +ve bias current raises E.S.Con. marginally.

For regular SAFT cells a -ve bias current depresses apparent E.S.Con. during both charge and discharge. Interactions with the measurement-hardware autoranging mechanism may produce fairly severe artefacts in E.S.Con. plots, as for Japanese-SAFT cells (See earlier).

RUN 108 (See Graphs 5(a-p))

Devices:-

1 of 500mAh Japanese-SAFT "AA" cell and 1 of 7Ah SAFT "F" cell.

Regime:-

For "AA" cell "S10" ...

Charge for 7 hours at C/5 ...

THEN Rest at zero-current for 1 hour ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current until 4 hours since the start of discharge ...

THEN (The charge-rest-discharge-rest cycle repeated).

For "F" cell "SF1" ...

Charge for 8 hours at C/5 ...

THEN Discharge at -C/5 to approximately 0.6-1.0 Volt ...

THEN Rest at approximate zero-current until 4 hours since the start of discharge ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

(10s), +/-8Hz, +/-2Hz, (10s), $+/-8Hz^{+}$, $+/-2Hz^{+}$, (10s), $+/-8Hz^{-}$, $+/-2Hz^{-}$.

where (10s) = 10-second wait, (+/-x) = (positive-sinewave-negative-sinewave) measurement doublet, (x^{+}) = with +C/5 bias, (x^{-}) = with

-C/5 bias.

Purpose:-

Fairly comprehensive tests at apparently valuable low frequencies on a small and a large cell with compensations for d.c. drift effects.

Special Notes:-

The hardware used to charge-discharge the "F" cell had an effective dropout voltage of about 0.6 Volt and was generally incapable of maintaining discharge currents at a constant value when cell voltage fell below about 1 Volt. Consequently, the "F" cell does not display a clearly defined cutoff. The discharge current for the "F" cell was allowed to taper off to an approximate zero rather than being terminated by reprogramming the charge-discharge hardware.

In Graphs 5(c-n) horizontal/vertical-arm crosses are used to represent +ve-sinewave measurements and diagonal-arm crosses are used to represent -ve-sinewave measurements.

For this RUN (and for all other two-cycle format RUNs except RUN18) the graphs provided in this thesis show results only for one charge-discharge-rest cycle (which is generally the first cycle).

Due to an incidence of disk corruption at one time the data now available relating to the first charge-discharge-rest cycle of RUN108 is partly corrupted and the results shown in Graphs 5(a-p) are actually those for the second charge-discharge-rest cycle.

Discussions:-

RUN108 was one of the first system RUNs to utilise +ve-sinewave/-ve-sinewave measurement doublets as a means of roughly quantifying and compensating for d.c. terminal voltage drift effects. The effects of such drifting may have extremely pronounced effects on profiles of apparent E.S.Con.; Graphs 5(i,j,m,n) provide good examples. Graphs 5(o,p) also show profiles of E.S.Con. (based on the same results as Graphs 5(i,j,m,n)) but

are compensated for d.c. drifts by means of averaging results from +ve-sinewave and -ve-sinewave measurements. For E.S.C. graphs the deviations between +ve and -ve measurements are fairly small and the average-value curves may easily be pictured mentally.

E.S.C. curves for the Japanese-SAFT cell were much as expected.

E.S.C. values for the 7 Ampere-hour "F" cell were, as expected, an approximate factor of 14 higher than for 500mAh cells but the E.S.C. profile during charge was somewhat intermediate between those of Japanese-SAFT and regular SAFT cells. With a +ve bias current applied during charge the E.S.C. values were depressed and the 2Hz E.S.C. profile showed a near-perfect rise-plateau-rise-plateau structure. With a -ve bias current applied during charge the E.S.C. values were raised and the E.S.C. profile became like that of a typical regular 500mAh SAFT cell.

The E.S.Con. graphs Graphs 5(i,j,n) show very clearly that the use of biases can lead to severe problems in E.S.Con. measurements even if a considerable rest period (in this case at least 10 seconds) is allowed between imposition of a bias current and the taking of measurements. Some sudden steps can be seen in Graphs 5(i,n); these are artefacts arising from side-effects of measurement-system autoranging. A point of interest is that the "F"-size cell was found to be very much more susceptible to drift-induced errors than the (Japanese-SAFT) "AA" cell; it displays a large systematic deviation between +ve-sinewave and -ve-sinewave measurement results which passes through a maximum during early overcharge. In RUN108, unlike RUN18, the pre-measurement wait time was sufficiently large such that overloading of the measurement-hardware Detector unit did not occur.

The (+ve-sinewave/-ve-sinewave)-average-E.S.Con. Graphs 5(o,p) show that the spoiling of E.S.Con. results by d.c. drift effects can be compensated for quite effectively. It should be noted, though, that for

perfect compensation the individual measurements involved in a +ve-sinewave/-ve-sinewave doublet ought to be taken simultaneously, which is a theoretical impossibility.

RUN 200 (See Graphs 6(a-u))

Devices:-

7 of 500mAh SAFT "AA" cell (4 of Japanese-SAFT and 3 of regular SAFT).

Regime:-

Charge for 8.5 hours total at C/5 interrupted by a discharge for 1 hour at -C/5 at a selected point (this phase lasts 9.5 hours total) ...

THEN Rest for 0.5 hour ...

THEN Discharge at -C/5 to 0-Volt cutoff interrupted by a charge for 1 hour at C/5 at a selected point ...

THEN Rest at zero-current.

Measurements:-

(10s), +/-8Hz, +/-2Hz, (10s), +/-8Hz^{+}, +/-2Hz^{+}, (10s), +/-8Hz^{-}, +/-2Hz^{-}.

where (10s) = 10-second wait, (+/-) = (+ve-sinewave/-ve-sinewave) measurement doublet, ($^{+}$) = with +C/5 bias, ($^{-}$) = with -C/5 bias.

Purpose:-

To study the effects of temporary reversals of charge-discharge current on the consistency of trends in E.S.C. and E.S.Con. during charge and discharge.

Special Notes:-

Bearing in mind that each cell rests at zero-current in the region

570-600 minutes and for a period after any incidence of zero-Volt cutoff, the timings of charge and discharge currents for individual cells are fairly obvious upon inspection of the d.c. terminal voltage profile graphs Graphs 6(a,b,c,d,e,f,g).

Cells "S8","S9","S10","S11" are Japanese-SAFT cells with "S9" having somewhat anomalous behaviour.

Cells "S5","S6","S7" are regular SAFT cells. However, the E.S.C. observed for "S5" is depressed during the second half of charge in an apparently anomalous manner; the reason for this is not clear.

Discussions:-

E.S.C. and E.S.Con. profiles are much as might be expected.

E.S.Con. displays a quite significant degree of 'piecewise-reversibility' except, perhaps, for "S9" which is a cell known to have generally anomalous behaviour.

E.S.C. displays less obvious 'reversibility' than E.S.Con. The most significant deviation from 'expected' behaviour occurs if the early stages of discharge (from the fully-charged state) are interrupted by a charge period whereupon, after an initial upward step, the E.S.C. at low frequencies continues to decrease; this behaviour indicates the presence within Ni-Cd devices of a powerful mechanism which has a time constant of greater than 1 hour and which is invoked by the early stages of discharge. It is interesting to note that effects of long time constant are generally associated with side-reactions within Ni-Cd devices such as the breakdown of higher oxides of nickel in the charged positive electrode. Thus, the observation of a long time-constant in E.S.C. response suggests that side-reactions play a very important role in the formulation of E.S.C. response of a Ni-Cd device.

RUNs 300-302, 304-310

Devices:-

48 of 500mAh SAFT "AA" cell (1 of regular SAFT, 37 of Japanese-SAFT), 10 of 500mAh cell (SAFT) extracted from two used PYE P.F.X. batteries.

Regime:-

RUNs 300/301/309/310:

Charge for 8 hours at C/5 ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current ...

THEN (The charge-discharge-rest cycle repeated).

RUNs 302/304/305/306/307:

Charge for a time calculated individually for each cell, by a means based on previous results, at a rate of C/5. ...

THEN Discharge at -C/5 to 0-Volt cutoff but noting the time at which terminal voltage passes 1 Volt ...

THEN Rest at zero-current.

Measurements:-

8Hz, 2Hz, (then possibly repeated with +C/5 bias).

Purpose:-

To identify possible simple end-of-charge indicators and to determine their approximate effectivenesses for use in charging cells (in terms of percentage of charge-holding capacity charged). The strategy used avoided the requirement for putting working end-of-charge algorithms into practice.

Special Notes:-

Some of these RUNs performed measurements with +ve bias as well as measurements with zero-bias; this was accomplished by means of applying

two different measurement programs consecutively. The results of the +ve bias measurements are not particularly valuable and are not discussed below.

Although a 1-Volt terminal voltage cutoff point was used for calculations of cell chargeable and charged capacities, this RUN should ideally have used discharge termination at 1-Volt cutoff so that the starting point for charges was identical to the discharge end-point effectively used for calculations. The use of discharge termination upon zero-Volt cutoff will have introduced a slight error in some calculations; for example calculated results of charge-efficiency will be slightly low, though probably so by less than 1 per cent.

Discussions:-

The strategy used for these RUNs was fairly simple and was designed to identify and simulate testing of possible end-of-charge indicators without requiring charging to be controlled in an unproven automatic manner, such as by a provisional experimental end-of-charge algorithm. The strategy is outlined as follows:-

(A) By using +C/5 charging with overcharge and then discharging to 1-Volt (not zero-volt) cutoff determine the true capacities of individual cells.

(B) By charging each cell with a quantity of charge equal to its true capacity as calculated in (A) and then discharging to 1-Volt cutoff determine the charge-efficiency of each cell (Note that charge-efficiency in the C-quantity charge case is identical to charging-effectiveness as a percentage of true capacity).

(C) Using the results of (A) and (B) and assuming that charge-efficiency is a constant value independent of degree of cell charging (which is highly invalid) estimate the charge required to be given to each cell in order to just charge it fully. Then perform such a charge on each cell and determine the charge effectiveness (capacity charged as a percentage of

true capacity).

(D) Inspect E.S.C. graphs for RUNs done in (B) and (C) and determine if any reliable, 'interesting' features are present at the points where charge has been terminated for each cell. An approximate appraisal may thus be given of possible end-of-charge indicators.

(E) Modify charge times for individual cells either so as to attempt to achieve specific percentage charged capacities or so as to cause charge to be terminated at selected 'interesting' points on E.S.C. profiles. Then perform experiments using the modified charges, make relevant observations and repeat and adjust experiments as necessary. (In practice, the Author did not persevere with this stage).

The most meaningful conclusions of the set of RUNs involved are as follows:-

(i) For Japanese-SAFT cells the charge efficiency of cells charged with unity overcharge factor (i.e. given a charge equal to cell true capacity) varied between 88% and 90% and was 89% on average. The charge efficiencies seem surprisingly good though it should be noted that the cells tested were virtually new and that charge efficiency might, perhaps, degrade with usage.

(ii) For PYE P.F.X. (SAFT) cells the charge efficiency for cells charged with unity overcharge factor varied between 81% and 87% and was 85% on average. It should be noted that the cells tested were well used which might, perhaps, have affected charge efficiency.

(iii) For Japanese-SAFT cells the position of the slight peak which marks the start of the 2Hz E.S.C. final plateau corresponded to the point at which cells were at least about 87% charged and on average about 94% charged relative to their individual true chargeable capacities.

(iv) For PYE P.F.X. (SAFT) cells the point at which zero-bias E.S.C. reached around 9-12 Farads corresponded to the point at which cells were

at least about 80% and on average about 88% charged relative to their individual true chargeable capacities (Note that this cell type has a final peak/plateau occurring too late to be useful for end-of-charge detection).

RUN 315 (See Graphs 7(a-i))

Devices:-

38 of 500mAh Japanese-SAFT "AA" cell, 10 of 500mAh "AA" (SAFT) cell extracted from two used PYE P.F.X. batteries.

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge for 0.5 hour at -C/5 ...

THEN Charge for 2 hours at C/5 ...

THEN Discharge at -C/2.5 to 0-Volt cutoff ...

THEN Rest at zero-current.

Measurements:-

64Hz, 32Hz, 2Hz, (then repeated with +C/5 bias).

Purpose:-

To test the effectiveness of the E.S.C. rise-to-final-plateau feature as an end-of-charge indicator when charging initially near-fully-charged batteries.

Special Notes:-

Two measurement programs were applied consecutively at each (10-minute) measurement point; the first program performed zero-bias measurements and the second program performed measurements with biases. The following discussions and Graphs 7(a-i) relate to zero-bias measurements. The measurements with bias show no particularly valuable or unexpected features and are not discussed below.

Discussions:-

For every cell the half-hour -C/5 discharge following the full charge brought the cell into such a state that resumption of charging produced an E.S.C. rise-to-plateau or rise which was very similar to the final-rise-to-plateau or final rise section normally observed upon early overcharge.

For the Japanese-SAFT cells the second overcharge plateau tended to be at a slightly lower level than the initial overcharge plateau. Considering also that overcharge plateaus for these cells have a slight downward gradient, a plausible explanation for this observation is that E.S.C. decreases as cell internal temperature rises during extended overcharge. However, other explanations involving electrochemical side-reactions are possible (c.f. the discussion of RUN200).

For the few P.F.X. (SAFT) cells which had reached an E.S.C. plateau during the initial overcharge period the second overcharge led to an E.S.C. plateau at a slightly higher level; for the other P.F.X. (SAFT) cells E.S.C. rose above previous attained values and reached a plateau in some cases.

The most significant result, which applies to all cells (and apparently to all SAFT cells that the Author has ever tested), is that the rapid-rise feature in low-frequency (about 2Hz) E.S.C. occurs upon overcharge even for cells that are initially nearly fully charged. Thus, it is evident that the 2Hz E.S.C. rise-to-final-plateau feature could form the basis of a fairly simple end-of-charge indicator for an intelligent-charging scheme. It should be borne in mind, though, that unless special precautions are taken then a necessity exists for part-discharging all cells prior to charging-proper to ensure that already-fully-charged cells will respond in a favourable manner.

RUN 400 (See Graphs 8(a-z))

Devices:-

1 of 450mAh (estimated) "AA" cell from a Casio calculator, 6 of 500mAh Japanese-SAFT "AA" cell, 1 of 500mAh regular SAFT "AA" cell, 8 of 500mAh "AA" cell extracted from two used (second-generation) PYE P.F.X. batteries, 1 of 500mAh VARTA "AA" cell, 3 of 500mAh "AA" cell from a Hewlett-Packard calculator, 1 of 500mAh SAFT "VT"-series (high-temperature) "AA" cell, 3 of 600mAh SAFT "VE"-series (high capacity) "AA" cell, 24 of 600mAh "AA" cell extracted from three new (third-generation) PYE P.F.X. batteries.

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/5 to 0-Volt cutoff ...

THEN Rest at zero-current until 4 hours since the start of discharge ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

32Hz, 2Hz, 2Hz.

Purpose:-

Tests on a variety of "AA"-size cell types at apparently valuable frequencies with duplication of 2Hz measurements to check consistency.

Special Notes:-

With reference to Graphs 8(a-z), cells of name "CCxx" are 450mAh (estimated) via Casio, cells of name "PPxx" are 500mAh (SAFT) cells extracted from used (second-generation) PYE P.F.X. batteries, cells of name "VAxx" are 500mAh VARTA, cells of name "HPxx" are 500mAh via Hewlett-Packard, cells of name "SVTxx" are 500mAh SAFT "VT"-series, cells of name "SVExx" are 600mAh SAFT "VE"-series, and cells of name "P6Pxx" are 600mAh

(SAFT) cells extracted from new (third generation) PYE P.F.X. batteries.

E.S.Con. was not studied in this RUN.

Discussions:-

600mAh P.F.X. (SAFT) cells were found to exhibit fairly similar characteristics to the 500mAh variety but with E.S.C. values scaled up in a manner approximately proportional to capacity. A fair degree of variation existed between individual cells in the slopes of 2Hz E.S.C. near overcharge; some cells displayed a distinct gradient increase upon overcharge whilst for others the gradients prior to and following the onset of overcharge were virtually indistinguishable. The Author had expected that the SAFT "SVE" cells would have virtually identical characteristics to the 600mAh P.F.X. (SAFT) devices but this was found not to be the case. For the three "SVE" cells tested an approximate rise-plateau-rise-plateau profile was observed for 2Hz E.S.C. during charge in which the initial plateau/peak was exceptionally high; the behaviour was rather like that of some SAFT cells when tested with -ve bias.

The SAFT "VT" (high-temperature) cell displayed a 2Hz E.S.C. profile during charge comprising an initial broad peak followed by a fall to a plateau and then a rise to a final plateau. The final plateau was considerably lower than for other types of SAFT cell and during continued overcharge the E.S.C. descended gradually towards the level of the initial peak.

The VARTA cell exhibited characteristics fairly similar to those of regular SAFT cells except that the initial 2Hz E.S.C. plateau was rather high.

The cells obtained via Hewlett-Packard (from a calculator battery pack) exhibited a low-frequency E.S.C. profile of a type that had not been seen before (but was seen later in cells via Motorola). During charge the 2Hz E.S.C. rose, fell and rose again in a gradual manner with final E.S.C.

sometimes being lower than the value reached in the initial broad peak. Between individual cells some considerable variations were present in absolute E.S.C. levels; this may be attributable to the fact that the cells had been very heavily used and were probably failing. For these cells it seemed that an accurate end-of-charge indicator based on measurements at 2Hz or higher was an unlikely proposition.

The cells obtained via Casio (from a calculator battery pack) showed characteristics vaguely similar to the Hewlett-Packard cells though the degree of variation of 2Hz E.S.C. during both charging and discharging was very limited.

RUN 500 (See Graphs 9(a-p))

Devices:-

2 of 4Ah SAFT "D" cell, 4 of 2Ah SAFT "C" cell, 8 of 850mAh 'stretched-AA' cell (SAFT) extracted from one new 850mAh PYE P.F.X. battery, 8 of 900mAh 'stretched-AA' cell (National Panasonic) extracted from one new Motorola battery.

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/2.5 to 1-volt-per-cell cutoff ...

THEN Rest at zero-current until 4 hours since the start of discharge ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

32Hz, 2Hz, 2Hz.

Purpose:-

Tests on a variety of cells other than "AA" types at apparently valuable frequencies with duplication of 2Hz measurements to check

consistency.

Discussions:-

2Hz E.S.C. profiles for the SAFT "C" and "D" cells were very much of the Japanese-SAFT cell type and had a near-ideal rise-plateau-rise-plateau structure. However, the E.S.C. values were 2-2.5 times higher than might have been expected from scaling up E.S.C. proportional to cell capacity with a typical 500mAh Japanese-SAFT cell used as a reference. If heights of final plateaus are considered then final E.S.C. is proportional to cell capacity to a reasonable accuracy provided that a typical 500mAh regular SAFT cell (if overcharged until it does reach an E.S.C. plateau) is used as a reference. The final rise in E.S.C. upon overcharge for 32Hz measurements appeared to be entirely suppressed for one of the Author's "D" cells.

The PYE P.F.X. (SAFT) 850mAh cells displayed 2Hz E.S.C. profiles similar to the SAFT "C" and "D" cells but with E.S.C. scaled down reasonably accurately in a manner proportional to capacity.

The Motorola 900mAh "stretched-AA" cells were found to display E.S.C. profiles quite unlike those of any cells previously tested with the exception of three cells obtained via Hewlett-Packard (See RUN400). During the charging process the 2Hz E.S.C. rises, falls and rises again in a gradual manner with final E.S.C. sometimes being lower than the value reached in the initial broad peak. The Motorola cells are believed to have been manufactured by National Panasonic (Japan); the Hewlett-Packard cells may have similar origins since they exhibit virtually identical qualitative E.S.C. profiles. In comparison with the near-equivalent PFX (SAFT) 850mAh cells the average E.S.C. of the 900mAh Motorola cells is smaller by a factor of about 4-5.

The E.S.Con. of Motorola cells increases during charge and decreases during discharge in a generally more linear manner than for SAFT

cells. In comparison with the near-equivalent PFX (SAFT) 850mAh cells the average E.S.Con. of 900mAh Motorola cells is lower by a factor of about 2.

RUNs 601/602 (See Graphs 10(a-f))

Devices:-

10 of new PYE P.F.X. 600mAh battery (8-cells in series with cells by SAFT).

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/2.5 to 1-volt-per-cell cutoff ...

THEN Rest at zero-current until 4 hours since the start of discharge ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

64Hz, 32Hz, 2Hz, 2Hz.

Purpose:-

Tests on 600mAh PYE P.F.X. battery packs at apparently valuable frequencies with duplication of 2Hz measurements to check consistency.

Discussions:-

The Author had expected that the 8-cell battery packs would have E.S.C. profiles qualitatively very similar to those of the corresponding single cells (See RUN400); this turned out not to be entirely the case. Wheras the single P.F.X. (SAFT) cells tested previously had given responses without obvious initial plateaus, the batteries which were tested displayed a very obvious rise-plateau-rise-plateau structure. It should be noted that apart from the addition of a 64Hz measurement to the measurement sequence and a reduction in the average pre-measurement rest time for RUNs 601/2 the measurement conditions for the single-cell and

battery RUNs were the same. Various explanations are possible for the difference in behaviour; perhaps variations exist between cells and the Author had been unlucky enough to extract single cells for testing from a battery containing a less common cell variant, or perhaps the effect is associated with the rise in temperature of cells during charge which is accentuated by placing many cells in close proximity in a battery pack, or perhaps an unknown flaw in the measurement hardware was being uncovered. The temperature-based explanation, though, seems the most plausible. It is interesting to note that E.S.Con. for most of the batteries tested displayed a decrease just prior to the onset of overcharge and showed little or no rise during overcharge; this suggests that some effect is causing the 'expected' E.S.Con. curve to become increasingly depressed from about the 0.7C-quantity charge point onwards. The E.S.Con. behaviour for batteries, as opposed to single cells, seems consistent with a hypothesis that an increase in battery internal temperature is occurring and is significantly influencing cell internal electrochemistry. It is fairly obvious from d.c. terminal voltage profiles that a greater temperature rise is occurring during overcharge than for the single-cell situation; the d.c. terminal voltage for P.F.X. batteries decreases quite significantly during overcharge due to the (well known) negative temperature coefficient.

Results indicated that, for purposes of possible end-of-charge methods for use with PYE P.F.X. 600mAh batteries, 2Hz E.S.C. seems to be of potential value due to the presence of a marked, repeatable change at the onset of overcharge. It should be noted, though, that the batteries tested by the Author had similar dates of manufacture and, thus, may not serve as a generally representative sample.

RUNs 604/605/606/610 (See Graphs 11(a-n))

Devices:-

10 of new PYE P.F.X. 600mAh battery (cells by SAFT).

Regime:-

Charge for 8 hours at C/5 ...

THEN Discharge at -C/2.5 to 1-volt-per-cell cutoff ...

THEN Rest at zero-current until 4 hours since the start of discharge ...

THEN (The charge-discharge-rest cycle repeated).

Measurements:-

RUN604: 32Hz, 16Hz, 8Hz, 4Hz, 2Hz.

RUN605: 8 ,8 ,8 ,8 ,8 ,8 ,8 ,8 (Hz).

RUN606: 4, 4, 4, 4, 4, 4, 4, 4 (Hz).

RUN610: 2, 2, 2, 2, 2, 2, 2, 2 (Hz).

(Second-harmonic response recorded for all)

Purpose:-

Investigations of second-harmonic response of batteries especially at low frequencies.

Special Notes:-

It is an unfortunate fact that capacitor "standards" of size of the order of 1 Farad are not readily available (if indeed they exist - a "stacked film" type 1 Farad polycarbonate capacitor would need to be about the size of an office filing cabinet!). It was thus impossible for the Author to test accurately for interactions, resulting from imperfections in the measurement hardware, which might cause fundamental response to contribute to some degree to apparent harmonic response. Due to the fact that nonlinearities of battery response are not particularly extreme, the accuracies of second-harmonic response measurements will generally suffer

errors via imprecisions in the measurement method to a rather greater extent than will fundamental response measurements. Tests done with a nearly-non-inductive resistor as a dummy load indicated that the 'phantom' second-harmonic response produced under these conditions was of an order of about 2000 less than fundamental response.

Graphs 11(a-n) are best considered in conjunction with Graphs 10(a,b) which have similar time axes.

Each of Graphs 11(a-n) shows a full set of superimposed measurement results for each measurement time-point; this format highlights noise and drift problems involved in these measurements.

Discussions:-

At each measurement frequency, Second-Harmonic-Transcapacitance (See Appendix 2) for batteries varied in much the same manner as E.S.C. and Second-Harmonic-Transconductance (See Appendix 2) varied in a fairly similar manner to E.S.Con..

Second harmonic response of the batteries was found to be smaller than fundamental response by a factor of about 30-50 which led to noise problems in measurements. Transcapacitance measurements seemed to suffer greater problems of random fluctuations than Transconductance measurements.

Transconductance measurements were highly sensitive to d.c. drifts in a systematic manner. In each RUN, for those batteries which had charge-discharge currents suspended for less than about 20 seconds before commencement of measurements a discernable set of 8 curves appeared in Transconductance plots which corresponded to the 8 consecutive same-frequency measurements. The individual curves were not spoiled to a significant degree by noise. For batteries which had charge-discharge currents suspended for more than about 20 seconds there still seemed to exist a set of curves; for each battery these curves appeared to tend

towards a final position in a manner suggesting that battery average terminal voltage was settling to an equilibrium state appropriate to the intermittent excitation conditions (These curves are too close to be identified clearly in a superimposed-plot form).

Second-harmonic response does not appear to provide much more useful information on cell/battery state-of-charge than is provided by fundamental response; furthermore, it appears not to be a particularly suitable technique for real-world battery analysis due to measurement difficulties. However, it is interesting to note that 2Hz Second-Harmonic-Transcapacitance profiles are qualitatively more like profiles of 2Hz E.S.C. for single 600mAh PFX (Saft) cells than like profiles of 2Hz E.S.C. observed for battery packs; this suggests, perhaps, that the mechanism responsible for the difference in response between single cells and multi-cell batteries does not greatly influence those electrochemical effects within Ni-Cd devices which cause nonlinearity of imaginary-part electrical response.

CHAPTER 11

Conclusions of the Research as Applicable to State-of-Charge and End-of-Charge Determination for Contemporary Commercial Sealed Sintered Ni-Cd Cells and Batteries

General Conclusions

The following general conclusions and related points can be made with reasonable certainty though it should be noted that the temperature dependence of effects studied has not been ascertained because all experimental runs have been done at or near 'room' temperature:-

(i) The Effective-Series-Capacitance and Effective-Series-Conductance of a Ni-Cd cell/battery are highly dependent on measurement frequency (as was known previous to the Author's research).

(ii) The Effective-Series-Capacitance and Effective-Series-Conductance of a Ni-Cd cell/battery are not related in a direct manner to the state-of-charge of the cell/battery but are dependent, especially at sub-audio measurement frequencies, on the recent charge-discharge history of the cell/battery. Within Ni-Cd devices effects are present that have characteristic time constants of greater than an hour. (Note that this last observation is consistent with the knowledge that side-reactions, such as breakdown of higher oxides of nickel, occur with characteristic decay periods of hours or days).

(iii) There may exist very significant differences between

characteristic impedance-parameter-versus-charge/discharge curves for cells from different sources, for example National Panasonic (the source for the Author's Motorola NTN5048A batteries) versus SAFT. Certain cell types may behave very favourably with respect to end-of-charge indication at certain measurement frequencies whereas others have poor responses. The reasons for this probably involve subtle differences in the physical structure and chemical composition of electrodes. It is quite possible that chemical side reactions or pseudo-reactions, which are not normally of interest to battery users, are responsible for some of the more 'interesting' aspects of Ni-Cd cell/battery response to complex impedance measurements.

(iv) For cells or batteries from a given manufacturer it is possible that significant differences may exist in cell/battery impedance-component response between cells/batteries from different production batches. These differences may be of sufficient magnitude as to make the use of impedance-component measurements risky for purposes of battery analysis unless cells can be specially selected so as to conform fairly closely to a 'standard' impedance-component response curve or, alternatively, unless characteristic impedance-component response curves can be recorded and applied for individual cells/batteries. If cells are not specially selected for impedance-component response in a general manner and if cells are required to be assembled into multi-cell battery packs which are to be analysed or charged using impedance-component measurements then, depending on the exact nature of impedance-component based analysis or end-of-charge determination methods to be used, it may be advisable to match cells within each pack for impedance-component characteristics (in a similar manner to which cells used in battery packs are matched for charge-storage capacity) if results are to be obtained with confidence. (As an example of

this last point, consider the case of an 8-cell battery constructed from Japanese-SAFT cells. If the cells are matched such that their 2Hz E.S.C. rise-to-final-plateau rises occur near-simultaneously during a charge of the battery then the battery as a whole should display a well-defined 2Hz E.S.C. rise-to-final-plateau during charging. If, however, the cells are poorly matched then the battery 2Hz E.S.C. rise-to-final-plateau is likely to be of low gradient and to be poorly defined).

(v) Considering all single cells studied, Effective Series Conductance shows rather greater variation between individual cells than does Effective Series Capacitance. However, for some types of SAFT cell tested, the degrees of variation of E.S.Conductance and E.S.Capacitance were similar and amounted to worst-case variations of about 20% around the mean value. Inspection of impedance-component-versus-charging/discharging curves indicates that the existence of such variations implies that a simple impedance-component-measuring battery processor without memory of individual cells/batteries will be incapable of indicating Ni-Cd state-of-charge to better than, perhaps, 30%; such an accuracy is not exceptionally helpful.

(vi) It seems likely that test frequencies in the range 2Hz to 32Hz are most suitable for a practical battery processor based on impedance-component measurement techniques for batteries of SAFT manufacture. Variations in impedance parameters near end-of-charge become especially pronounced for SAFT cell types at frequencies lower than 4Hz but measurements at about 32Hz may also provide valuable information.

(vii) It appears that for purposes of end-of-charge indication the application of -ve-direction (discharge-direction) d.c. current bias

during measurements is not helpful and that application of +ve-direction (charge-direction) bias is generally not helpful, with the possible exception of the case of SAFT cells of large capacity. It should be noted that even if such biases improve characteristic curves in certain cases they may spoil result consistency or reproducibility in practical situations unless great care is taken to define bias-current magnitudes and measurement timings in a strict manner.

(viii) Second harmonic responses of cells/batteries appear generally to be smaller than fundamental responses by a factor of about 30-50. This creates considerable noise and drift problems for practical measurement strategies utilising second harmonic response. Second-harmonic response does not appear to provide significantly more useful information on cell/battery state-of-charge than fundamental response.

(ix) Measurements of Effective-Series-Capacitance are preferred to measurements of Effective-Series-Conductance in a practical situation for the following reasons. Firstly, cell conductance depends to some extent on the degree and integrity of bulk electrical connections within the cell but these are not at all related to cell state-of-charge. Secondly, contact resistances between cell/battery terminals are inconsequential to a first approximation in the nominal "Effective-Series-Capacitance" measurement; this may enable simple two-terminal measurements to be utilised (as opposed to the four-terminal system adopted in the research test system) which simplifies battery contacts and hardware considerably.

(x) It seems probable that for typical cells of SAFT and VARTA manufacture and for multicell batteries containing such cells it will be possible to develop an effective intelligent battery charger incorporating

end-of-charge sensing via an algorithm based partly on trends in Effective-Series-Capacitance and partly on absolute Effective-Series-Capacitance values. The end-of-charge sensing method is likely to be sufficiently reliable that batteries may be charged from any initial charge state in periods of a few hours whilst only rarely producing harmful excess overcharging. It may be possible to develop a similar charger based on measurements at 2Hz and higher for cells of National Panasonic manufacture and for multicell batteries containing such cells but the charging process may be required to contain a discharging phase and the charging algorithm is likely to be rather less reliable than for SAFT or VARTA devices (but see Chapter 15 also).

(xi) For a practical intelligent battery charger of a type having no ability to recognise individual batteries it will almost certainly be necessary to tailor measurement types and state/end-of-charge determination algorithms to suit each particular battery type from each battery manufacturer. This, unfortunately, may create problems if semi-compatible batteries of differing nominal capacities (such as PYE P.F.X. 600mAh and 800mAh types) are available for a particular application or if batteries used for a particular application are sourced by more than one manufacturer.

Possible End-of-Charge Algorithms

The Author considered a number of algorithms to use for the purpose of defining a practical end-of-charge point for single-cell charging at rates greater than C/10. With reference to Graphs 12(a,b) three of these algorithms are outlined below.

Algorithm "A"

Major notes:-

- For Japanese-SAFT cells only.
- Uses zero-bias (or possibly +ve bias) measurements.
- Uses 2Hz measurements only.

Notes:-

- Refer to Graph 12(a).
- "C_2" is used to represent 2Hz E.S.C.
- The main problem is that of distinguishing phase (v) from phase (i).

Algorithm Main Components:-

(1) IF { C_2 > LIMIT1 AND (dC_2/dt) > SLOPE1 } for a time duration TIME1 THEN phase (v) is in progress.

(2) IF phase (v) has been passed AND { (dC_2/dt) < SLOPE2 for a time duration TIME2 } THEN terminate charge.

Additional Provisos:-

For the algorithm to work with cells of all initial states of charge including fully-charged it is necessary EITHER to give all cells a discharge of about C/20-quantity prior to charging to ensure that phase (v) always occurs (this discharge should be truncated if voltage cutoff occurs) OR to include a second termination condition as follows:

(3) IF { C_2 > LIMIT2 AND (dC_2/dt) < SLOPE2 } for a time duration TIME3 THEN terminate charge.

An overall time limit should be imposed, in case any cell behaves in such a manner as to fail to satisfy the end-of-charge algorithm conditions, as follows:

(4) IF charge-time duration > TIME4 THEN terminate charge

Values of Parameters:-

Inspections of certain graphs indicate that for a charge rate of

C/5 (which is not particularly high) the following values may be suitable:

LIMIT1 = 5.2 Farad

LIMIT2 = 5.7 Farad

SLOPE1 = (fairly critical)

SLOPE2 = (fairly critical)

TIME1 = 10 minutes

TIME2 = 10 minutes

TIME3 = 20-30 minutes

TIME4 = 8 hours (dependent on the degree of cell overcharge protection)

Algorithm "B"

Major notes:-

- For regular SAFT cells only (and possibly VARTA cells)
- Uses zero-bias (or possibly +ve bias) measurements.
- Uses 2Hz measurements only.

Notes:-

- Refer to Graph 12(b).
- "C_2" is used to represent 2Hz E.S.C..
- The main problem is that no pronounced feature exists at early overcharge that is consistent between cells.

Algorithm Main Components:-

(1) If { C_2 > LIMIT3 AND (dC_2/dt) < SLOPE3 } for a time duration TIME5 THEN terminate charge.

(2) If C_2 > LIMIT4 for a time duration TIME6 THEN terminate charge.

Additional Provisos:-

An overall time limit should be imposed, in case any cell behaves in such a manner as to fail to satisfy the end-of-charge algorithm conditions, as follows:

(3) IF charge-time duration > TIME7 THEN terminate charge.

Values of Parameters:-

Inspections of certain graphs indicate that for a charge rate of C/5 (which is not particularly high) the following values may be suitable:

LIMIT3 = 8.5 Farad

LIMIT4 = 9-10.5 Farad

SLOPE3 = (fairly critical)

TIME5 = 10 minutes

TIME6 = 10 minutes

TIME4 = 8 hours (dependent on the degree of cell overcharge protection)

Algorithm "C"

Major Notes:-

- For both Japanese-SAFT and regular SAFT cells.
- Uses zero-bias (or possibly +ve bias) measurements.
- Uses 2Hz and 32Hz measurements.

Notes:-

- Refer to Graphs 12(a) AND 12(b).
- "C_2" is used to represent 2Hz E.S.C. and "C_{32}" is used to represent 32Hz E.S.C..
- The main problem is that of distinguishing phase (vii) of Japanese-SAFT cells from phase (iii) of regular SAFT cells.

Algorithm main components:-

(1) IF { C_2 > LIMIT1 AND (dC_2/dt) > SLOPE1 AND C_{32} > LIMIT5 } for a time duration TIME1 THEN phase (v) of a Japanese-SAFT" cell is in progress.

(2) IF phase (v) of a Japanese-SAFT cell has been passed AND { (dC_2/dt) < SLOPE2 for a time duration TIME2 } THEN terminate charge.

(3) IF { C_2 > LIMIT3 AND {(dC_2/dt) < SLOPE3 } for a time duration TIME5

THEN terminate charge.

(4) IF C_2 > LIMIT4 for a time duration TIME6 THEN terminate charge.

Additional Provisos:-

All cells should be given a discharge of about C/20-quantity or to cutoff, whichever occurs sooner, prior to charging.

An overall time limit should be imposed, in case any cell behaves in such a manner as to fail to satisfy the end-of-charge algorithm conditions, as follows:

(5) IF charge-time > TIME7 THEN terminate charge.

Values of Parameters:-

Inspections of certain graphs indicate that for a charge rate of C/5 (which is not particularly high) the following values may be suitable:

LIMIT1 = 5.2 Farad

LIMIT3 = 8.5 Farad

LIMIT4 = 9-10.5 Farad

LIMIT5 = 1.6 Farad

SLOPE1 = (fairly critical)

SLOPE2 = (fairly critical)

SLOPE3 = (fairly critical)

TIME5 = 10 minutes

TIME6 = 10 minutes

TIME4 = 8 hours (dependent on the degree of cell overcharge protection)

Other Discussions and Conclusions

Additional discussions and conclusions are included in the "Discussions" sections of individual experiments in Chapter 10. Some of the points made in each section are best considered within the context and regime of the associated experiment and the reader should be cautious if

inferring conclusions which are not explicitly stated. One of the more unfortunate conclusions of the experimentation is that the analysis of cells and batteries by impedance methods is a rather inexact science plagued by anomalies and ambiguities. The example graphs included in this thesis relating to the research cell/battery test rig have been selected to give a general impression of the normal variations between responses of individual cells and batteries but do not show the most severe and problematic cases. The reader should maintain an appreciation that the nominal "impedance-component" methods used by the Author produce results which can be influenced significantly, though in a systematic manner, by the charge-discharge conditions in force prior to and during measurements. For more detailed discussions and conclusions to be obtained a specific charge-discharge regime needs to be considered; the case of the "J.P.B./U.C.S." stand-alone charger provides an example where finer points of observations are discussed (See Chapter 14), though the treatment is still largely qualitative.

CHAPTER 12

Development of the J.P.B./U.C.S. Charger for PYE P.F.X. Radio Communications Handset Batteries

Background to the Development of the Charger

An experimental circuit was devised by the Author, incorporating novel analogue electronics, for measuring the imaginary component of Ni-Cd battery impedance (which is inversely proportional to battery Effective-Series-Capacitance) at frequencies of 2Hz, 8Hz and 32Hz. With the aid of an undergraduate student, the circuit was constructed in printed circuit board form. It was initially thought that the board would be incorporated into a simple demonstration unit controlled from a computer or a dedicated microprocessor. However, it was realised that by including a current generator within the demonstration unit an intelligent single-battery charger could be obtained for experimentation and demonstration purposes. The Author constructed a controller board based on a 6303 microprocessor for the measurement board; the controller board was initially very simple but was designed in such a manner that considerable hardware expansion was possible.

It was later decided, in consultation with the Home Office, that a full-specification prototype charger for PYE P.F.X. 600mAh batteries would be built, based upon the newly developed circuit boards. The principles of operation and the charge regime of the unit would be optimised to suit an 8-hour shift system of battery usage whilst allowing a moderate degree of flexibility. The charger was intended to be used at least for purposes of demonstration and possibly for field trials and data collection.

General Details of the J.P.B./U.C.S. Charger

In order to produce an instrument of robust nature and professional appearance a dump-charge based batch charger for PYE P.F.X. batteries, type "BP12/81C MKII" manufactured by Stoneleigh Electronics (U.K.), was acquired and converted to house the Author's hardware. The conversion process took 3-4 months since new circuit boards had to be developed and tested, a certain amount of chassis modification was required for mounting the new components and the wiring strategy was critical in parts. The machine when completed was basically a prototype as it incorporated seven separate circuit boards, of which two were of printed construction, two were wirewrapped and three were on stripboard; the consequent inter-board wiring layout was not particularly convenient. However, the internal construction was of a quality such that the machine could be expected to operate for many years in service use. The prototype charger was provided with an RS-232 serial-out interface (without handshake control) for purposes of outputting status and measurement data to an external computer. This facility would enable the charger to form part of a data-logging facility which could be of great value for conducting long-term tests on batteries and tests of the long-term effectiveness of the charger in practical use.

The software for the charger, which was written in machine code, took several months to develop and was written in as intelligible and highly-commented a manner as possible so as to allow future modification and development by persons other than the Author.

A partial description of the charger, which will hereforth be referred to as the "J.P.B./U.C.S." charger, with particular reference to its user-interface and charging regime, follows.

Externally the charger looks very much like a conventional charger

of Stoneleigh manufacture except that it has only 10 (as opposed to an original 12) battery sockets and has a control panel with different styling and functions. Each battery holder has next to it a bi-colour "Battery-Status" l.e.d.. When lit continuous-green a Battery-Status l.e.d. indicates that the associated battery is nominally charged and usable; a flashing-red l.e.d. indicates that the associated battery is not sufficiently charged for use and should not be removed. The control panel contains a l.e.d.-illuminated yellow "UPDATE" button for use by general users of the charger and a red "RESET/IDENTIFY" button. The red button can be lit by means of a l.e.d. and has special functions that most users of the charger normally need not concern themselves with. The control panel also contains a "BAD-BATTERY" warning l.e.d. which can be lit flashing-red to provide a warning to the user in connection with certain battery-serviceability tests that can be done by the charger.

The J.P.B./U.C.S. charger is controlled by an internal 6303 microprocessor provided with R.O.M. (up to 32kbytes) containing a control program and data and provided with battery-backed R.A.M. (up to 16kbytes).

The charger operates on up to 10 batteries at a time in a mutually independent manner such that batteries may be inserted into sockets at any time provided that a standard procedure is adopted by the user. As the J.P.B./U.C.S. charger incorporates a method for sensing battery end-of-charge it is possible for a user to insert batteries of any initial state-of-charge (including fully-charged) into the machine without risk of significant damage.

The charging regimes eventually tested for the J.P.B./U.C.S. charger involved giving individual batteries an initial (fairly) "Fast" charge at the C/2.5 rate which was nominally terminated by the end-of-charge algorithm but which had a time limit of about 4 hours imposed. The batteries were then subjected to a "Top-Up" charge at the "standard" C/10

rate and, if not removed from the charger by a user, were transferred to an intermittent C/10 "Maintenance" charge after a further period of a few hours. It was intended that the duration of the initial C/4-rate charge would be such as to generally charge batteries to at least 80% of their nominal capacities; under such conditions any remaining chargeable capacity could be largely topped-up by a few hours of C/10-rate charging.

A considerable amount of work was required to select and refine an effective end-of-charge algorithm for use by the charger. Prior to construction of the J.P.B./U.C.S. charger, PFX batteries had been found to display a Effective-Series-Capacitance which generally increased during charge. Also, it had been found that the variation in absolute value of series-capacitance between batteries (of equivalent states-of-charge) was generally only about 12%. These two facts suggested possibilities of viability for a simple algorithm involving a single-frequency measurement with charge termination occurring upon a preset E.S.C. threshold being exceeded for a few consecutive measurements. Early experiments, though, indicated that a simple threshold method was rather imprecise; hence, in order to avoid possible inadequate charging of batteries the capacitance threshold would have to be set rather higher than might be expected. The use of a high capacitance threshold increases the risk of excessive C/4-rate charging; under such conditions a strict timeout limit for fast-charging, of perhaps 4-4.5 hours, may be required in order to restrict degradation of battery performance arising from excessive overcharging.

More precise end-of-charge algorithms based on analysis during charging of E.S.C. trends and gradients would, apart from involving more complex software algorithms, possibly necessitate the use of a part-discharge of perhaps 5-10%, though not beyond a safe voltage cutoff, of all non-exhausted batteries placed in the charger (which is similar to a principle involved in the Redif(fusi)on BC21 charger).

Returning to the operation of the J.P.B./U.C.S. charger, many of the details of the charger and its operating characteristics are explained in the "J.P.B./U.C.S. Charger Provisional User Manual" which is listed in Appendix 7. Additional notes on certain aspects of charger operation are provided as follows:-

- The function of the BAD-BATTERY l.e.d. and the "IDENTIFY" function of the RESET/IDENTIFY button are explainable as follows. The charger is able to detect certain faults in batteries by means of appropriate d.c. and a.c. measurement strategies. The most simple test that can be done, which can detect open-circuit batteries and shorted or otherwise unchargeable cells within batteries, is that of on-load terminal voltage. This test is possible since the charger has the capability to discharge individual batteries at the C/5 rate. An appropriate time to apply this test might be at the transition point between C/4- and C/10- rate charges; this was done in practice. It is conceivable that certain characteristics of measured Effective-Series-Capacitance curves may be related to battery operational quality and that battery faults and imminent failures may be thus identifiable (the Author did not collect enough information to attempt to use a.c. methods for identifying any but the most drastic battery faults). When the J.P.B./U.C.S. charger determines that an identifiable fault of important magnitude is present in one or more batteries currently present in its sockets then the BAD-BATTERY l.e.d. is lit flashing-red. It should be noted that the Battery-Status l.e.d. associated with any battery determined to be "Bad" will never be allowed to turn green whilst the battery remains in its holder.

- The J.P.B./U.C.S. charger has an ability to tolerate mains power failures of several to many hours (by means of double-layer-capacitor-backed R.A.M.). If a mains failure occurs whilst batteries are being charged (in either the "Intelligent-Charge" or the "C/10-Charge" mode)

then on resumption of power within an acceptable period the charging process will continue from the point at which it was halted. The charger is also immune to partial mains voltage losses ("brownouts") and to brief mains abnormalities (unlike the Redif(fusi)on BC21 prototype which was easily "crashed" by momentary power losses) and should prove to be be dependable in service.

- The transition of an individual Battery-Status l.e.d. from flashing-red to continuous-green does not necessarily need to be made simultaneous with the C/4-rate to C/10-rate charge transition (Note that simultaneous transitions are involved in the corresponding procedure of the Redif(fusi)on BC21 charger). The l.e.d. status transition can be delayed for up to a few hours in order to provide a guaranteed minimum topping-up period before the battery is made recognisable to the user as being "Charged". However, in a realistic shift system of battery usage it is quite possible that batteries may occasionally be placed on charge late or that batteries may be required during mid-shift in which case an early l.e.d. red-to-green transition would be valuable in helping a user to identify usable (perhaps in practice, at least 80% charged) batteries.

CHAPTER 13

The Hardware and Software (Final Versions) for the J.P.B./U.C.S. PFX Battery Charger

The (Novel) Phase-Sensitive Detector

The J.P.B./U.C.S. charger utilises the same theoretical principle for measurement of Effective-Series-Capacitance as the research cell/battery test rig, namely, a sinewave current excitation and a phase-sensitive analysis of resulting a.c. perturbation voltages. In order to reduce the cost and complexity of the d.c.-voltage-nulling detector circuitry (and partly as an academic exercise - the circuit raised a few eyebrows!) an analogue system was used incorporating a form of pure a.c. coupling.

Figs. 101(a,b) show the circuitry involved in the J.P.B./U.C.S. charger detector unit; with reference to these diagrams the following notes are given:-

- The "072" is a dual op-amp equivalent to Texas TL072CP, half of which acts as a preamplifier (first in chain) and the second half of which (second in chain) acts as a low-gain buffer.
- Whilst the detector is in a quiescent state (not operating) the analogue switches *"A"* and *"B"* are closed such that the "4.7μF" and "1μF" coupling capacitors are forced to attain d.c. equilibrium states and so that both 072 op-amp outputs settle to near-ground voltage, subject to errors arising from input offsets. Any battery d.c. terminal voltage present at the input of the 4.7μF capacitor is effectively nulled out from the point of view of the preamplifier op-amp and the input offset voltage of the preamplifier op-amp is effectively nulled out by the 1μF capacitor

from the point of view of the buffer op-amp.

- It should be noted that accurate settling of the d.c. null requires that the detector be held in a quiescent state for many input-stage time-constant periods.

- Immediately before the detector is put into operation the analogue switches *"A"* and *"B"* are opened. This results in the "4.7μF" and "1μF" capacitors providing a form of a.c. coupling which is near-perfect since the time constant for capacitor voltage drift is very long compared even to 1/(2Hz) = $^1/_2$ second. Stability of the a.c. coupling is dependent on such factors as op-amp input bias currents, p.c.b. surface leakages, and on internal leakages of analogue switches, protection diodes and the capacitors themselves. The 072 op-amp has F.E.T. inputs with extremely low bias currents and, in practice, the analogue switches may present the worst leakage sources (if this design were ever to go into production the analogue switches might need to be individually selected to weed out particularly leaky devices).

- The half-072 preamplifier is configured for a gain of about 30 and provides the primary amplification for detected response voltages.

- The half-072 buffer serves to provide an extra gain of 2 and in conjunction with its input capacitor serves to null out the output offset voltage (up to about 90mV) of the preamplifier op-amp. The output of the buffer op-amp is fed to the input of analogue switch *"C"* and also to an inverter stage.

- The OP-07 is configured to provide an inverted version of the signal present at the output of the buffer op-amp. The OP-07 was chosen for this purpose since the inversion stage must have a low output offset (it can be shown fairly easily that an output offset in this stage will lead to a constant additive error term in phase-sensitive detection results - the gain accuracy of the stage, though, is not at all critical). The output of

the inverter stage is fed to analogue switch *"D"*.

- Analogue switches *"C"* and *"D"* are switched in mutual antiphase and in quadrature with the excitation signal used in any measurement. These analogue switches perform the timed signal switching required for phase-sensitive detection (by square-wave multiplication) and have commoned outputs which are fed to an A-to-D converter.

- The 7109 A-to-D converter (Intersil ICL7109CPL or equivalent) is a fairly low-cost 12-bit integrating converter incorporating auto-zeroing of internal offset voltages. The converter is designed primarily for the measurement of d.c. voltages but is used in this instance for integrating a complicated a.c. waveform present at its input. The 12-bit resolution of the converter enables signals to be integrated to a good accuracy over a fairly large dynamic range. The converter is operated with a clock frequency considerably lower than normal.

- Selection of the various passive components associated with the converter is not as simple a matter as for cases where d.c. signals are integrated. Care must be taken to avoid overloading both the input stage of the converter and the integrator stage since overloads, even if only transient, may generate ambiguous or freak results. Conversely, care must be taken to keep all signals involved as large as possible to minimise errors resulting from converter accuracy limitations and general leakage currents.

- The detector incorporates a degree of input protection against abnormal inputs.

- The detector involved the most critical design of all of the circuits in the J.P.B./U.C.S. charger and was constructed in a very compact and neat form on a single-sided printed circuit board. The p.c.b. layout incorporated a partial ground plane to limit noise pickup and included grounded guard tracks around all high impedance conductors for protection

from general surface leakage currents.

- In practice, some detector circuit parameters, such as the preamplifier gain, were optimised through experimental measurements on a sample of batteries.

- Note that the value of the 7109 integrator capacitor used in the prototype (and shown as C_{AZ} in Fig. 101b) is not optimised. This capacitor ought to have a value of 1.25μF for best system accuracy.

The (Simplified) Sine-Generator

The J.P.B./U.C.S. charger contains a dedicated-hardware, current-mode-output sinewave generator bearing many similarities to the "Sinegenerator" of the research cell/battery test rig but of a much simpler design.

Figs. 102(a,b) show the circuitry involved in the J.P.B./U.C.S. charger sine-generator; with reference to these diagrams the following notes are given:-

- The sine-generator has three programmable frequencies, namely 2Hz, 8Hz and 32Hz.

- The sine-generator has a fixed output current amplitude, namely +/-50mA peak, which is obtained via an op-amp driving a complementary transistor pair.

- A 512-byte-by-8-bit bipolar R.O.M. is used for storing sinewave data, the logic addresses for which are provided from a resettable counter circuit.

- A very-low-cost DAC-08 8-bit DAC is utilised in a circuit very similar (with the elimination of a feedback-buffer op-amp) to the research cell/battery test rig "Charge-Discharge" module current generator circuit.

- The sine-generator incorporates a degree of output protection against

abnormal loads.

- It should be noted that the polarity of the sinewave generated by the sine-generator may be significant in practice (in relation to considerations of battery terminal-voltage drifting - discussed elsewhere). The J.P.B./U.C.S. charger was configured via EPROM programming to generate (positive-then-negative)-going sinewave bursts.

The D.c.-Sensing Voltage Comparators

Unlike the system used in the research cell/battery test rig, measurements of battery d.c. terminal voltage are performed by a circuit independent of the voltage-nulling detector. The d.c.-sensing circuit is as simple as the requirements of the prototype J.P.B./U.C.S. charger allow and is based upon a pair of comparators rather than on an A-to-D converter.

Fig. 103 shows the circuitry of the voltage comparators involved in the J.P.B./U.C.S. charger; with reference to this diagram the following notes are given:-

- Two LM393 comparators are used to test battery d.c. voltage, each of which is given a small degree of hysteresis for 'clean' operation.
- One comparator has a threshold set at about 3V and is used for determining the presence or absence of a battery in a selected holder.
- The second comparator has a threshold set at about 9.7V and is used during a battery on-load terminal-voltage test for gauging battery serviceability.
- The voltage comparators have substantial input protection against abnormal inputs.

The 10-Channel Charge/Discharge Board

The J.P.B./U.C.S. charger incorporates a charge-discharge board containing 10 independently-programmable charge-discharge current generators which share power rails and a voltage reference. For reasons of cost the current generator circuit, unlike the analogous circuit in a research test rig "Charge-Discharge" module, does not involve an integrated circuit DAC.

Fig. 104 shows the circuitry involved in the J.P.B./U.C.S. charger charge-discharge board; with reference to this diagram the following notes are given:-

- Each current generator has three TTL-compatible control inputs and is split into a charging section and a discharging section.
- As well as a zero-current quiescent state, three values of charge current and one value of discharge current can be usefully generated, namely 60mA, 240mA, 300mA and -120mA. These correspond, respectively, to charge rates for 600mAh batteries of C/10, C/2.5, C/2 and a discharge rate of C/5.
- The 10 current generators share a common voltage reference for their discharge sections. An extra input is provided to the charge-discharge board which enables the voltage reference to be disabled. This feature is of great value for preventing discharge of batteries through the discharge current generators when the charger is not properly powered up.
- Each of the 10 current generators has its output permanently connected to a charger battery holder, unlike the research cell/battery test rig where connection was made via a (reed) relay.
- The current generators incorporate a degree of protection against abnormal loads and contain various important bypass capacitors for purposes of stability and noise reduction.

- Note that 74LS05 open-collector inverter gates are specified for outputs of no more than about 5V and that the devices used in the prototype were selected for breakdown voltage (at the collector) of greater than 25V). In a production version of this charger, discrete transistors or transistor arrays would be preferred for the interface between control logic and the current generators.

Measurement Multiplexing and Grounding Schemes, the Relay Board and Battery Holders

Grounding problems involved within the J.P.B./U.C.S. charger are significant but not as severe as in the research cell/battery test rig. Instead of adopting a scheme in which the excitation unit and the detector are mutually floating and floating with respect to the charge-discharge current generators (as in the research cell/battery test rig), the excitation unit is non-floating and the detector is made semi-floating via a judicious arrangement of ground conductors. A full four-terminal method of measurement is not required. However, a problem exists in that 10 batteries must be multiplexed to the sine-generator and detector; for this purpose the J.P.B./U.C.S. charger uses relays for general robustness and simplicity of control. In order to avoid inherently variable relay contact resistances from contributing to measured battery impedance the (single-ended as opposed to differential-pair) excitation and response signal leads must be connected via separate relay poles to any battery under test.

Fig. 105 shows the circuitry involved in the J.P.B./U.C.S. charger relay-board and the battery holder section; with reference to this diagram the following notes are given:-

- The relay board contains 11 2-pole miniature (not reed) relays. One

relay is allocated to each of 10 battery holders and an additional relay is provided connected to an 11 Volt voltage reference for possible charger self-test purposes. The relay board is mounted on the charger front panel which also contains the battery holders.

- Each relay has one pole allocated to the excitation signal and one to the response signal. All relays have comparable charger-side (as opposed to battery-side) output poles commoned and fed to the sine-generator and detector circuits respectively.
- Each relay has its two battery-side poles (as opposed to charger-side) commoned and connected via the centre conductor of a screened cable to the positive terminal of one battery holder. The outer conductor of the screened cable forms the ground return for that battery holder (Note that separate excitation and response conductors might have been used to remove lead resistance and inductance but the grounds are necessarily commoned, lead resistance is of no consequence for Imaginary-component impedance measurements and inductance was not thought to pose a major problem provided that the effective lead lengths for the 10 batteries were kept reasonably similar and as small as possible).
- The inner conductor of a relay-to-battery cable (which carries excitation and response signals) also carries the charge-discharge current for the battery. The charge-discharge current generator associated with a battery is coupled to the conductor at the battery-side poles of the associated relay such that charge-discharge currents do not flow through the relay.
- Note that during operation of the charger d.c. measurements are generally required to be much more frequent than a.c. measurements. It is possible that future versions of the charger might use solid-state devices as multiplexer switches for d.c. measurements in order to reduce relay wear or that high-quality solid-state devices might be used to replace the

relays entirely.

The Charger Power Supply

The J.P.B./U.C.S. charger operates from a.c. mains power and includes a linear-mode power supply to provide three low-voltage rails. The power supply is based on internally protected monolithic regulator i.c.'s and is fairly conventional except for the use of a special voltage doubler for providing the low-current negative rail; this makes more efficient use of a the mains transformer than a split-supply configuration based on a rectifier bridge and a centre-tapped transformer. Due to the incorporation of a controlled powerdown mechanism into the charger the 5-Volt supply circuitry is given as high a voltage overhead as possible and a large primary reservoir capacitor is provided.

Fig. 106 shows the circuitry involved in the J.P.B./U.C.S. charger power supply.

The Powerup/Powerdown Sensor

The J.P.B./U.C.S. charger incorporates a powerful powerup/powerdown mechanism based on a hardware powerup/powerdown sensor, double-layer-capacitor-backed R.A.M. and appropriate software. The hardware sensor is based around two low-power (Intersil) ICL8211 comparators which are capable of functioning at supply voltages of as low as 1.8 Volts.

Fig. 107 shows the circuitry involved in the J.P.B./U.C.S. charger powerup/powerdown sensor; with reference to this diagram the following notes are given:-

- One comparator has a switching threshold set at 7.5V without explicit

hysteresis and is involved in generating the Not-Reset (NRST) signal for the 6303 microprocessor.

- The second comparator is given hysteresis with thresholds of 12.0V and 14.9V. Via additional logic gating this comparator generates the Non-Maskable-Interrupt (NMI) signal for the 6303 microprocessor.
- Note that the values of the input divider and feedback resistors for the comparators (as given in Fig. 107) are somewhat (perhaps 3 times) larger than might be optimum.

The Control Logic

The control logic for the J.P.B./U.C.S. charger is based around a (Hitachi) 6303RP microprocessor and utilises HCMOS logic for low power consumption and for ease of interface to non-logic devices. In the prototype charger certain aspects of the logic, including the processor bus buffering and the battery-status l.e.d. drivers, are technically inadequate (though perform well in the one-off prototype).

Fig. 108 shows the general architecture, in block form, of the control logic within the J.P.B./U.C.S. Charger and its connections to other component circuits. Figs. 109(a,b,c) show, in schematic form, component sections of the control logic circuitry. With reference to these diagrams a few notes are given concerning the less conventional aspects of the control circuit design, as follows:-

- The Red-User-Button switch is connected to logic via a simple deglitcher based on an R-C integrator followed by a Schmitt-input buffer.
- The Yellow-User-Button switch is connected to logic via a simple one-shot and a deglitcher.
- The green/flashing-red battery-status indicator l.e.d.'s are connected internally in a common-cathode configuration and, hence, must be driven by

switched current-sourcing devices. For purposes of the prototype charger the l.e.d.'s had to be driven from available HCMOS latch outputs. Each green l.e.d. was driven via a 130Ω resistor from a single output. Each red l.e.d. (having internal current limiting) was driven from paralleled outputs though it was considered wise to insert a 220Ω resistor in series with one output of each latch pair to eliminate the possibility of damage by freak programming of latches within a pair into opposite states.

- Note that the output drive capabilities of the l.e.d. driver arrangements used were marginal and were particularly so for the flashing-red l.e.d.'s which may not function at terminal voltages of less than 4.75 Volts. A more satisfactory arrangement would involve the use of paralleled HCMOS buffers as drivers, PNP-transistor drivers or AC-series CMOS drivers with care being taken to ensure that the relevant logic supply voltage is at least 5.2 Volts.

- The 6264ALP (very low standby current) R.A.M. is deselected under charger powerdown conditions and is given a voltage supply backup. The backup system simply comprises a double-layer-capacitor (0.1 Farad or greater) in parallel with a tantalum capacitor and fed via a Schottky diode. In order that coupling problems do not result via the R.A.M. having an effective lower supply voltage than other CMOS devices on the control board, the diode is a 1 Ampere device that has a voltage drop of less than about 300mV under normal R.A.M. operating conditions. Such a large diode, however, may contribute to overall leakage current from the backup capacitor under standby conditions.

- Note that the double-layer capacitor perhaps ought to be given a series resistor to limit its charging current and that the R.A.M. supply diode leakage problem could be solved if a 5.75V voltage regulator were used supplying the R.A.M. via a conventional diode and other circuits via a separate diode.

Control Software (Version 1.1)

The software for the J.P.B./U.C.S. charger was written in machine code for compactness and versatility. Sheet 2 contains the 6303 microprocessor machine code listing "Version 1.1" which was the final version installed by the Author into the charger EPROM. As the listing is highly commented and some information is given in the "J.P.B./U.C.S. Charger Provisional User Manual" (contained in Appendix 7), only a few comments are given here, as follows:-

- The software treats all batteries (of a possible ten) individually and keeps a separate record of the state of progress of charging of each battery present in the charger.
- In charger Intelligent-Charge mode (the normal operating mode) the charging process involves a "Fast-Charge" phase, utilising a C/2.5 charge rate with intelligent termination via the "Charge/End-of-Charge" algorithm, followed by a time-limited "Top-Up" phase, utilising a C/10 charge rate, followed by an indefinite C/40-(average-)rate "Maintenance" charge phase (actually a C/10 current supplied in a 15 second pulse once per minute). It is convenient to define the following nominal states through which batteries pass, in the following order, during charge:-
  (1) "On-Fast-Charge" (during Fast-Charge).
  (2) "Fast-Charged" (during the first part of Top-Up in which the relevant Battery-Status l.e.d. remains set to flashing-red).
  (3) "Nominally-Charged" (during the second part of Top-Up in which the relevant Battery-Status l.e.d. has been set to continuous-green).
  (4) "Topped-Up" (after completion of Top-Up).
- In Intelligent-Charge mode the charger operates with an effective 5-minute cycle time in that it does many major charging-related operations, including applications of charging algorithms, in a cyclic manner dealing

with two adjacent battery holders (out of ten) at a time at one-minute intervals.

- The software includes an interrupt-driven clock which is responsible for timings of major system operations.

- In order to cope with inherent variability of the duration of measurements (caused by variability of the 7109 A.D.C. conversion time and the possibility of measurement retries) the main measurement operations are requested indirectly via the setting of system flags by the system-clock mechanism.

- Due to the highly asynchronous nature of the interface of the machine with the real-world, many system functions (other than main measurement operations) are controlled via system flags.

- To maximise the lifetime of the relays which multiplex batteries to the charger measurement circuitry the d.c. test sweeps of battery holders which are necessary for determining the presence or absence of batteries are done as infrequently as possible. In practice, automatic d.c. test sweeps are done once per minute; this results in the charger being fairly slow on average to respond via automatic means to insertion or extraction of batteries. Consequently, a mechanism is provided for manual requesting of a d.c. test sweep (and associated internal operations) via the charger's "Update" button. Manual "Update" operations are invoked via a route employing a system flag and are always performed as promptly as is possible without harming automatic operations that may be in progress within the charger.

- A.c. measurements are done only during the Fast-Charge phase of charging.

- Prior to commencement of an a.c. measurement or measurements on any given battery the charge current for that battery is suspended for a precisely defined period during which time the battery terminal-voltage

settles partially.

- All a.c. measurement results are checked for validity of range; if any result seems invalid then a measurement retry may be requested.
- Every battery is given an on-load terminal voltage test during the "Top-Up" charge phase; each battery must pass the test in order to become registered as "Nominally-Charged" and to have its associated status l.e.d lit continuous-green.
- Upon power failure the charger attempts to save, to battery-backed R.A.M., selected data on charger operational status and on the charging status of any batteries present in holders. On normal charger powerup the software waits until the 6303 microprocessor NIRQ input becomes high (by testing the line via a port input) and then attempts to restore the charger into the state existing prior to the previous powerdown.
- Methods are provided during powerup for setting the charger manually into specific operating modes.
- Note that more charger operating modes, including battery test/evaluation modes, could be included in possible future versions of the charger.
- Note that control software Version 1.1 includes code which causes data obtained from a.c. and d.c. measurements to be transmitted, in a proprietary format, via the charger's serial output link.

CHAPTER 14

Experiments with the J.P.B./U.C.S. Charger and a Working Charge/End-of-Charge Algorithm

Some Experiments with the J.P.B./U.C.S. Charger

During evaluation of the J.P.B./U.C.S. charger some experiments were done in which measurements taken on a set of batteries by the charger's hardware were transferred (via the charger's integral RS-232 serial-data output) to a B.B.C. microcomputer and stored on floppy-disk for analysis. The results were later plotted in graph form and were studied in a similar manner to results obtained from the research cell/battery test rig. Profiles of battery Effective-Series-Capacitance measured at 2Hz were, as expected, of a similar form to results obtained previously with the research test rig. Some results can be seen in Graphs 101(a,b,c,d). Results from several tests, mainly using a sample of 8 new PYE P.F.X. batteries, were used to optimise program timings and to optimise charger calibration parameters such as the preamplifier gain and the values of passive components associated with the 7109 A.D.C.. Tests were also done to optimise parameters for a charge/end-of-charge algorithm (Discussed later).

Important tests were done to determine the requirements associated with suspension of charging currents prior to the taking of a.c. measurements. It should be noted that no method was ever used by the Author to compensate the charger's a.c. measurement results for errors resulting from battery terminal-voltage drifting during measurements. The Author decided that the 'error' factors involved were best considered as integral parts of measurement results and that program timings should be

chosen such as to either make the 'error' factors small yet perhaps variable or to make them constant and repeatable yet perhaps large. It should also be noted that a fixed polarity of sinewave excitation (positive-then-negative) was used for excitation purposes and that the polarity of the waveform, being a single-cycle burst for a 2Hz measurement, probably plays a significant role in the interaction of effects due to sinewave excitation and battery terminal-voltage drift. The Author did no experiments in which the sinewave polarity was reversed. It is possible that reversal of the excitation sinewave could improve measurement results for purposes of end-of-charge detection though it should be noted that this might require rest-period timings to be changed.

It was found that unless a battery had its charge current suspended for more than about 20 seconds prior to a 2Hz E.S.C. measurement then the zero-current rest period was required to be timed accurately in order to achieve acceptably repeatable results. After a 20 second rest period the d.c. terminal voltage of a battery generally appeared to have settled sufficiently such that residual settling had fairly small effects; hence, only small errors in repeatability would result from a loosely specified rest time of, for example, a variable 25-35 seconds. The Author's tests, though, were not thorough and it is possible that at some states-of-charge batteries may require longer rest periods in order to maintain measurement repeatability. An early version of the J.P.B./U.C.S. charger software utilised a long but loosely-specified pre-measurement rest period because this mode of operation provided certain programming advantages. However, a version of the program involving precise timings was eventually adopted for peace of mind, although this involved a complete rethink on program operation sequencing. It was known that a rest time of greater than about 2-3 seconds was required to allow sufficient battery terminal voltage settling such that d.c. voltage nulling would be

effective and so that the waveform processed by the detector would not be so asymmetrical as to cause overloads. It was found that rest times of a fraction of a second often generated results of negative sign; probably in most such cases the detector amplifier/p.s.d.-switching stages were being overloaded.

Rest periods in the range 5-10 seconds were investigated more thoroughly, with 10 seconds being considered the longest value practical to allow convenient charger operation sequencing. The Author decided that a 10-second period probably improved measurement results for purposes of end-of-charge detection since it appeared that use of the shorter rest periods caused apparent battery E.S.C. during the early part of charging to rise uncomfortably close to the value at the overcharge plateau. However, the experiments involved did not produce unambiguous results since it appeared that battery E.S.C. during the early part of charging (corresponding generally to phase *(ii)* of Graph 101(a)) was increasing gradually with successive charge-discharge cycles (which is a potentially disturbing discovery and will be mentioned later).

Some simple experiments were done in which batteries of abnormally high internal impedance were simulated by placing resistors in series with good batteries during measurements. In general, this situation causes apparent E.S.C. values to become abnormally low due to saturation or part-saturation of the detector amplifiers (which presents a waveform approximating to an in-phase square-wave to the phase-sensitive detector). The response of the measurement unit to abnormal test devices (such as faulty batteries) is made complicated by the fact that the detector has two stages, namely the amplifier and the integrator, which are susceptible to saturation independently and under different conditions. Furthermore, because a.c. waveforms are involved then cases of saturation may be transient. Except for the case of overflow at the end of integration (i.e.

"overrange"), there is no means by which incidences of integrator saturation may be explicitly signalled. One very pleasing observation from these tests, though, was that provided that the magnitude of the response voltage was not caused to become so high as to lead to detector overloads then the introduction of low resistances in series with battery terminals did not significantly perturb measurement results (which are dependent according to simple theory only on battery Imaginary-part impedance). In experiments, a series resistance between battery and holder of as great as 0.5Ω was tolerated. This value is somewhat larger than contact resistances normally expected for a battery/battery-holder link which confirms that conventional two-terminal battery contacts ought to be adequate for the charger.

A Working Charge/End-of-Charge Algorithm for the Charger "Fast-Charge" Phase of Charging

For simplicity, control software Version 1.1 utilises measurements at frequency 2Hz only and involves no battery discharge phase. Graph 101(a) is used as an example 2Hz E.S.C. graph for showing features relevant to discussions of E.S.C. profiles and charge/end-of-charge algorithms. With reference to Graph 101(a) the charge/end-of-charge algorithm is nominally as follows:-

Charging is terminated ...

IF (a) ... for four consecutive measurements the battery 2Hz E.S.Capacitance exceeds a preset threshold (shown as "Threshold 0" on Graph 101(a)) ... AND ... the difference between every pair of adjacent measurements exceeds a preset value (corresponding to the gradient of the

profile being greater than a limiting value - shown as "Slope 0" on graph 101(a))

OR IF (b) ... for four consecutive measurements the battery 2Hz E.S.Capacitance exceeds a given limit (shown as "Threshold 1" on Graph 101(a))

OR IF (c) ... the duration of the Fast-Charge phase has exceeded 4 hours (shown as "4hr" on Graph 101(a)).

In practice, however, the charge/end-of-charge algorithm is not as simple as described above since allowances must be made for possible measurement inaccuracies and for failures induced by effects such as undesirable interactions within the charger (which are known to exist), electrical noise, and temporary instabilities within batteries. The complete algorithm implementation, which is readable from the software listing in Sheet 2, utilises two counters which are incremented or decremented in a manner dependent upon tests of measurement results. The charge-algorithm counters are inspected regularly and Fast-Charge is terminated if either counter reaches a predefined threshold.

The limiting thresholds, gradient and time involved in the charge/end-of-charge algorithm for the Fast-Charge phase were determined largely from the Author's previous knowledge and experience of batteries but were finely adjusted via experimentation on 8 new PYE P.F.X. batteries. These batteries ought not to be considered as forming a particularly representative sample since they all had similar dates of manufacture. After being subjected to conditioning cycles the batteries, named "P6PB5", "P6PB6", "P6PB7","P6PB9", "P6PB10", "P6PB11", "P6PB12", "P6PB13", had their true capacities measured using the research

cell/battery test rig by means of a standard C/10-rate charge followed by a C/5 discharge to 1 Volt-per-cell cutoff. This procedure was called RUN1000 and its results are shown in Fig 111(a). The capacities of the batteries were found to vary over a range of about 10%.

Some variations existed between the 8 batteries in (the rather loosely defined) 'absolute' magnitudes of 2Hz E.S.C.. These variations appeared to be unrelated in any simple manner to variations in battery true capacity. For example, for the 7 batteries tested other than "P6PB5" (which had anomalous behaviour - see later) the correlation coefficient for the phase-*(vi)* plateau height observed for one test run versus battery true capacity was -0.178 whilst the correlation coefficient for the phase-*(ii)* peak height averaged over three test runs versus battery true capacity was -0.363; the signs of the values are contrary to what might be intuitively expected.

As well as variations in absolute value of 2Hz E.S.C., some significant variations existed between batteries in the shapes of 2Hz E.S.C.-versus-charging curves. With reference to Graph 101(a), phase *(ii)* did not necessarily contain a peak; the gradient in phase *(iii)* was variable and could be negative or positive; phase *(iv)* sometimes contained a distinct trough; and the range of gradients observed for phase *(v)* was extremely variable. During successive tests on batteries, it appeared that all batteries, except "P6PB5" (see later) were tending to develop a distinct trough in phase *(iv)* and a peak in phase *(ii)*. The Author expected that with continued cycling the E.S.C.-versus-charging curves for each cell would eventually stabilise but had cause to be concerned about the behaviour of the peak since its presence is detrimental to the reliability of end-of-charge algorithms.

Although E.S.C. gradients in phase *(v)* for single-cells on charge vary between individual cells, the fact that gradients observed in phase

(v) for multi-cell batteries were extremely variable may be due largely to the fact that each battery is composed of 8 cells of differing capacities which thus reach overcharge at differing times (though it is reasonable to assume that cells within each battery have been matched for charge-holding capacity to some degree - perhaps to within a 5% range). It is fairly obvious that if all individual cells within a battery enter phase *(v)* simultaneously then the phase *(v)* for the battery as a whole is likely to be well defined and to have a relatively high average gradient. However, if cells within a battery individually enter phase *(v)* at significantly differing times then phase *(v)* for the whole battery will be less clearly defined and will have a relatively low mean gradient.

In setting each threshold, a balance had to be achieved between setting the threshold low enough so that it would be exceeded sufficiently early by all batteries in phase *(v)* and between setting it high enough so that it would be unlikely to be exceeded by any peak occurring in phase *(ii)*. Fortunately, because of the manner in which the end-of-charge algorithm part (a) monitors gradient and because of the manner in which parts (a) and (b) utilise counters, certain limited excursions of E.S.C. above either threshold in phases *(i)*, *(ii)* and *(iii)* are tolerated.

In setting the limiting gradient value, a balance had to be achieved between ensuring that the value was sufficiently low that the end-of-charge algorithm part (a) would be unlikely to fail to operate via the required gradient not being maintained for the required number of successive measurements, and between ensuring that the value was sufficiently high so as to make algorithm part (a) highly immune to early excursions of E.S.C. above Threshold 0, such as might be caused by peaking in phase *(ii)*.

Two working tests were done of the Fast-Charge phase of the J.P.B./U.C.S. charger incorporating the charge/end-of-charge algorithm as

defined by the machine-code listing of Sheet 2 (except that the Fast-Charge time limit during these tests was 4.25 hours instead of 4 hours - this is significant for one result). The tests were done on the set of 8 PYE P.F.X. batteries (described earlier) and the results are shown in Figs. 111(b,c). It should be noted that charging of every battery in these tests was terminated completely at the end of the Fast-Charge phase so that batteries were not subjected to "Top-Up" or "Maintenance" charges. Charged capacities were determined via C/5-rate discharges to 1 Volt-per-cell cutoff using the research cell/battery test rig. In every case, it appeared that the algorithm part (a) was responsible for charge termination and the effectiveness of the Fast-Charge phase (relative to battery true capacity) was at least 90%. These results, even if a pessimistic view is taken, seem to indicate that the charging-control method ought to produce good results in the long term.

A Predictor of Battery Failure?

Some of the new PYE P.F.X. batteries in the sample of 8 tested had suffered inadvertent overdischarge prior to use with the J.P.B./U.C.S. charger. One of these batteries, namely "P6PB5", was known to have vented internally during an overdischarge. The battery can therefore be considered as having been damaged to a degree although no evidence of this was given by measurements of cell charge-holding capacity. It is probable that only one cell within the battery was damaged, though it should be noted that the damage ought not to be 'fatal' since SAFT cells normally possess self-resealing safety vents. It was discovered in subsequent charges that in the 2Hz E.S.C.-versus-charging curve the peak in phase *(ii)* (see Graph 101(a)) was never present and that E.S.C. was lower than normal in phase *(iii)*. Furthermore, a spike of extremely variable height

was occurring during phase *(i)*. In one charging session (Shown in Graph 103) the spike was barely visible but in a later session the spike was nearly at the height of the final capacitance plateau (Large spikes for battery P6PB5 are visible in Graphs 102(a) and 102(e)). The Author cannot say with certainty that the venting of the battery and the anomalous E.S.C.-versus-charging response are directly connected; even if a connection exists then the explanation of the response observed is not easily explainable. The observation may amount to one of a useful predictor of a form of early battery failure, although it should be noted that the fault was 'artificially' induced in a fairly severe manner. In practice, batteries need not receive significant overdischarge from the J.P.B./U.C.S. charger even if the charging method is modified so as to include a discharge phase. However, partial overdischarges in the form of cell-reversal are always liable to occur during usage of batteries in powered equipment; these may result in cumulative damage.

CHAPTER 15

Late Developments and Discoveries and Overall Conclusions

0.5 Hertz Measurements with Motorola Batteries

Near the end of the active period of research the Author performed a series of charge-discharge runs with Motorola NTN5048A 8-cell 900mAh batteries using measurements at frequencies including 1Hz and 0.5Hz in order to determine whether frequencies below 2Hz produced a more pronounced E.S.C.-versus-charging response. The results for 3 batteries for RUN806 are shown in Graphs 13(a,b,c). RUN806 utilised the same charge-discharge regime as RUN601 (see Chapter 10) and used measurements at 16, 8, 4, 2, 1 and 0.5Hz. A very important feature of RUN806 was that for each battery involved the charge-discharge current was suspended a precisely defined time, namely 10 seconds, before the measurement sequence was applied to it.

The curves of 0.5Hz E.S.C during charge obtained from RUN806 were found to be somewhat 'startling' since they appeared to provide an end-of-charge indicator far superior to any that had been found for cells and batteries of SAFT manufacture. During charge from the fully-discharged state the E.S.C. values observed at frequencies in the range 0.5-2Hz increased to a peak at about the 0.4C-quantity charge point. On continued charge E.S.C. values at these frequencies decreased fairly linearly until a point within about 6% of the nominal C-quantity charge point; after this point E.S.C. either remained almost constant or remained near-constant for a 0.2C-quantity further charge and then began to increase. The interesting points to note are that at frequency 0.5Hz the transition at the C-

quantity charge point was always marked by a sharp gradient change; that the position of the transition point always seemed well-defined; and that the ratio of the height of the early-charge peak to the final low plateau (or approximate plateau) was always at least 3.5:1. The Author wondered if the C-quantity charge point transitions were due to the action of a series polymer thermistor (a self-heating +ve temperature-coefficient device) which is included in Motorola NTN5048A battery packs for protection of batteries against external shorts: perhaps this thermistor was responding to the rise in internal temperature of batteries caused by overcharge. However, the thermistor was thought to operate at temperatures higher than those likely to be encountered during C/5-rate charging. Furthermore, the thermistor was expected to influence only E.S.Con., rather than E.S.C., directly and large interactions were not expected between E.S.Con. and E.S.C.. Plots of E.S.Con. at frequencies in the range 0.5-16Hz showed that E.S.Con. variations were slight and were generally devoid of 'interesting' features; this indicated that the polymer thermistors within batteries were not playing any significant role in modifying E.S.C. response.

A test run similar to RUN806 was done in which charge-discharge currents were maintained throughout the whole of the run inclusive of measurement excitation periods. The resulting 0.5Hz E.S.C. curves obtained showed a transition feature at about the C-quantity charge point which was consistent and appeared to be very useful for purposes of end-of-charge indication. For some batteries, though, invalid measurement results were produced at and beyond the C-quantity charge point; the Author suspects that the spoiling of results may partly be due to noise in charge-discharge module current generators with possible enhancement via inductive elements within the batteries. The run also showed that +ve bias did not improve the usefulness of measurements at frequencies of 2Hz and higher for purposes of end-of-charge indication.

Possible Trials and Evaluation of the J.P.B./U.C.S. Charger

In early 1990 the prototype "J.P.B./U.C.S." Charger Mk. I. for PYE P.F.X. 600mAh batteries was handed over to the Home Office Directorate of Communications together with information, a selection of pre-tested P.F.X. batteries and a program for outputting data to a B.B.C. microcomputer. The Author hoped that the charger might be put on field trials for perhaps a year or more at a selected location so that its performance and "user-friendliness" could be judged, at least, subjectively. Home Office representatives considered also that the charger might be used for purposes of battery inspection and evaluation in parallel with techniques and schedules already in use by the Directorate.

A Possible J.P.B./U.C.S. Charger Mk. II

Possible future developments ensuing from the Author's research include design and construction of a Mk. II. charger. The Author considers that certain aspects of the Mk. I. charger can be improved upon in order to increase accuracy of measurements and to increase the versatility of the charger whilst reducing the overall component count and component cost. A Mk. II. charger might utilise the modifications suggested as follows:-

(a) The dedicated logic of the sine-generator would be eliminated and the 7109 A.D.C. and sine-generator DAC would be interfaced directly to the system microprocessor (6303 or otherwise). This would enable the sine-generator control and timing functions to be provided in a flexible manner by software routines. Furthermore, the sinewave sample words (8-bit) could then be stored in the same (E)PROM as the charger control program. It

should be noted that this scheme would require IRQ1 interrupts to be disabled during sinewave generation which necessitates that the Yellow-User-Button be coupled to the microprocessor by a different means, such as to a regularly polled port bit via a logic bistable.

(b) The battery d.c. voltage nulling method would be a hybrid of that used in the research test rig and the Mk. I. J.P.B./U.C.S. charger. The battery response signal would be fed into one input of a differential input amplifier of gain approximately 20. The second input of the differential amplifier would be connected to the output of a low-cost, low-drift DAC which would provide a primary voltage-nulling function. The output of the differential amplifier would be fed to a polarity-detecting comparator. By means of appropriate software the differential-amplifier/DAC/comparator arrangement could be operated as an 8-bit resolution A-to-D converter for purposes of measuring battery d.c. terminal voltage and simultaneously nulling out the bulk of battery d.c. in preparation for a.c. measurements. An advantage of this arrangement is that the need for d.c.-sensing comparators is eliminated. For purposes of a.c. measurements the output of the differential amplifier would be connected to a buffer amplifier/phase-sensitive-detector arrangement via a capacitor/analogue-switch coupling arrangement as used in the Mk I. charger. The capacitor coupling to the buffer/p.s.d. arrangement would serve the purpose of removing any residual d.c. voltage existing at the output of the differential amplifier due to imperfect nulling by the DAC.

(c) The interface between the control logic and the analogue charge-discharge circuitry would be improved and would utilise discrete transistors or transistor arrays rather than selected 74LS05 drivers.

(d) The multiplexer relays might be replaced with solid-state analogue switches built from back-to-back discrete MOSFETs. This scheme would allow d.c. measurements to be made with great regularity and might remove the

necessity for the Yellow-User-Button function. Much care would have to be taken in the design of circuits for providing gate drive for such switches and for protecting the MOSFET devices from overvoltages. An alternative method would involve provision of relays for accurate d.c. and a.c. measurements backed up by simple (probably PNP) transistor switches in the response-bus multiplexer for the less exacting but more often used function of battery presence detection via terminal voltage.

New Developments by Motorola Inc.

In April 1990 the Author engaged in a conversation with representatives of Motorola Inc. (U.S.A.) in which many factors pertinent to the value of the Author's research were discussed. It was claimed that Motorola had effectively eliminated the "memory" effect in all of its forms and that, based on information feedback from battery users, continuous "trickle"-charging (possibly implying a C/10 rate) had no apparent harmful effect.

The Author was told that the Rediff(usi)on BC10-type charger was no longer in production, although in use by some British Police divisions, and that "problems" had been experienced with it.

The Author was informed that Motorola Inc. was developing new types Ni-Cd of battery of higher specific energy densities. Unlike previous cells which had both electrodes of sintered construction, a range of batteries was in production incorporating one sintered electrode and one metal "foam" electrode; these batteries have about 20% greater capacity than all-sintered types. Future planned developments included foam-foam electrode cells; a 1300mAh battery having similar dimensions to current 900mAh types was expected within two years. Other possible future battery systems were discussed. Motorola now includes thermistors within

its battery packs such that the batteries currently superceding NTN5048A and similar types have six terminals in total. Motorola has developed a charger for the new varieties of battery which monitors each battery for internal temperature rise as an indicator of commencement of overcharge. The charger initially uses a constant current at an approximate C rate and switches to a low charge rate after a predetermined internal temperature rise (ΔT) is detected. The internal thermistor is also used to determine if the internal temperature of a battery is initially too low or too high for safe charging; if necessary, the charger will delay the commencement of charging of a battery until the battery internal temperature is within preset limits of acceptance. End-of-charge indication methods are also under study which involve monitoring of both temperature rise (ΔT) and terminal voltage rise (ΔV). It was pointed out that ΔT and ΔV methods are extremely advantageous since T and V profiles show a considerable degree of quantitative similarity for batteries over a fairly wide capacity range. It was claimed that this fact enables a single Motorola charger to operate with semi-compatible batteries of varying nominal capacity (for example 900mAh to 1300mAh) without a requirement for adapting charge rates and end-of-charge determination parameters to suit individual battery sizes. The charge rates used in the new Motorola charger are high enough such that the largest sizes of battery likely to be encountered in service are charged in an acceptably fast manner.

The Author's end-of-charge scheme involved in the J.P.B./U.C.S. charger was criticised as being unsuitable for use with batteries of mixed capacity due to the nature of variations of measured parameters with battery capacity. However, the same basic criticism, though for different reasons, was levelled at the Stoneleigh dump-charge charger and at the Redif(fusi)on BC10 charger (which provided some consolation to the Author). The Author subsequently pointed out that profiles during charge

discovered of 0.5Hz Effective-Series-Capacitance for Motorola NTN5048A batteries were of such a form that an end-of-charge indicator based predominantly on trends and gradients, rather than on absolute measured values, seems possible. Hence, provided that future types of Motorola battery display qualitatively similar E.S.C. behaviour then a significant possibility exists that a charger could be developed for Motorola batteries of mixed capacity utilising 0.5Hz measurements for purposes of end-of-charge indication.

A Summary of the Conclusions and Worth of the Research

The reader should note that the technical conclusions of the general cell/battery research are primarily contained in Chapter 11 and in the "Discussions" sections of individual example experiments in Chapter 10. The reader should also note that experimental observations relating to the "J.P.B./U.C.S." stand-alone battery charger are discussed in Chapter 14 and that some late discoveries are outlined at the start of this Chapter. A summary of the overall value of the research project is now given, as follows.

The Author considers that he has performed a very thorough search for results of past research into the field of Ni-Cd battery analysis and charging and that he has given a cautious but realistic appraisal of the usefulness of such work.

The Author has tackled the task of analysing Ni-Cd cells in a far more detailed and thorough manner than previous known researchers, for which purpose the design and construction of a cell/battery testing rig tailored to meet the exact requirements of the task, was of fundamental importance. The capability of the research cell/battery testing rig to

handle up to 48 cells/batteries simultaneously allowed far more extensive studies of Ni-Cd devices than had been achieved by previous known researchers and potentially provided for large-scale meaningful statistical analysis of results (though conflicts of priorities precluded this task in practice); the use of large samples of cells/batteries did have important consequences in that problematic variabilities in impedance parameters between individual cells/batteries were made very obvious.

The Author has consistently applied his knowledge and experimental technique in such a manner as to aim for results which are useful in real-world situations, rather than merely useful for academic appreciation; in particular, when formulating charging-control algorithms the variations in impedance-component response inherent between individual cells/batteries have been allowed for fully. In contrast, previous researchers have generally failed to appreciate the existence of problematic variations or, at least, have not commented at length upon their magnitude and impact.

The Author's most significant discovery is that the impedance-parameter response characteristic of a cell/battery during a charge-discharge process is a function of the origin of manufacture of the cell/battery; for example, cells manufactured by SAFT and VARTA have fundamentally similar characteristic Effective-Series-Capacitance responses during charge-discharge cycling but the corresponding characteristic response for cells by National Panasonic (via Motorola) is most dissimilar.

The Author has concluded that impedance-component measurements are unlikely to be useful for monitoring Ni-Cd cell/battery state-of-charge to a useful accuracy in real-world situations. There is, however, some potential for further research upon state-of-charge indication with relation to highly specific situations where a selected set of cells/batteries is used under a well-defined and regular charge-discharge

regime and, perhaps, where calibration data can be stored for individual cell/battery packs.

The Author has concluded that measurements of cell/battery Effective-Series-Capacitance are usable for purposes of cell/battery end-of-charge detection provided that impedance measurement methods are integrated into a carefully defined charging strategy. The Author has described three possible charging algorithms (See Chapter 11) for use with cells of SAFT manufacture; these algorithms should be considered as non-exhaustive examples and serve to illustrate important considerations.

The Author has investigated the influence upon impedance-component results of d.c. currents applied through cells and batteries at the time of a.c. impedance measurements. The influence of such currents was not known to have been studied by previous researchers. The worth of such "bias" currents was found to be dependent upon the exact type of cell/battery under study. With regard to charge-discharge currents in an essential sense from the point of view of hardware design, the Author has described serious problems associated with the modification of cell/battery charge-discharge currents prior to measurements which afflict short-duration "a.c." measurements in a systematic manner.

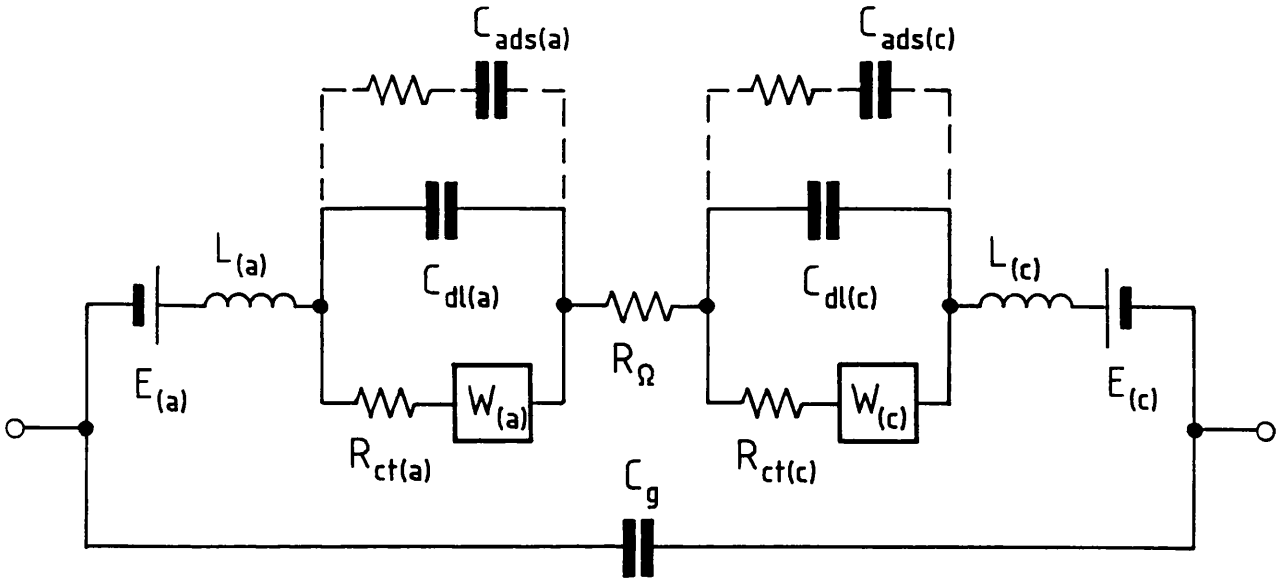
The Author has briefly investigated the second-harmonic response of one type of battery to sinewave excitation at test frequencies of 2Hz to 32Hz. The concept was not known to have been considered by previous researchers in the field of Ni-Cd battery study. Experiments indicated that second-harmonic response did not appear to be of much worth from the point of view of analysis of battery charge status because results were closely related to fundamental response and were very susceptible to problematic side-effects and noise.

Finally, the Author applied his knowledge and experience of Ni-Cd cells/batteries and of electronics to design and construct a unique,

nominally "intelligent", stand-alone battery charger/processor, namely the "J.P.B./U.C.S." charger for PYE P.F.X. radio communications handset batteries. This charger incorporates a microprocessor, utilises Effective-Series-Capacitance measurements at sub-audio frequencies and has many advanced hardware features that would not normally be expected of a battery charger. The charger is designed for a specific application and utilises a charging and measurement strategy tailored to suit the application. With modifications and upgrades, which the Author has described, the charger has some potential as a marketable product.

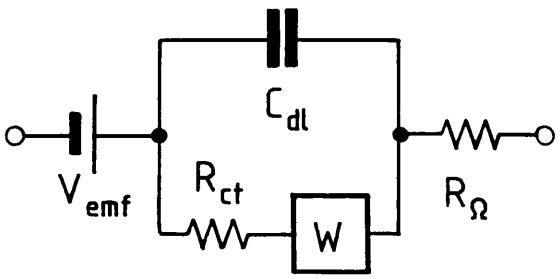
As a concluding statement of this document, the Author considers it wise to suggest that any possible future continuation of the research scheme, initiated at the University College of Swansea, is unlikely to achieve useful results unless a close liaison is developed with a selected major battery manufacturer.

(i) A comprehensive Electrical Equivalent Circuit for a Ni-Cd Cell
(not considering transmission-line behaviour of porous electrodes)



Notes :- Subscripts (a) and (c) denote anode and cathode respectively
E = Electrode potential
L = Electrode/conductor inductance
C_{dl} = Double-layer (non-Faradaic) capacitance
R_{ct} = Charge-transfer resistance
W = Warburg (diffusional) impedance
C_{ads} = Adsorption pseudocapacitance
R_Ω = Electrolyte/separator resistance
C_g = Interelectrode (geometric) capacitance

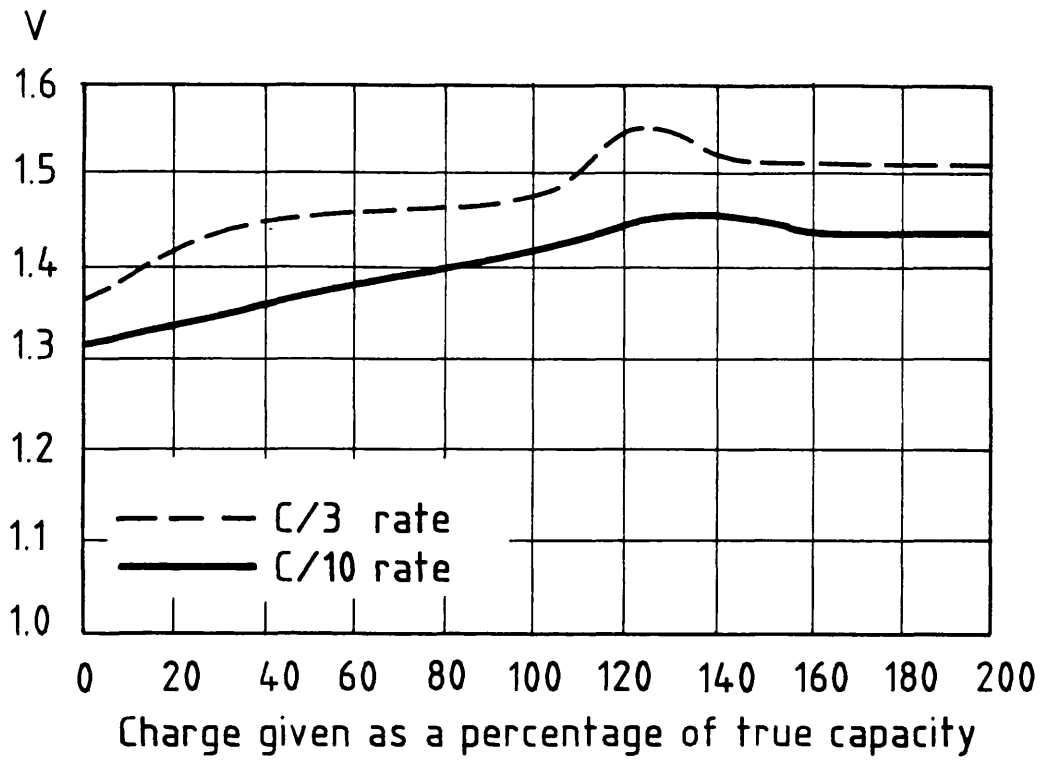
(ii) The Randles Electrical Equivalent Circuit for the Ni-Cd Cell



Notes :- $V_{emf} = (E_a - E_c)$ = cell/battery e.m.f.
(Other components are as for (i) above)

FIGURE 1

(i) Typical Profiles of Terminal Voltage for a Ni-Cd Cell on Charge at Two Charge Rates



(ii) Typical Profiles of Internal Temperature and Internal Pressure for a Ni-Cd Cell on Charge at Two Charge Rates

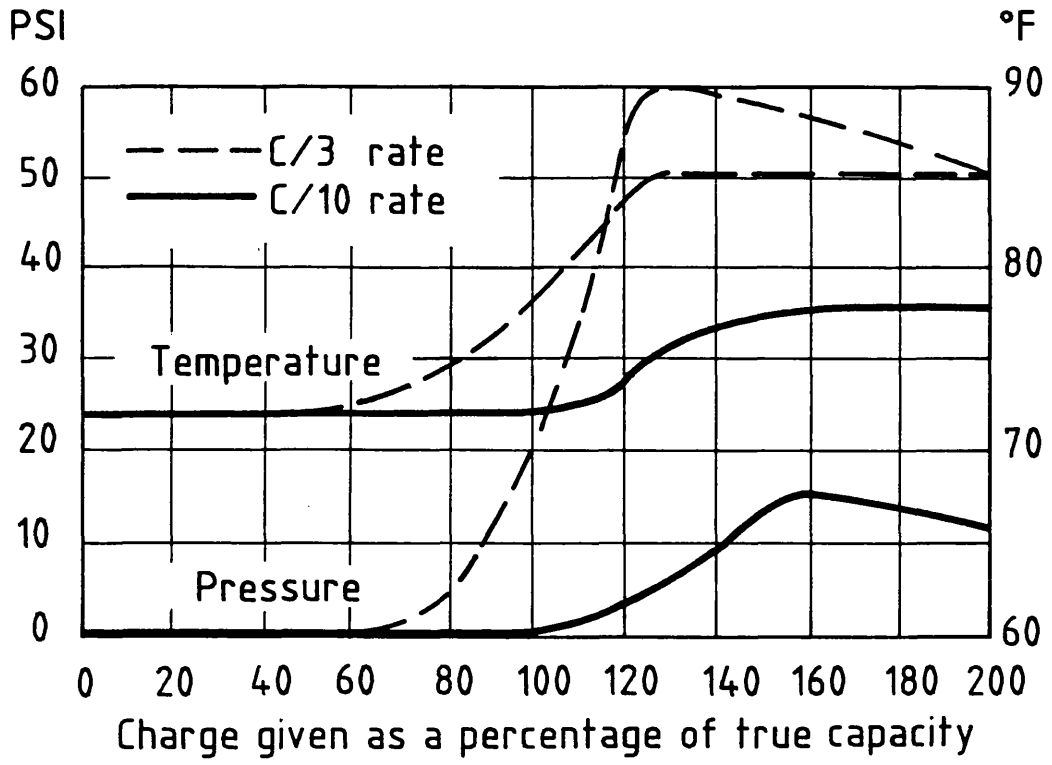


FIGURE 2

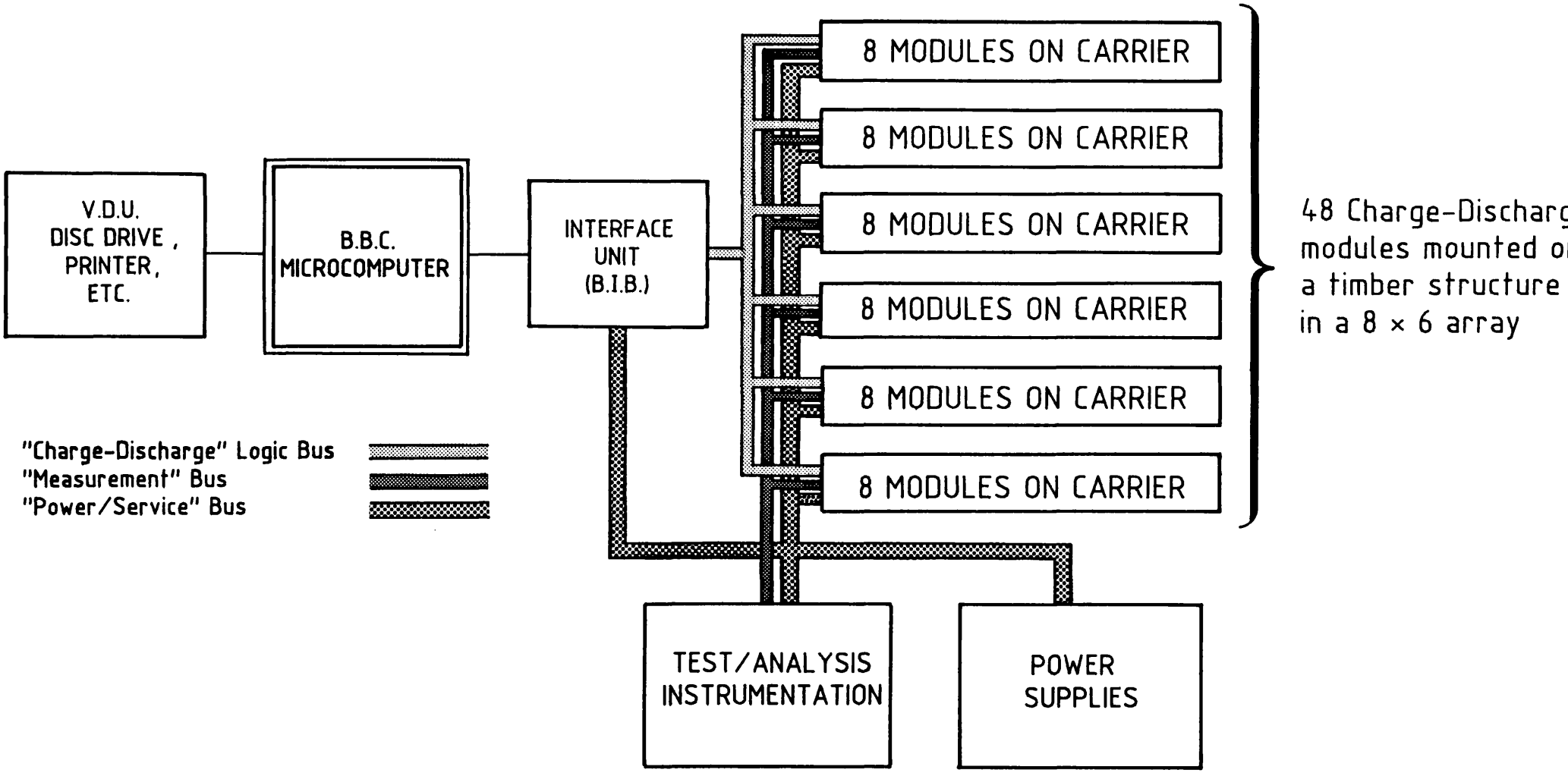
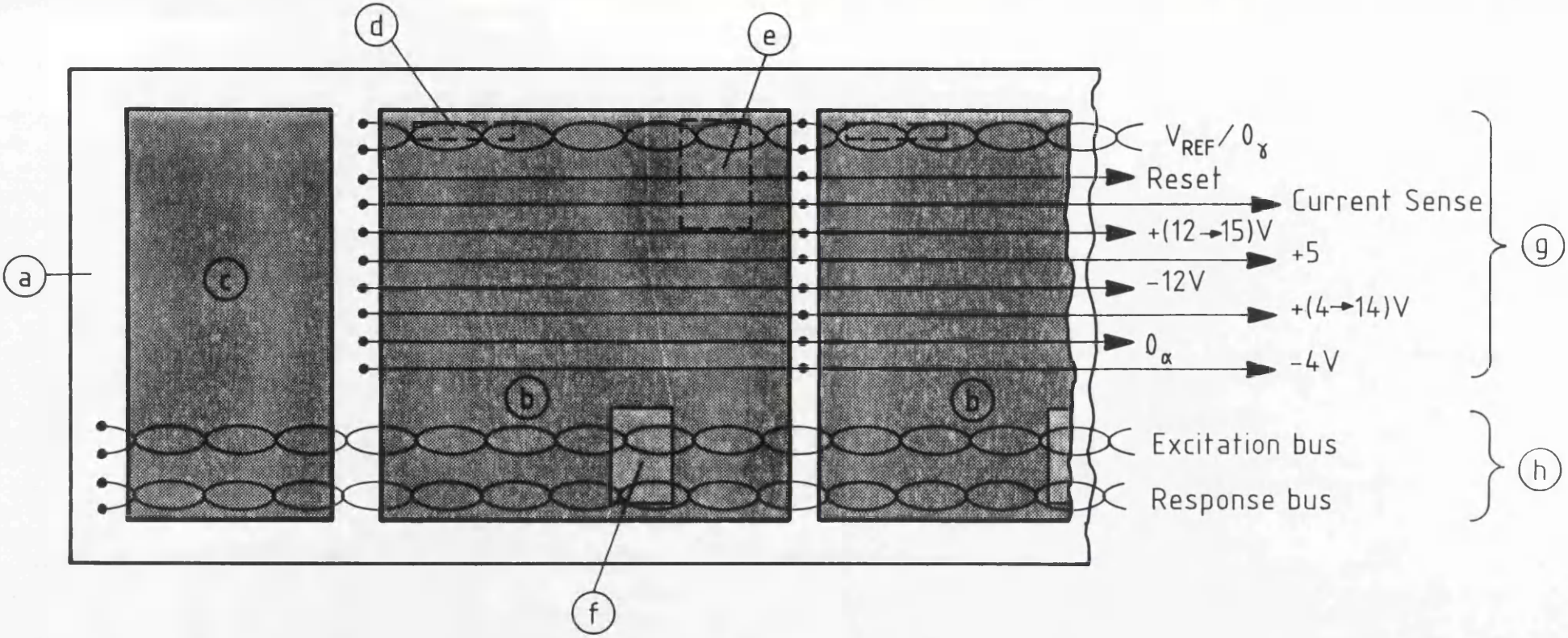


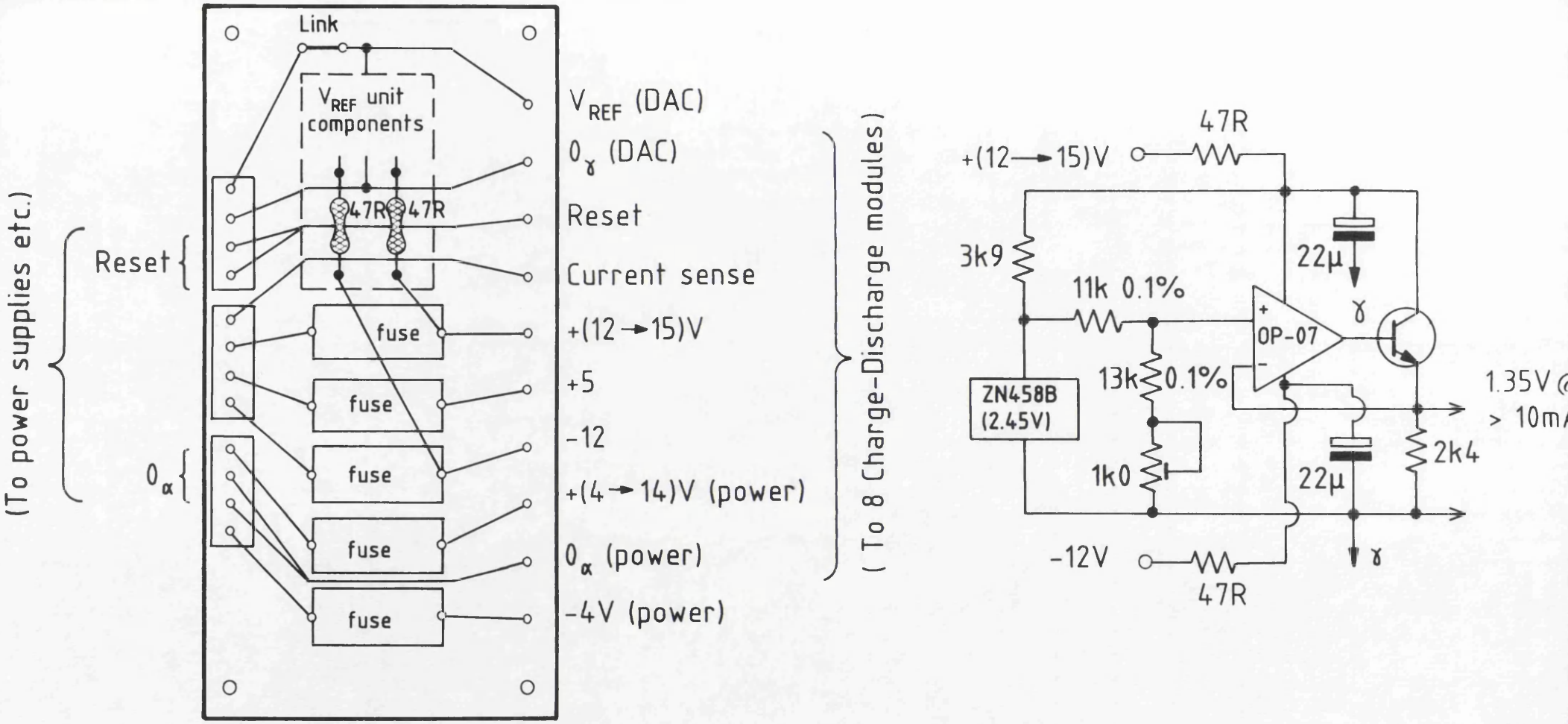
FIGURE 3 THE GENERAL ARCHITECTURE OF THE CELL/BATTERY TEST RIG



Notes :-

- a Board Carrier of timber construction (one of six in a vertical stack on a timber frame)
- b Charge-Discharge board (eight per carrier in a row) mounted on front surface of Board Carrier
- c Fuse/V_{REF} board (one per carrier) - connected permanently to Power/Service bus
- d Power/Service connector on Ch-D board - connected via connector/wires to Power/Service bus
- e Logic connector on Ch-D board - connected via connector to daisy-chained logic bus (the logic bus is of ribbon-cable and runs in front of Ch-D modules)
- f Four-pole relay on Ch-D board -connected via soldered wires to Measurement bus
- g Power/Service bus of discrete wire construction mounted on rear surface of Board Carrier
- h Measurement bus of discrete wire construction mounted on rear surface of Board Carrier

FIGURE 4 THE LAYOUT OF A CH-D BOARD CARRIER AND SOME ASSOCIATED PARTS



Note :- The board layout is to scale and shows the positions of fuses , terminal blocks/pins and the V_{REF} circuitry

FIGURE 5 THE LAYOUT AND CIRCUIT OF A FUSE/V_{REF} BOARD

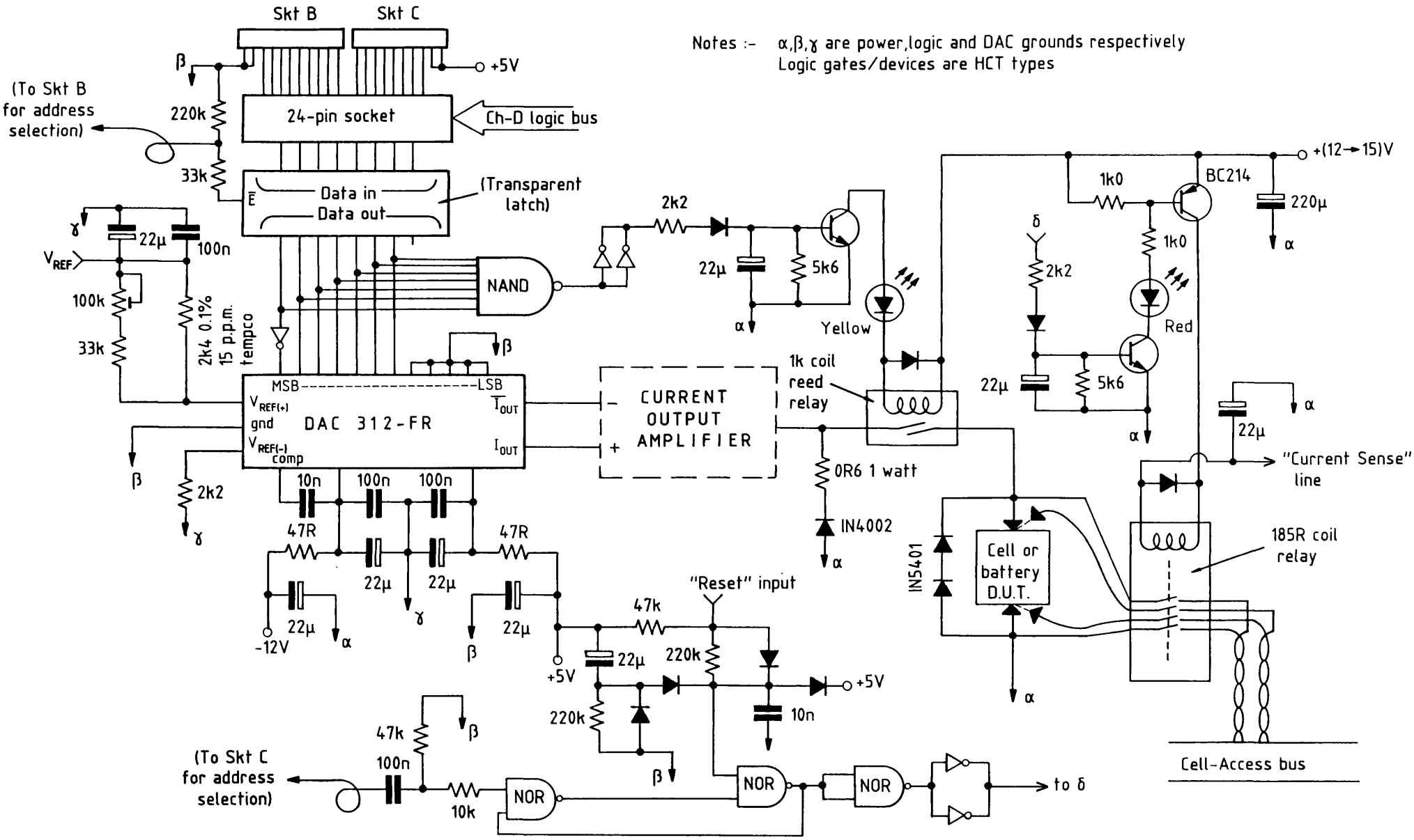
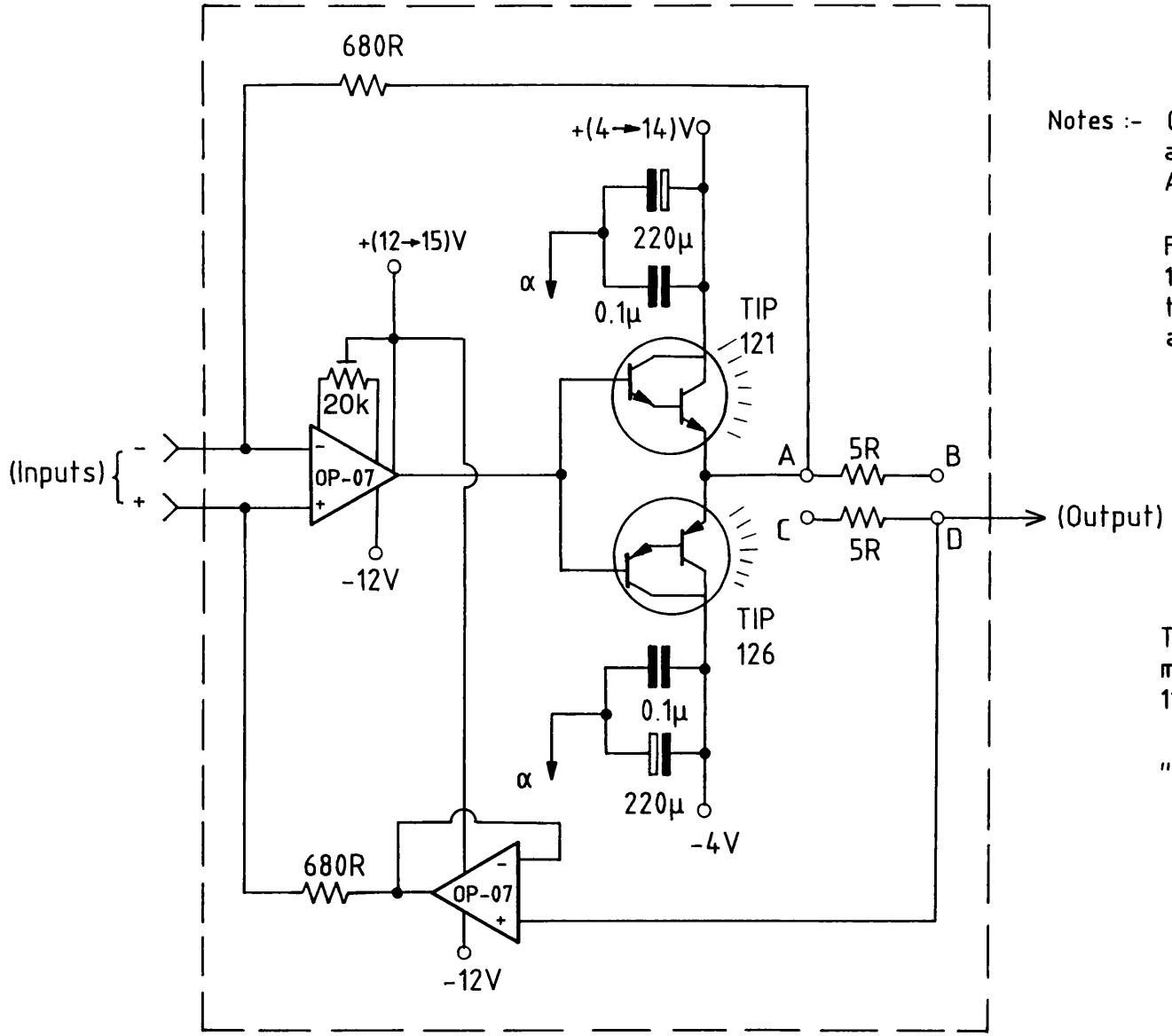


FIGURE 6(a) THE CIRCUITRY OF A CHARGE-DISCHARGE MODULE/BOARD



Notes :- Current gains of 68,136 or 272 are selectable by linking points A,B,C,D appropriately

Fixed resistors are 0.1% , 15 p.p.m. tempco types and the "5Ω" resistors have an effective 1 watt rating

The output transistors are mounted on a shared 11.5°C/watt heatsink

"α" refers to Power ground

FIGURE 6(b) THE CHARGE-DISCHARGE MODULE CURRENT OUTPUT AMPLIFIER

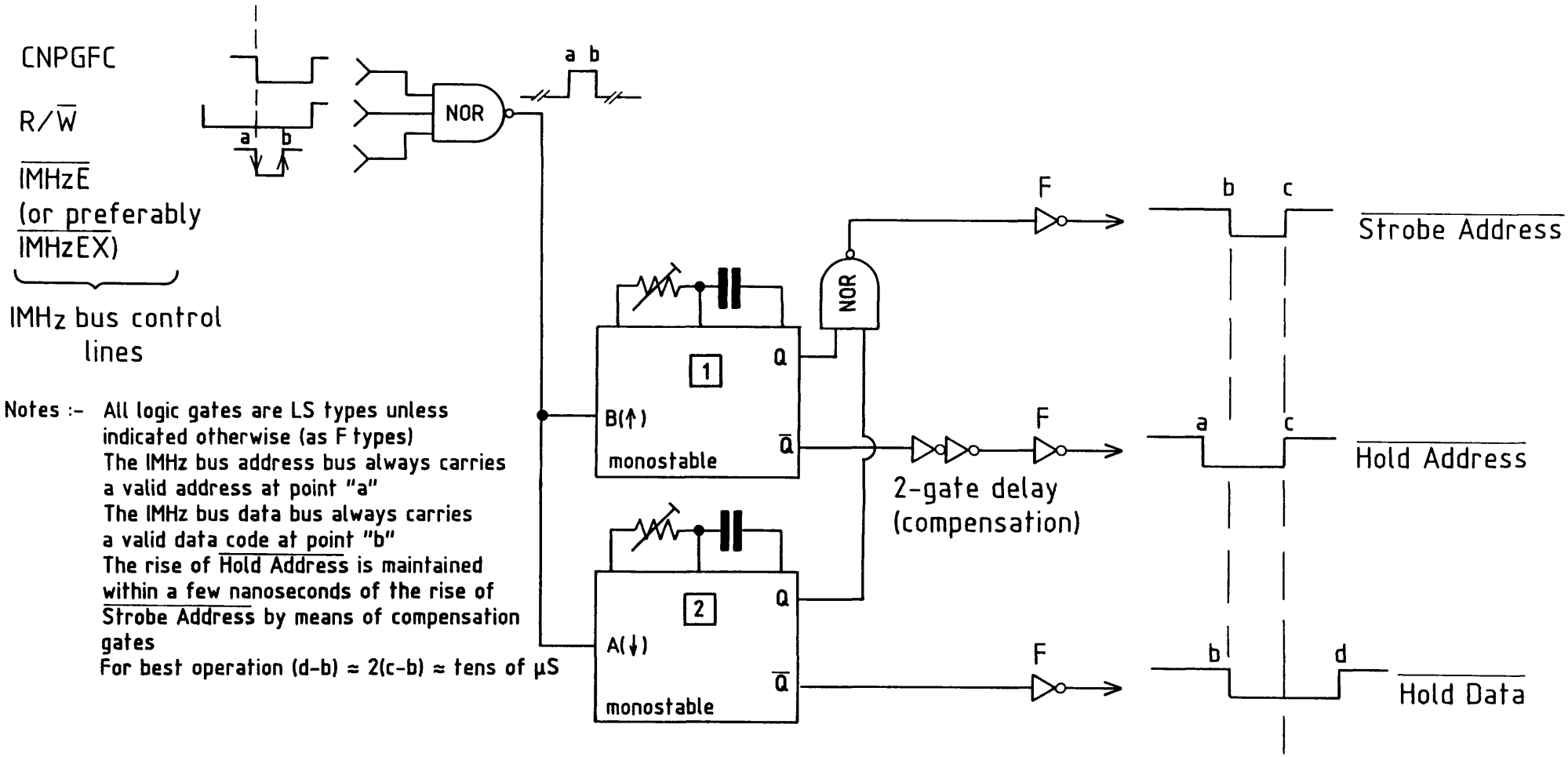
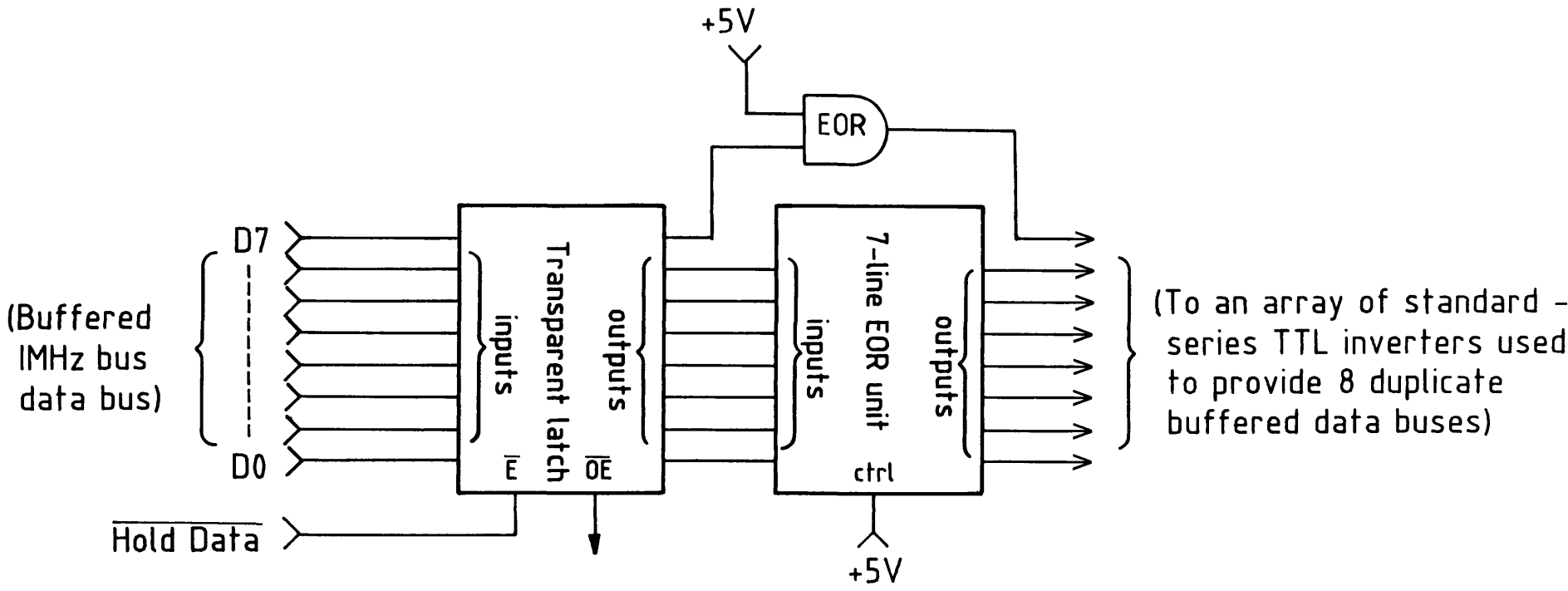
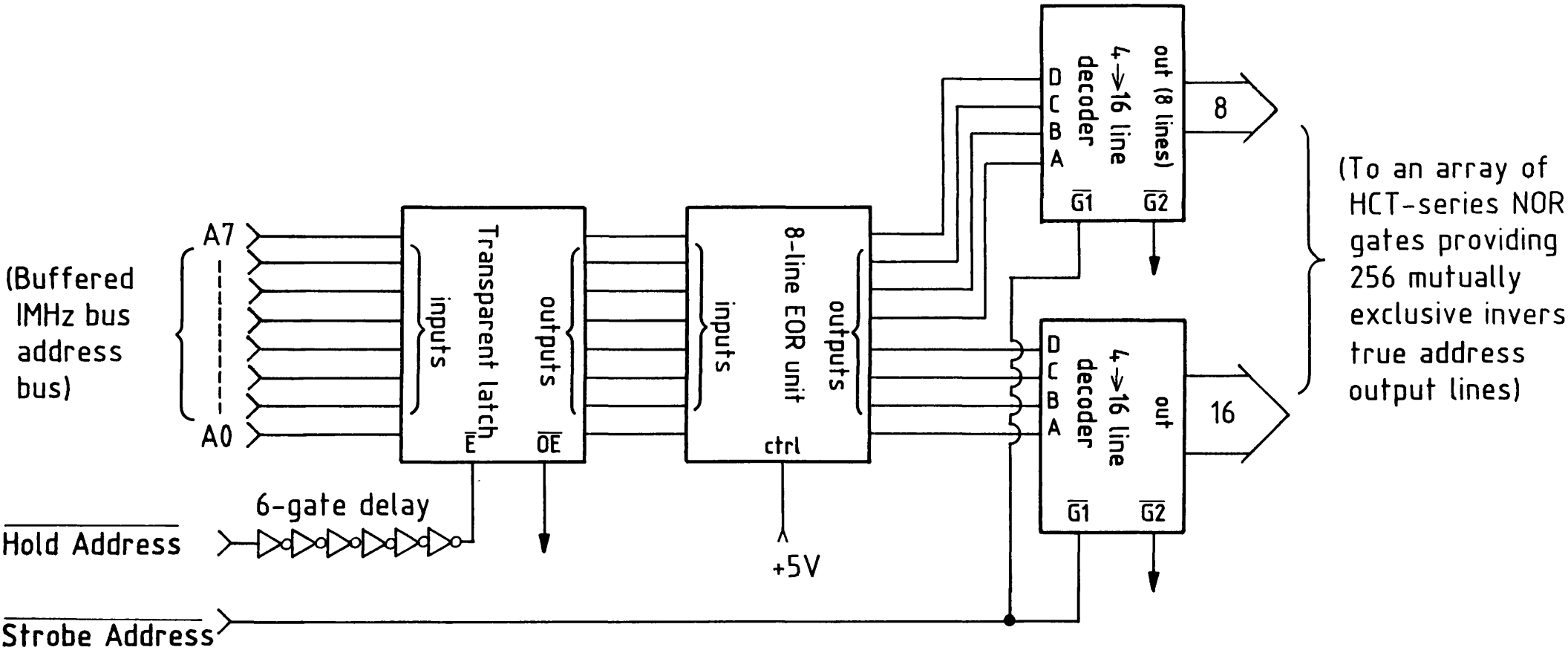


FIGURE 7(a) THE Ch-D LOGIC BUS PULSE EXTENSION TIMING LOGIC AND TIMINGS



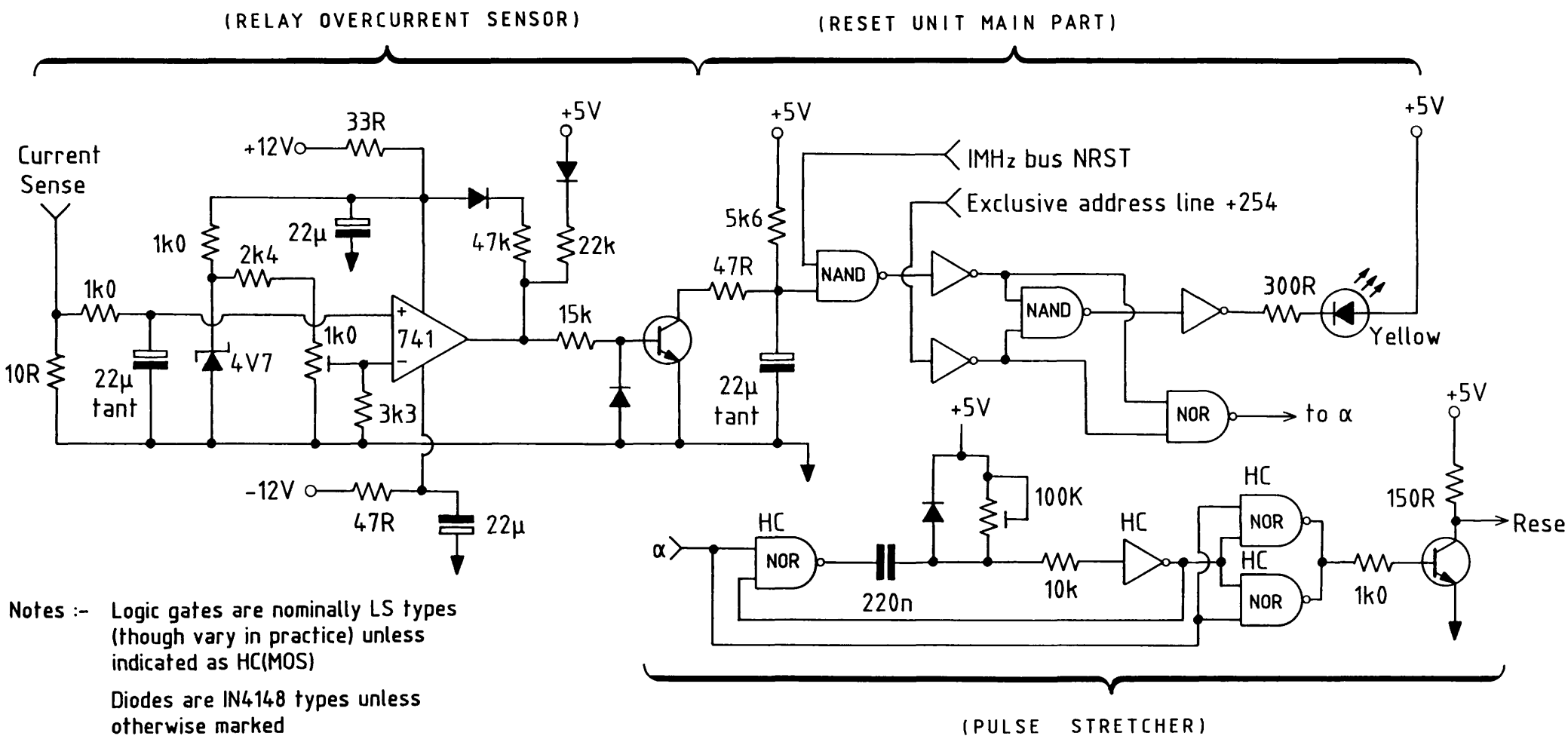
Notes :- All logic gates are LS types unless indicated otherwise (as standard TTL types)
The EOR gate and "7-line EOR unit" allow selection between direct buffering or inverted buffering of data lines (D0→D6) and D7 separately (In practice all data lines are direct buffered)
The ground shown is local (logic)

FIGURE 7(b) THE Ch-D LOGIC BUS DATABUS EXPANDER/BUFFER INCORPORATING DATA PULSE EXTENSION



Notes :- All logic gates are LS types unless indicated otherwise (as HCT types)
The 4→16 line decoder outputs are used in a reverse configuration such that these decoders require inverse-logic codes at inputs A,B,C,D
The "8-line EOR" unit allows selection between true-logic and inverse--logic address inputs (but in practice is set always for the true-logic case)
All grounds shown are local (logic)

FIGURE 7(c) THE Ch-D BUS ADDRESS DECODER INCORPORATING ADDRESS PULSE EXTENSION



Notes :- Logic gates are nominally LS types (though vary in practice) unless indicated as HC(MOS)

Diodes are IN4148 types unless otherwise marked

FIGURE 8 THE RESET UNIT AND RELAY OVERCURRENT SENSOR

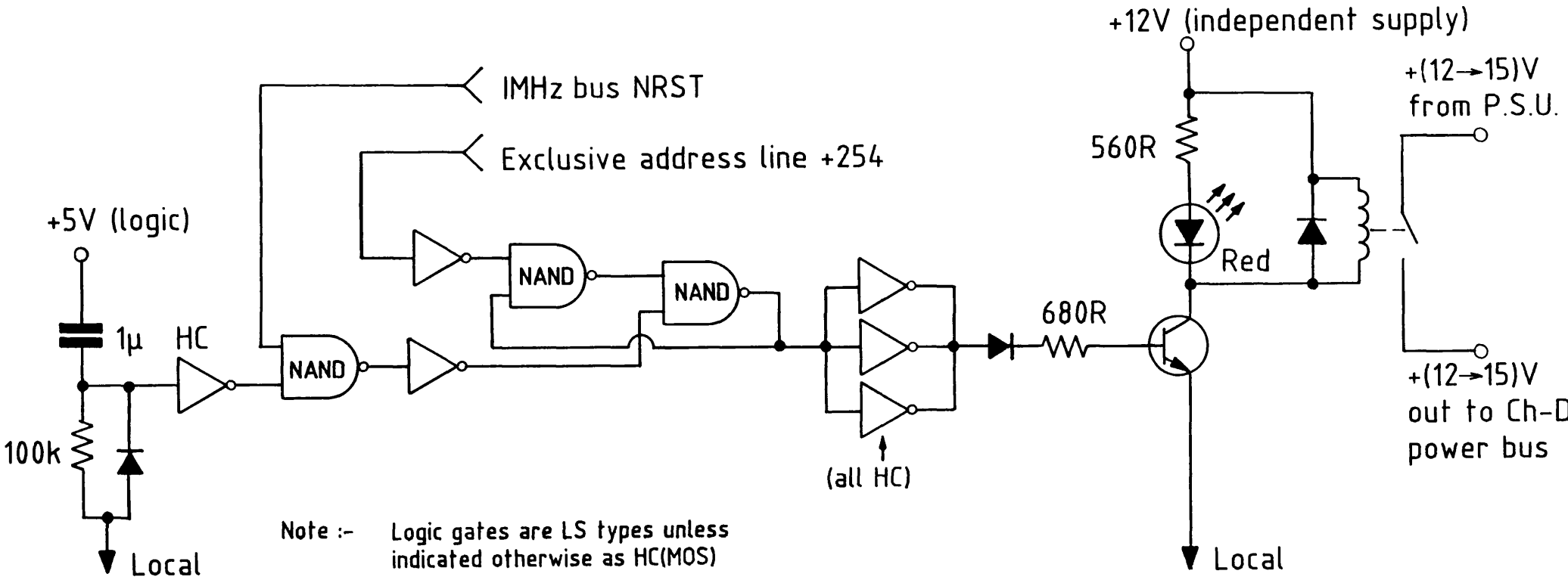
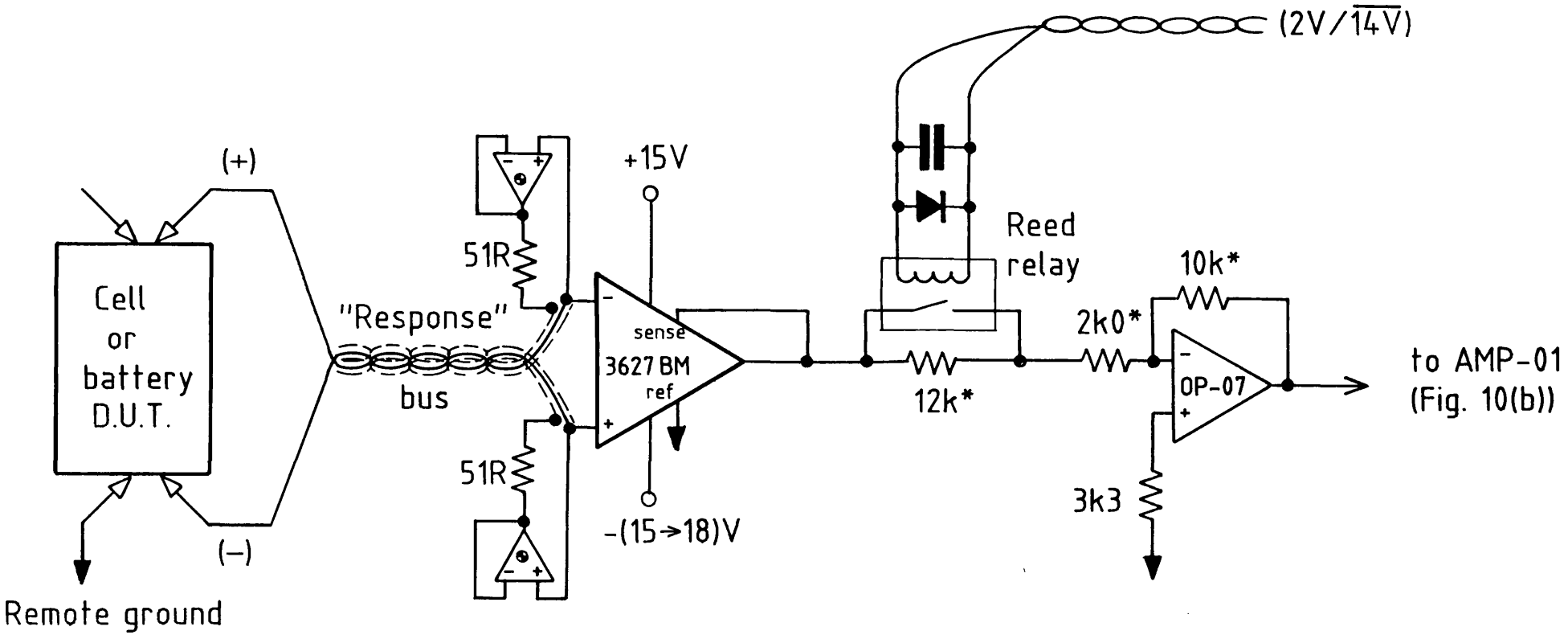


FIGURE 9 THE CIRCUIT OF THE POWER CRASH PROTECTOR



Notes :- The 3627 BM differential amplifier is unity gain and has input impedance of 25k
The resistors marked * are matched to ±0.1% , are matched for tempco to ±5p.p.m. and are cemented together in thermal contact
The reed relay is mercury-wetted type and is driven via a low-noise driver from the 2V/14V signal
The input leads to the 3627 should be well matched since , for example, a 2Ω source imbalance degrades the C.M.R.R. to less than 80dB
The Response bus in the completed system included a section of individually-screened , twisted-pair conductors. These require a pair of shield (screen) drivers . These comprise two OP-07 op-amps marked ⊛ in the above diagram

FIGURE 10(a) THE DETECTOR UNIT PREAMPLIFIER AND AMPLIFIER STAGES

Notes:- Null polarity and magnitude data informtion is provided from a latch on the Control Board
The resistors marked * are 0.1% , 3p.p.m. tempco types and are a closely matched pair (with optional trimming)
Other precision resistors are 15p.p.m. tempco types
The relay is driven via a driver circuit from the A.C./$\overline{D.C.}$ signal

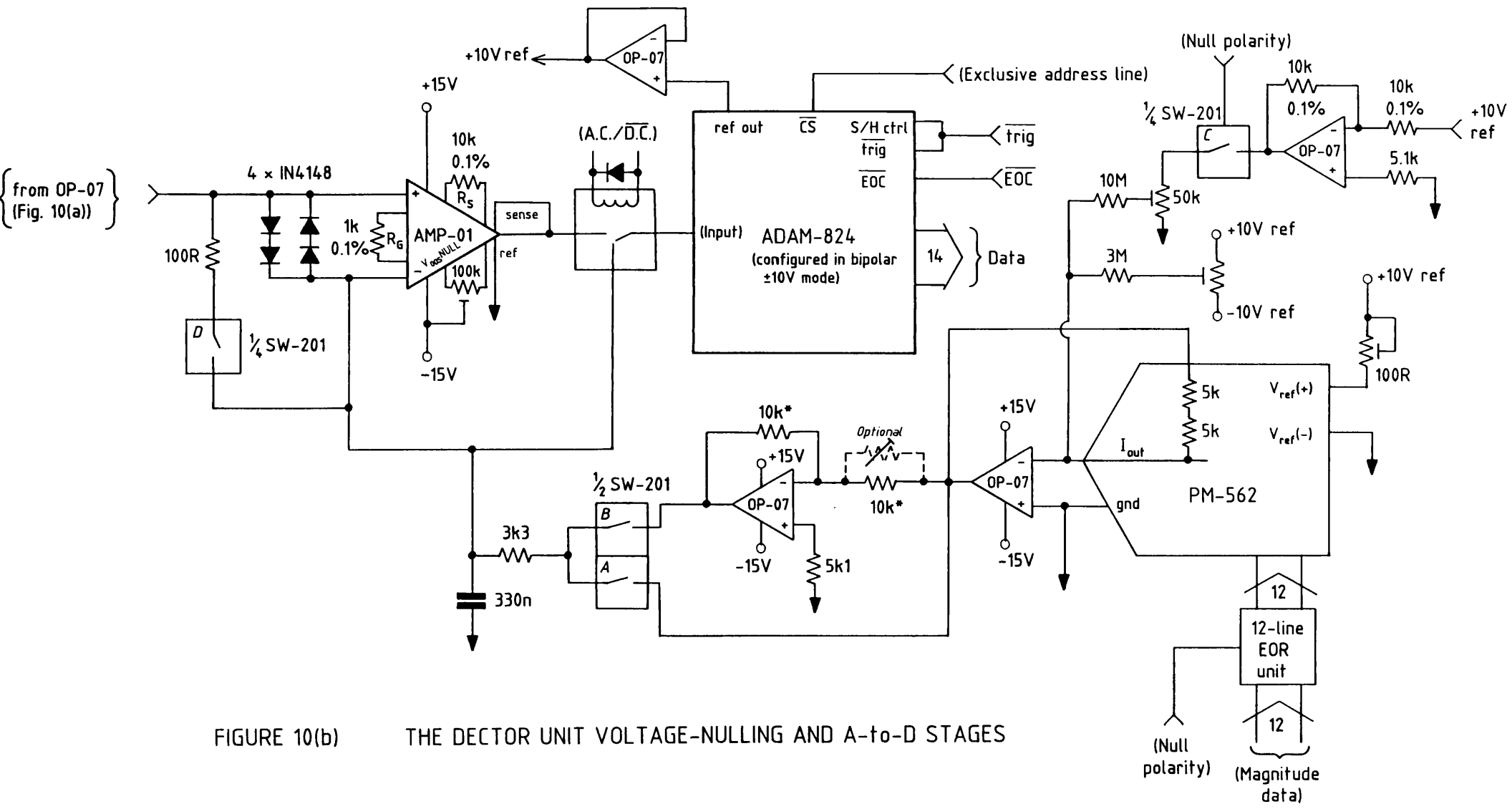


FIGURE 10(b) THE DECTOR UNIT VOLTAGE-NULLING AND A-to-D STAGES

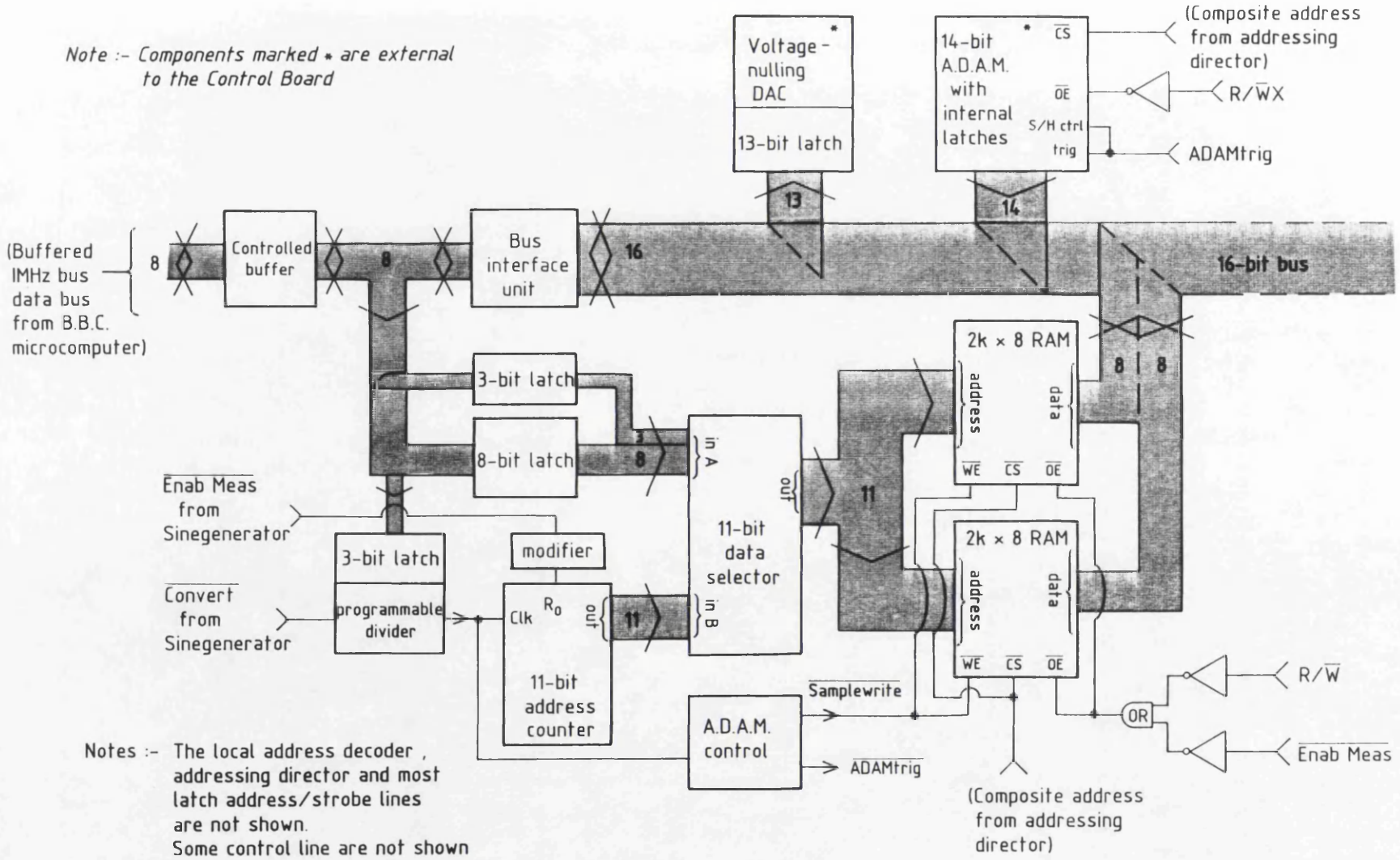


FIGURE 11 THE ARCHITECTURE OF THE CONTROL (LOGIC) BOARD

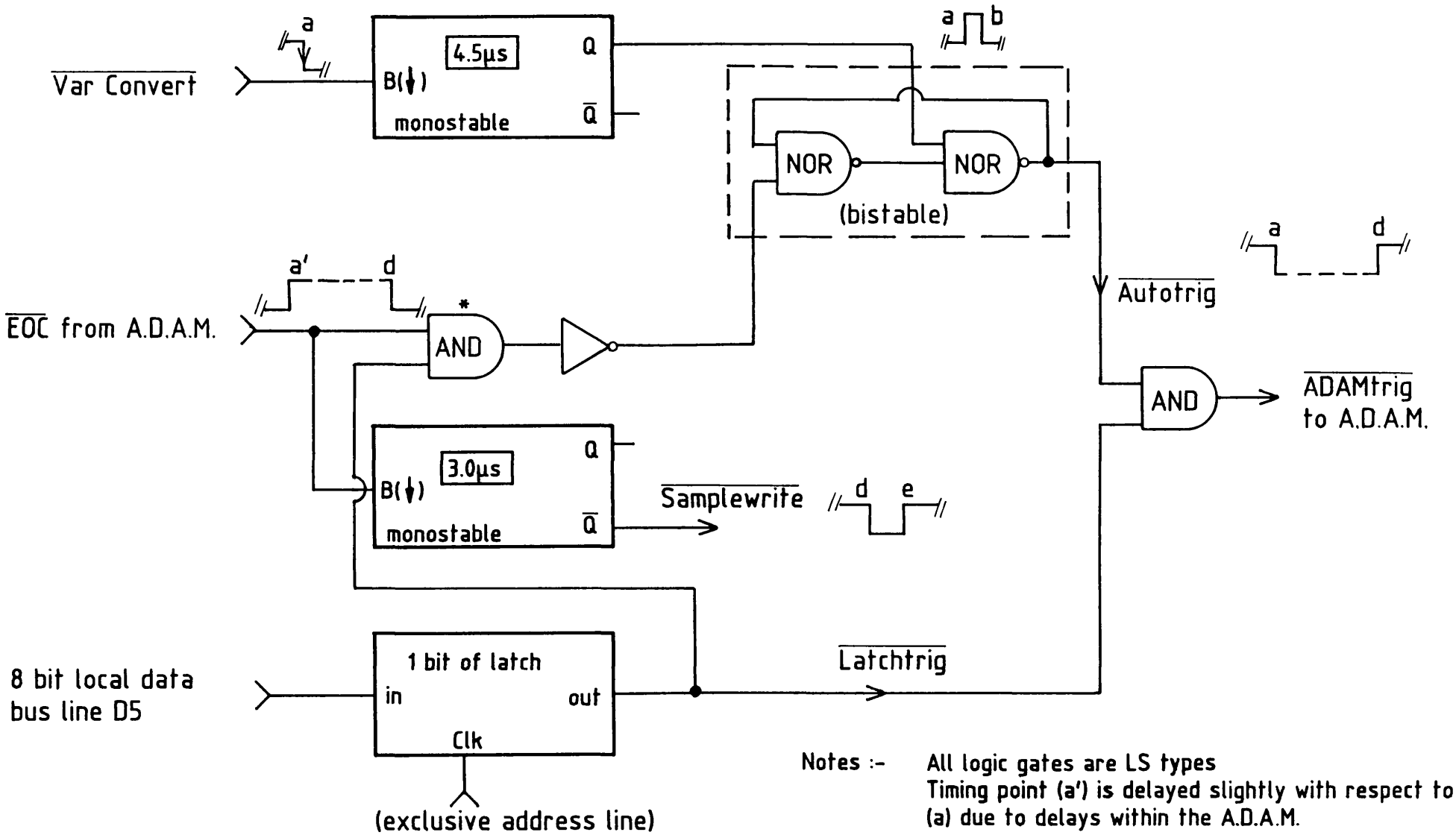
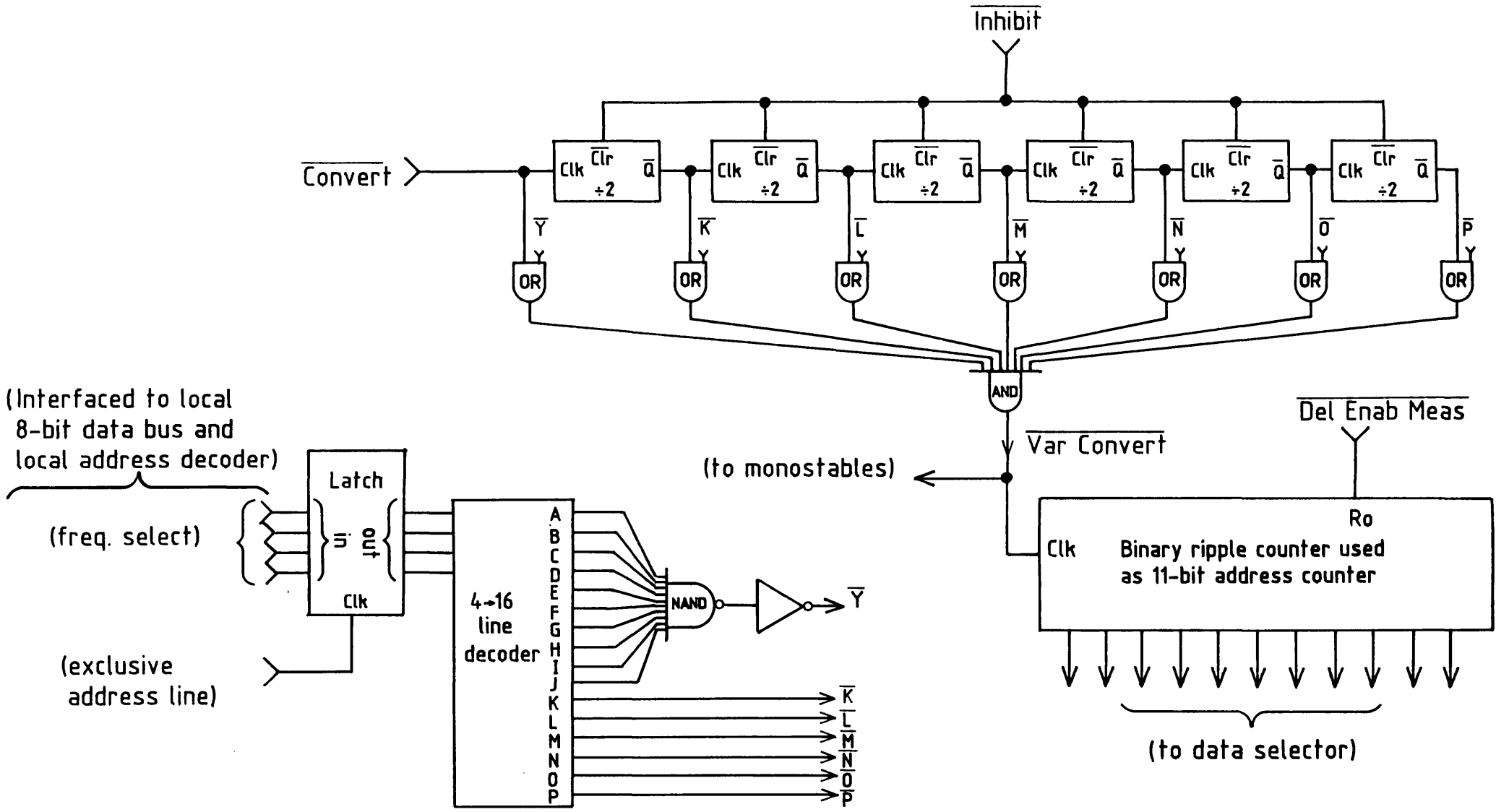
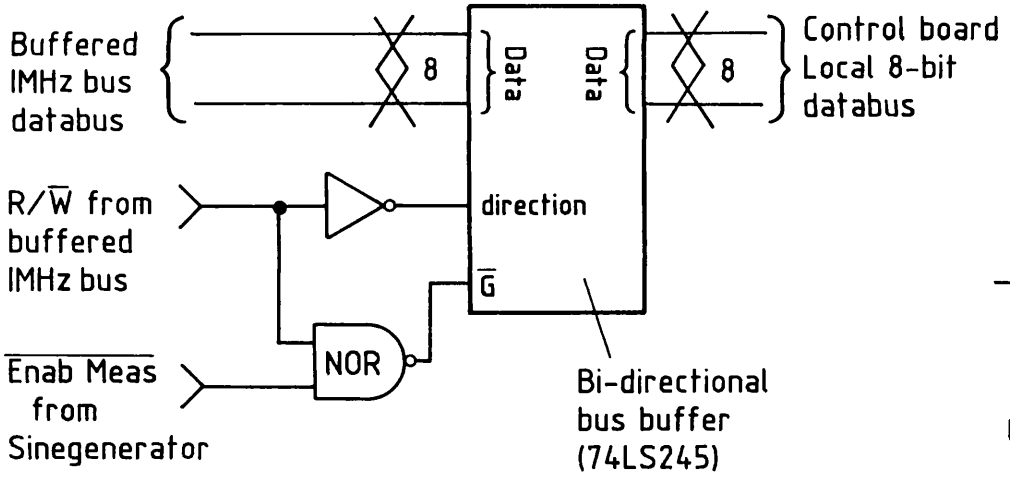


FIGURE 12(a) THE A.D.A.M. TIMING/TRIGGER LOGIC
(part a)



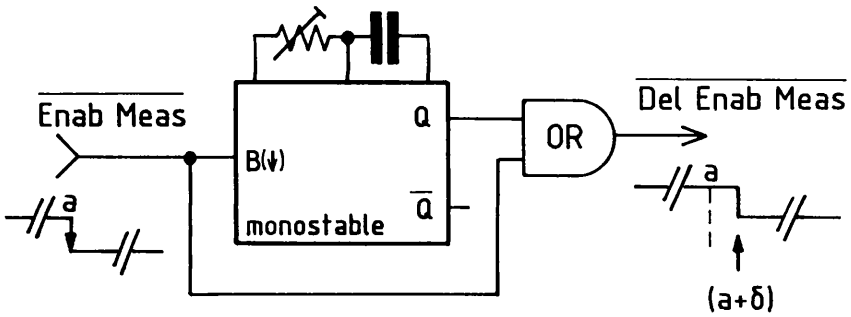
Notes :- All logic gates are LS types
The latch is programmed in parallel with the programming latch on board the Sine Generator

FIGURE 12(b) THE A.D.A.M. TIMING/TRIGGER LOGIC {part (b)}



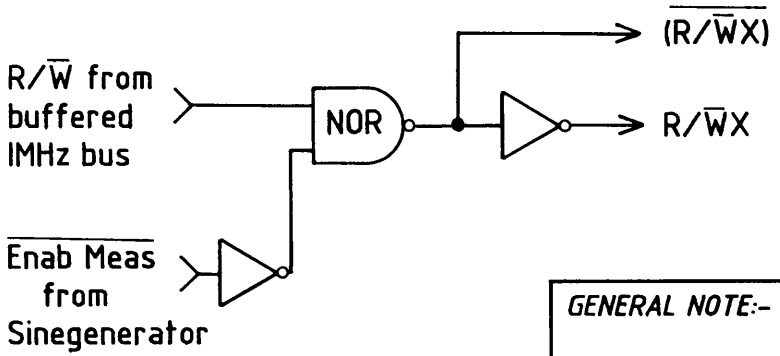
Note :- This logic control disables IMHz bus "Write" operations when Enab Meas is low

(i)

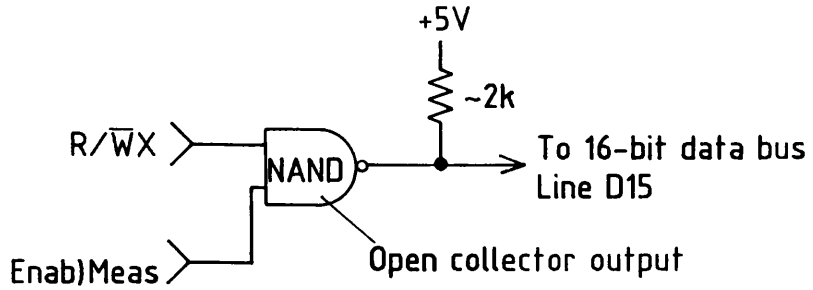


Note :- Del Enab Meas is used to clear the 11-bit address counter
The monostable gives a pulse of length δ≈1.65μs

(ii)



(iii)



Note :- This arrangement allows the state of the Enab Meas line to be monitored by a controller computer

(iv)

GENERAL NOTE:- All logic gates are LS types

FIGURE 13 DATA BUS NOT-ENAB(LE) MEAS(UREMENT) AND READ-NOT-WRITE LINE MODIFICATION

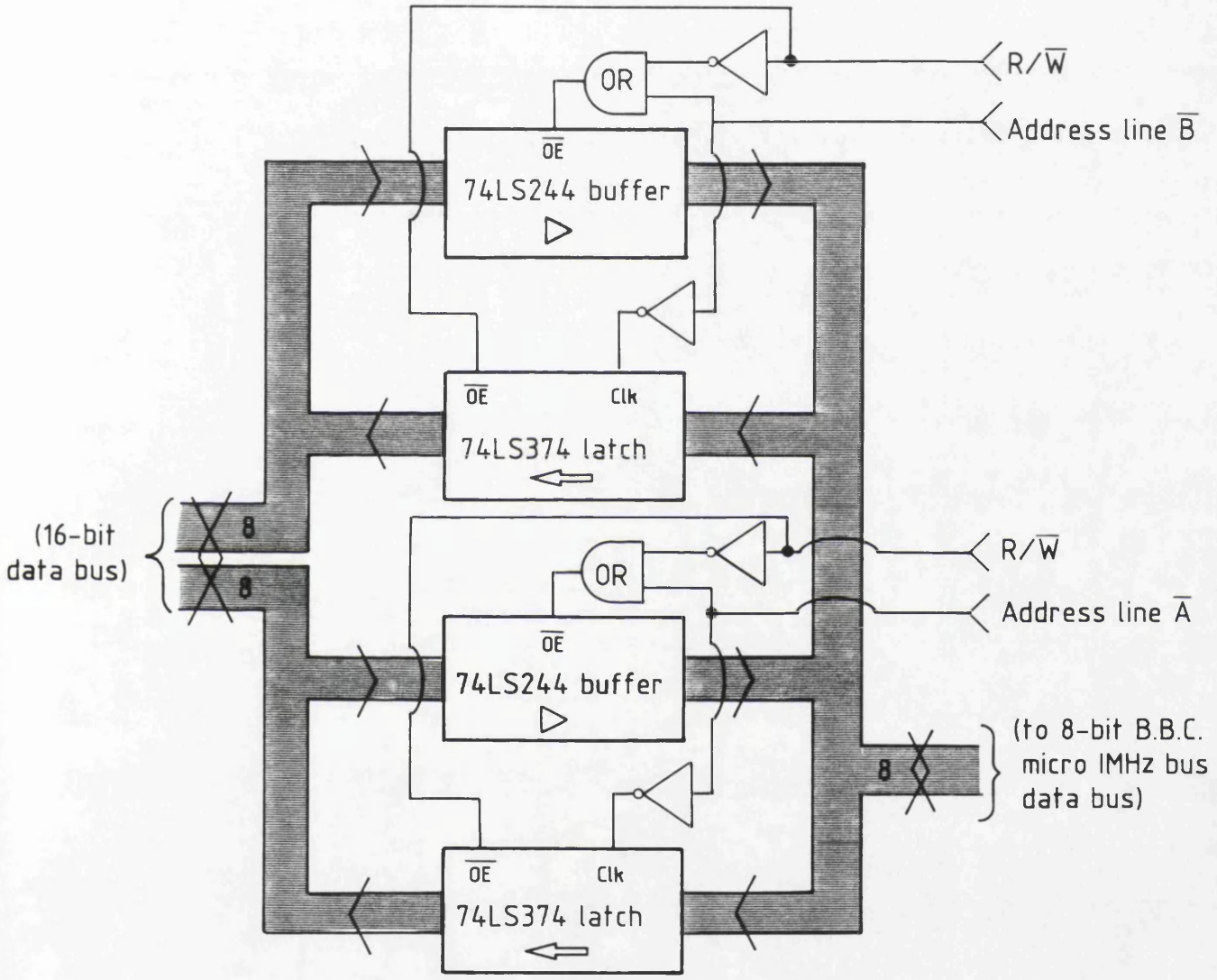


FIGURE 14 THE BUS-INTERFACE UNIT

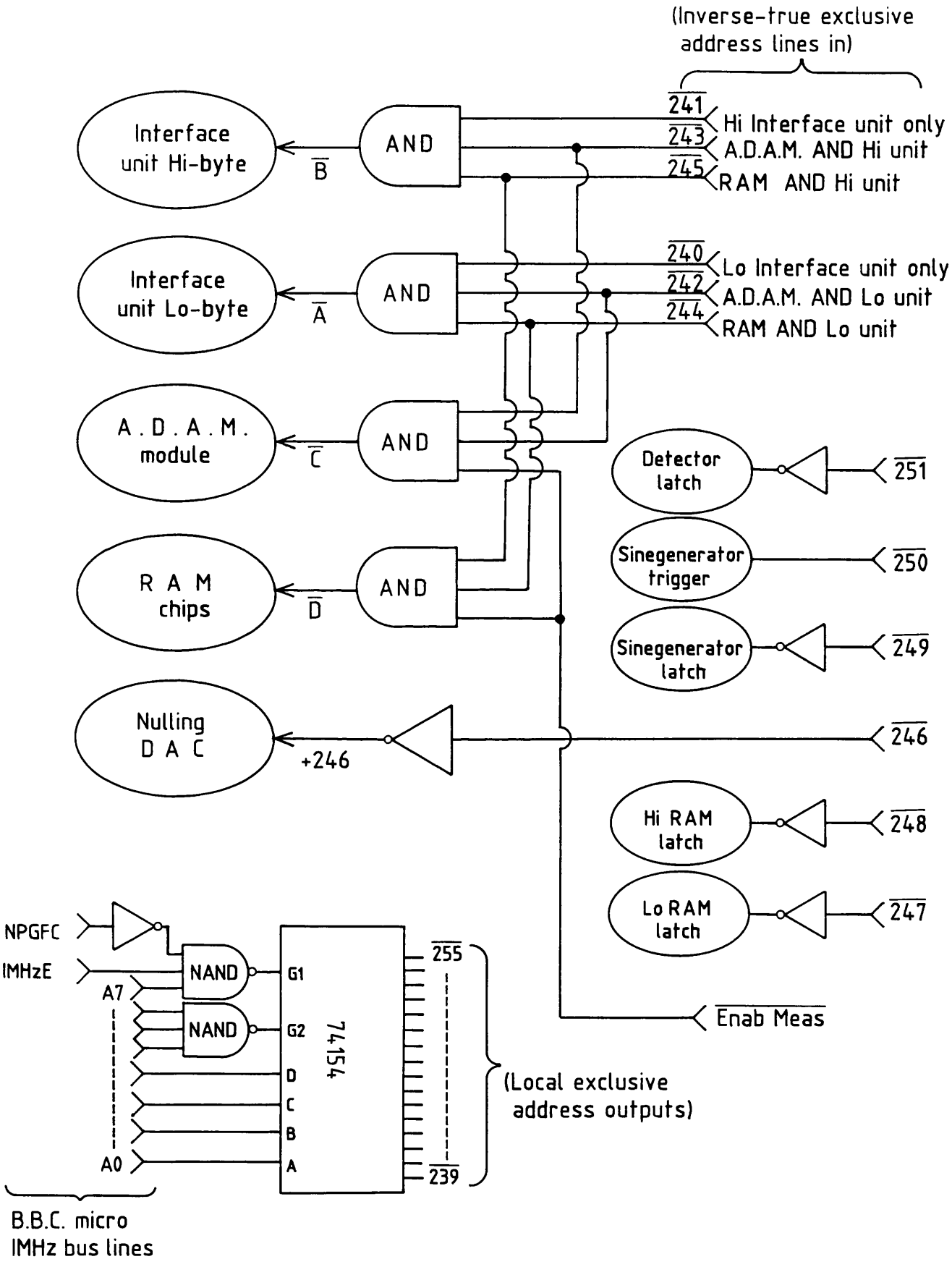
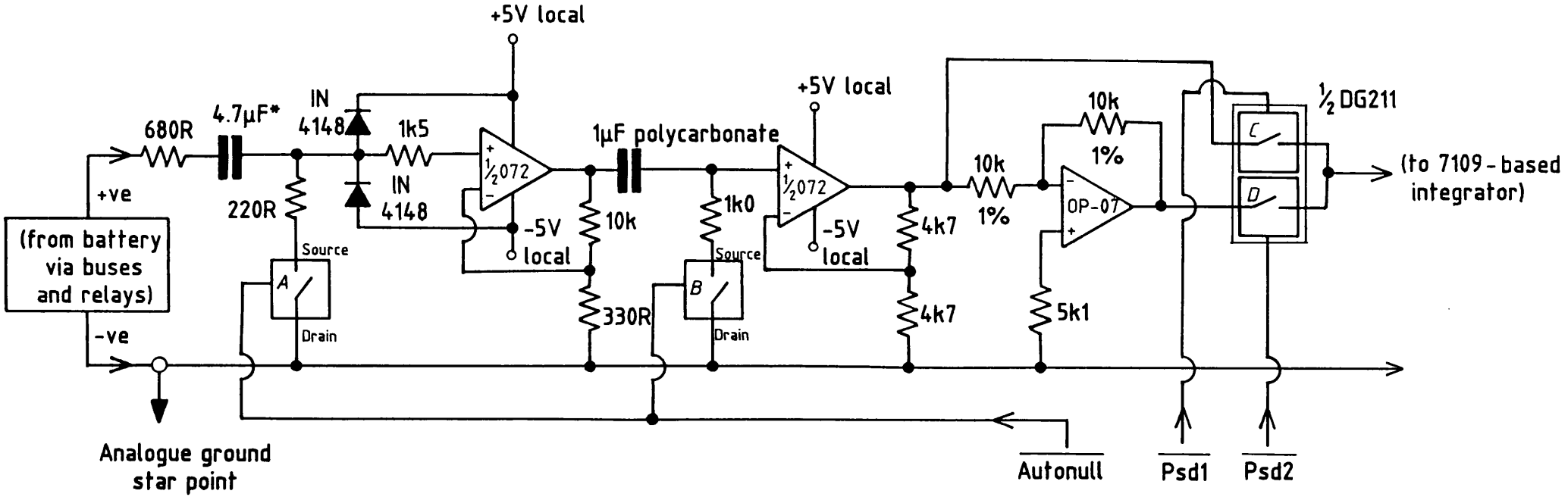


FIGURE 15 THE LOCAL ADDRESS DECODER AND ADDRESSING-DIRECTOR LOGIC (ON CONTROL BOARD)



Notes :- Supply decoupling capacitors are omitted for clarity
The capacitor marked * was a polycarbonate type
in the prototype but a polypropylene type is preferable

FIGURE 101(a) THE AMPLIFIER AND PHASE-SENSITIVE RECTIFIER STAGES OF THE J.P.B./U.C.S. CHARGER (RESPONSE-VOLTAGE) DETECTOR

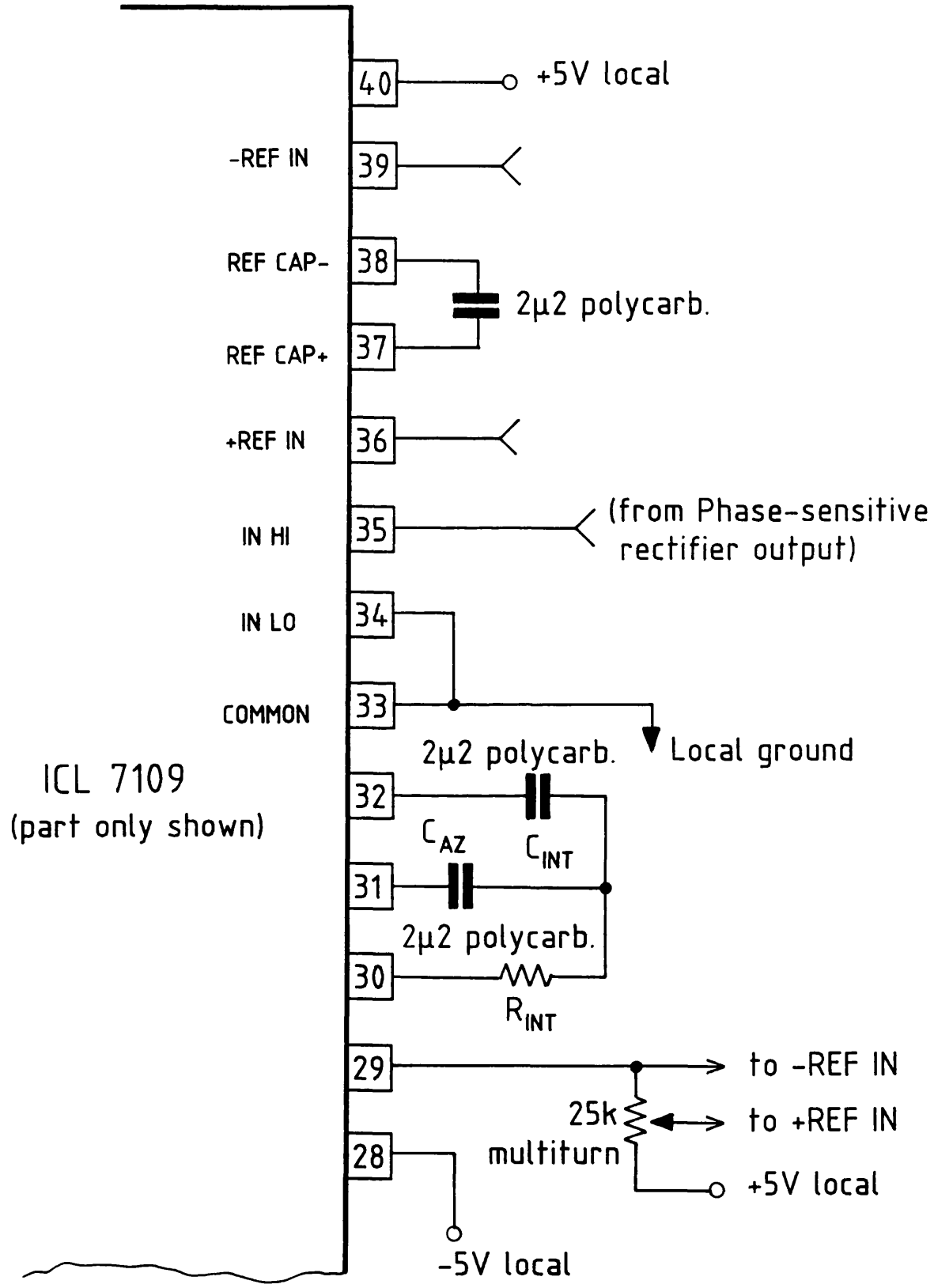
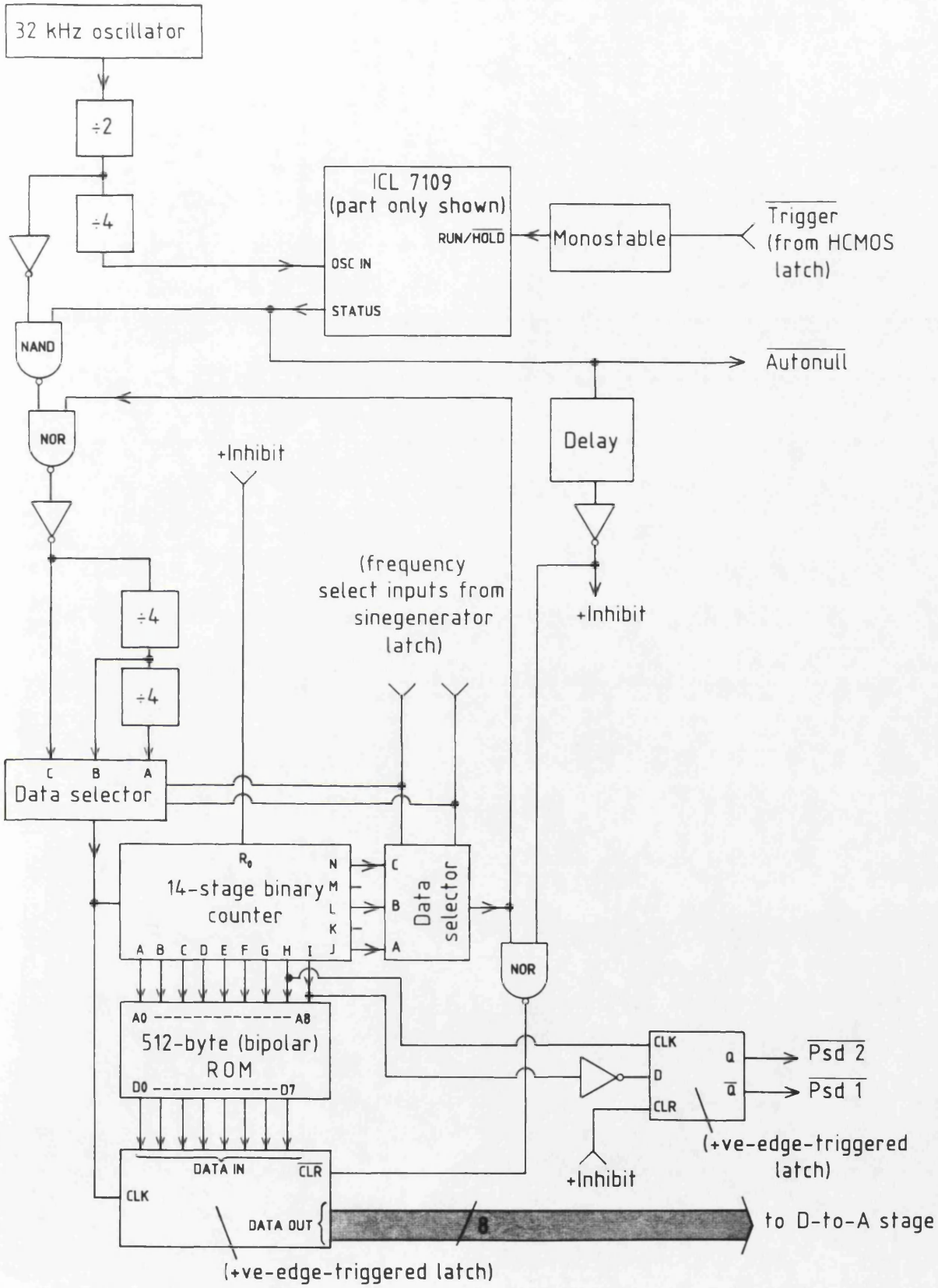
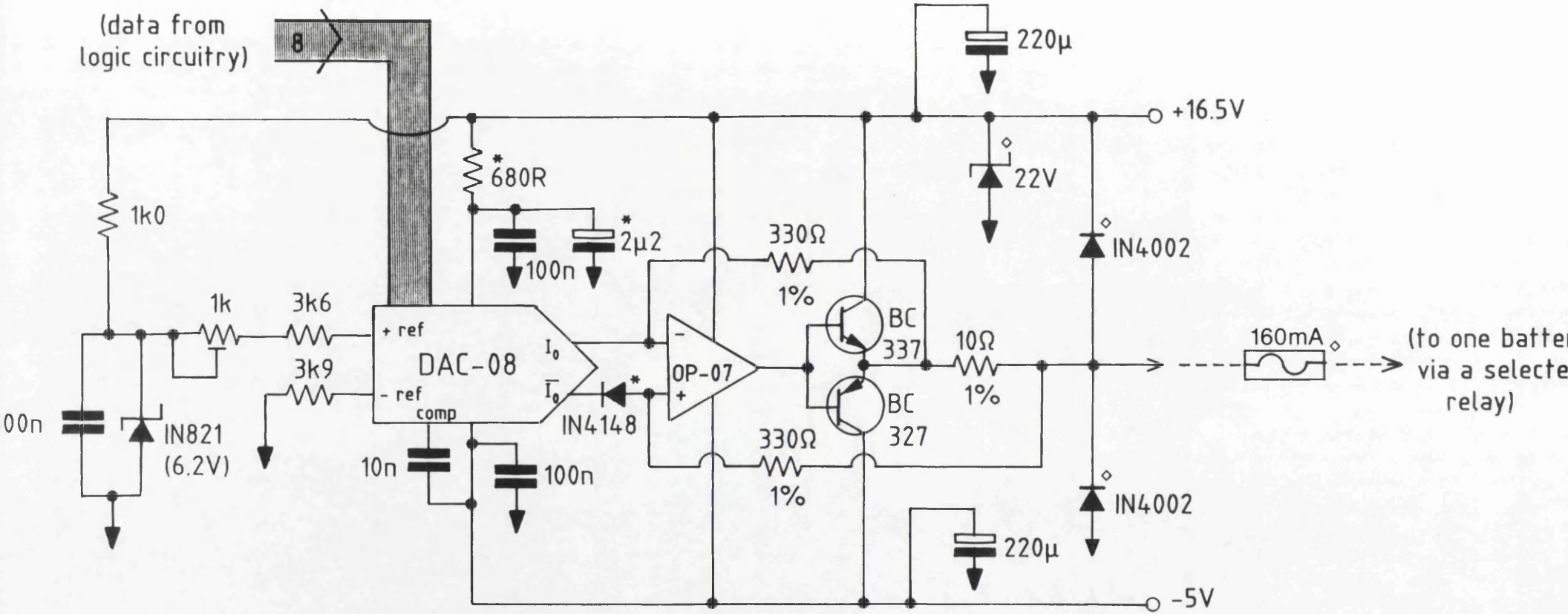


FIGURE 101(b) THE INTEGRATOR AND A-to-D STAGES OF THE J.P.B./U.C.S. CHARGER (RESPONSE-VOLTAGE) DETECTOR (certain parts only shown - refer to the ICL 7109 manufacturer's data sheet also)



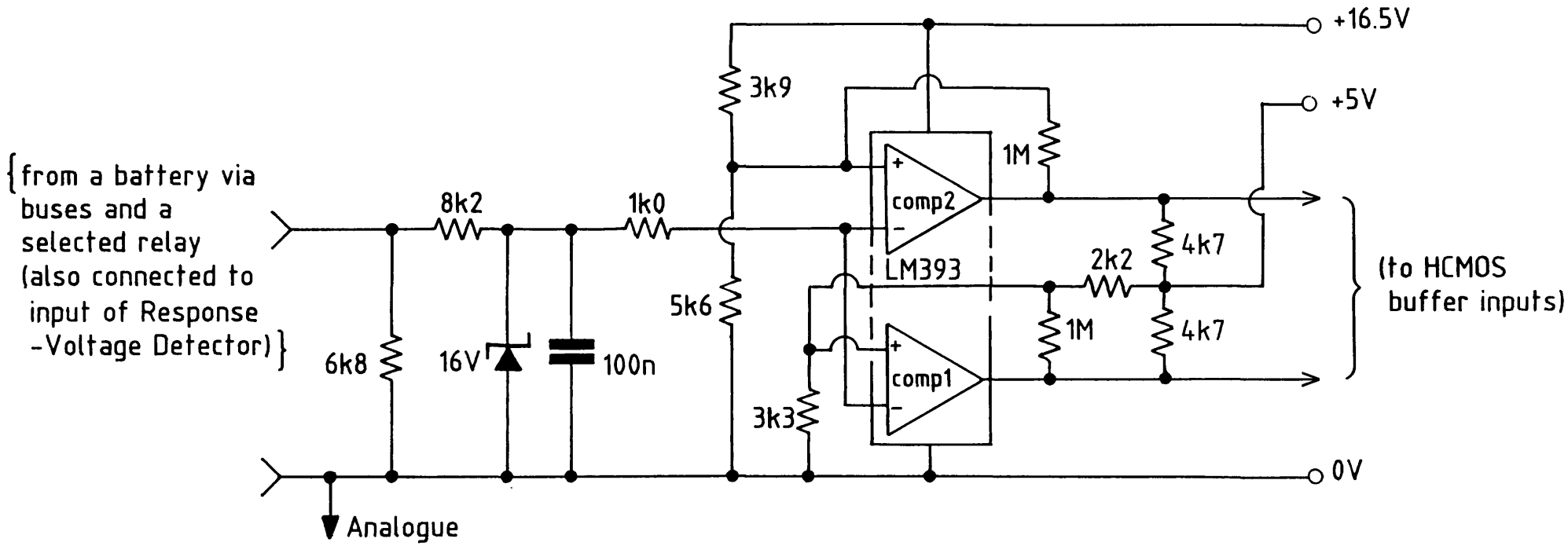
Notes :- All gates used in the prototype were LS types but HC types are preferable
All counters are asynchronous (ripple) types

FIGURE 102(a) THE J.P.B./U.C.S. CHARGER SINE GENERATOR LOGIC CIRCUITRY (BLOCK DIAGRAM)



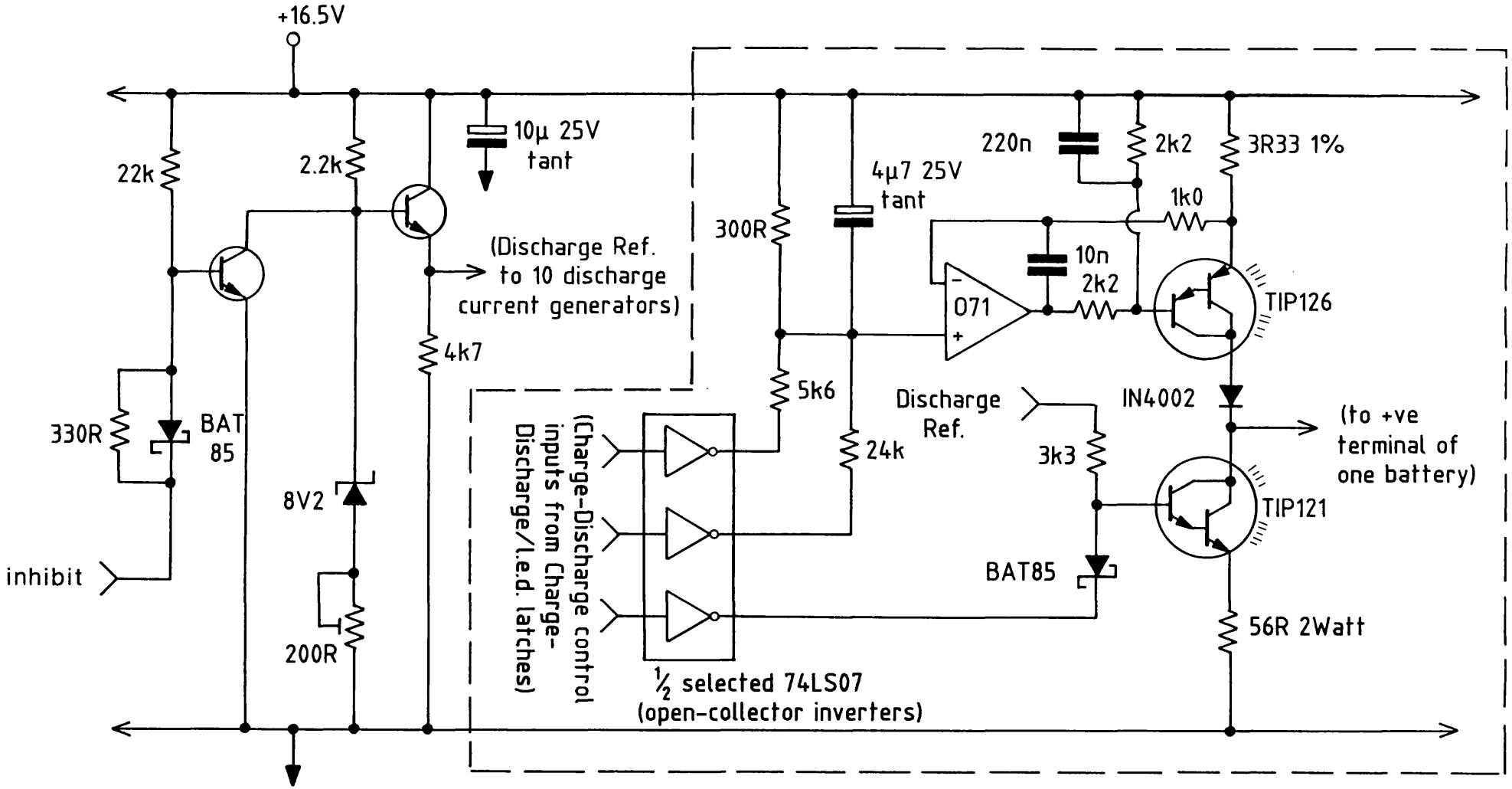
Notes :- Components marked * are for circuit protection in the event of -ve supply failure
Components marked ◇ are for protection against output overvoltages (fuse is on Relay Board)
All grounds are local analogue ground

FIGURE 102(b) THE J.P.B./U.C.S. CHARGER SINE GENERATOR ANALOGUE CIRCUITRY



Notes :- It should be remembered that the input capacitor and resistors of the Response-Voltage Detector are effectively in parallel with the input of this circuit
Supply decoupling capacitors and some non-essential components used in the prototype are omitted for clarity

FIGURE 103 THE J.P.B./U.C.S. CHARGER BATTERY VOLTAGE COMPARATORS



Notes :- The circuit enclosed in dotted lines is duplicated 10 times
The 74LS07 Buffers ought to be replaced with discrete transistor buffers
The ground shown is a local (power) ground
Output transistor pairs are on shared 11.5°C/Watt heatsinks

FIGURE 104 THE J.P.B./U.C.S. CHARGER CHARGE-DISCHARGE CIRCUITRY

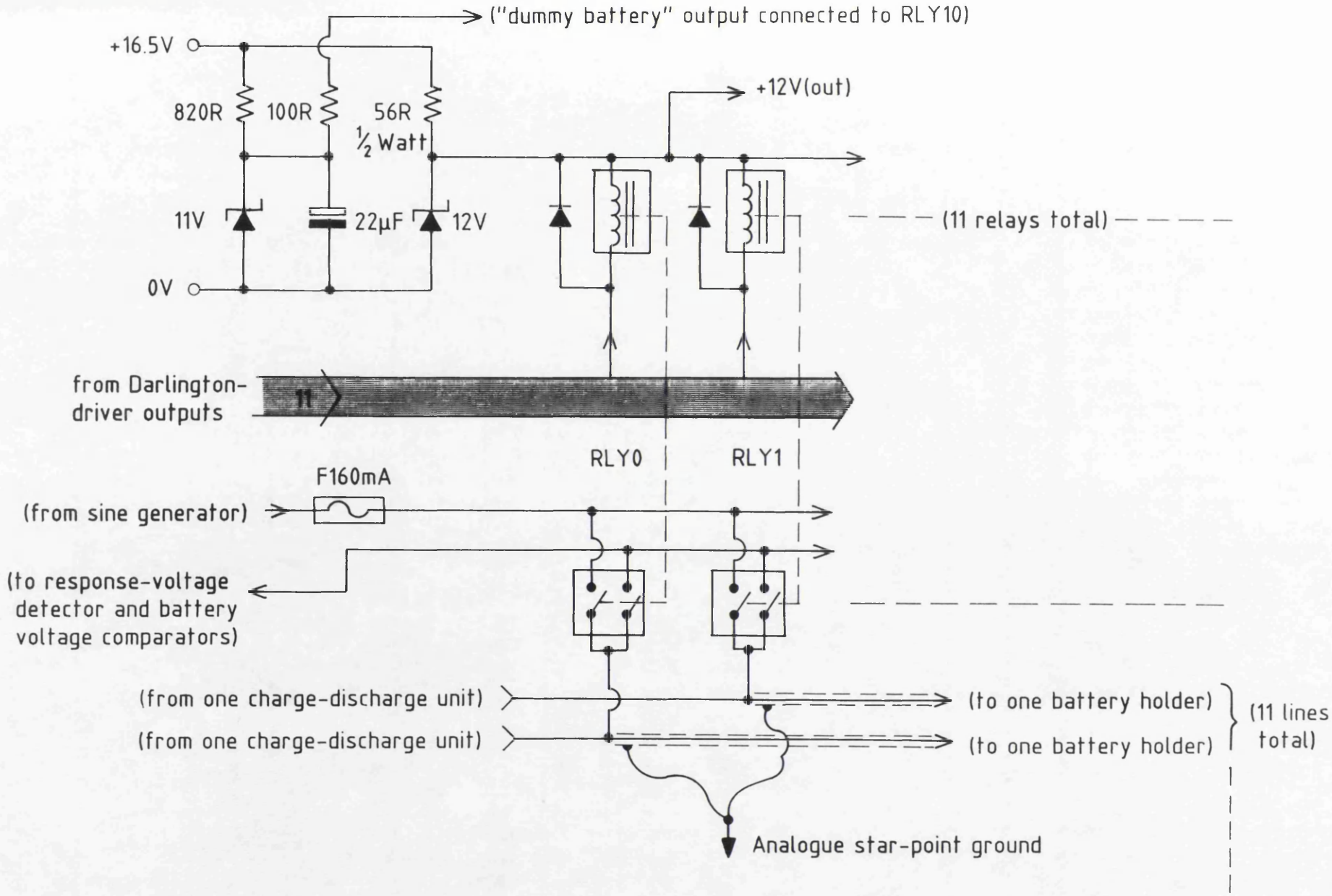


FIGURE 105 THE J.P.B./U.C.S. CHARGER RELAY BOARD

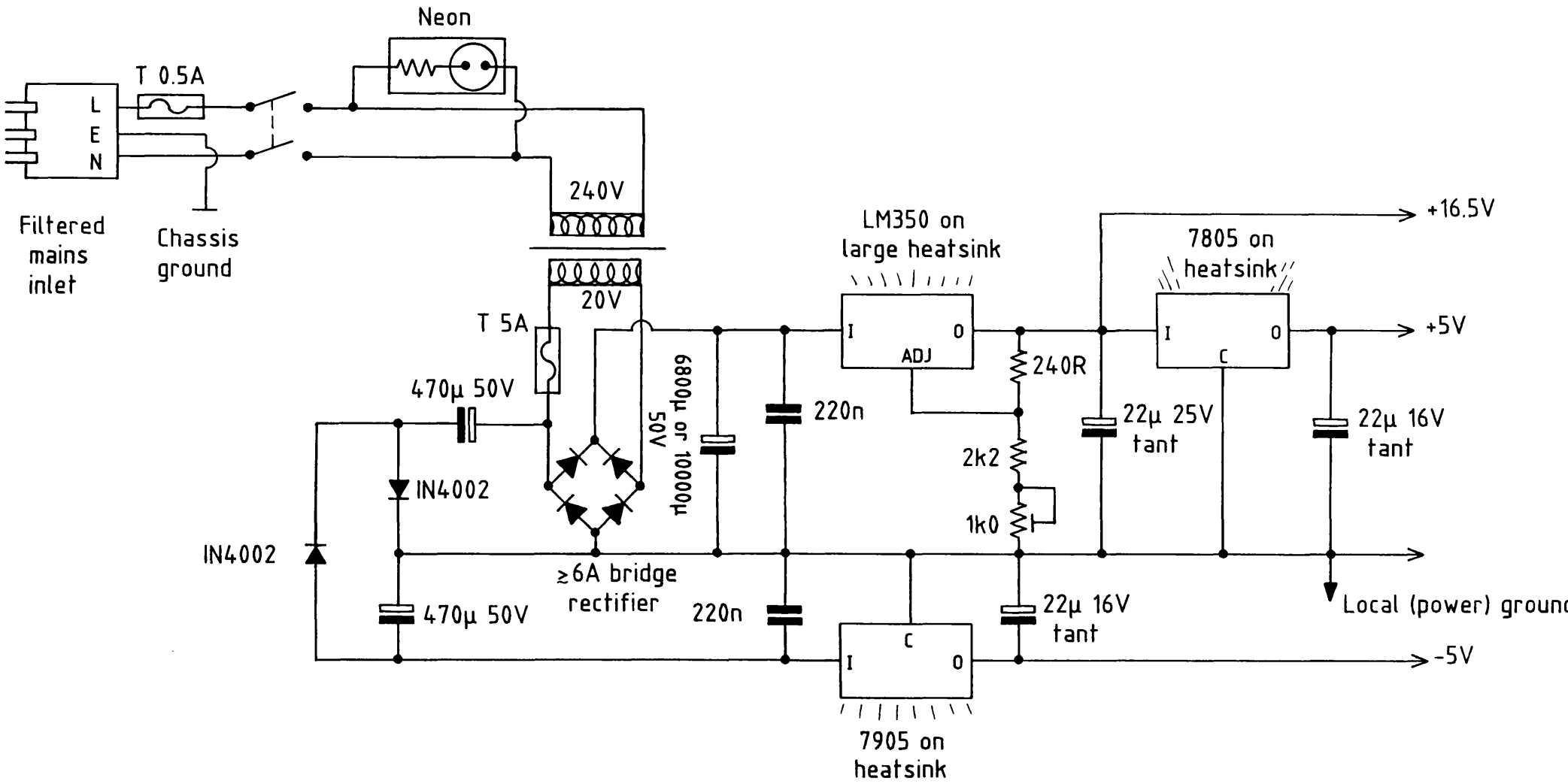
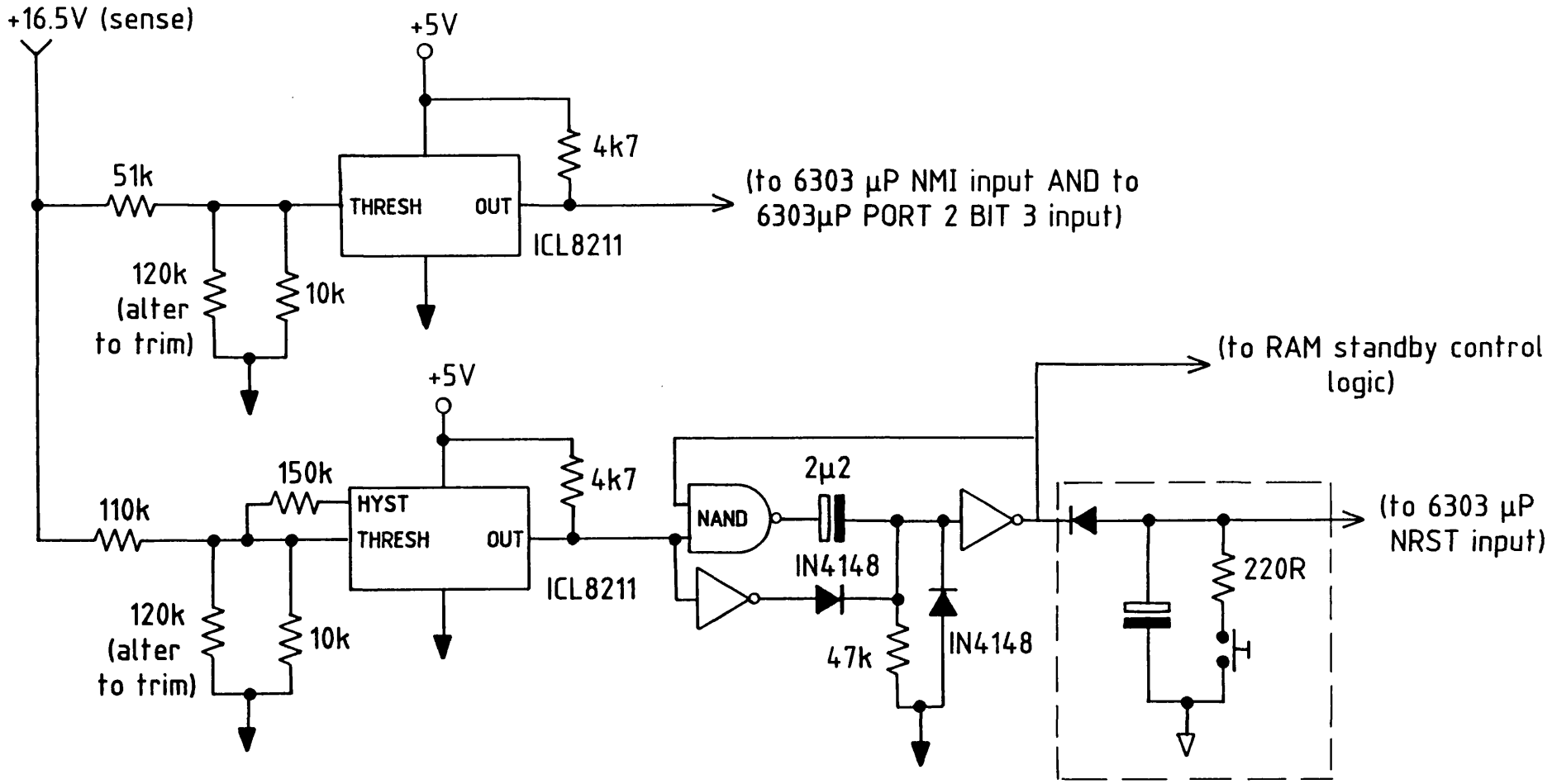
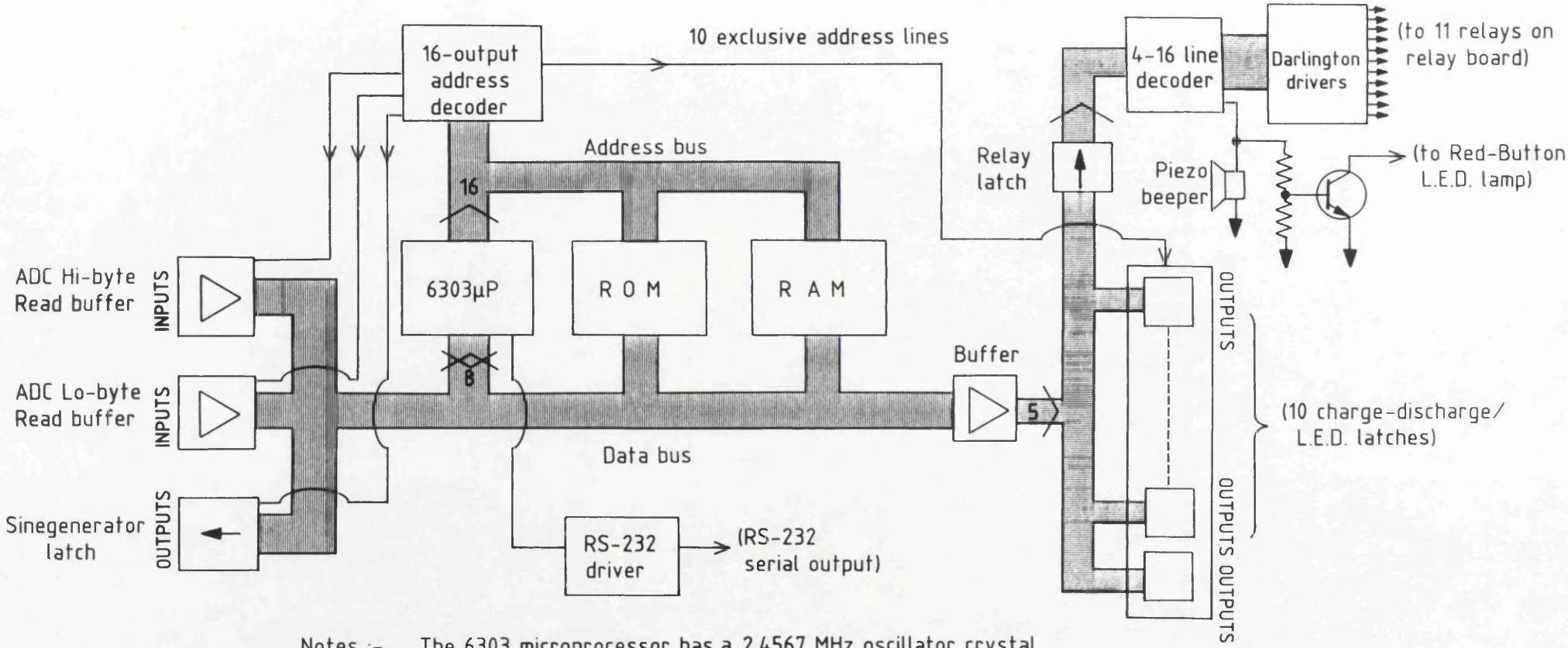


FIGURE 106 THE J.P.B./U.C.S. CHARGER POWER SUPPLY



Notes :- All logic gates are HCMOS types
The circuitry enclosed in dotted lines is optional and provides a processor reset function for test purposes only
Grounds are local (analogue/logic) ground

FIGURE 107 THE J.P.B./U.C.S. CHARGER POWERUP/POWERDOWN SENSOR



Notes :- The 6303 microprocessor has a 2.4567 MHz oscillator crystal
The databus and address bus buffering are perhaps inadequate
Many specific details including those of address decoding , logic line buffering , standard processor connections and logic decoupling are not decribed in these sheets
All logic gates in the control logic are HCMOS types
Grounds shown are local logic grounds

FIGURE 108 THE GENERAL ARCHITECTURE OF THE CONTROL LOGIC FOR THE J.P.B./U.C.S. CHARGER

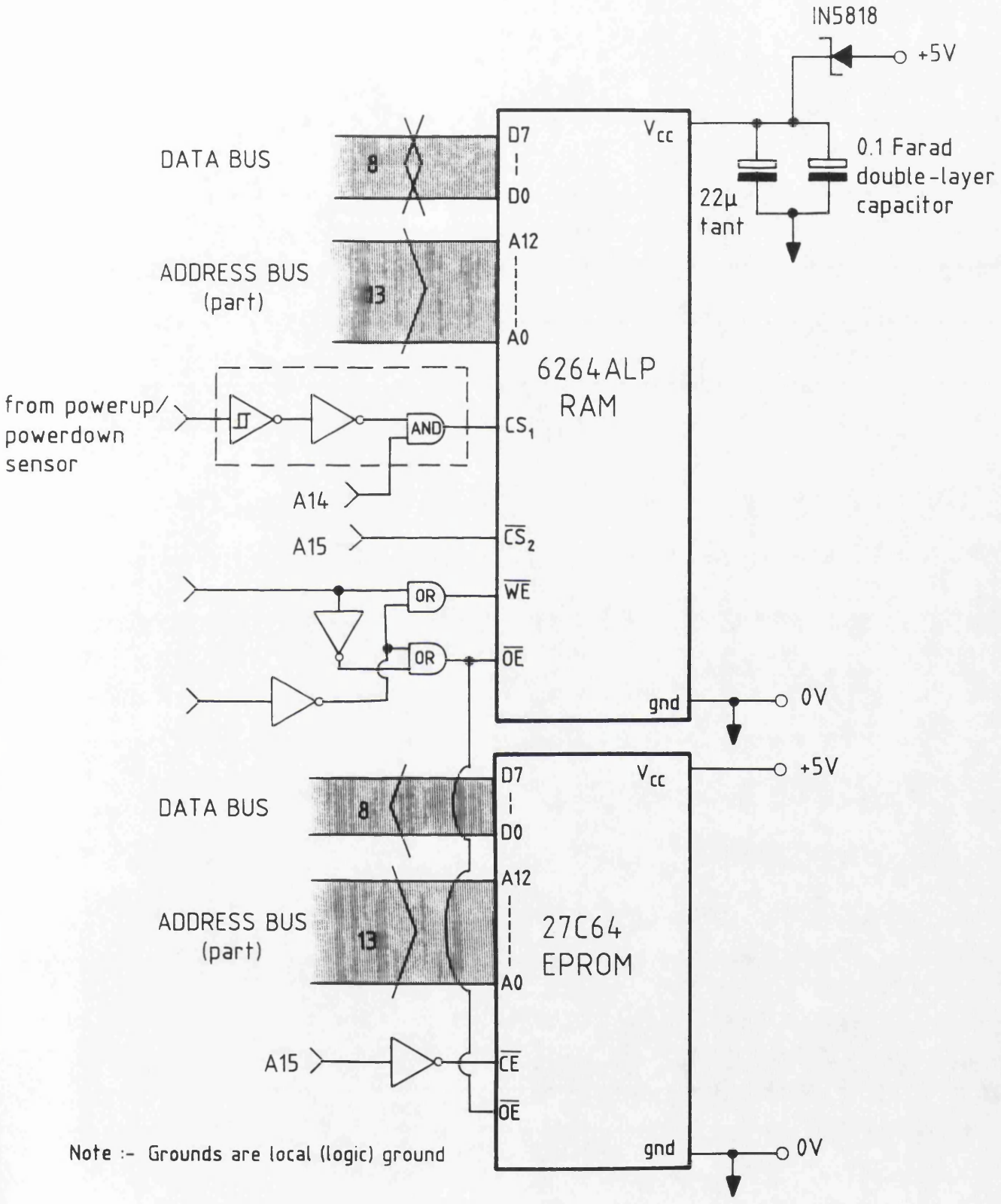
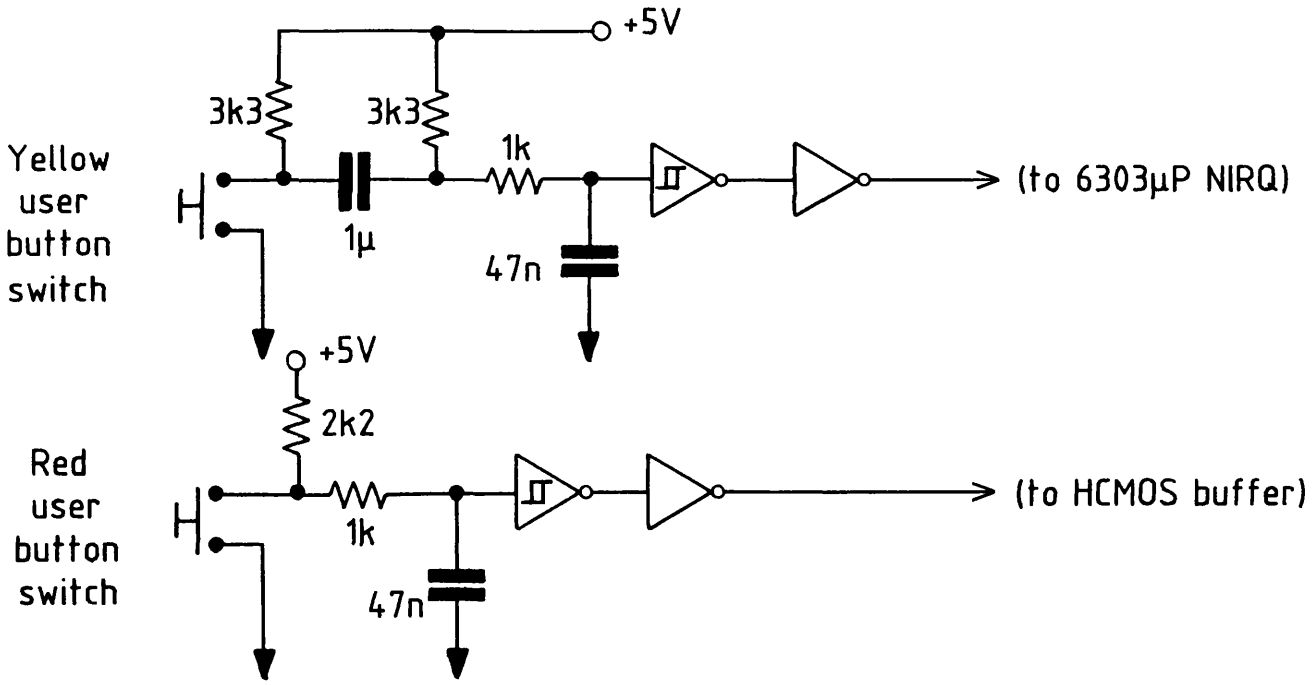


FIGURE 109(a) CONNECTIONS TO THE RAM AND ROM OF THE J.P.B./U.C.S. CHARGER - INCLUDING THE MEMORY BACKUP CIRCUITRY

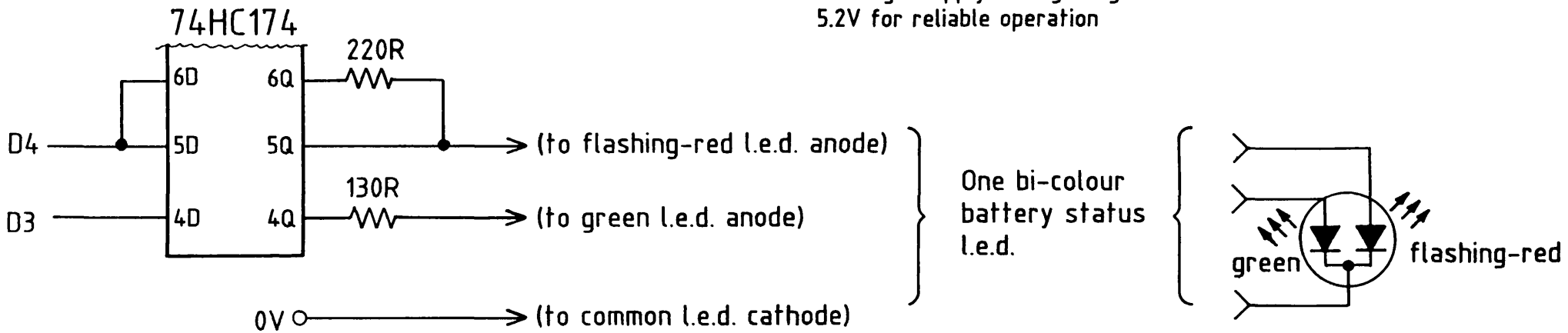


Note :- All logic gates are HCMOS types

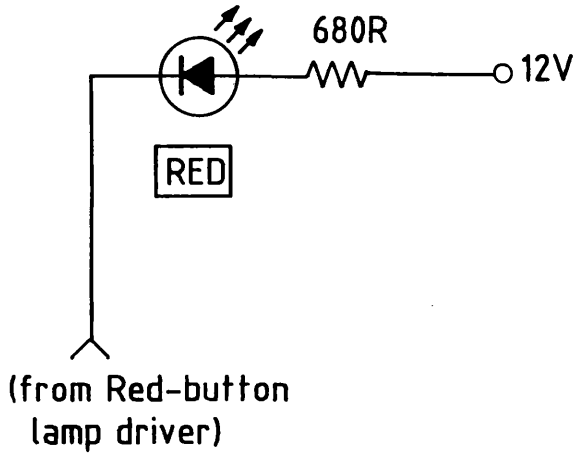
FIGURE 109(b) CIRCUITRY ASSOCIATED WITH THE J.P.B./U.C.S. CHARGER USER BUTTONS

Notes :- The l.e.d.'s ought to be driven from paralleled HCMOS buffer outputs rather than directly from latch outputs
The logic supply voltage ought to be at least 5.2V for reliable operation

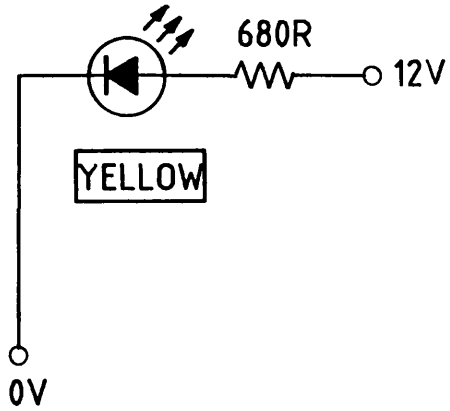
BATTERY STATUS l.e.d. (driver)



RED BUTTON ILLUMINATION



YELLOW BUTTON ILLUMINATION



BAD-BATTERY l.e.d. (driver)

This is a flashing-red l.e.d. which is driven from BIT7 of the Sinegenerator latch in a similar manner to flashing-red battery status lamps.

FIGURE 109(c) L.E.D. DRIVERS IN THE J.P.B./U.C.S. CHARGER

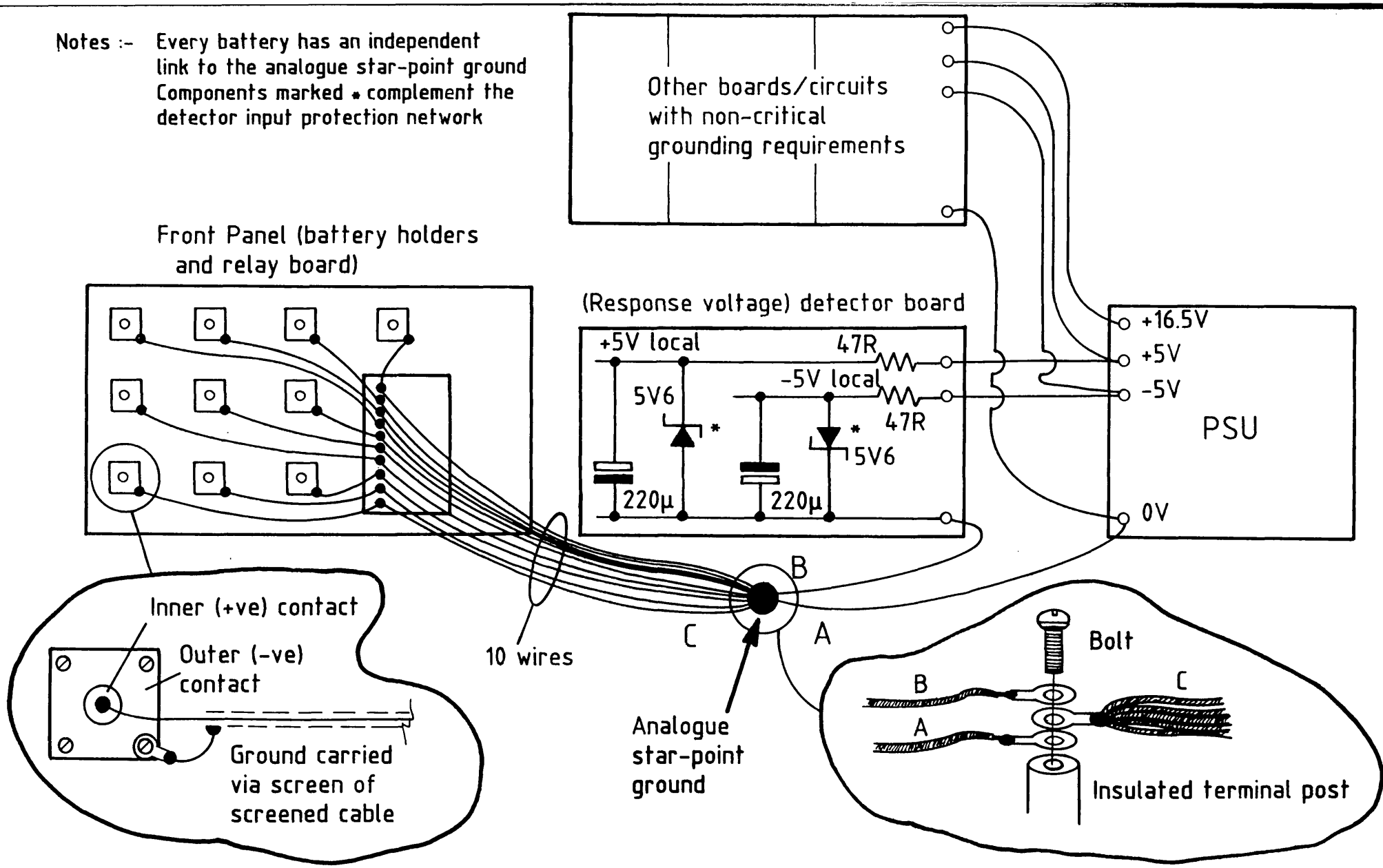


FIGURE 110 GROUND-LOOP PREVENTION METHODS USED WITHIN THE CHARGER

Fig. 111(a)

Measured True Capacities of 8 PYE P.F.X. Batteries used with the J.P.B./U.C.S. Charger

Battery Name	Measured Capacity (mAh)
P6PB5	684
P6PB6	735
P6PB7	664
P6PB9	654
P6PB10	716
P6PB11	658
P6PB12	665
P6PB13	688

Notes:-

- The batteries are all nominally 600mAh types.
- Battery true capacities were measured at the C/5 discharge rate after a standard C/10-rate charge using the research cell/battery test rig. This procedure was called "RUN1000".
- Batteries were subjected to two standard conditioning cycles prior to RUN1000.

Fig. 111(b)

Measures of Charging Effectiveness for 8 PYE P.F.X. Batteries in J.P.B./U.C.S. Charger-RUN 6

Battery name	% of nominal capacity charged	% of true capacity charged	% charge efficiency
P6PB5	107	94	84
P6PB6	116[a]	95[a]	83
P6PB7	105	94	81
P6PB9[b]	---	--	--
P6PB10	112	94	82
P6PB11	105	96	85
P6PB12	104	94	81
P6PB13	109	95	80
Average	107[c]	94.5[c]	82.3

Notes:-

- Batteries were charged in the J.P.B./U.C.S. charger with the Fast-Charge phase operational and the Top-up phase disabled.

- Battery charged capacities were measured at the C/5 discharge rate using the research cell/battery test rig.

Note[a] - Battery P6PB6 was charged for 4.083 hours which is 5 minutes longer than the 4-hour Fast-Charge timeout period set finally for the J.P.B./U.C.S. charger. Hence the capacity-charged figures may be regarded for purposes of charger evaluation as being slightly too high.

Note[b] - Results for this battery were spoilt by error.

Note[c] - These averages do not include battery P6PB6.

Fig. 111(c)

Measures of Charging Effectiveness for 8 PYE P.F.X. Batteries in J.P.B./U.C.S. Charger-RUN 7

Battery name	% of nominal capacity charged	% of true capacity charged	% charge efficiency
P6PB5	104	91	86
P6PB6	114	93	86
P6PB7	103	93	83
P6PB9	100	90	86
P6PB10	110	92	85
P6PB11	102	93	84
P6PB12	103	93	83
P6PB13	106	93	82
Average	105.3	92.3	84.4

Notes:-

- Batteries were charged in the J.P.B./U.C.S. charger with the Fast-Charge phase operational and the Top-up phase disabled.
- Battery charged capacities were measured at the C/5 discharge rate using the research cell/battery test rig.

INDEX TO GRAPHS AND GENERAL NOTES ON GRAPHS

Research Test Rig Results - Graphs 1(a)-13(i)

Graphs 1(a,b,c,d,e,f,g,h,i,j,k) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. for 500mAh "AA" Japanese-SAFT cell "S4" and 500mAh "AA" regular SAFT cell "S6" for system RUNs 6 and 8. Measurement frequencies used were 32, 16, 8, 4, 2Hz. Charge rates used were C/10 and discharge rates were -C/5.

Graphs 2(a,b,c,d,e,f) - Graphs of d.c. terminal voltage, E.S.C., E.S.Con. and (E.S.C.)*(E.S.Con) for 500mAh "AA" Japanese-SAFT cell "S2" and 500mAh "AA" regular SAFT cell "S5" for system RUN11. Measurement frequencies used were 32, 16, 8, 4, 2, 1Hz. Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 3(a,b,c,d,e,f,g,h) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. for 500mAh "AA" Japanese-SAFT cell "S4" and 500mAh "AA" regular SAFT cell "S5" for system RUN14. Measurement frequencies used were 32, 16, 8, 4, 2, 1Hz. Charge rates used were C/10 and discharge rates were -C/5.

Graphs 4(a,b,c,d,e,f,g,h,i,j,k,l,m,n) - Graphs of d.c. terminal voltage, E.S.C.(+ve bias), E.S.C.(zero bias), E.S.C.(-ve bias), E.S.Con.(+ve bias), E.S.Con.(zero bias), E.S.C.(-ve bias) for 500mAh "AA" Japanese-SAFT cell "S4" and 500mAh "AA" regular SAFT cell "S5" for system RUN18. The single measurement frequency used was 2Hz. Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 5(a,b,c,d,e,f,g,h,i,j,k,l,m,n,o,p) - Graphs of d.c. terminal

voltage, E.S.C.(+ve bias), E.S.C.(zero bias), E.S.C.(-ve bias), E.S.Con.(+ve bias), E.S.Con.(zero bias), E.S.Con.(-ve bias), for 500mAh "AA" Japanese-SAFT cell "S10" and 7Ah "F" SAFT cell "SF1" for system RUN108. Measurement frequencies used were 8Hz and 2Hz with two polarities of sinewave excitation. Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 6(a,b,c,d,e,f,g,h,i,j,k,l,m,n,o,p,q,r,s,t,u) - Graphs of d.c. terminal voltage and E.S.C.(zero bias) for 4 "AA" Japanese-SAFT cells "S8","S9","S10","S11" and 3 "AA" regular SAFT cells "S5","S6","S7" for system RUN200. Measurement frequencies used were 8Hz and 2Hz with two polarities of sinewave excitation. Charge rates used were C/5 and discharge rates were -C/5. At different times for each cell a short discharge period was included within the charging phase and a short charge period was included within the discharge phase.

Graphs 7(a,b,c,d,e,f,g,h,i) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. for system RUN315 for 500mAh "AA" Japanese-SAFT cell "S13" and two 500mAh "AA" cells (SAFT) "PP7","PP13" extracted from used PYE P.F.X. batteries. Measurement frequencies were 64, 32, 2Hz. Charge rates used were C/5 and discharge rates were -C/2.5. At the end of the charging phase a short discharge was done followed by a recharge.

Graphs 8(a,b,c,d,e,f,g,h,i,j,k,l,m,n,o,p,q,r,s,t,u,v,w,x,y,z, aa,bb,cc,dd,ee,ff,gg) - Graphs of d.c. terminal voltage and E.S.C. for 11 size-"AA" cells of differing types for system RUN400. Measurement frequencies used were 32Hz and 2Hz. Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 9(a,b,c,d,e,f,g,h,i,j,k,l,m,n,o,p) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. (4 cells only) for 6 cells of differing types and sizes for system RUN500. Measurement frequencies used were 32Hz and 2Hz. Charge rates used were C/5 and discharge rates were -C/2.5

Graphs 10(a,b,c,d,e,f) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. for 2 PYE P.F.X. 8-cell batteries for system RUN601. Measurement frequencies used were 64, 32, 2Hz. Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 11(a,b,c,d,e,f,g,h,i,j,k,l,m,n) - Graphs of d.c. terminal voltage (RUN605 only), "Second-Harmonic-Transcapacitance" and "Second-Harmonic-Transconductance" for 2 PYE P.F.X. 8-cell batteries using measurement frequencies 8Hz (RUN605), 4Hz (RUN606), 2Hz (RUN610). Charge rates used were C/5 and discharge rates were -C/2.5.

Graphs 12(a,b) - Graphs Demonstrating Features and Thresholds Associated with Possible End-of-Charge Algorithms for Cells of SAFT manufacture.

Graphs 13(a,b,c,d,e,f,g,h,i) - Graphs of d.c. terminal voltage, E.S.C. and E.S.Con. for 3 Motorola NTN5048A batteries for system RUN806. Measurement frequencies used were 16, 8, 4, 2, 1, 0.5Hz. Charge rates used were C/5 and discharge rates were -C/2.5.

Notes on Graphs 1(a)-13(i)

- The x axes (parallel with the document spine) represent time and are marked in minutes.
- The x axes are generally linear only in a piecewise manner but time

annotation is always accurate.

- The interval in the x direction between any two successive plotted points is always 10 minutes.
- For some graphs which display results involving two or more measurements at same measurement frequency the resulting multiple curves may be largely indistinguishable.
- Where multiple curves are plotted for multiple measurement frequencies the order of the curves is shown at the top of the page as "XXHz >>> YYHz" where ">>>" indicates direction up the (+ve) y axis. For nearly all multiple-frequency plots the curves are clearly separated and in a fixed order.

J.P.B./U.C.S. Charger Results - Graphs 101(a)-103

Graphs 101(a,b,c,d) - Graphs of 2Hz E.S.C. for 8 PYE P.F.X. batteries as determined by the J.P.B./U.C.S. charger during charge in Charger-RUN3 (at the C/2.5 rate). Included on Graph 101(a) are features relevant to discussion of E.S.C. profiles and a charging/end-of-charge algorithm.

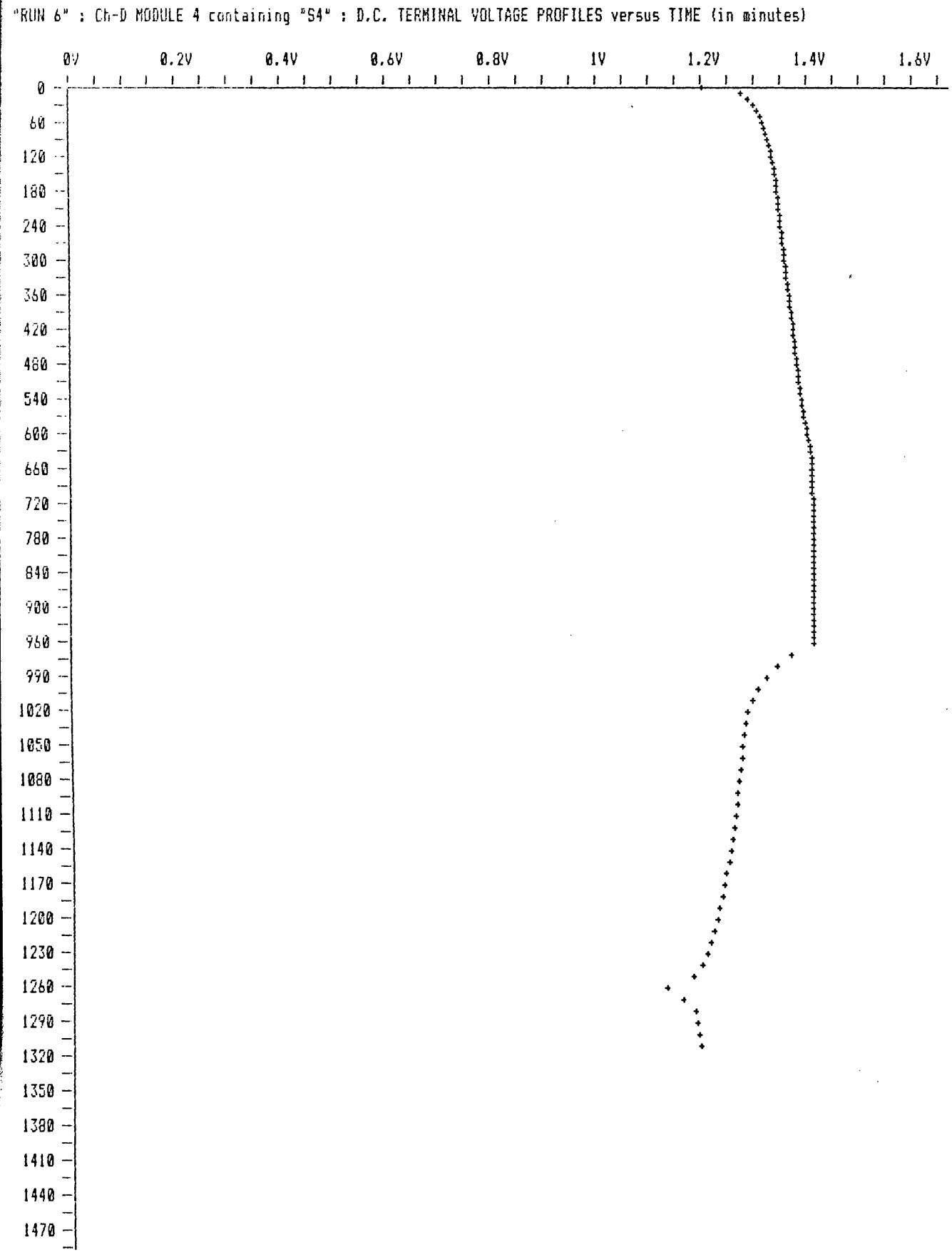
Graphs 102(a,b,c,d,e) - Graphs of 2Hz E.S.C. for PYE P.F.X. batteries as determined by the J.P.B./U.C.S. charger during charge with a charge/end-of-charge algorithm operational in Charger-RUN5 and Charger-RUN6.

Graph 103 - A Graph of an amomalous 2Hz E.S.C. response from a damaged battery as determined by the J.P.B./U.C.S. charger during charge in Charger-RUN3.

Notes on Graphs 101(a)-103

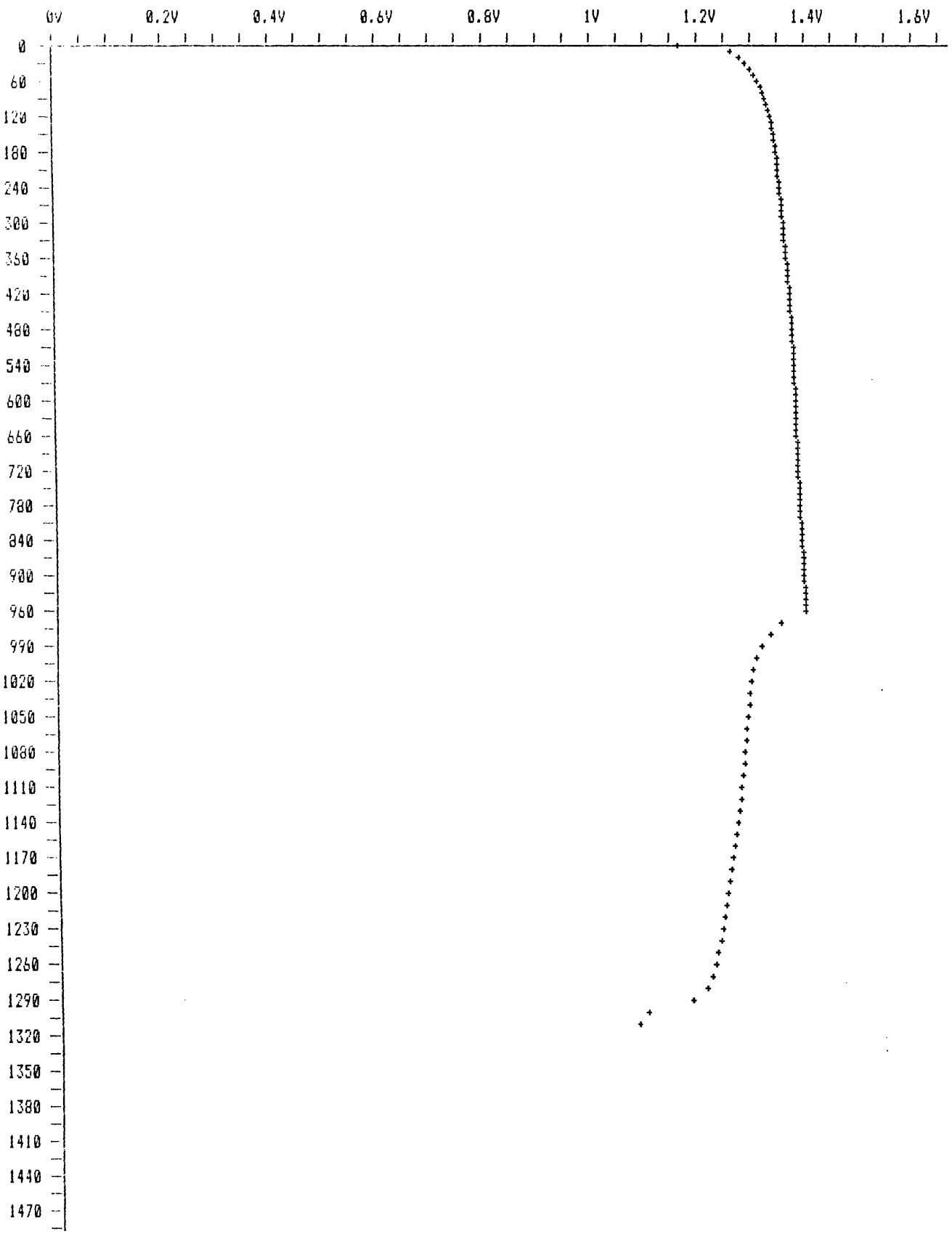
- The x axes (parallel with the bottom of the page) represent time and are marked in hours.
- The y axes represent 2Hz Effective Series Capacitance and are uncalibrated but constant amongst graphs.
- Charger socket "0" contains battery "P6PB5", socket "1" contains "P6PB6", socket "2" contains "P6PB7", socket "3" contains "P6PB9", socket "4" contains "P6PB10", socket "5" contains "P6PB11", socket "6" contains "P6PB12" and socket "7" contains "P6PB13".
- Graph 101(a) includes features relevant to discussions of E.S.C. profiles and charge/end-of-charge algorithms.
- Graphs 102(a,b,c,d,e) are for RUNs in which an end-of-charge algorithm was operational. The extreme end of each plotted E.S.C. curve indicates the point at which charging was terminated for the associated battery.
- Graphs 102(a,b,c,d,e) show the positions of the two E.S.C. thresholds involved in the operational end-of-charge algorithm.

Graph 1(a)


"RUN 6" : Ch-D MODULE 4 containing "S4" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
990
1020
1050
1080
1110
1140
1170
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 1(b)

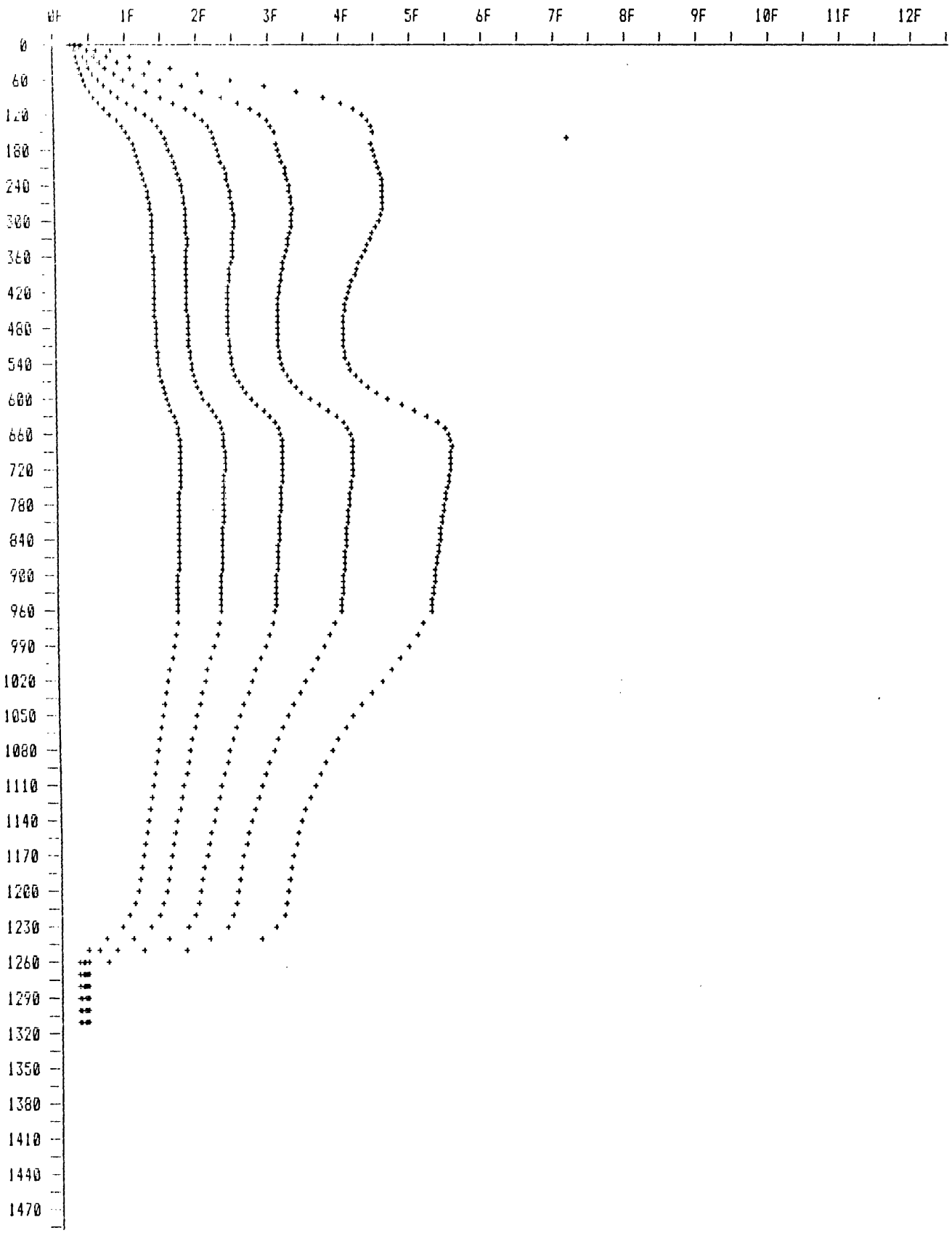
"RUN 6" : Ch-D MODULE 6 containing "S6" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 1(8)

Note: Curve order is 32Hz >>> 2Hz

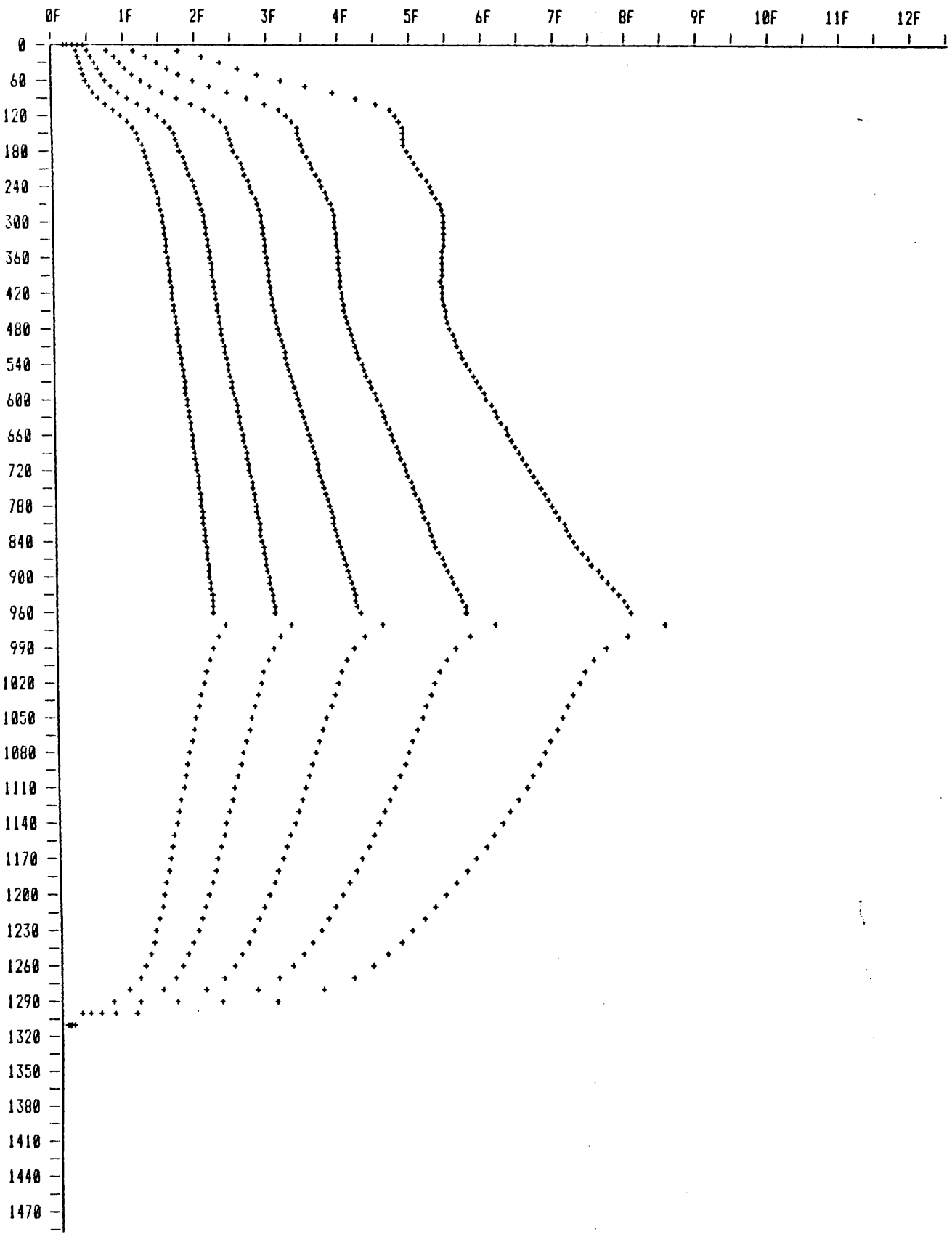
"RUN 6" : Ch-D MODULE 4 containing "S4" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2Hz



Graph 1(d)

Note: Curve order is 32Hz >>> 2Hz

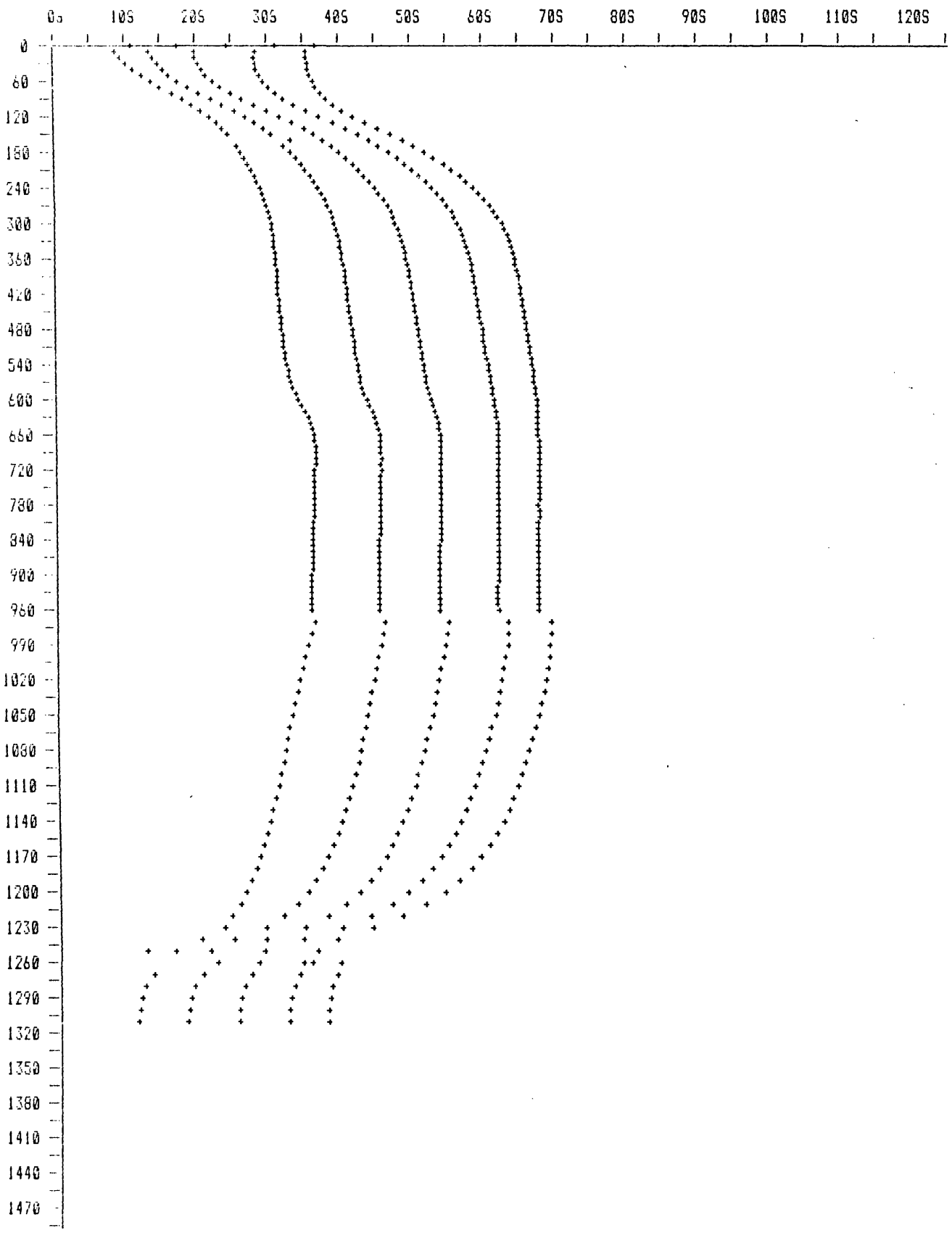
"RUN 6" : Ch-D MODULE 6 containing "S6" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2Hz



Graph 1(8)

Note: Curve order is 2Hz >>> 32Hz

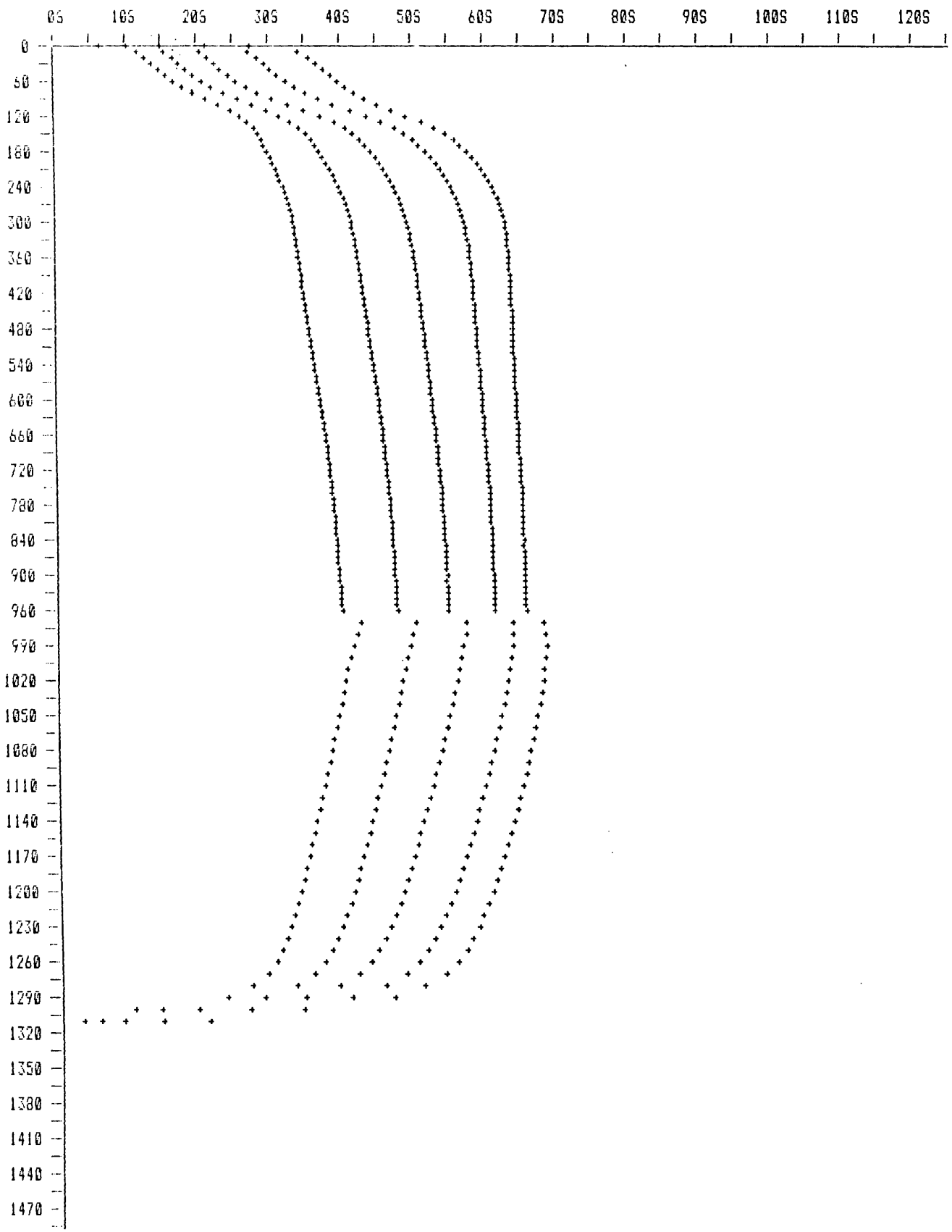
RUN 6" : Ch-D MODULE 4 containing "S4" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2Hz



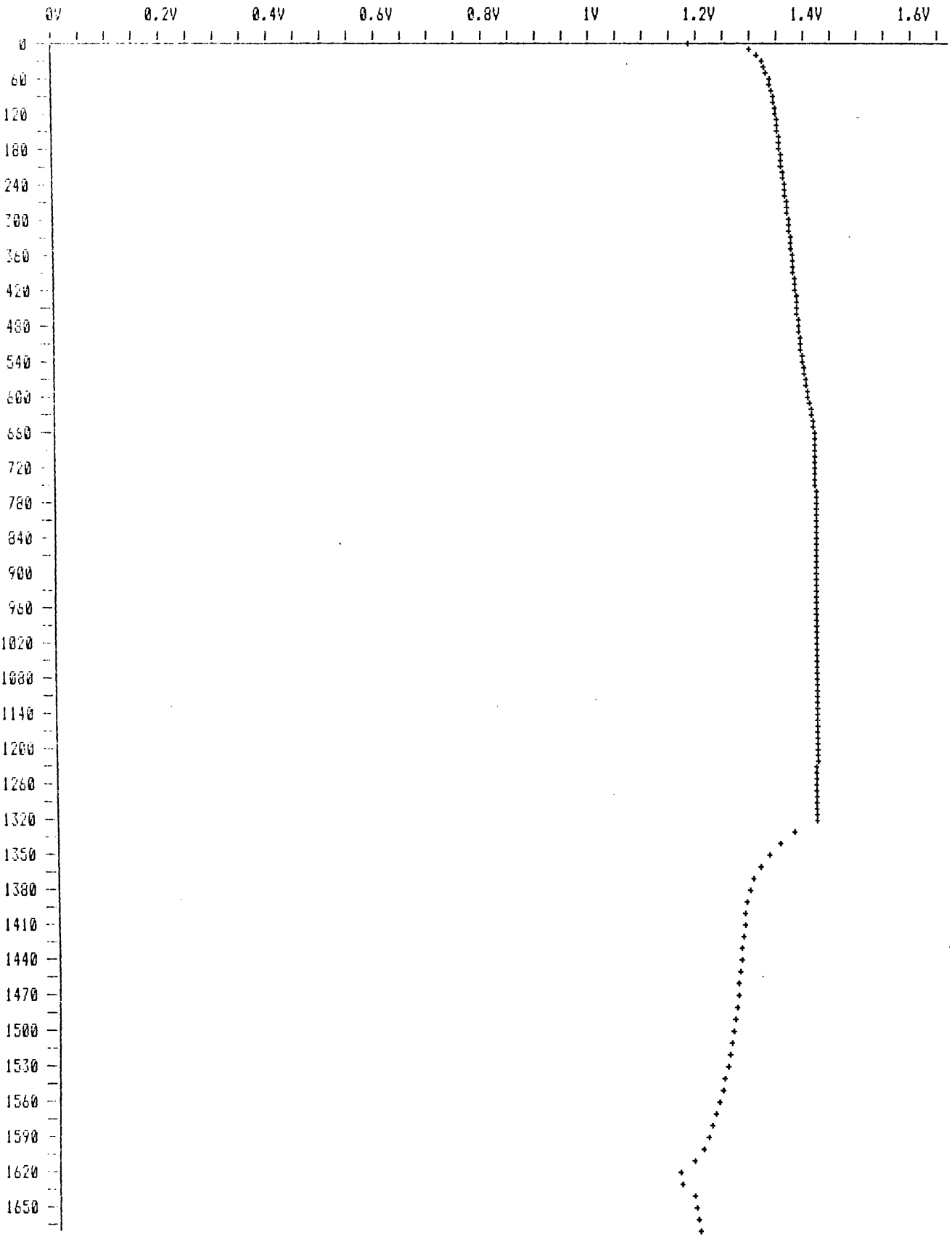
Graph 1(1)

Note: Curve order is 2Hz >>> 32Hz

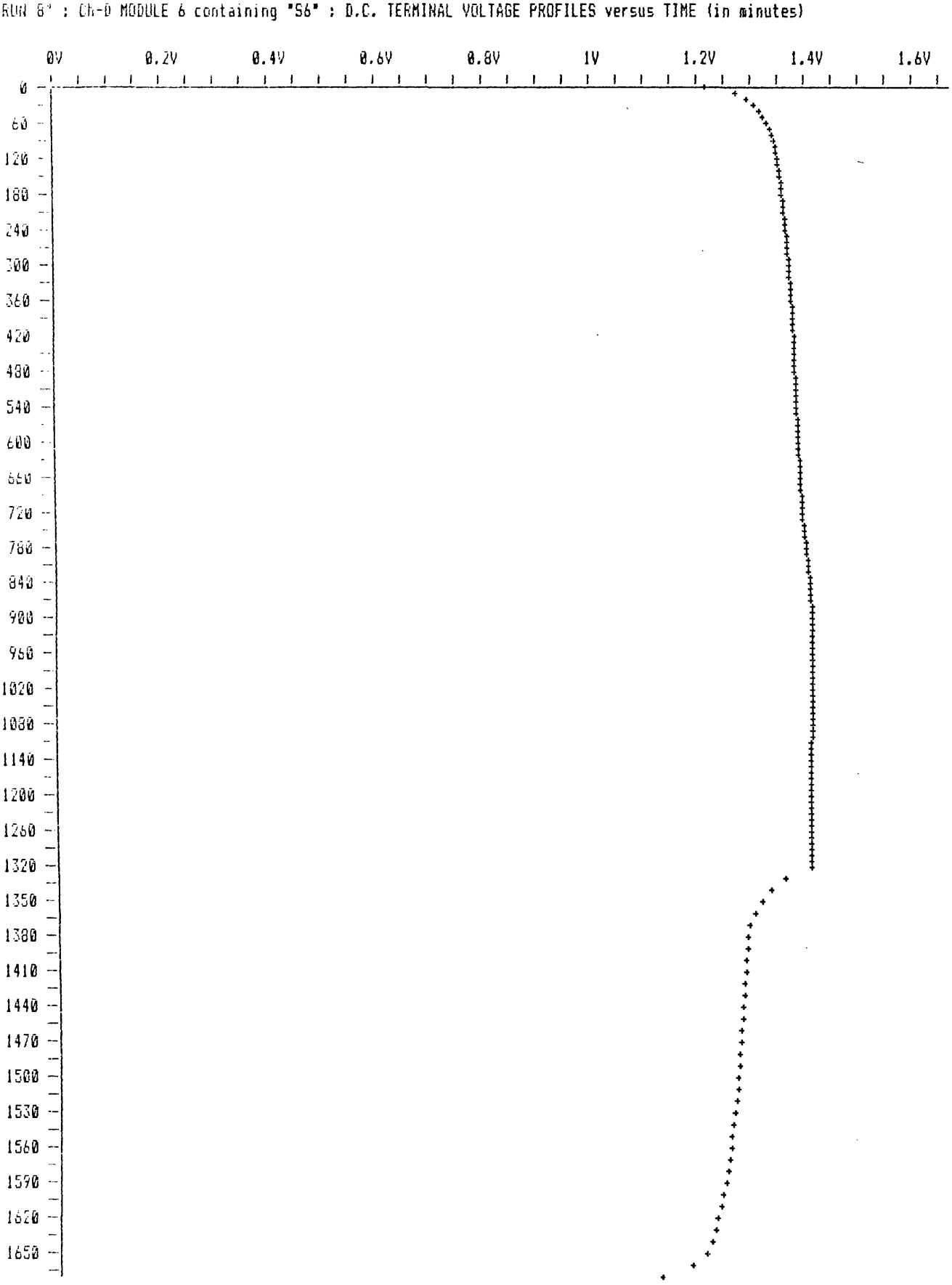
"RUN 6" : CH-B MODULE 6 containing "S6" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2Hz



"RUN 8" : Ch-D MODULE 4 containing "S4" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



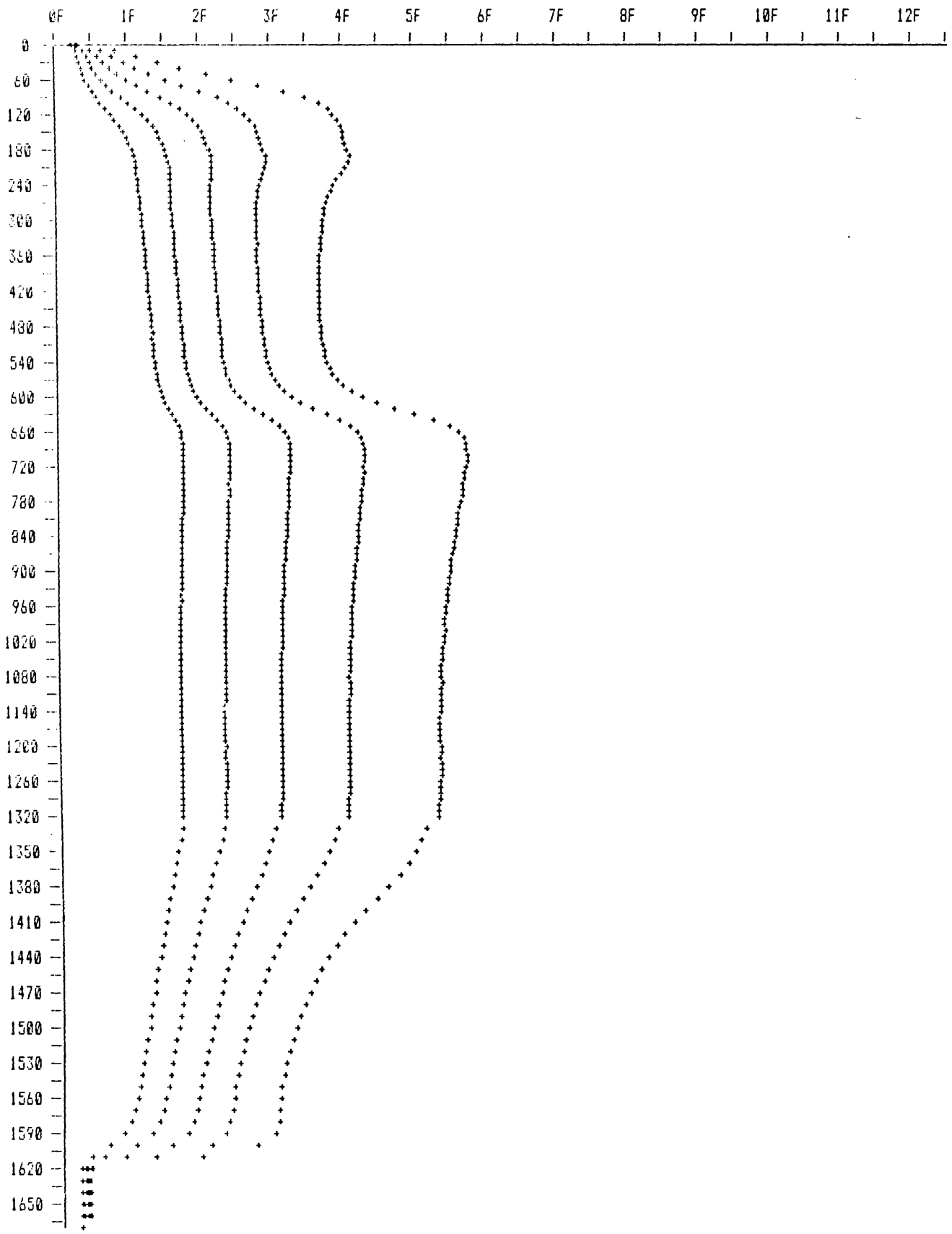
Graph 4(ii)


"RUN 8" : Ch-D MODULE 6 containing "S6" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200
1260
1320
1350
1380
1410
1440
1470
1500
1530
1560
1590
1620
1650

Graph 1(i)

Note: Curve order is 32Hz >>> 2Hz

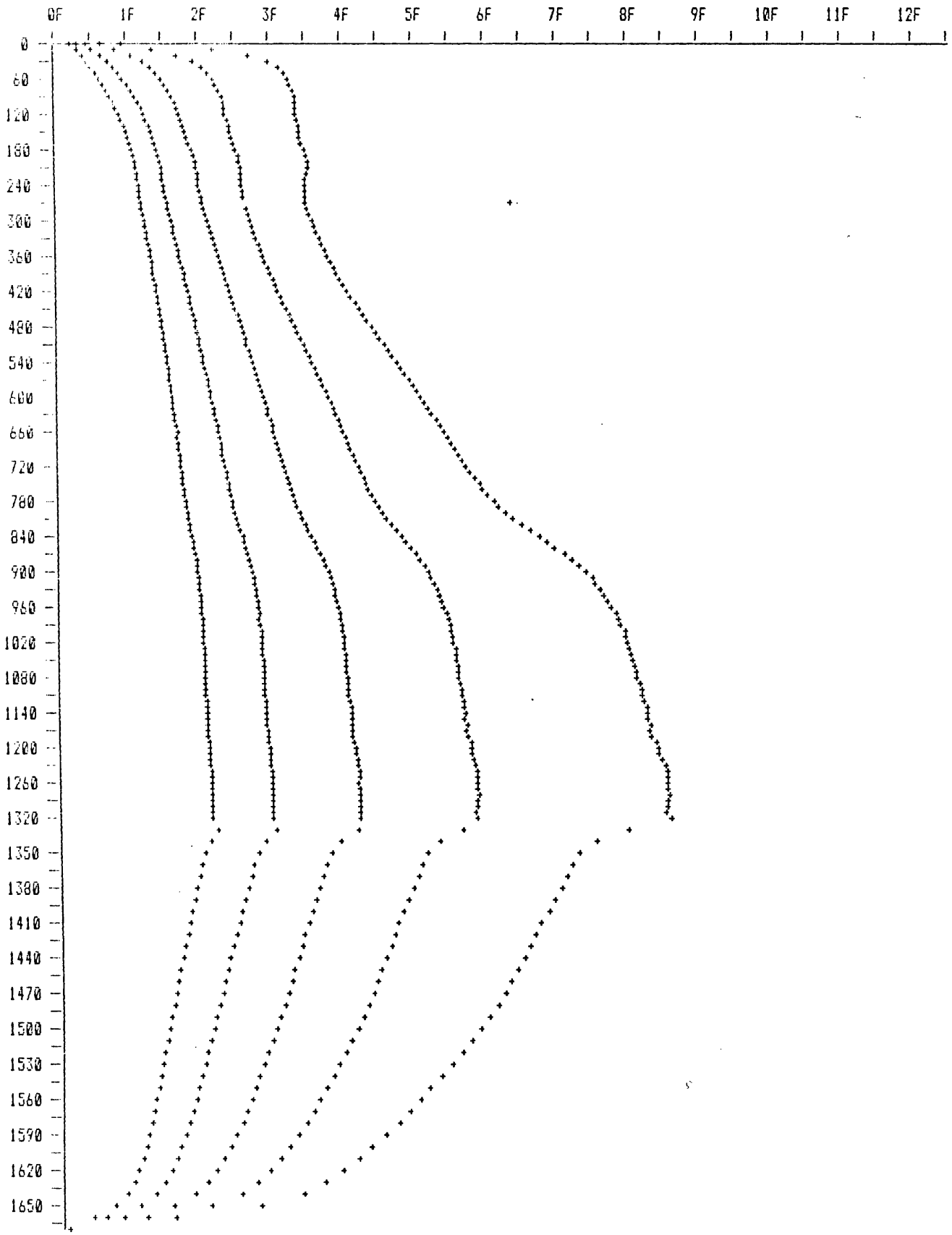
"RUN 8" : Ch-D MODULE 4 containing "S4" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2Hz



Graph 1(j)

Note: Curve order is 32Hz >>> 2Hz

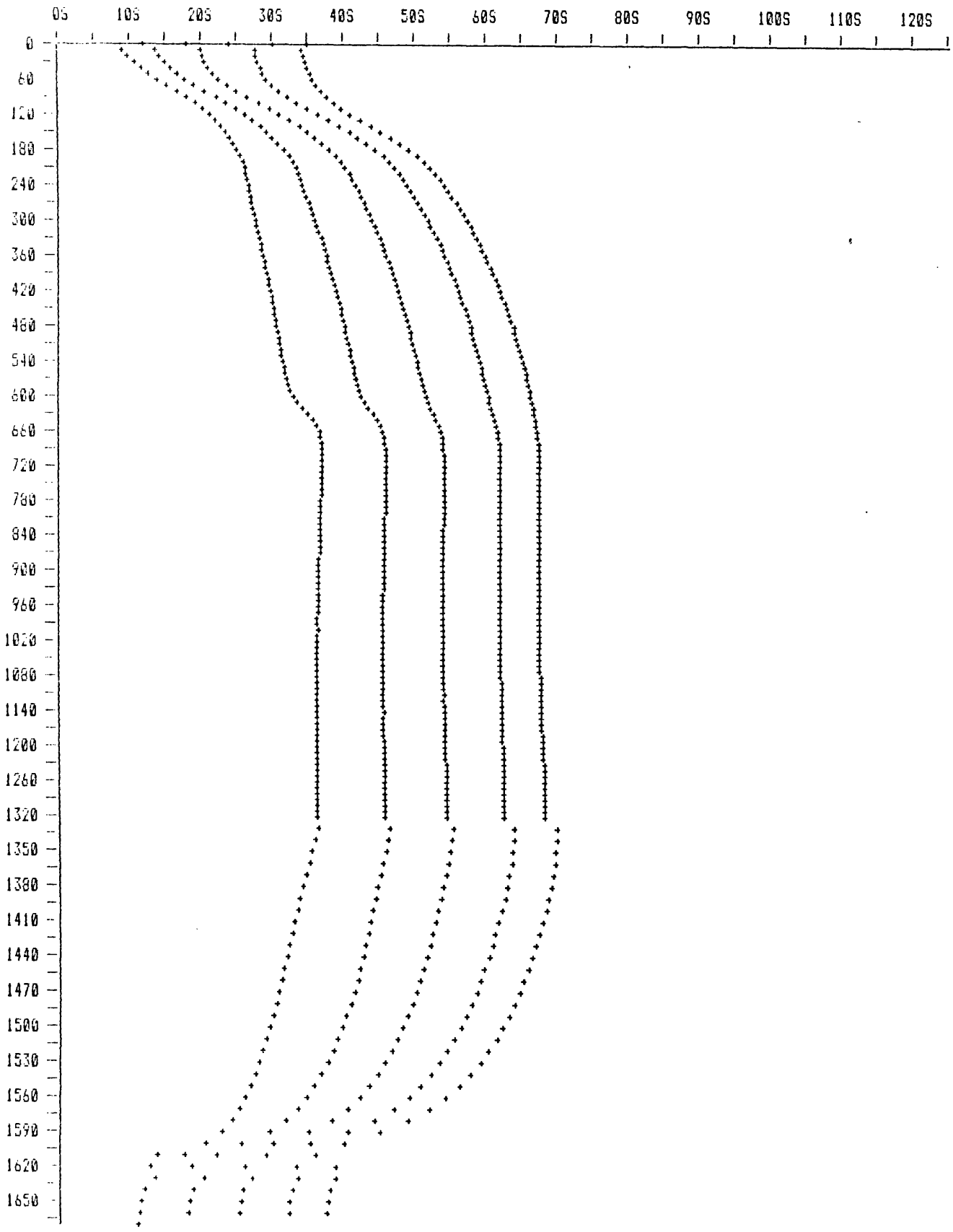
"RUN 8" : Ch-D MODULE 6 containing "S6" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2Hz



Graph 1(a)

Note: Curve order is 2Hz >>> 32Hz

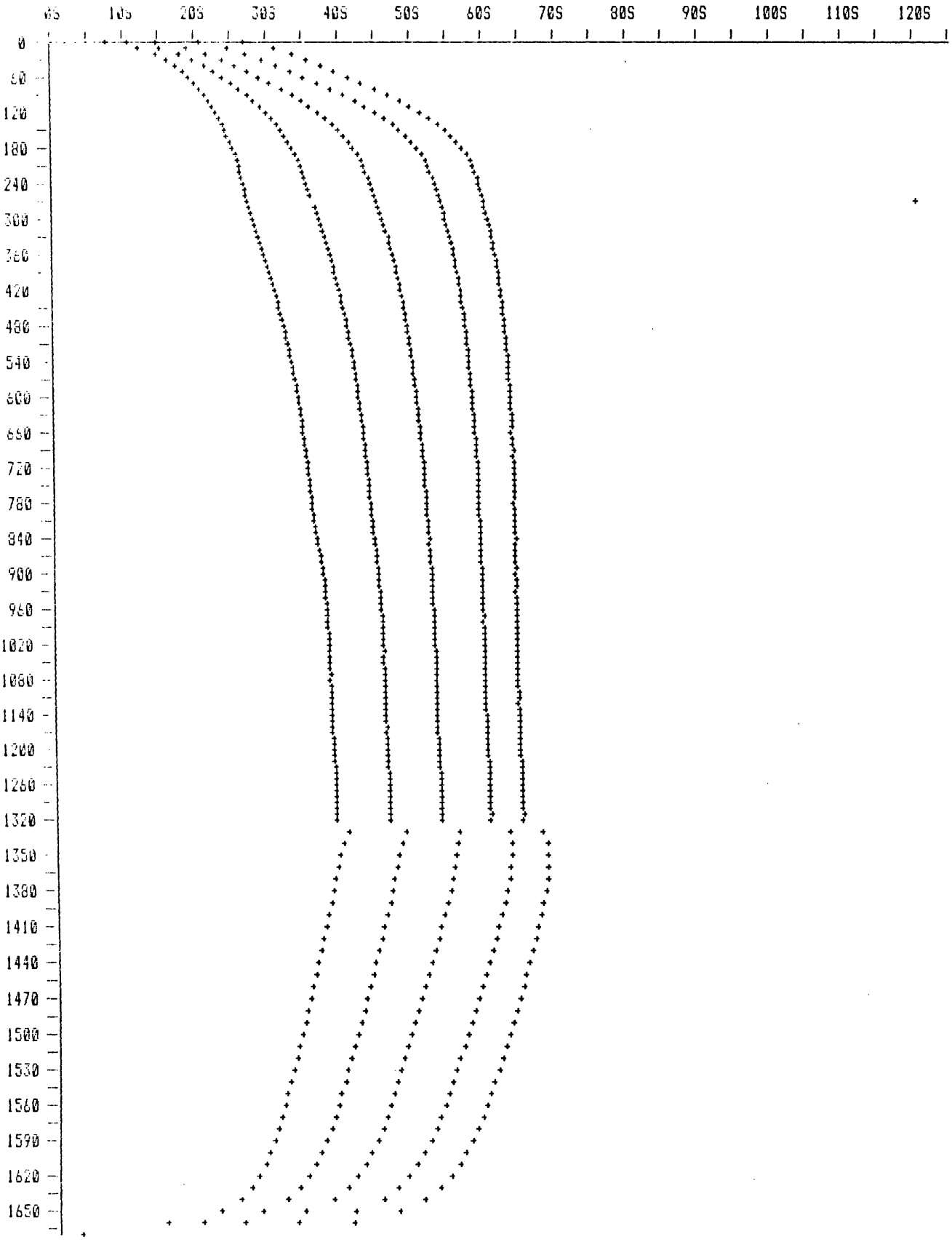
"RUN 8" : Ch-D MODULE 4 containing "S4" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2Hz



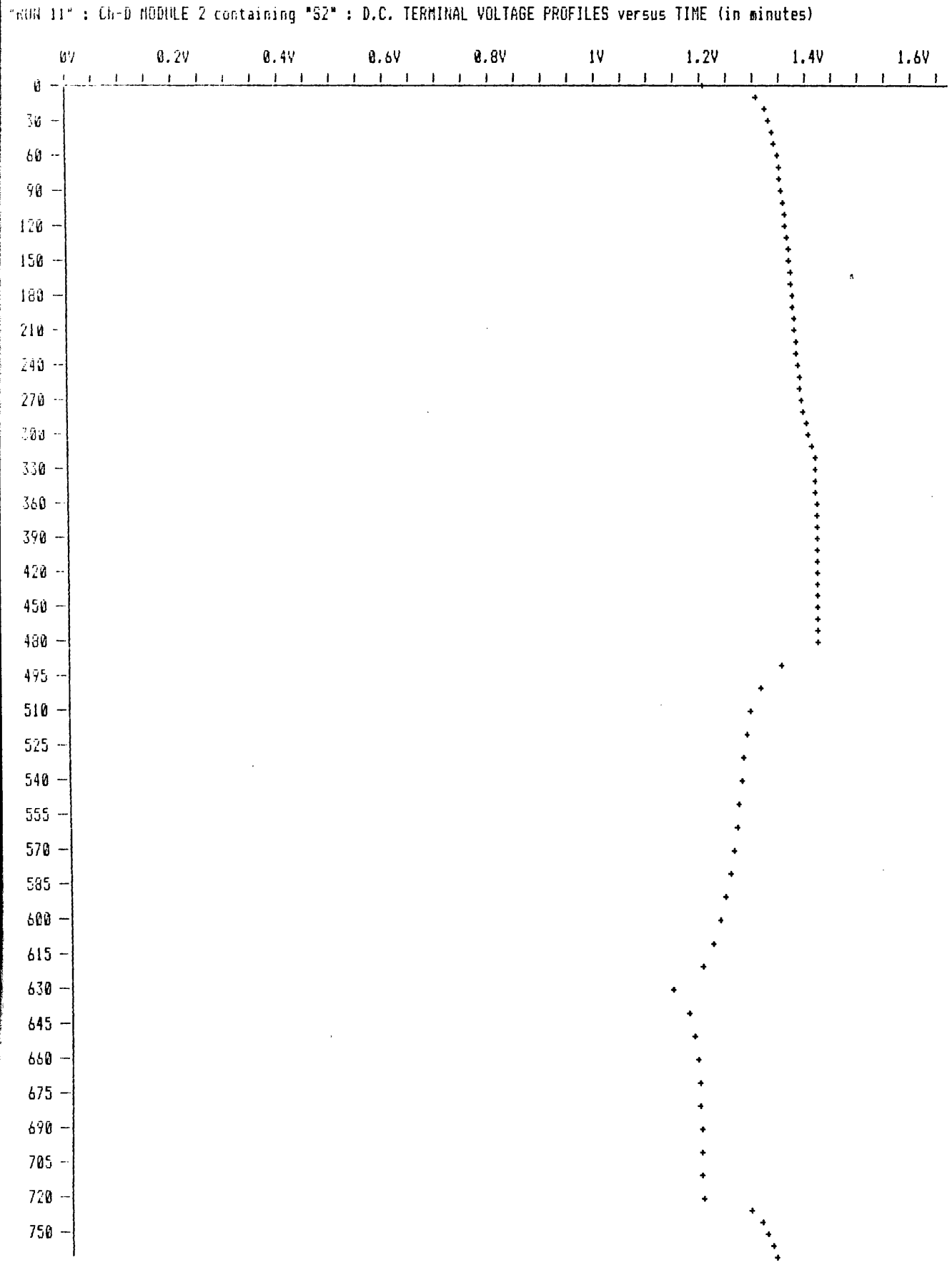
Graph 1(I)

Note: Curve order is 2Hz >>> 32Hz

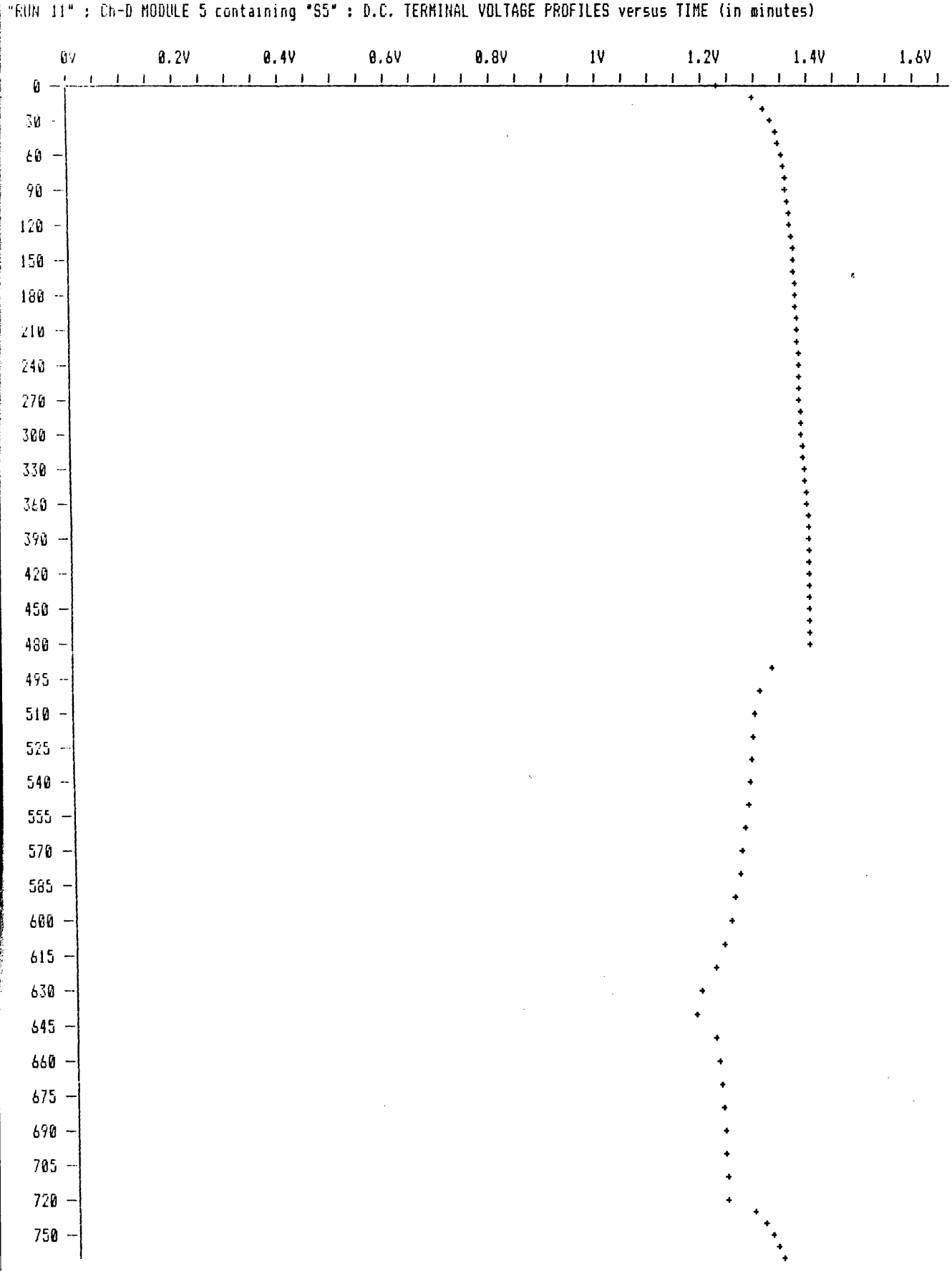
"RUN 8" : Ch-D MODULE 6 containing "S6" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2Hz



Graph 2(a)


"RUN 11" : Ch-D MODULE 2 containing "S2" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

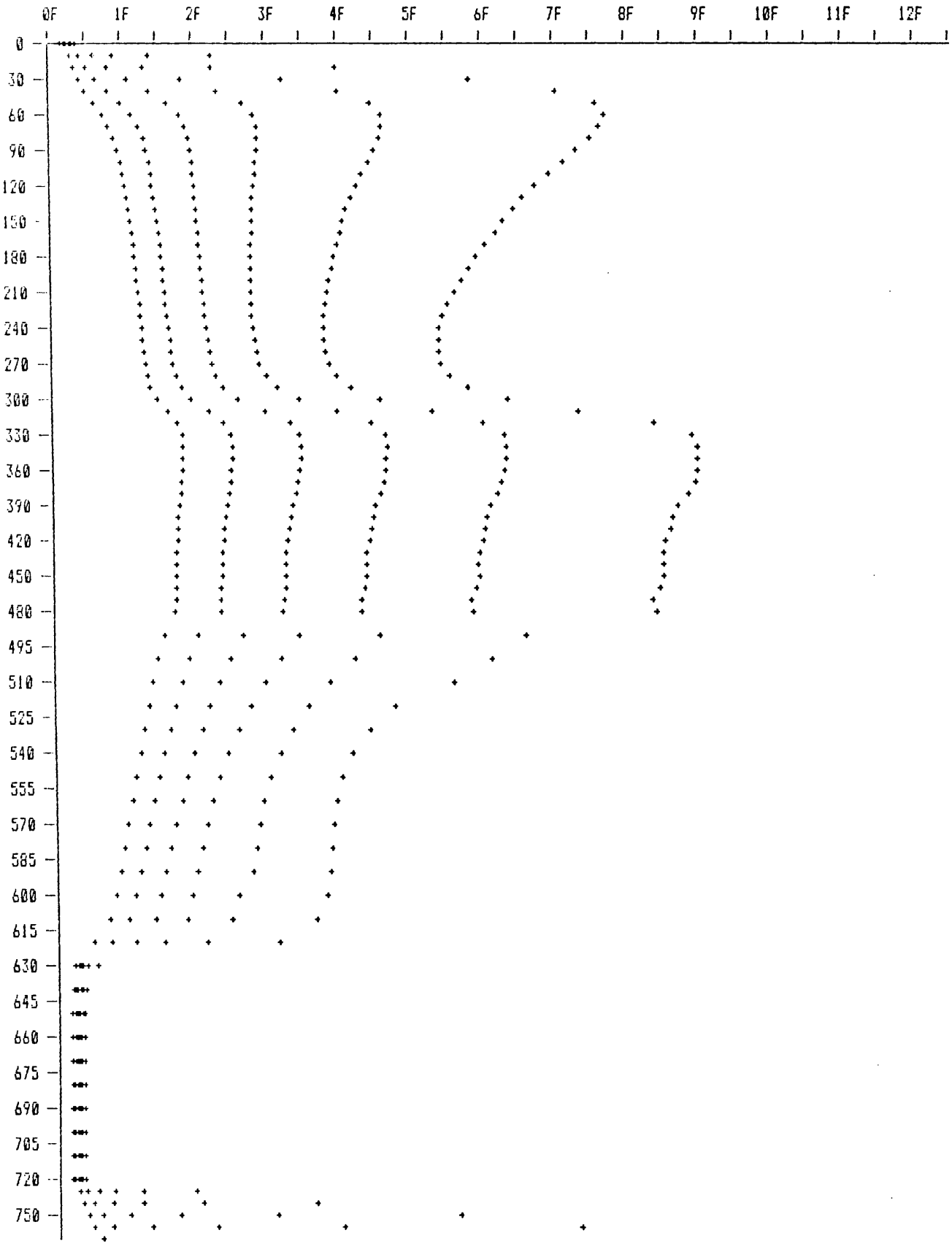
Graph 2(b)


"RUN 11" : Ch-D MODULE 5 containing "S5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 2(c)

Note: Curve order is 32Hz >>> 1Hz

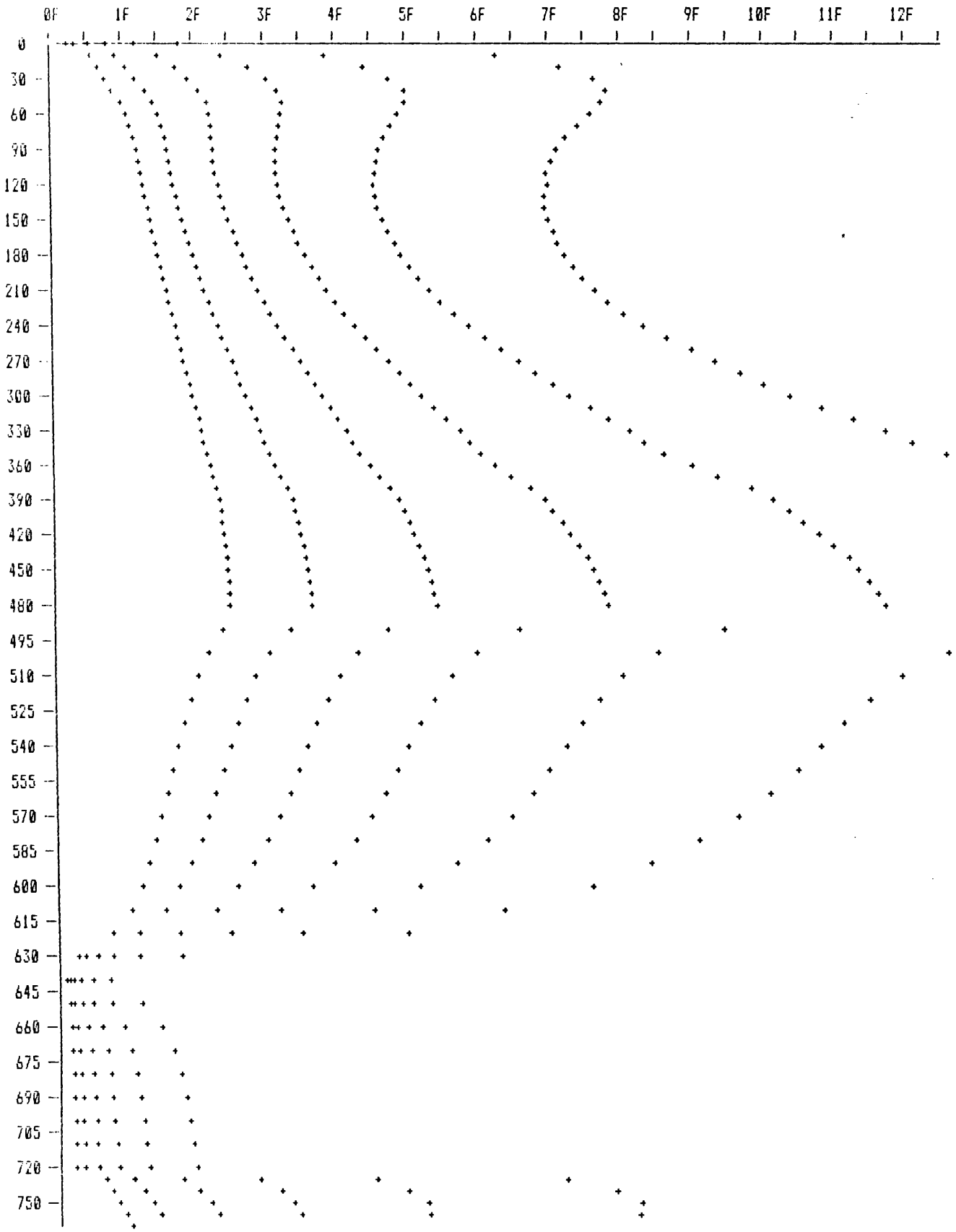
"RUN 11" : Ch-D MODULE 2 containing "S2" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 2(d)

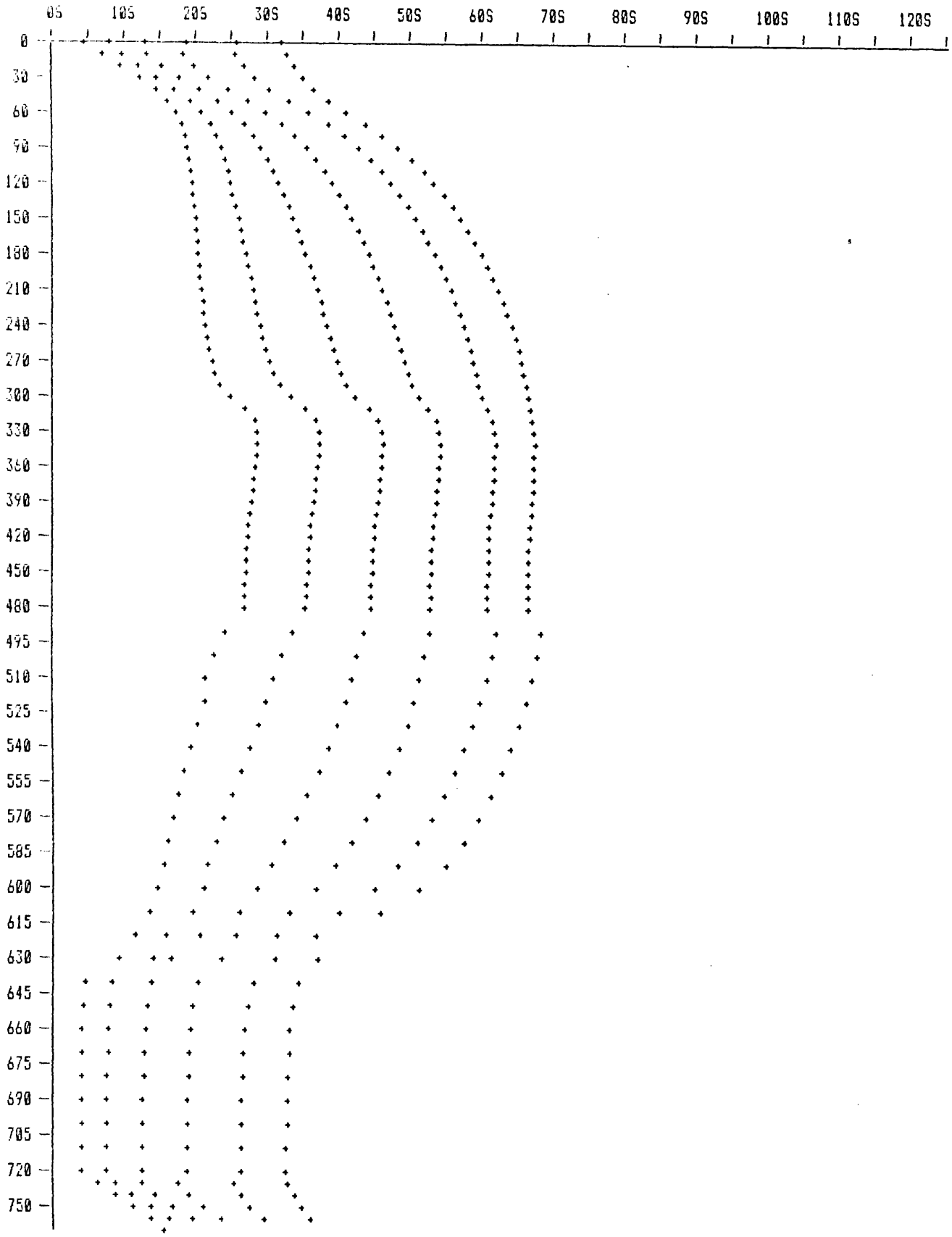
Note: Curve order is 32Hz >>> 1Hz

"RUN 11" : Ch-D MODULE 5 containing "S5" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Note: Curve order is 1Hz >>> 32Hz

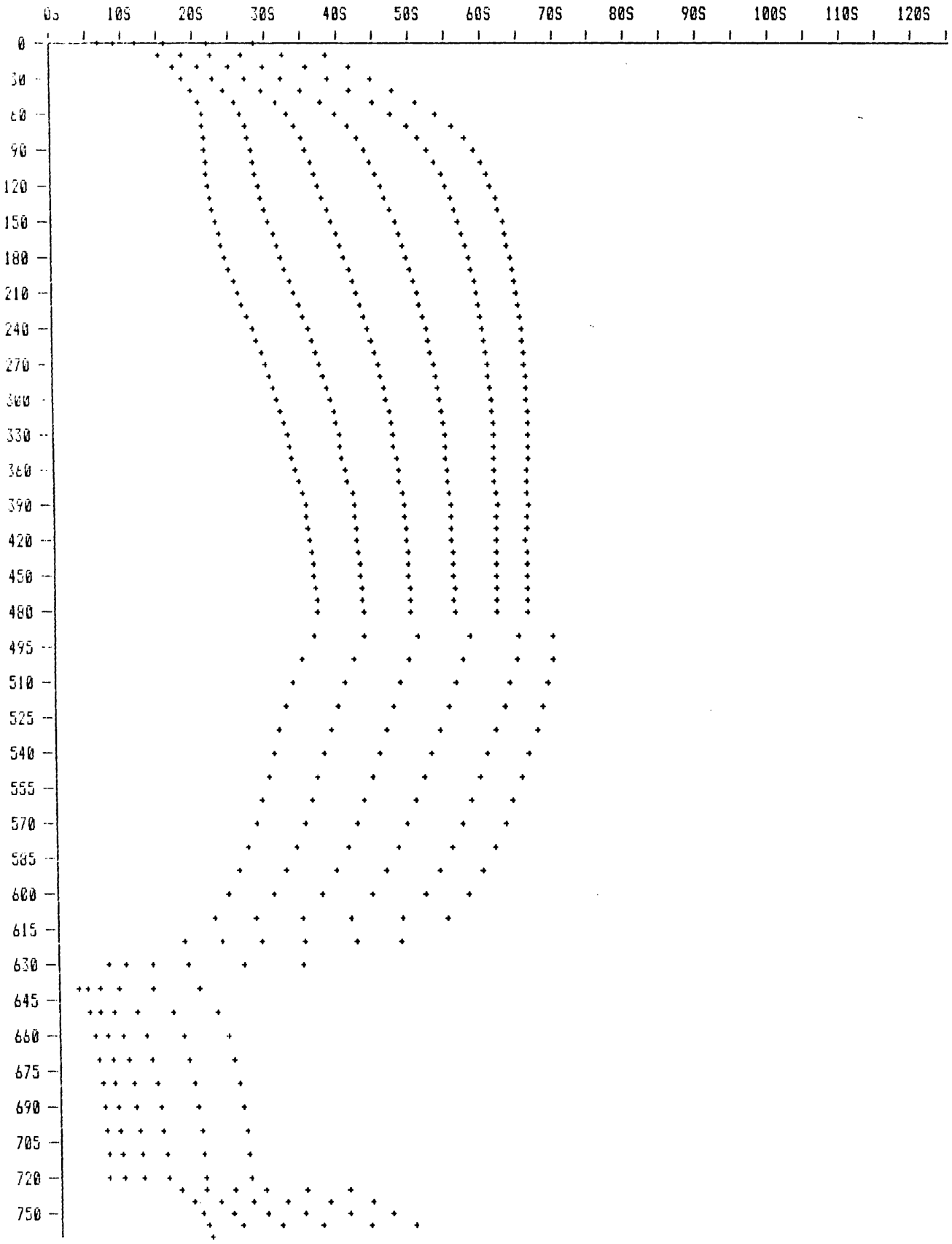
"RUN 11" : Ch-D MODULE 2 containing "S2" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 2(i)

Note: Curve order is 1Hz >>> 32Hz

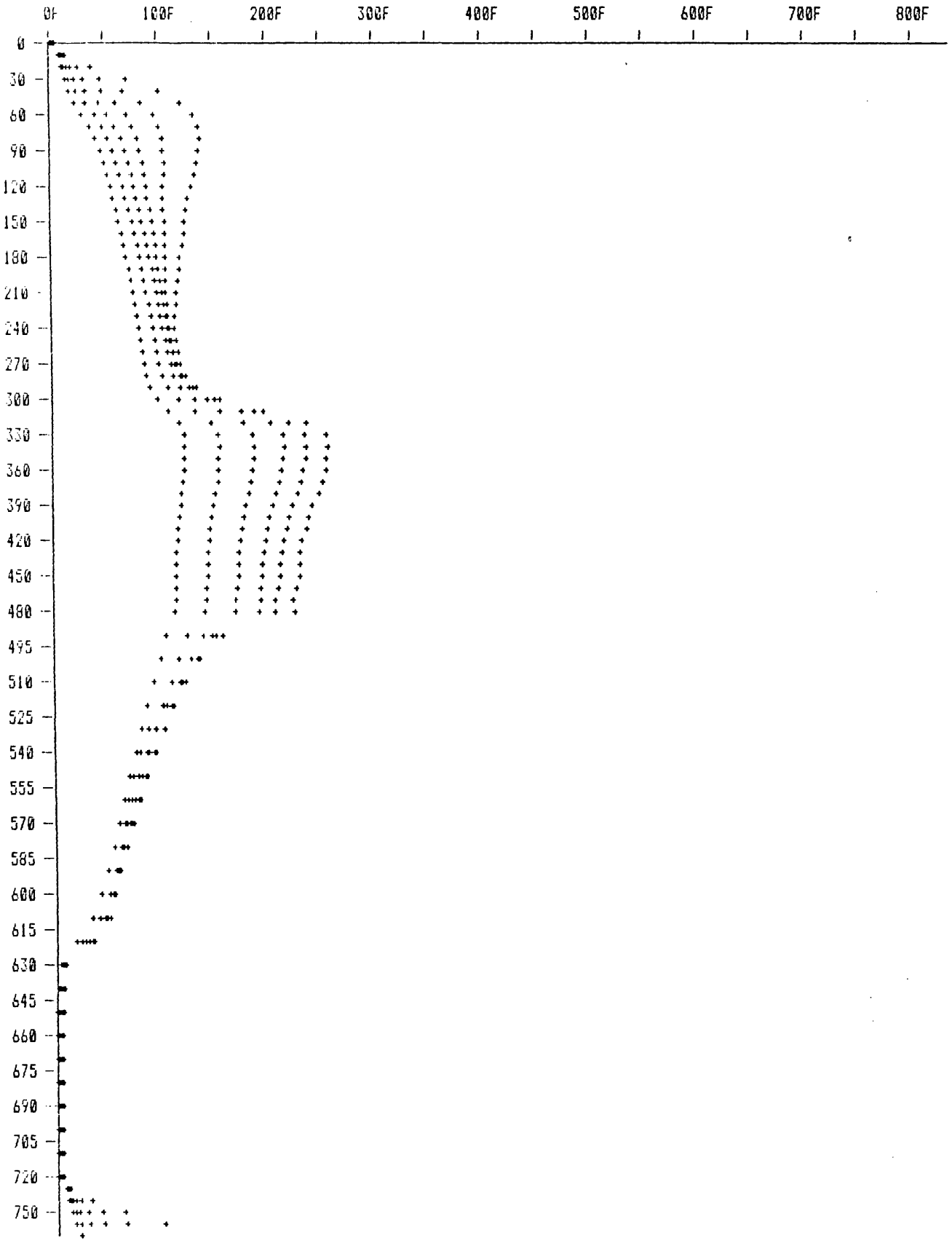
"RUN 11" : Ch-0 MODULE 5 containing "S5" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 2(g)

Note: Curve order is generally 32Hz >>> 1Hz

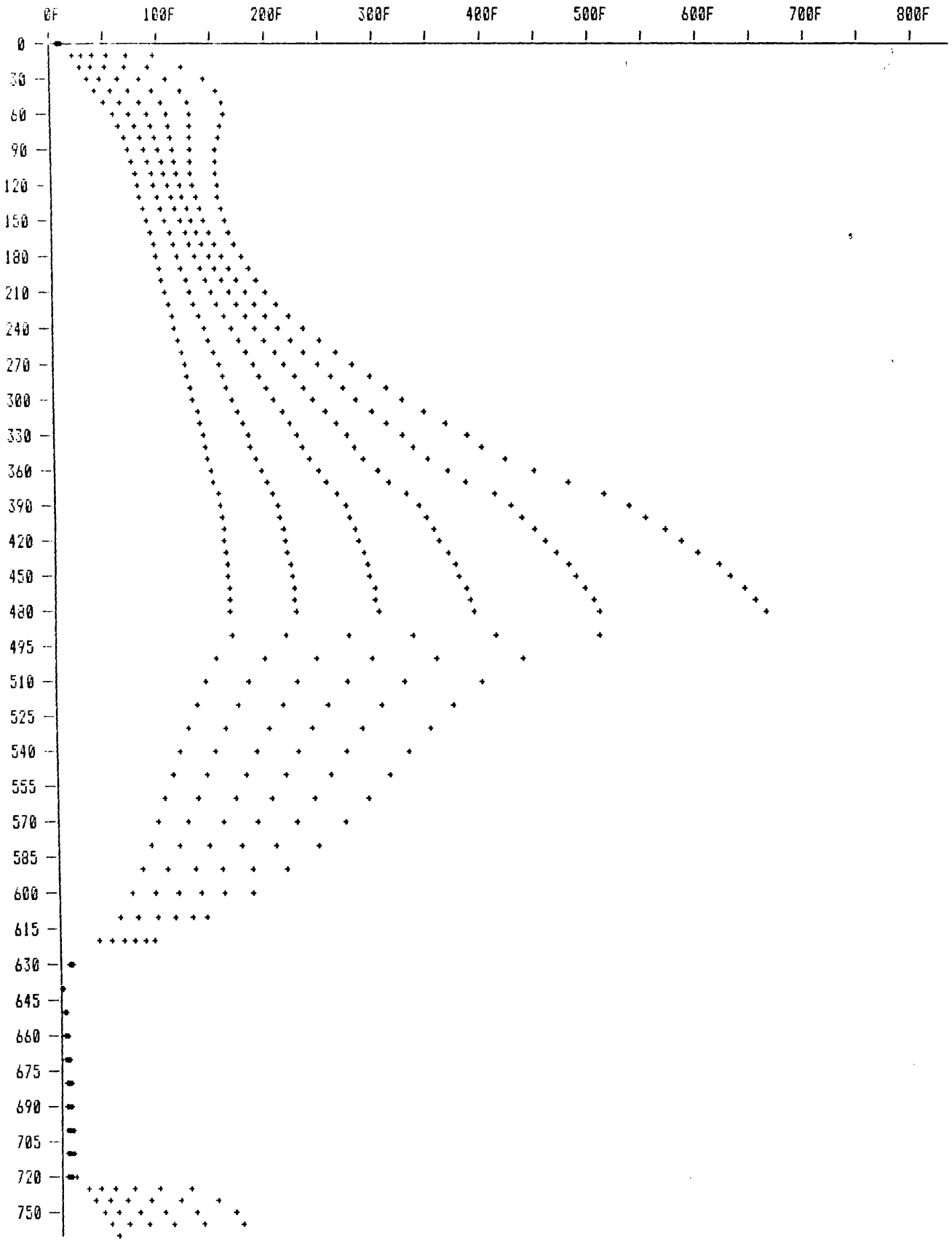
"RUN 11" : Ch-D MODULE 2 containing "S2" : (E.S.C. + E.S.CON.) PROFILES at frequencies 32,16,8,4,2,1Hz



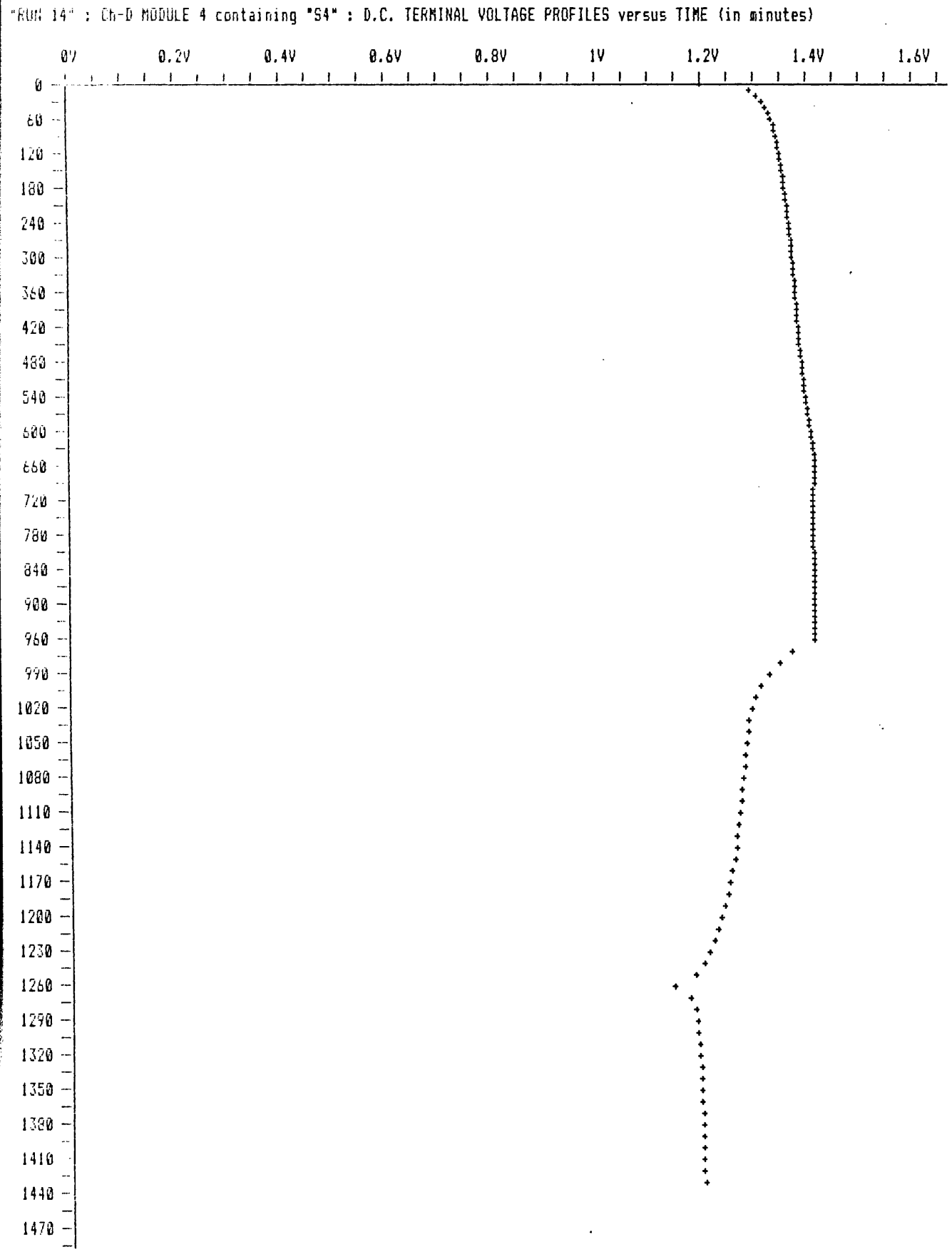
Graph 2(h)

Note: Curve order is 32Hz >>> 1Hz

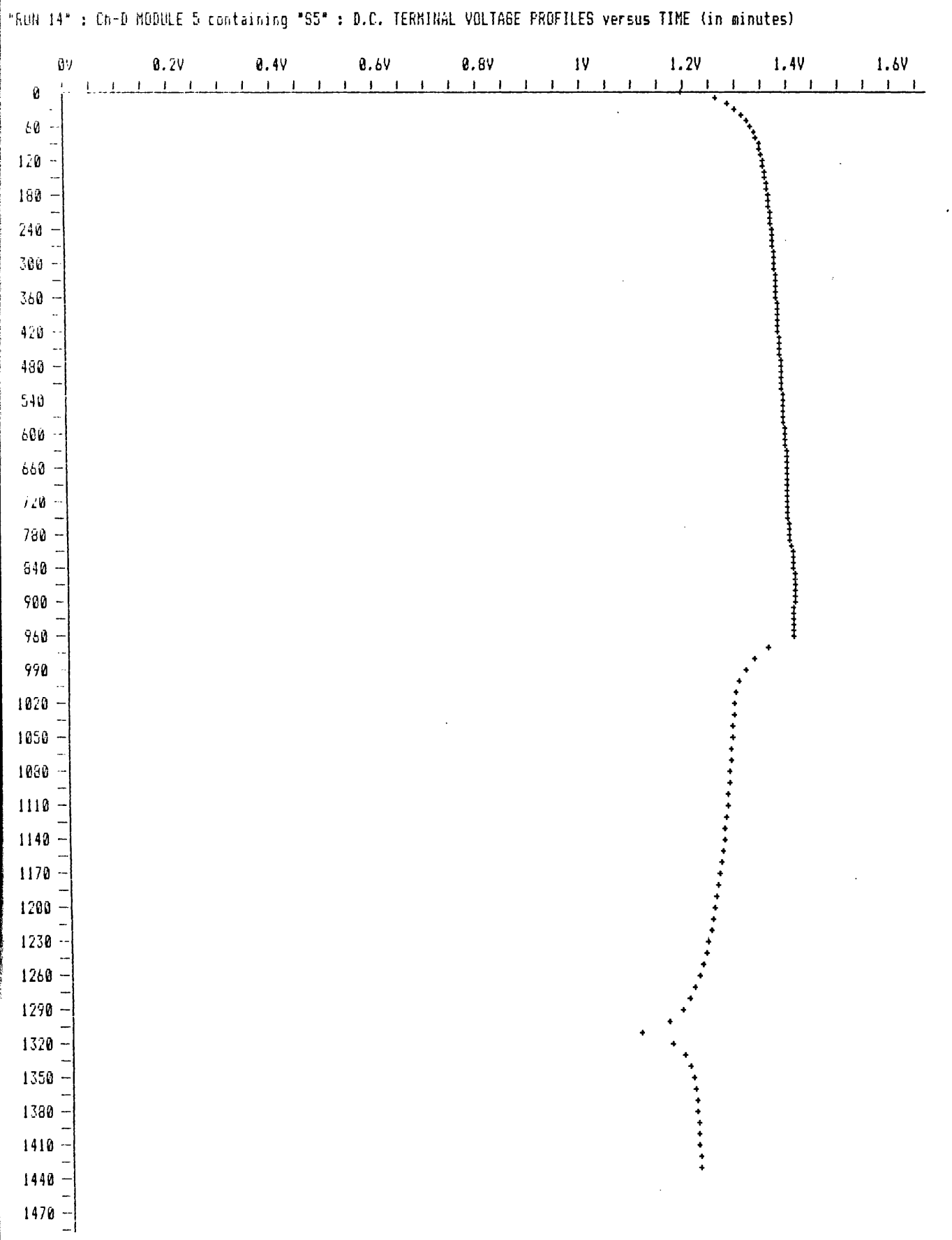
"RUN 11" : Ch-0 MODULE 5 containing "S5" : (E.S.C. & E.S.CON.) PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 3(a)

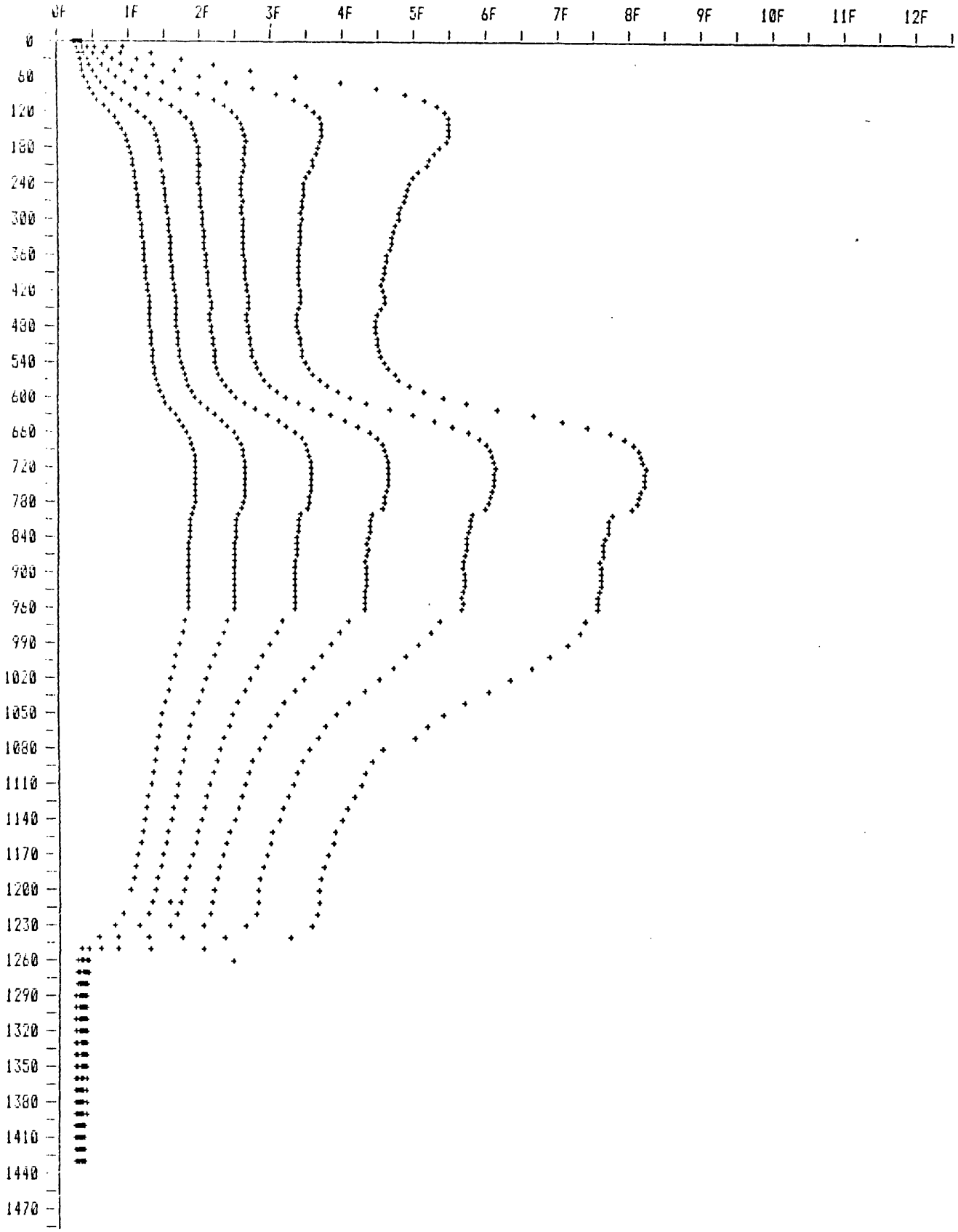

"RUN 14" : Ch-D MODULE 4 containing "S4" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
990
1020
1050
1080
1110
1140
1170
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 3(b)


"RUN 14" : Ch-D MODULE 5 containing "S5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
990
1020
1050
1080
1110
1140
1170
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Note: Curve order is 32Hz >>> 1Hz

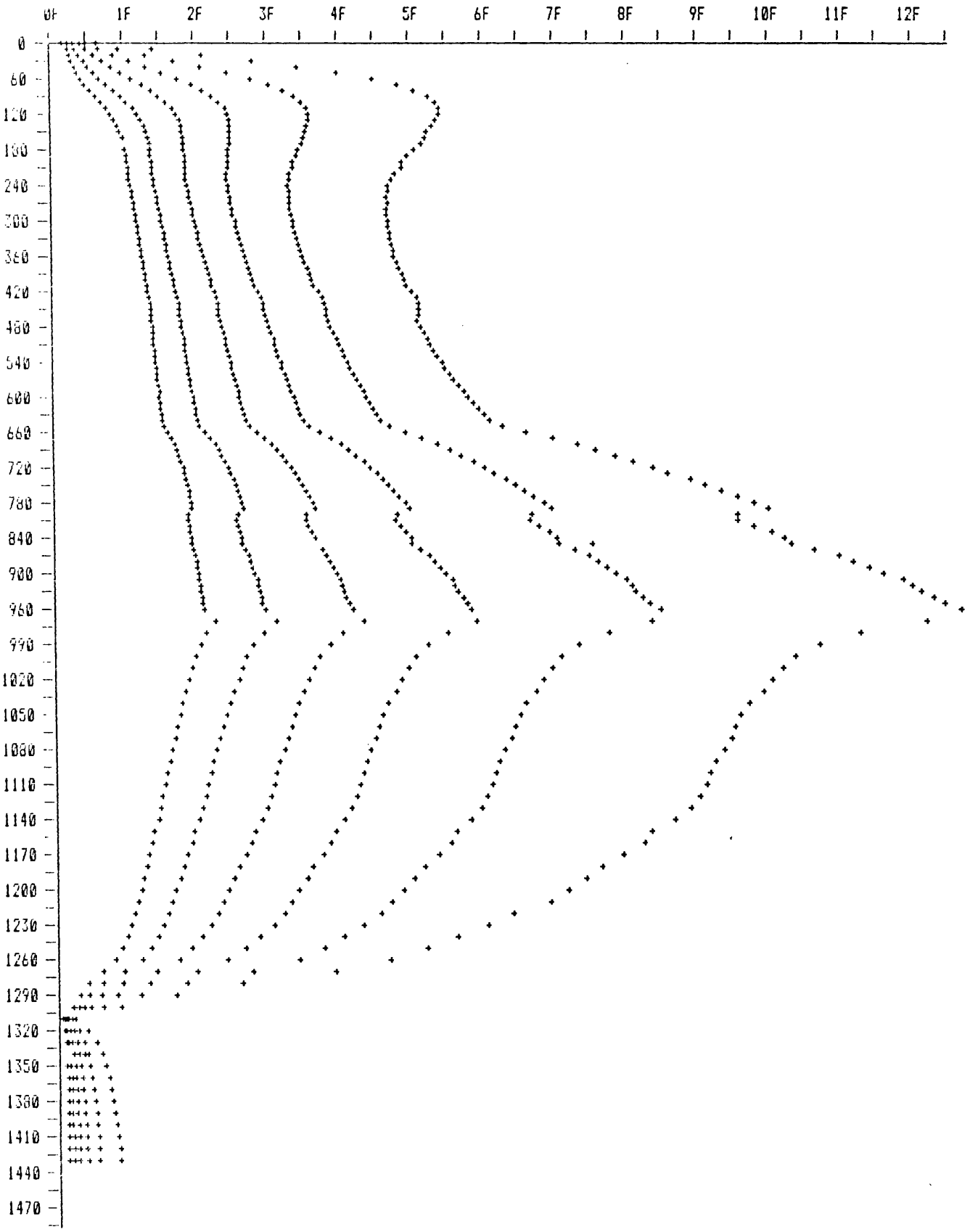
"RUN 14" : Ch-D MODULE 4 containing "S4" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 3(d)

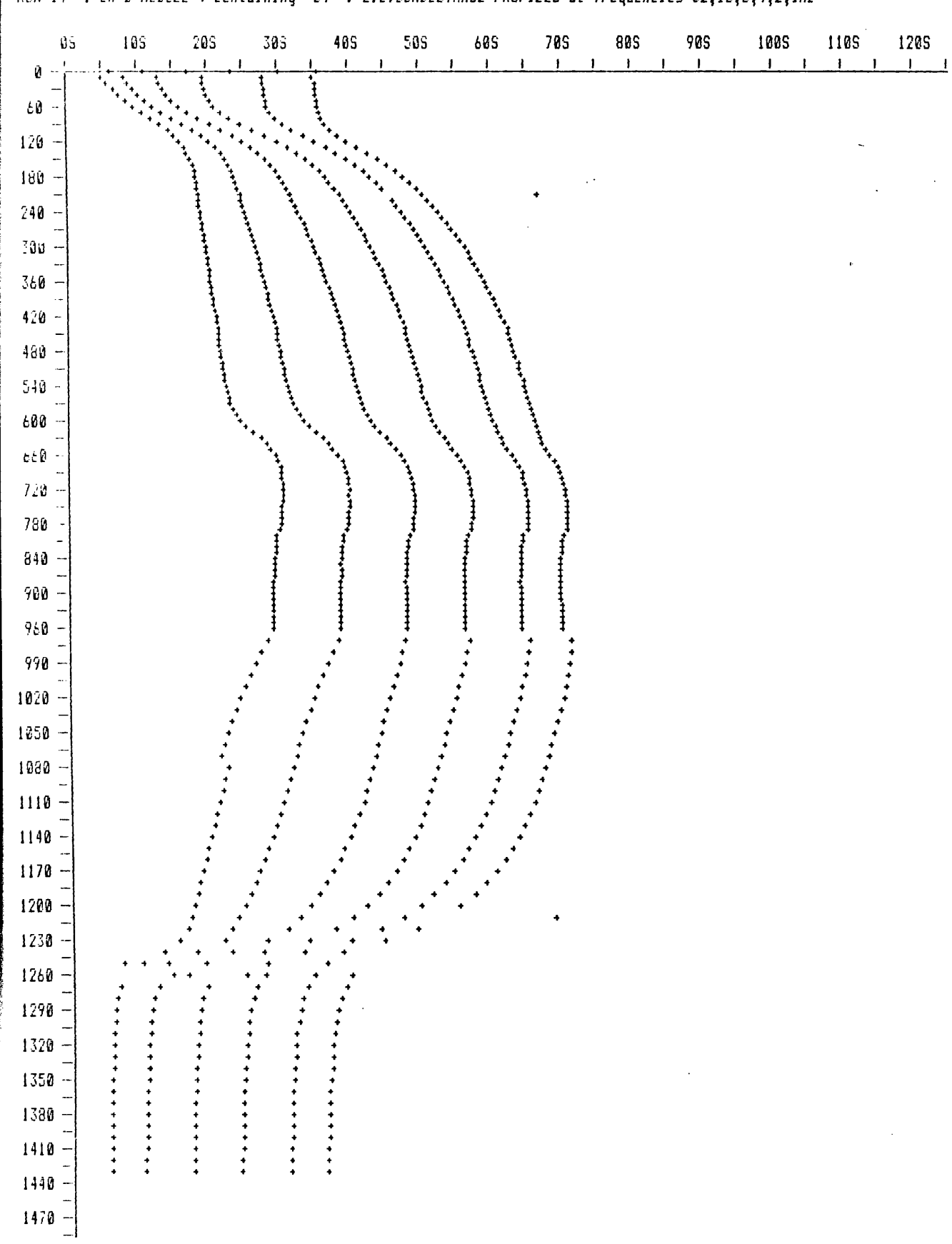
Note: Curve order is 32Hz >>> 1Hz

"RUN 14" : Ch-0 MODULE 5 containing "S5" : E.S.CAPACITANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 3(e)

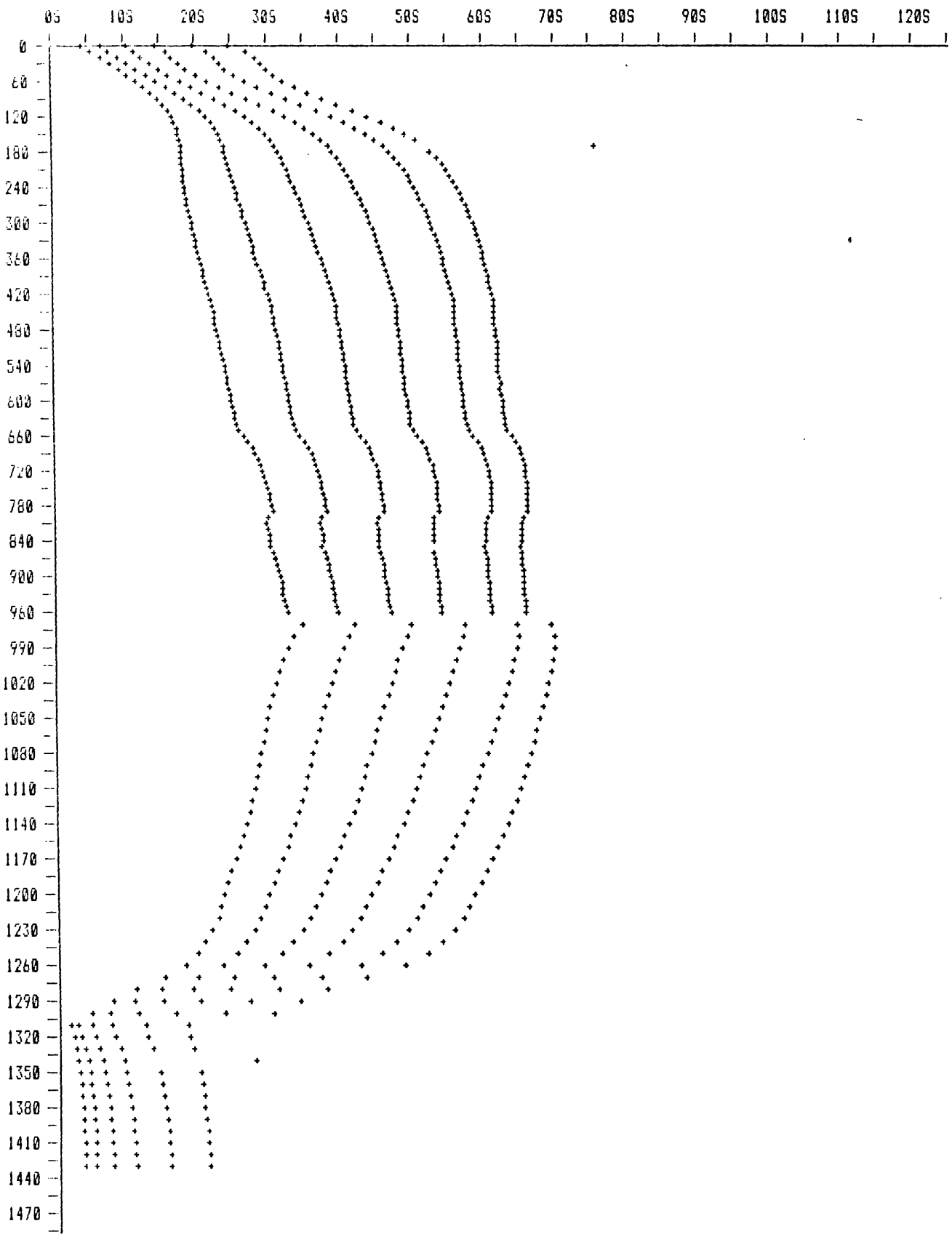
Note: Curve order is 1Hz >>> 32Hz



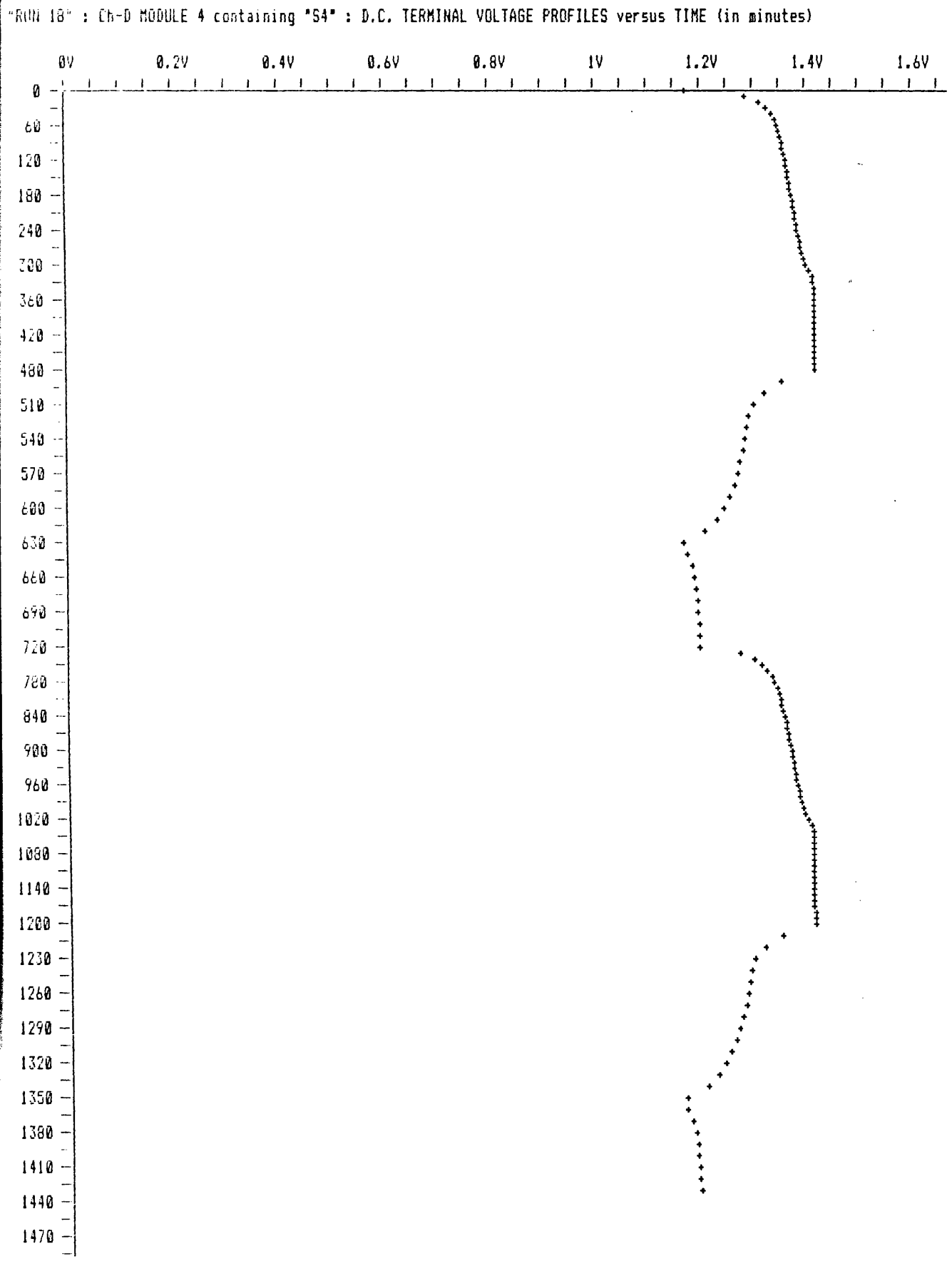
Graph 3(f)

Note: Curve order is 1Hz >>> 32Hz

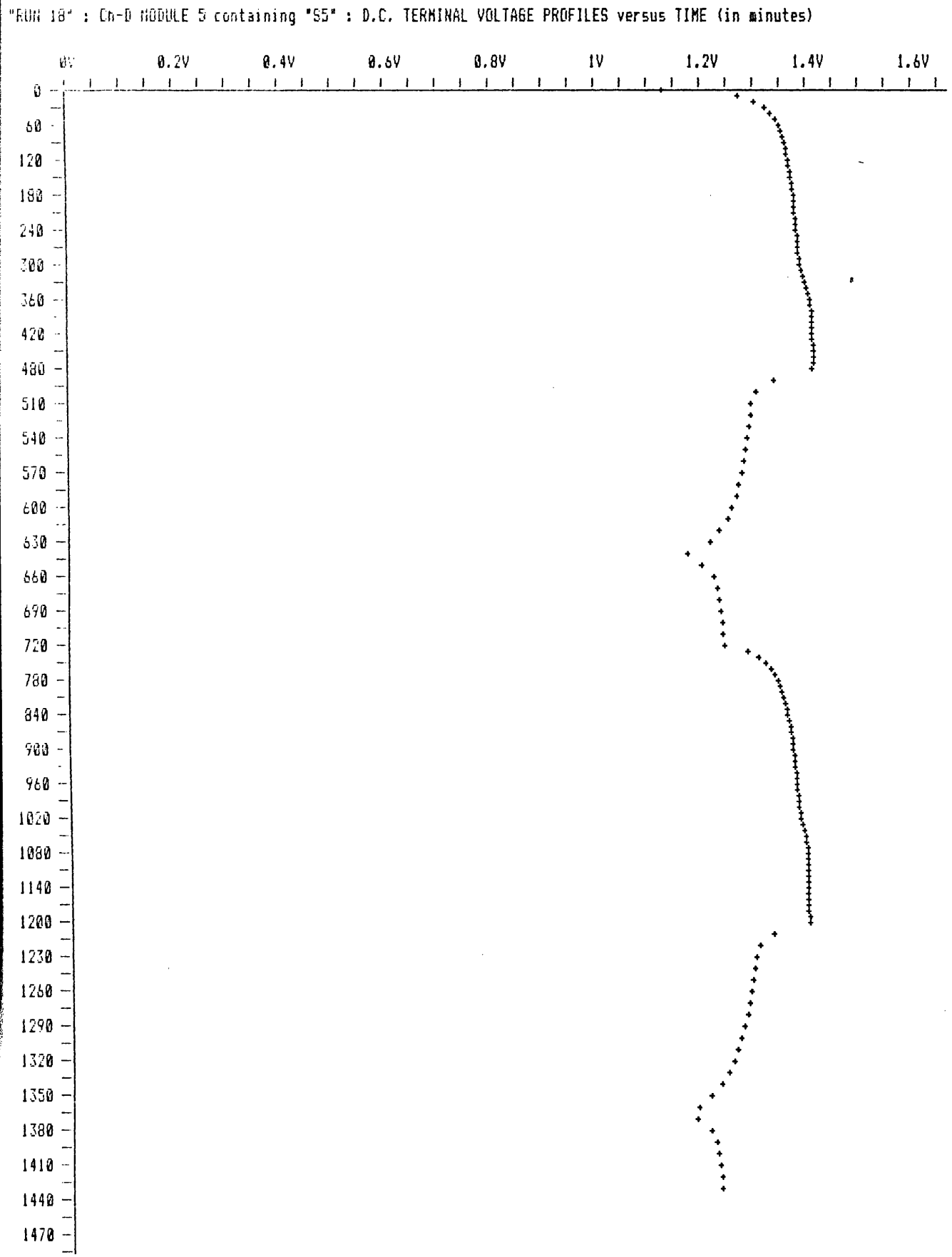
"RUN 14" : Ch-D MODULE 5 containing "S5" : E.S.CONDUCTANCE PROFILES at frequencies 32,16,8,4,2,1Hz



Graph 4(a)

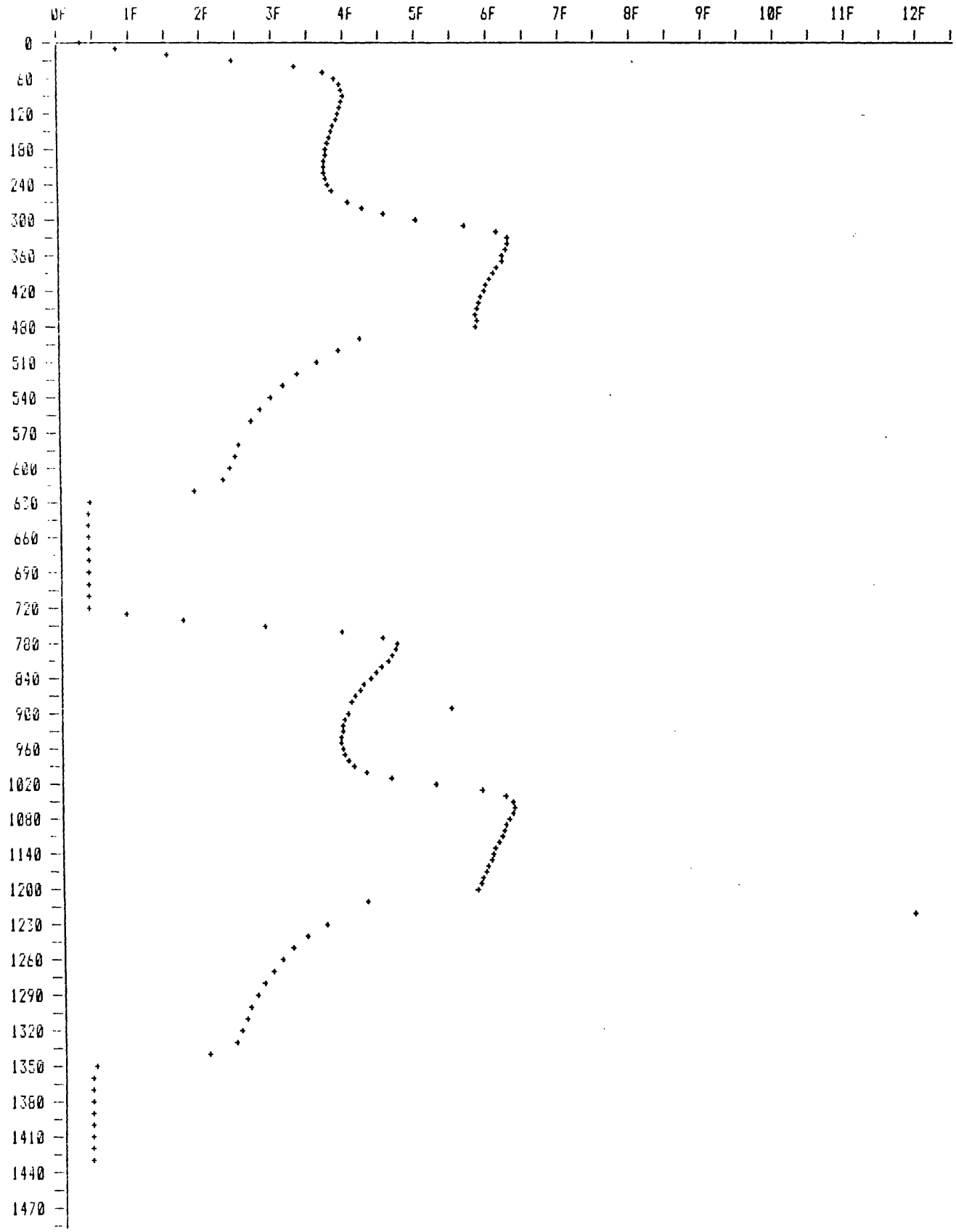

"RUN 18" : Ch-D MODULE 4 containing "S4" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(b)

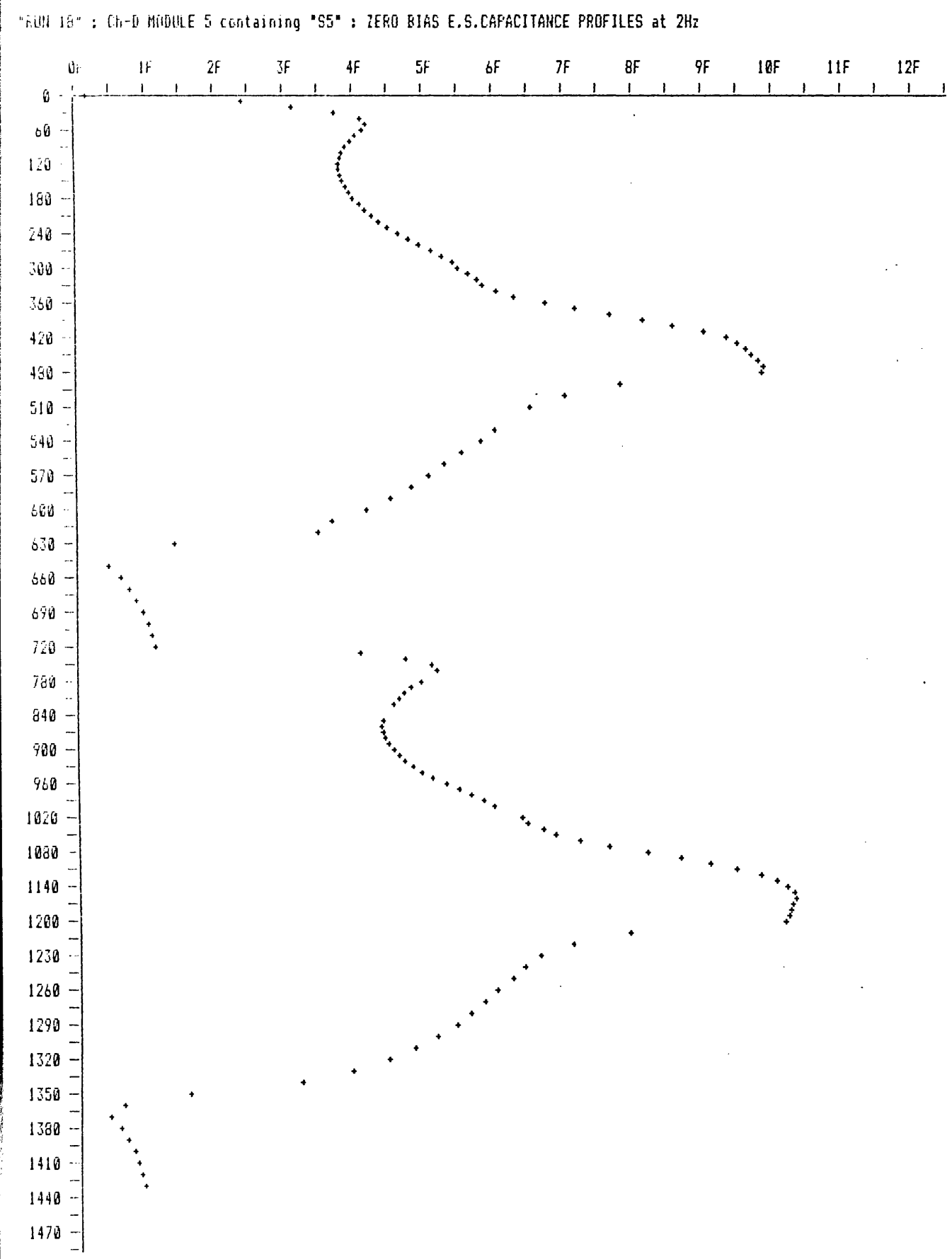

"RUN 18" : Ch-D MODULE 5 containing "S5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(c)

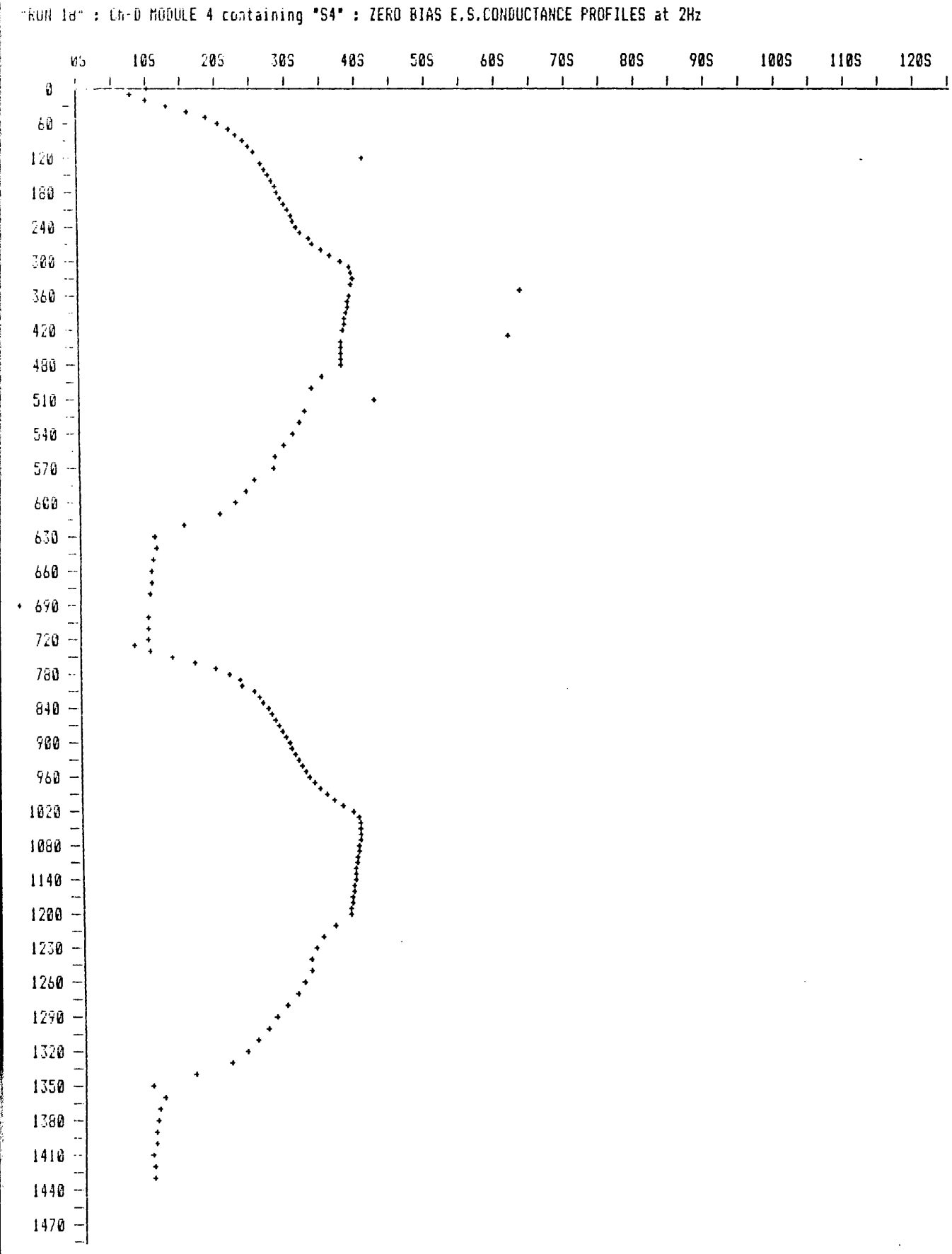
"RUN 18" : Ch-D MODULE 4 containing "S4" : ZERO BIAS E.S.CAPACITANCE PROFILES at 2Hz



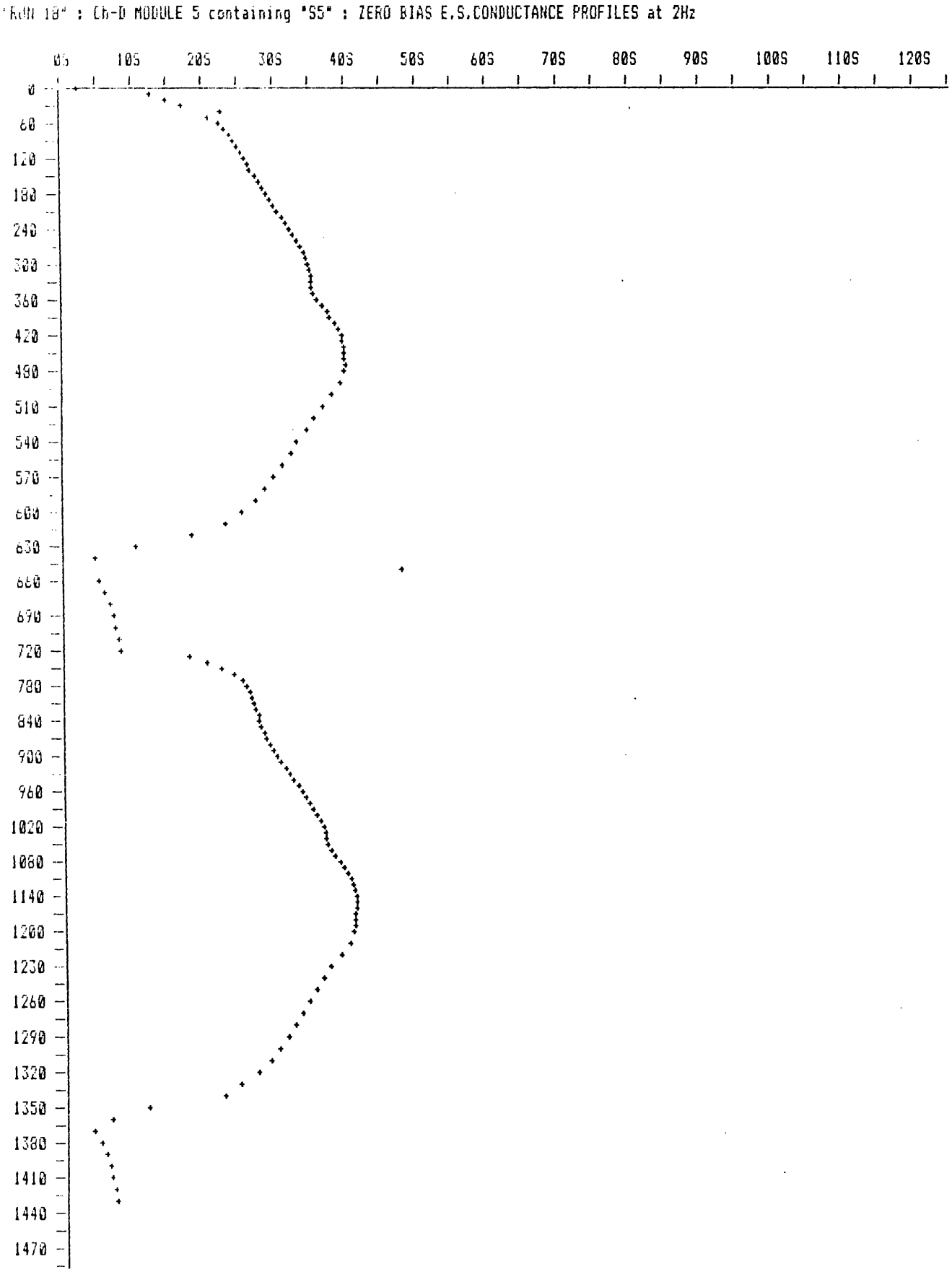
Graph 4(d)


"RUN 18" : Ch-D MODULE 5 containing "S5" : ZERO BIAS E.S.CAPACITANCE PROFILES at 2Hz
0F
1F
2F
3F
4F
5F
6F
7F
8F
9F
10F
11F
12F
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(e)

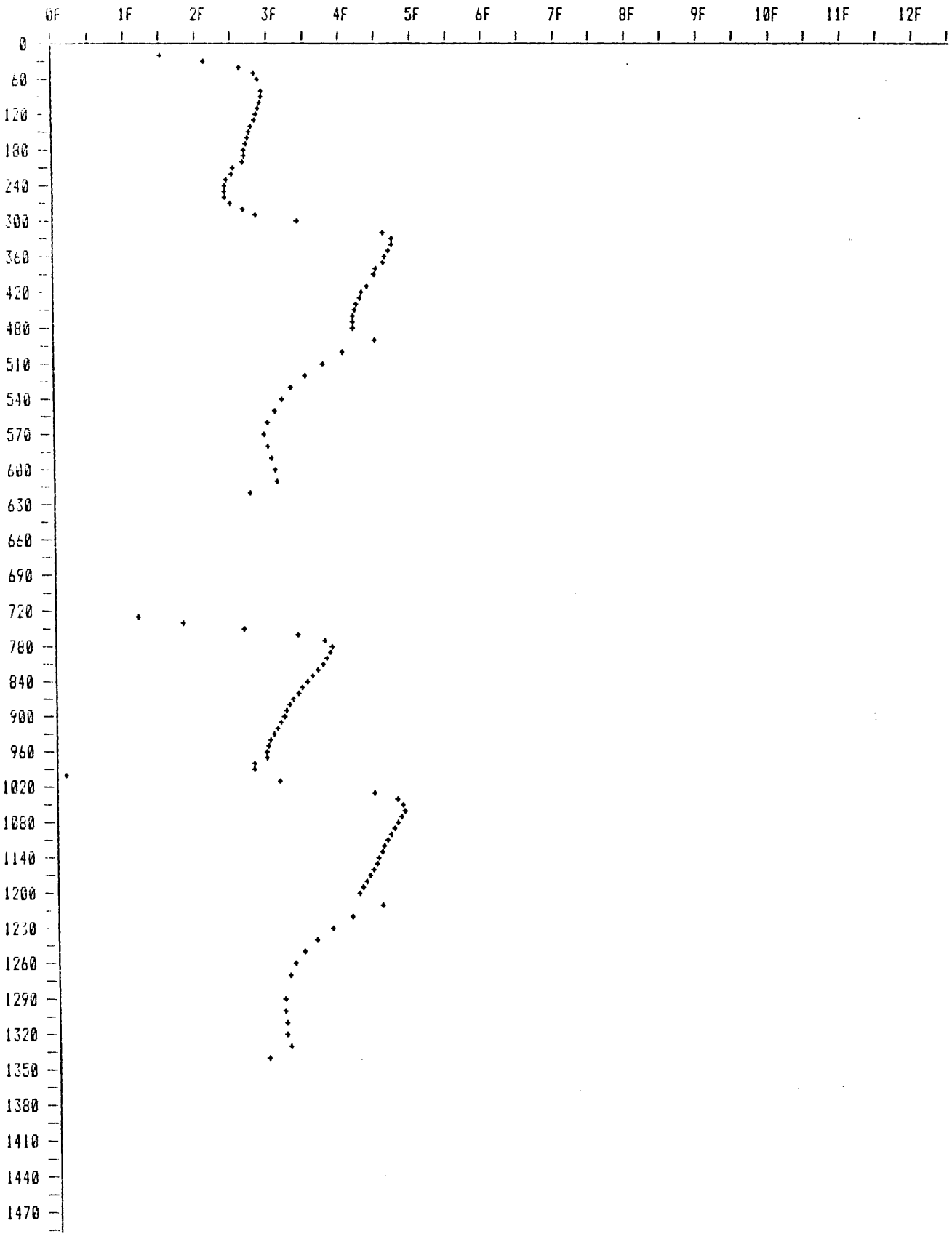

"RUN 1a" : Ch-D MODULE 4 containing "S4" : ZERO BIAS E.S.CONDUCTANCE PROFILES at 2Hz
0S
10S
20S
30S
40S
50S
60S
70S
80S
90S
100S
110S
120S
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(1)

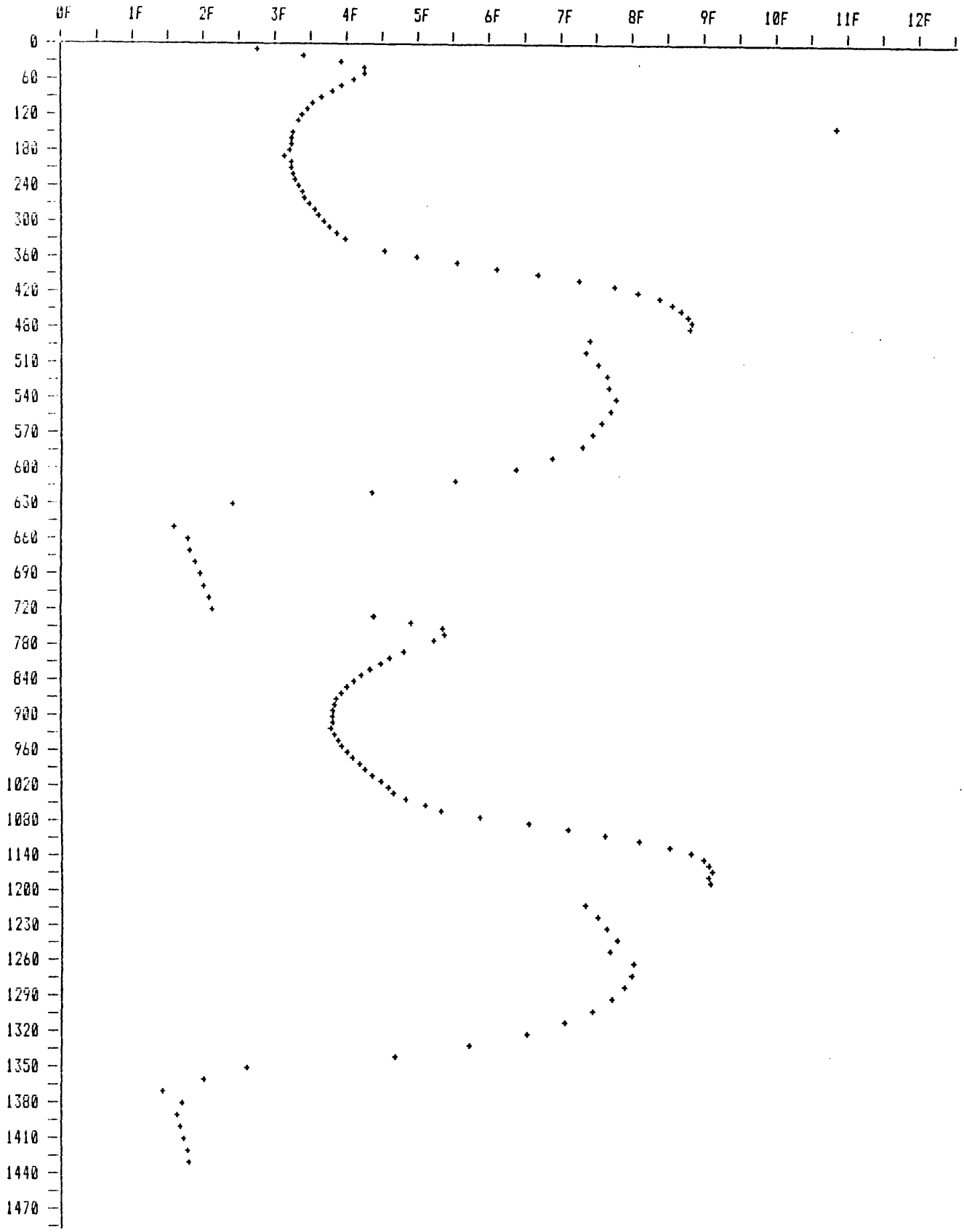

"RUN 18" : Ch-D MODULE 5 containing "S5" : ZERO BIAS E.S.CONDUCTANCE PROFILES at 2Hz
0S
10S
20S
30S
40S
50S
60S
70S
80S
90S
100S
110S
120S
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(g)

"RUN 18" : Ch-D MODULE 4 containing "S4" : +100μA BIAS E.S.CAPACITANCE PROFILES at 2Hz

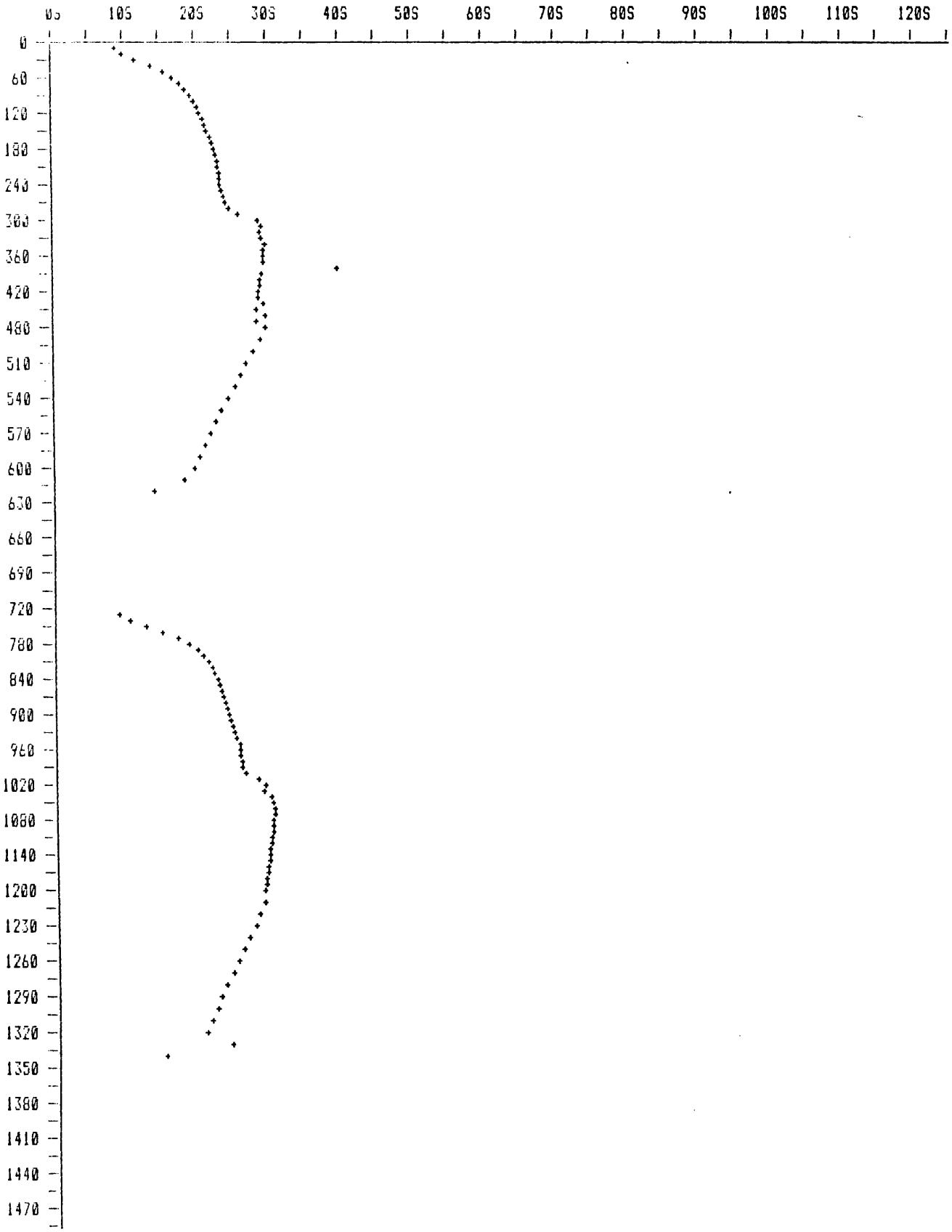


"RUN 18" : Ch-D MODULE 5 containing "S5" : +100nA BIAS E.S.CAPACITANCE PROFILES at 2Hz

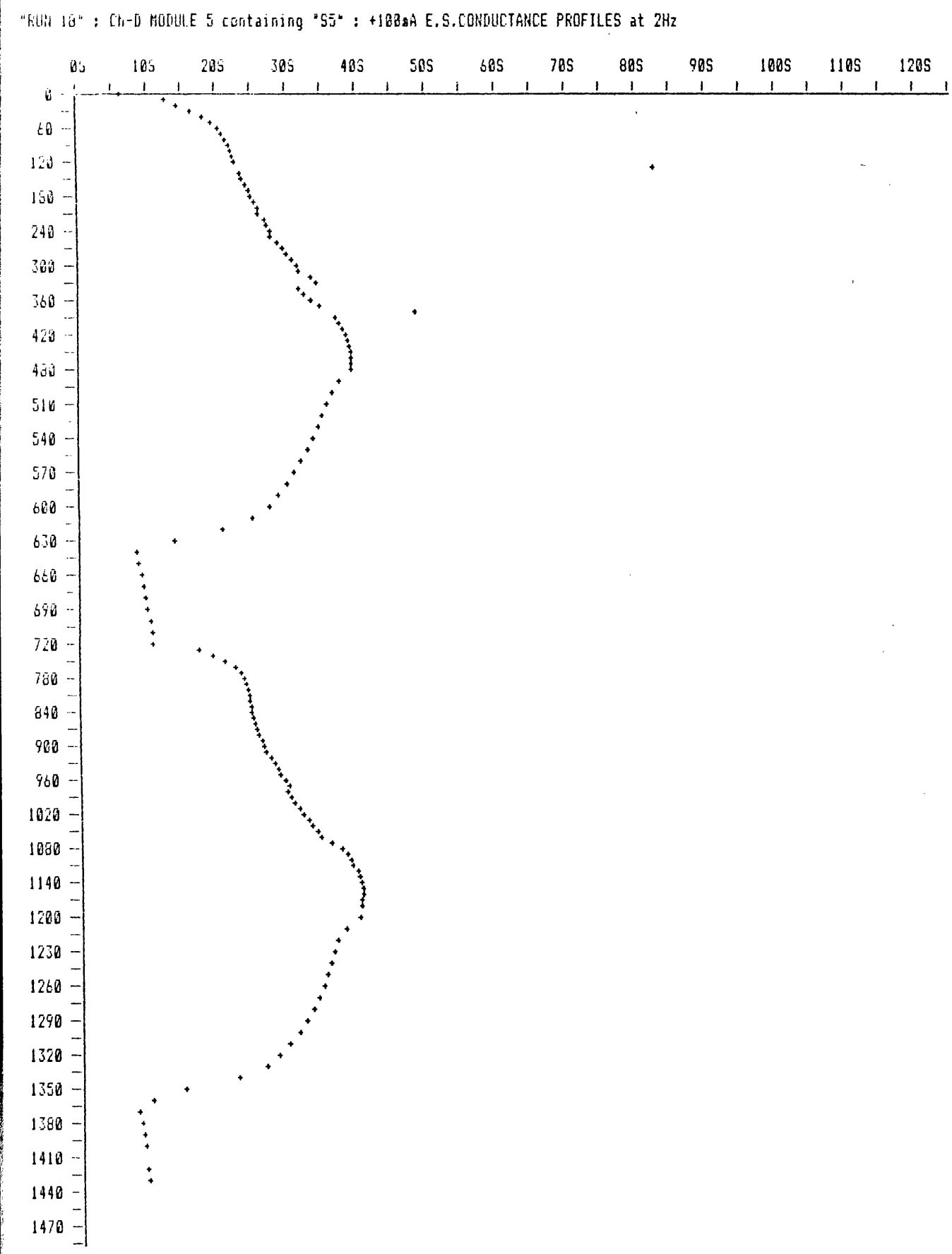


Graph 4(I)

"RUN 18" : Ch-D MODULE 4 containing "S4" : +100mA E.S.CONDUCTANCE PROFILES at 2Hz

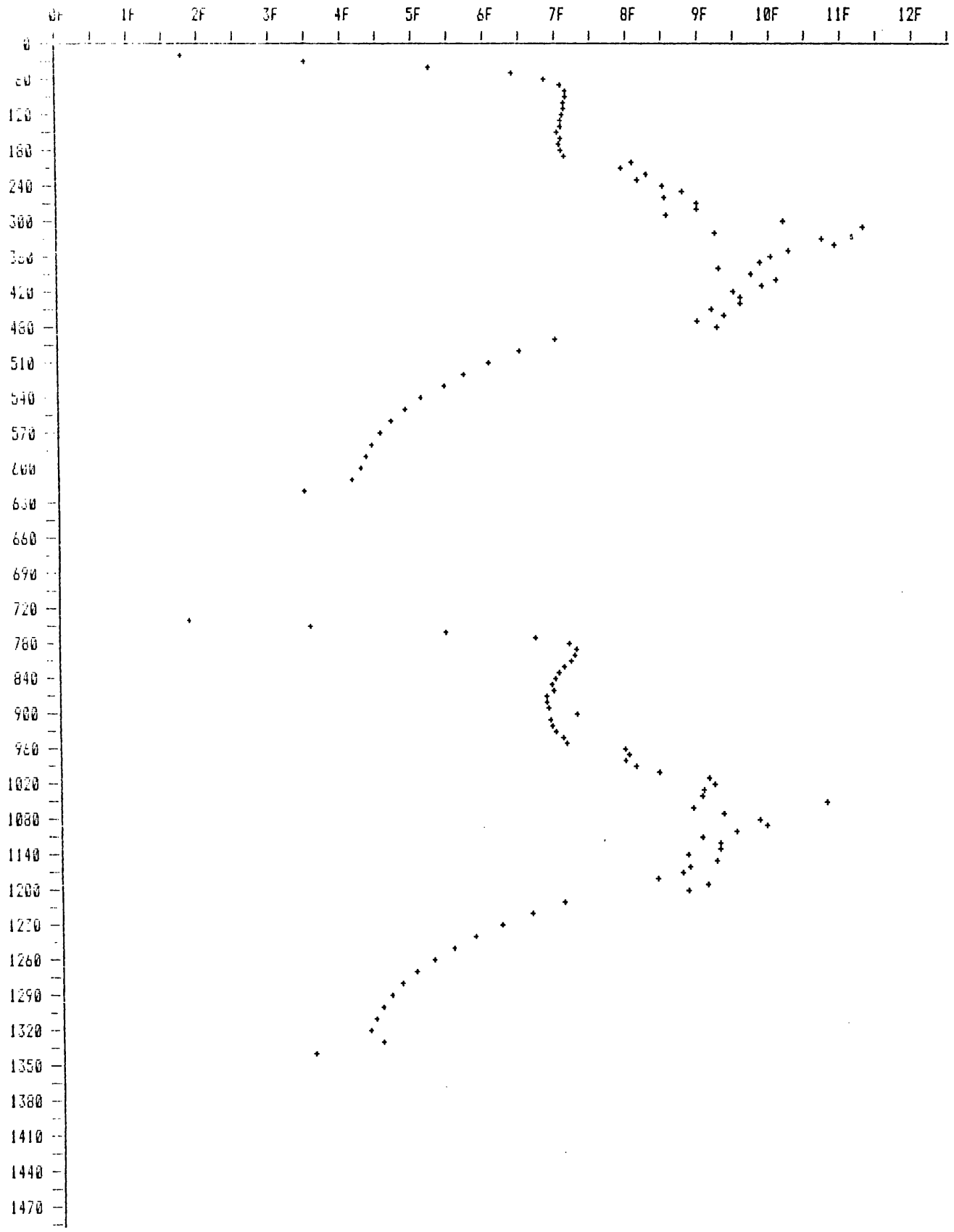


Graph 4(j)

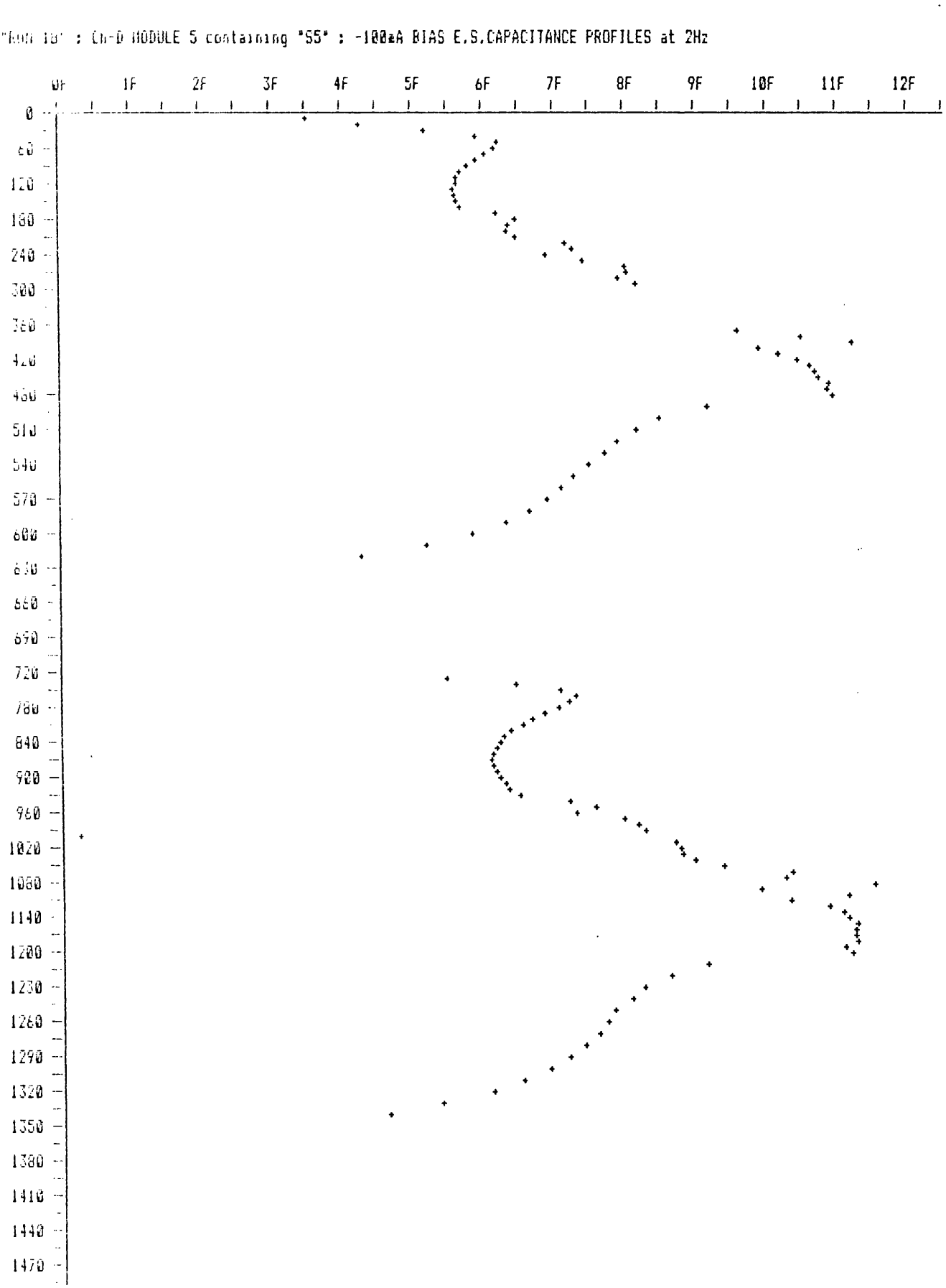

"RUN 18" : Ch-D MODULE 5 containing "S5" : +100mA E.S.CONDUCTANCE PROFILES at 2Hz
0S
10S
20S
30S
40S
50S
60S
70S
80S
90S
100S
110S
120S
0
60
120
150
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(k)

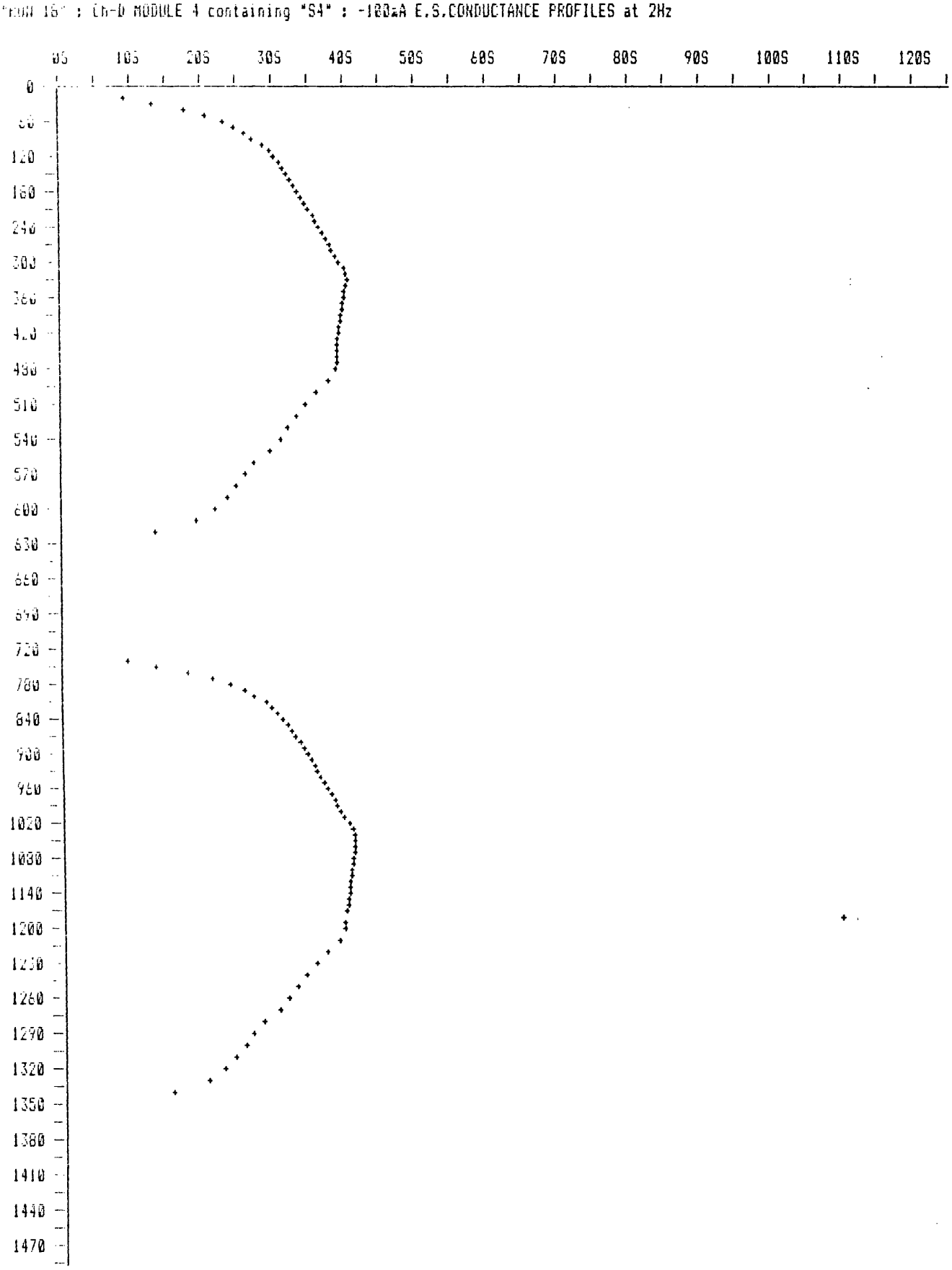
"RUN 16" : Ch-D MODULE 4 containing "S4" : -100mA BIAS E.S.CAPACITANCE PROFILES at 2Hz



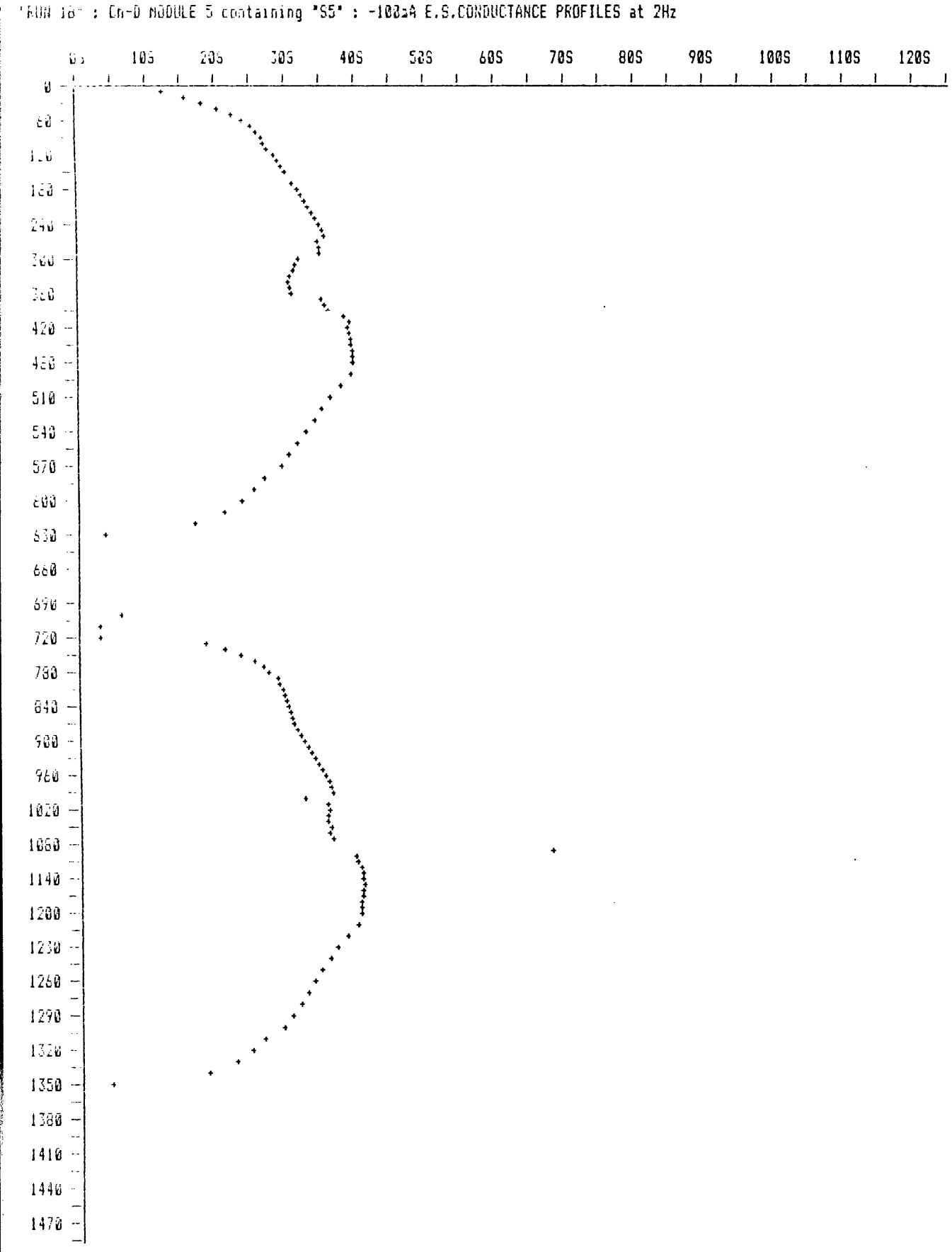
Graph 4(1)


"Book 18" : Ch-D MODULE 5 containing "S5" : -100aA BIAS E.S.CAPACITANCE PROFILES at 2Hz
0F
1F
2F
3F
4F
5F
6F
7F
8F
9F
10F
11F
12F
0
60
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

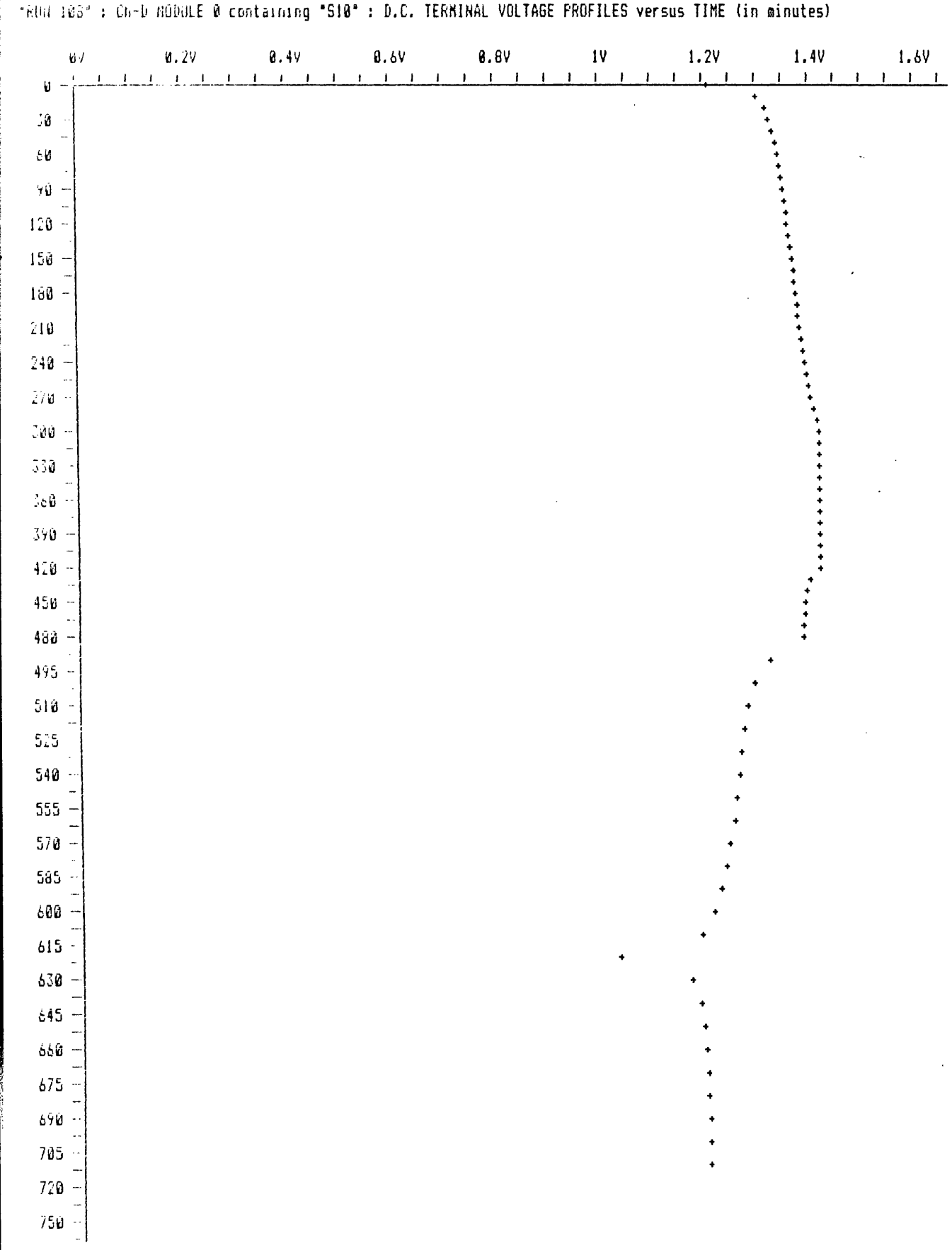
Graph 1(m)


"RUN 15" : Ch-D MODULE 4 containing "S4" : -100zA E.S.CONDUCTANCE PROFILES at 2Hz
0S
10S
20S
30S
40S
50S
60S
70S
80S
90S
100S
110S
120S
0
120
180
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 4(ii)

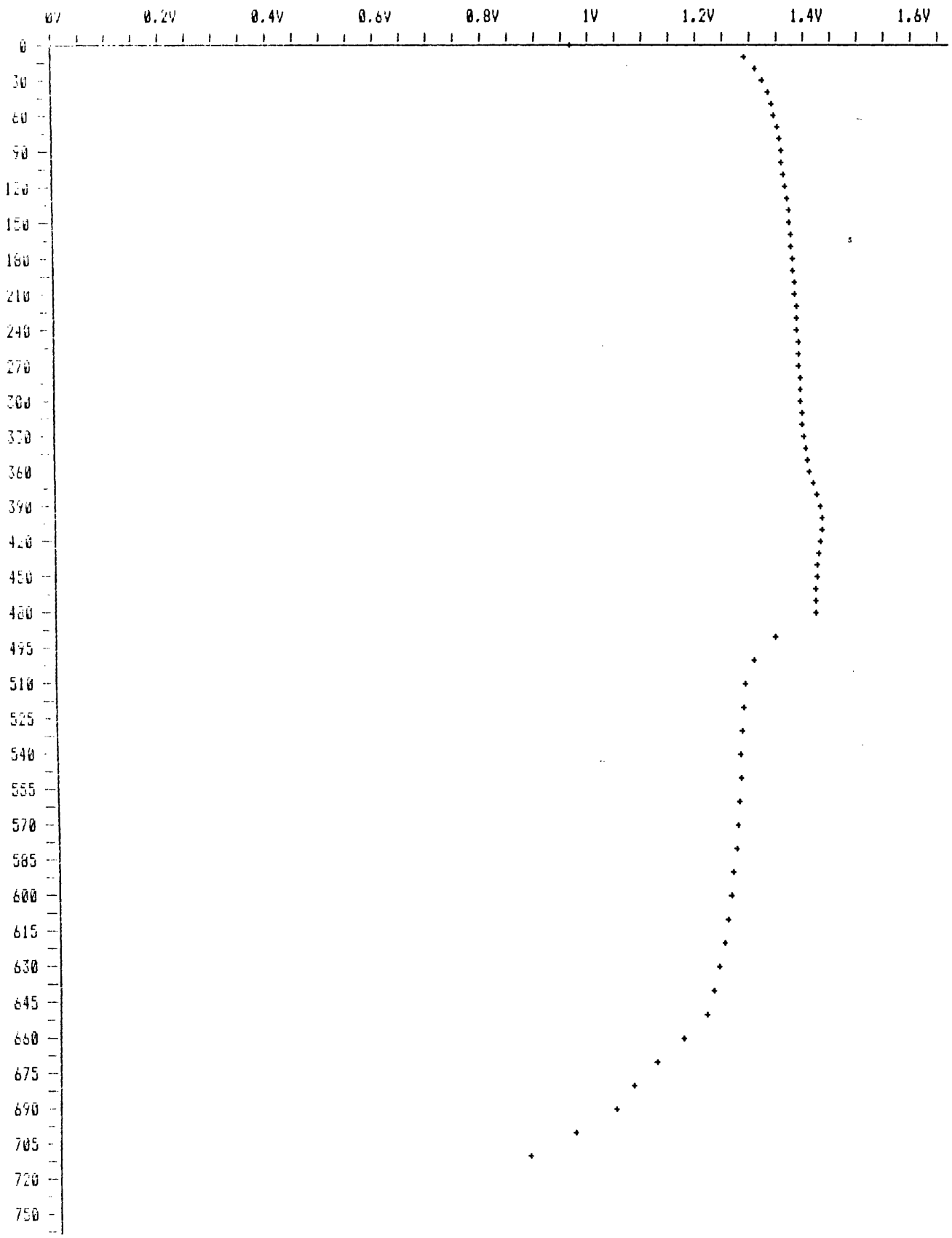

'RUN 16' : Ch-D MODULE 5 containing "S5" : -100±4 E.S.CONDUCTANCE PROFILES at 2Hz
10S
20S
30S
40S
50S
60S
70S
80S
90S
100S
110S
120S
0
60
120
240
300
360
420
480
510
540
570
600
630
660
690
720
780
840
900
960
1020
1080
1140
1200
1230
1260
1290
1320
1350
1380
1410
1440
1470

Graph 3(a)


"RUN 103" : Ch-b MODULE 0 containing "S10" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 3(D)

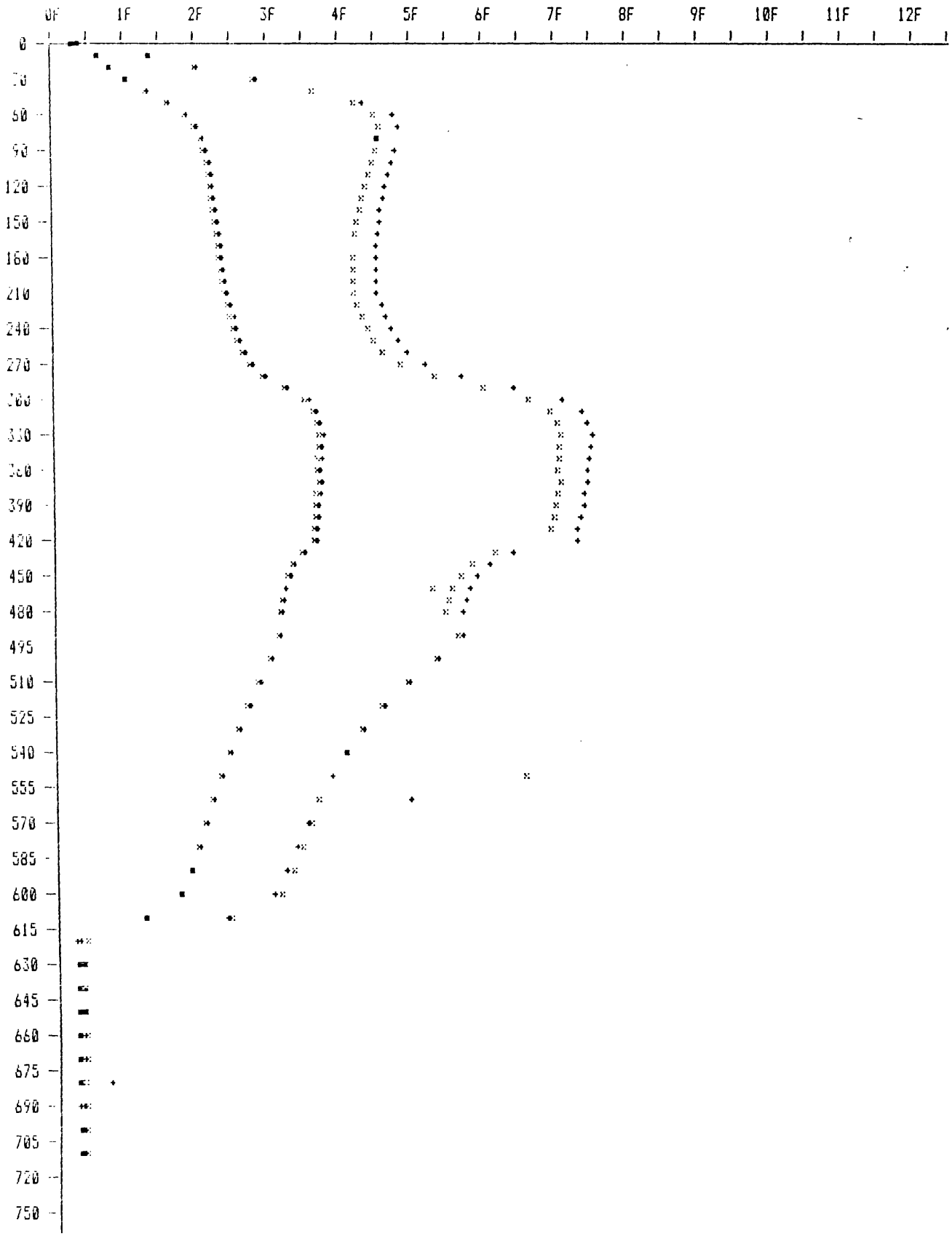
"RUN 108" : CH-D SPECIAL MODULE containing "SF1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 3(c)

Note: Curve order is 8Hz pair >>> 2Hz pair

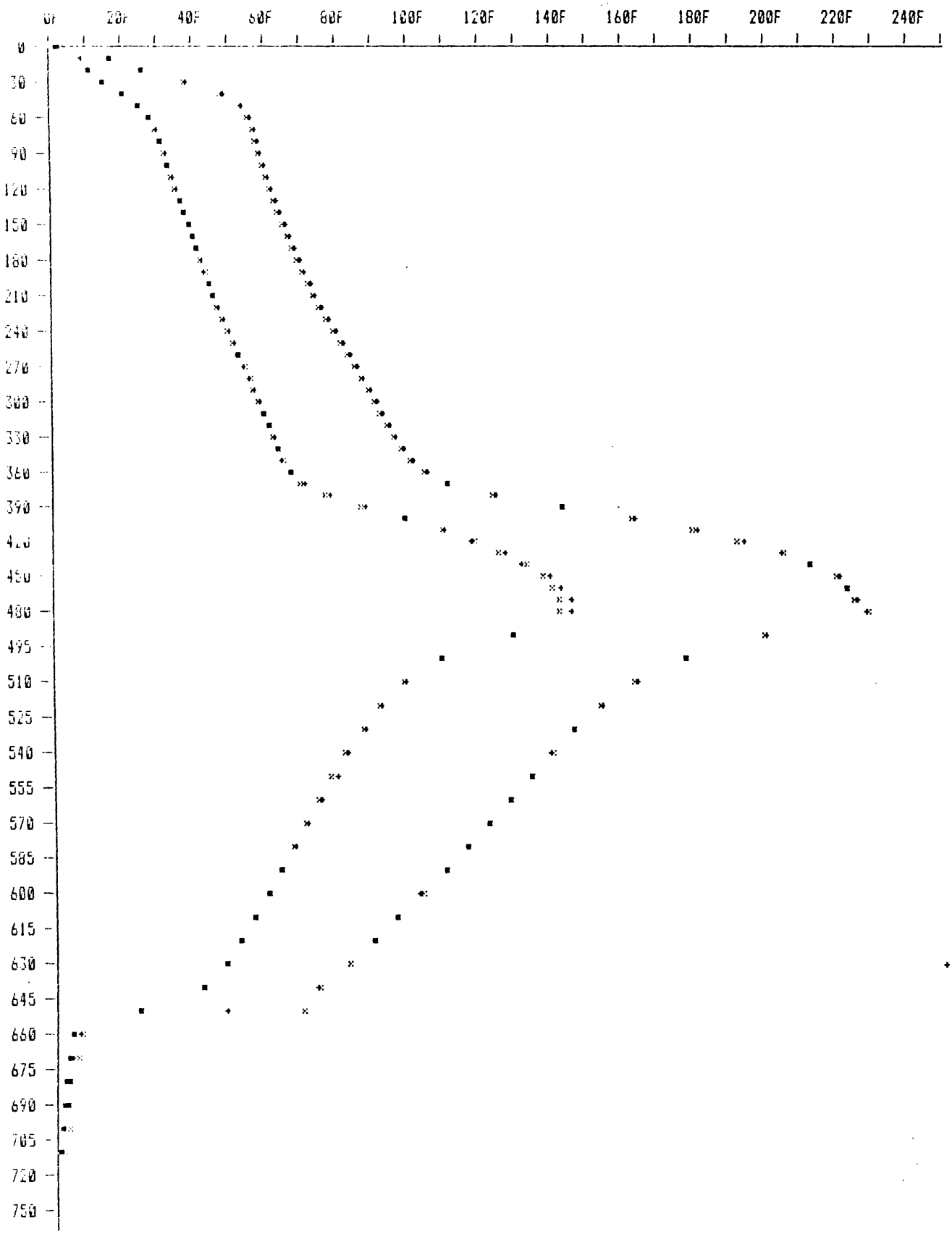
ROW 105" : CH-D MODULE 0 containing "S10" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(a)

Note: Curve order is 8Hz pair >>> 2Hz pair

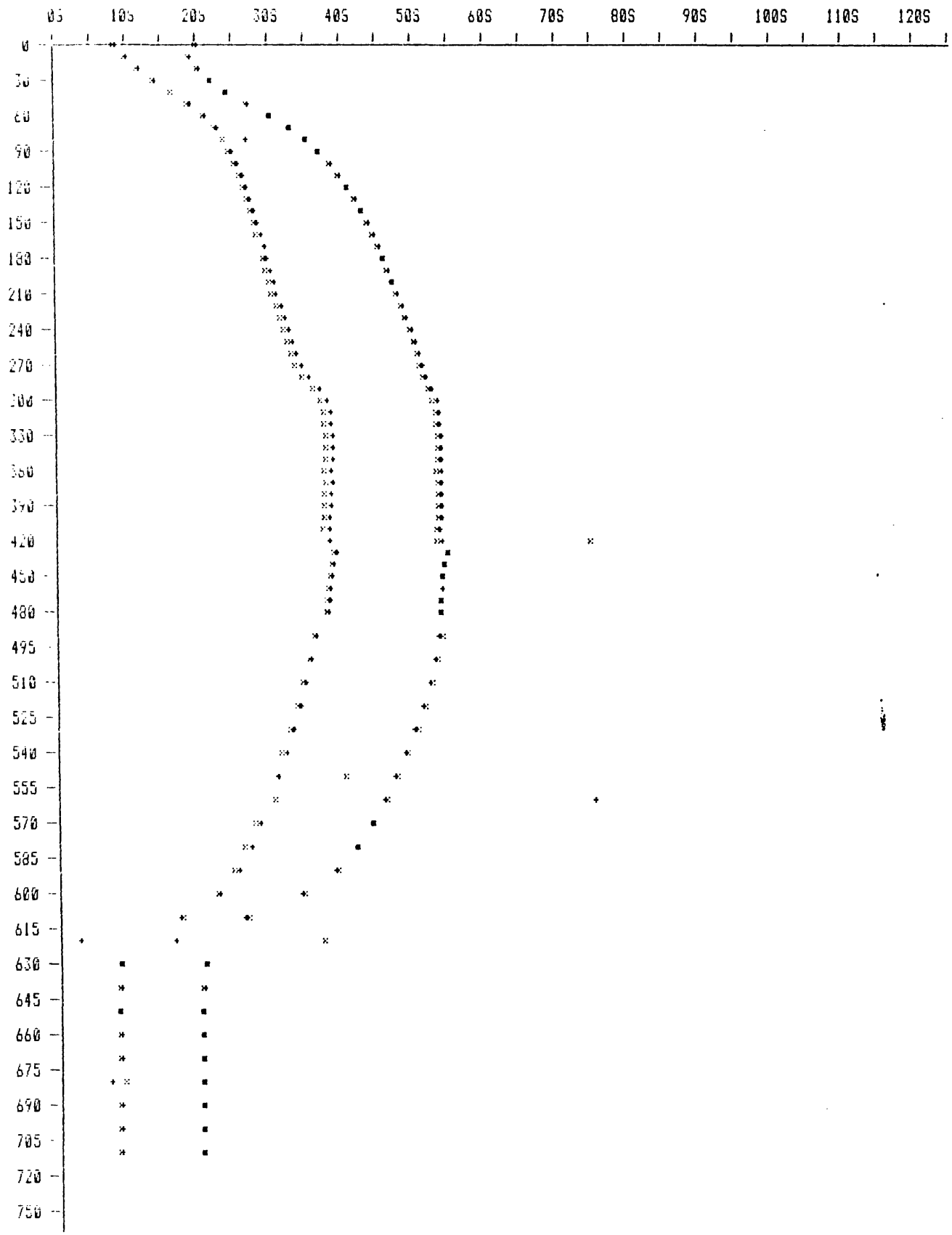
"RUN 108" : Cm-D SPECIAL MODULE containing "SF1" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(e)

Note: Curve order is 2Hz pair >>> 8Hz pair

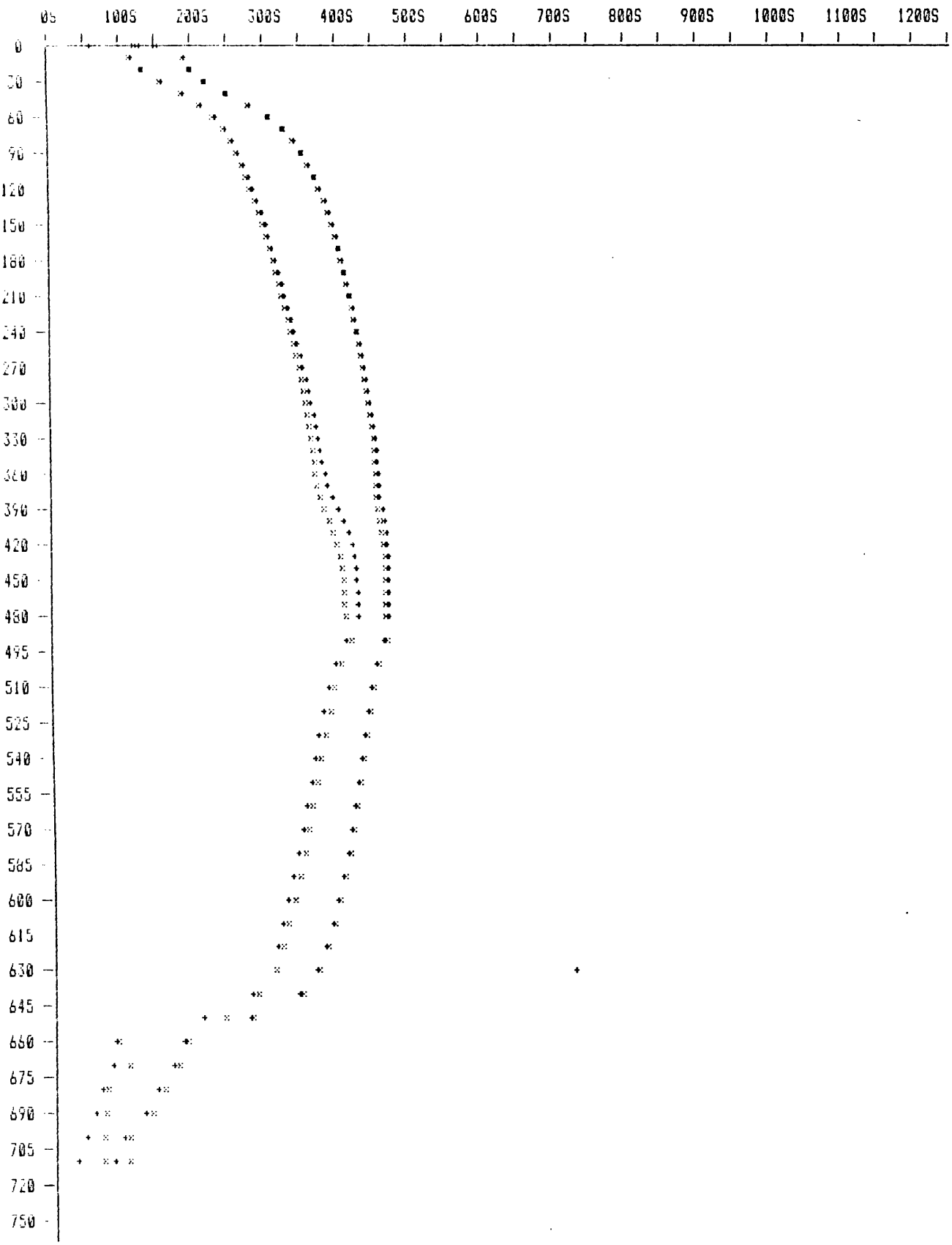
"RUN 108" : Ch-D NODULE 0 containing "S10" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(I)

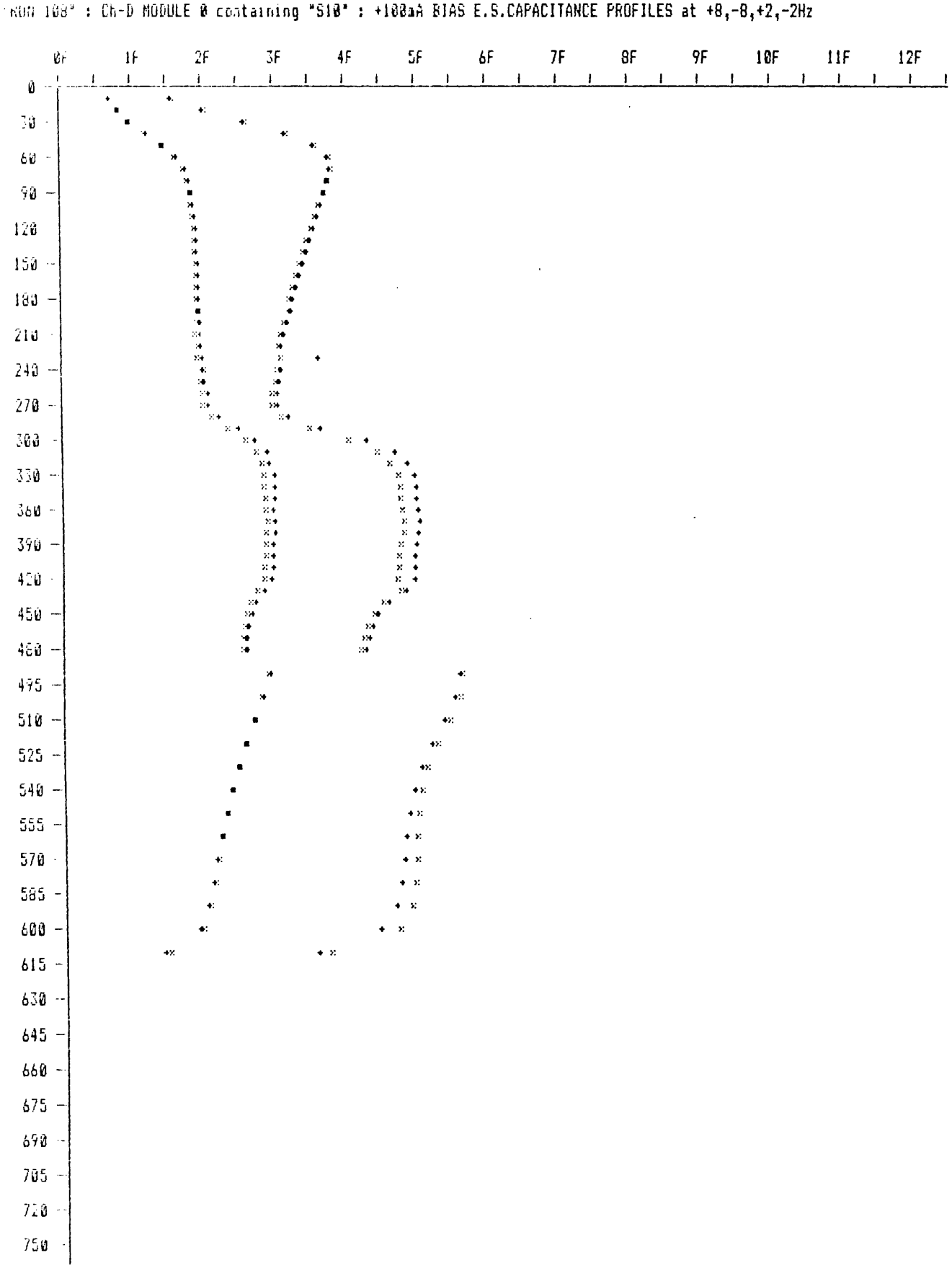
Note: Curve order is 2Hz pair >>> 8Hz pair

"RUN 108" : Ch-D SPECIAL MODULE containing 'SF1' : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



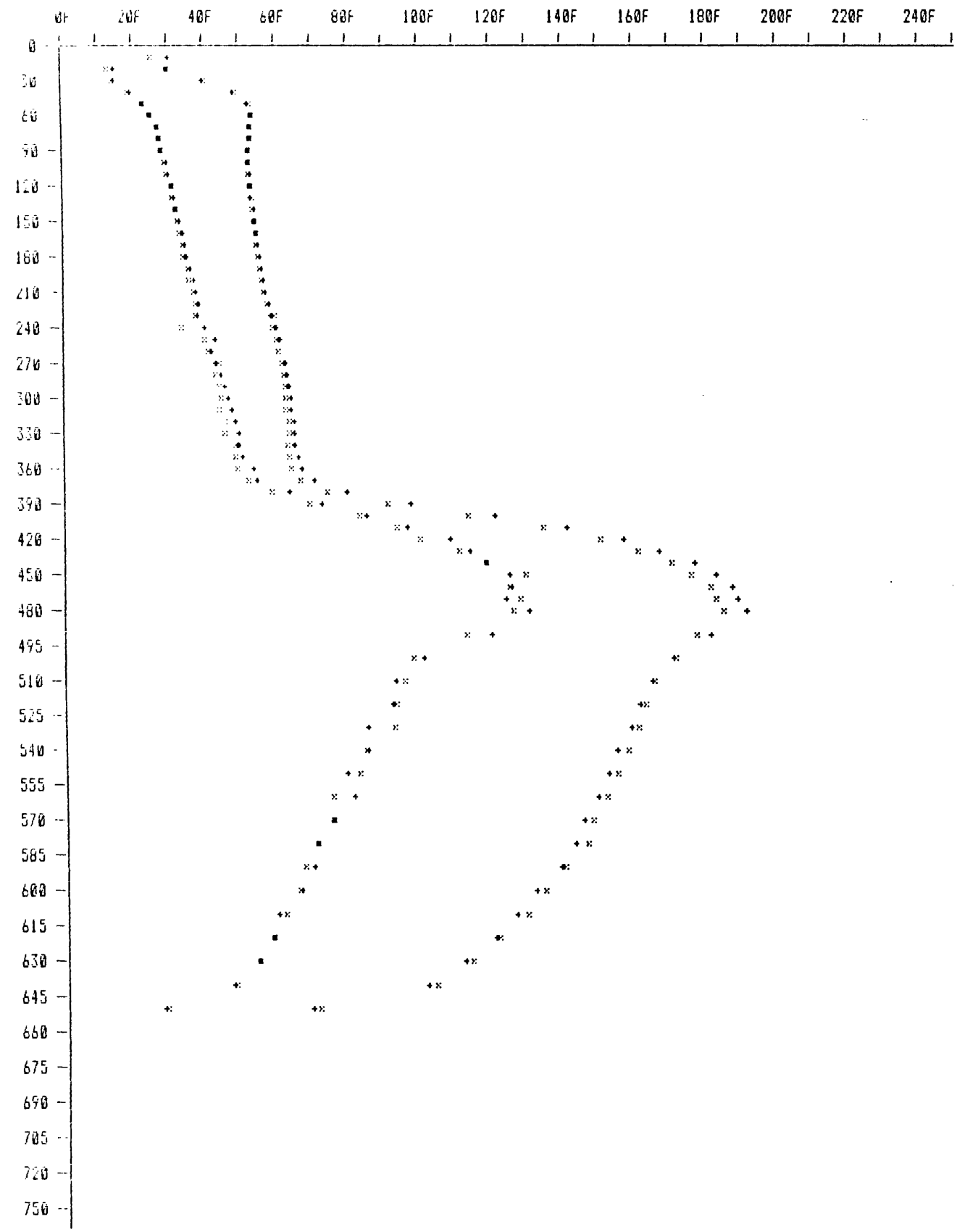
Graph 5(g)

Note: Curve order is 8Hz pair >>> 2Hz pair



Graph 3(H)

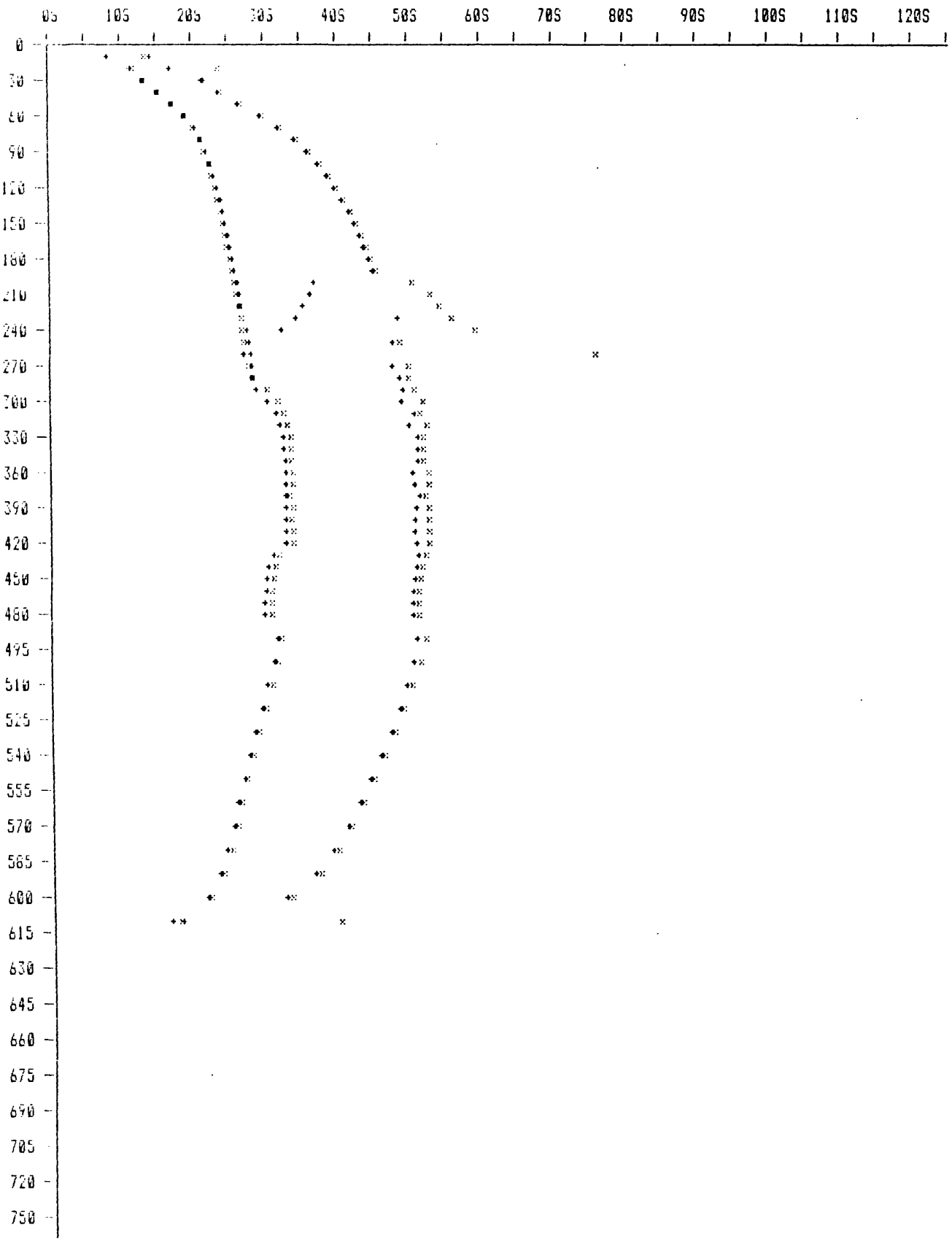
Note: Curve order is 8Hz pair >>> 2Hz pair



Graph 3(1)

Note: Curve order is 2Hz pair >>> 8Hz pair

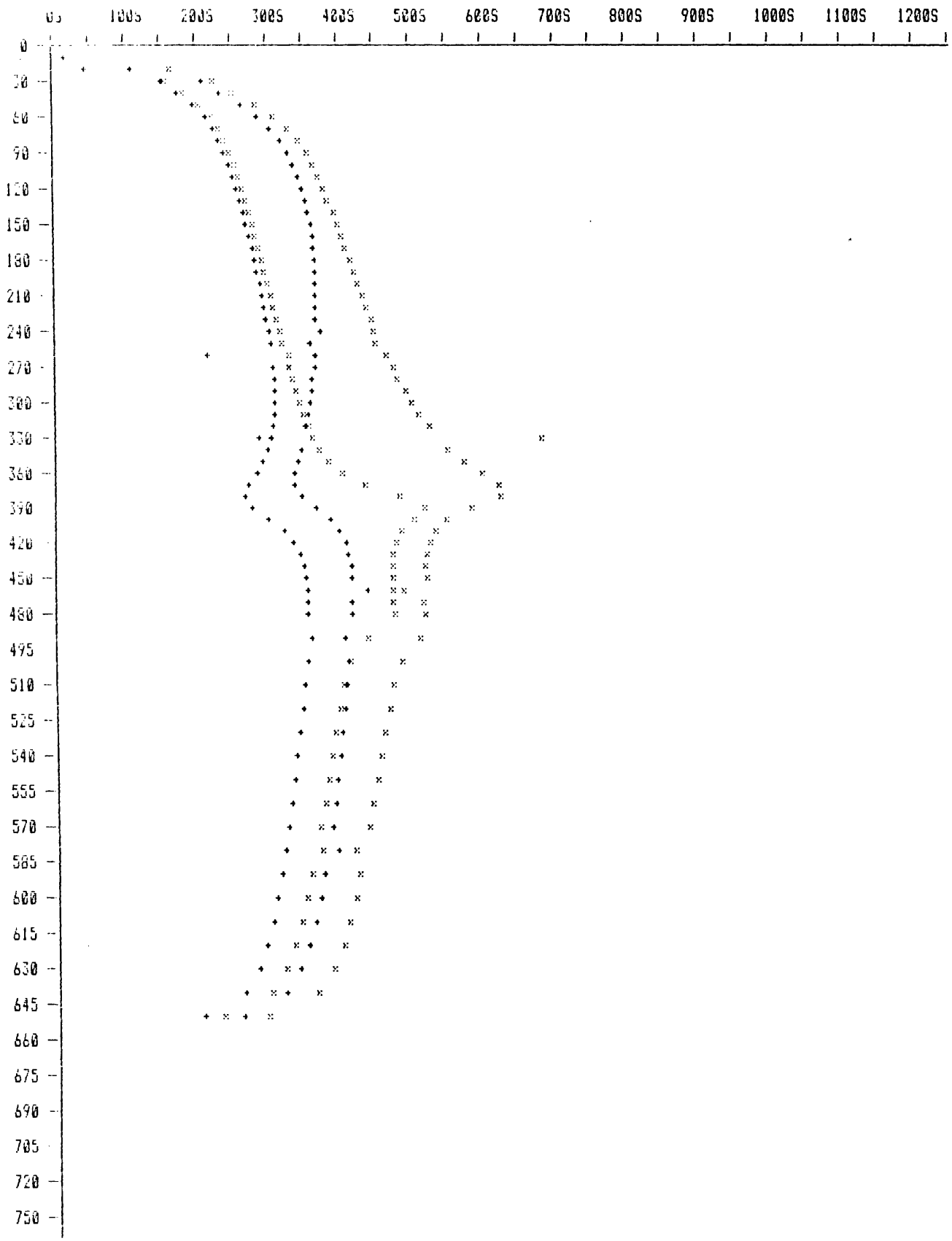
"RUN 108" : Ch-D MODULE 0 containing "S18" : +108aA E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(ii)

Note: Curve order is 2Hz pair >>> 8Hz pair

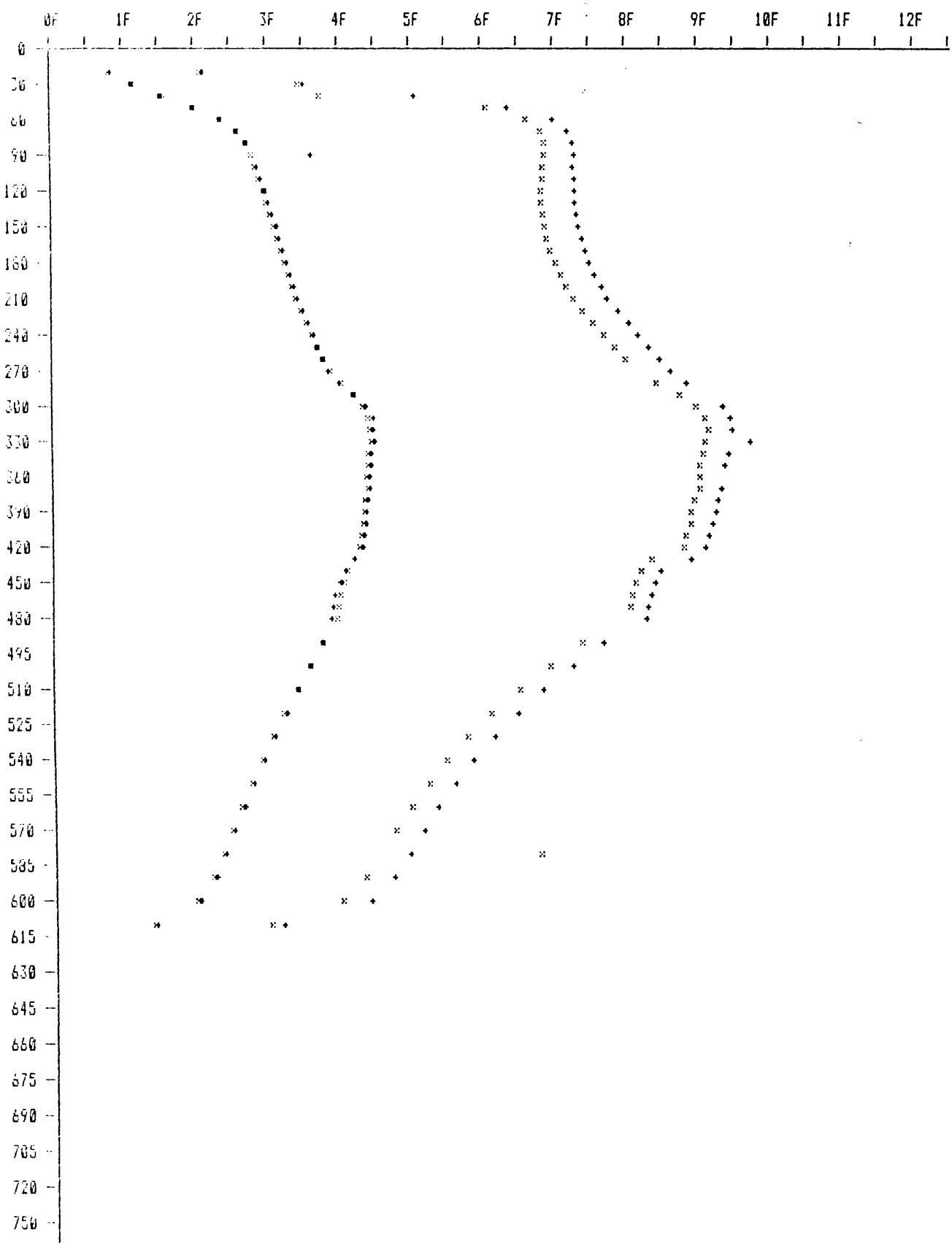
"RUN 108" : Ch-D SPECIAL MODULE containing "SF1" : +1400uA E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(K)

Note: Curve order is 8Hz pair >>> 2Hz pair

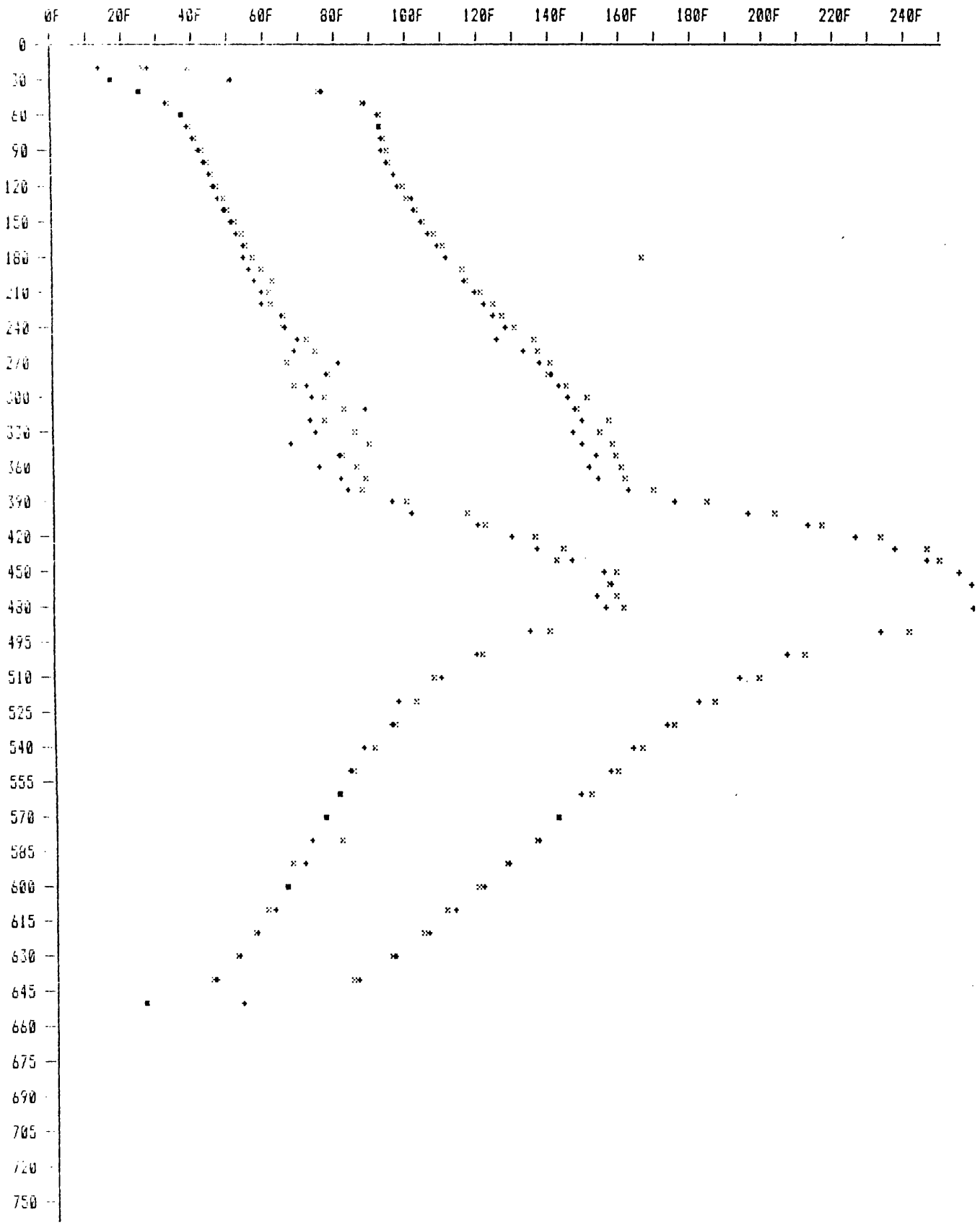
"RUN 103" : Ch-D MODULE 0 containing "S10" : -100aA BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(1)

Note: Curve order is 8Hz pair >>> 2Hz pair

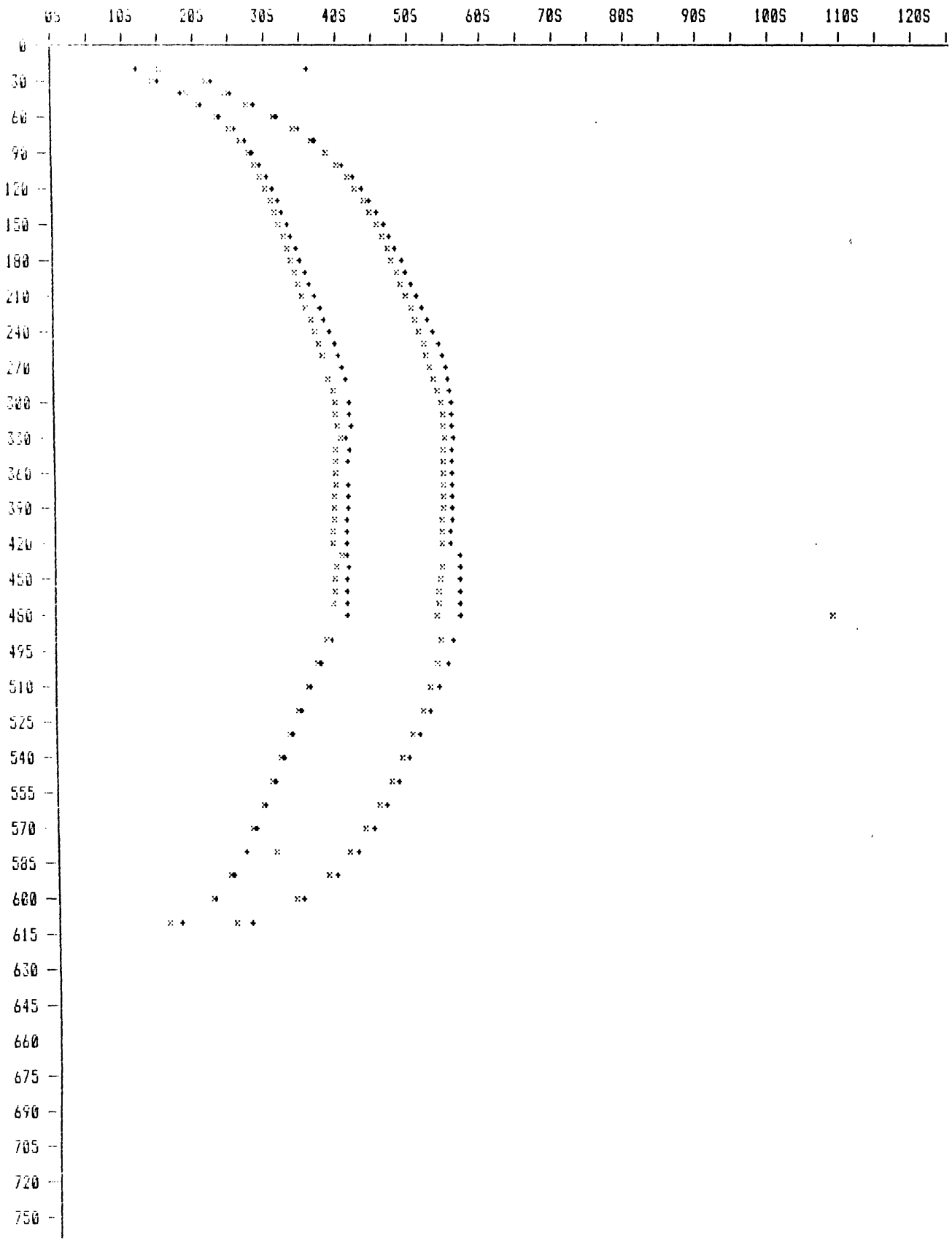
"RUN 168" : Ch-D SPECIAL MODULE containing "SF1" : -1400aA BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 5(m)

Note: Curve order is 2Hz pair >>> 8Hz pair

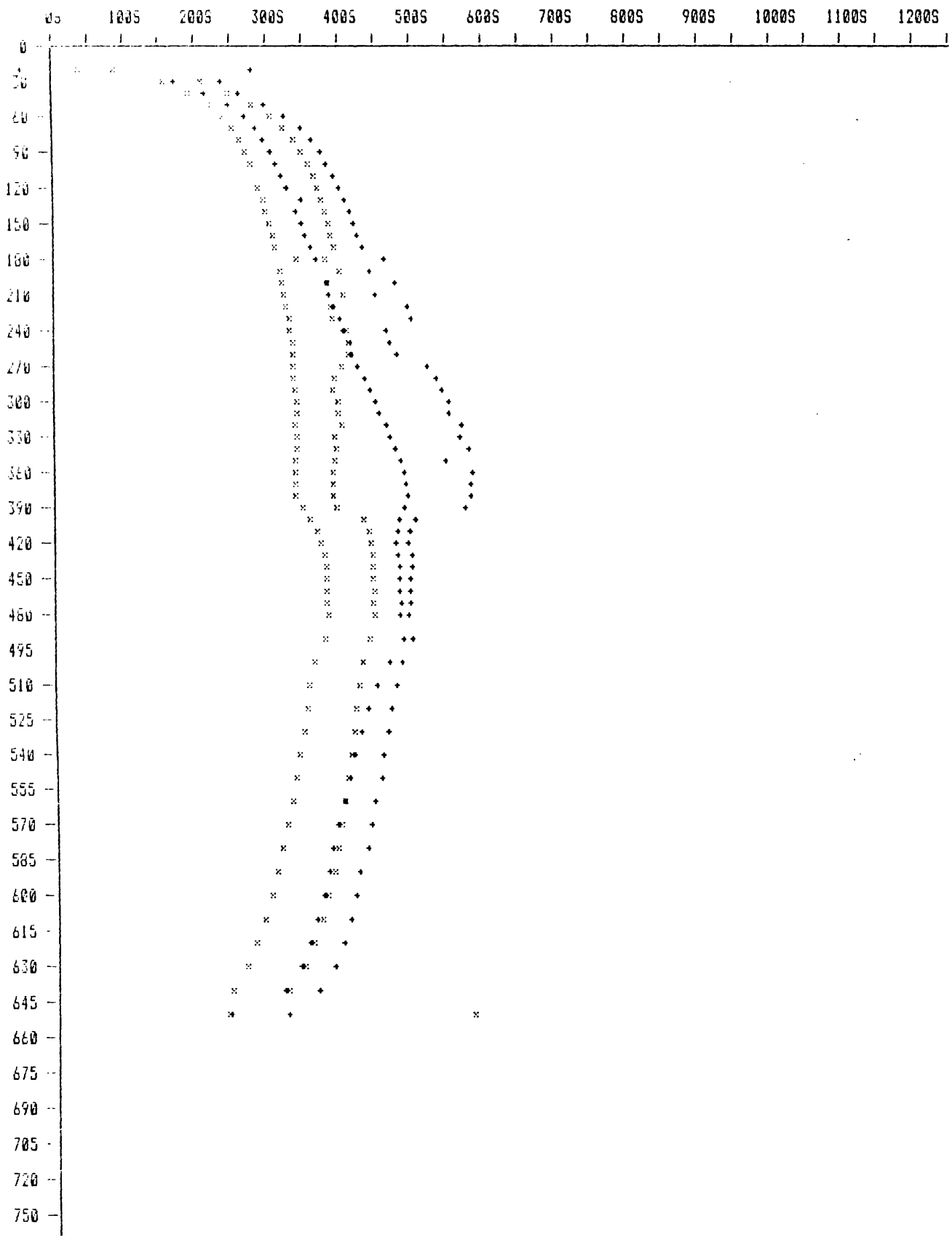
"ROW 106" : Ch-D MODULE 0 containing "S10" : -100sA E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(a)

Note: Curve order is 2Hz pair >>> 8Hz pair

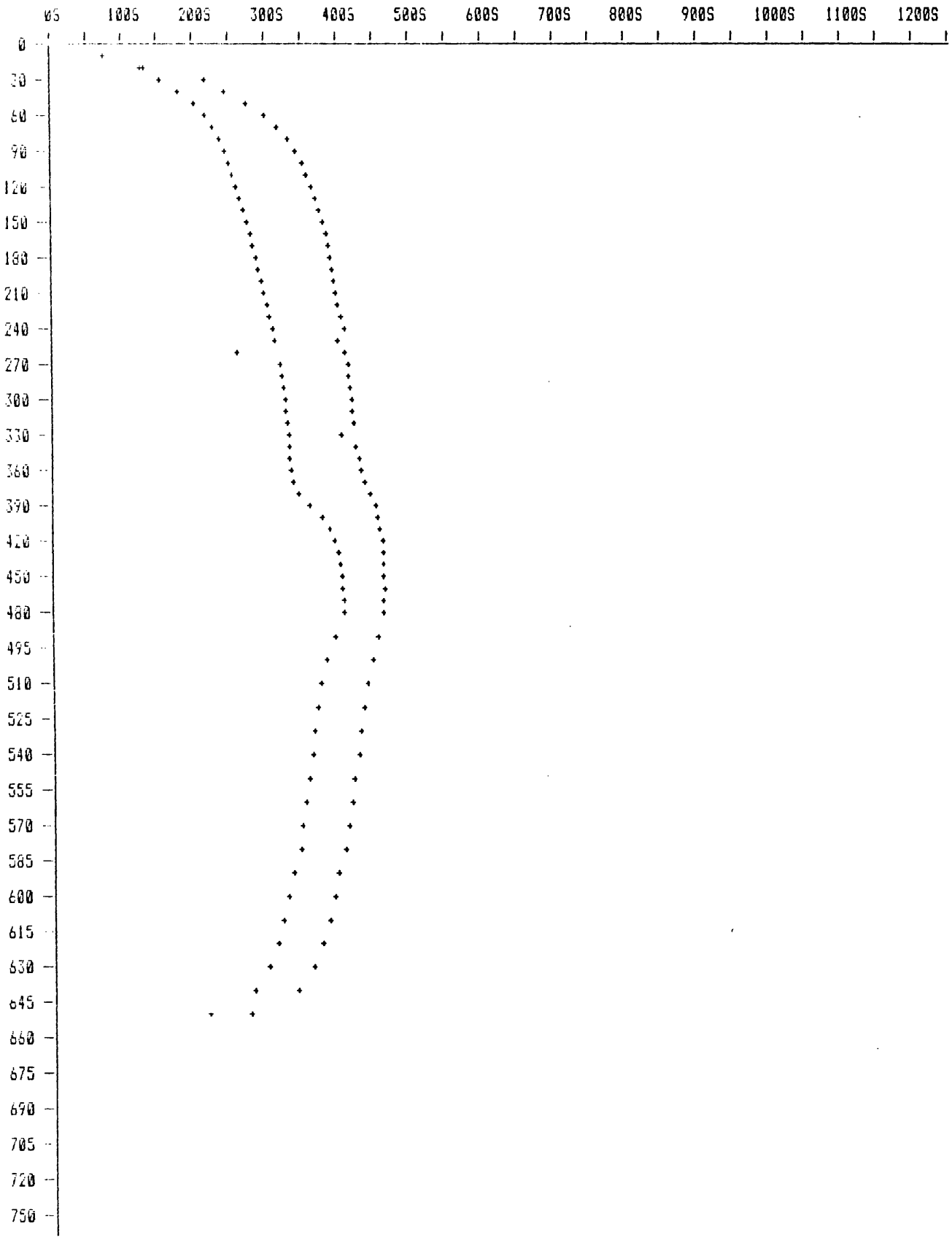
"RUN 138" : Ch-D SPECIAL MODULE containing "SF1" : -1400aA E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(3)

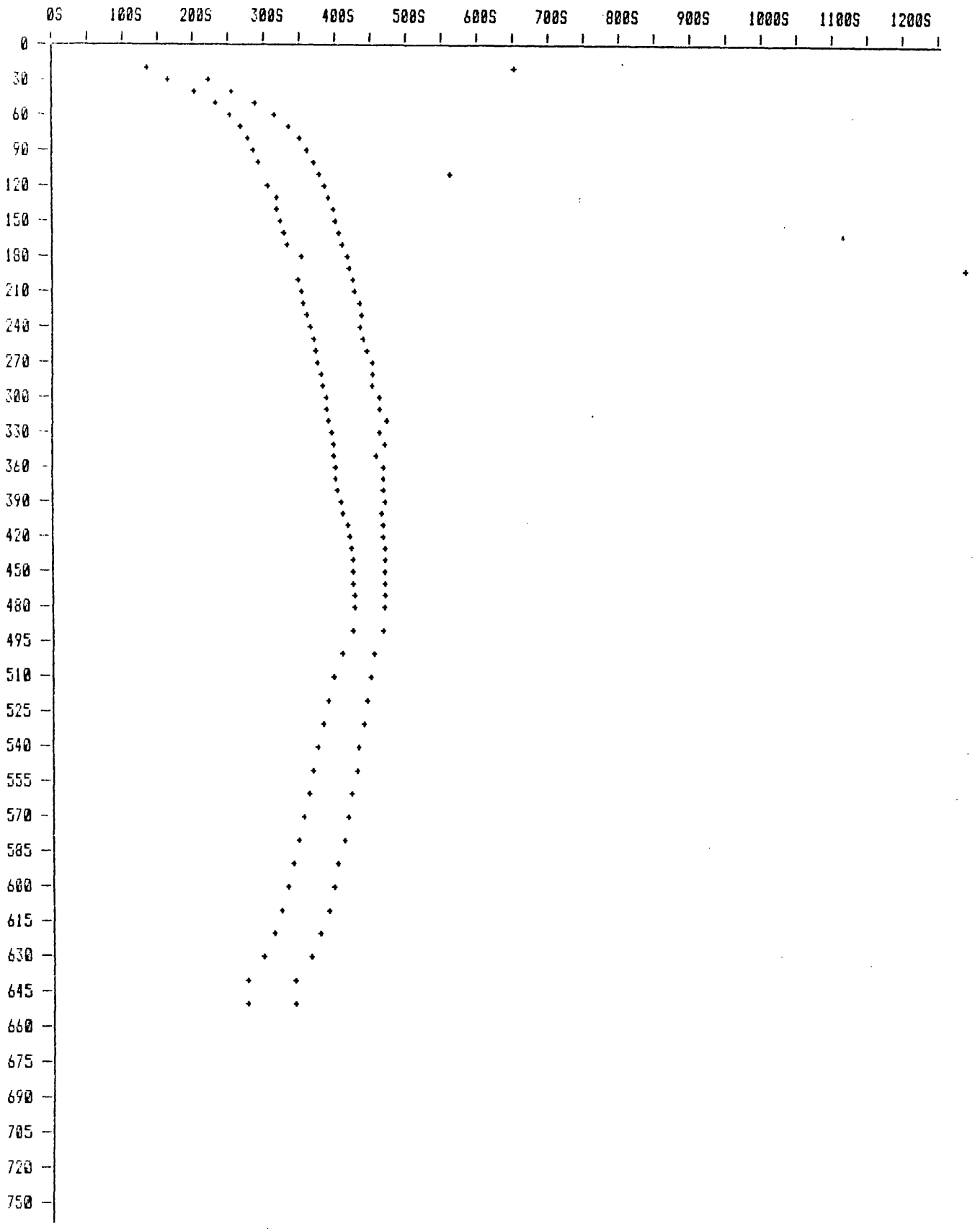
Note: Curve order is 2Hz >>> 8Hz

"RUN 103" : Ch-D SPECIAL MODULE containing "SF1" : +1400mA bias E.S.CONDUCTANCE AVERAGED FOR +/- MEASUREMENTS

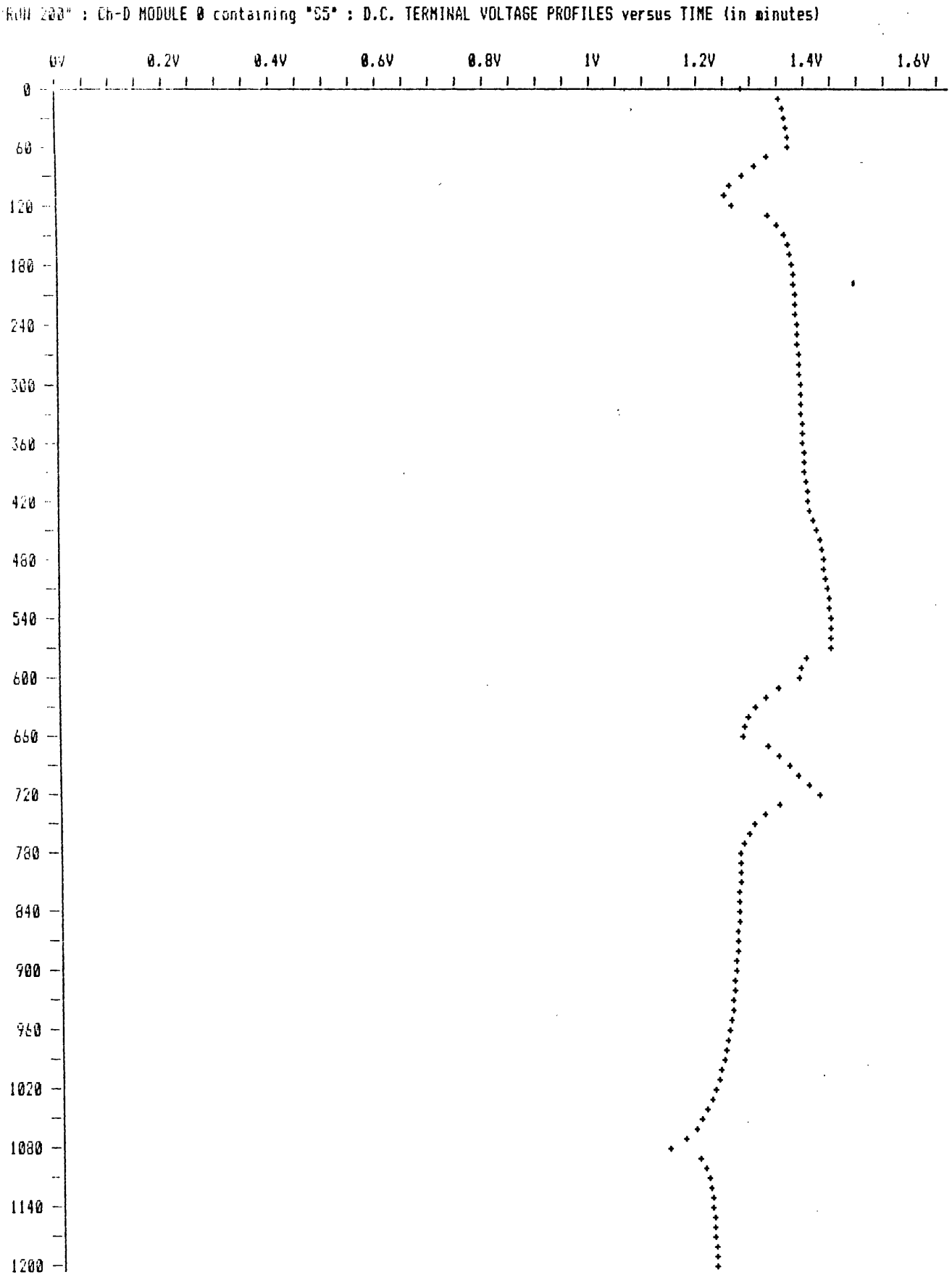


Note: Curve order is 2Hz >>> 8Hz

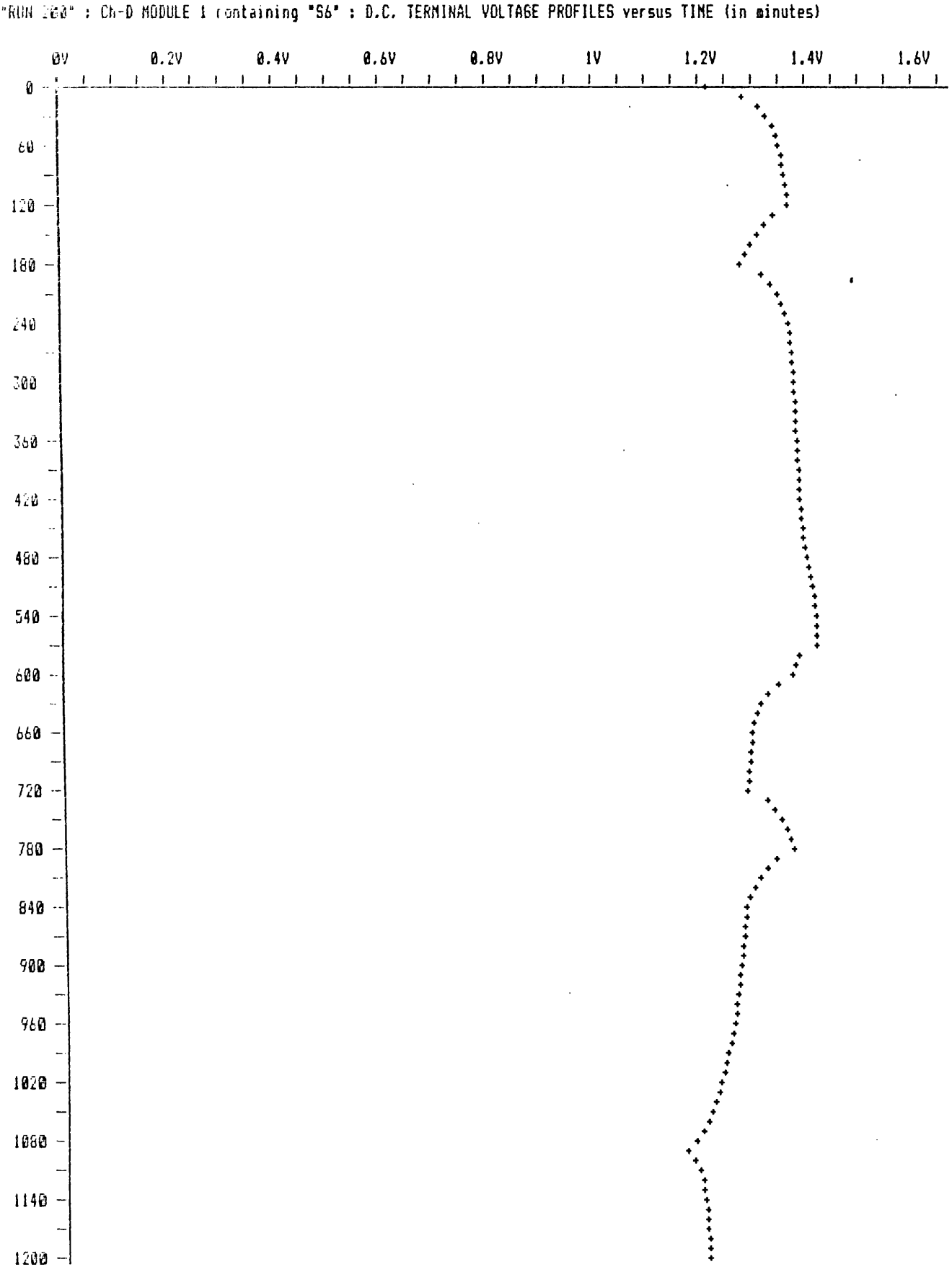
"RUN 108" : Ch-D SPECIAL MODULE containing "SF1" : -1400mA bias E.S.CONDUCTANCE AVERAGED FOR +/- MEASUREMENTS



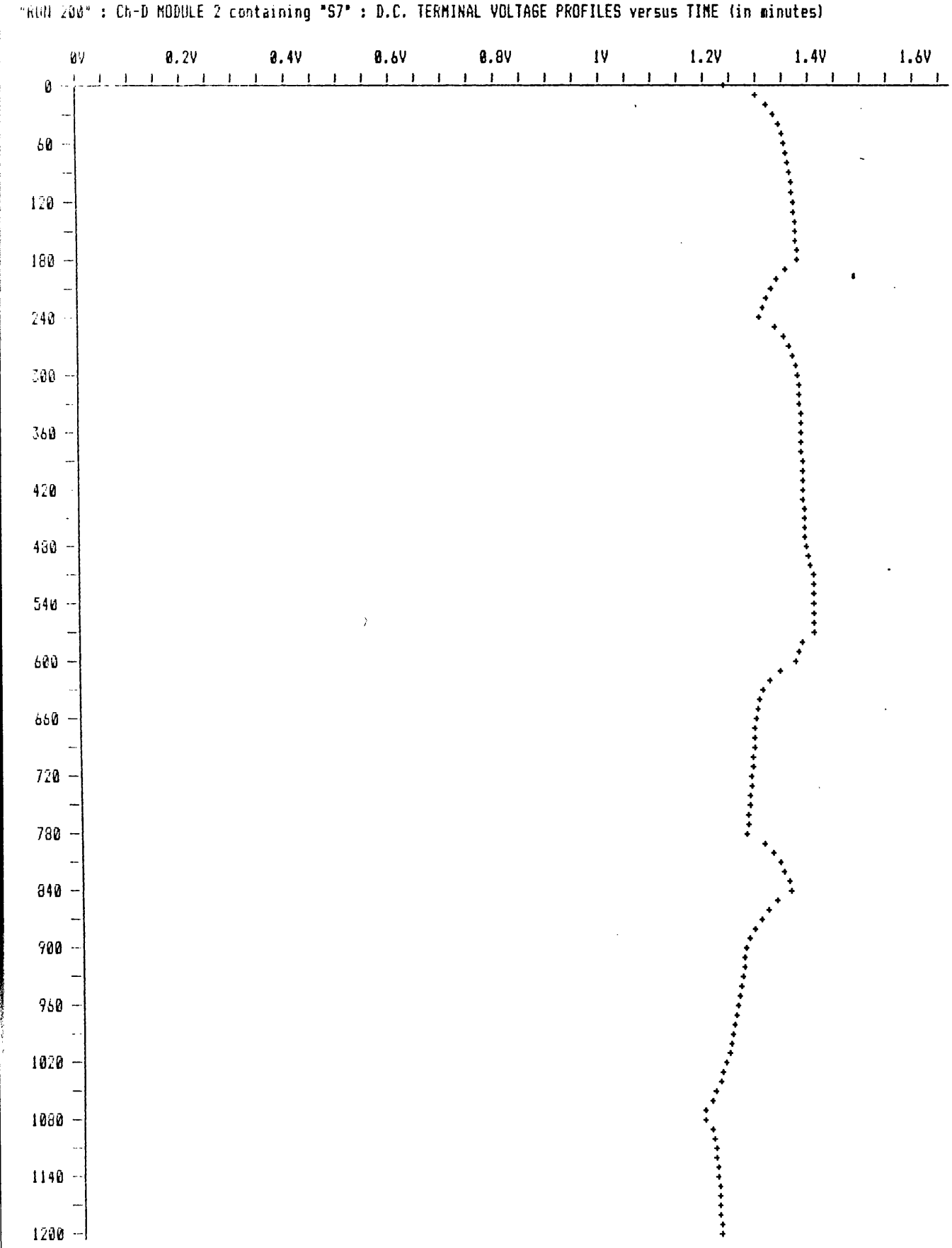
Graph 6(a)


RUN 200" : Ch-D MODULE 0 containing "S5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200

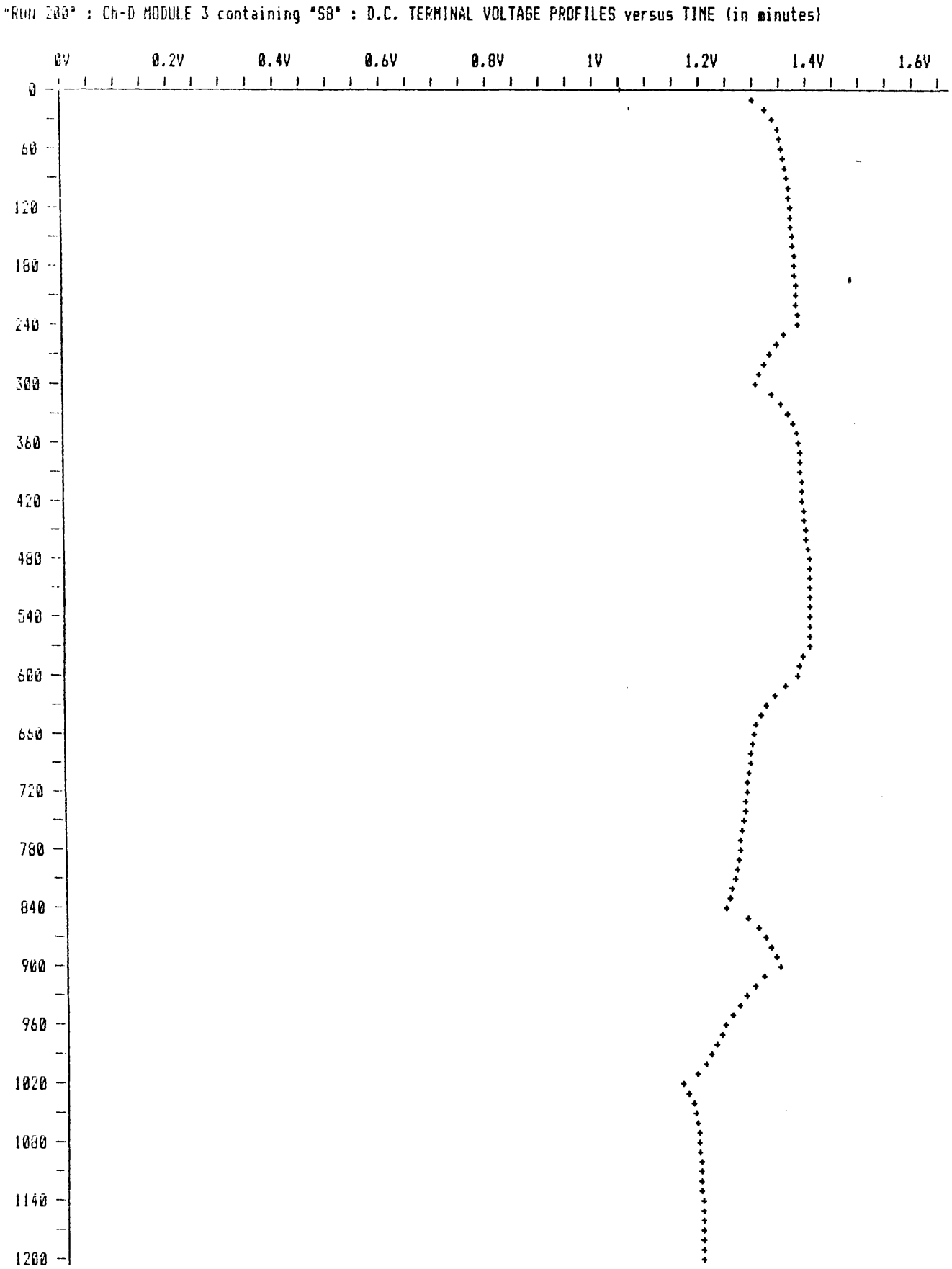
Graph 6(b)


"RUN 260" : Ch-D MODULE 1 containing "S6" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200

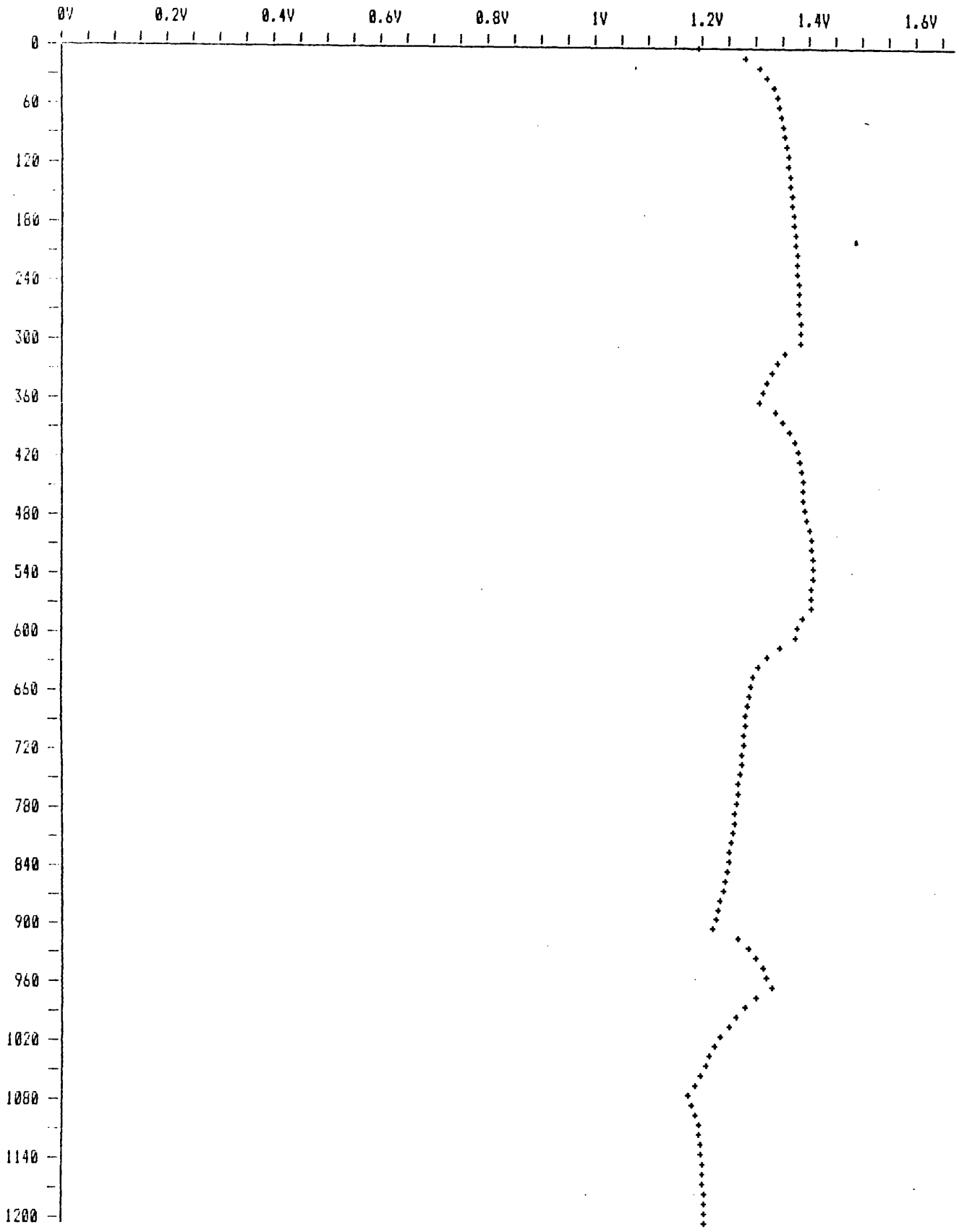
Graph 6(c)


"RUN 200" : Ch-D MODULE 2 containing "S7" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200

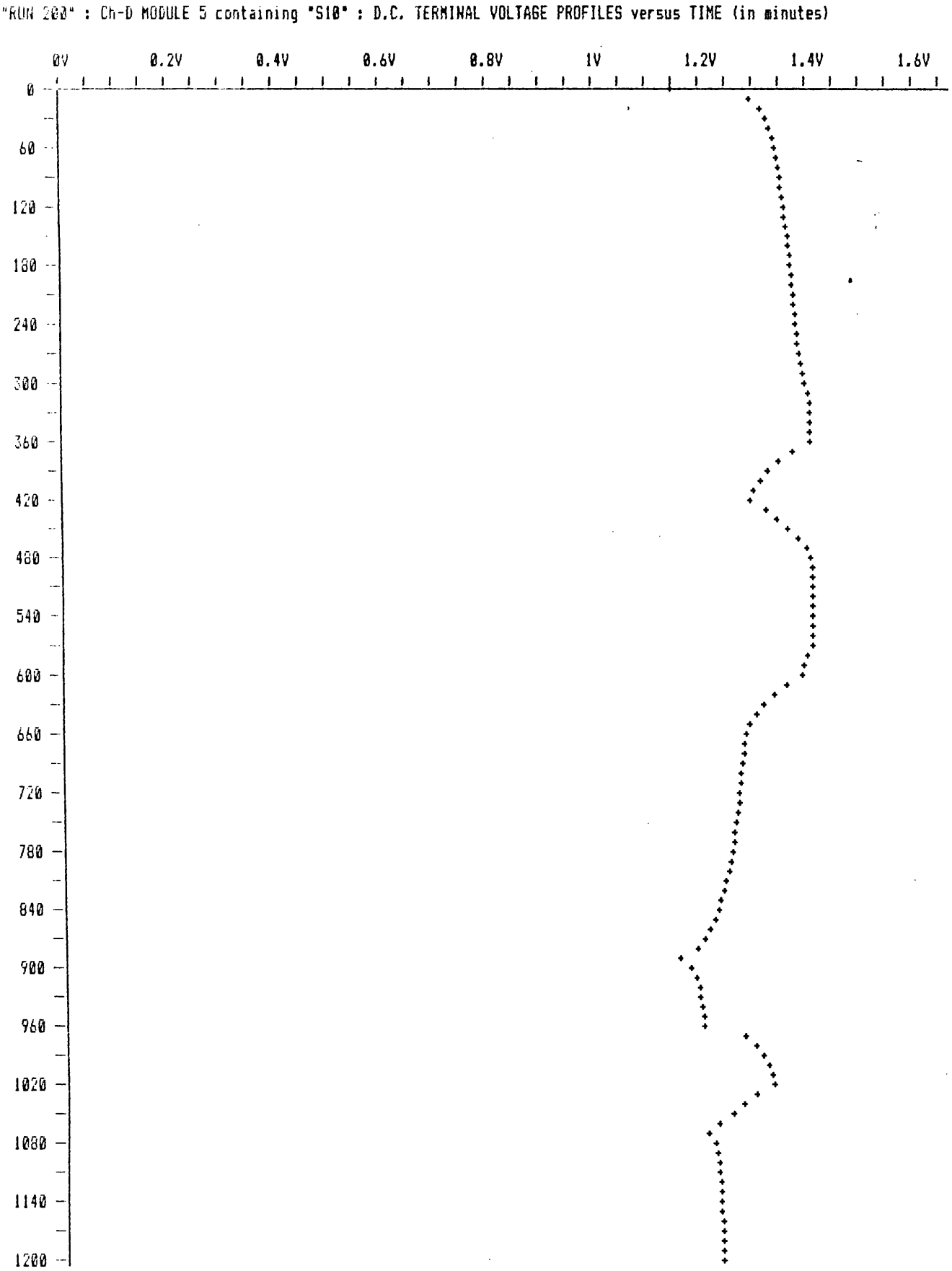
Graph 6(d)


"RUN 200" : Ch-D MODULE 3 containing "SB" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200

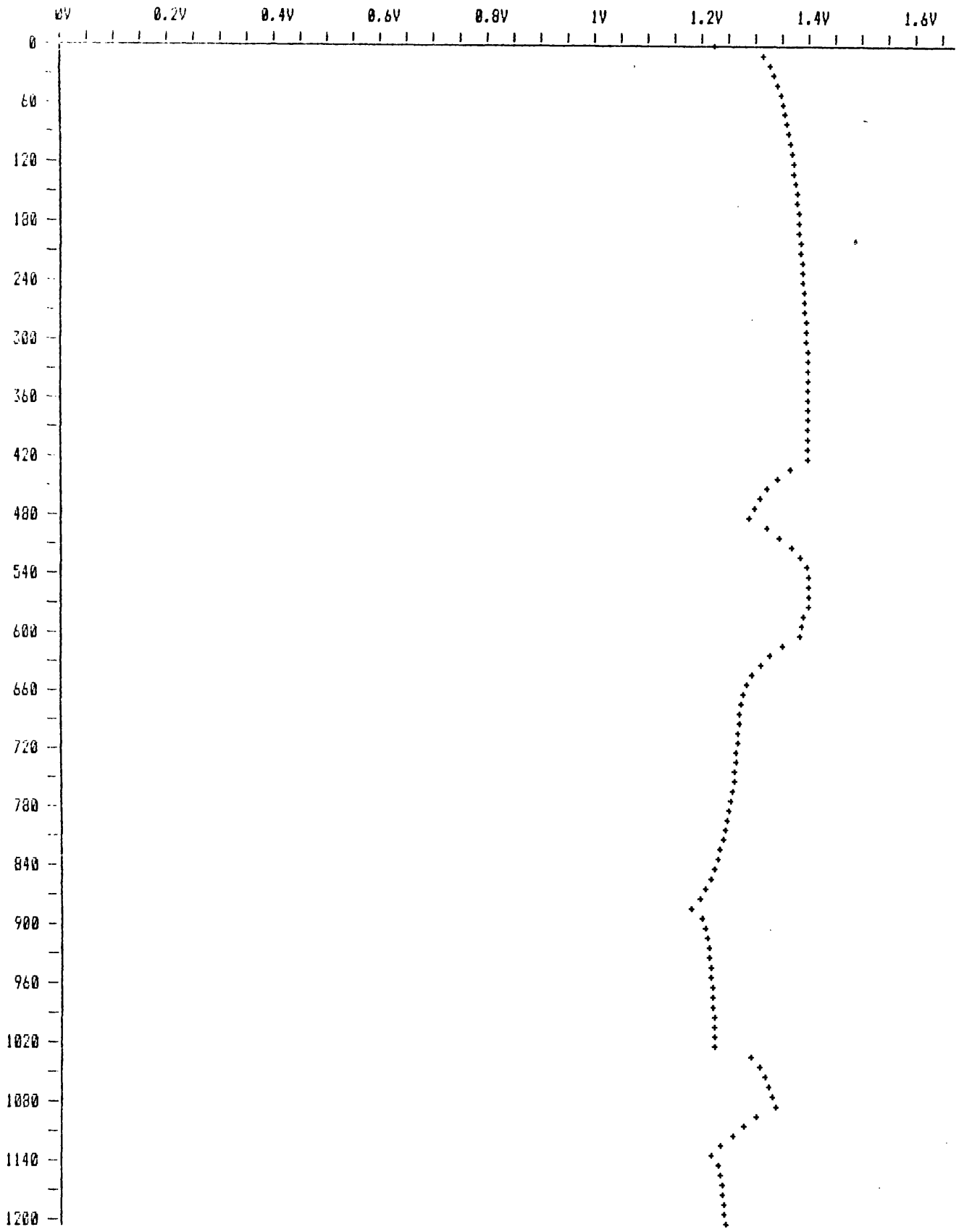
"RUN 200" : Ch-D MODULE 4 containing "S9" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 8(1)


"RUN 200" : Ch-D MODULE 5 containing "S10" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
60
120
180
240
300
360
420
480
540
600
660
720
780
840
900
960
1020
1080
1140
1200

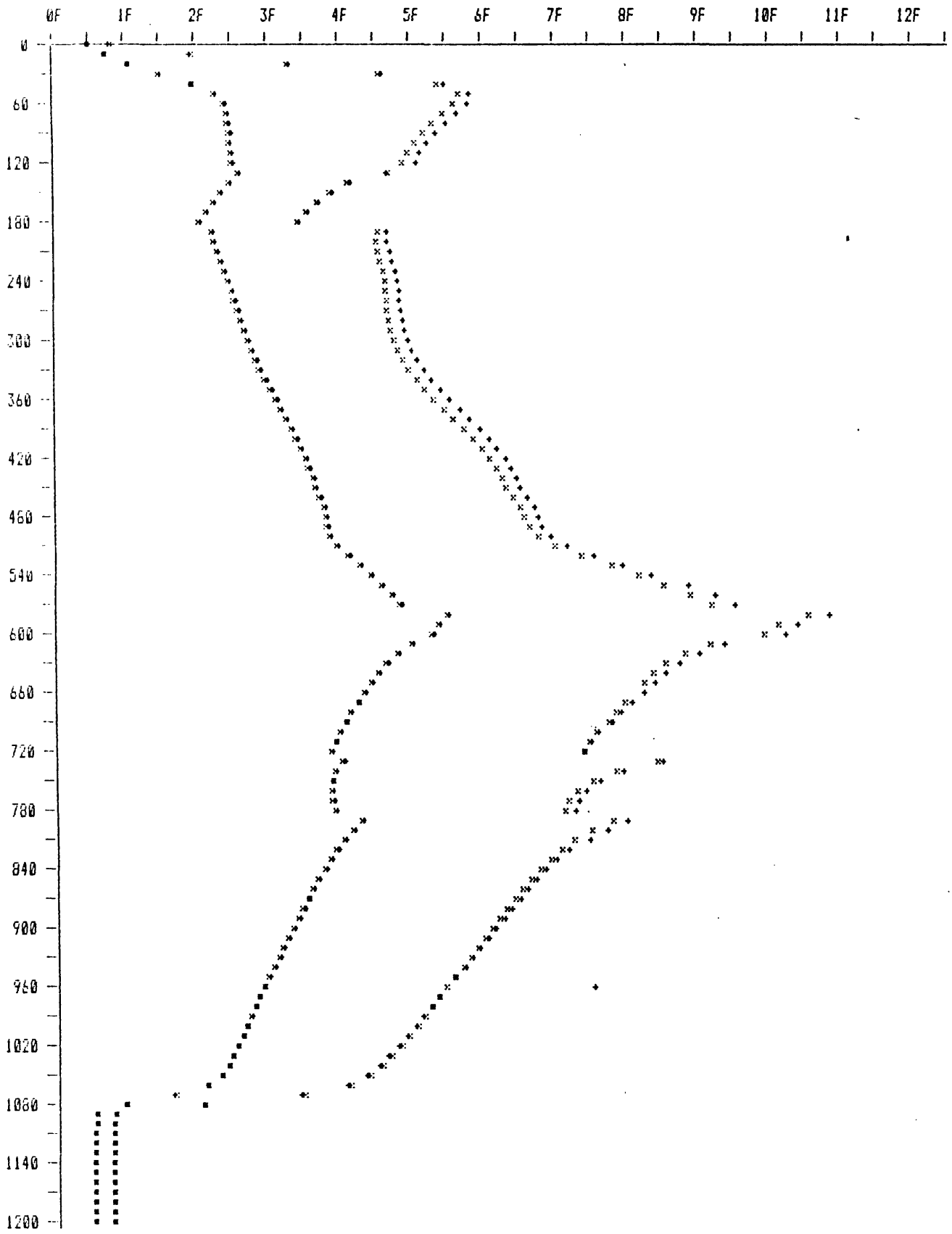
"RUN 203" : Ch-D MODULE 6 containing "S11" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 6(1)

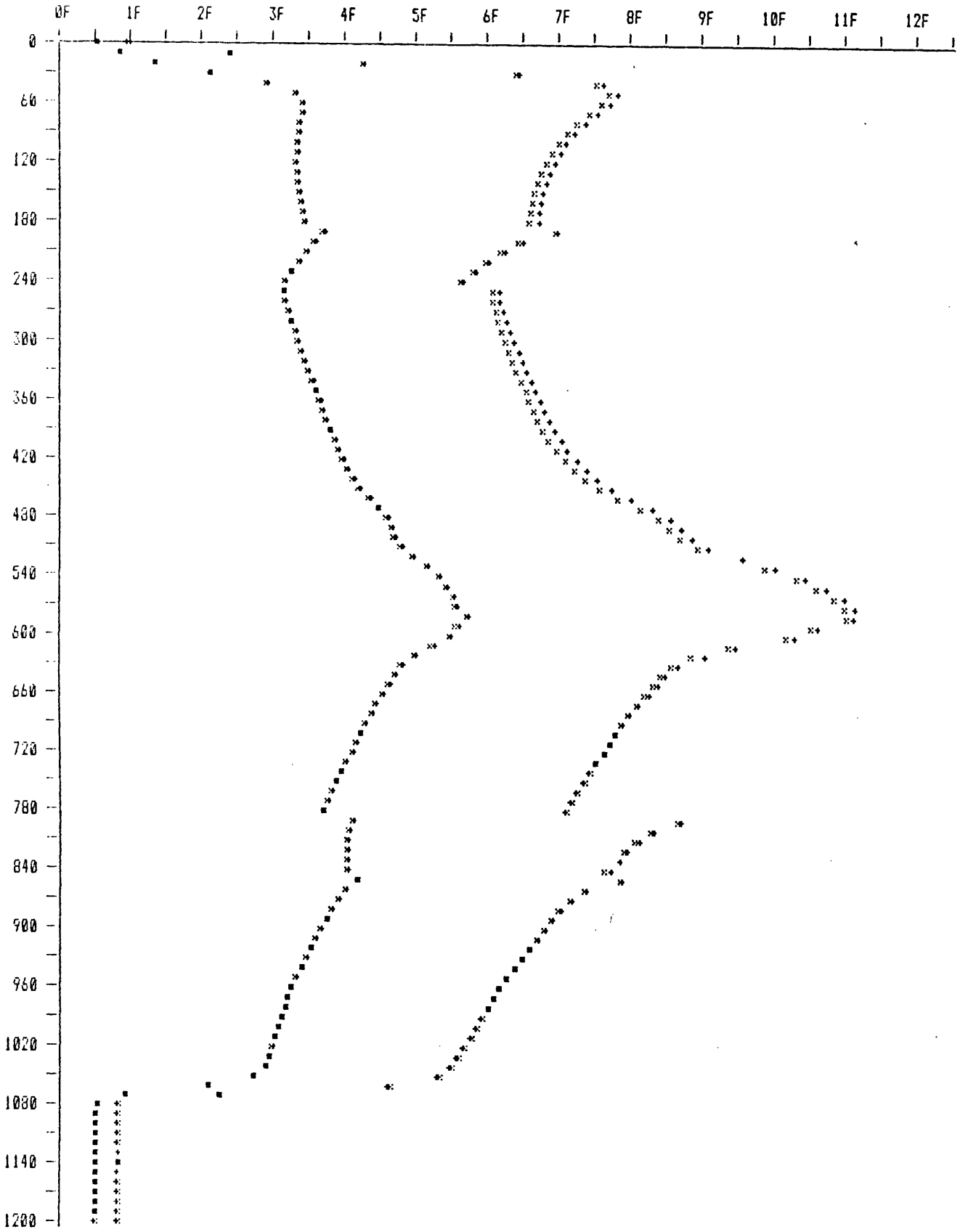
Note: Curve order is 8Hz pair >>> 2Hz pair

"RUN 200" : Ch-D MODULE 1 containing "S6" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Note: Curve order is 8Hz pair >>> 2Hz pair

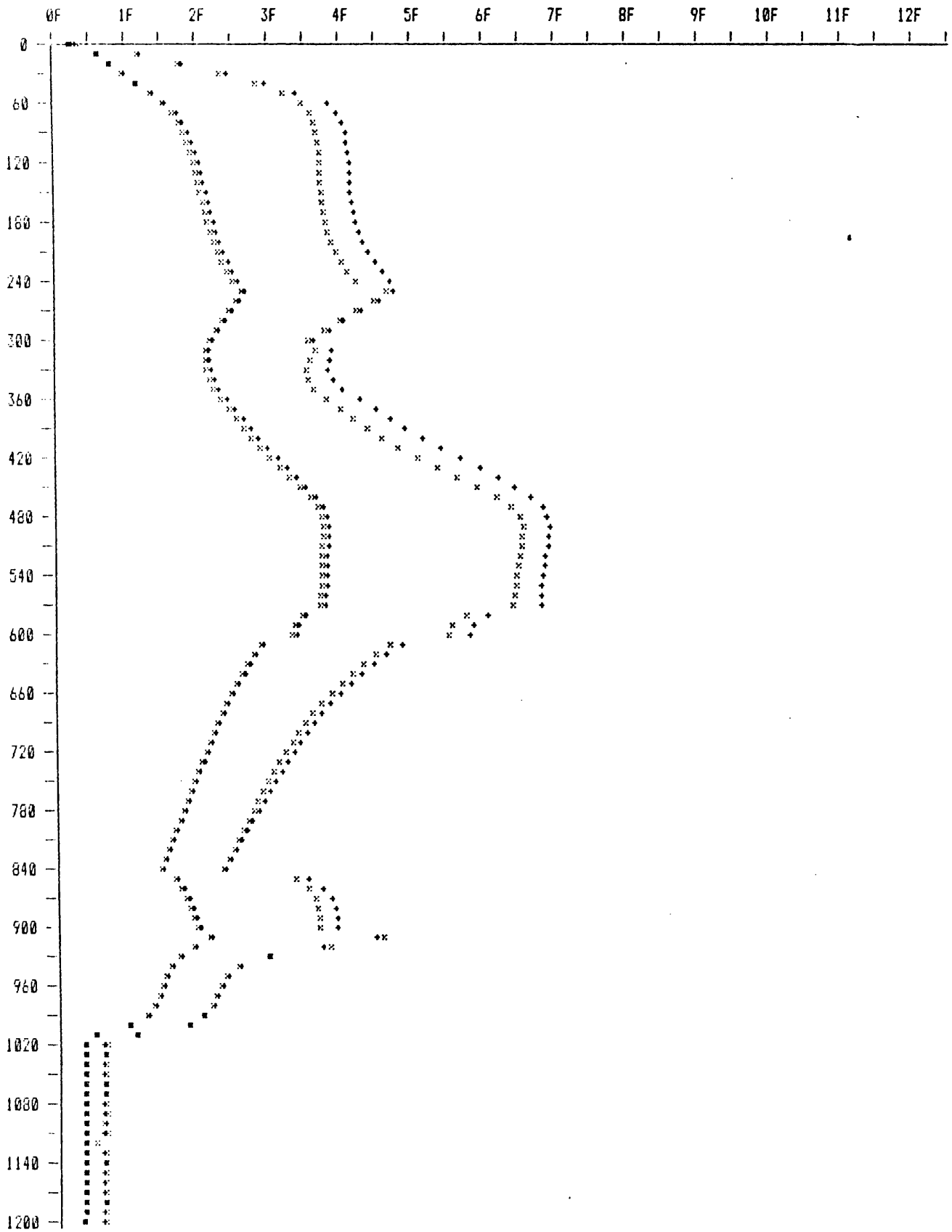
"RUN 200" : Ch-D MODULE 2 containing "S7" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 8(k)

Note: Curve order is 8Hz pair >>> 2Hz pair

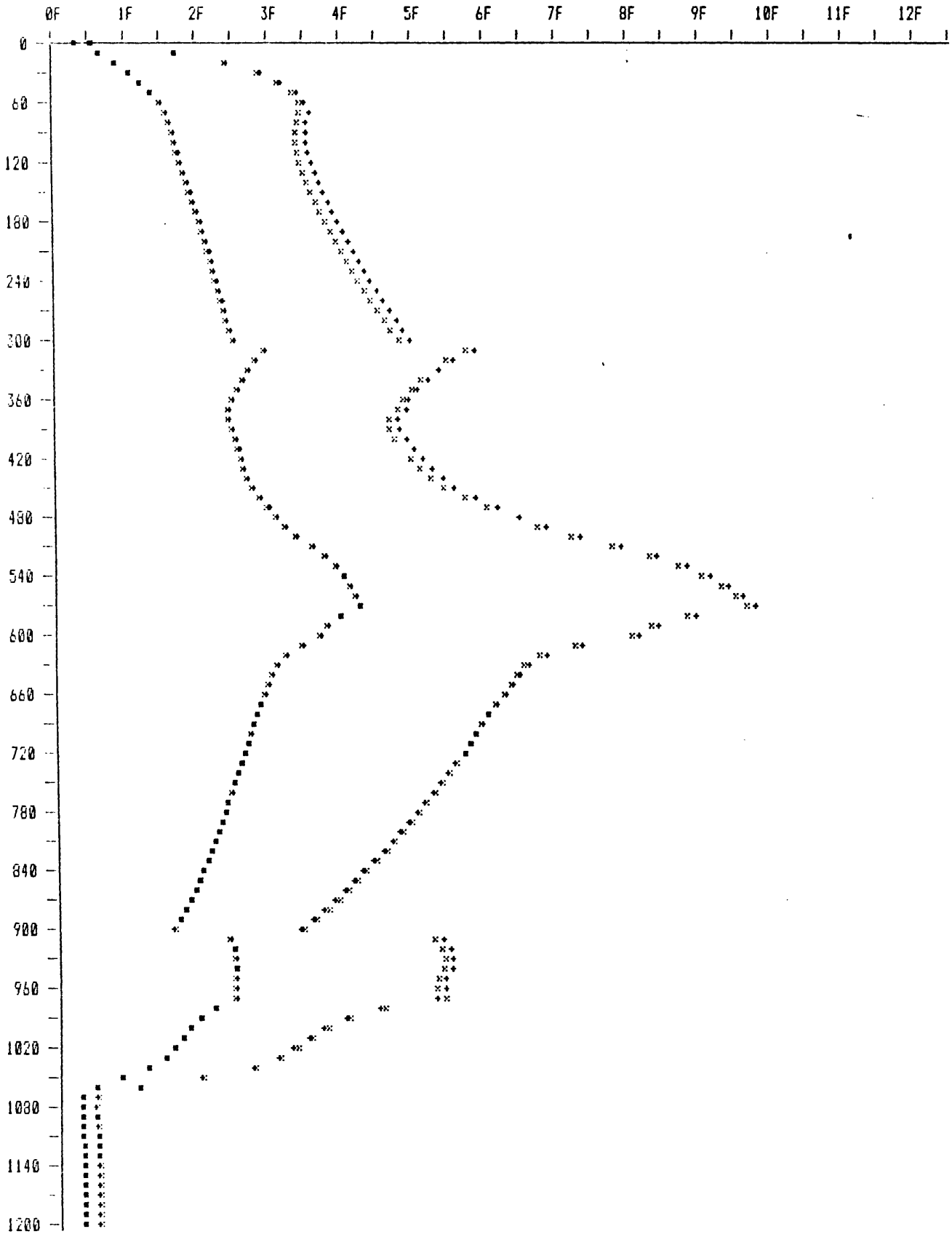
"RUN 200" : Ch-0 MODULE 3 containing "S8" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 6(1)

Note: Curve order is 8Hz pair >>> 2Hz pair

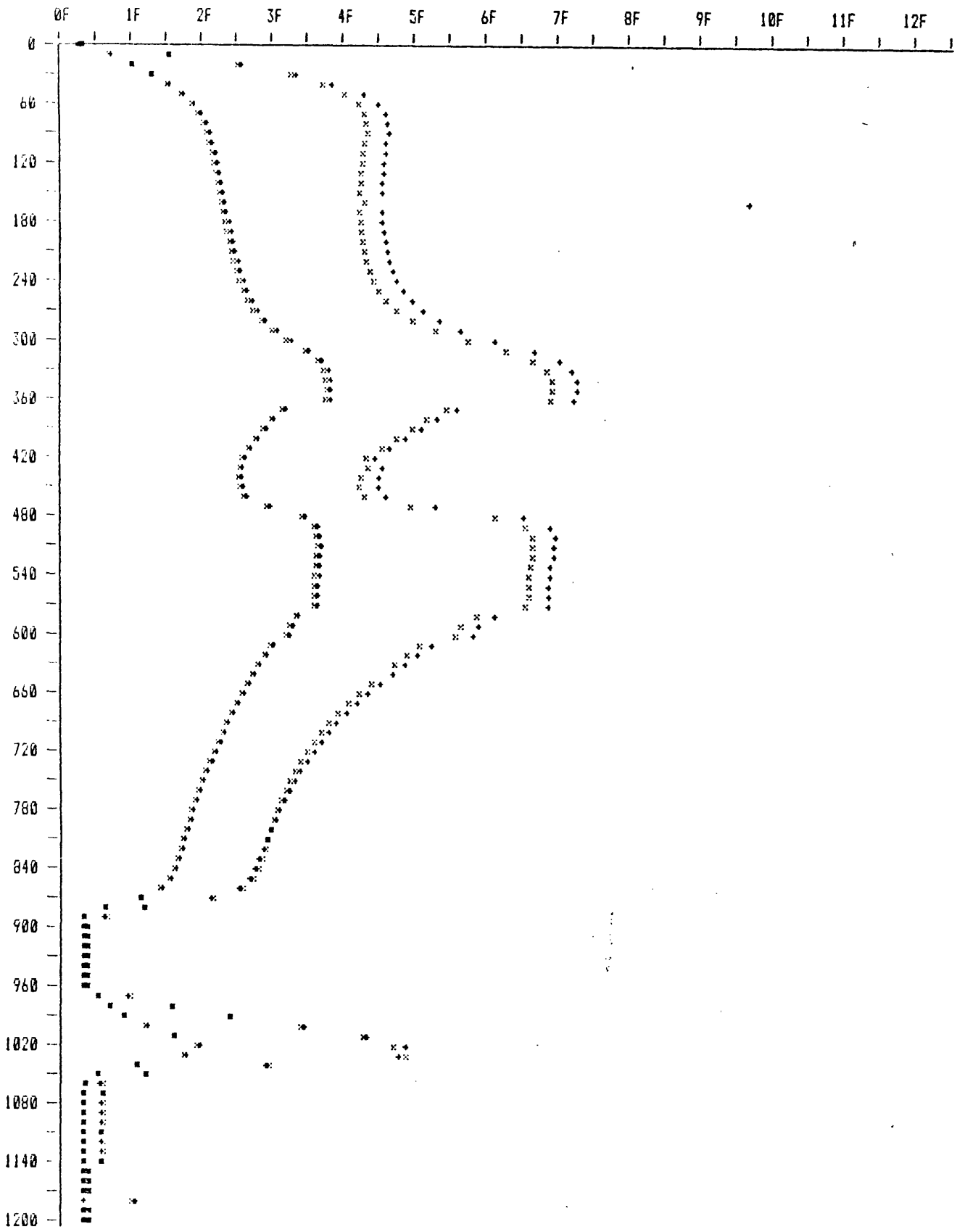
"RUN 230" : Ch-D MODULE 4 containing "S9" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 8(m)

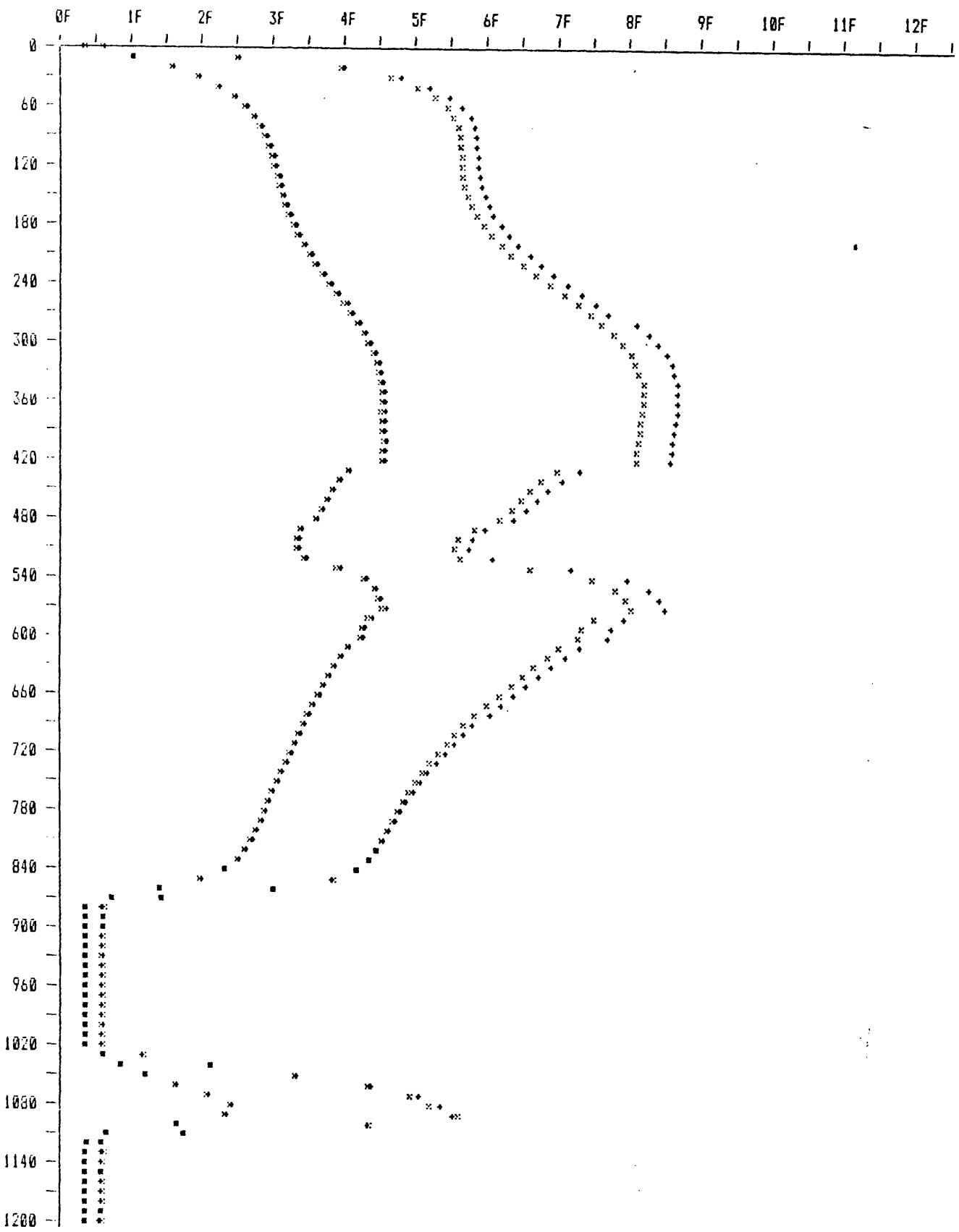
Note: Curve order is 8Hz pair >>> 2Hz pair

"RUN 200" : Ch-D MODULE 5 containing "S18" : ZERO BIAS E.S.CAPACITANCE PROFILES at +8,-8,+2,-2Hz



Graph 8(a)

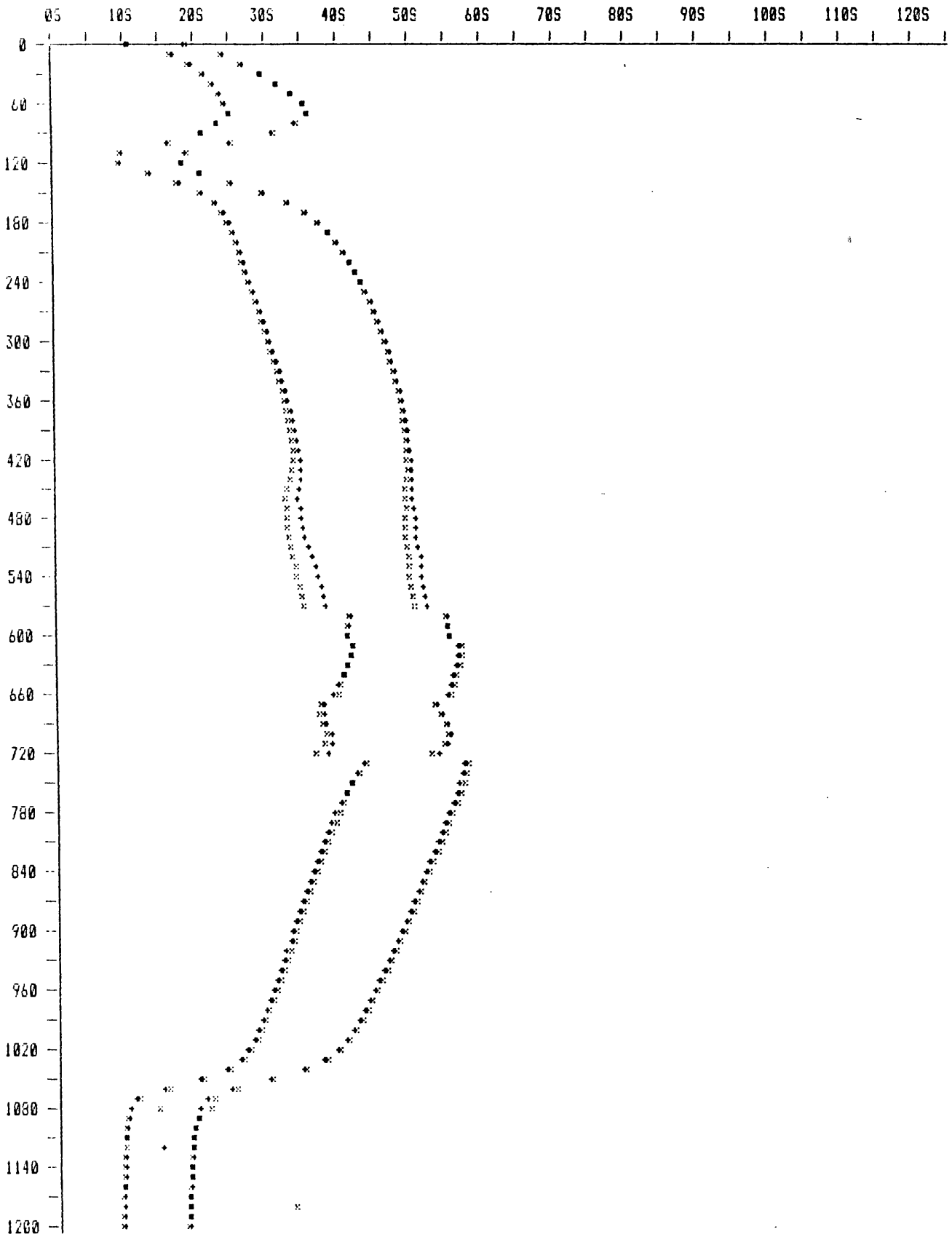
Note: Curve order is 8Hz pair >>> 2Hz pair



Graph 6(o)

Note: Curve order is 2Hz pair >>> 8Hz pair

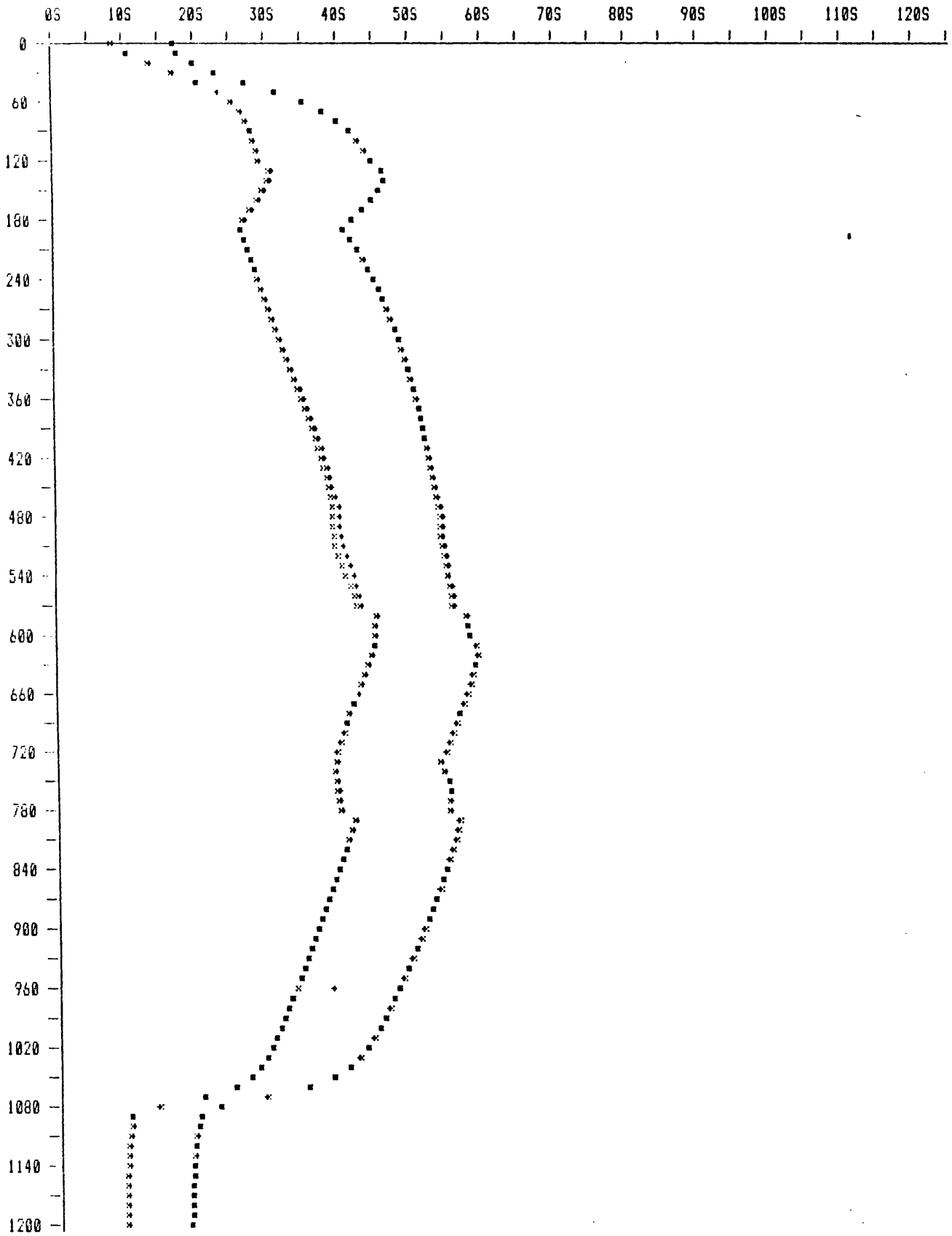
"RUN 288" : Ch-D MODULE 0 containing "S5" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 6(p)

Note: Curve order is 2Hz pair >>> 8Hz pair

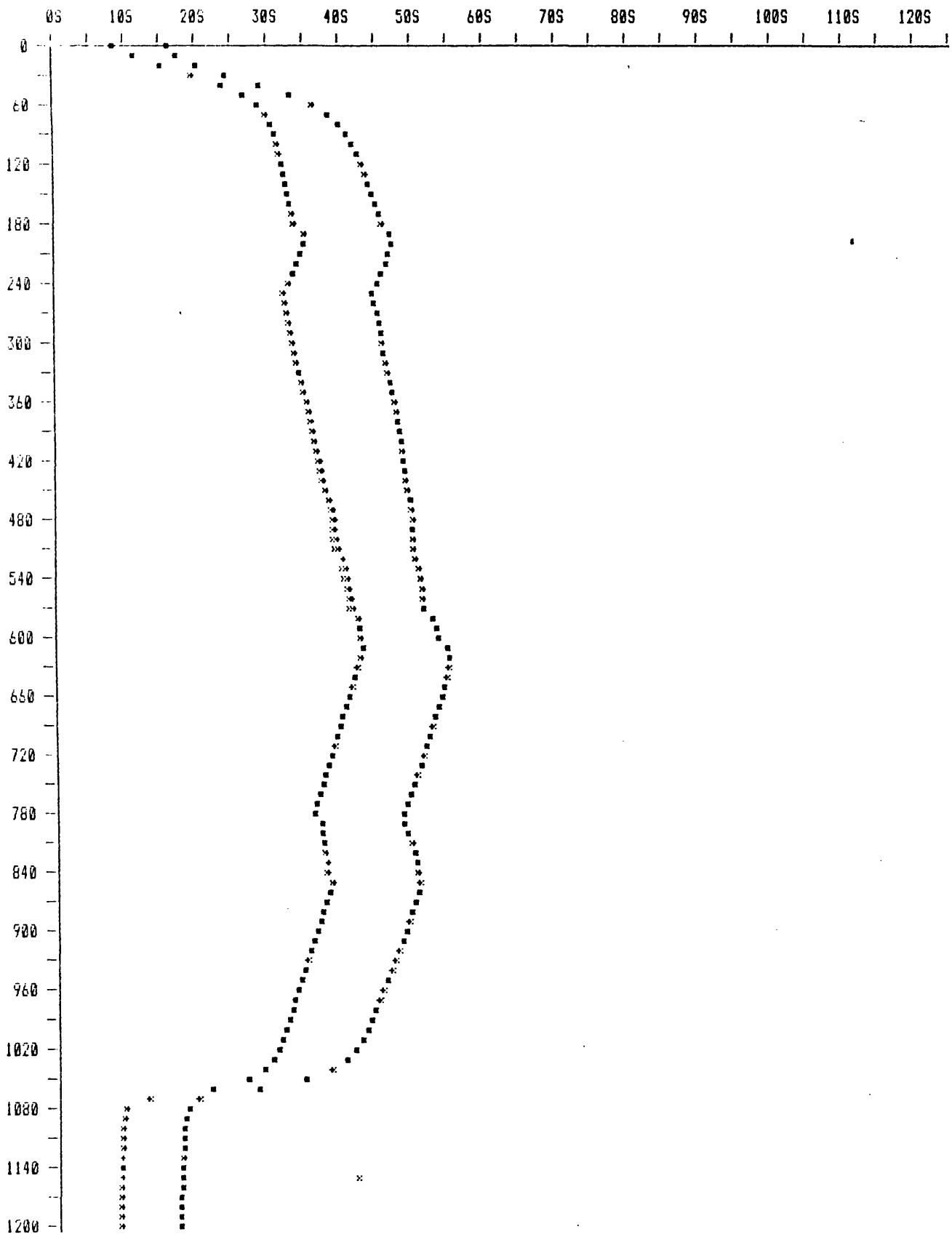
"RUN 208" : Ch-D MODULE 1 containing "56" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 3(g)

Note: Curve order is 2Hz pair >>> 8Hz pair

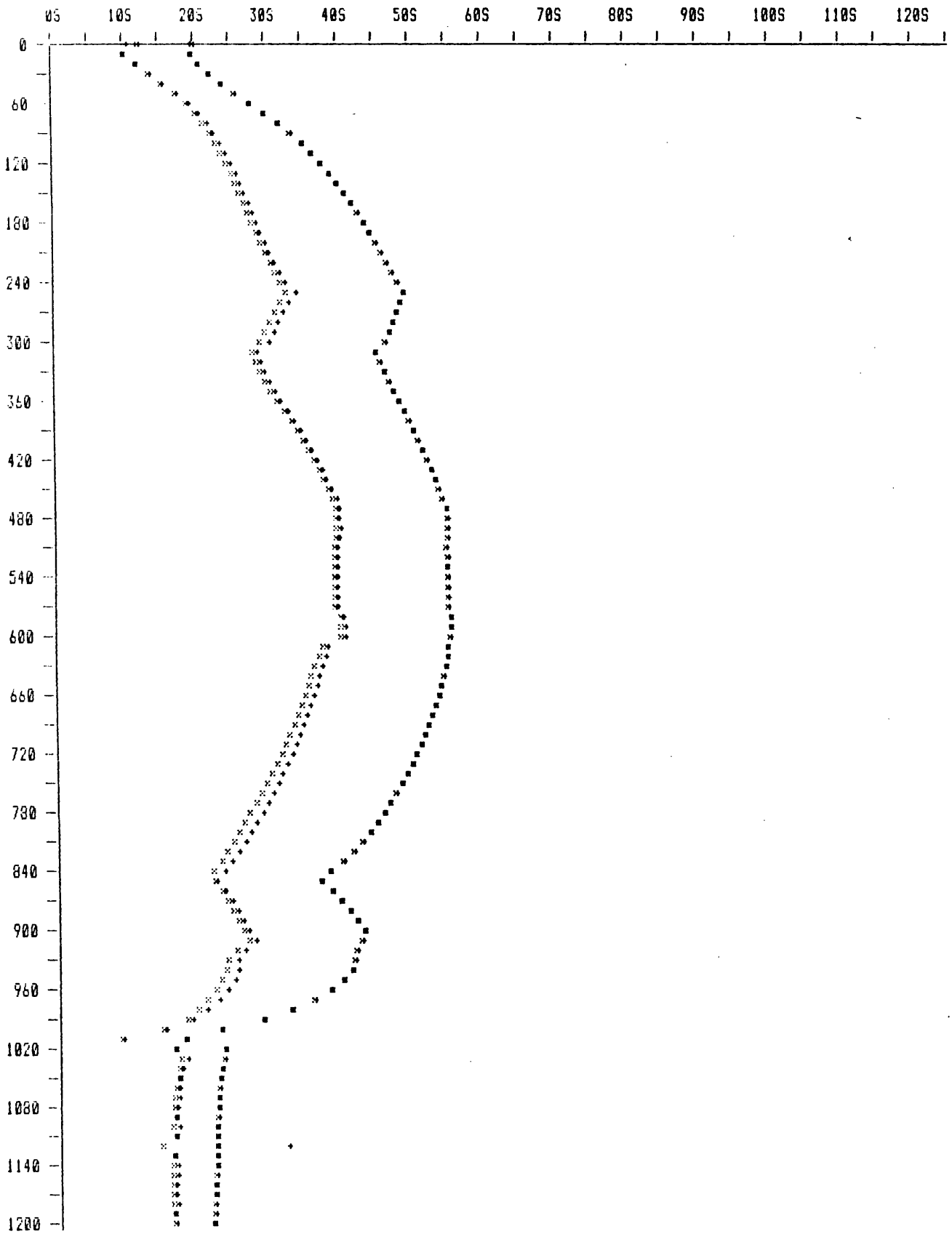
"RUN 200" : Ch-0 MODULE 2 containing "S7" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 8(I)

Note: Curve order is 2Hz pair >>> 8Hz pair

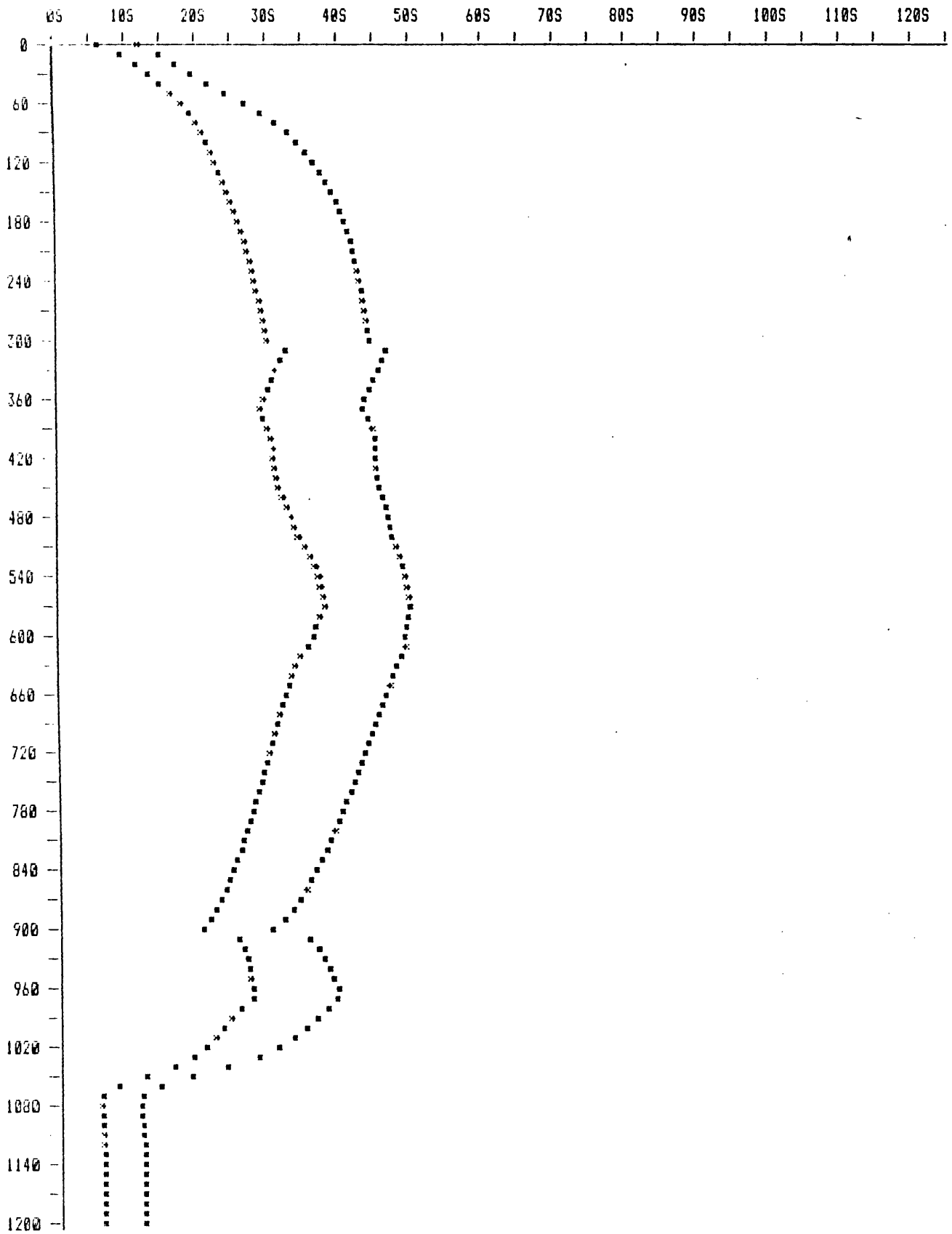
"RUN 200" : Ch-D MODULE 3 containing "S8" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 6(s)

Note: Curve order is 2Hz pair >>> 8Hz pair

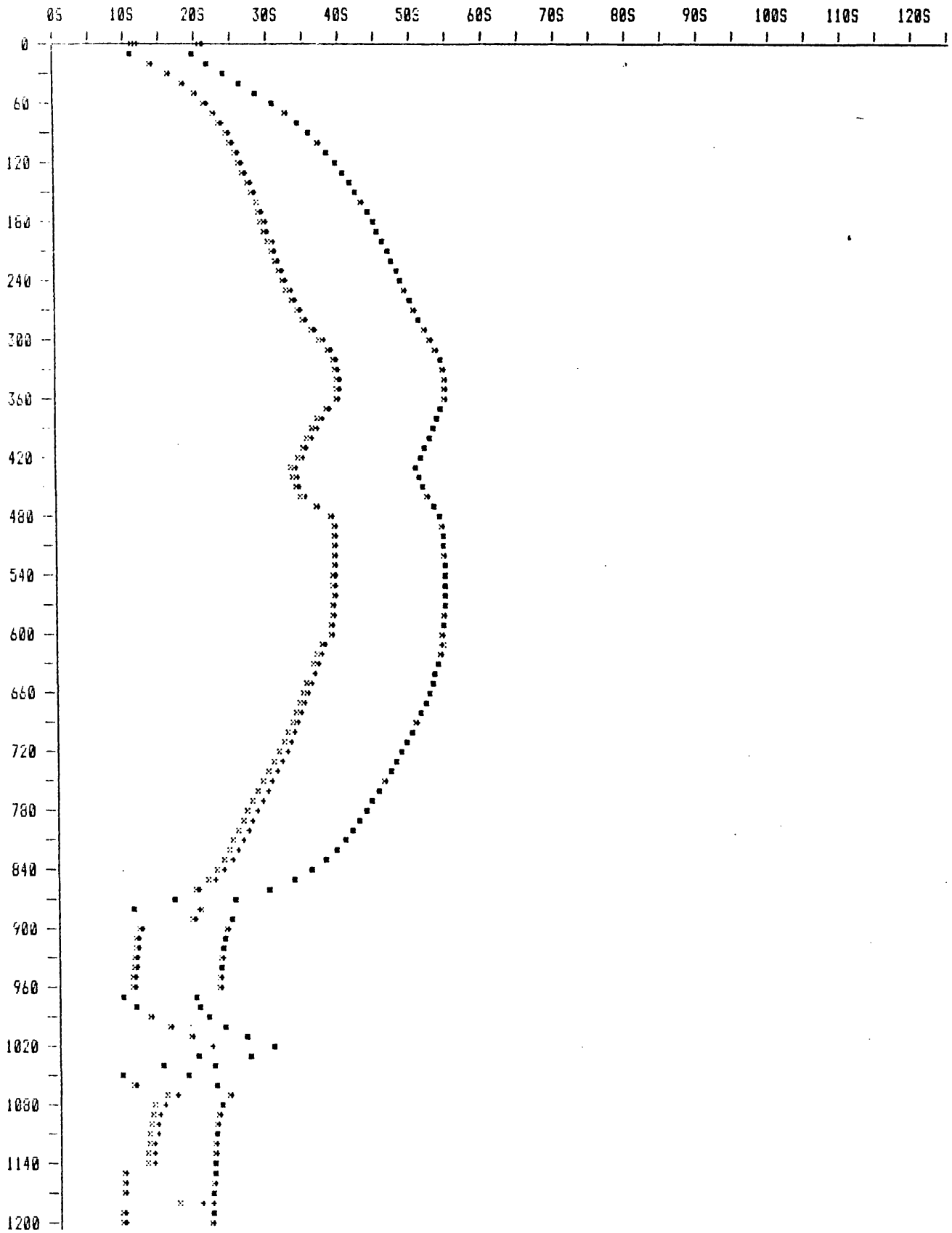
"RUN 200" : Ch-D MODULE 4 containing "S9" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



Graph 8(c)

Note: Curve order is 2Hz pair >>> 8Hz pair

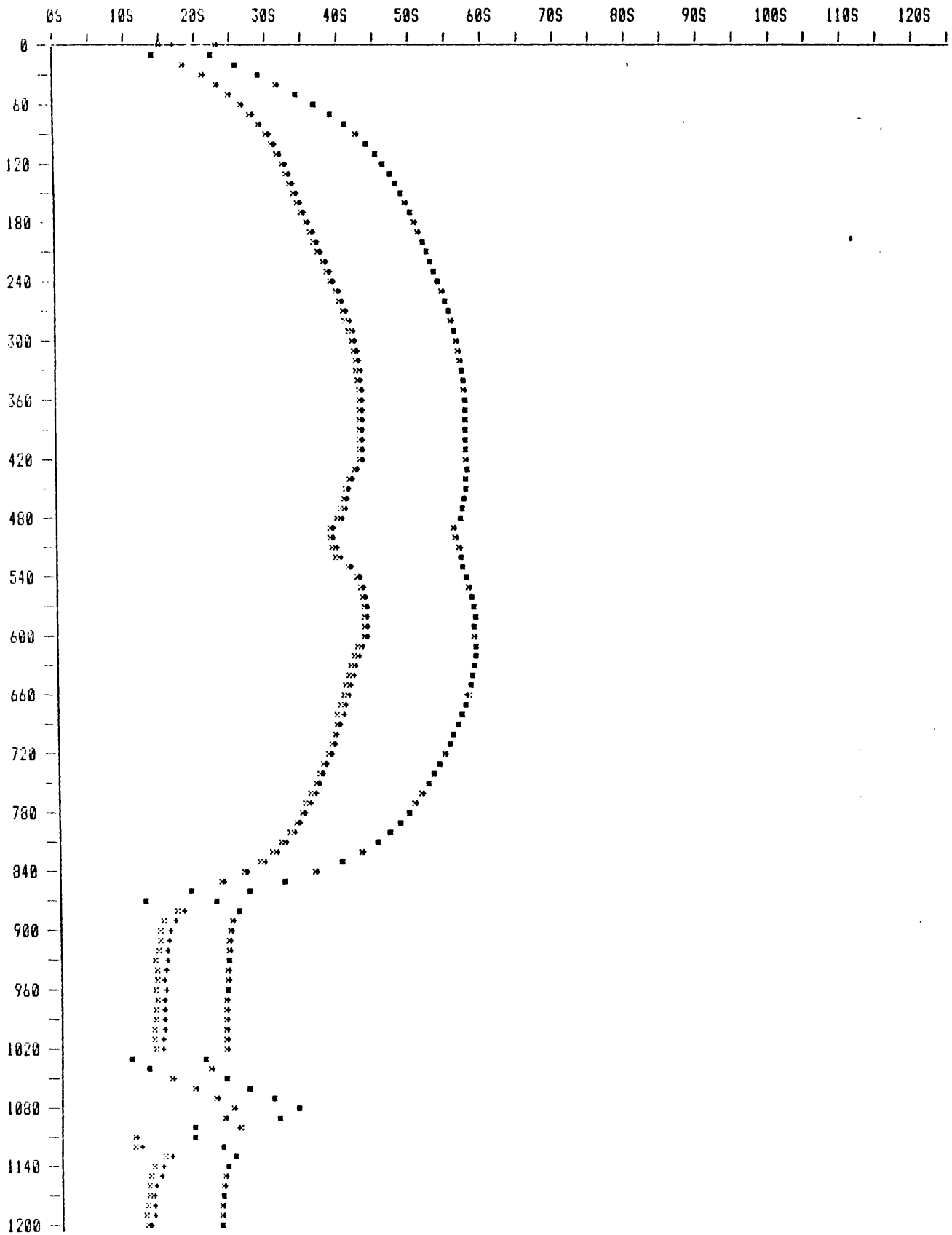
"RUN 203" : Ch-D MODULE 5 containing "S10" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz



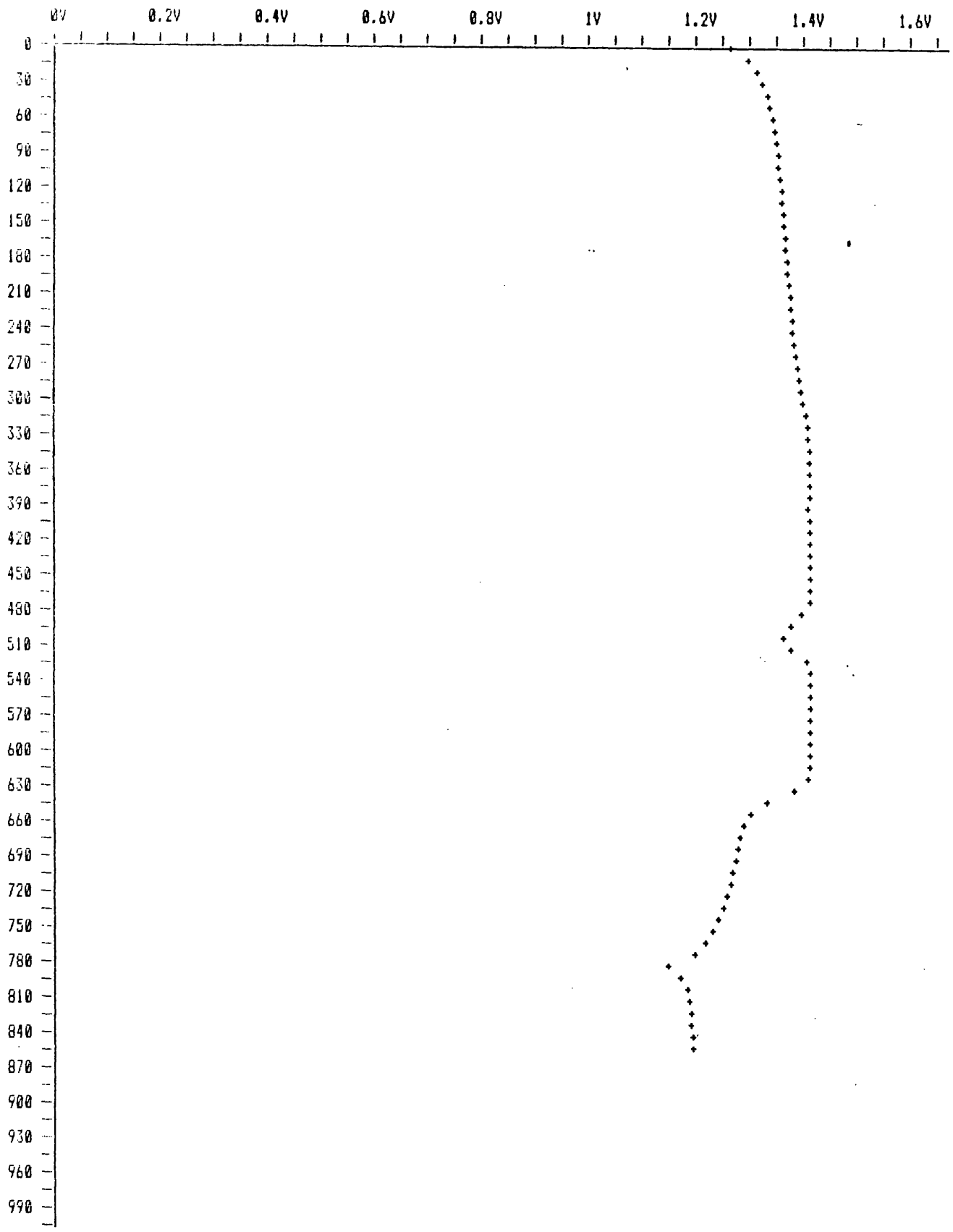
Graph 6(d)

Note: Curve order is 2Hz pair >>> 8Hz pair

"RUN 208" : Ch-D MODULE 6 containing "S11" : ZERO BIAS E.S.CONDUCTANCE PROFILES at +8,-8,+2,-2Hz

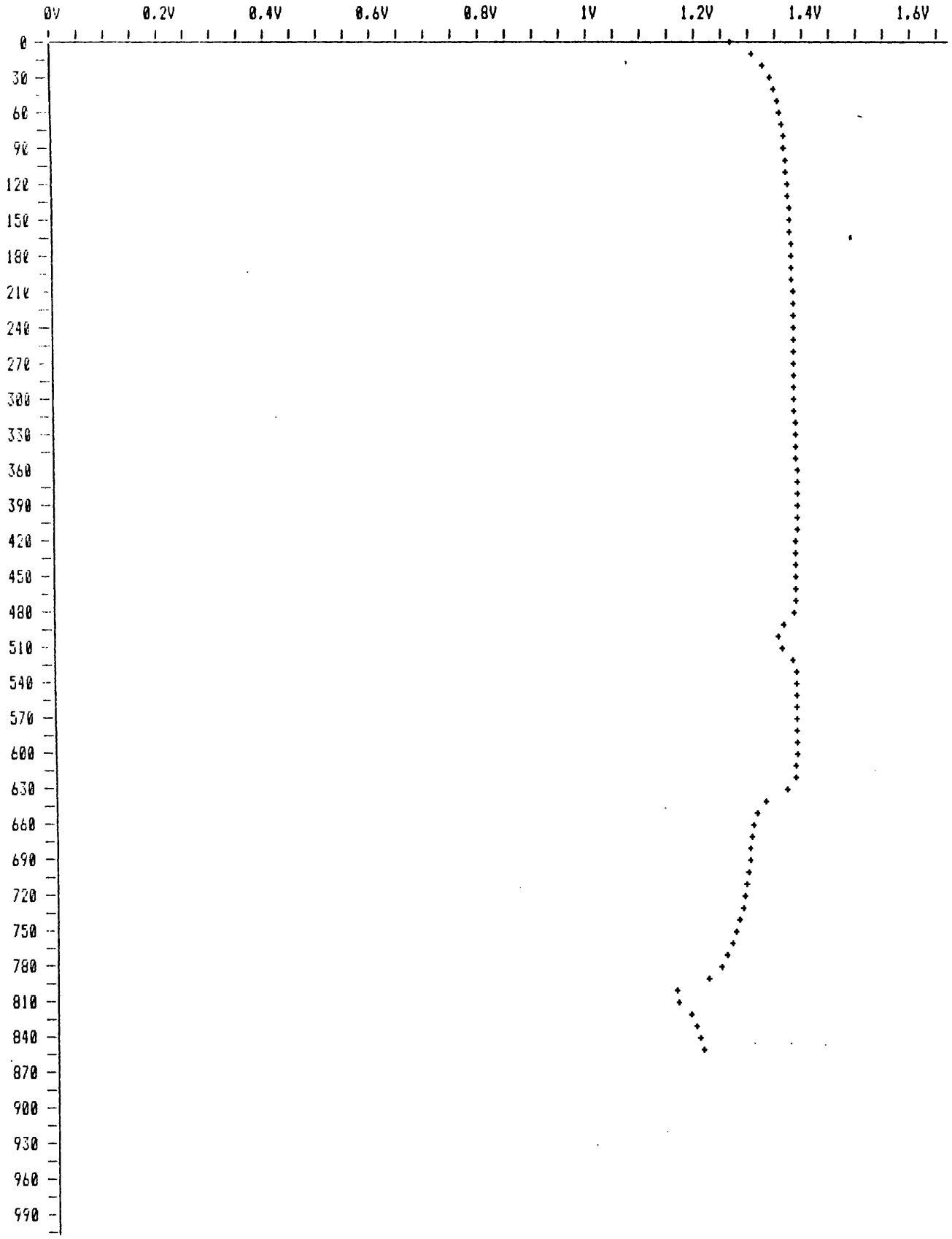


"RUN 315" : Ch-D MODULE 4 containing "S13" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



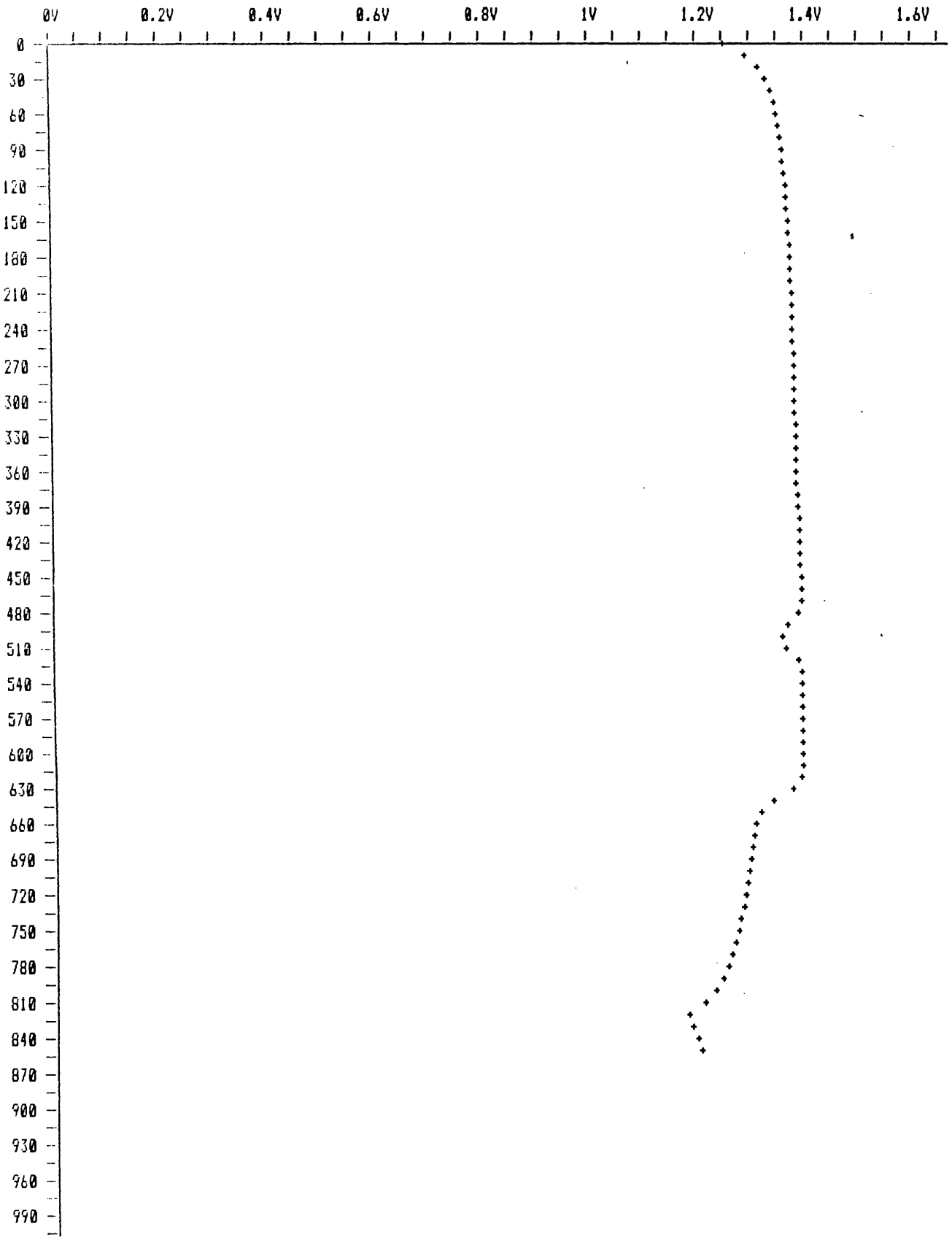
Graph 7(b)

"RUN 315" : Ch-D MODULE 43 containing "PP13" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 7(c)

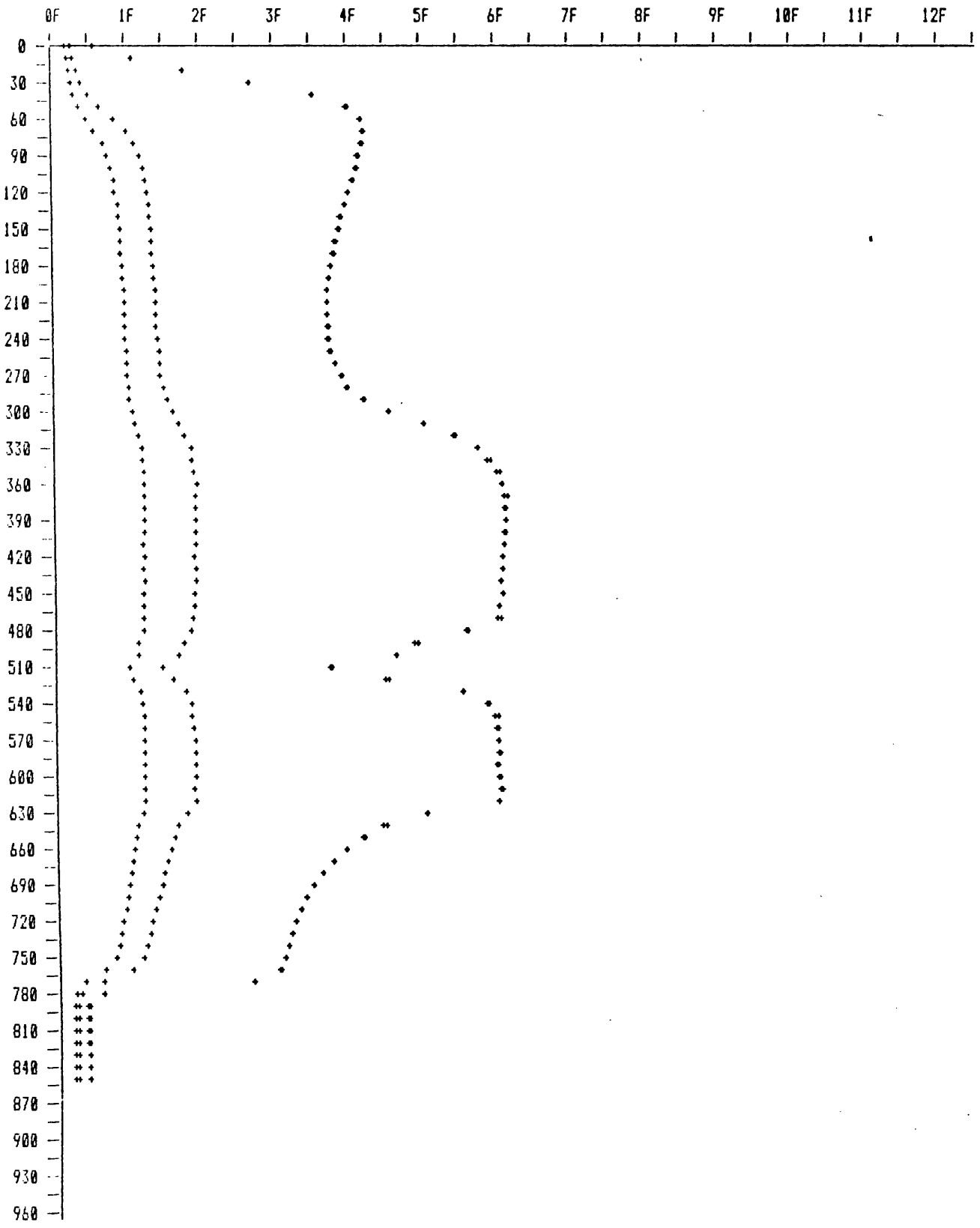
"RUN 315" : Ch-D MODULE 44 containing "PP7" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 7(d)

Note: Curve order is 64Hz >>> 32Hz >>> 2Hz pair

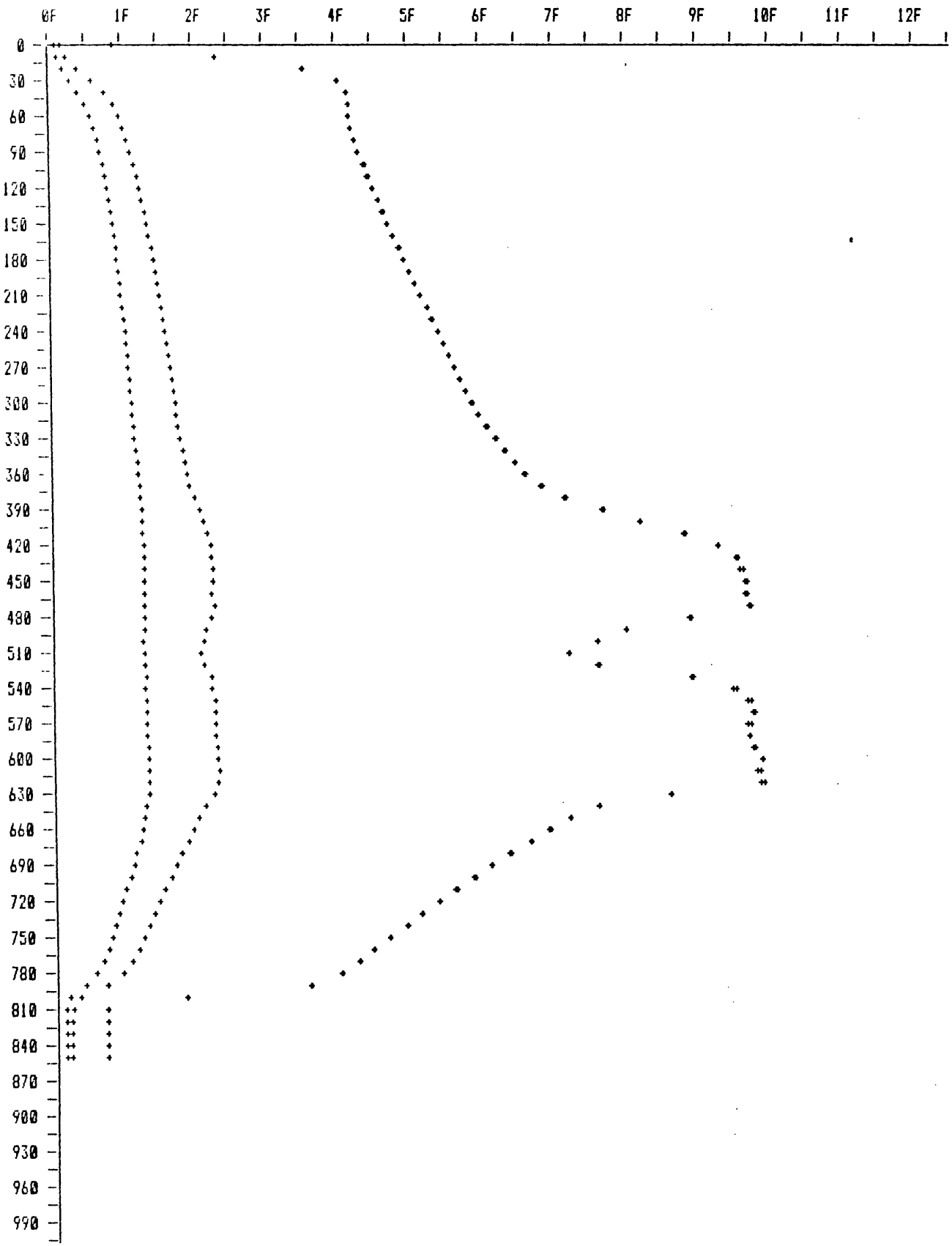
"RUN 315" : Ch-D MODULE 4 containing "S13" : E.S.CAPACITANCE PROFILES at frequencies 64,32,2,2Hz



Graph 7(e)

Note: Curve order is 64Hz >>> 32Hz >>> 2Hz pair

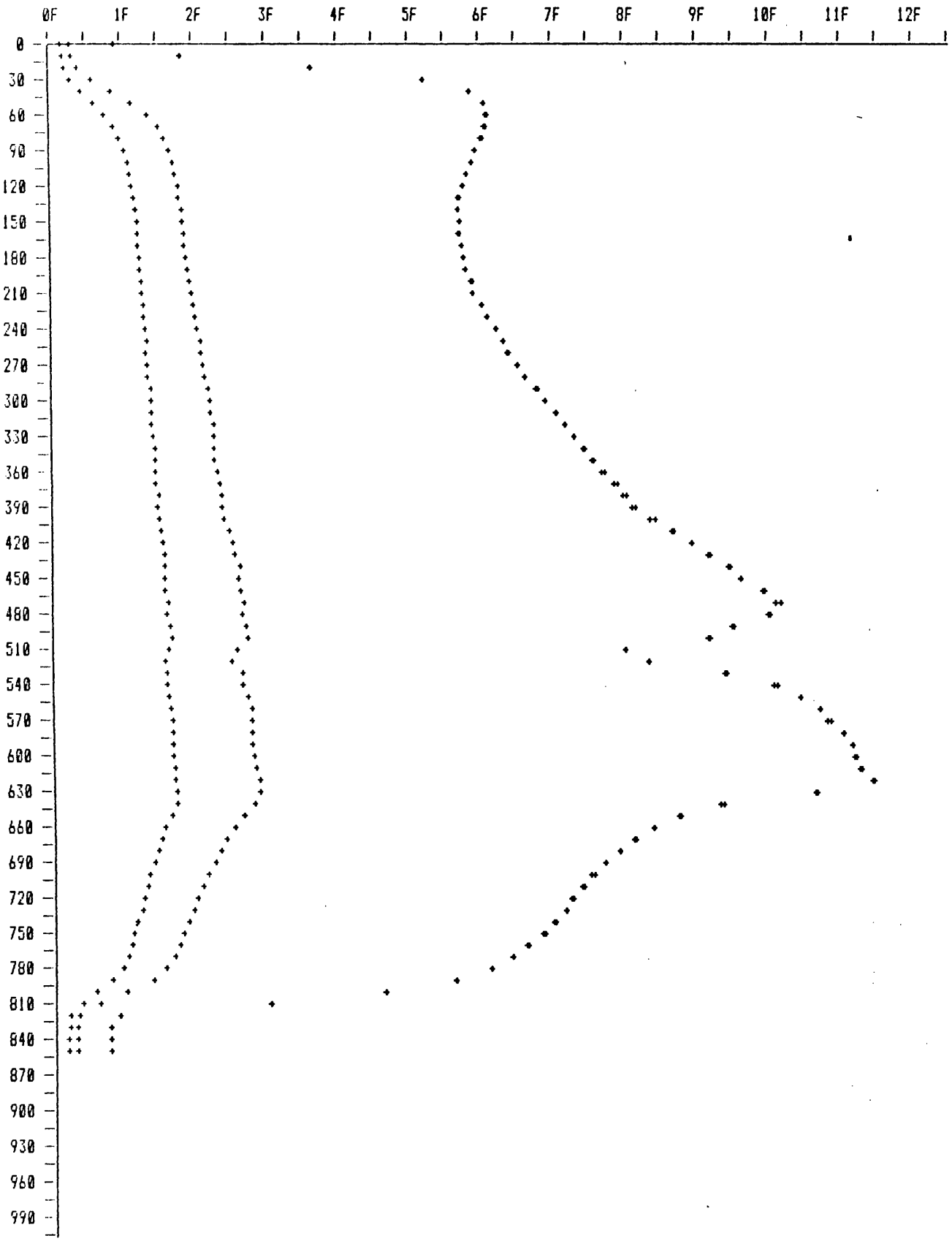
"RUN 315" : Ch-D MODULE 43 containing "PP13" : E.S.CAPACITANCE PROFILES at frequencies 64,32,2,2Hz



Graph 7(f)

Note: Curve order is 64Hz >>> 32Hz >>> 2Hz pair

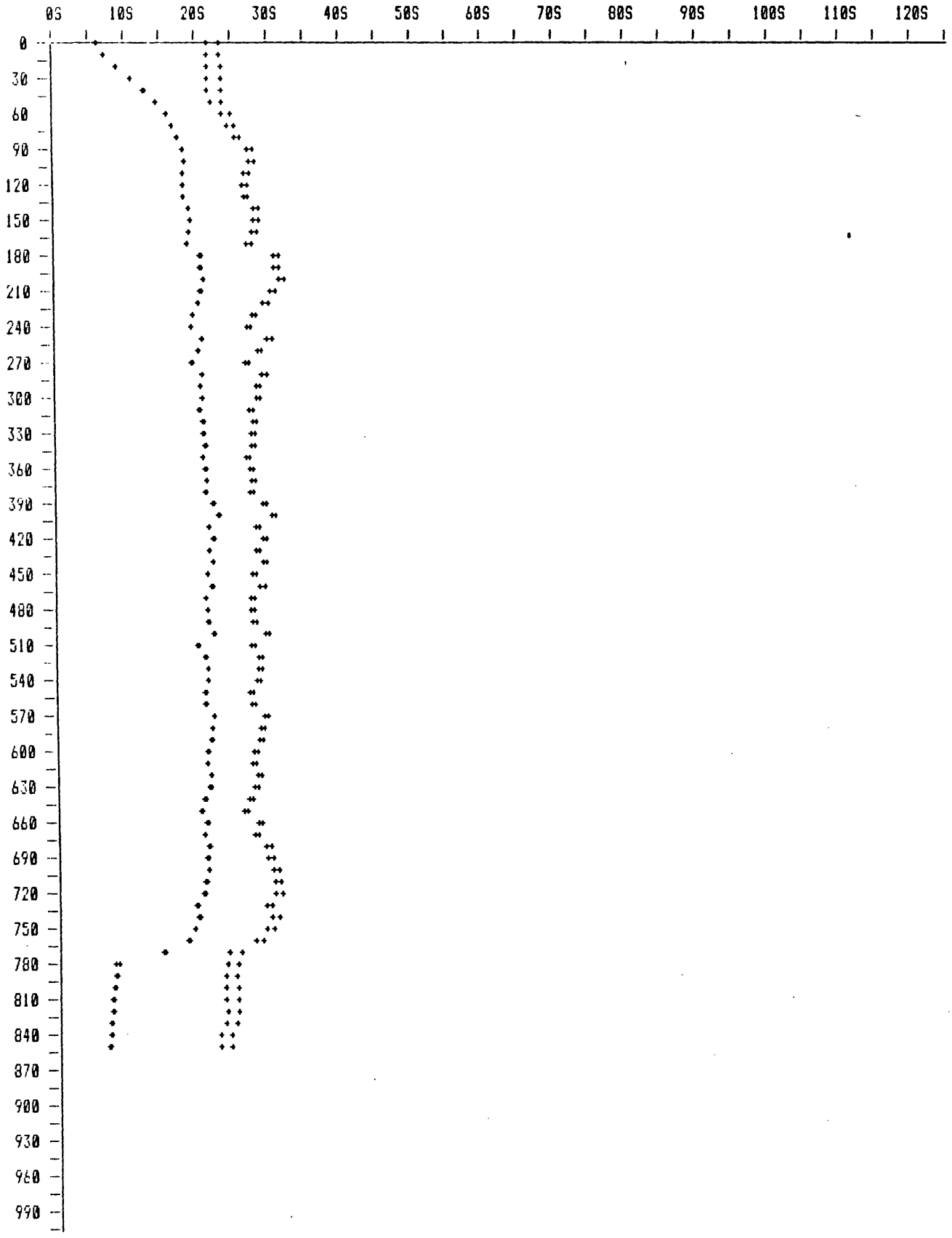
"RUN 315" : Ch-D MODULE 44 containing "PP7" : E.S.CAPACITANCE PROFILES at frequencies 64,32,2,2Hz



Graph 7(g)

Note: Curve order is 2Hz pair >>> 32Hz >>> 64Hz

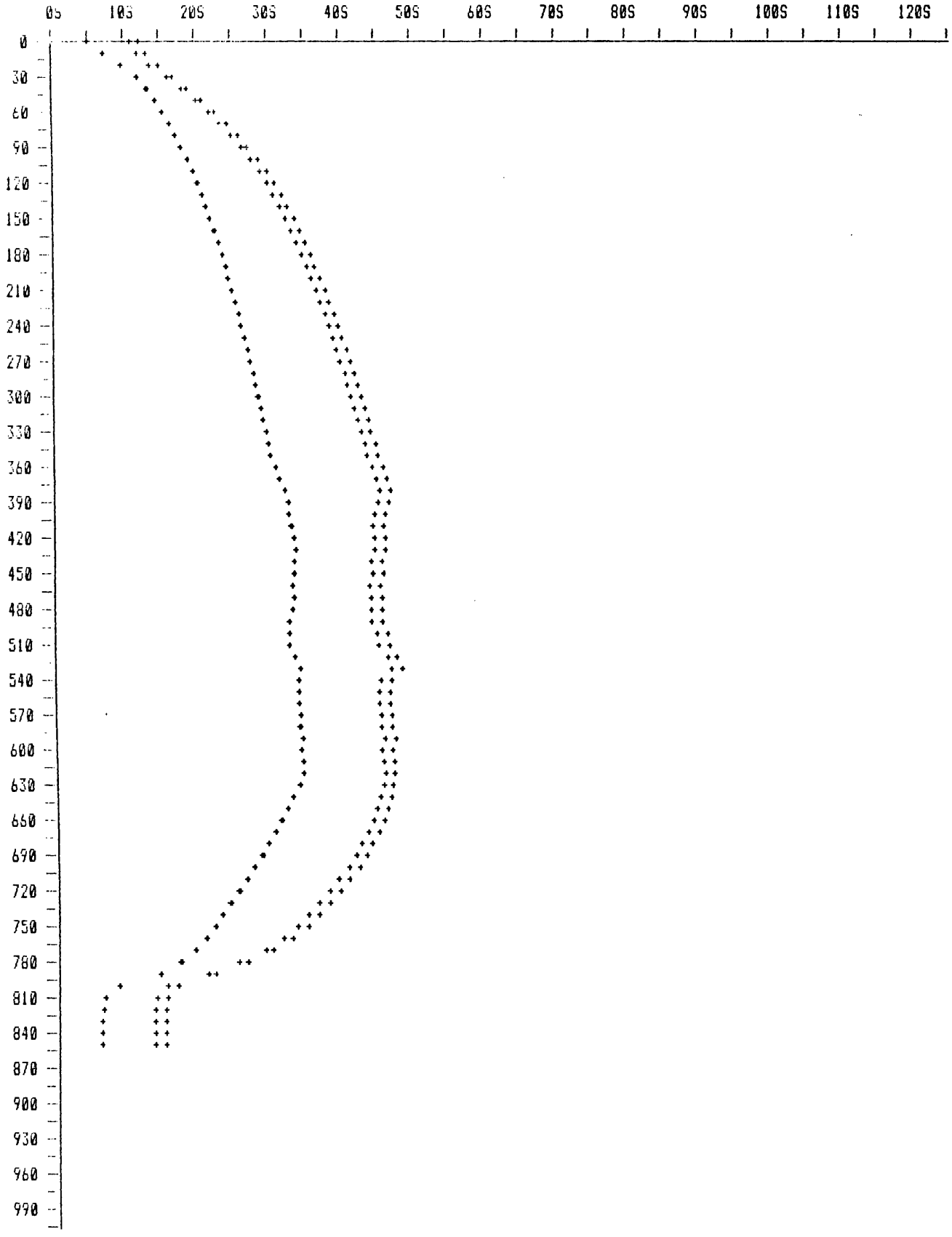
"RUN 315" : Ch-D MODULE 4 containing "S13" : E.S.CONDUCTANCE PROFILES at frequencies 64,32,2,2Hz



Graph 7(h)

Note: Curve order is 2Hz pair >>> 32Hz >>> 64Hz

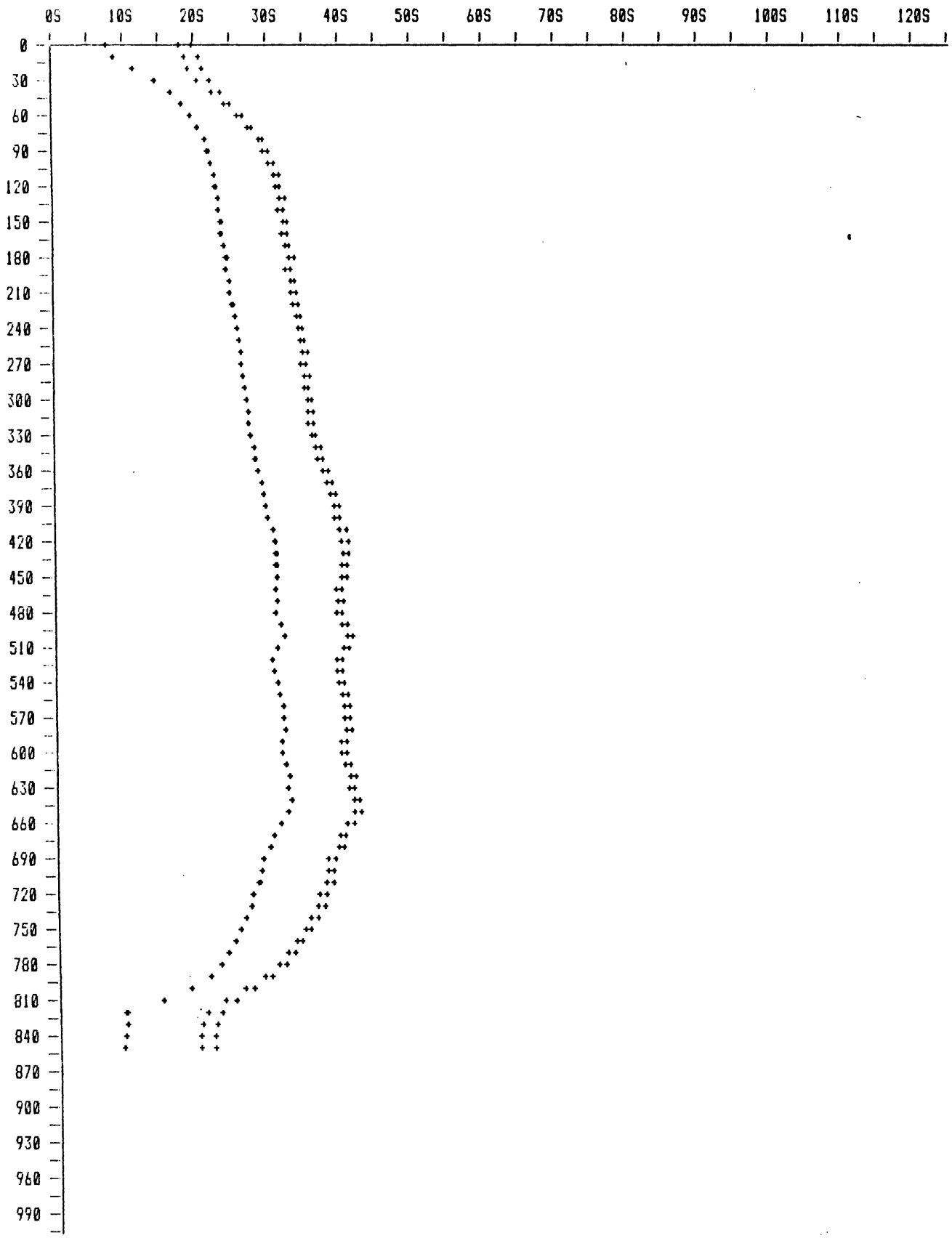
"RUN 315" : Ch-D MODULE 43 containing "PP13" : E.S.CONDUCTANCE PROFILES at frequencies 64,32,2,2Hz



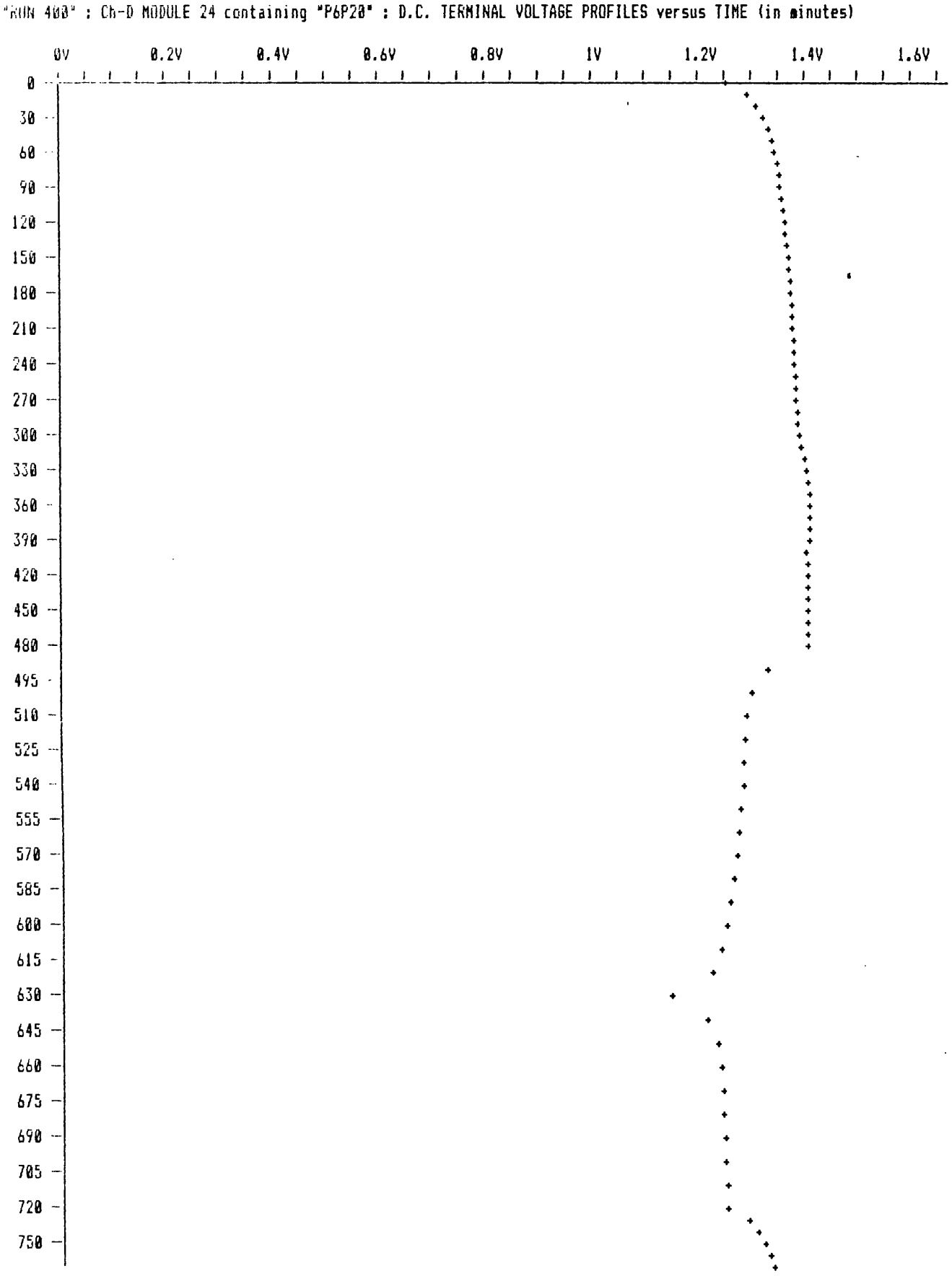
Graph 7(i)

Note: Curve order is 2Hz pair >>> 32Hz >>> 64Hz

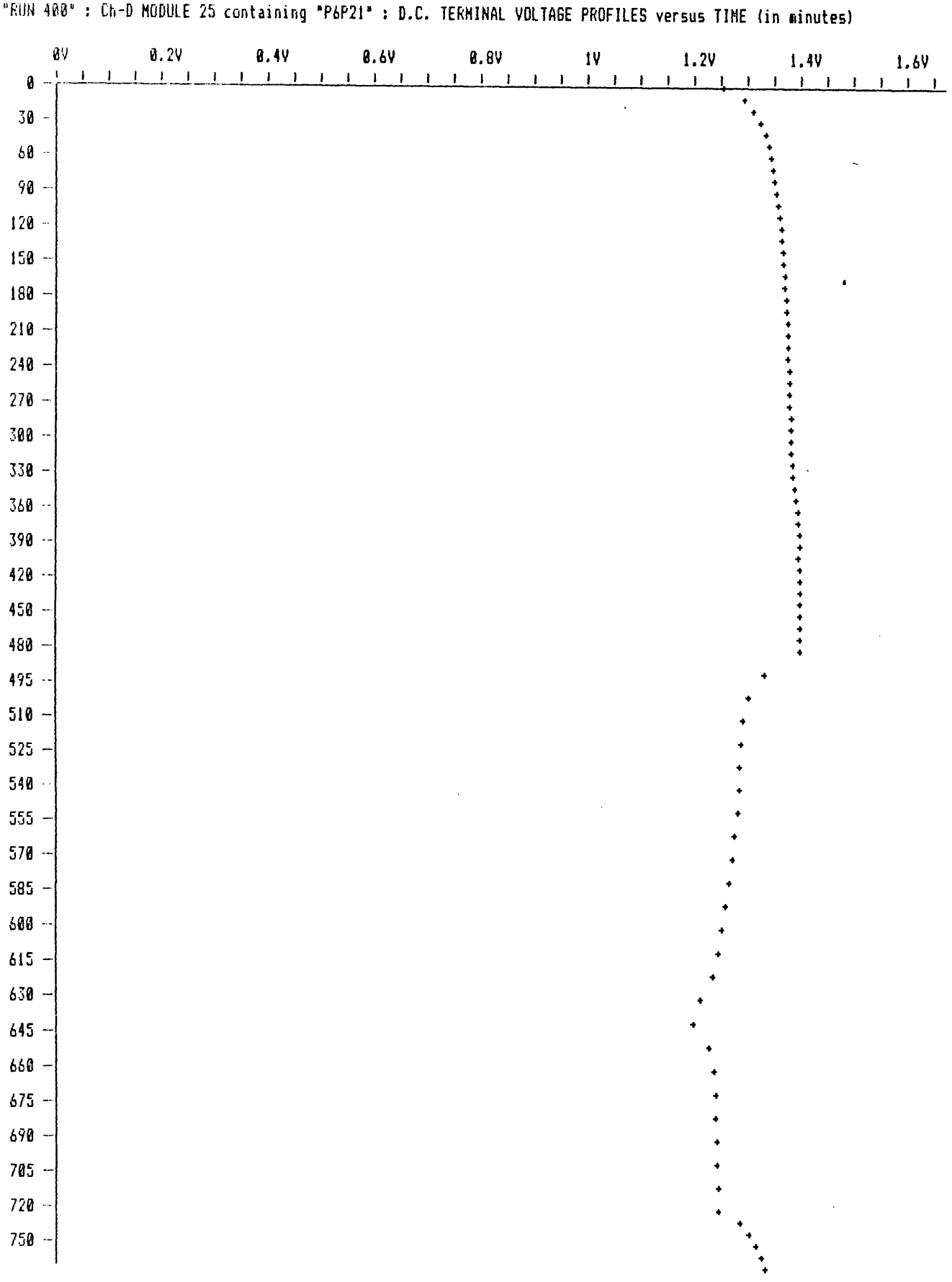
"RUN 315" : Ch-D MODULE 44 containing "PP7" : E.S.CONDUCTANCE PROFILES at frequencies 64,32,2,2Hz



Graph 8(a)

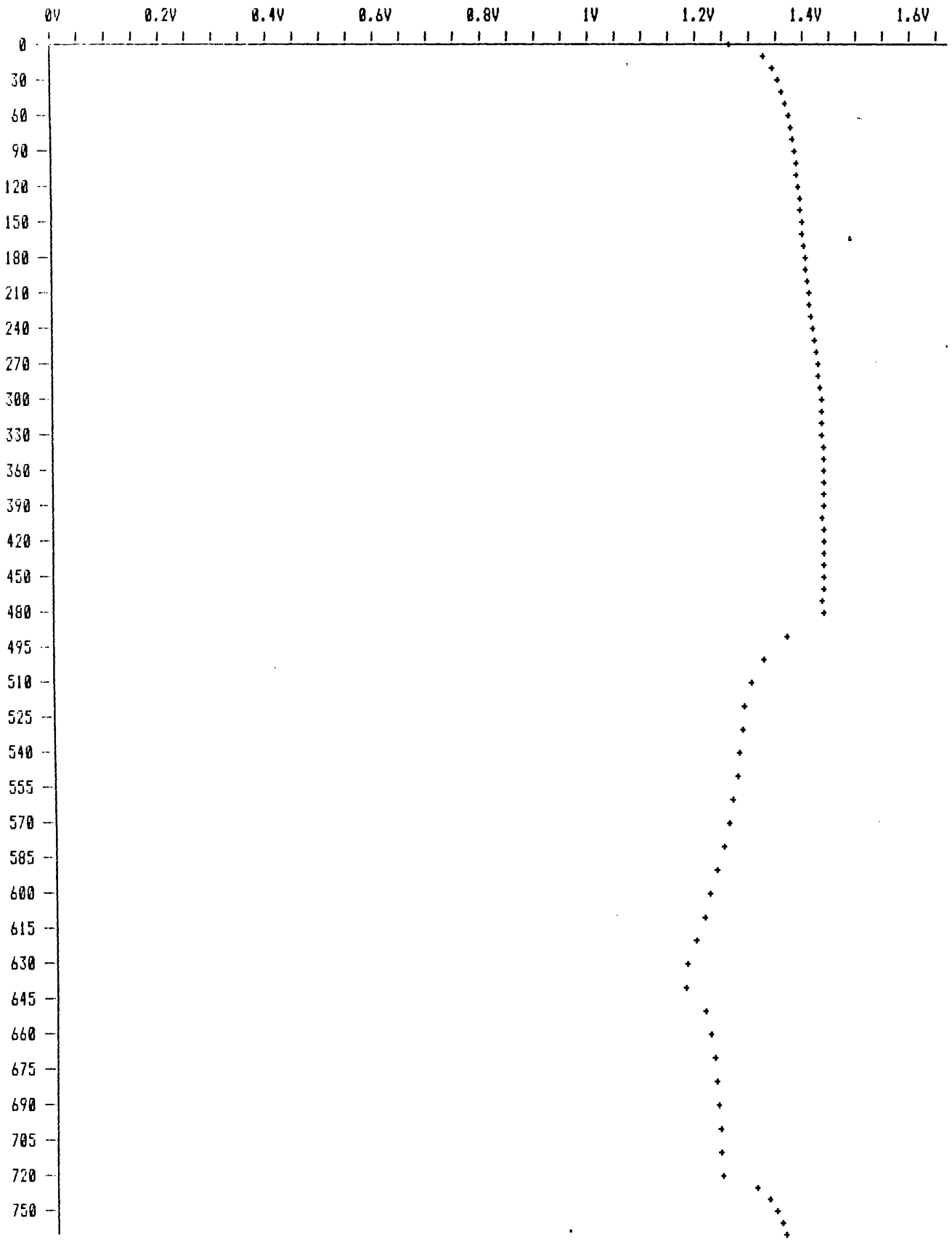

"RUN 400" : Ch-D MODULE 24 containing "P6P20" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 8(B)

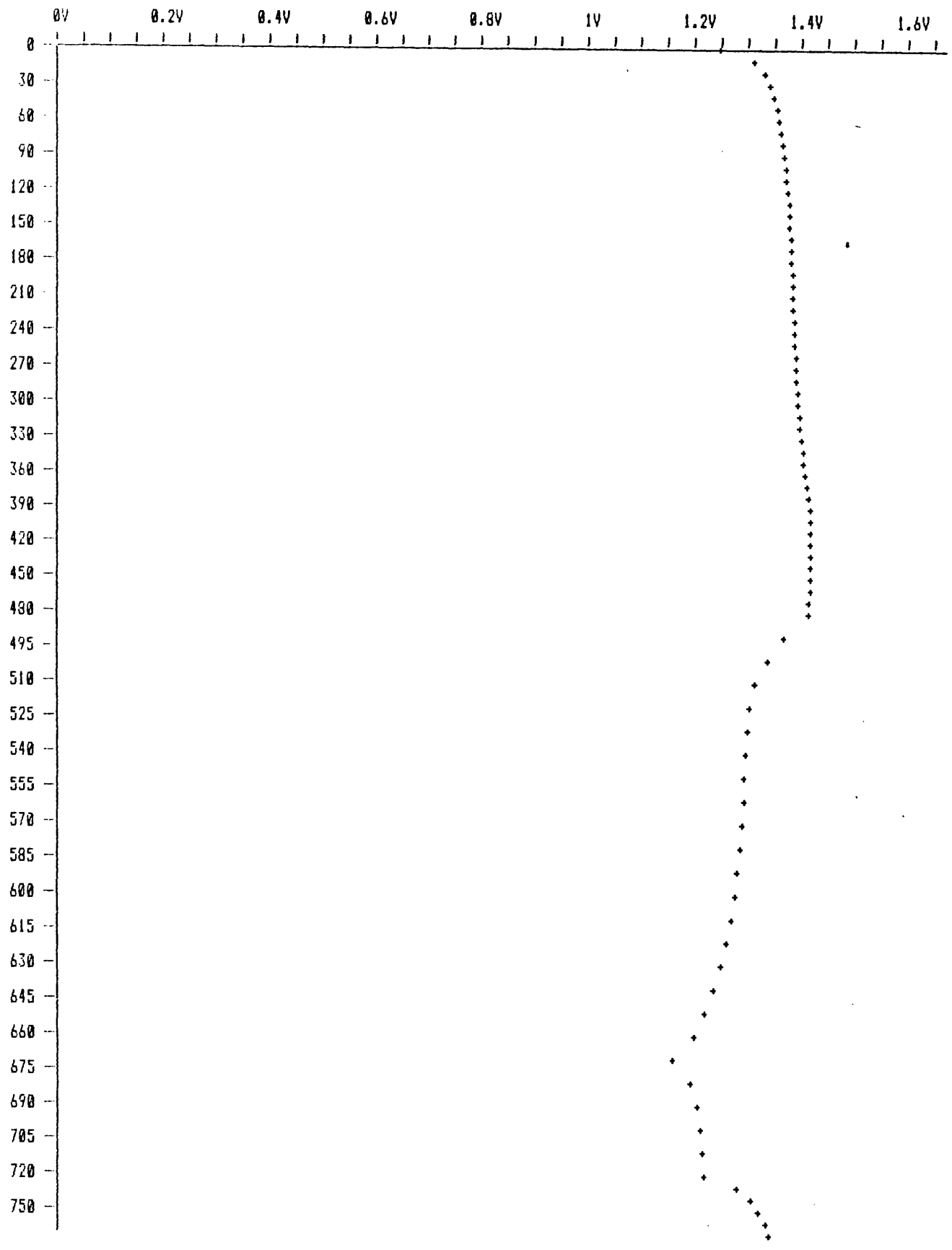

"RUN 400" : Ch-D MODULE 25 containing "P6P21" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 8(c)

"RUN 400" : Ch-D MODULE 32 containing "HP1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

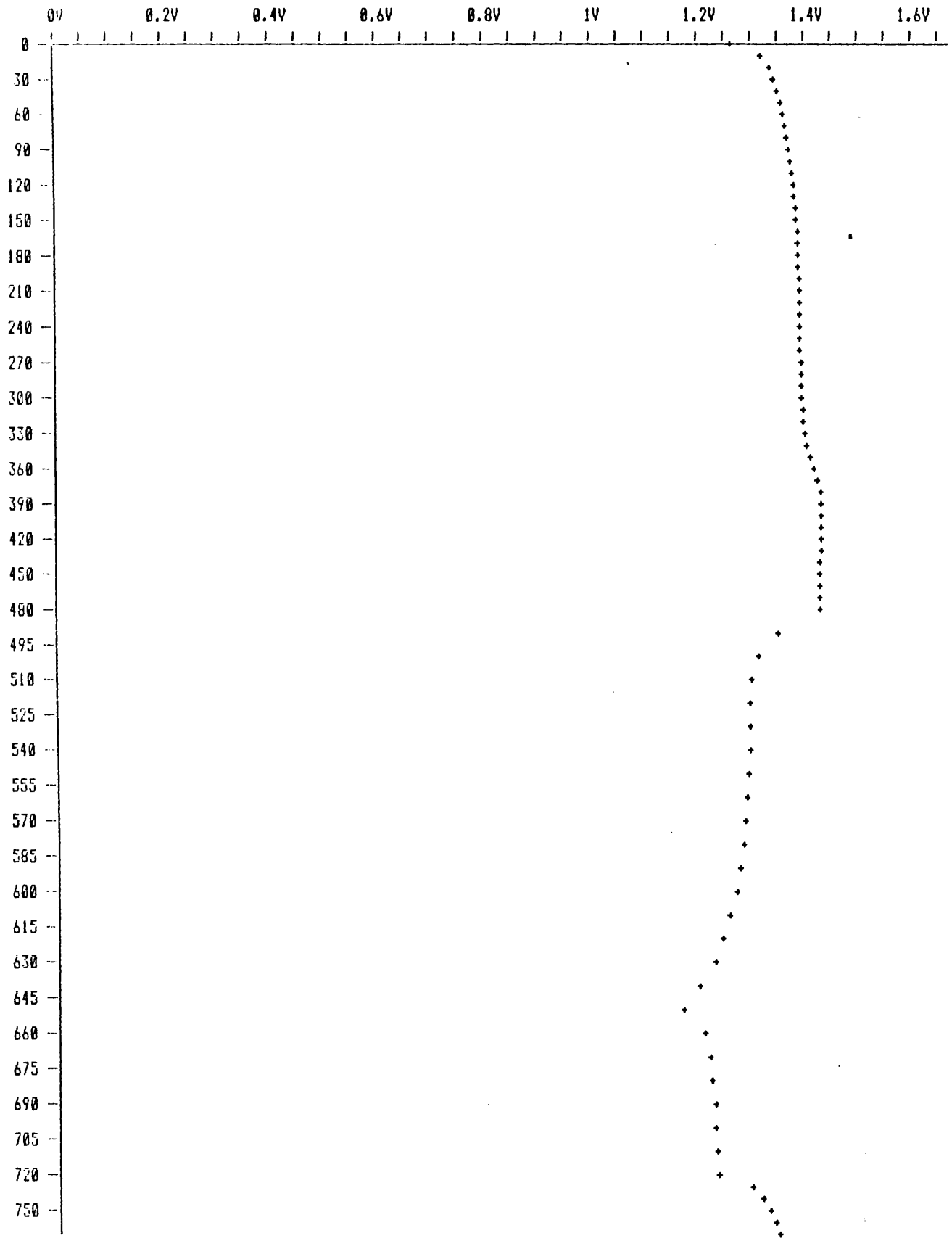


Graph 6(a)


"RUN 400" : Ch-D MODULE 33 containing "HP2" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

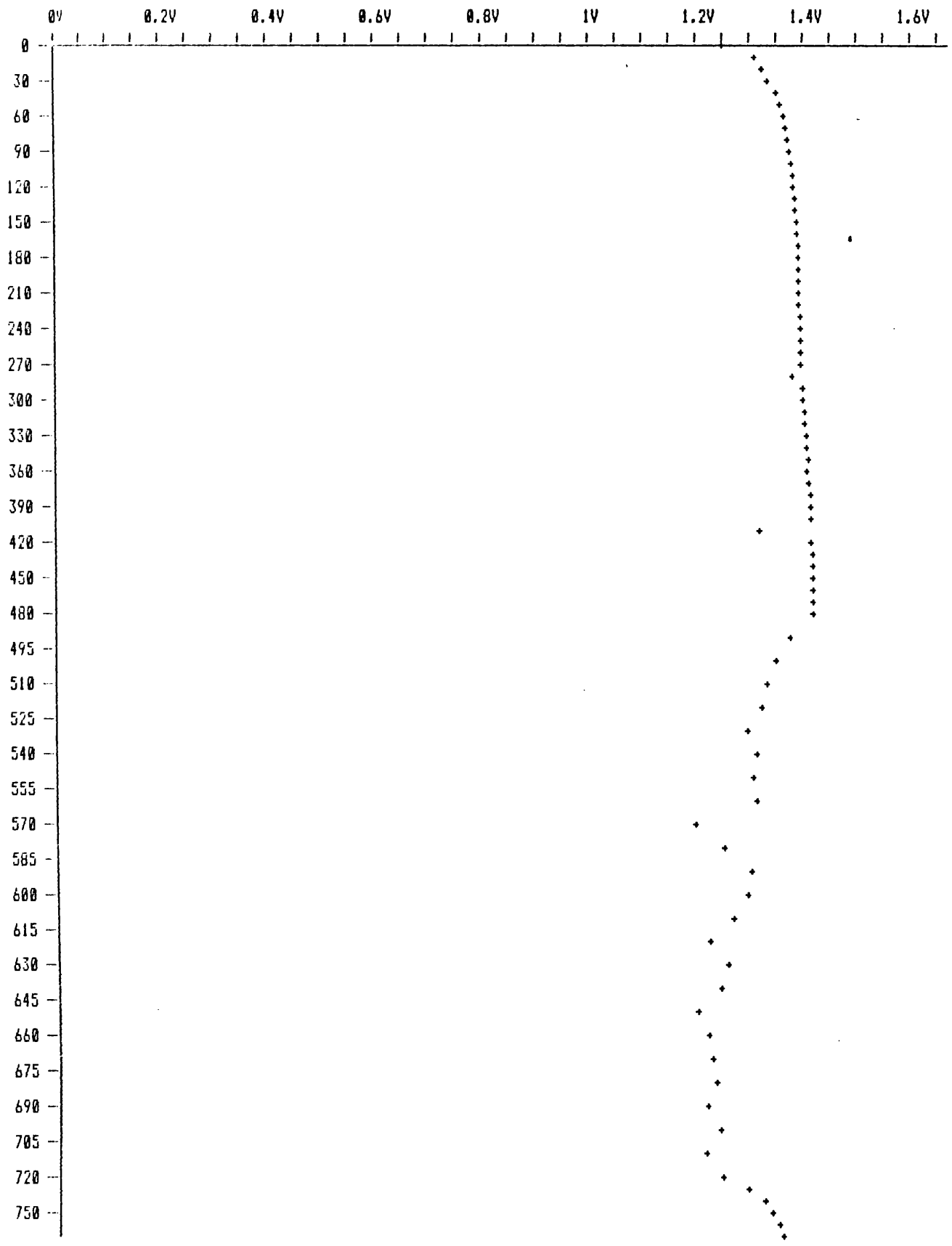
Graph 8(a)

"RUN 400" : Ch-D MODULE 35 containing "VA8" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

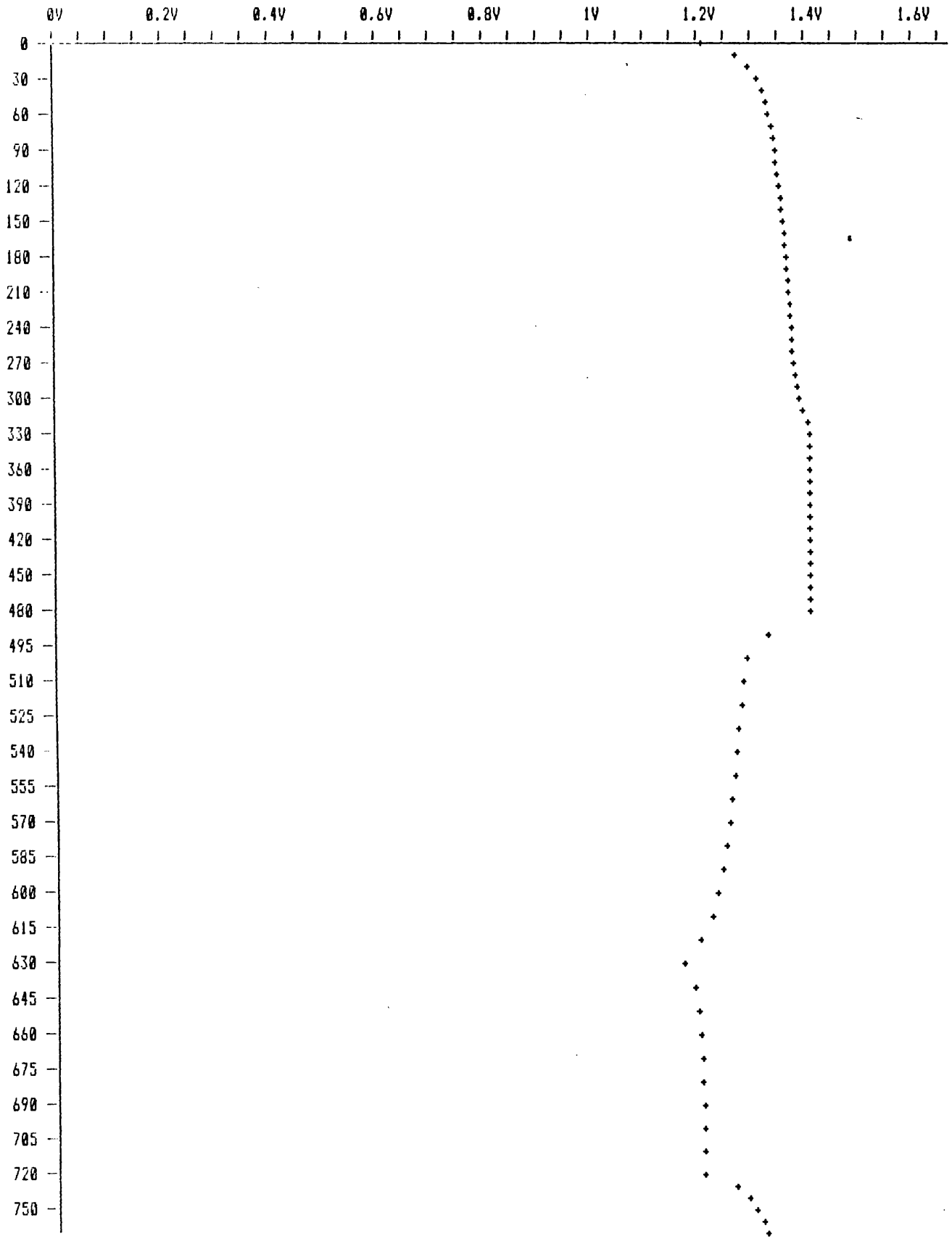


Graph 3(1)

"RUN 40J" : Ch-D MODULE 36 containing "CC0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

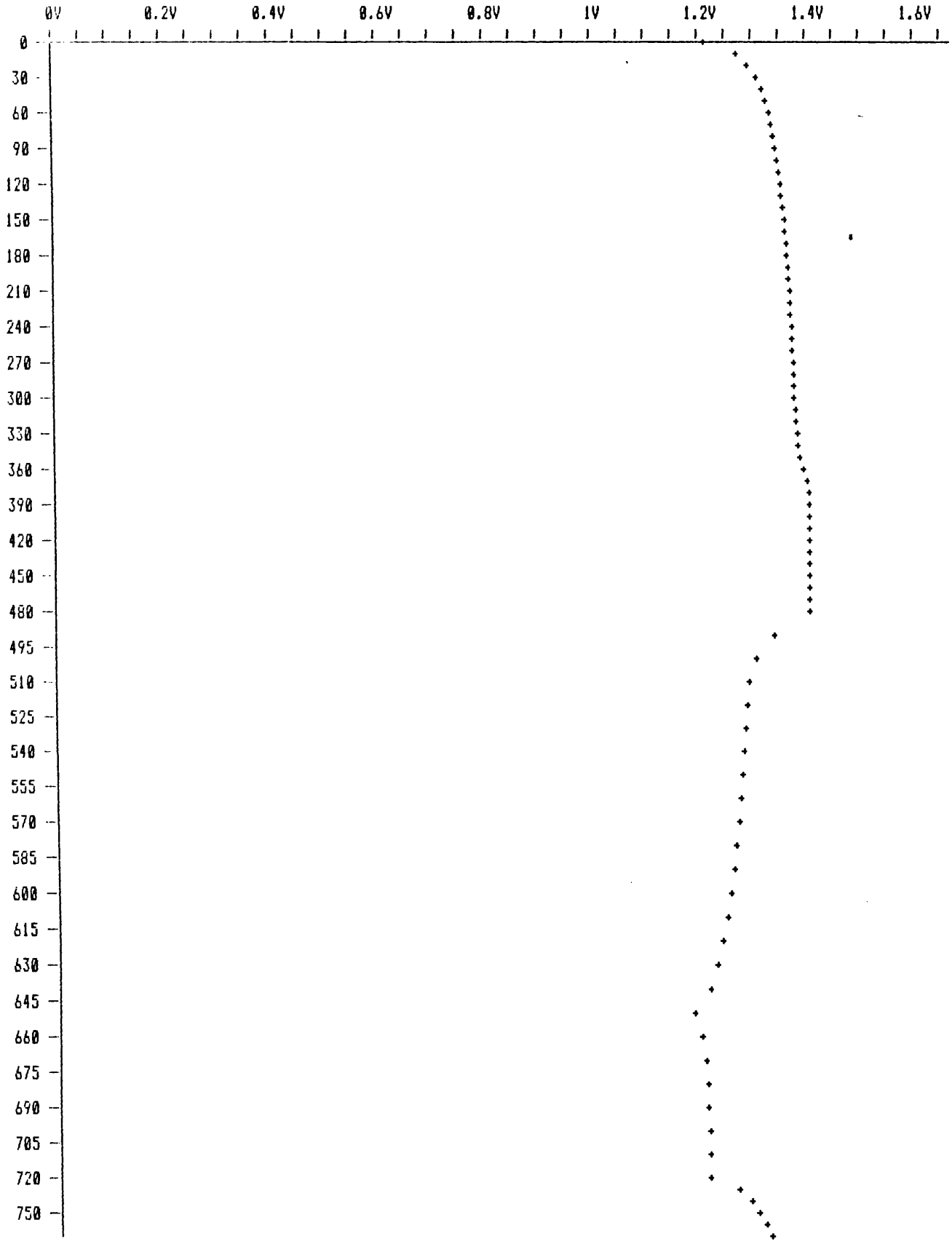


"RUN 400" : Ch-D MODULE 39 containing "SVE0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



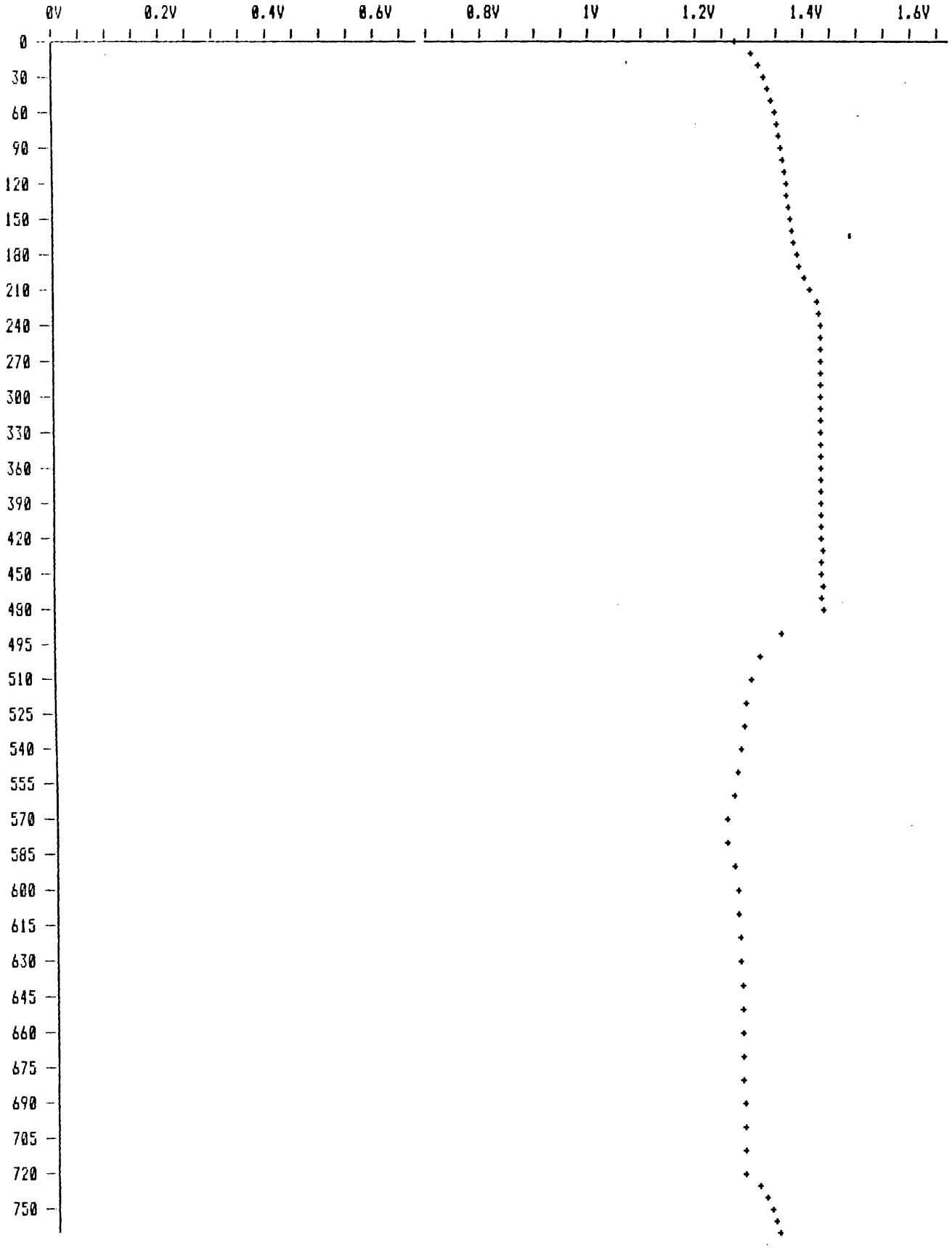
Graph 8(h)

"RUN 400" : Ch-D MODULE 41 containing "SVE2" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



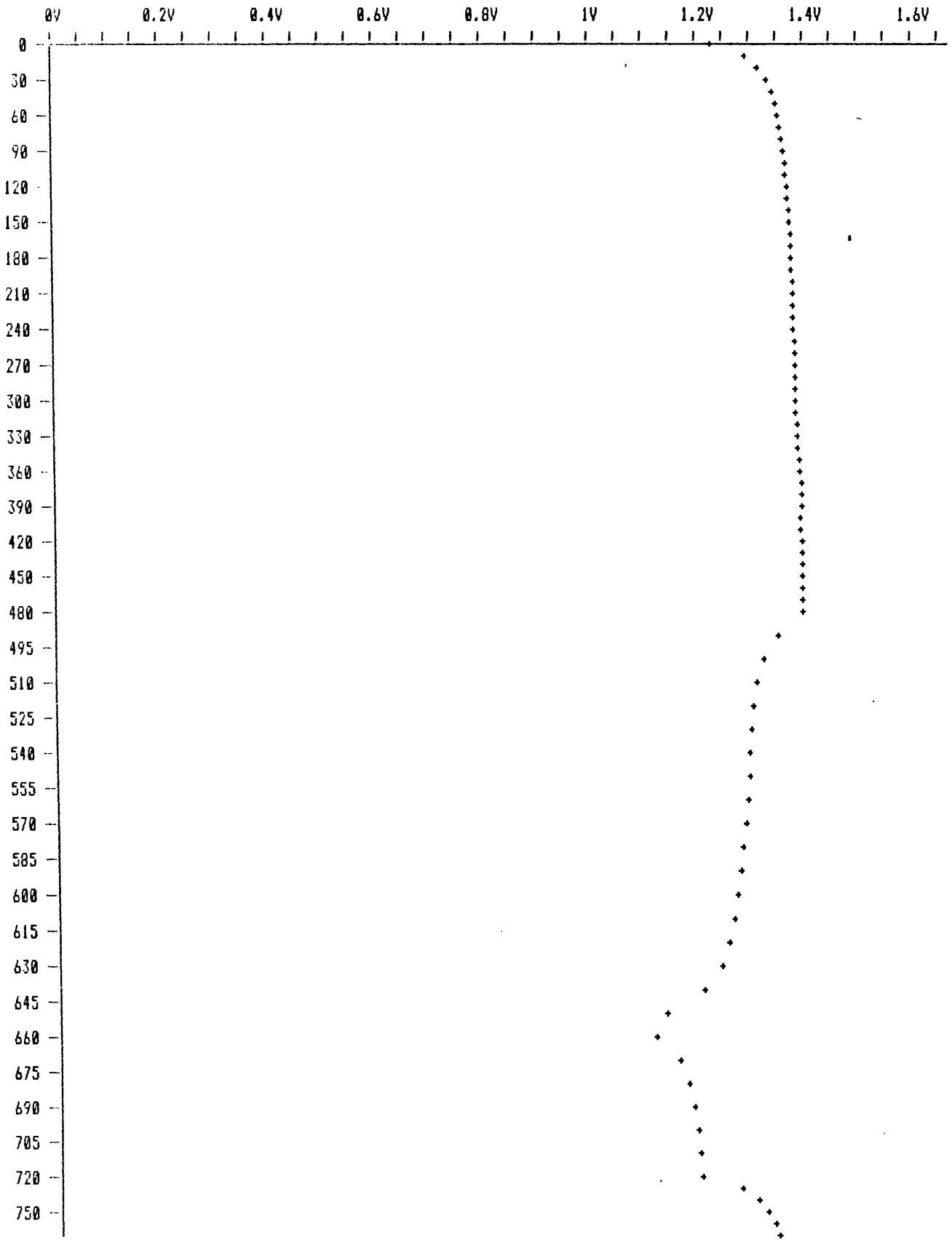
Graph 8(1)

"RUN 400" : Ch-D MODULE 42 containing "SVT0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

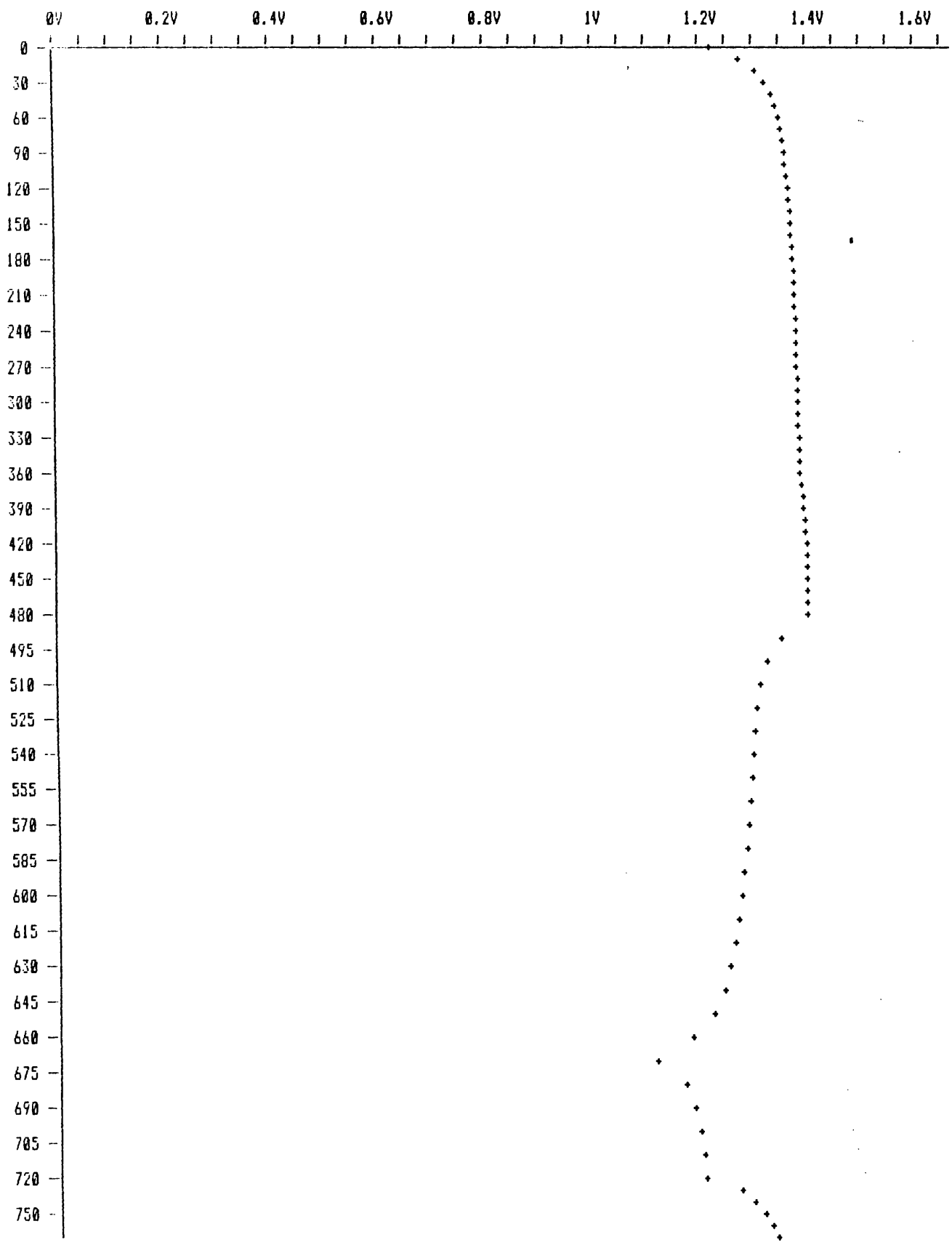


Graph 8(j)

"RUN 403" : Ch-D MODULE 43 containing "PP13" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

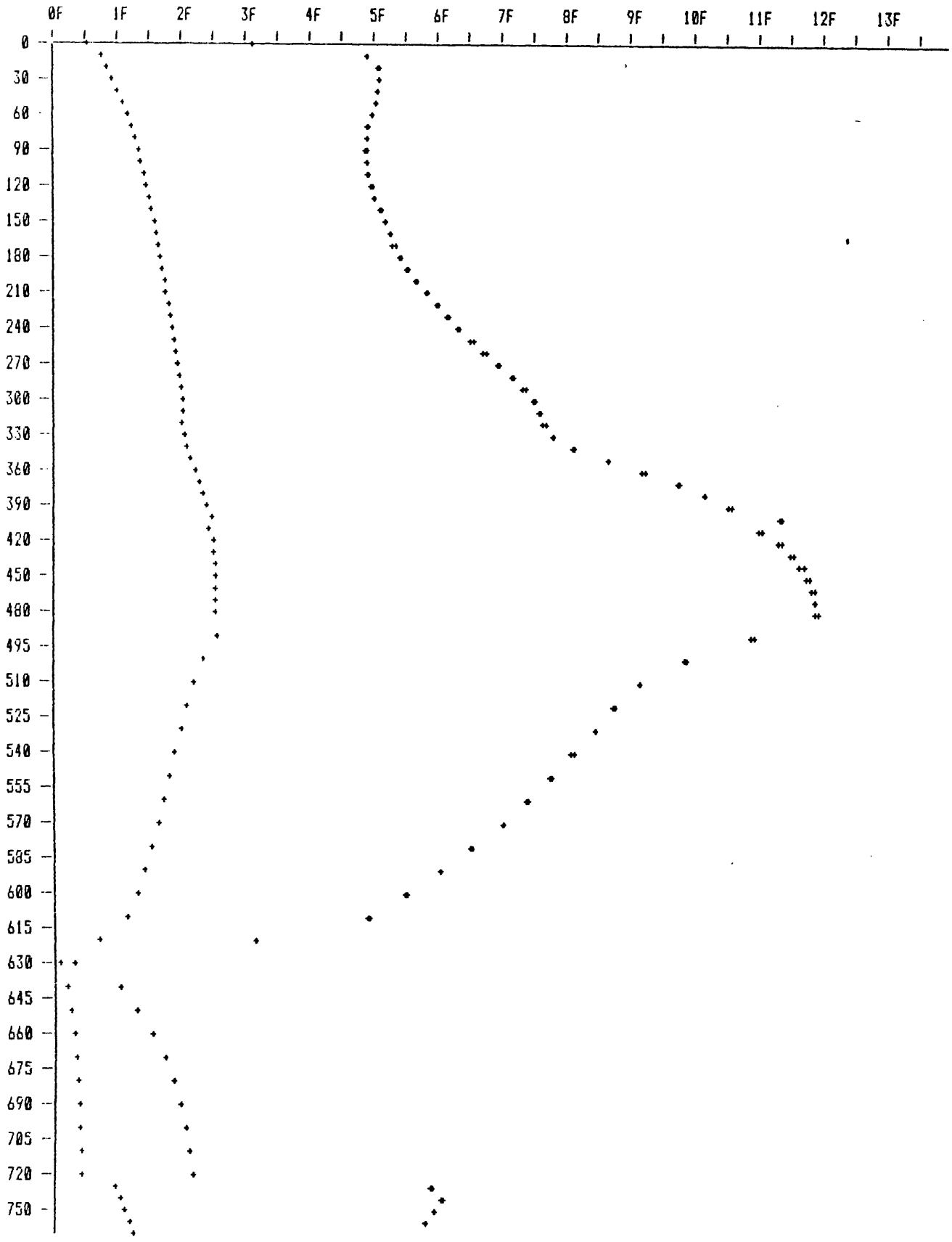


Graph 8(K)


"RUN 400" : Ch-D MODULE 44 containing "PP7" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Note: Curve order is 32Hz >>> 2Hz pair

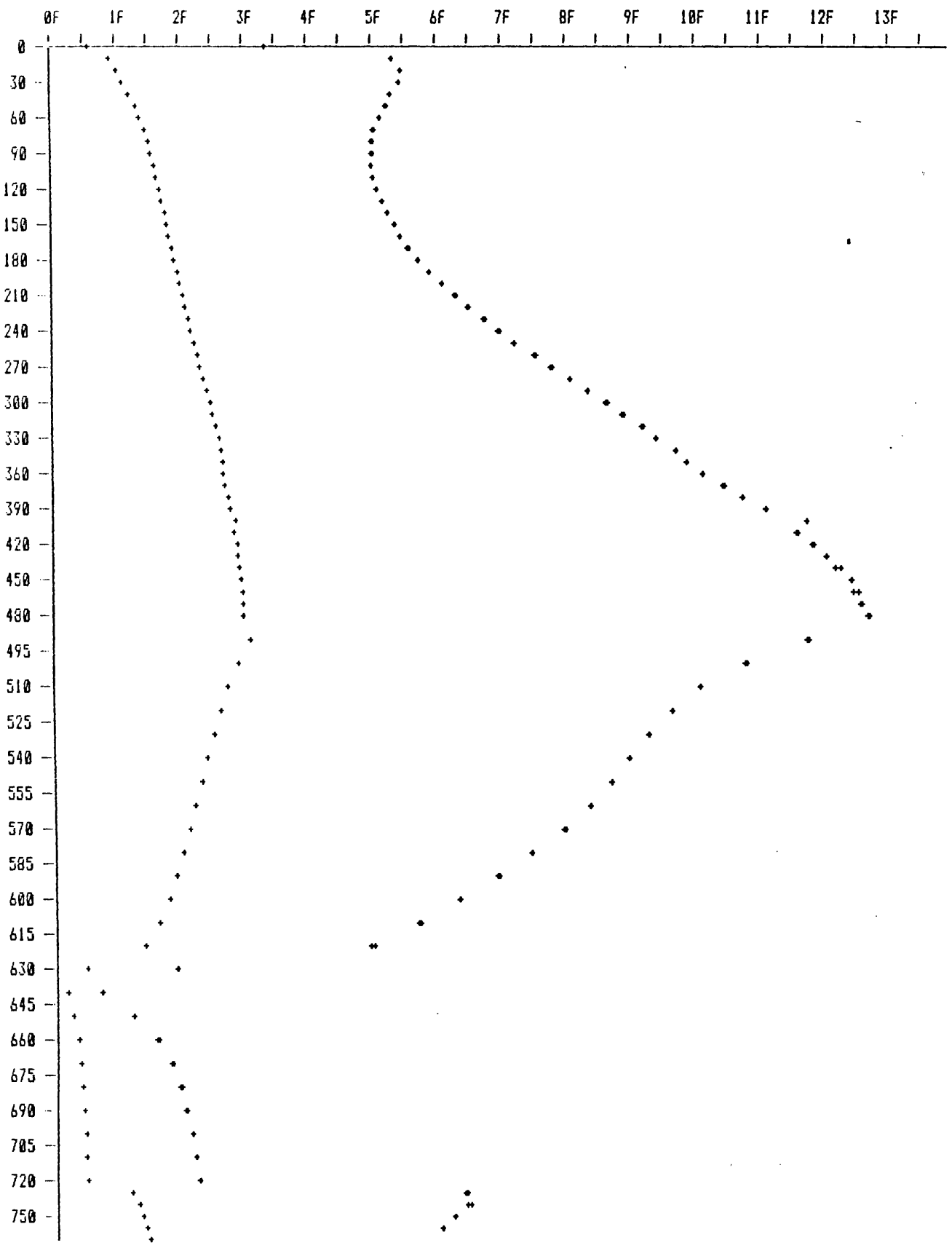
"RUN 400" : Ch-D MODULE 24 containing "P6P20" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 3(m)

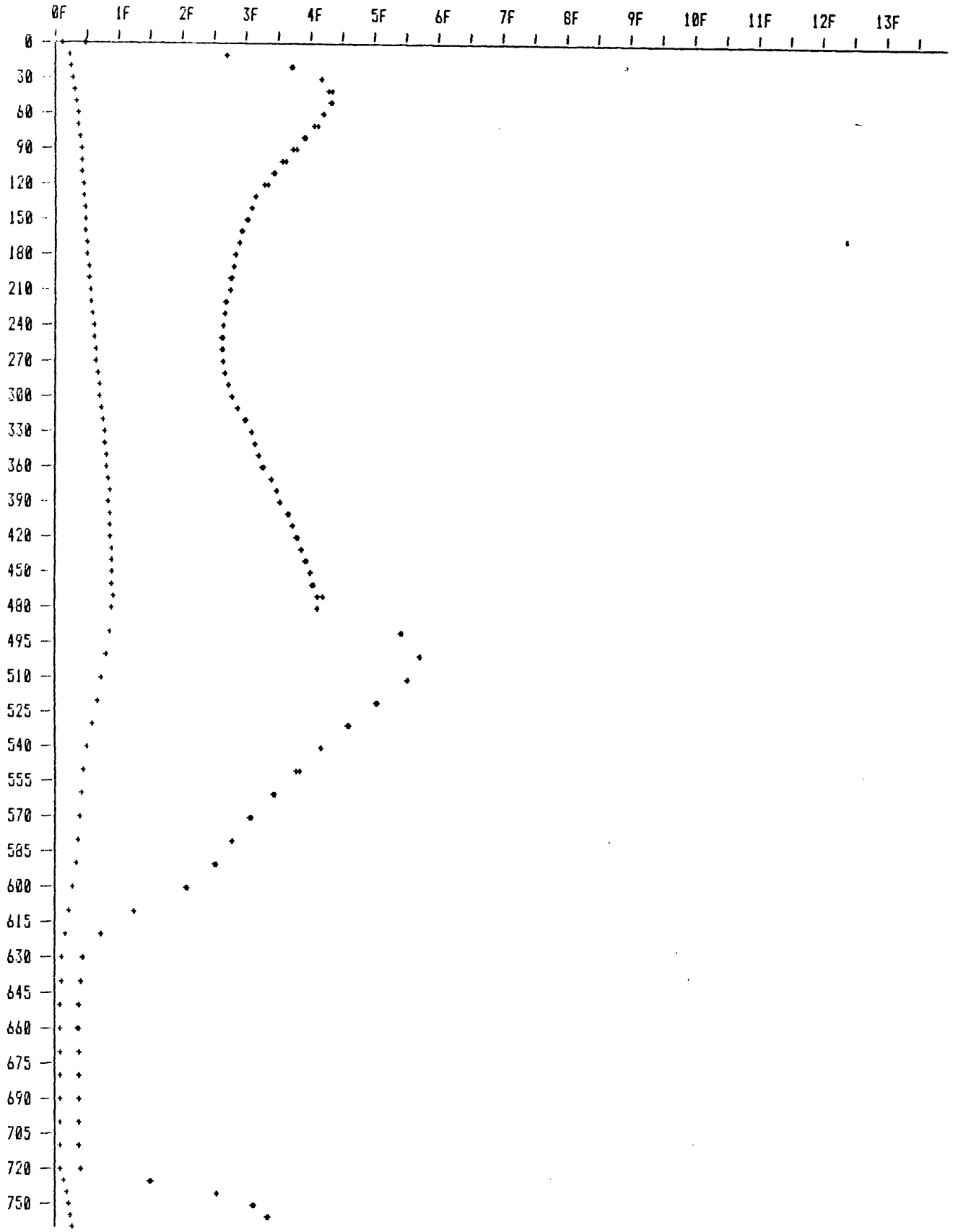
Note: Curve order is 32Hz >>> 2Hz pair

"RUN 400" : Ch-D MODULE 25 containing "P6P21" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Note: Curve order is 32Hz >>> 2Hz pair

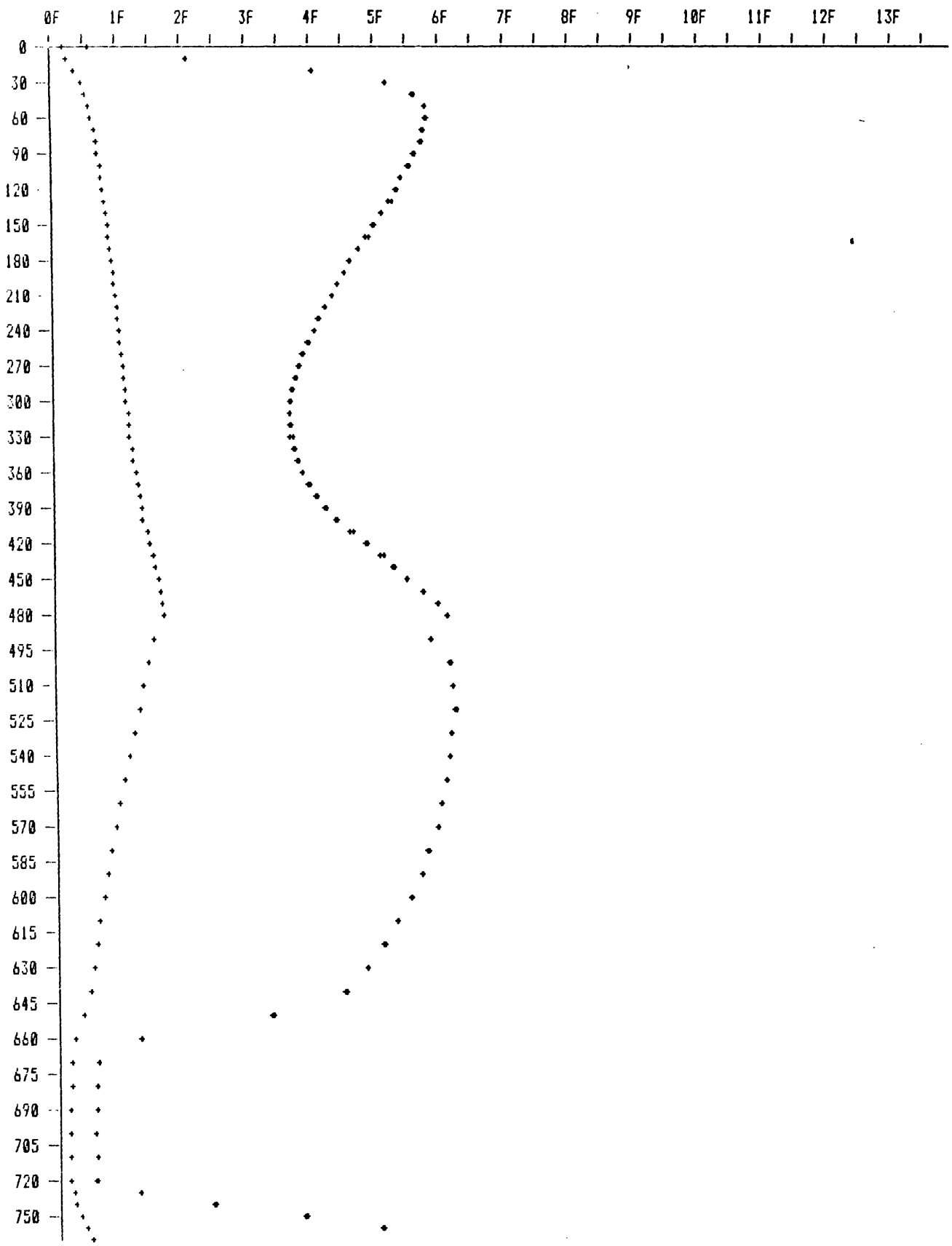
"RUN 400" : Ch-D MODULE 32 containing "HP1" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(8)

Note: Curve order is 32Hz >>> 2Hz pair

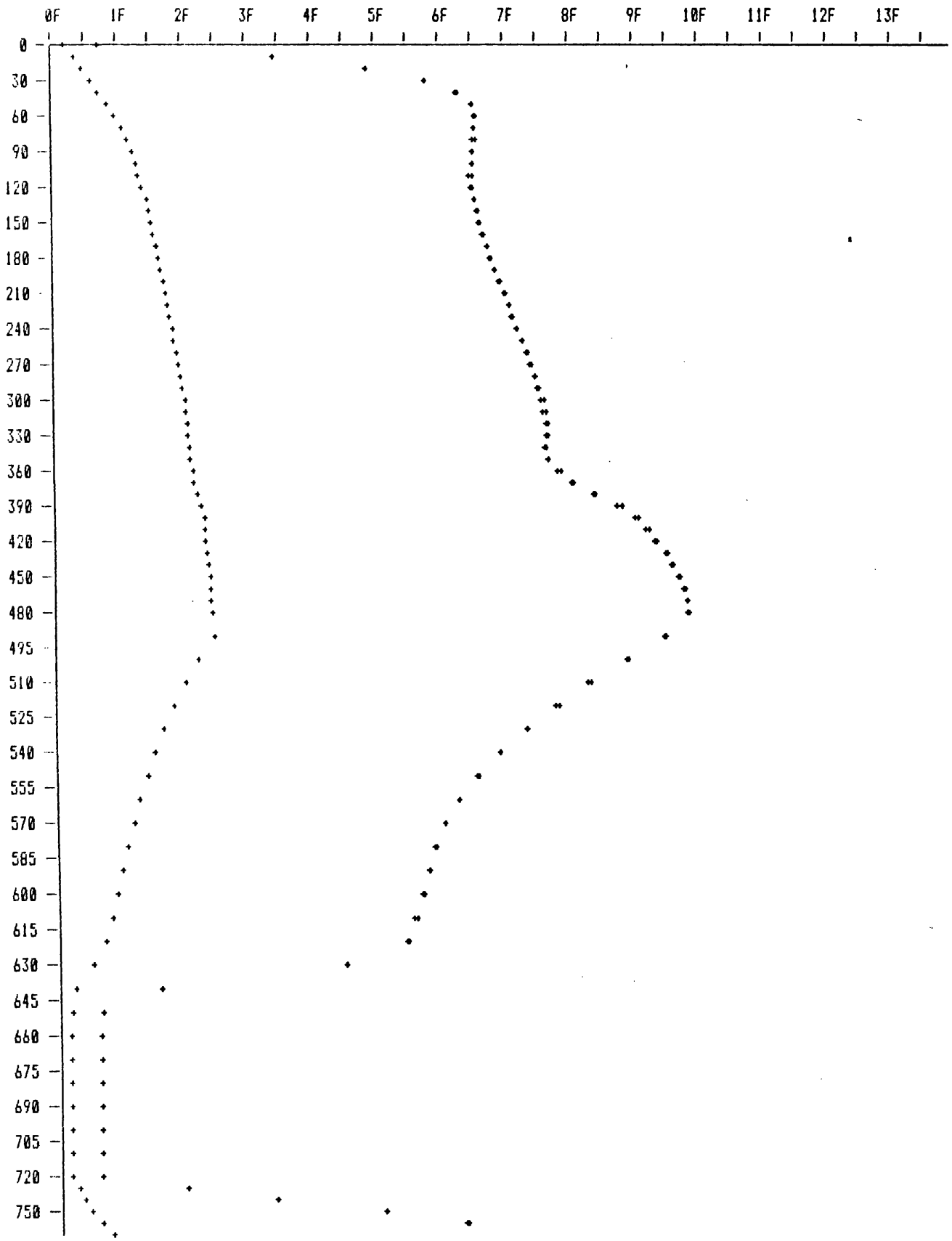
"RUN 400" : Ch-D MODULE 33 containing "HP2" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(p)

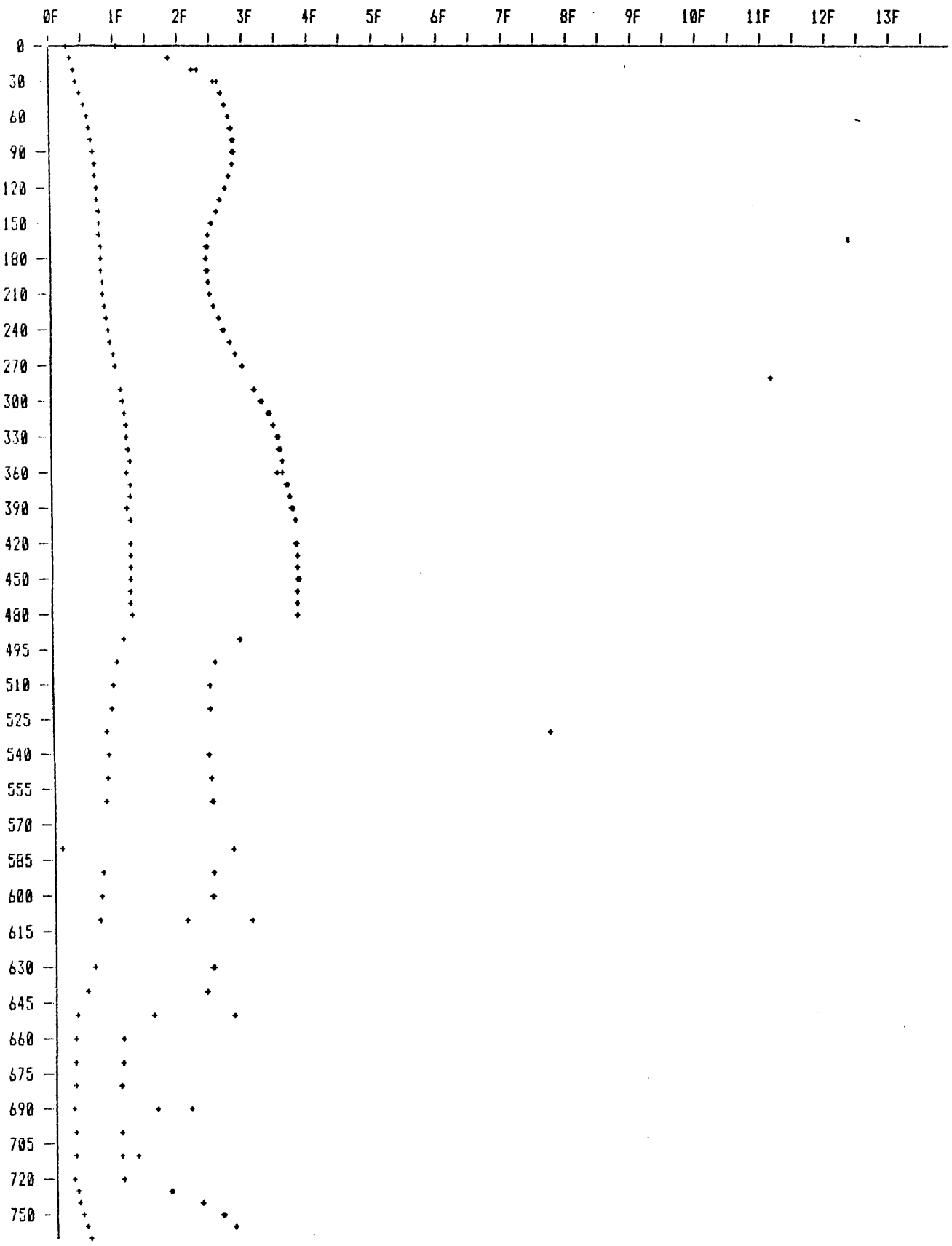
Note: Curve order is 32Hz >>> 2Hz pair

"RUN 400" : Ch-D MODULE 35 containing "VA0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Note: Curve order is 32Hz >>> 2Hz pair

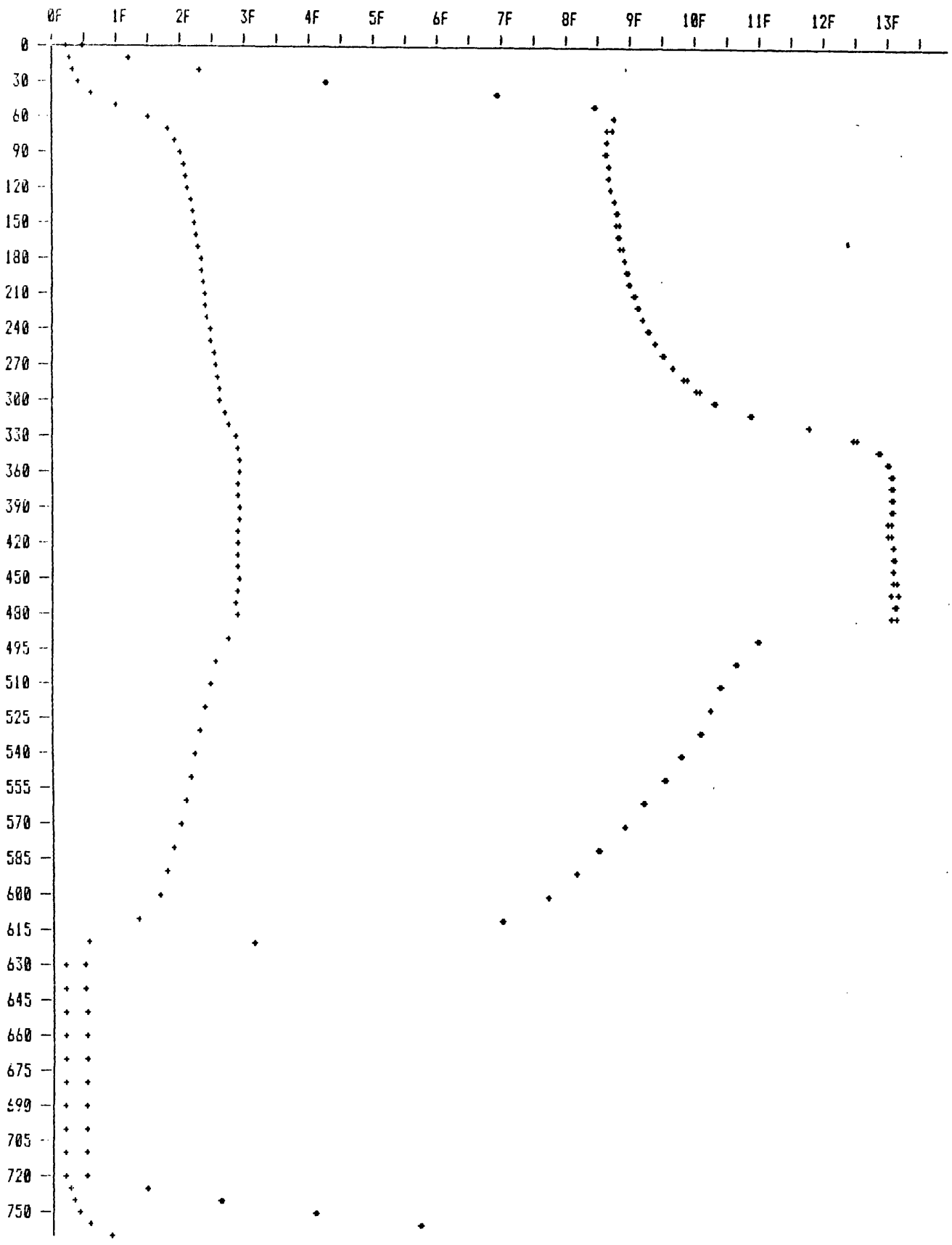
"RUN 400" : Ch-D MODULE 36 containing "CC0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 3(1)

Note: Curve order is 32Hz >>> 2Hz pair

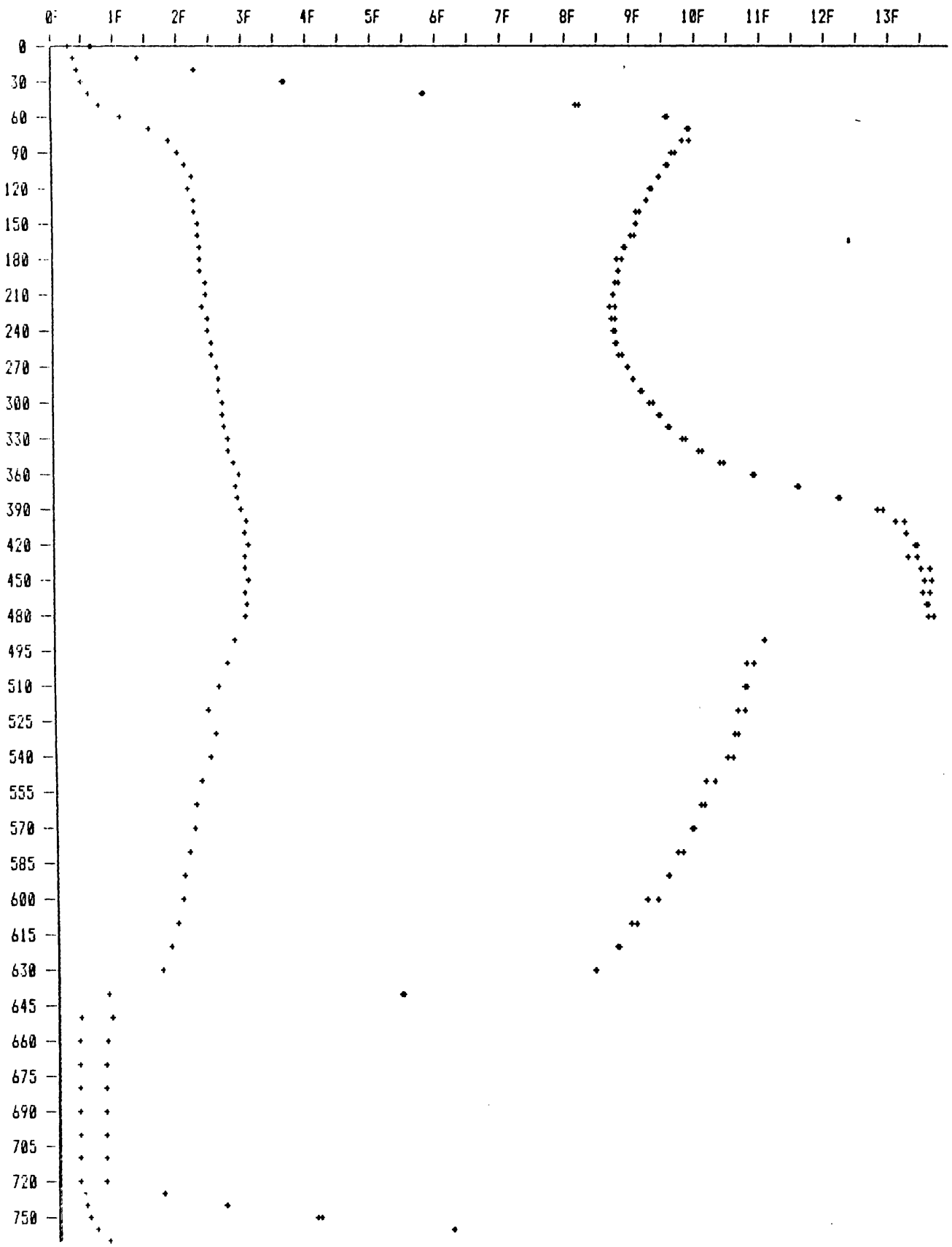
"RUN 400" : Ch-D MODULE 39 containing "SVE0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(s)

Note: Curve order is 32Hz >>> 2Hz pair

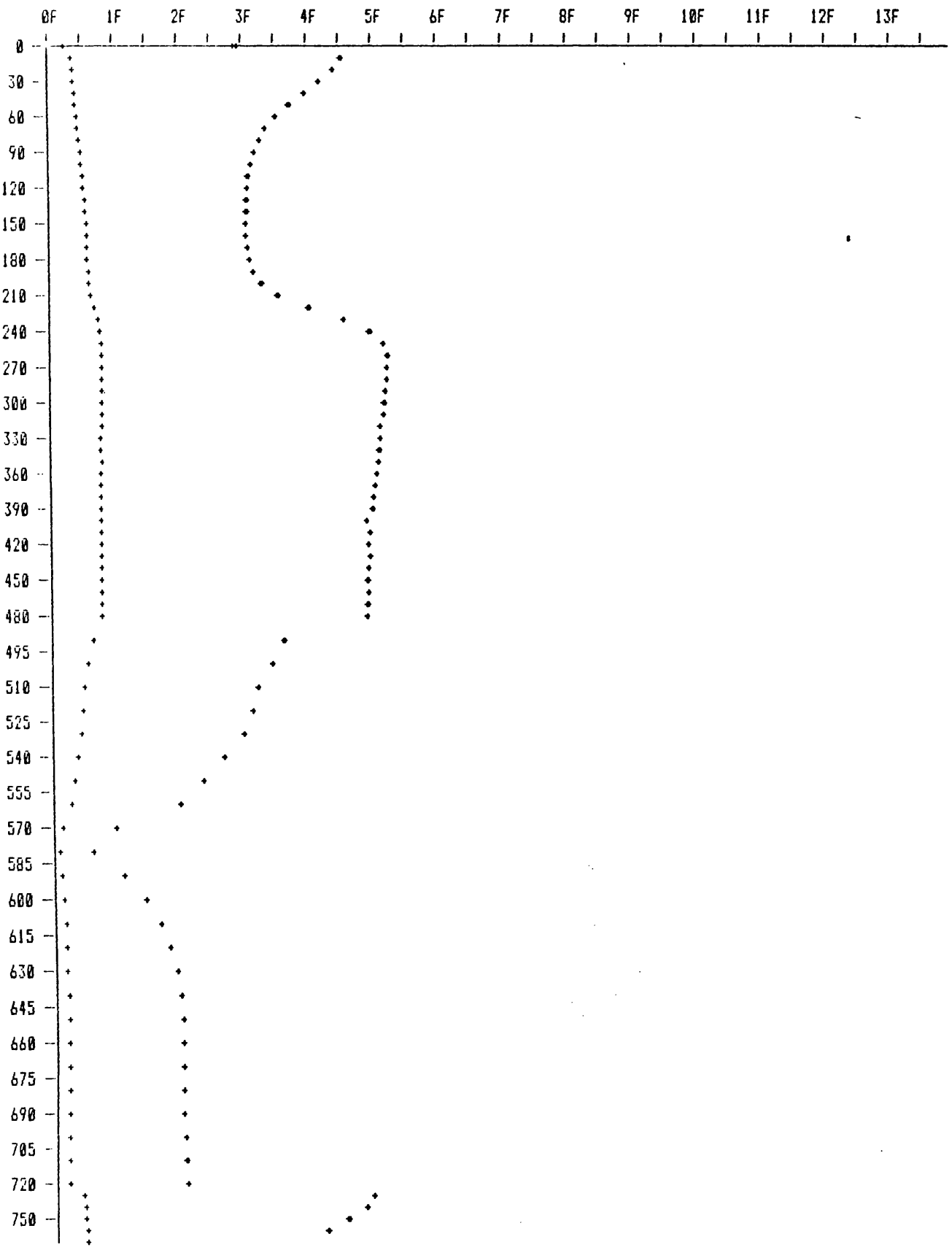
"RUN 400" : Ch-D MODULE 41 containing "SVE2" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(t)

Note: Curve order is 32Hz >>> 2Hz pair

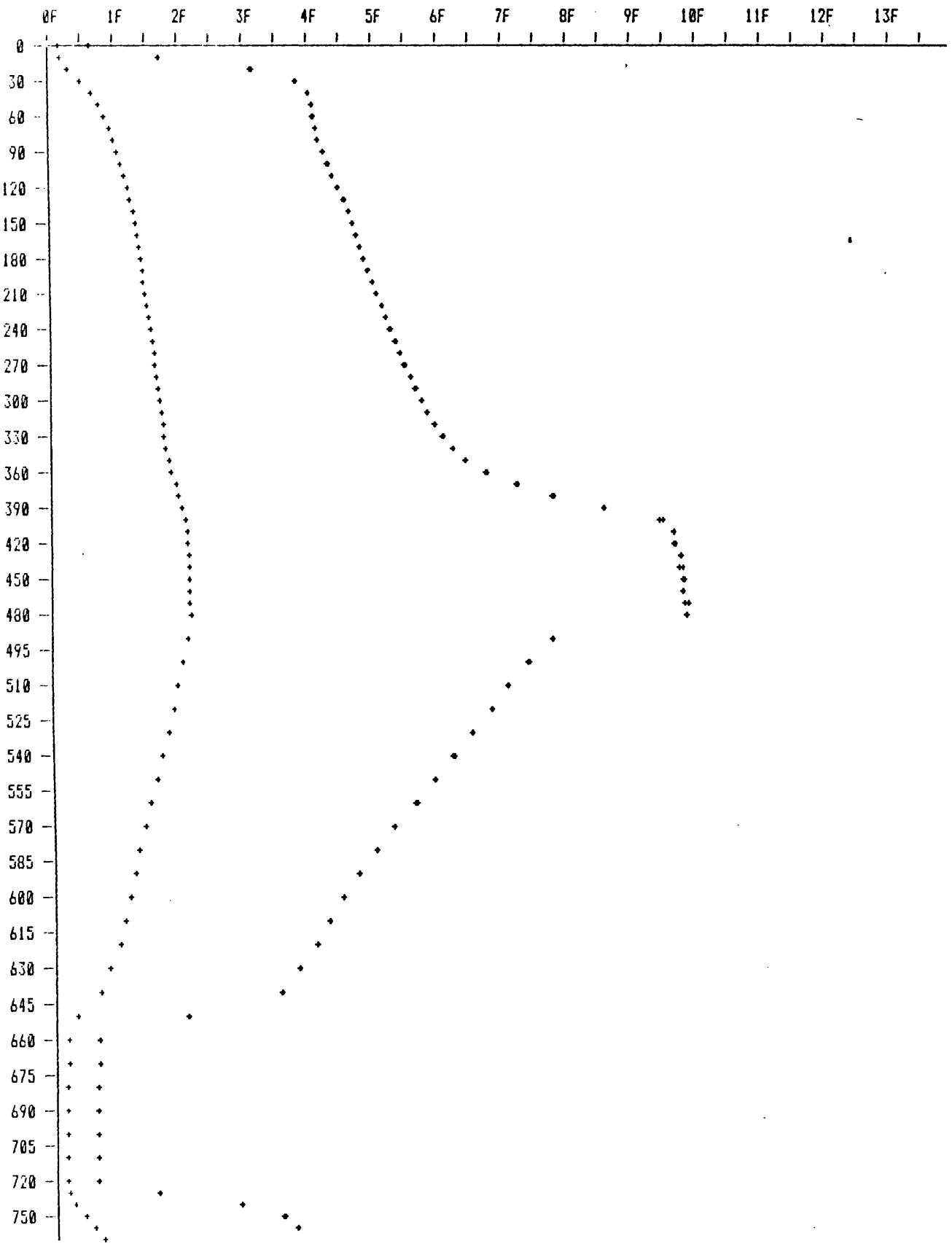
"RUN 400" : Ch-D MODULE 42 containing "SVT0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(u)

Note: Curve order is 32Hz >>> 2Hz pair

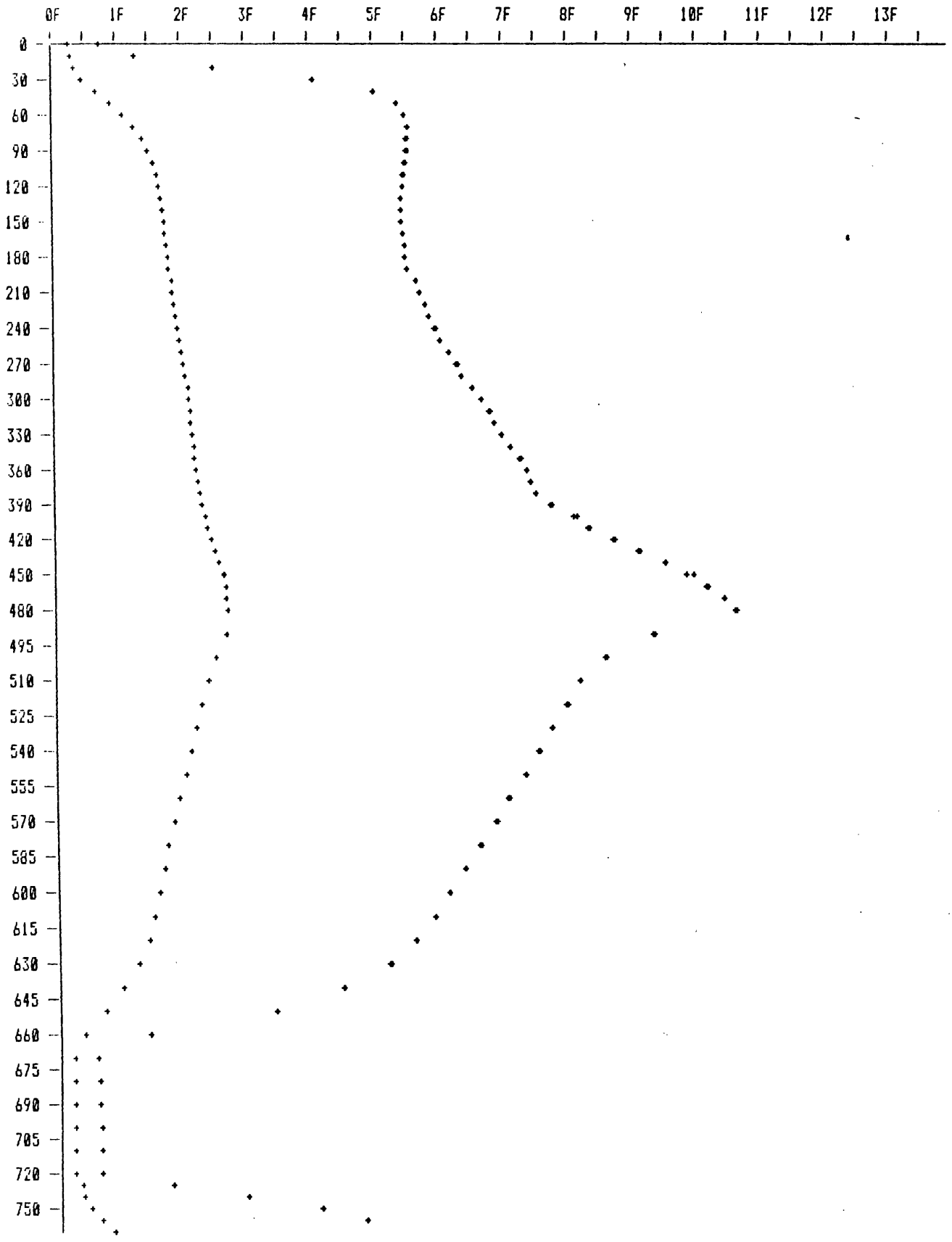
"RUN 400" : Ch-D MODULE 43 containing "PP13" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(V)

Note: Curve order is 32Hz >>> 2Hz pair

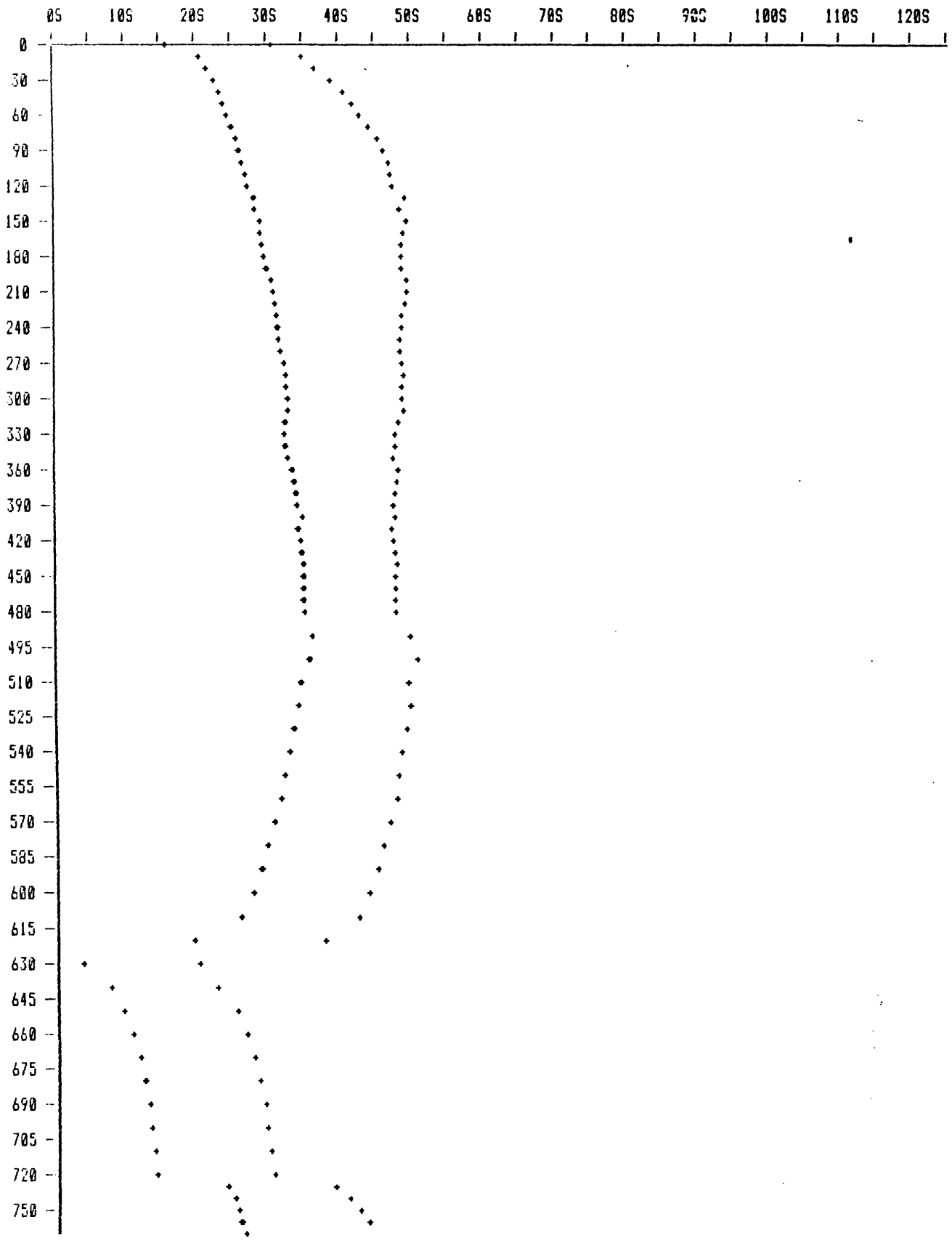
"RUN 400" : Ch-D MODULE 44 containing "PP7" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 8(W)

Note: Curve order is 2Hz pair >>> 32Hz

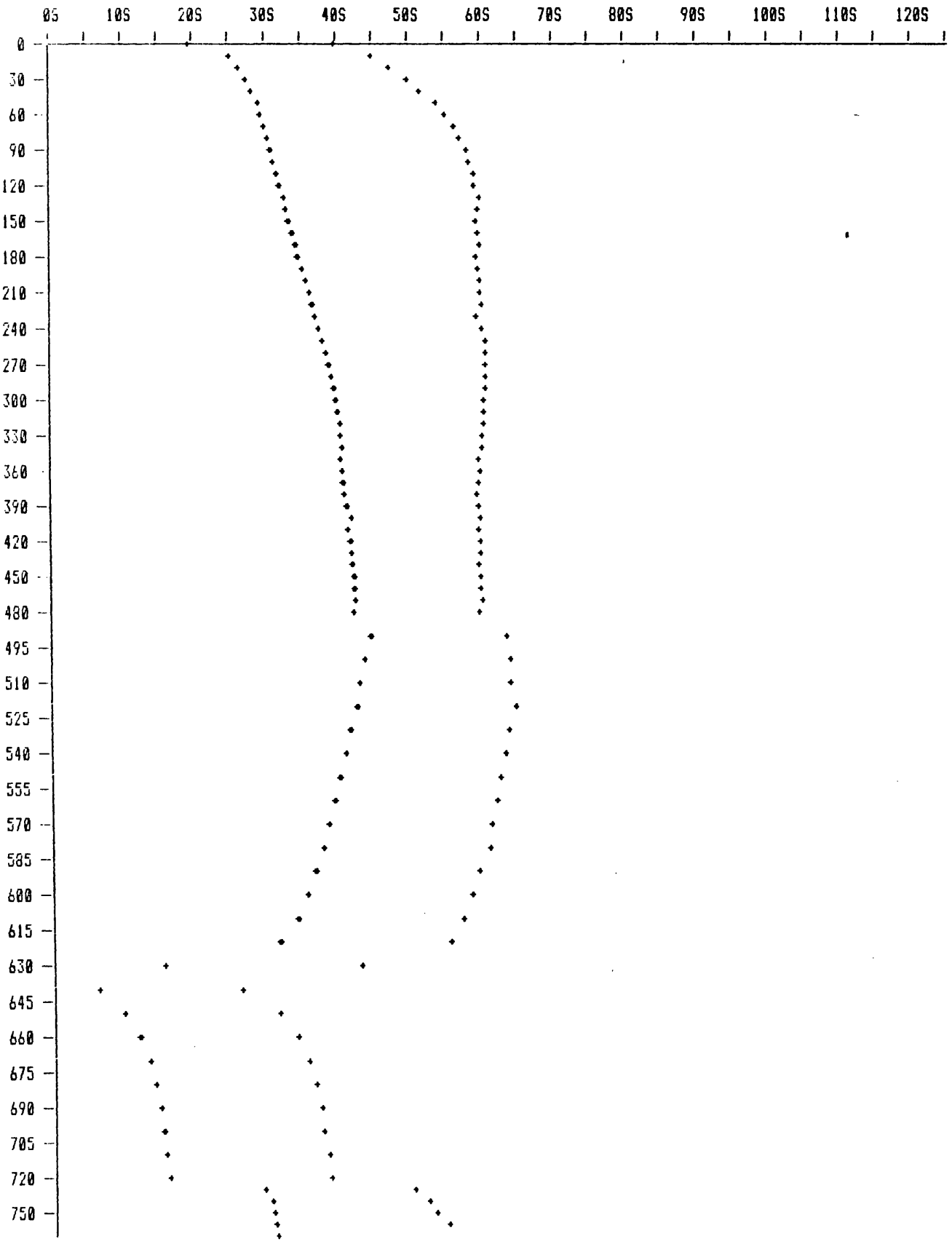
"RUN 400" : Ch-D MODULE 24 containing "P&P20" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 8(x)

Note: Curve order is 2Hz pair >>> 32Hz

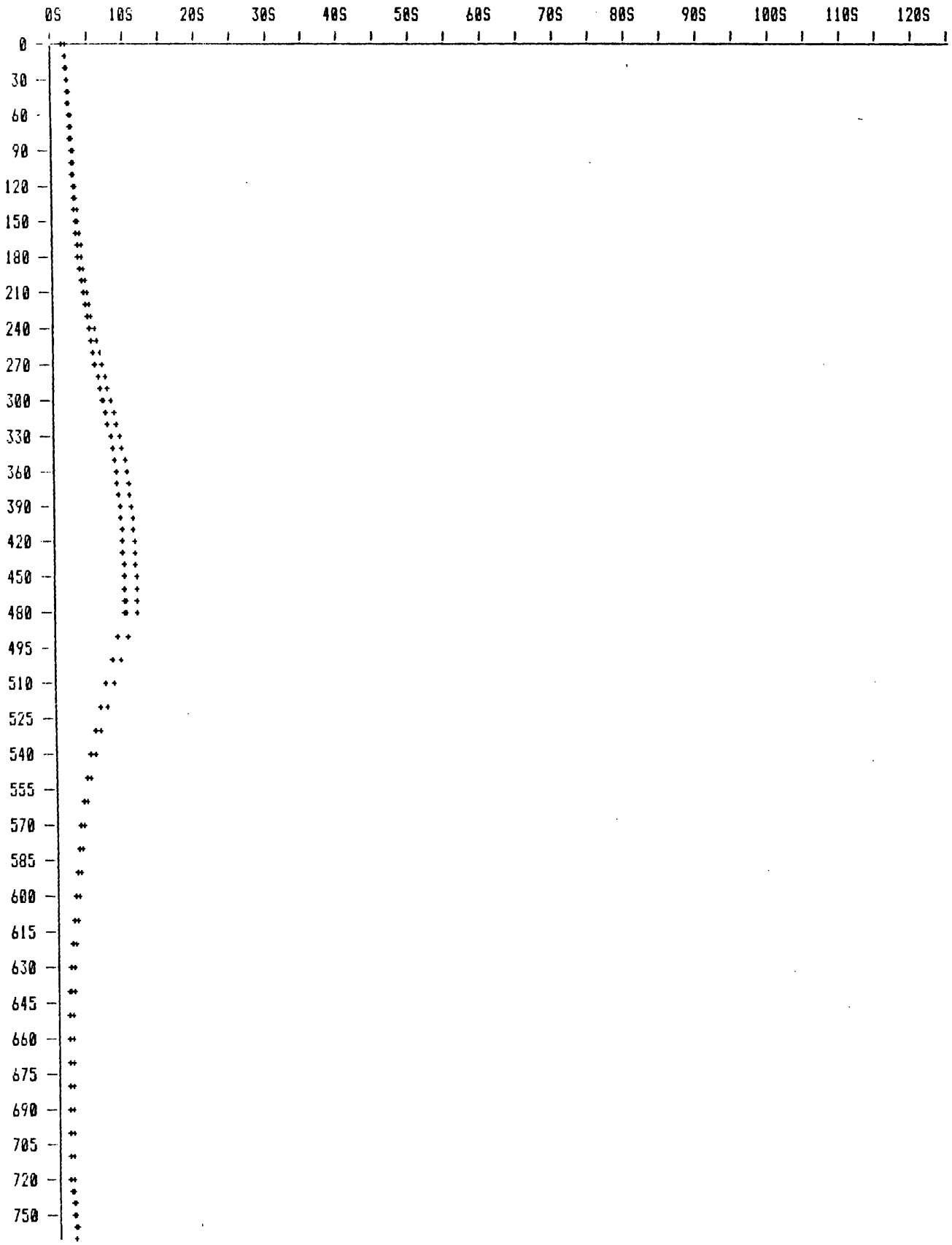
"RUN 400" : Ch-D MODULE 25 containing "P6P21" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 8(y)

Note: Curve order is 2Hz pair >>> 32Hz

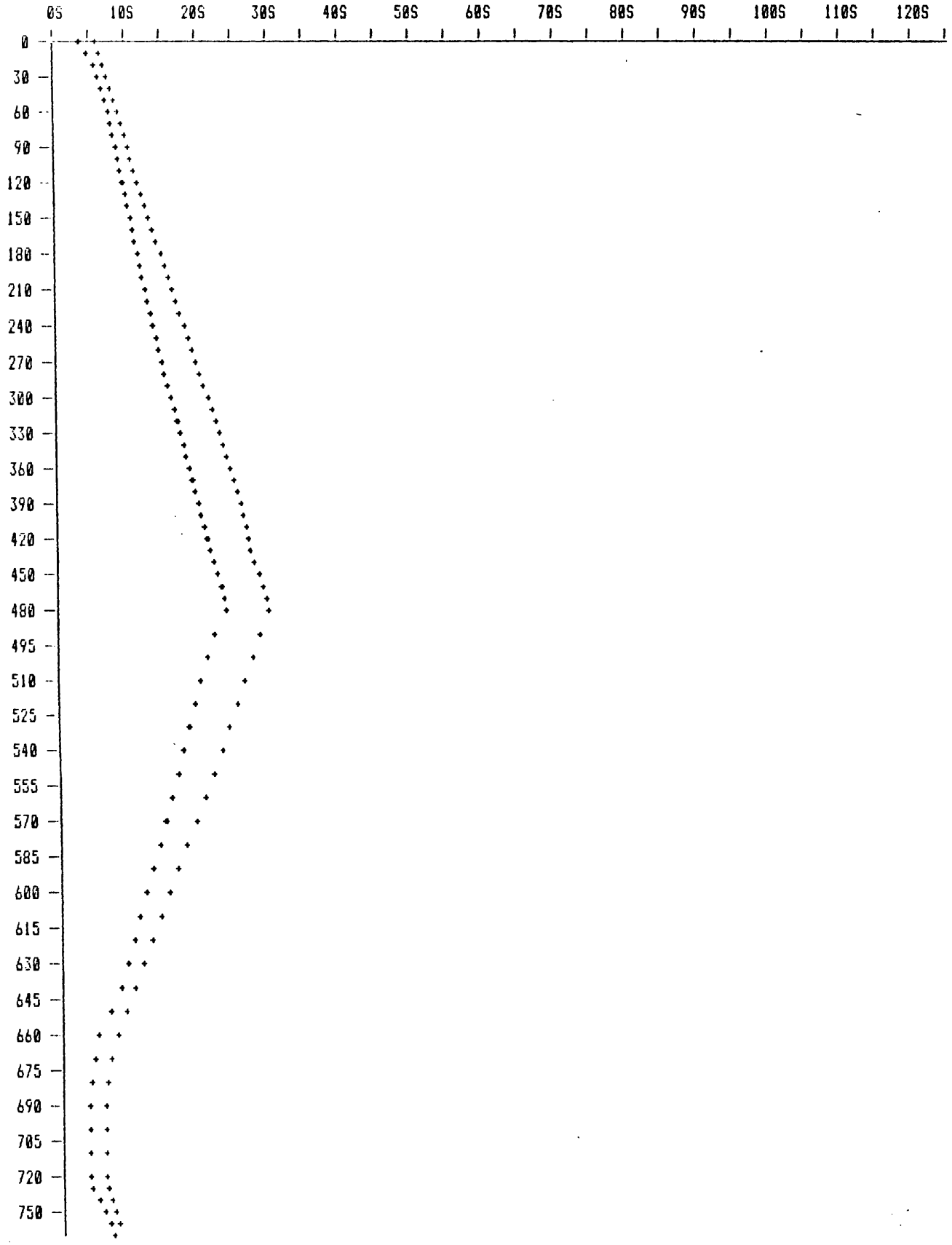
"RUN 400" : Ch-D MODULE 32 containing "HF1" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 8(2)

Note: Curve order is 2Hz pair >>> 32Hz

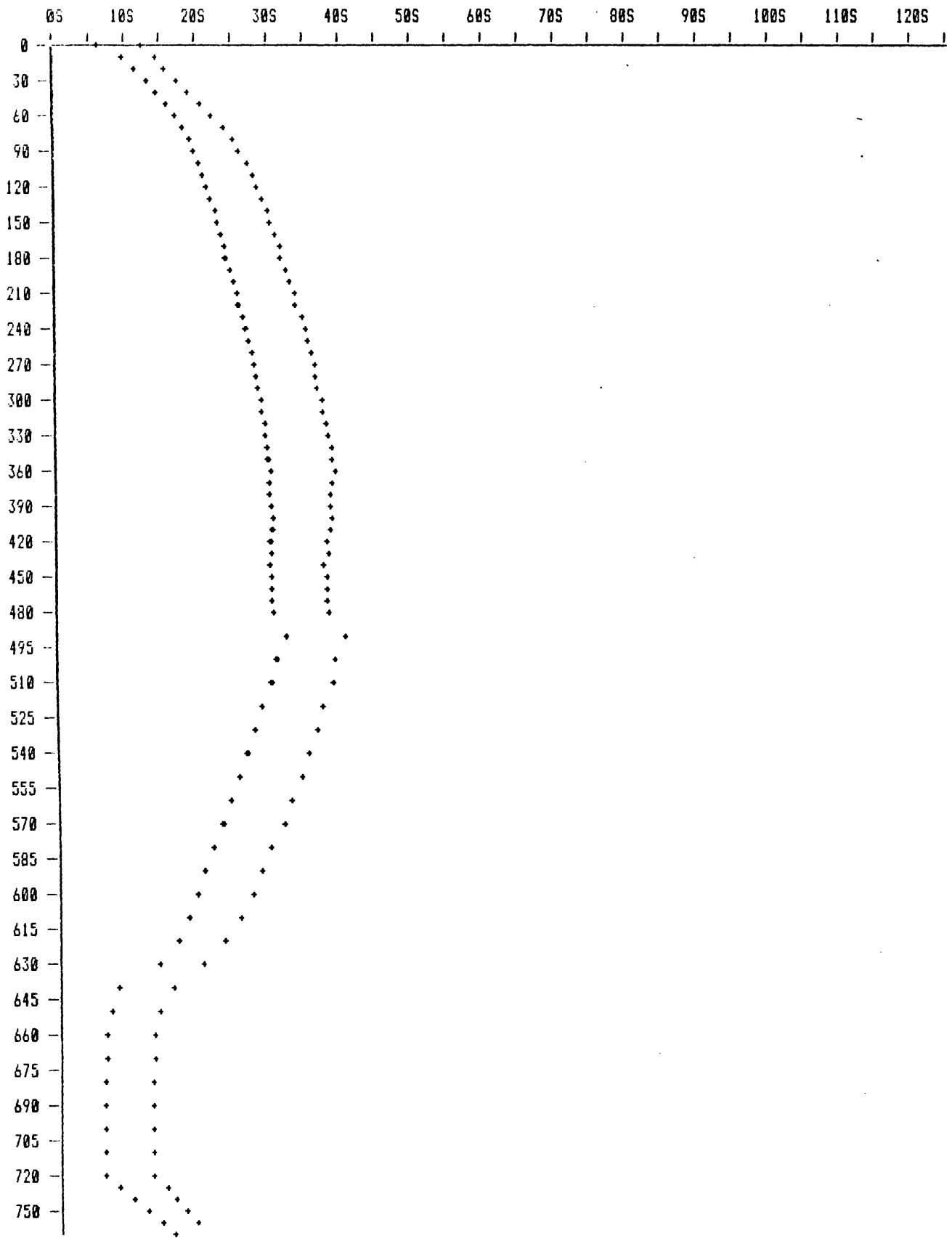
"RUN 400" : Ch-D MODULE 33 containing "HP2" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 8(aa)

Note: Curve order is 2Hz pair >>> 32Hz

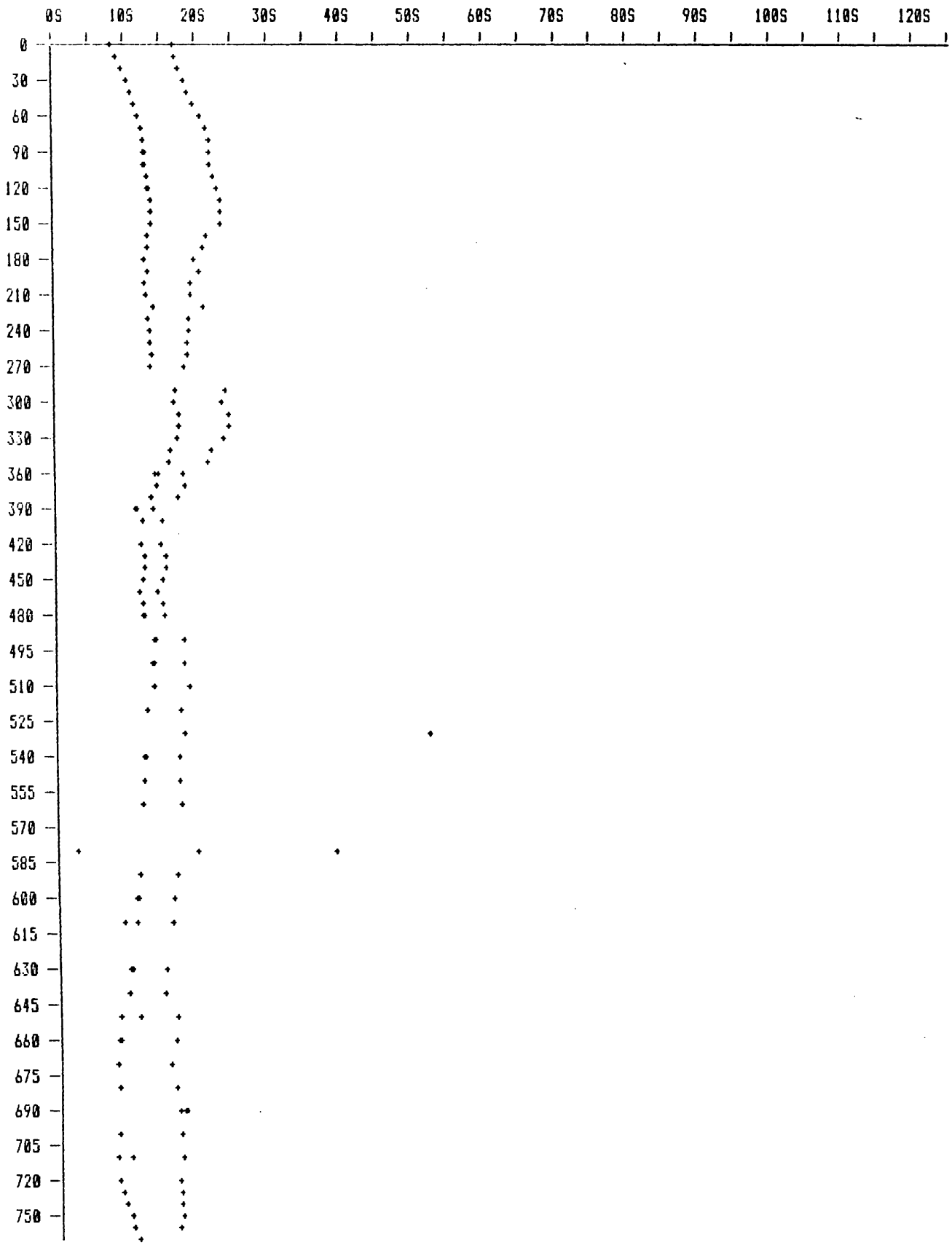
"RUN 400" : Ch-D MODULE 35 containing "VA0" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 8(BB)

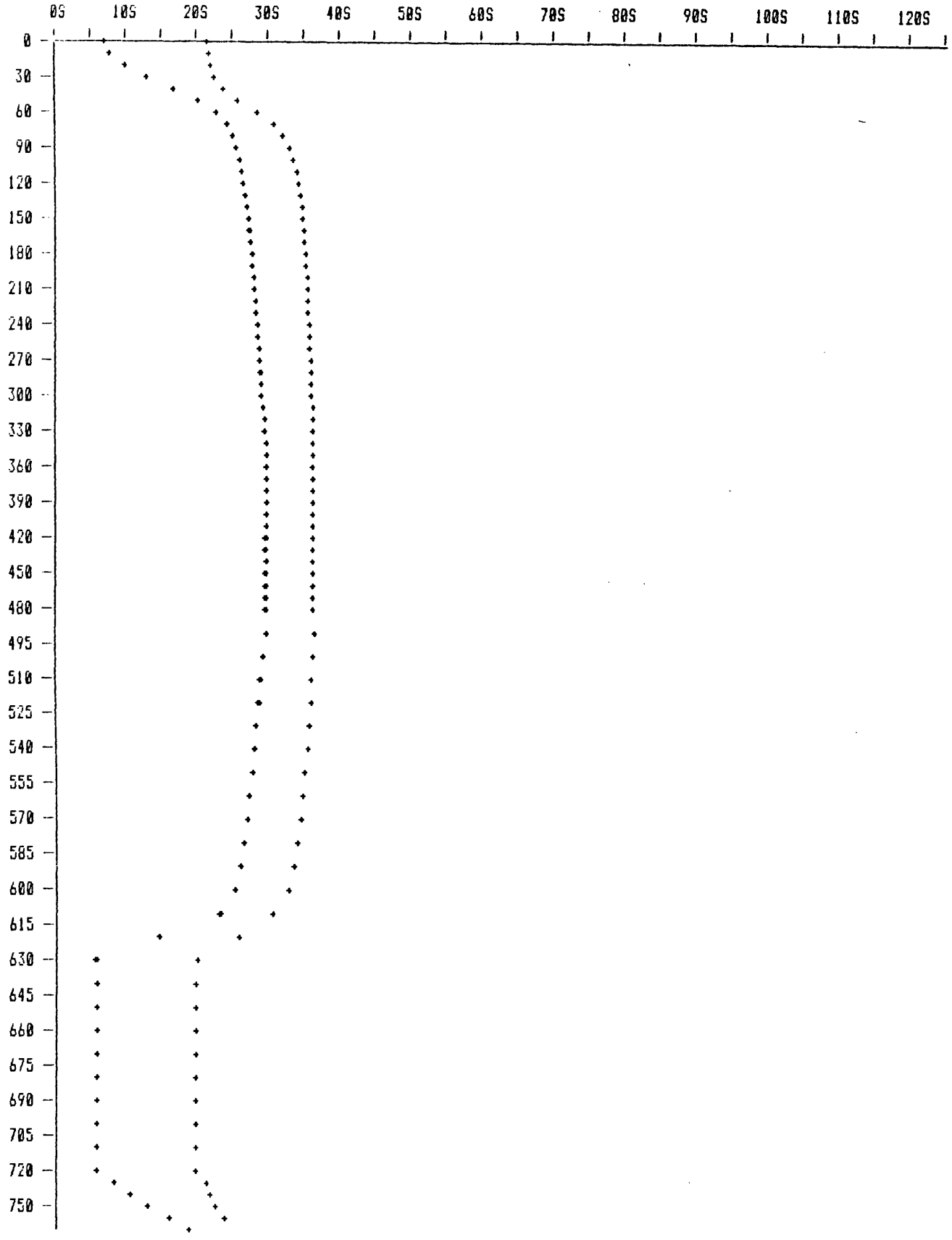
Note: Curve order is 2Hz pair >>> 32Hz

"RUN 400" : Ch-D MODULE 36 containing "CC0" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Note: Curve order is 2Hz pair >>> 32Hz

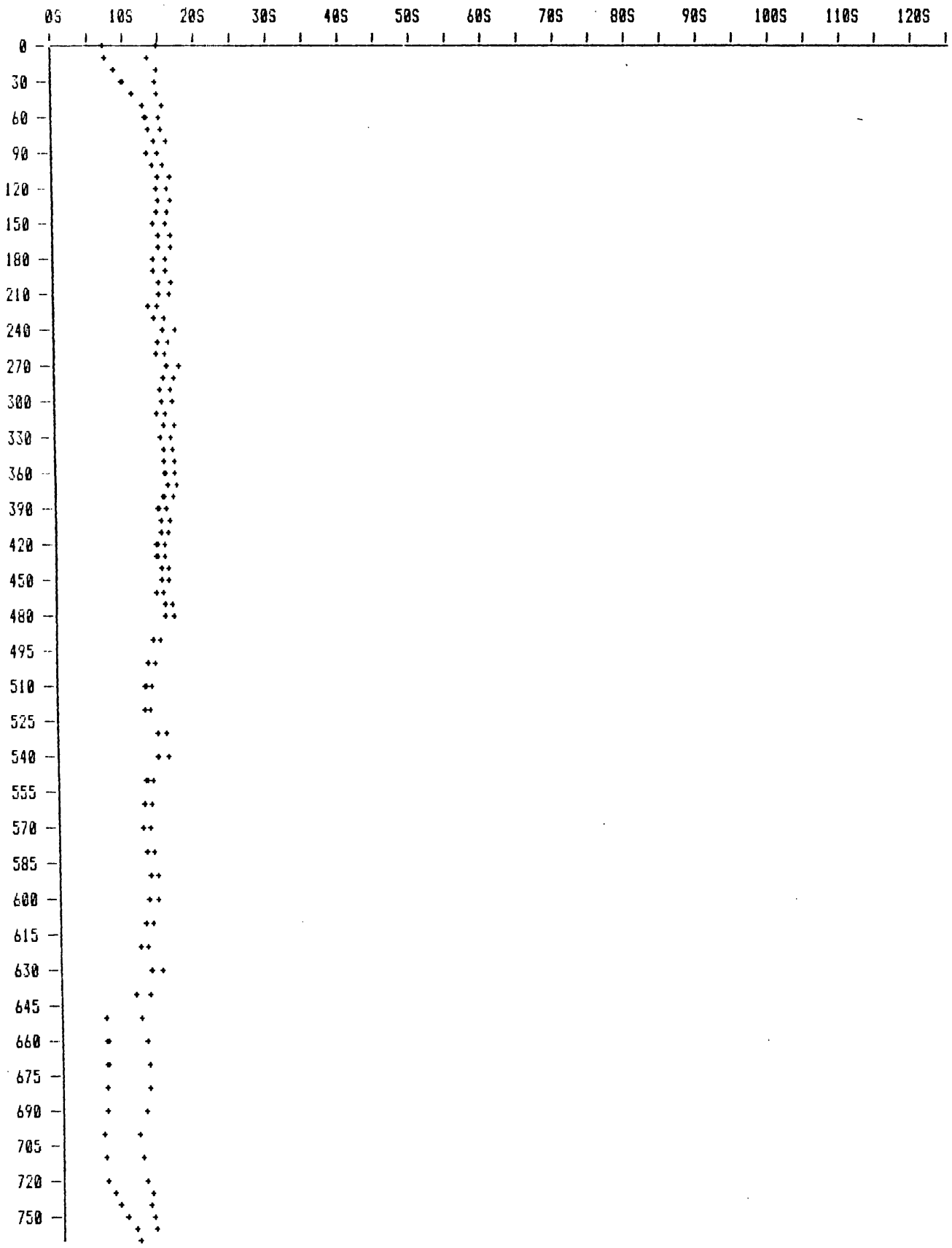
"RUN 400" : Ch-D MODULE 39 containing "SVE0" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 3(dd)

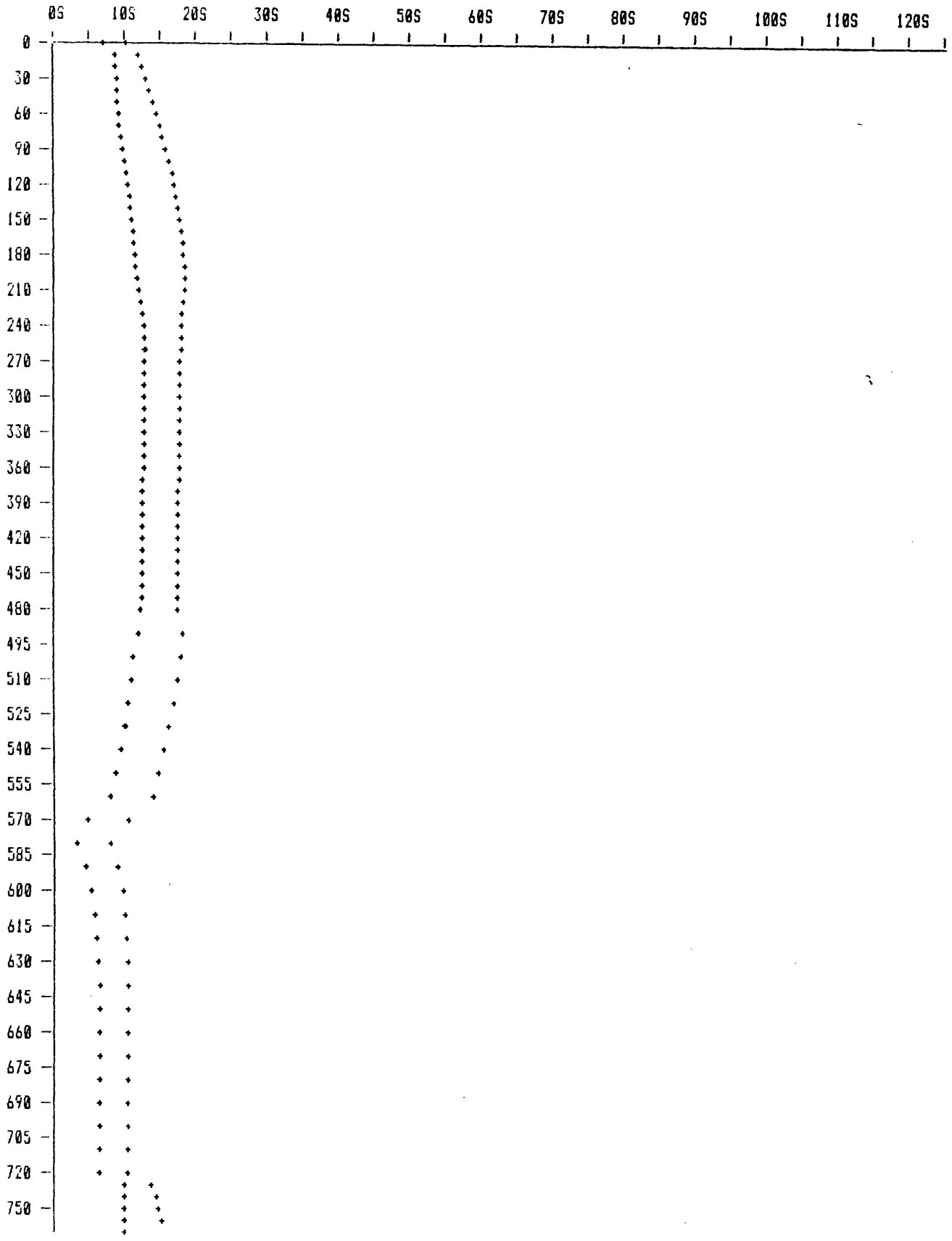
Note: Curve order is 2Hz pair >>> 32Hz

"RUN 400" : Ch-D MODULE 41 containing "SVE2" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Note: Curve order is 2Hz pair >>> 32Hz

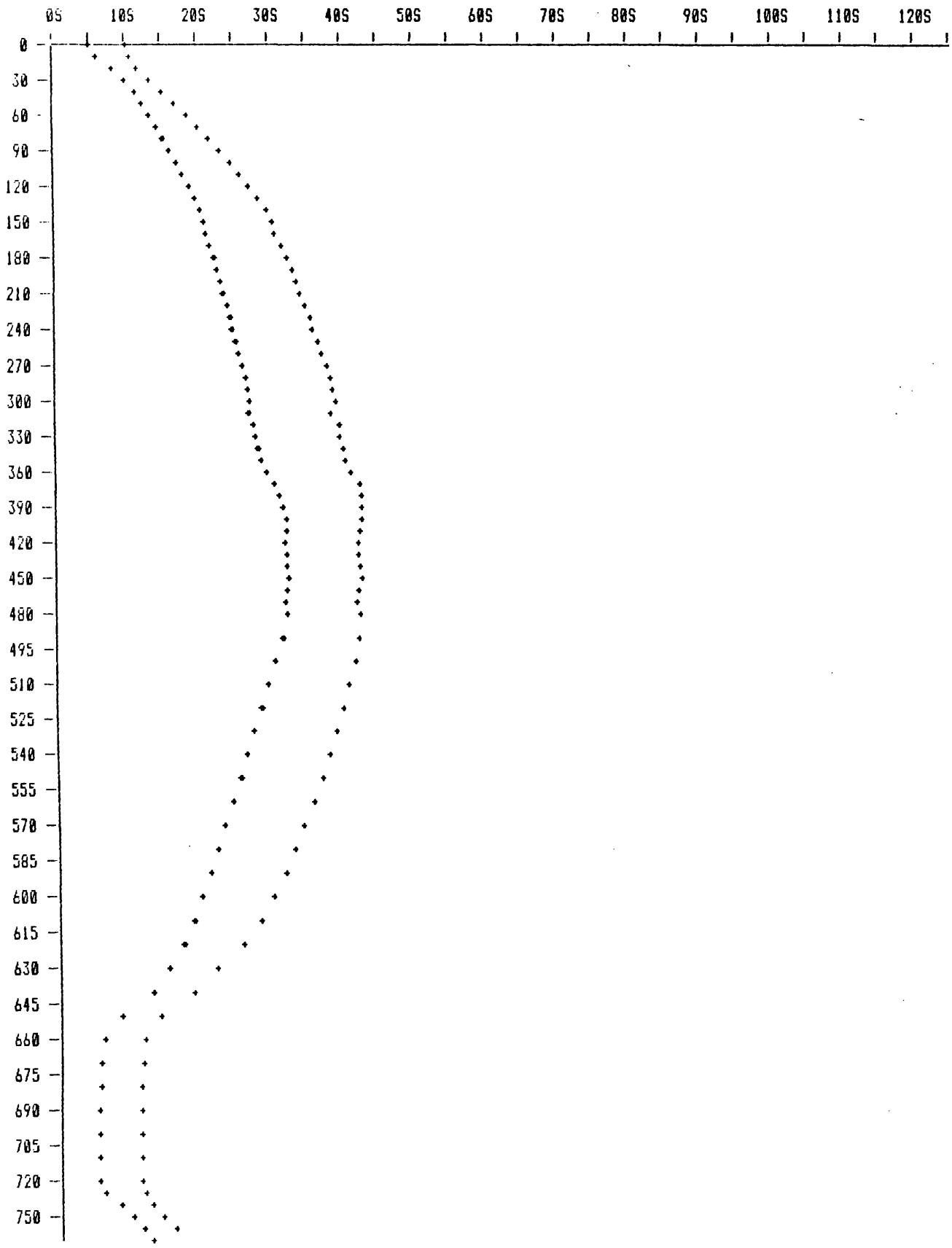
"RUN 400" : Ch-D MODULE 42 containing "SVT0" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 3(11)

Note: Curve order is 2Hz pair >>> 32Hz

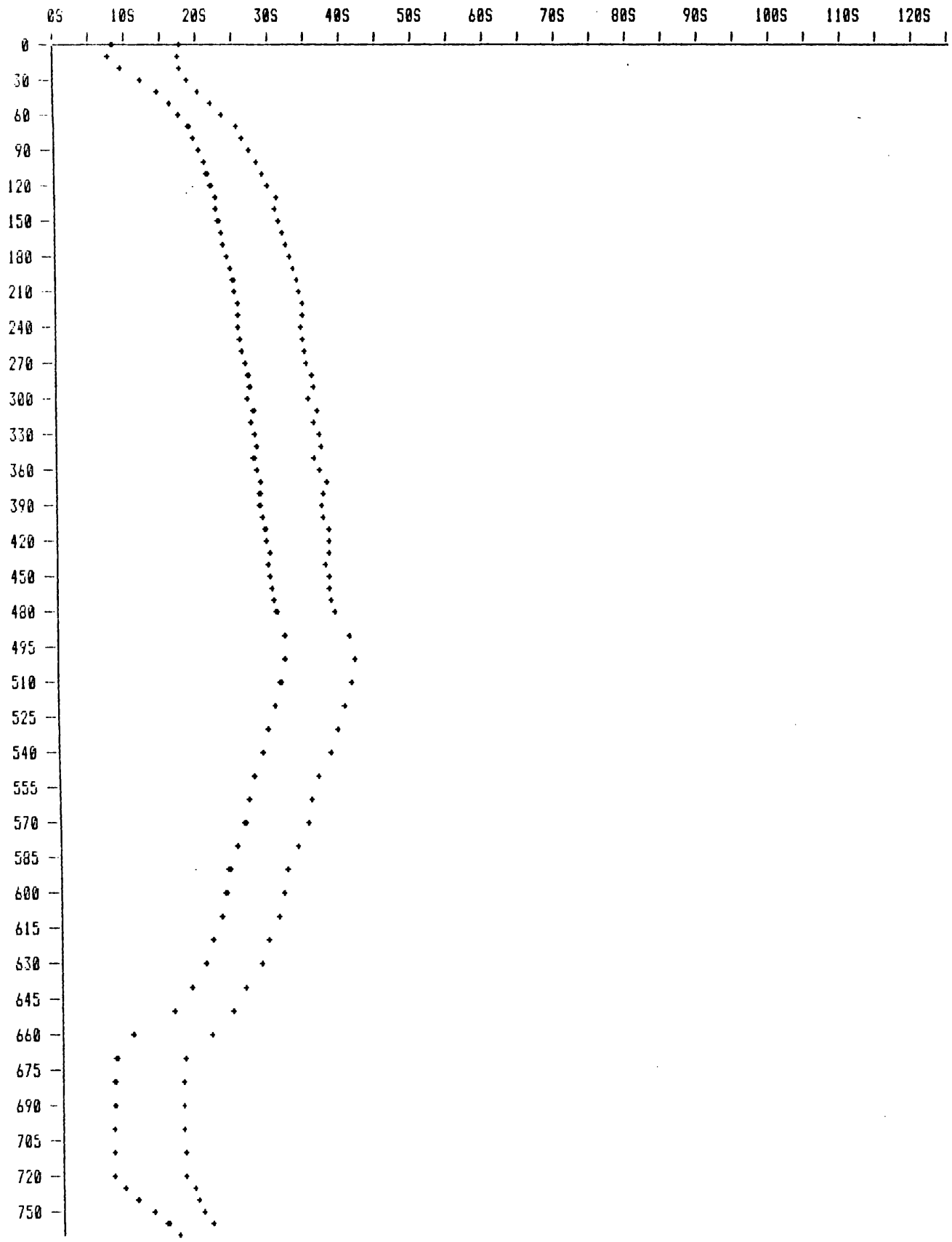
"RUN 400" : Ch-D MODULE 43 containing "PP13" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



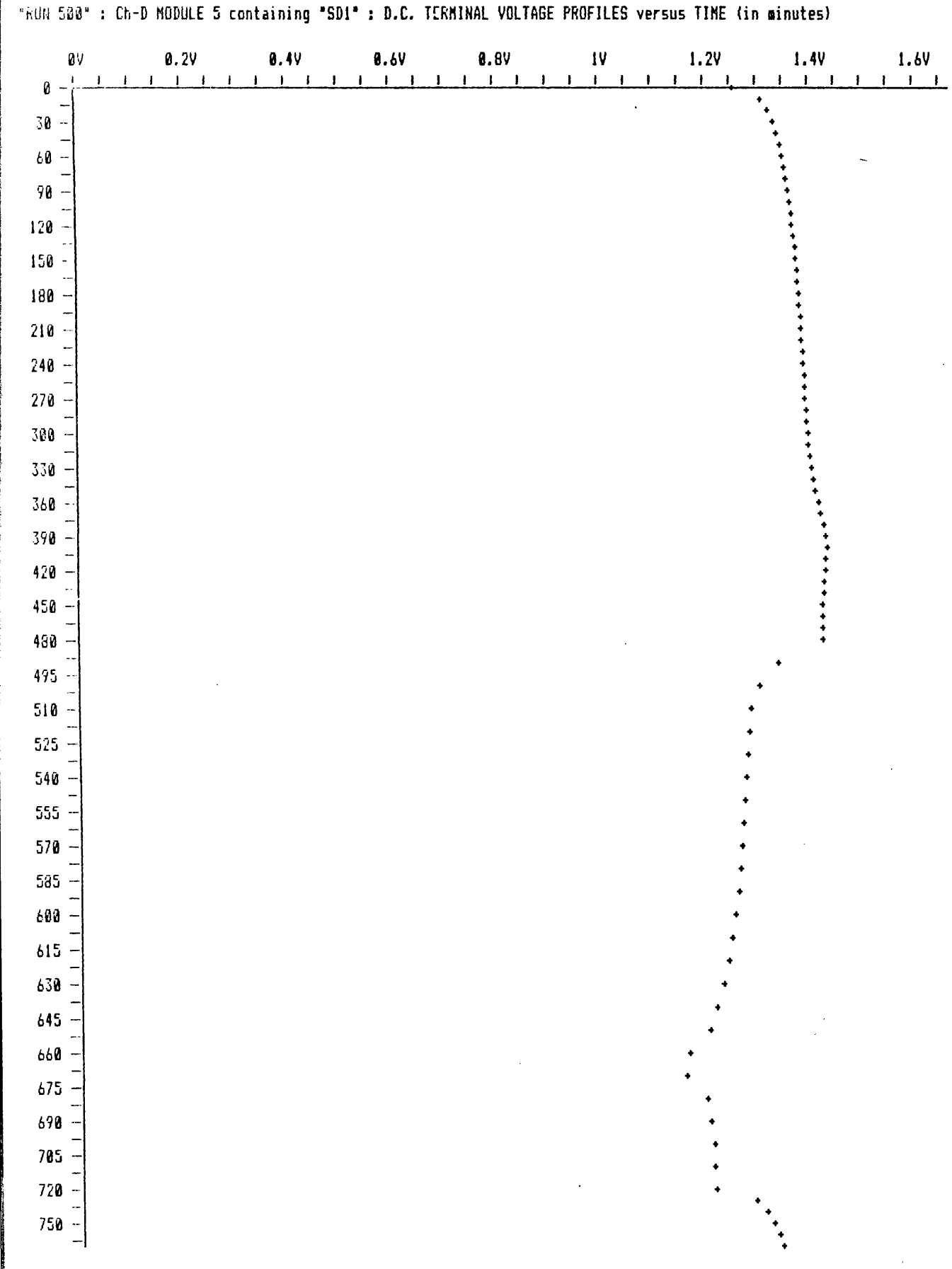
Graph 8(99)

Note: Curve order is 2Hz pair >>> 32Hz

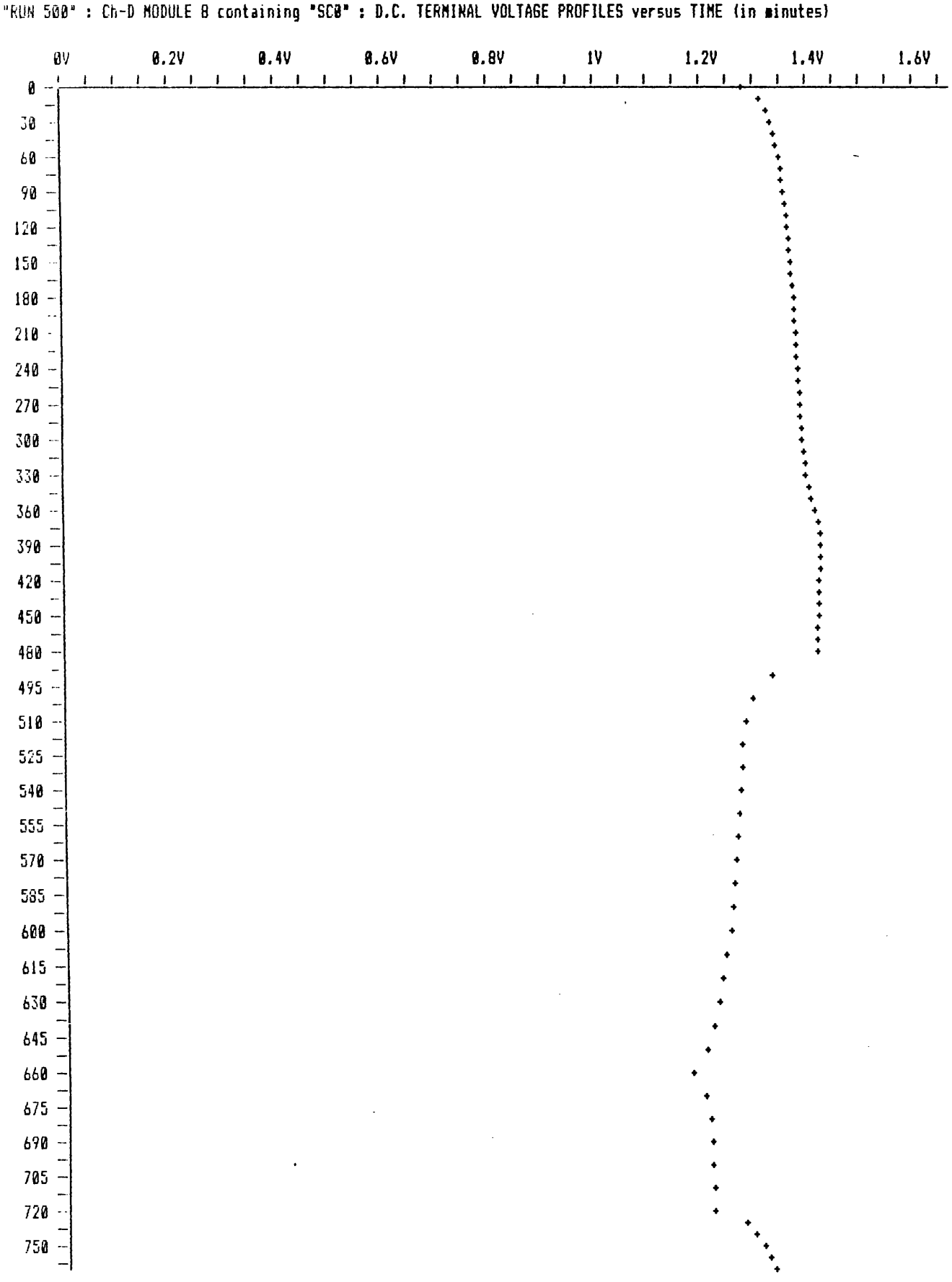
"RUN 400" : Ch-D MODULE 44 containing "PP7" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 3(a)

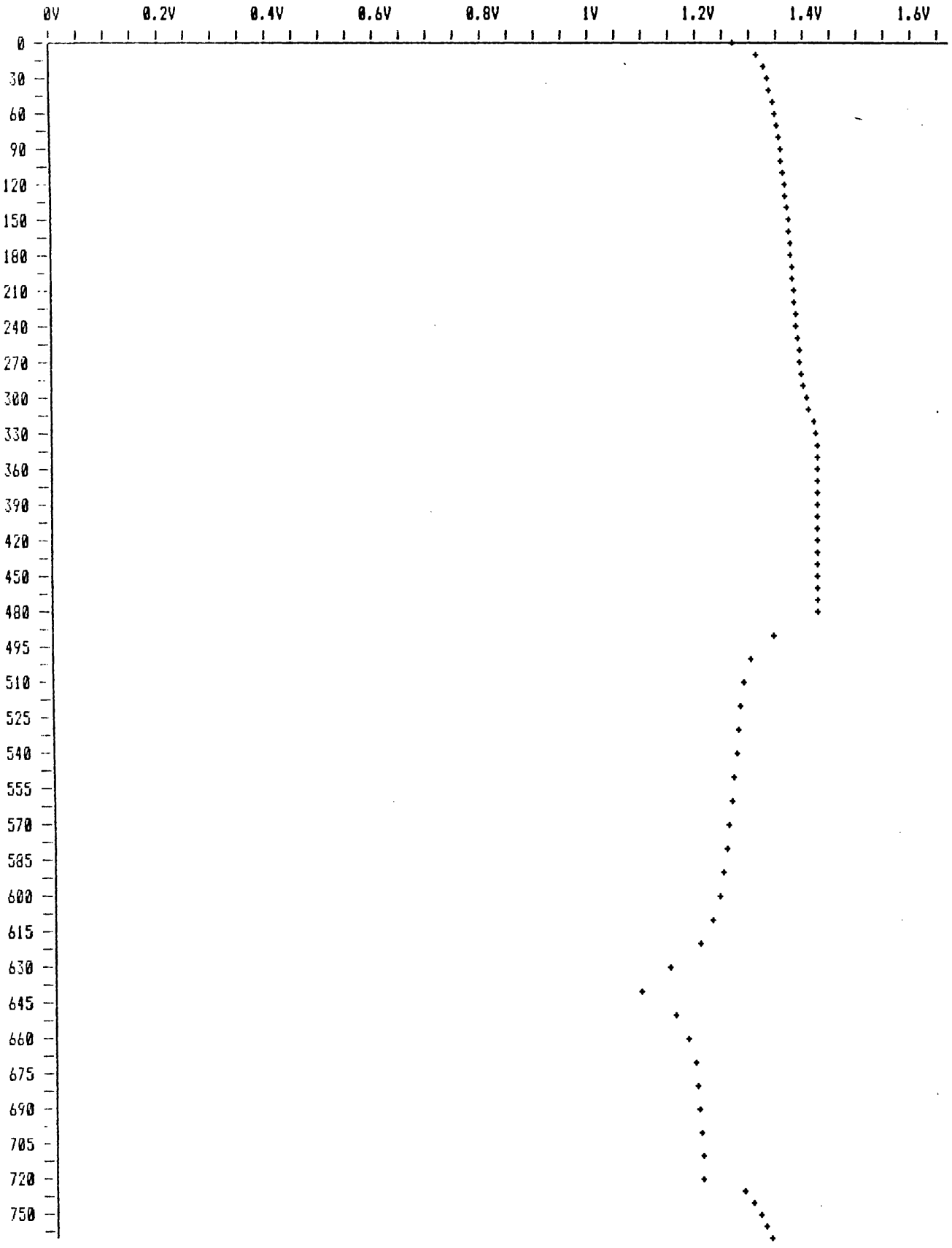

"RUN 580" : Ch-D MODULE 5 containing "SD1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 9(B)

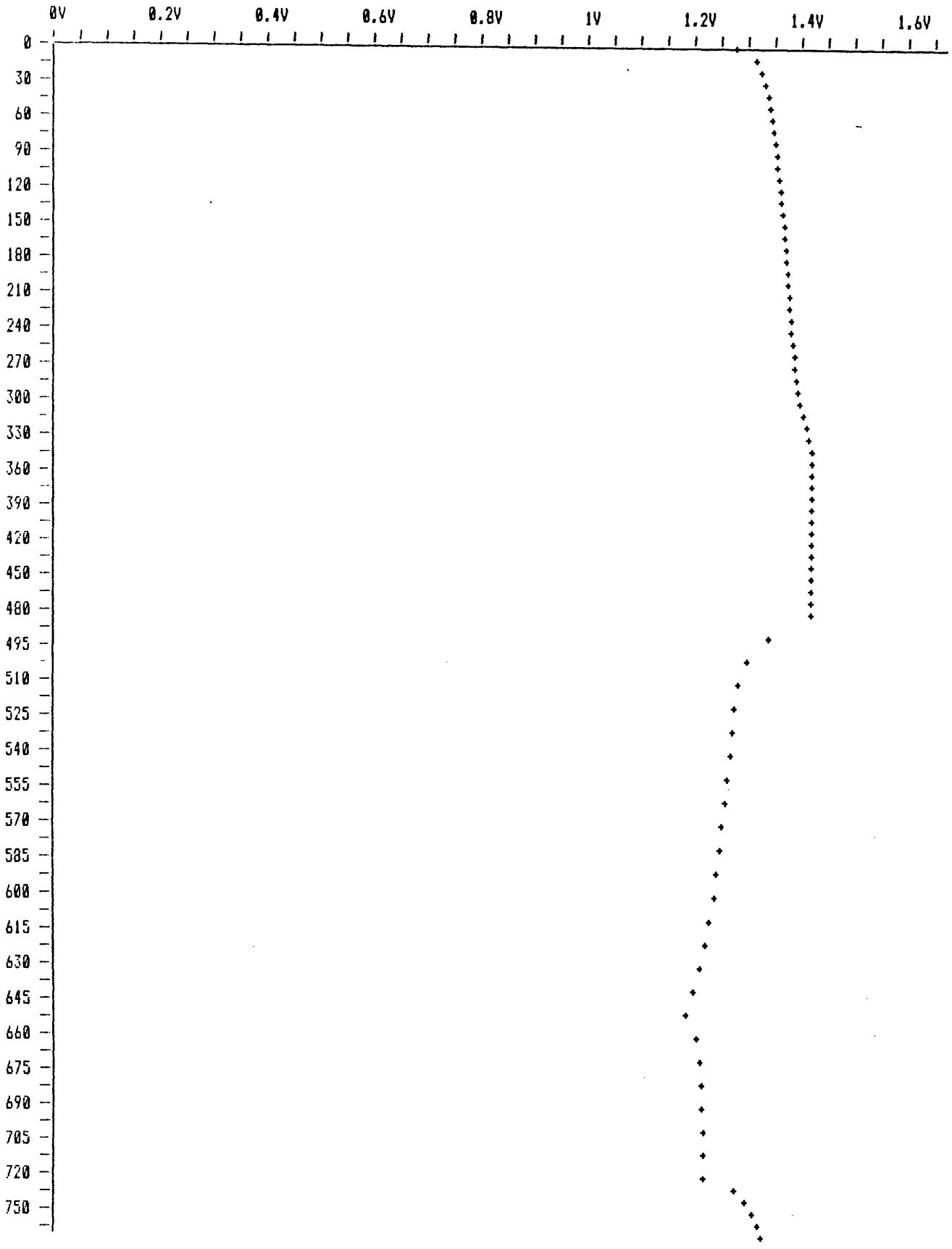

"RUN 500" : Ch-D MODULE B containing "SC8" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
0.2V
0.4V
0.6V
0.8V
1V
1.2V
1.4V
1.6V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 9(c)

"RUN 500" : Ch-D MODULE 16 containing "P8/5P0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

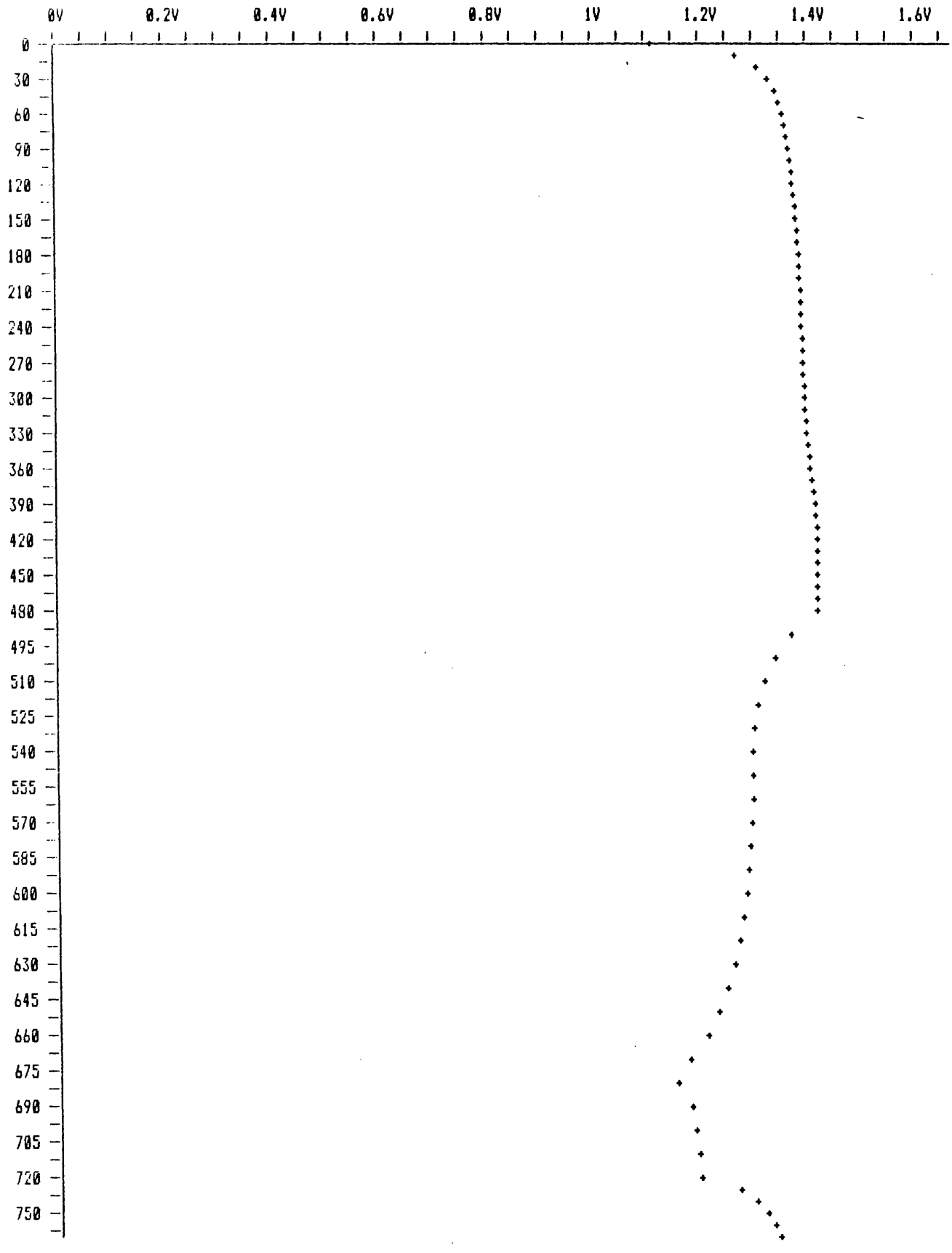


"RUN 503" : Ch-D MODULE 17 containing "P8/5P1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

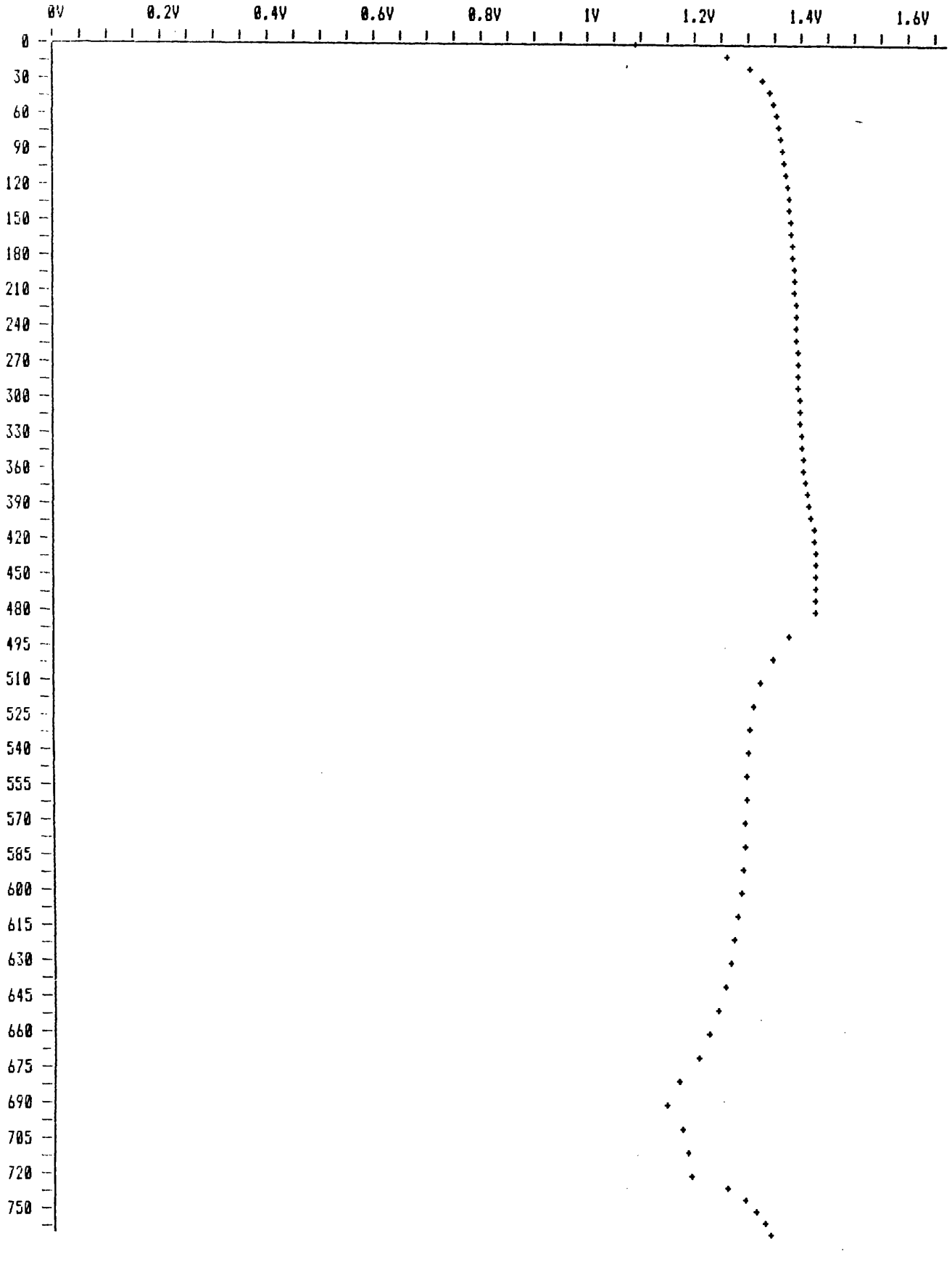


Graph 9(a)

"RUN 500" : Ch-D MODULE 24 containing "MR0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



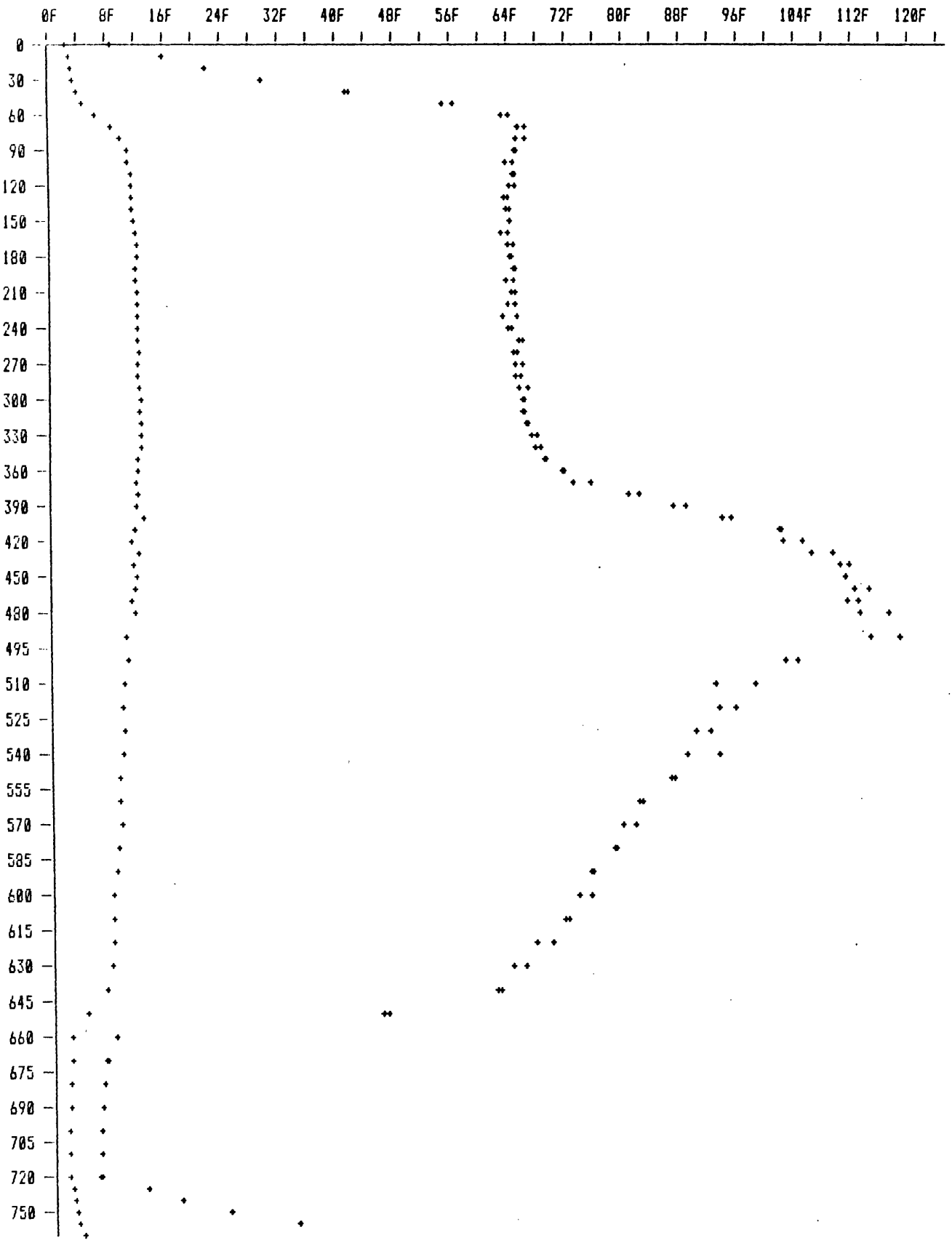
"RUN 500" : Ch-D MODULE 25 containing "MR1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 9(g)

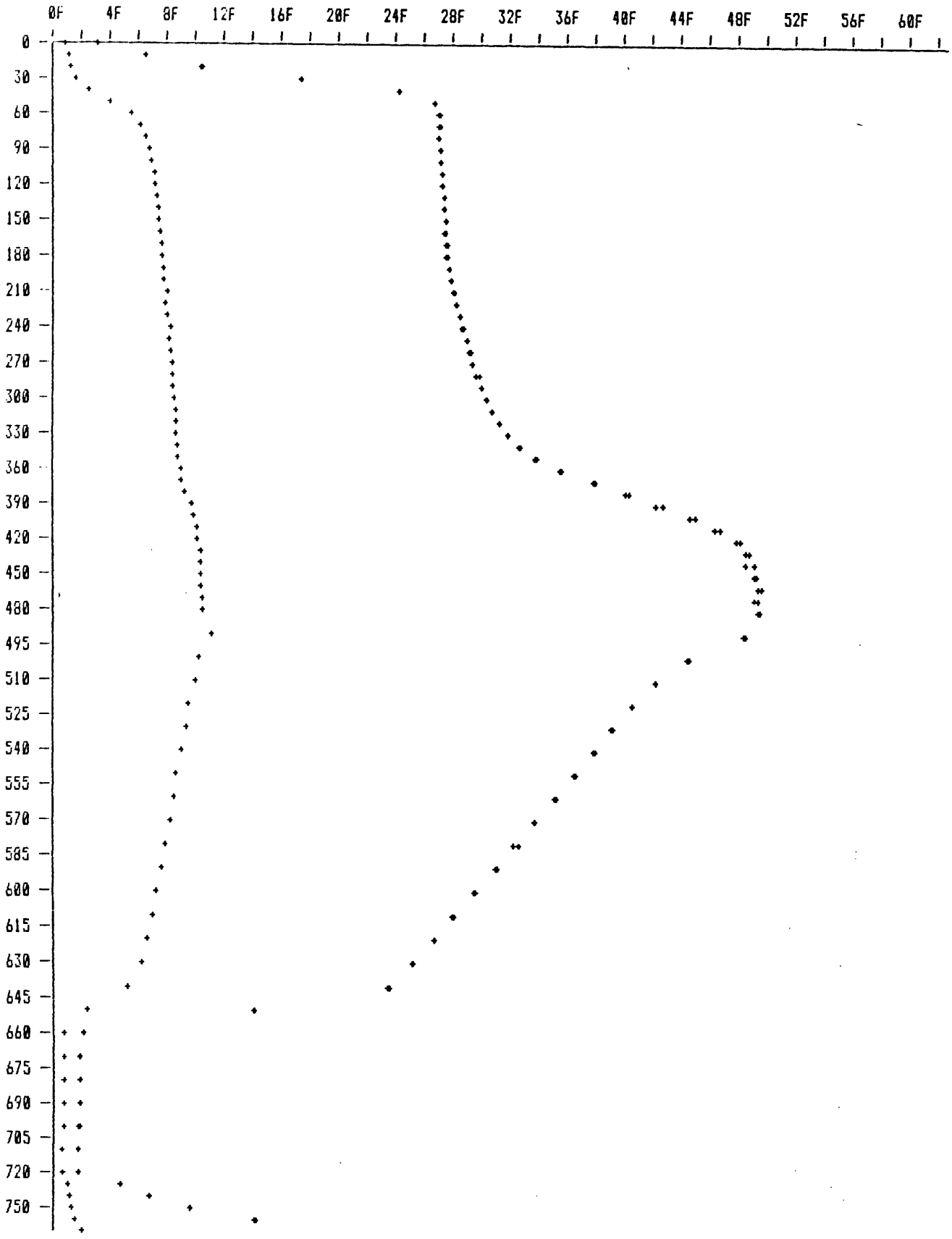
Note: Curve order is 32Hz >>> 2Hz pair

"RUN 500" : Ch-D MODULE 5 containing "SDI" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Note: Curve order is 32Hz >>> 2Hz pair

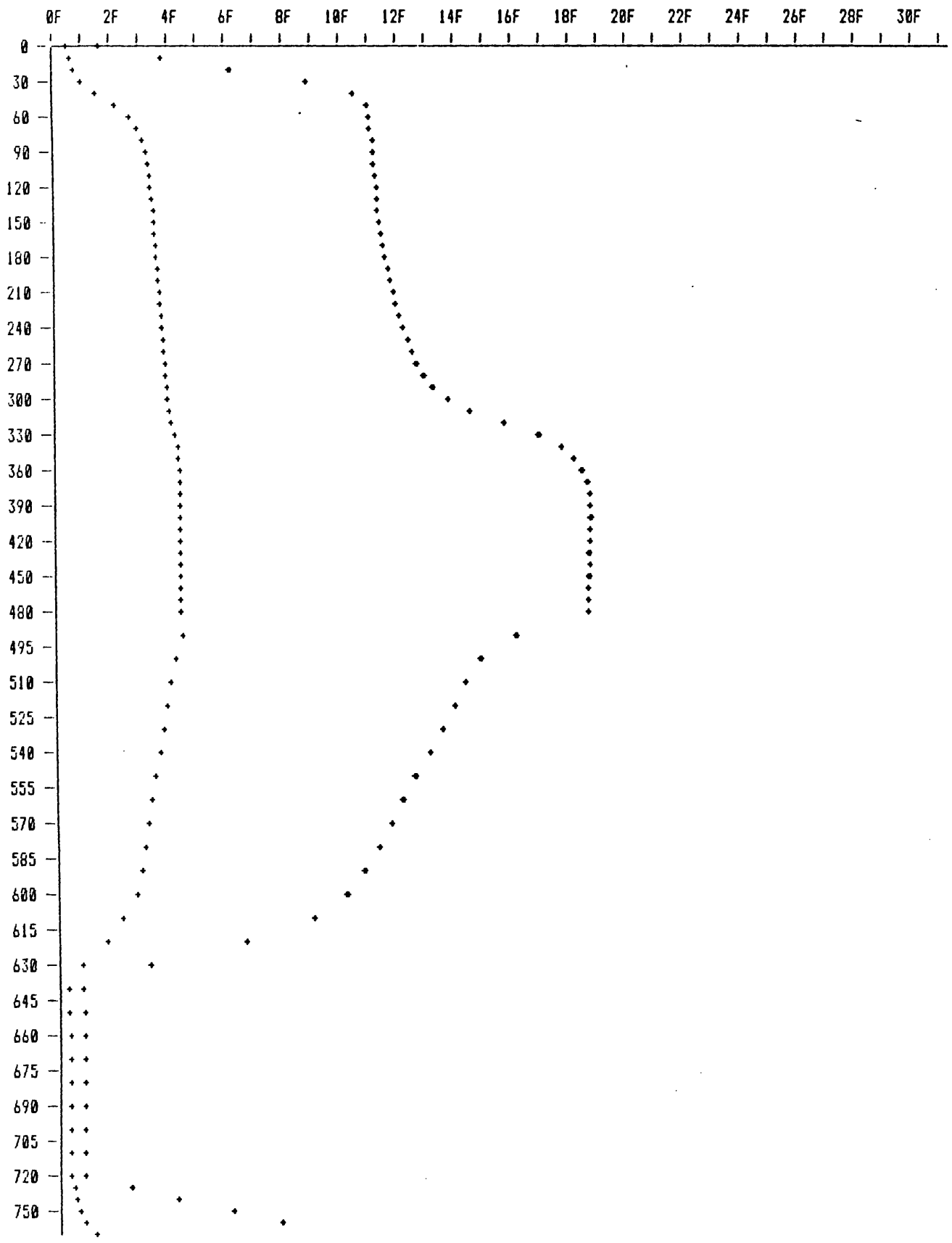
"RUN 500" : Ch-D MODULE 8 containing "SC0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 3(1)

Note: Curve order is 32Hz >>> 2Hz pair

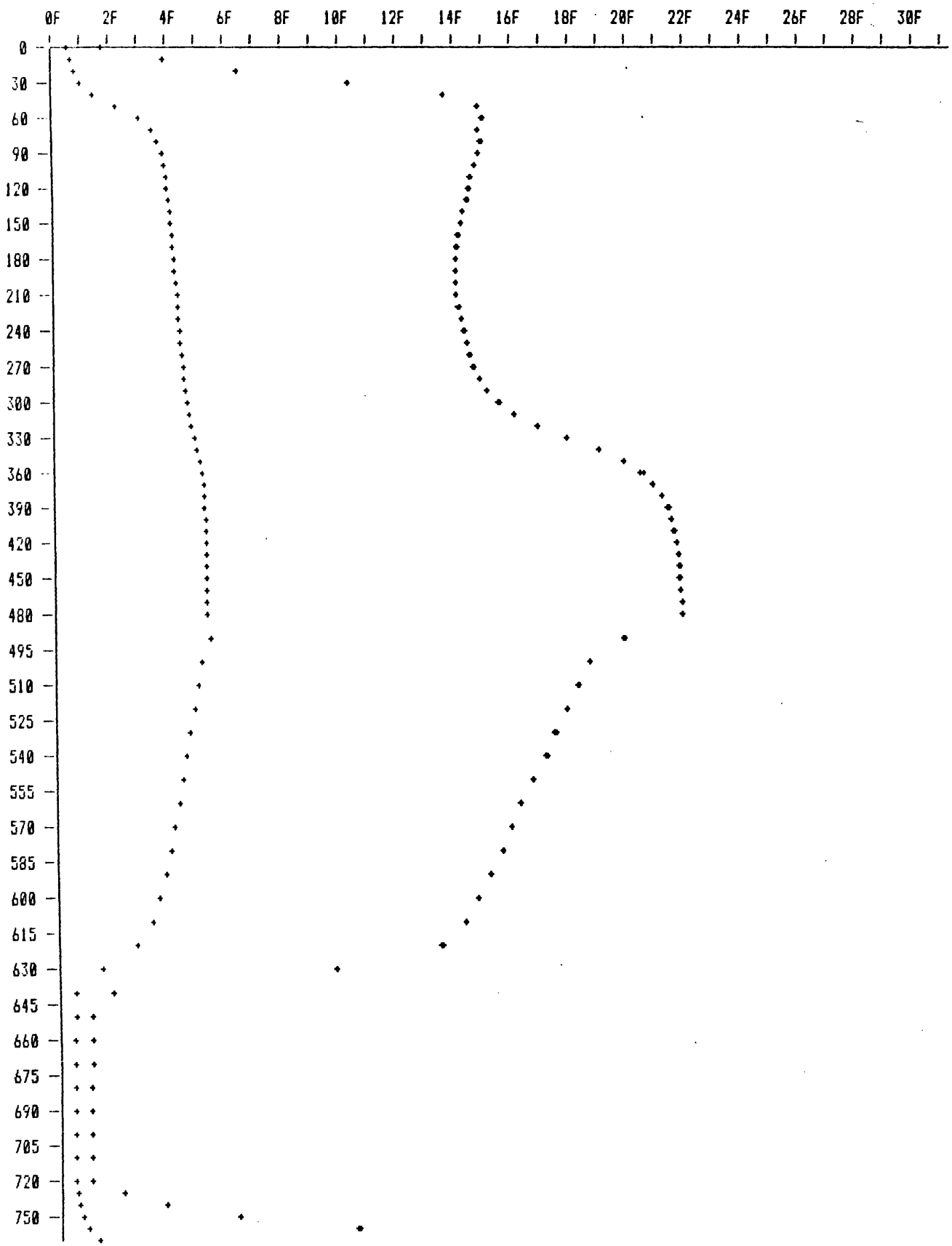
"RUN 500" : Ch-D MODULE 16 containing "P0/5P0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 9(i)

Note: Curve order is 32Hz >>> 2Hz pair

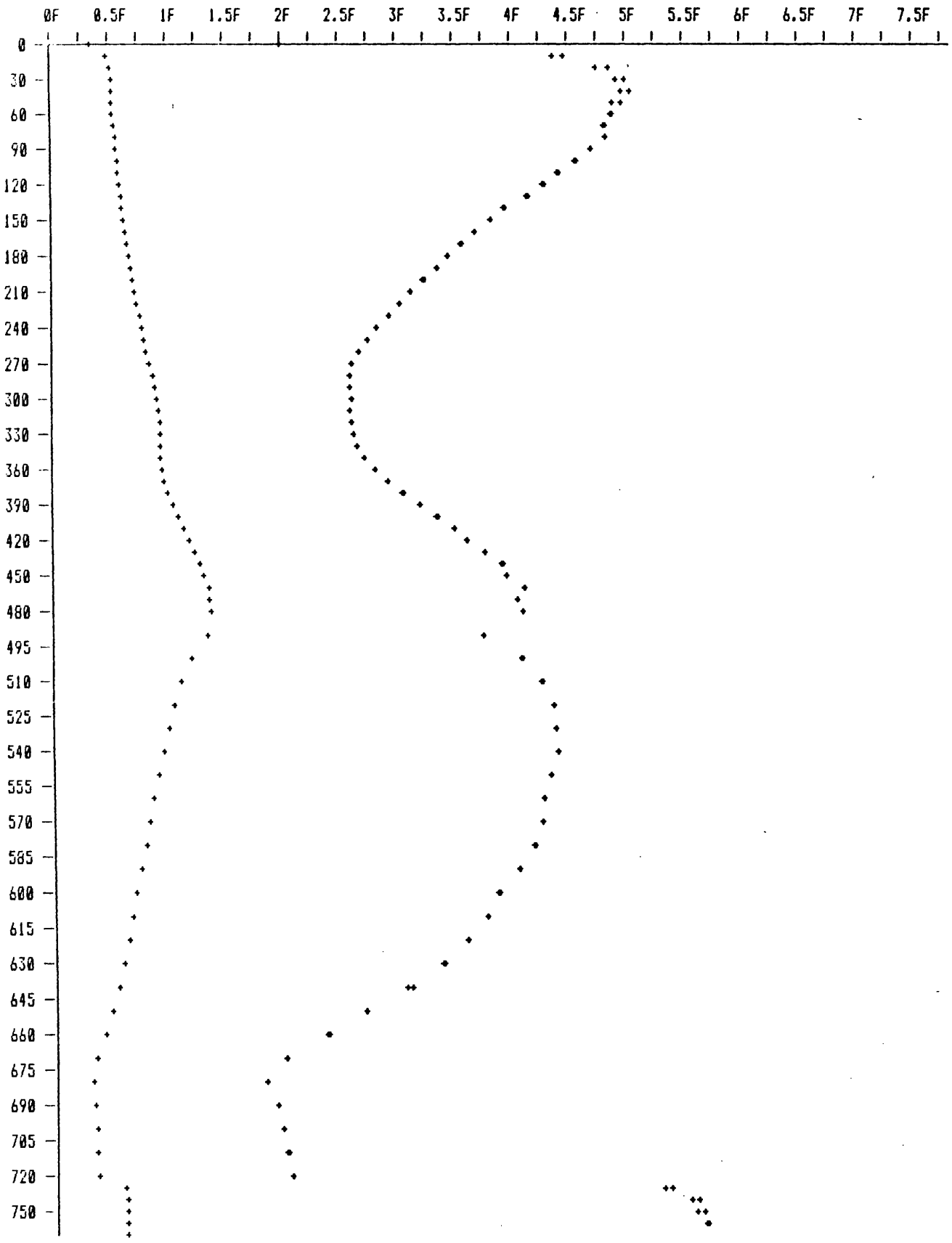
"RUN 500" : Ch-D MODULE 17 containing "P8/5P1" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 5(A)

Note: Curve order is 32Hz >>> 2Hz pair

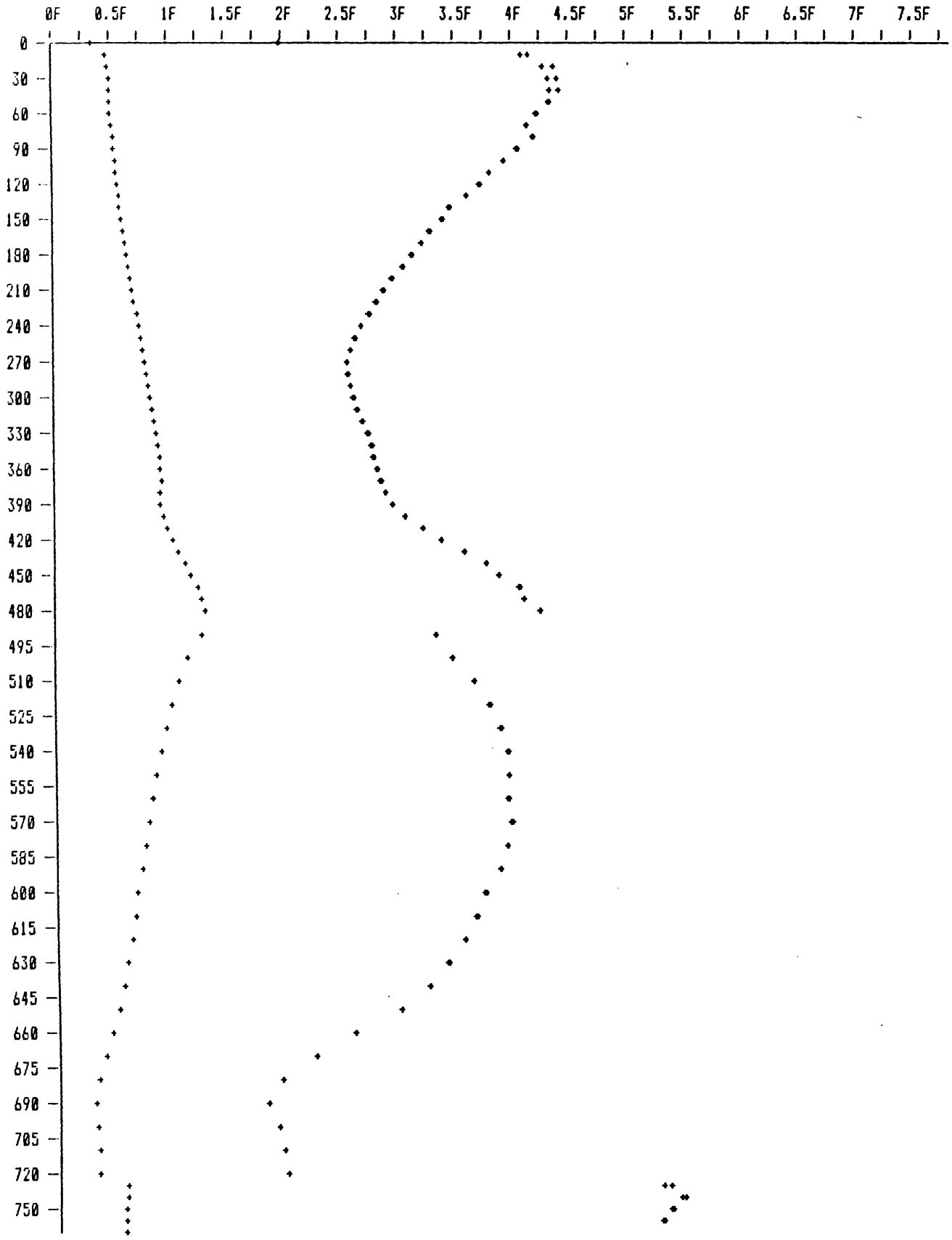
"RUN 500" : Ch-D MODULE 24 containing "MR0" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 9(1)

Note: Curve order is 32Hz >>> 2Hz pair

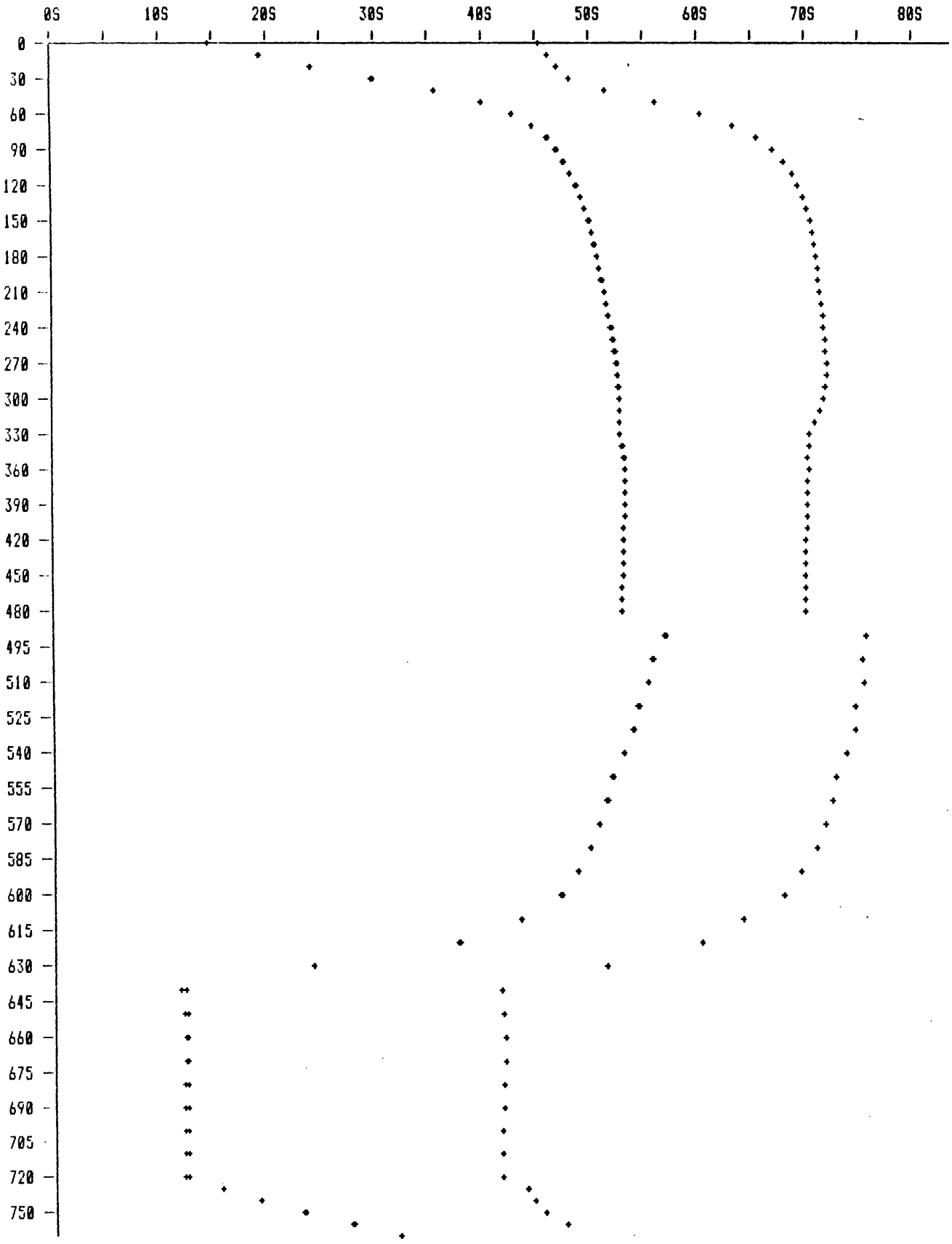
"RUN 500" : Ch-D MODULE 25 containing "MR1" : E.S.CAPACITANCE PROFILES at frequencies 32,2,2Hz



Graph 9(m)

Note: Curve order is 2Hz pair >>> 32Hz

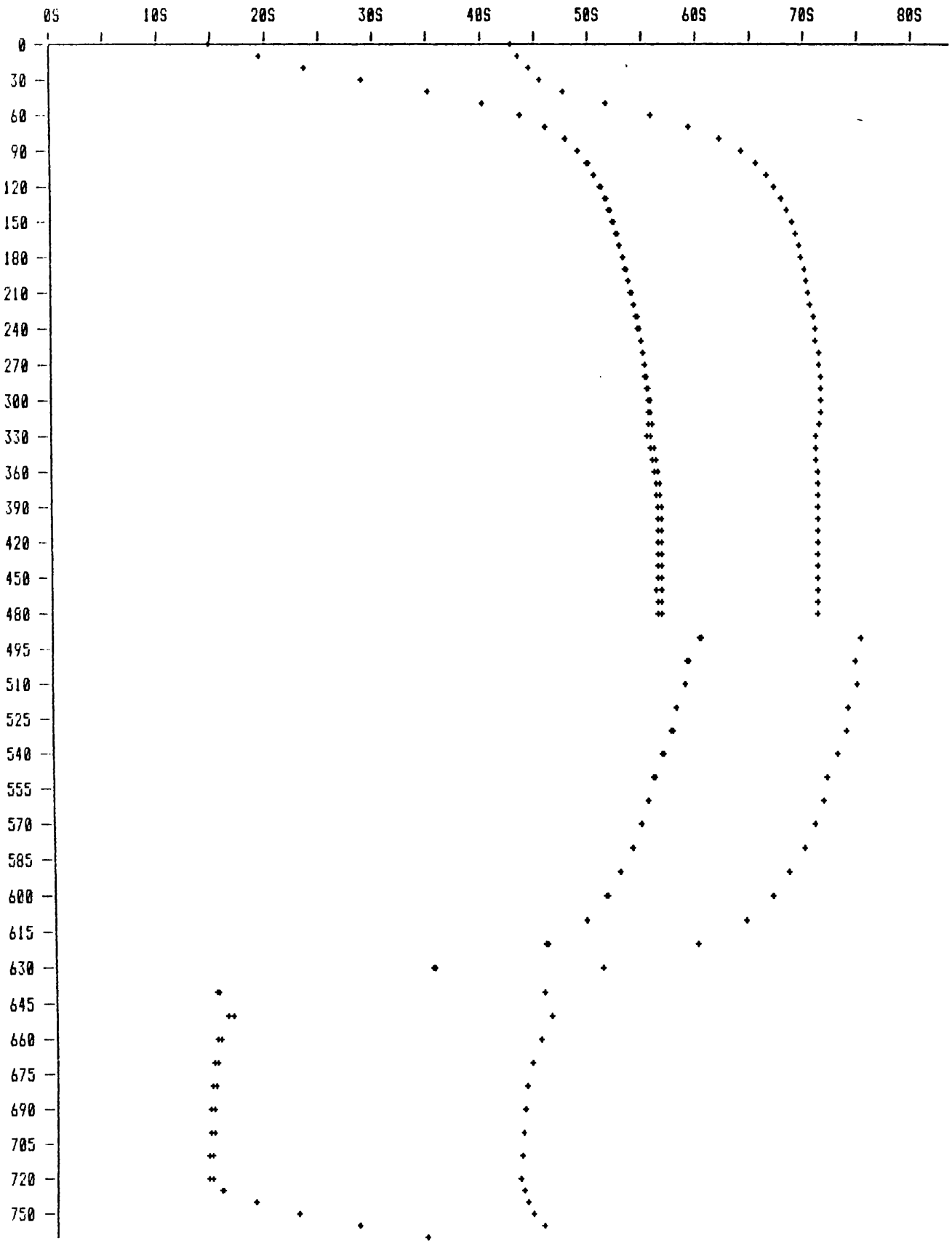
"RUN 500" : Ch-D MODULE 16 containing "P8/5P8" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 9(ii)

Note: Curve order is 2Hz pair >>> 32Hz

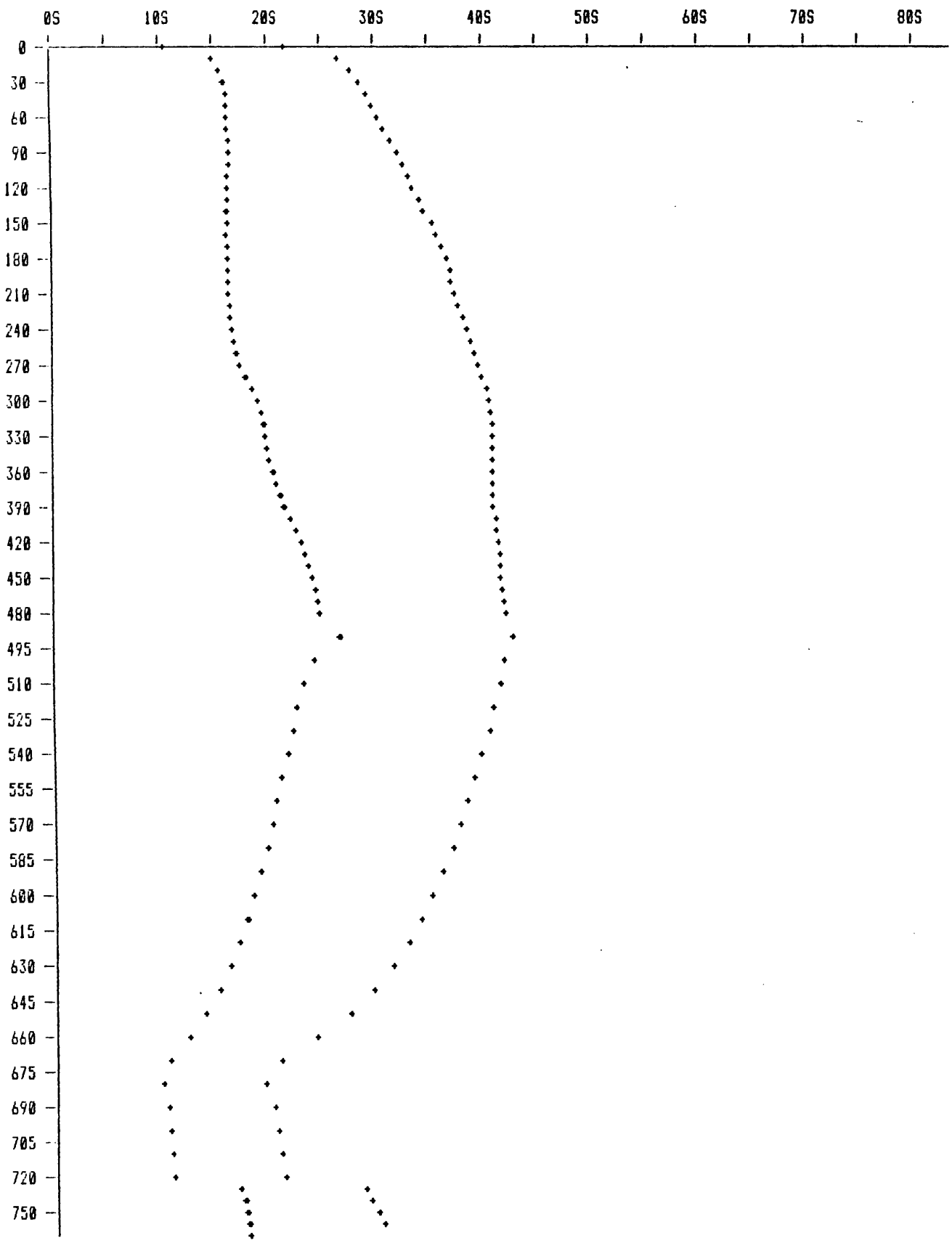
"RUN 500" : Ch-D MODULE 17 containing "P8/5P1" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz



Graph 9(8)

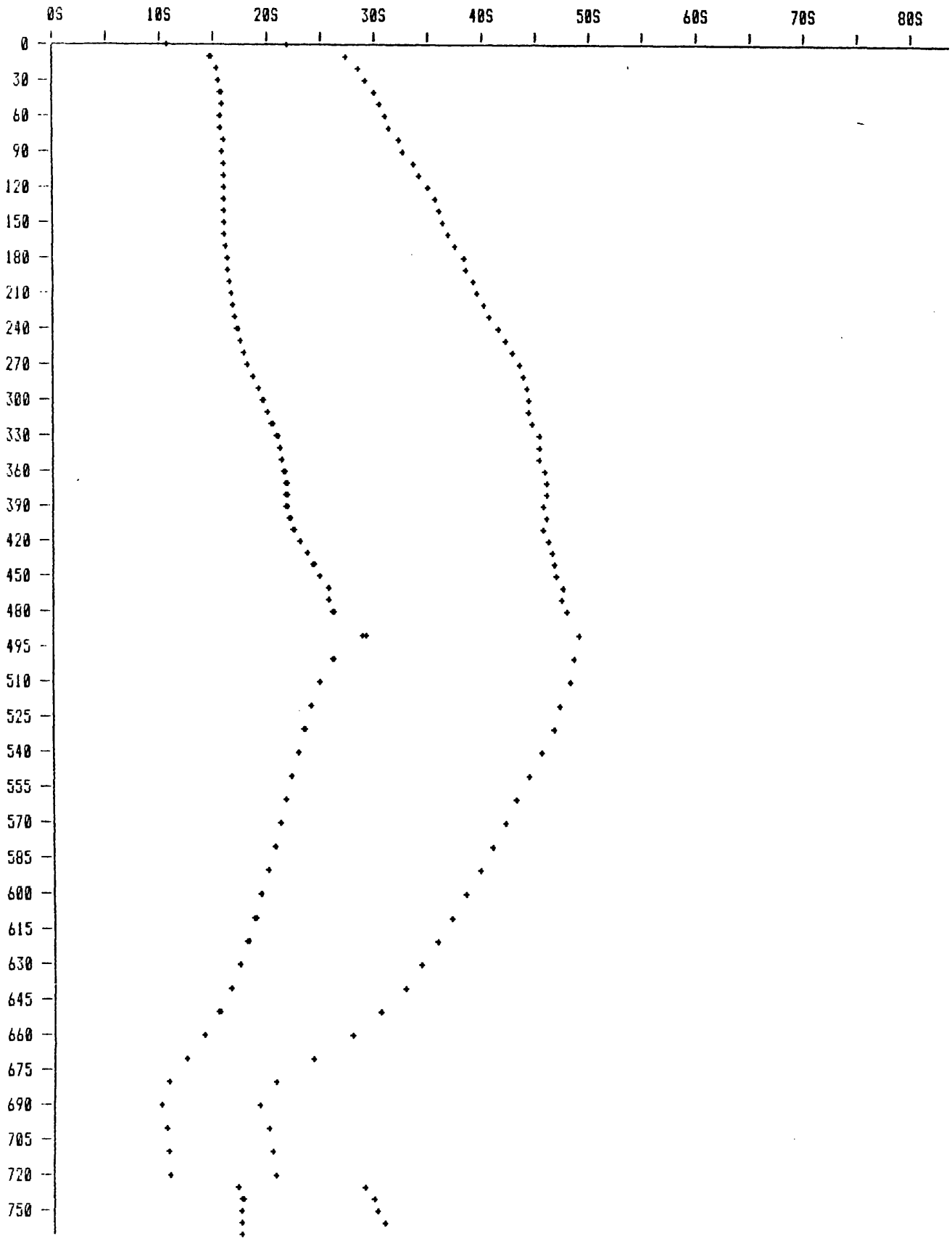
Note: Curve order is 2Hz pair >>> 32Hz

"RUN 500" : Ch-D MODULE 24 containing "MR0" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz

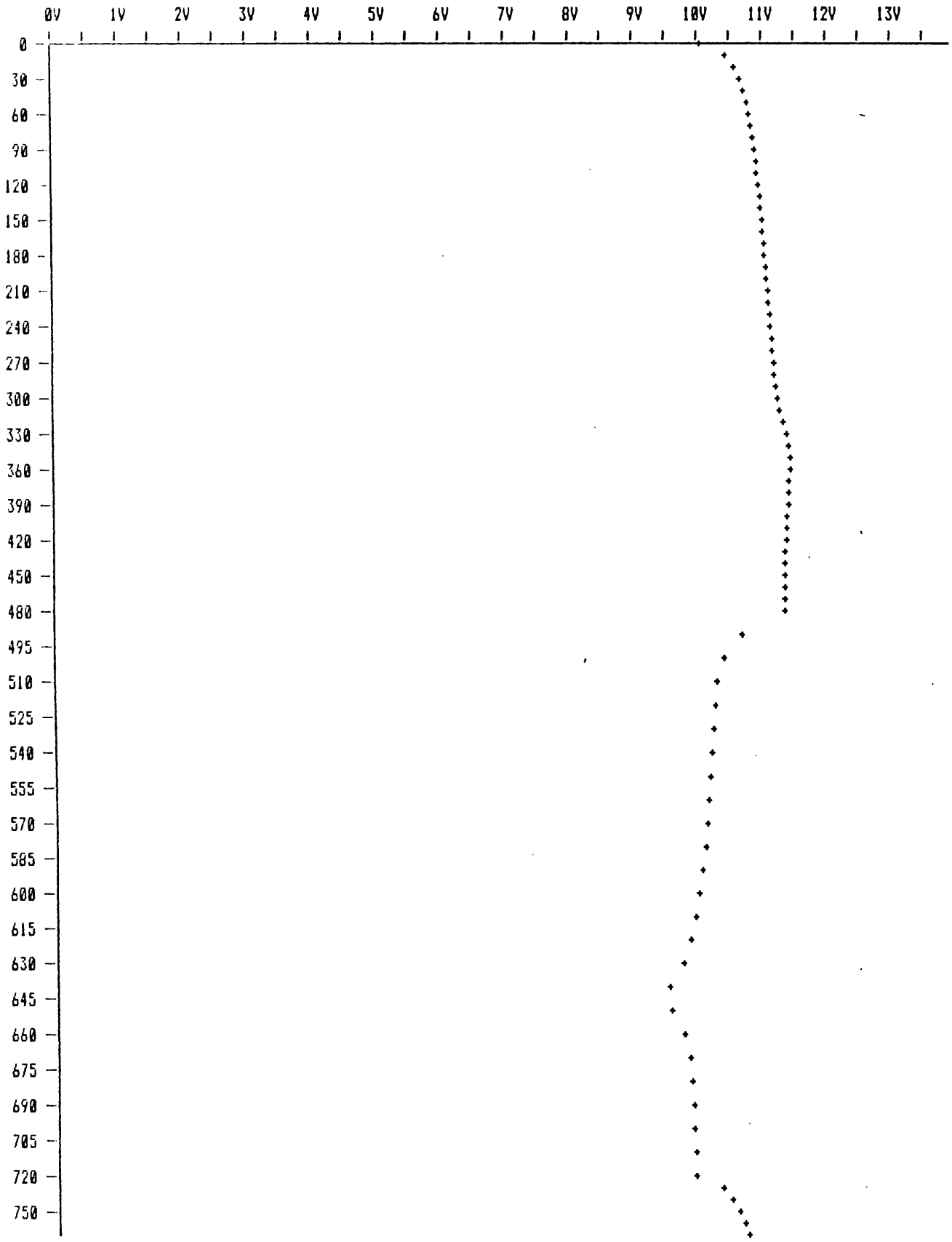


Note: Curve order is 2Hz pair >>> 32Hz

"RUN 500" : Ch-D MODULE 25 containing "MR1" : E.S.CONDUCTANCE PROFILES at frequencies 32,2,2Hz

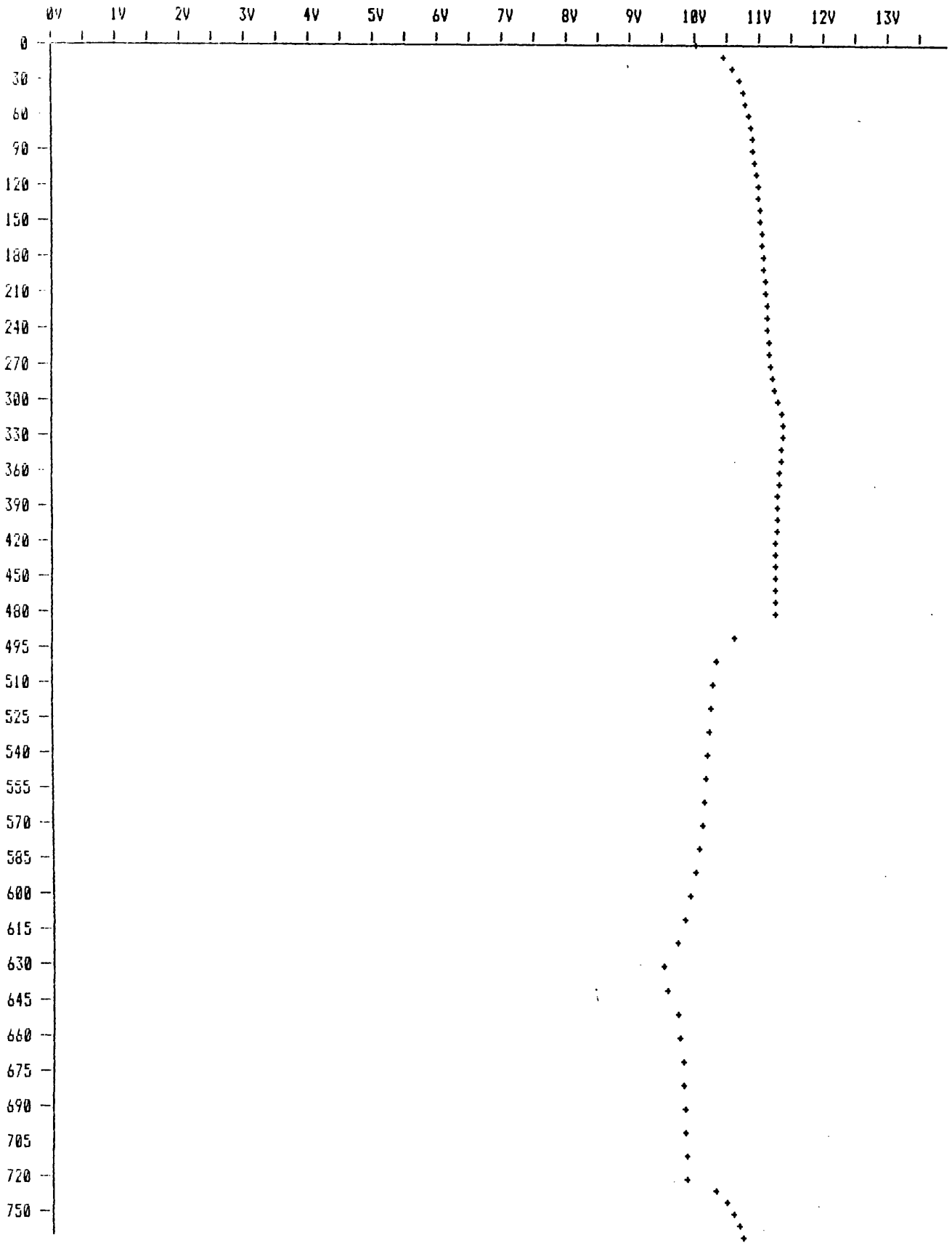


"RUN 601" : Ch-D MODULE 5 containing "P6PB5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 10(D)

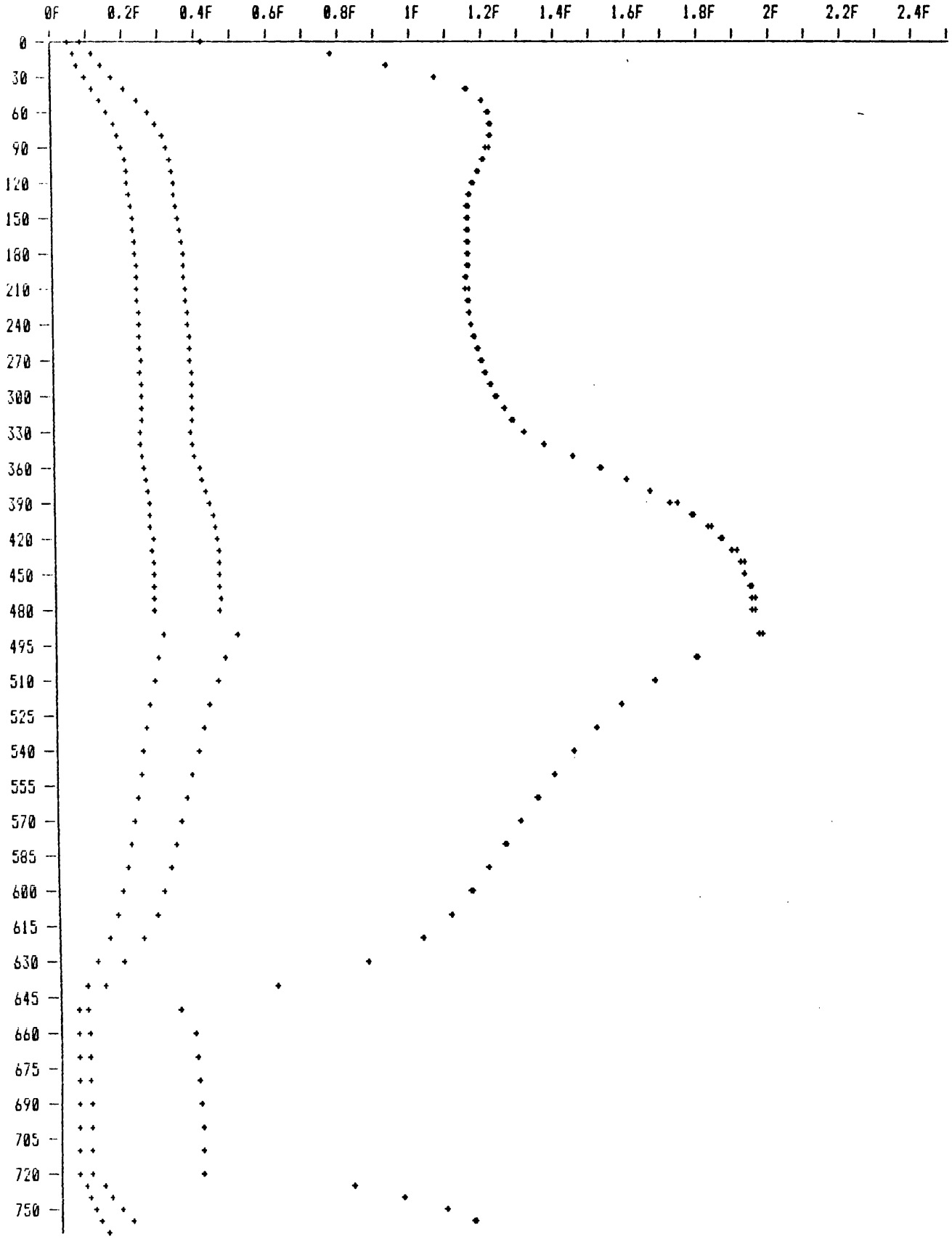
"RUN 601" : Ch-D MODULE 6 containing "P6PB6" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 10(c)

Note: Curve order is 64Hz >>> 32Hz >>> 2Hz pair

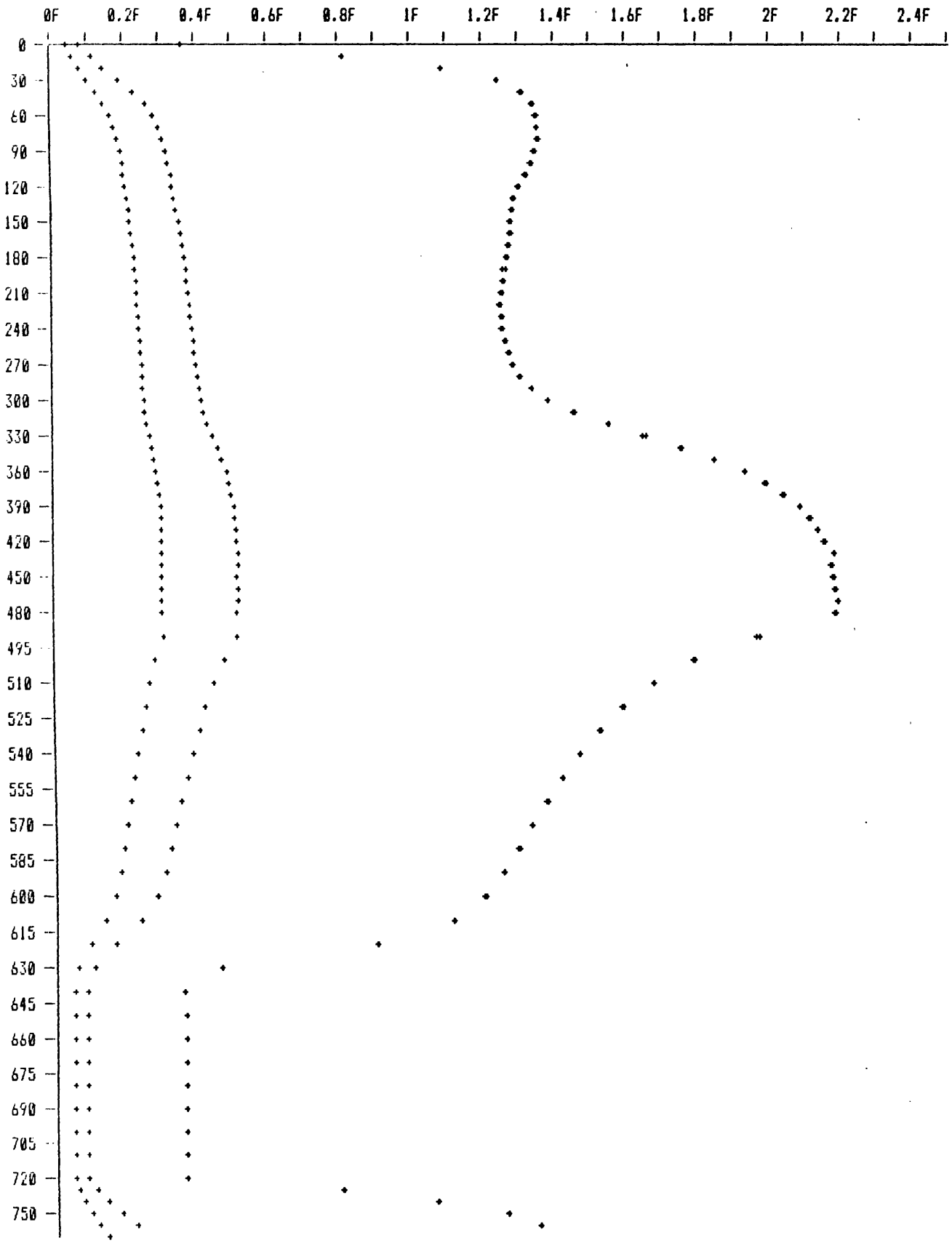
"RUN 601" : Ch-D MODULE 5 containing "P6PB5" : E.S.CAPACITANCE PROFILES at frequencies 64,32,2,2Hz



Graph 10(d)

Note: Curve order is 64Hz >>> 32Hz >>> 2Hz pair

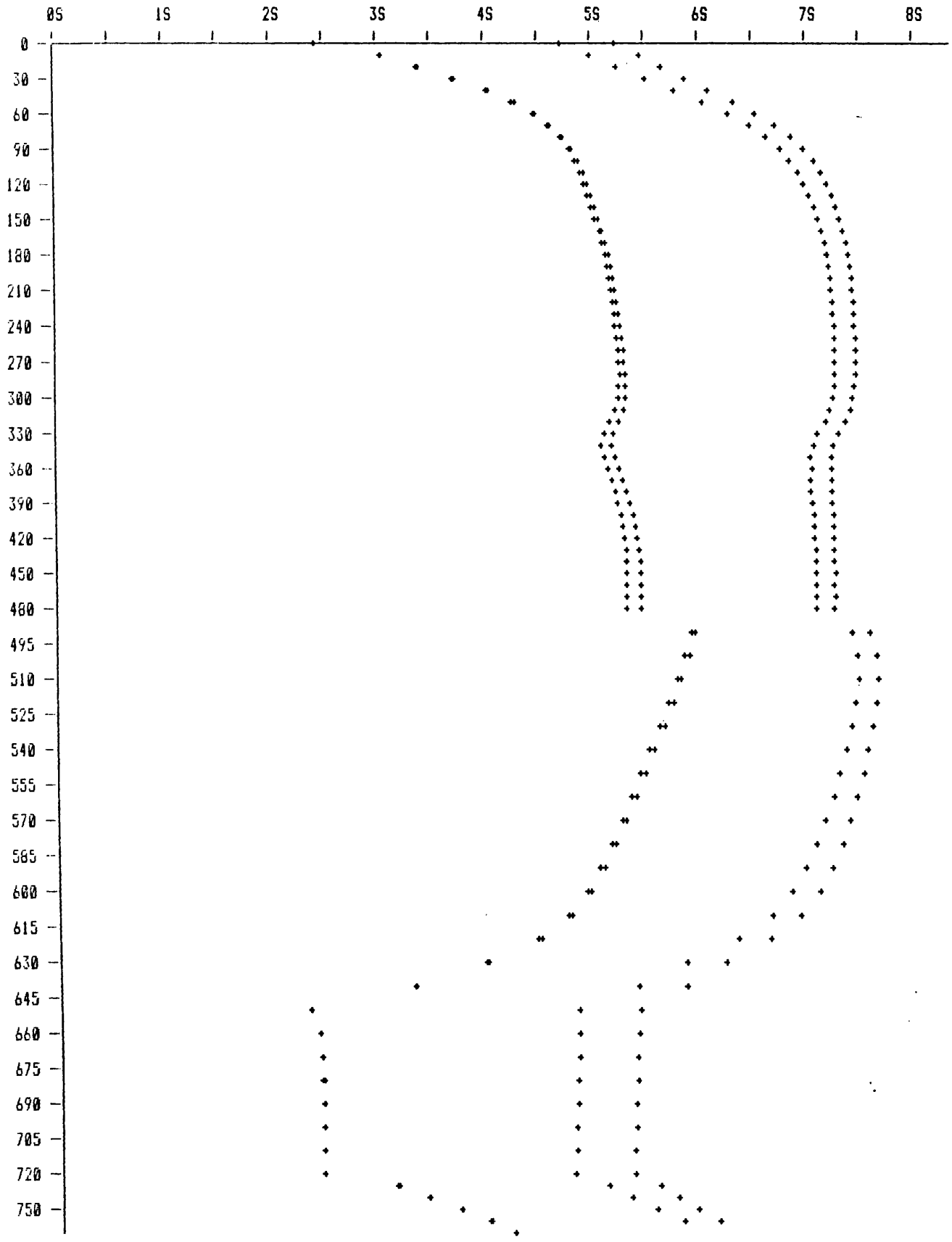
"RUN 601" : Ch-D MODULE 6 containing "P6PB6" : E.S.CAPACITANCE PROFILES at frequencies 64,32,2,2Hz



Graph 10(3)

Note: Curve order is 2Hz pair >>> 32Hz >>> 64Hz

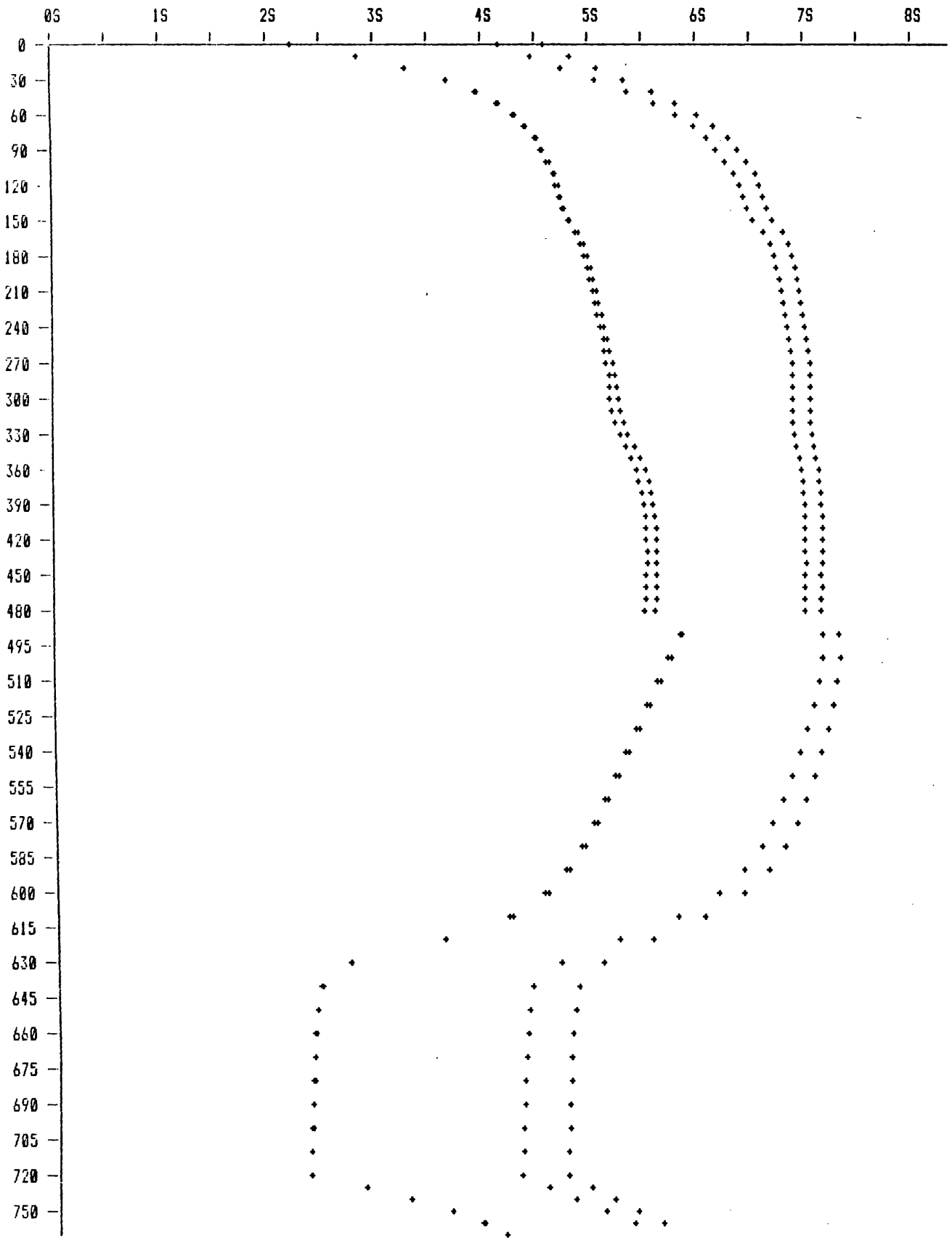
"RUN 601" : Ch-D MODULE 5 containing "P6PB5" : E.S.CONDUCTANCE PROFILES at frequencies 64,32,2,2Hz



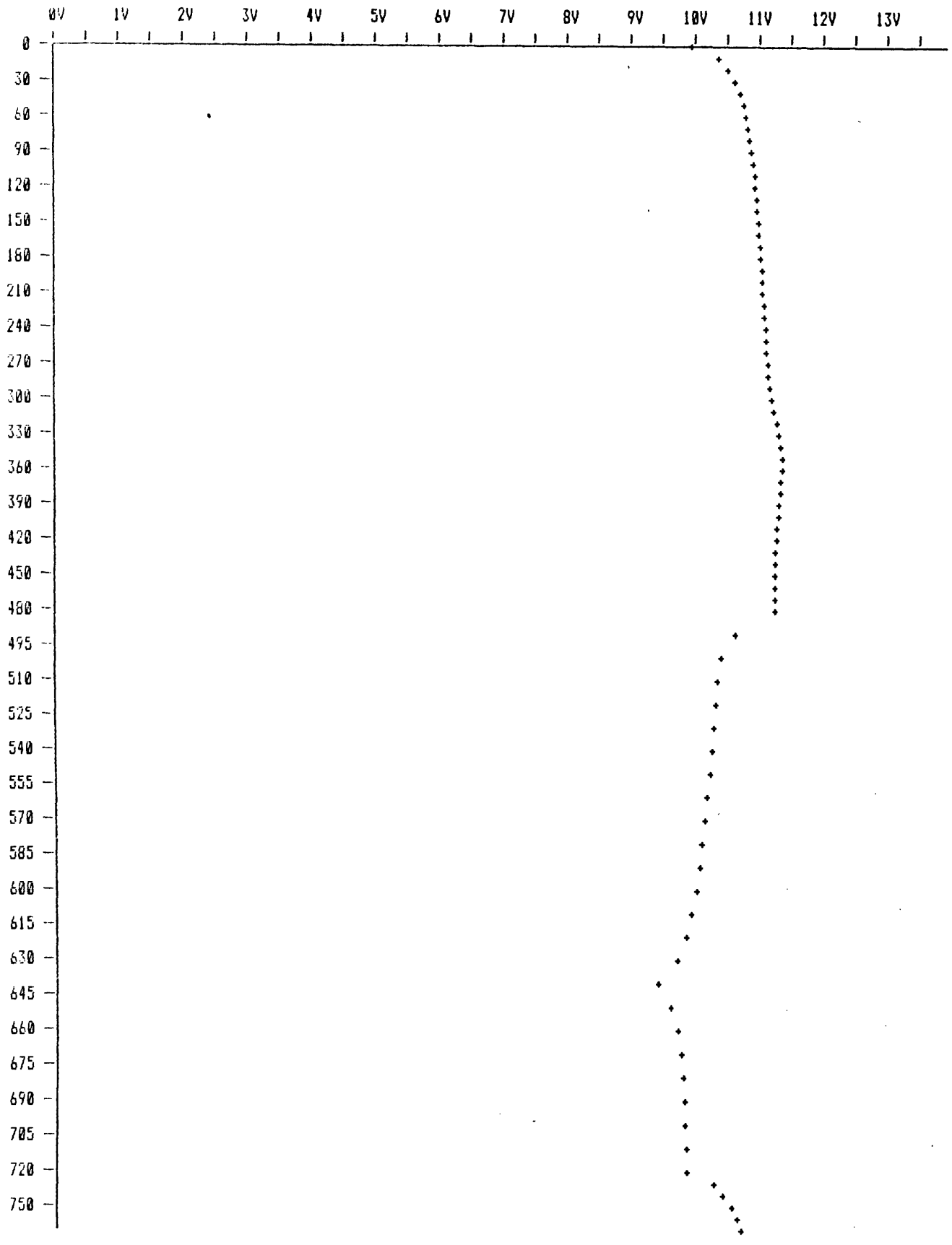
Graph 10(1)

Note: Curve order is 2Hz pair >>> 32Hz >>> 64Hz

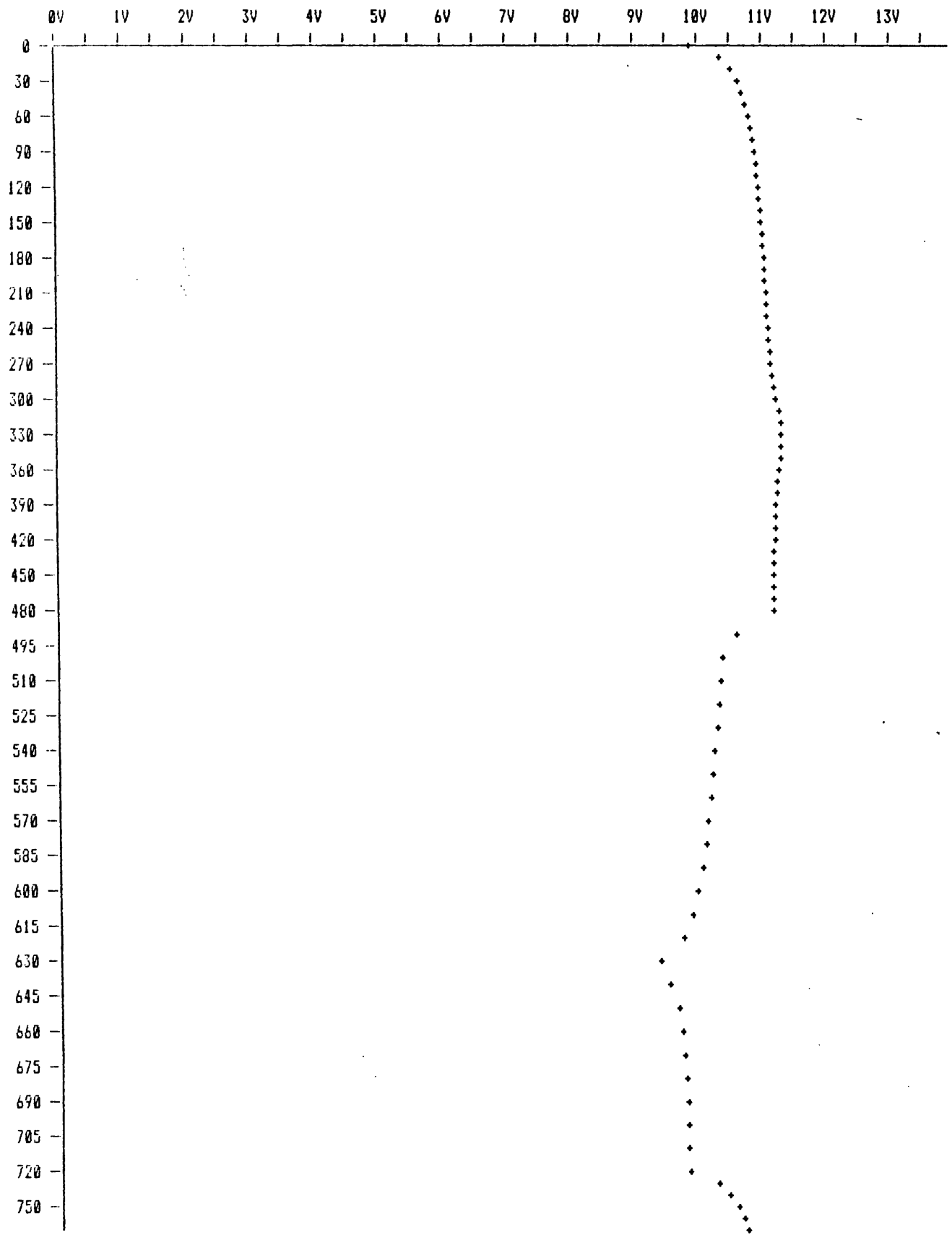
"RUN 601" : Ch-D MODULE 6 containing "P6PB6" : E.S.CONDUCTANCE PROFILES at frequencies 64,32,2,2Hz



"RUN 685" : Ch-D MODULE 5 containing "P6PB5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

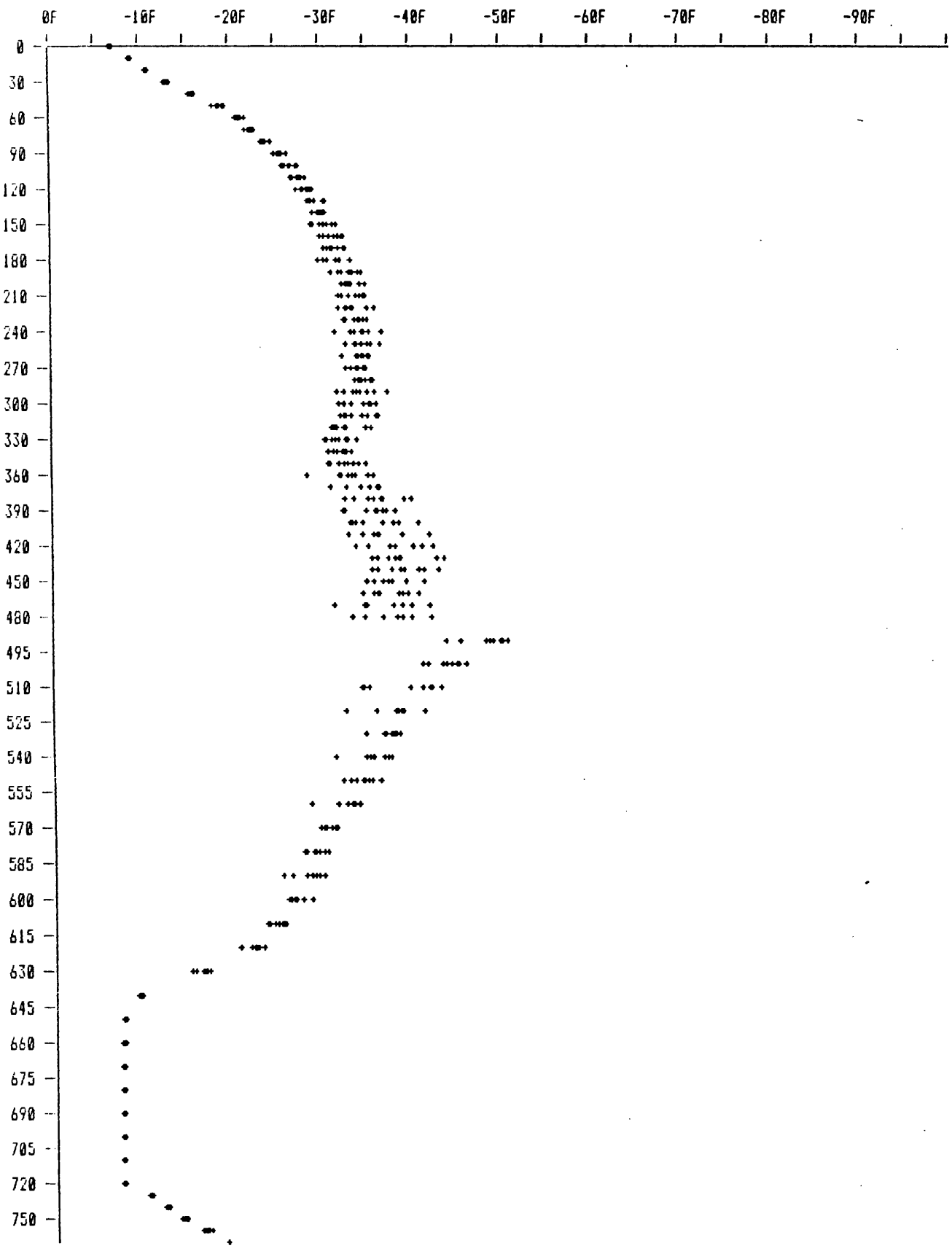


"RUN 605" : Ch-D MODULE 6 containing "P6PB6" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)

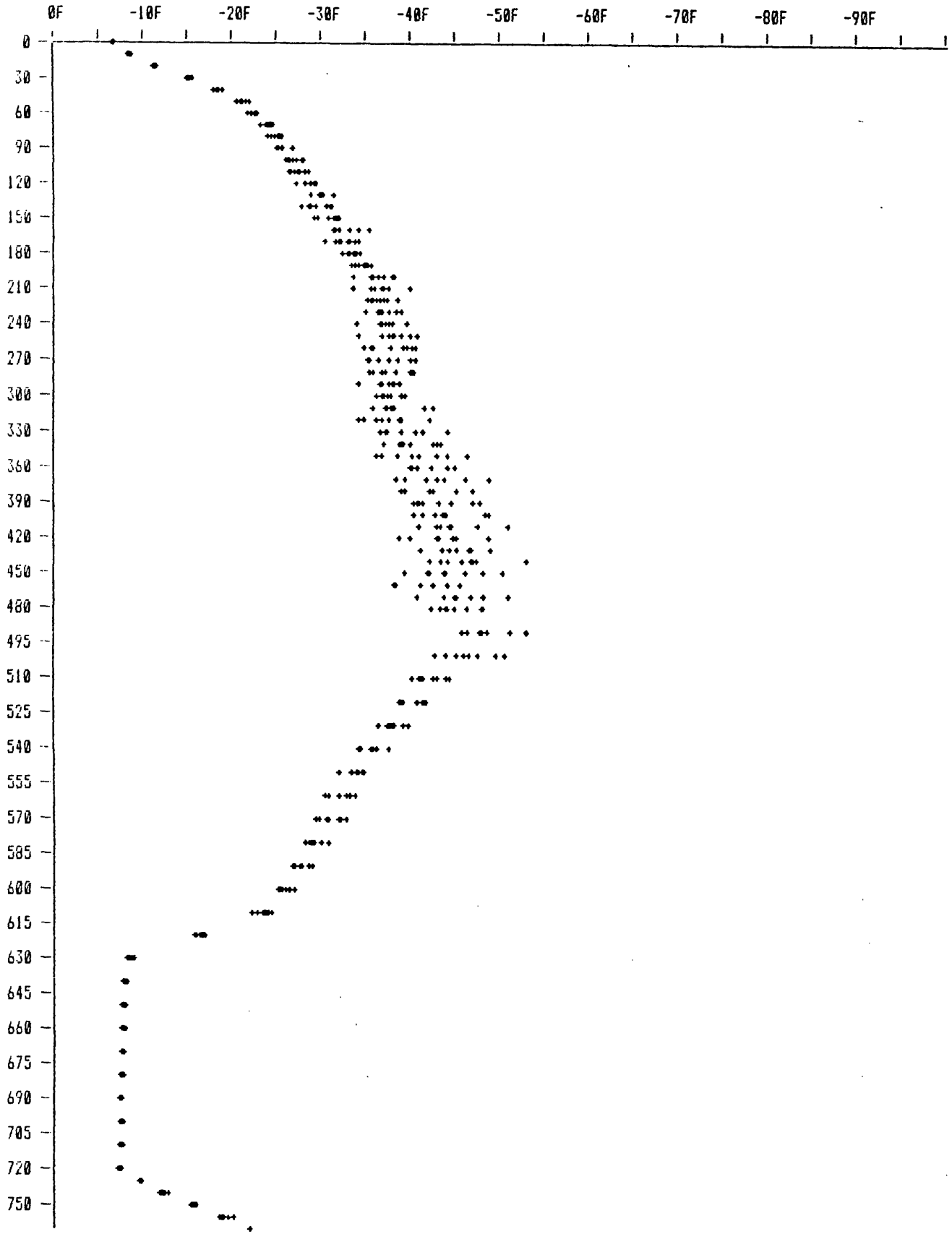


Graph 11(c)

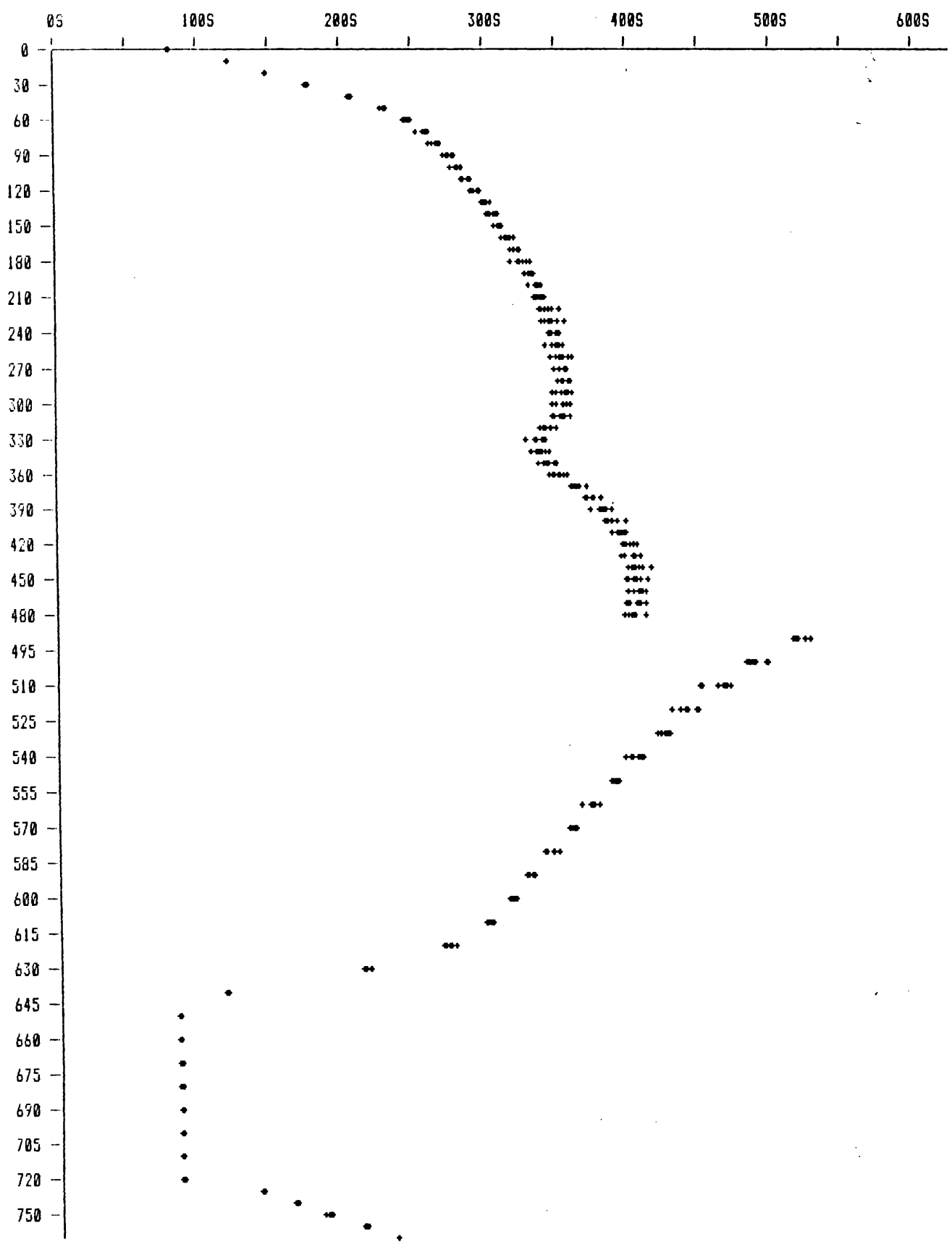
"RUN 605" : Ch-D MODULE 5 containing "P6PB5" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 8,8,8,8,8,8,8,8Hz



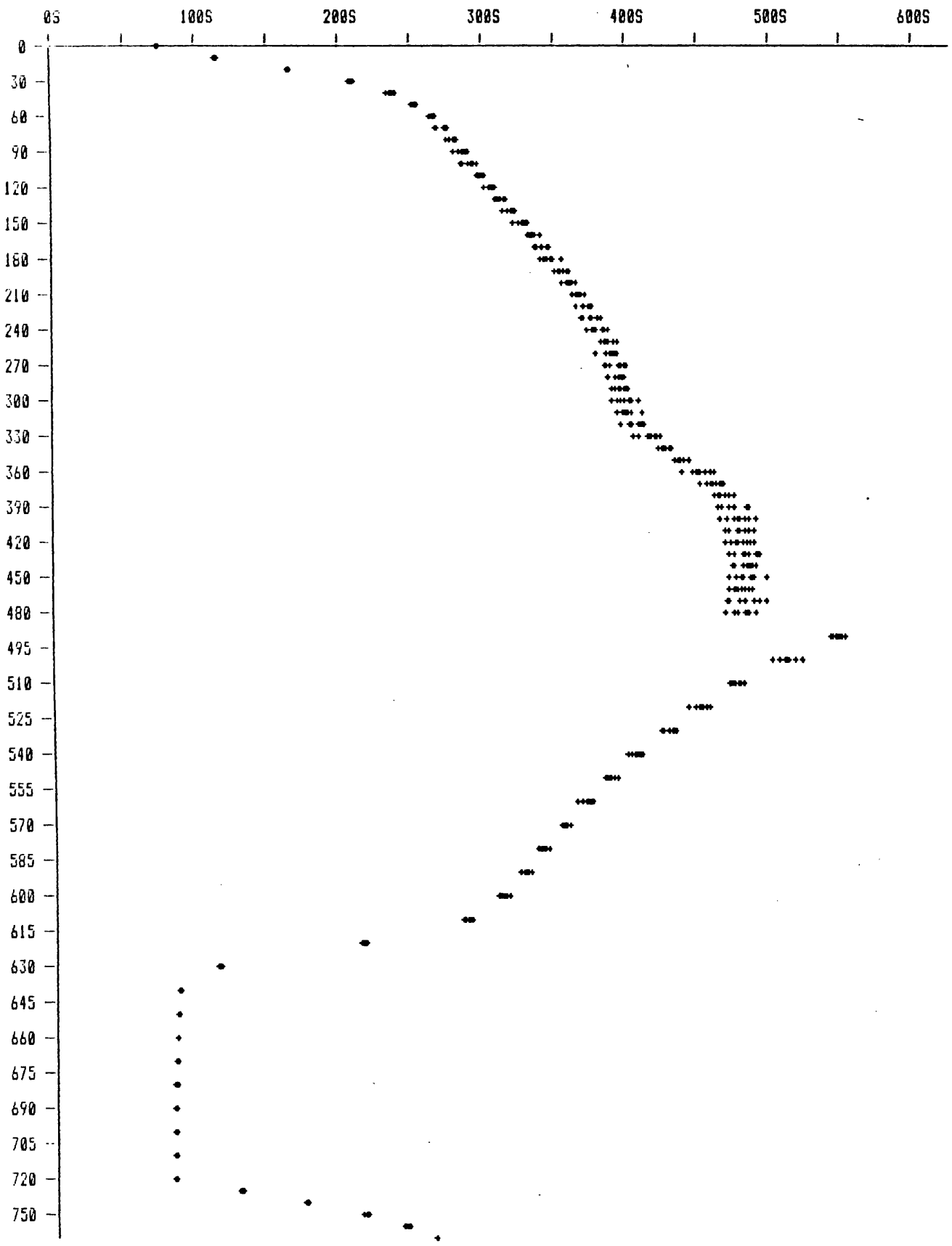
"RUN 605" : Ch-D MODULE 6 containing "P6PB6" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 8,8,8,8,8,8,8,8Hz



Graph 11(8)

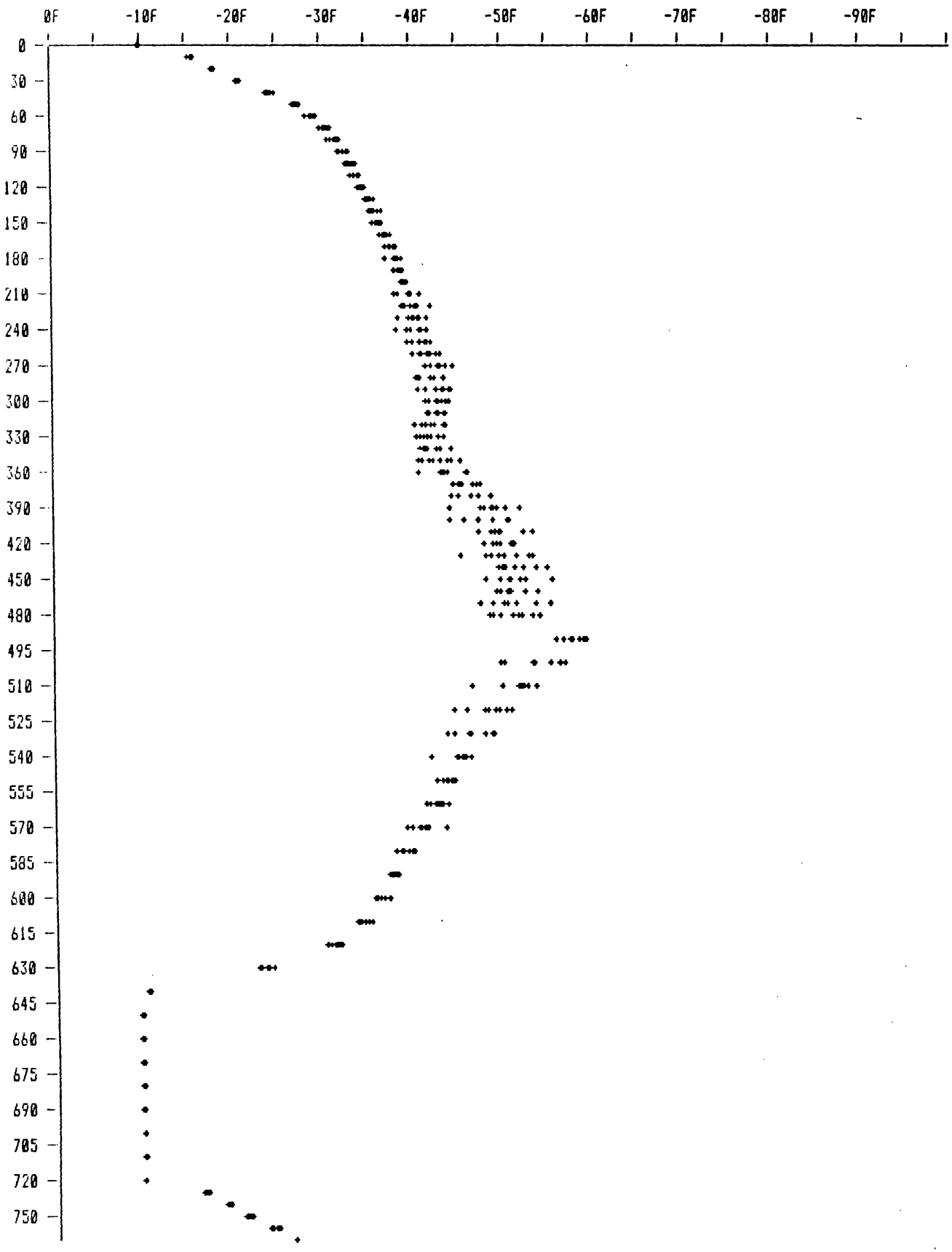

"RUN 605" : Ch-D MODULE 5 containing "P6P85" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 8,8,8,8,8,8,8,8Hz
0S
100S
200S
300S
400S
500S
600S
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

"RUN 605" : Ch-D MODULE 6 containing "P6PR6" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 8,8,8,8,8,8,8,8Hz

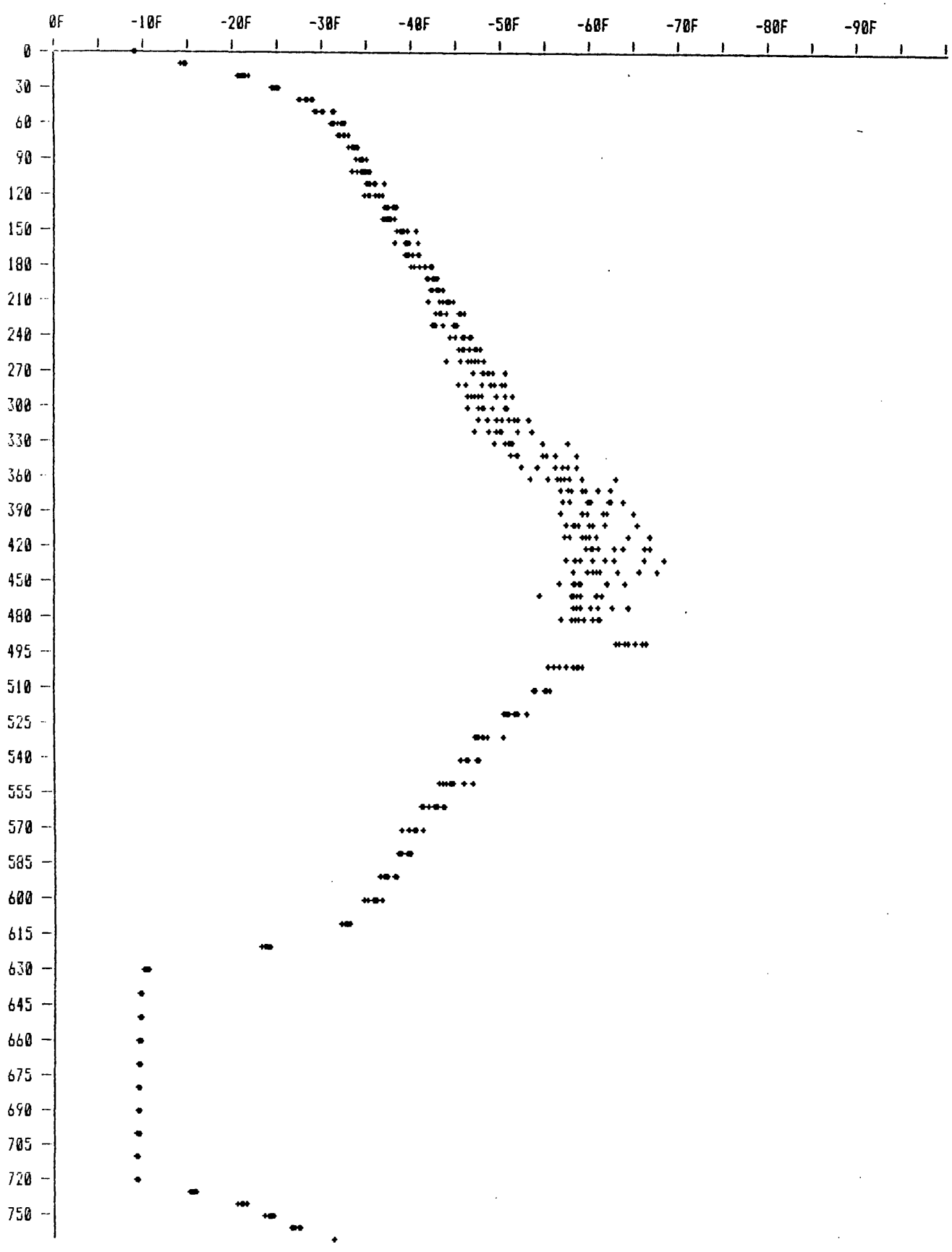


Graph 11(g)

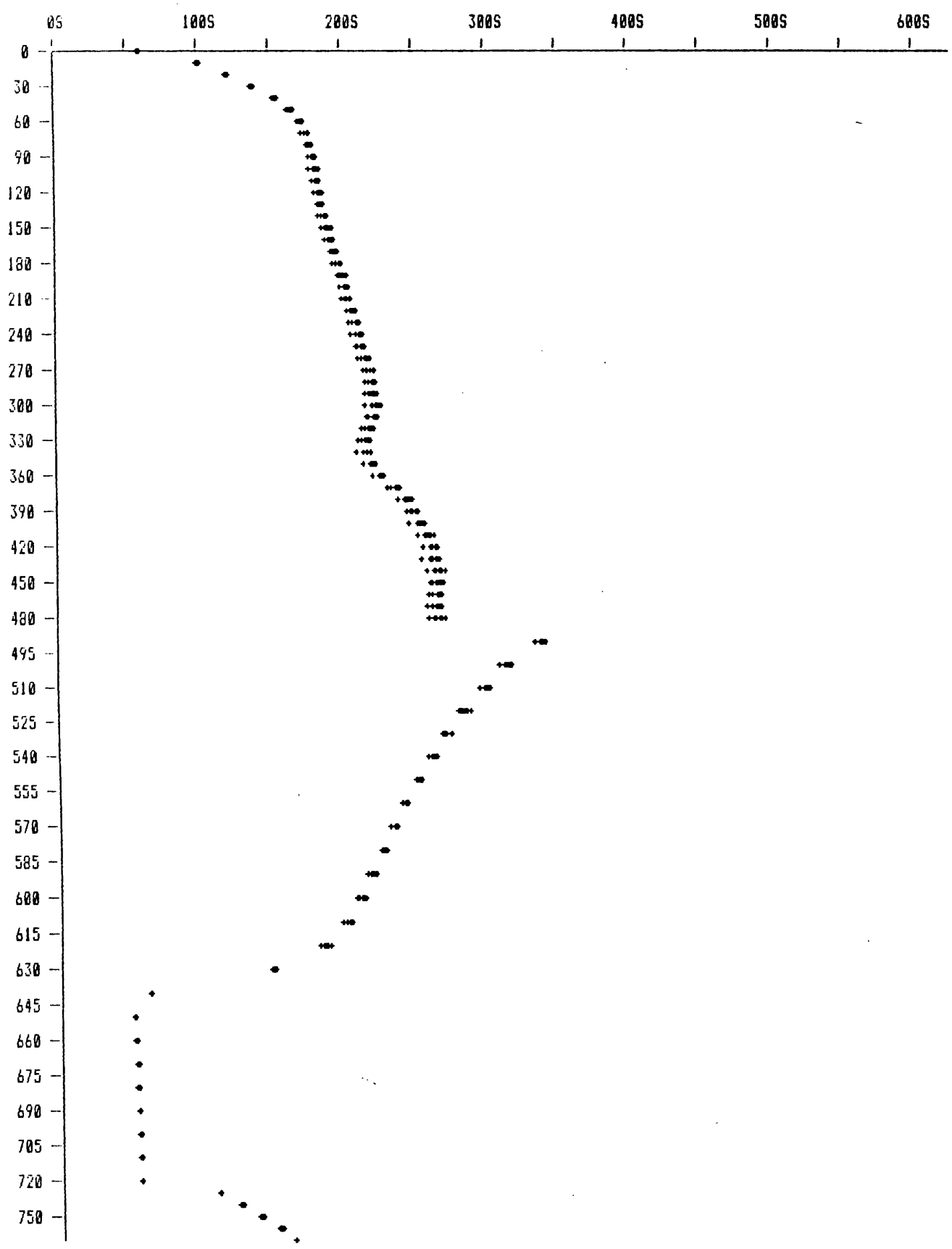
"RUN 606" : Ch-D MODULE 5 containing "P6PB5" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 4,4,4,4,4,4,4,4Hz



"RUN 606" : Ch-D MODULE 6 containing "P6PB6" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 4,4,4,4,4,4,4,4Hz

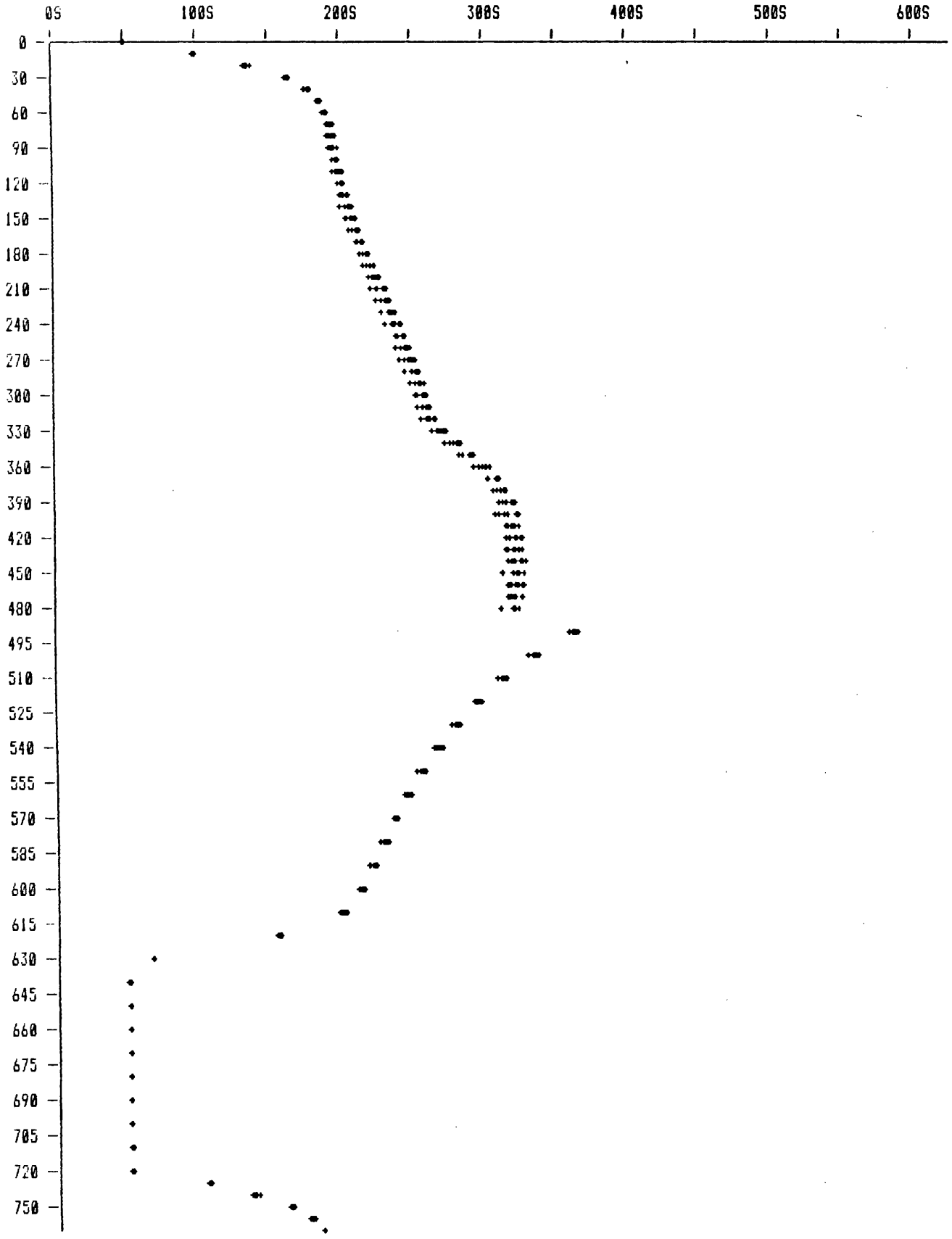


Graph 11(i)


"RUN 606" : Ch-D MODULE 5 containing "P&PB5" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 4,4,4,4,4,4,4,4Hz
0S
100S
200S
300S
400S
500S
600S
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

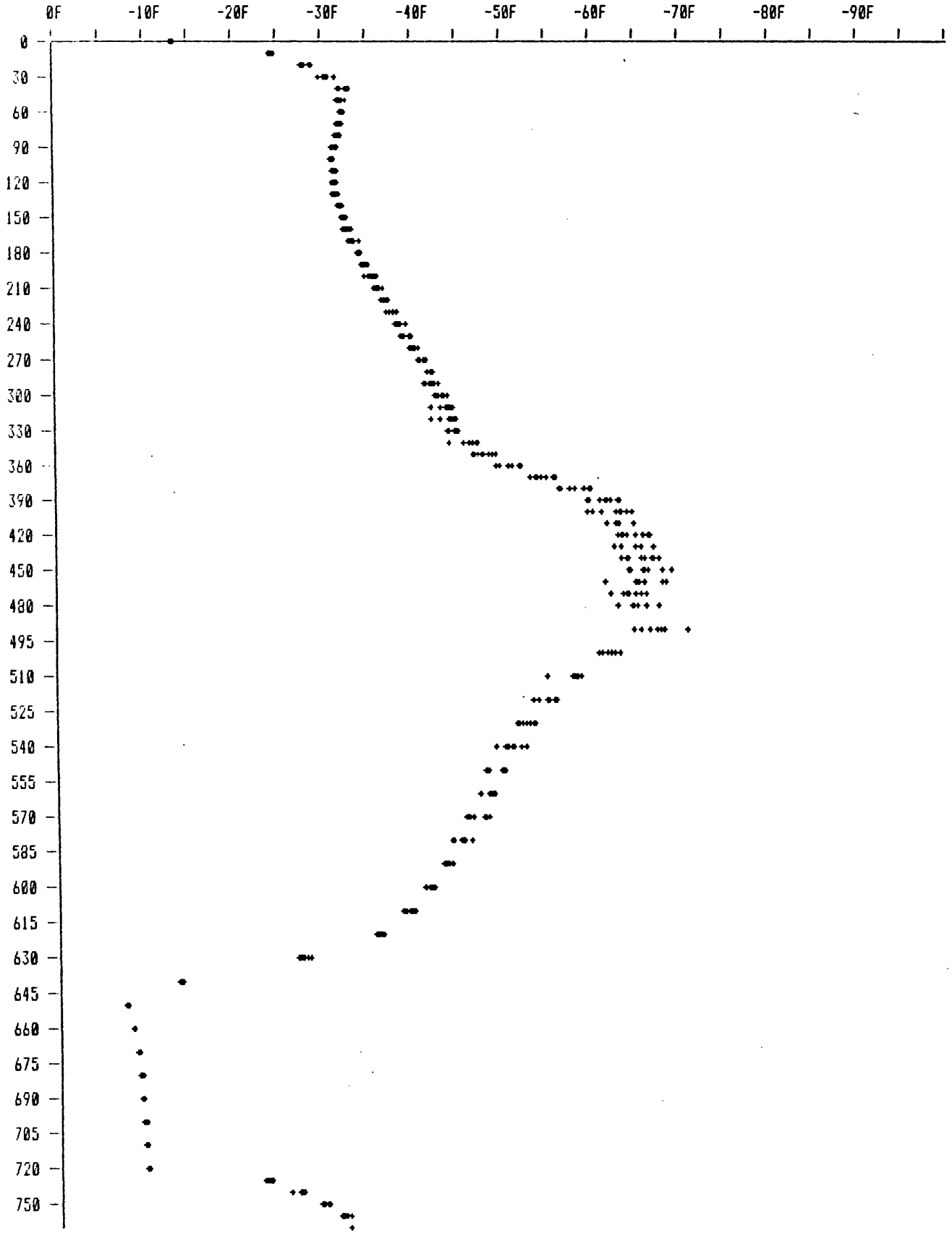
Graph 11(j)

"RUN 606" : Ch-D MODULE 6 containing "P6PB6" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 4,4,4,4,4,4,4,4Hz

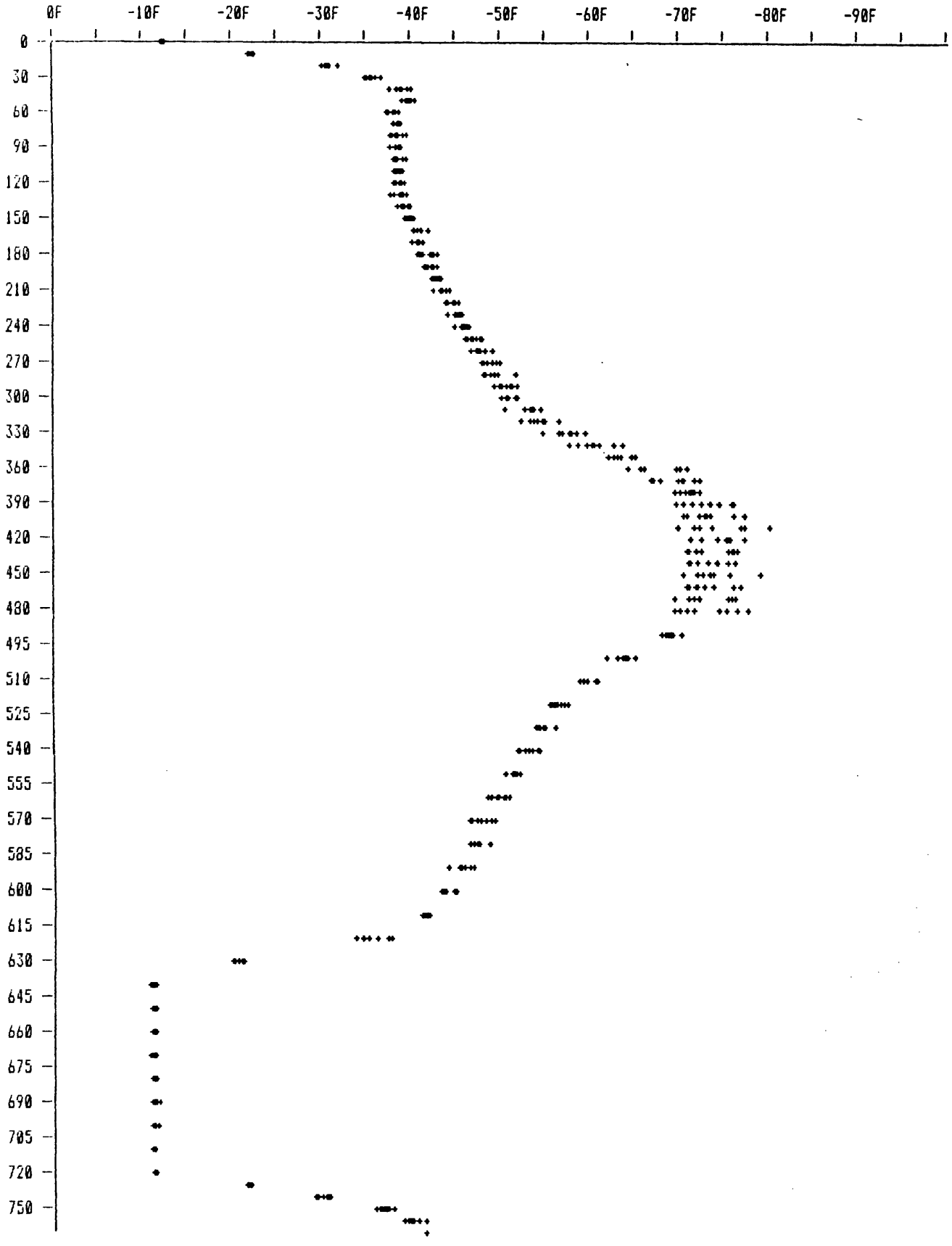


Graph 11(k)

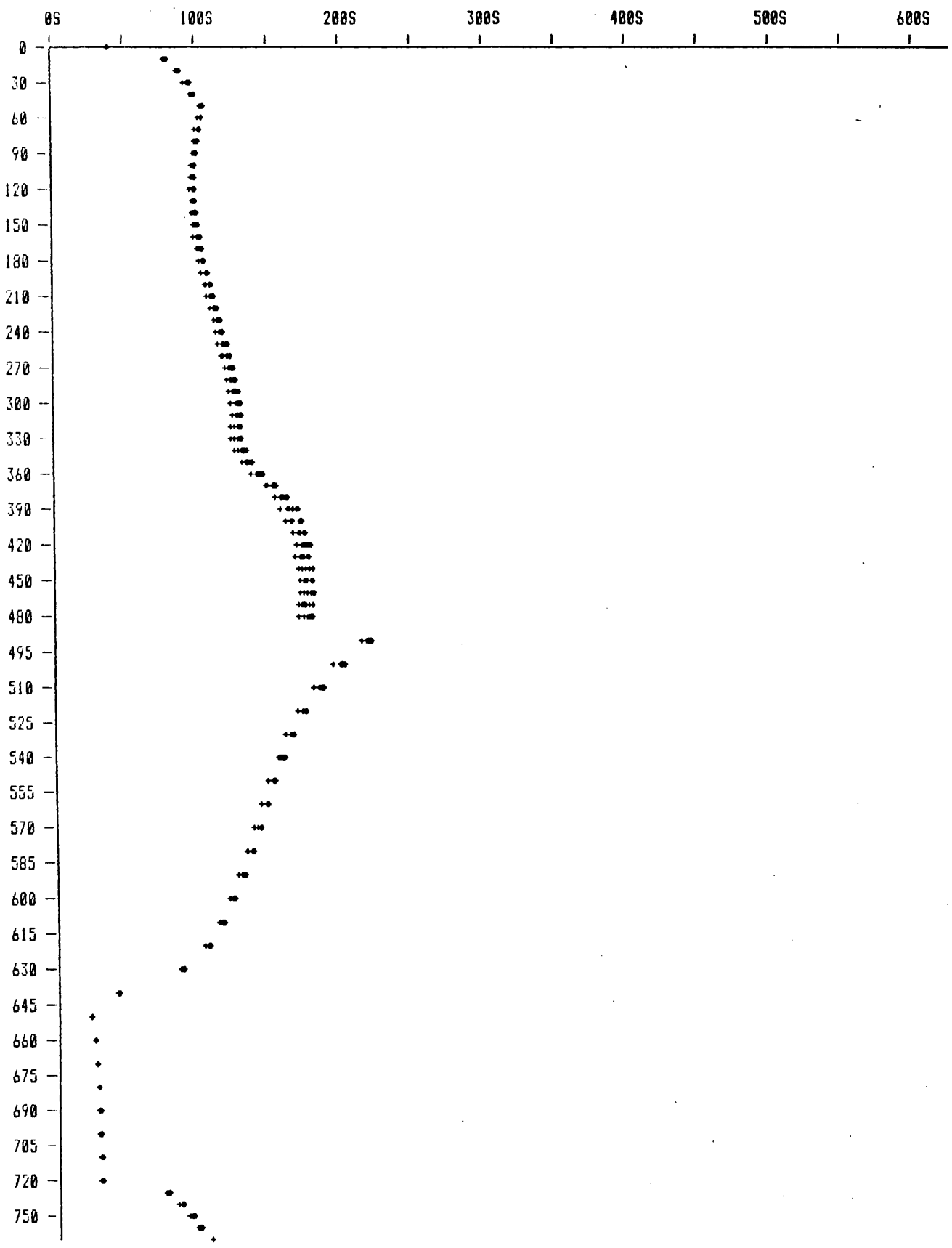
"RUN 610" : Ch-D MODULE 5 containing "P6PB5" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 2,2,2,2,2,2,2,2Hz



"RUN 610" : Ch-D MODULE 6 containing "P6PB6" : 2nd HARMONIC TRANSCAPACITANCE PROFILES at 2,2,2,2,2,2,2,2Hz

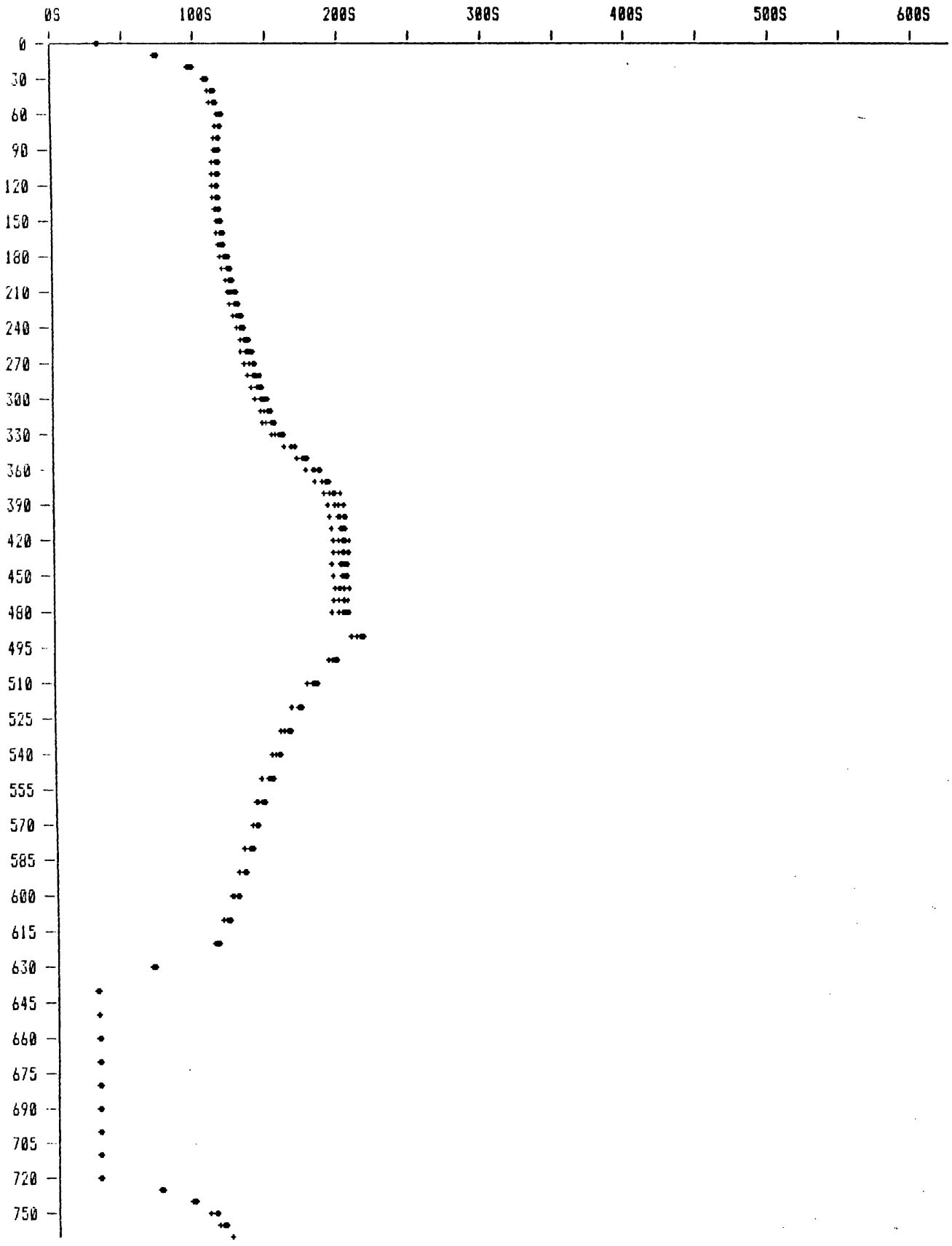


Graph 11(a)

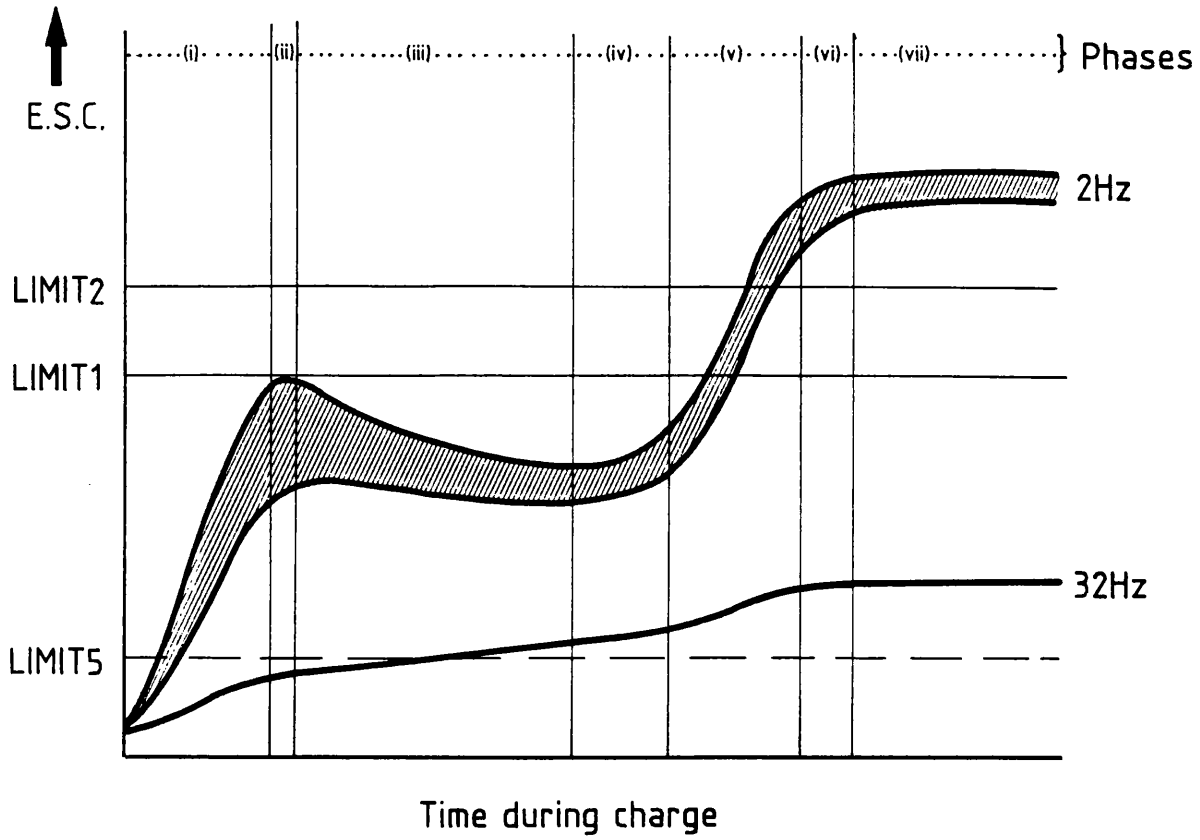

"RUN 610" : Ch-D MODULE 5 containing "P6PB5" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 2,2,2,2,2,2,2,2Hz
0S
100S
200S
300S
400S
500S
600S
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

Graph 11(a)

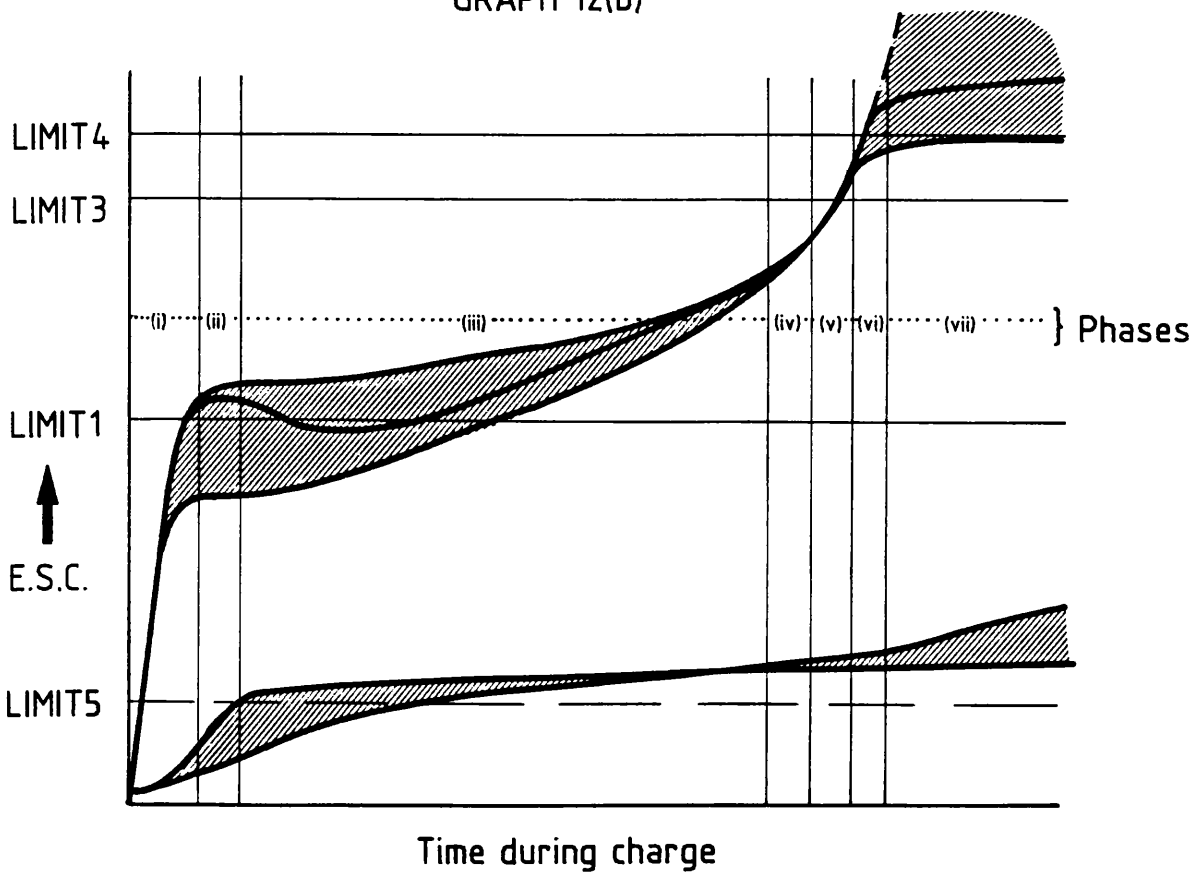
"RUN 610" : Ch-D MODULE 6 containing "P6P86" : 2nd HARMONIC TRANSCONDUCTANCE PROFILES at 2,2,2,2,2,2,2,2Hz



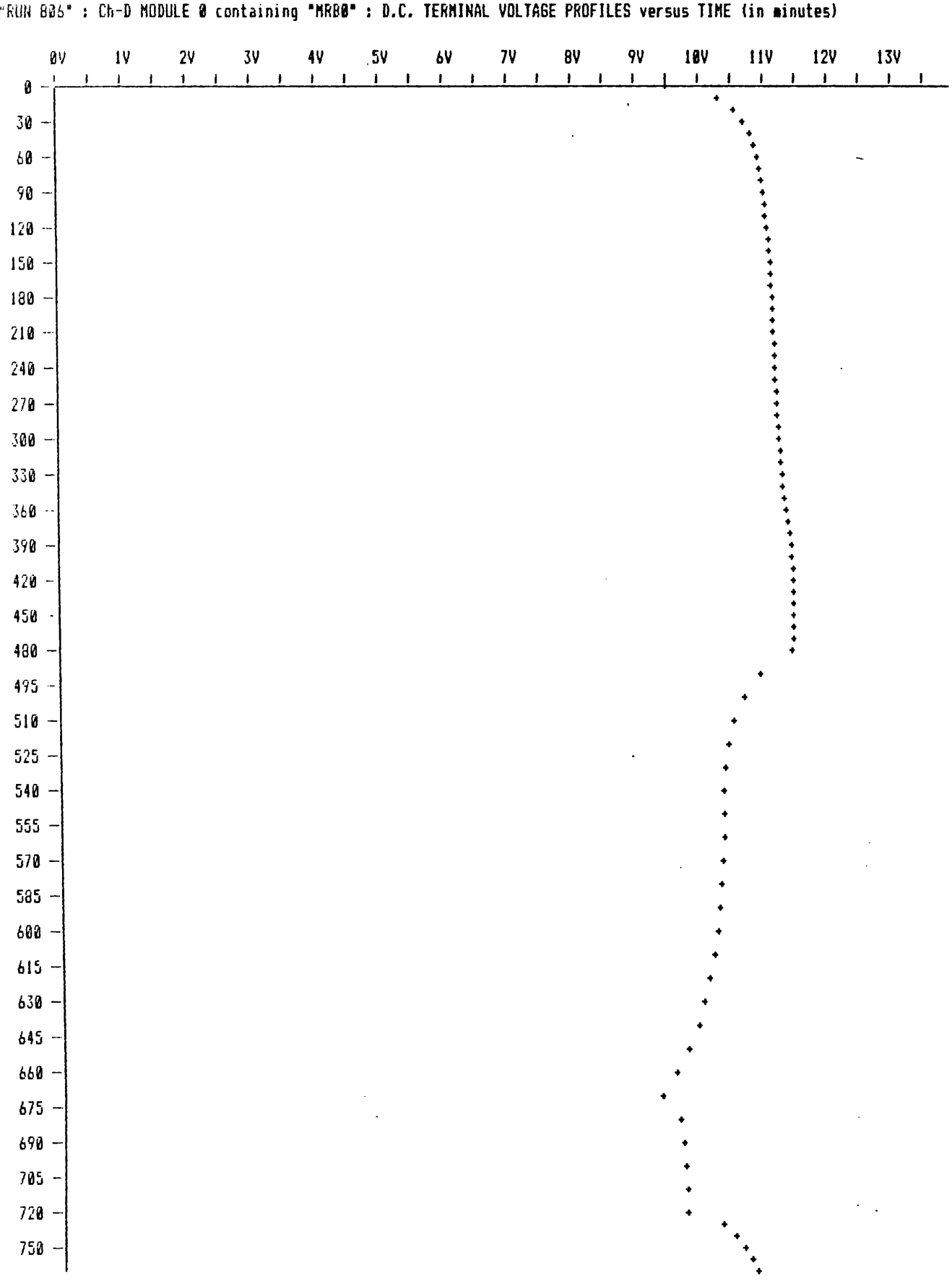
GRAPH 12(a)



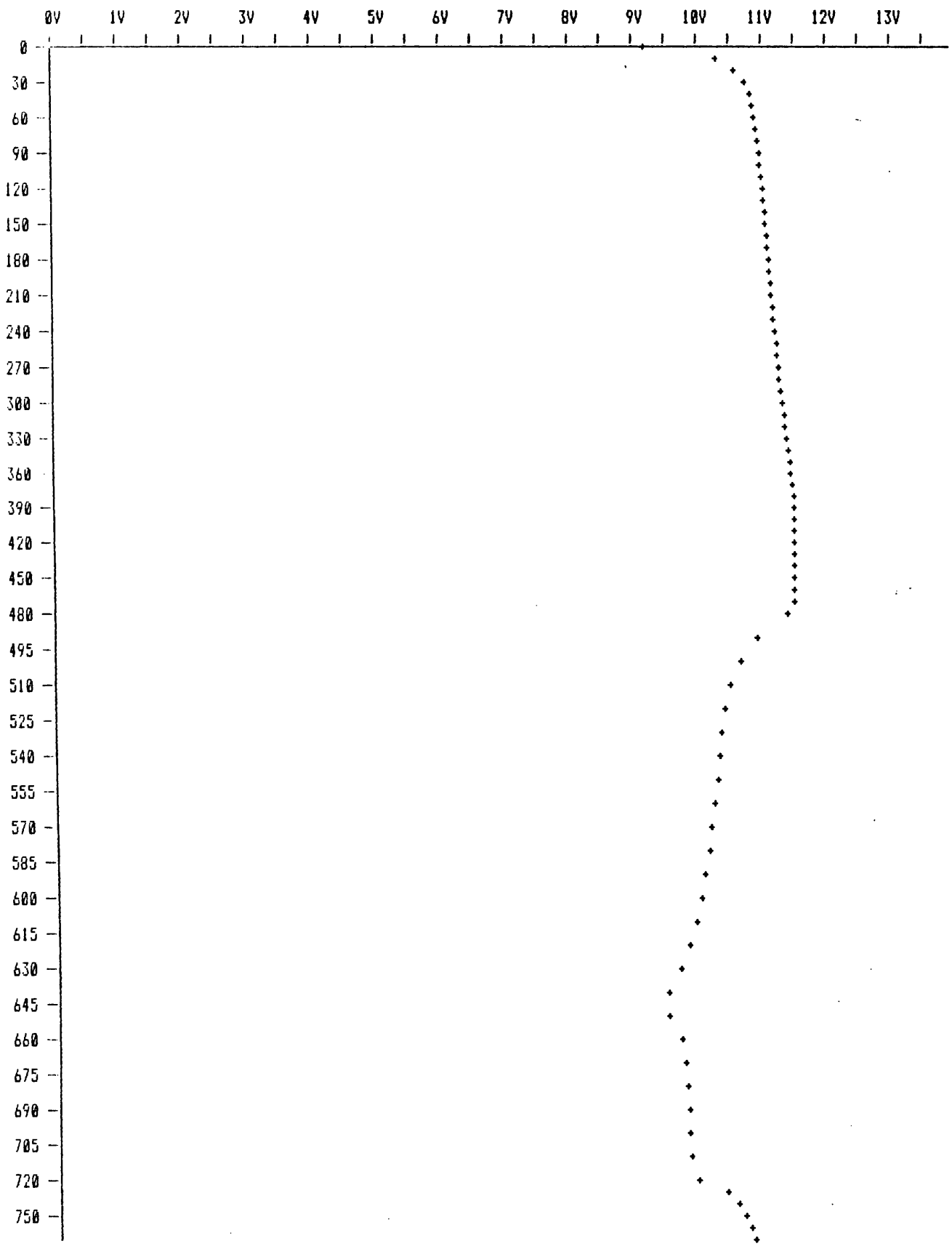
GRAPH 12(b)



Graph 13(a)

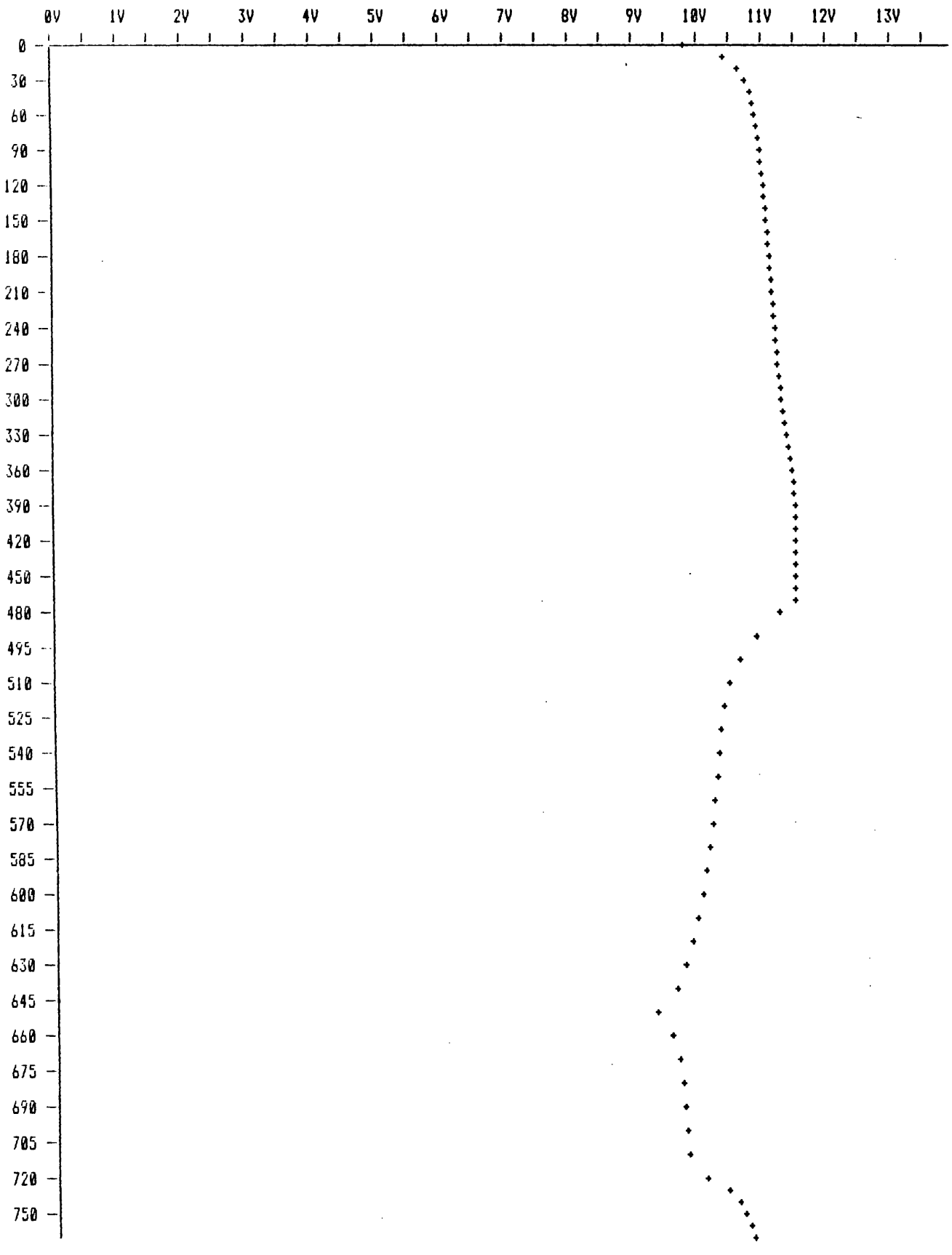

"RUN 806" : Ch-D MODULE 0 containing "MRB0" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)
0V
1V
2V
3V
4V
5V
6V
7V
8V
9V
10V
11V
12V
13V
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
495
510
525
540
555
570
585
600
615
630
645
660
675
690
705
720
750

"RUN 806" : Ch-D MODULE 1 containing "MRB1" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 15(8)

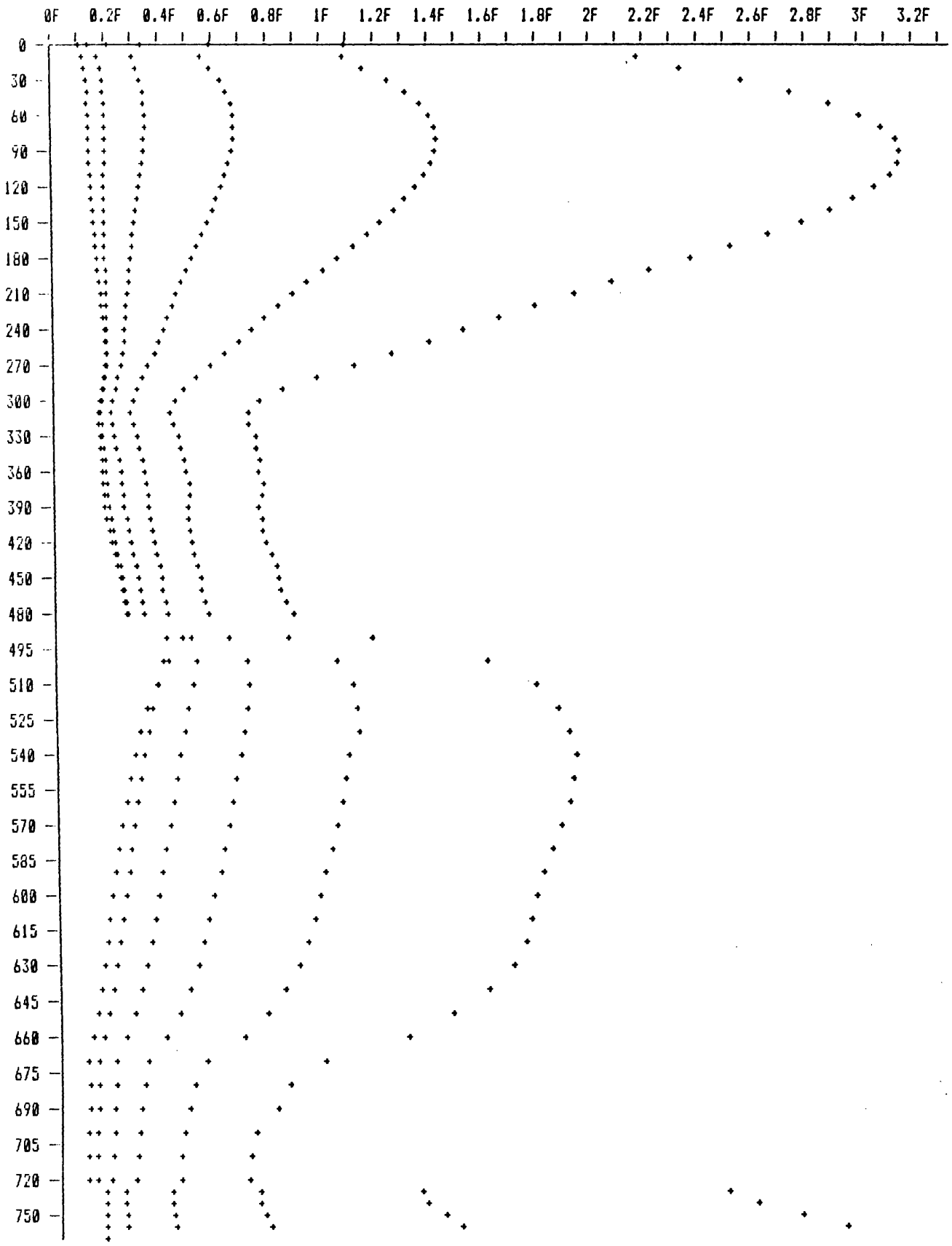
"RUN 806" : Ch-D MODULE 5 containing "MRB5" : D.C. TERMINAL VOLTAGE PROFILES versus TIME (in minutes)



Graph 16(c)

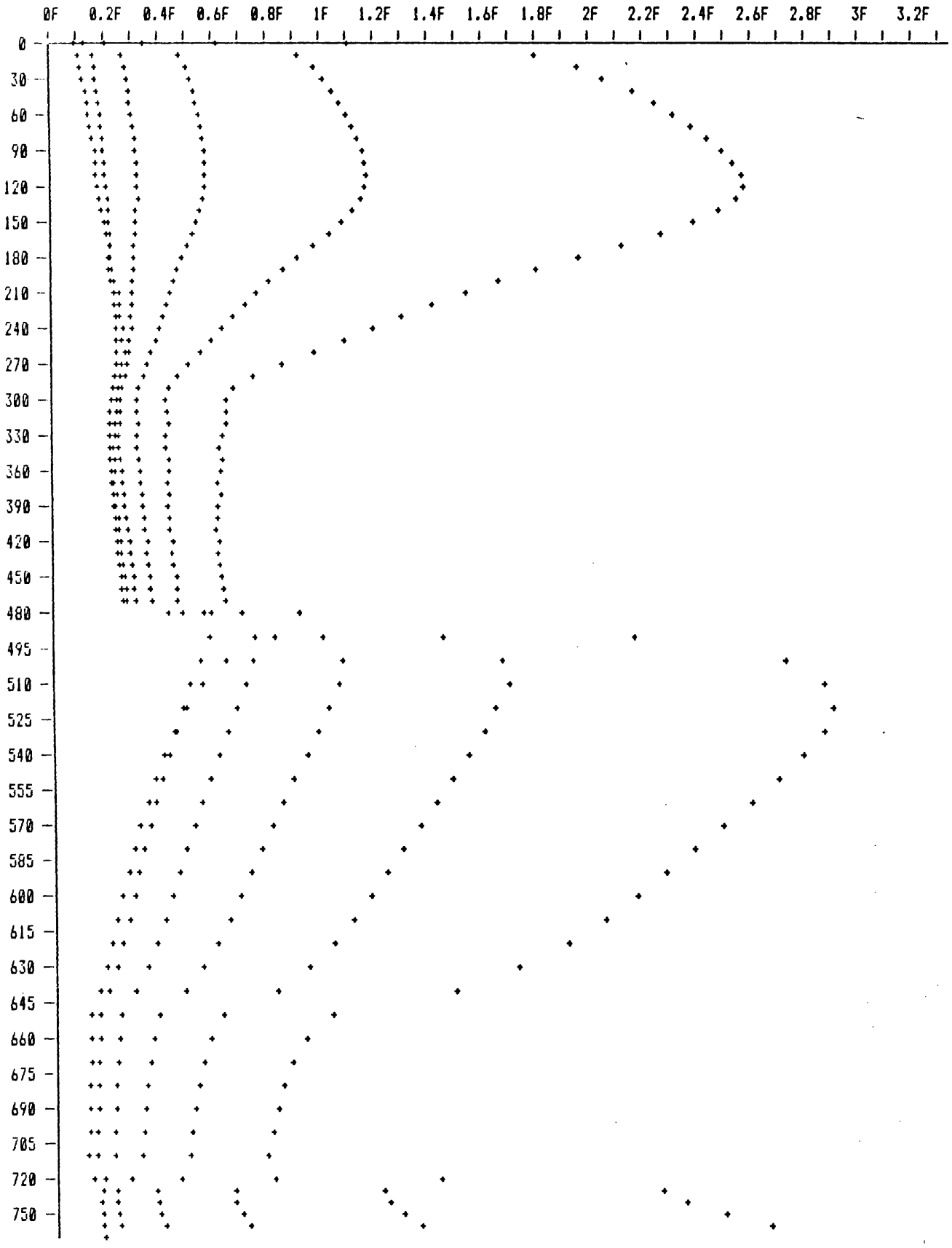
Note: Curve order is generally 16Hz >>> 0.5Hz

"RUN 806" : Ch-D MODULE 0 containing "MR80" : E.S.CAPACITANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Note: Curve order is generally 16Hz >>> 0.5Hz

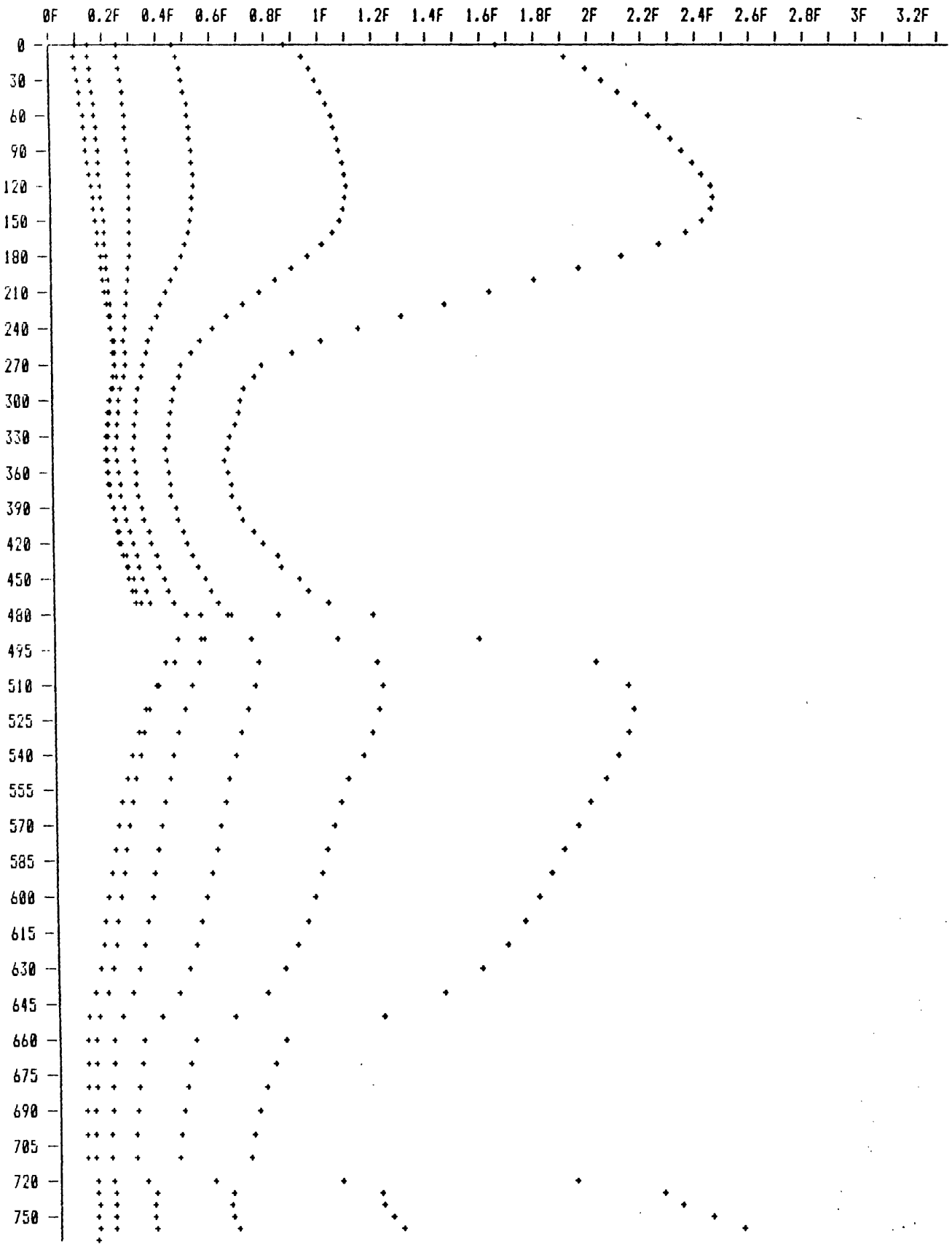
"RUN 806" : Ch-D MODULE 1 containing "MRB1" : E.S.CAPACITANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Graph 13(1)

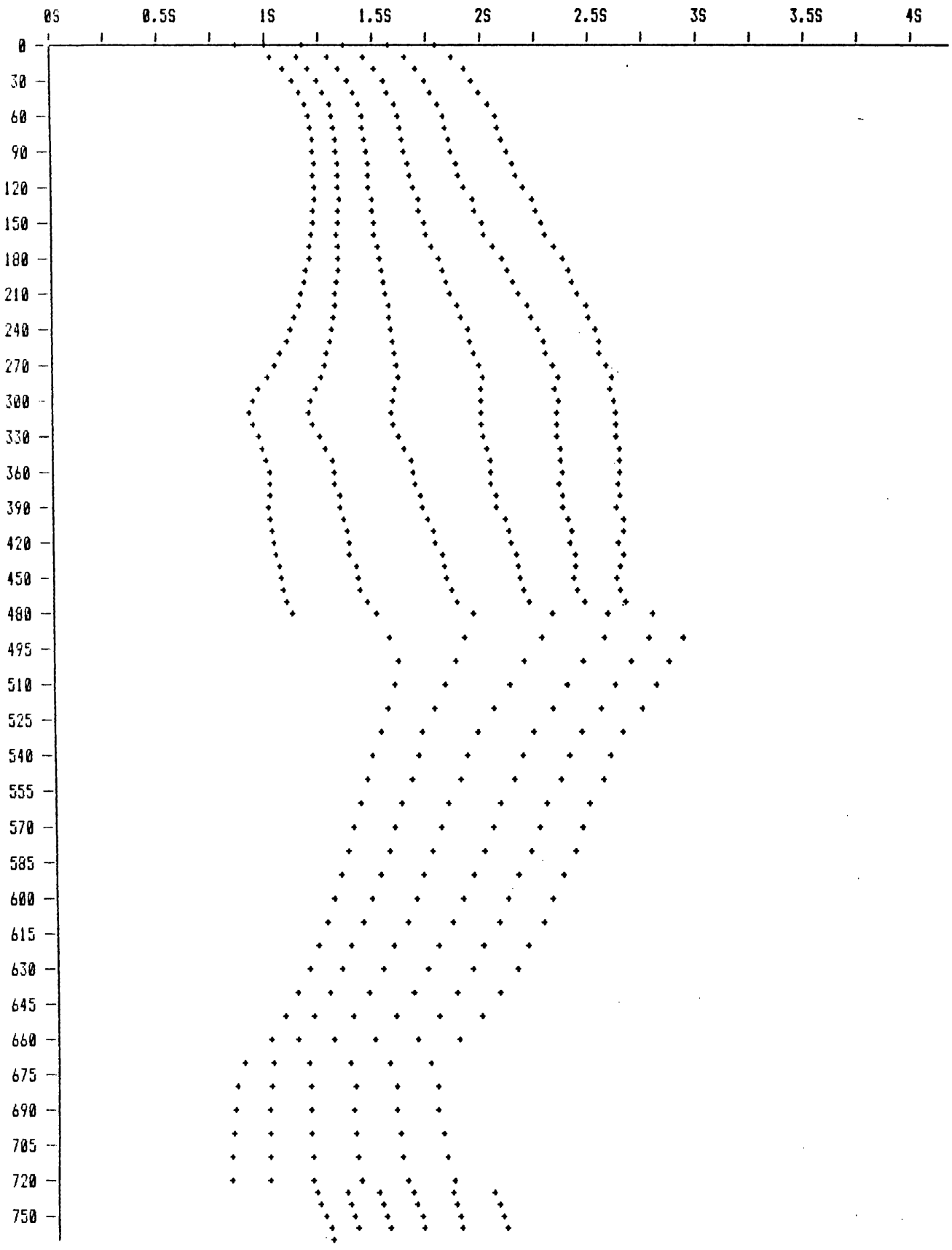
Note: Curve order is generally 16Hz >>> 0.5Hz

"RUN 806" : Ch-D MODULE 5 containing "MRB5" : E.S.CAPACITANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Note: Curve order is 0.5Hz >>> 16Hz

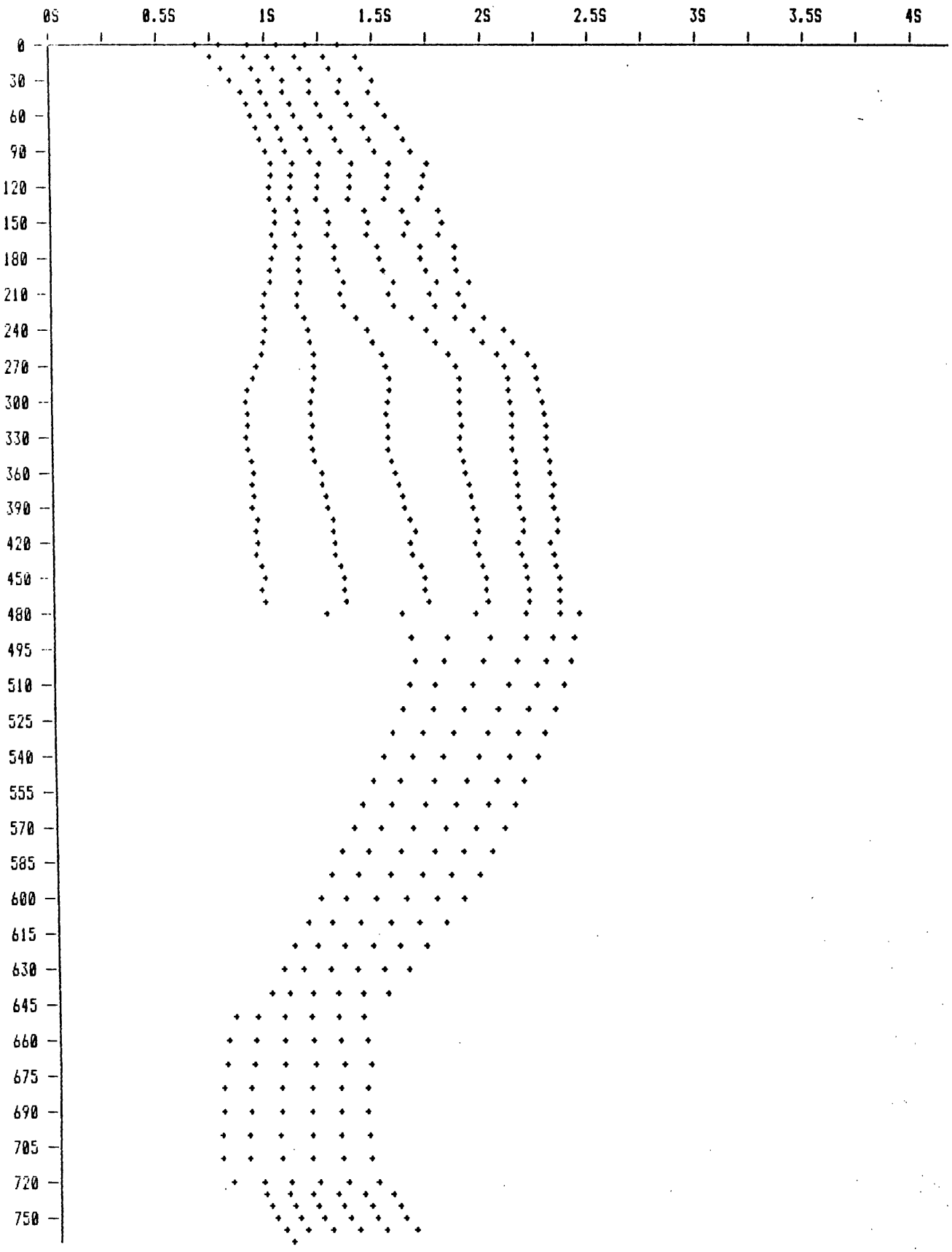
"RUN 006" : Ch-D MODULE 0 containing "MRB0" : E.S.CONDUCTANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Graph 13(A)

Note: Curve order is 0.5Hz >>> 16Hz

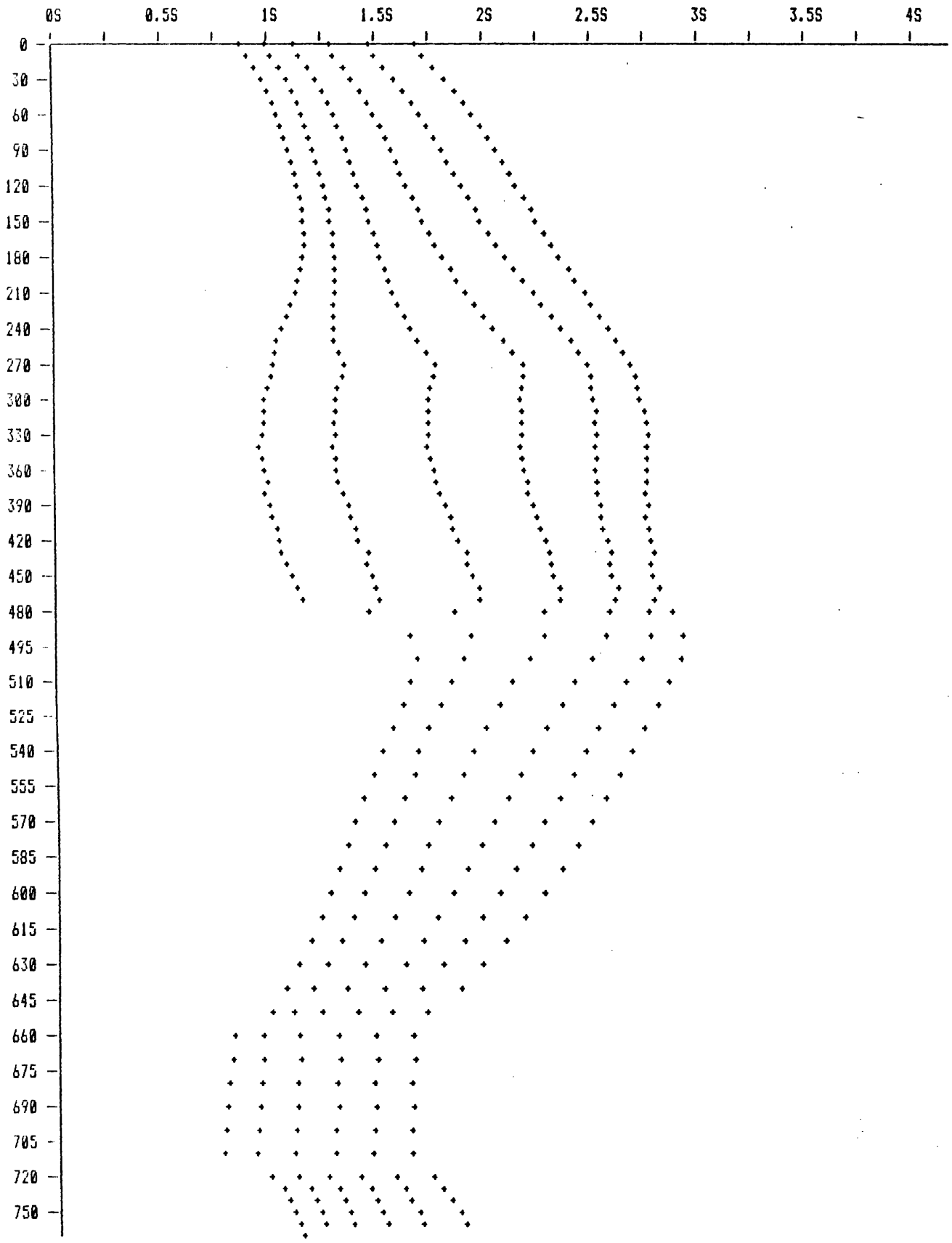
"RUN 806" : Ch-D MODULE 1 containing "MRB1" : E.S.CONDUCTANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Graph 15(1)

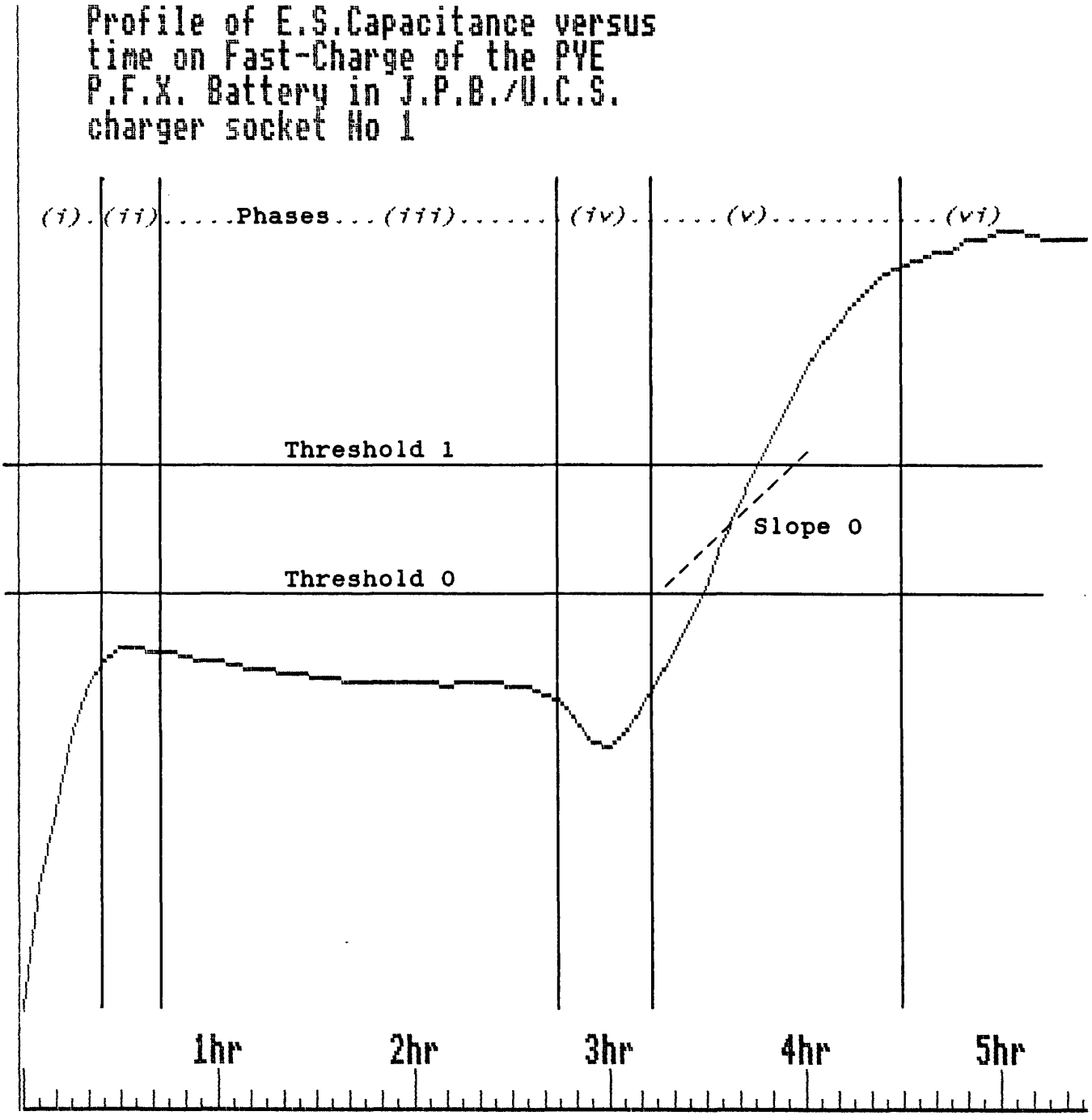
Note: Curve order is 0.5Hz >>> 16Hz

"RUN 806" : Ch-D MODULE 5 containing "MRB5" : E.S.CONDUCTANCE PROFILES at frequencies 16,8,4,2,1,0.5Hz



Graph 101(a)

Result for J.P.B./U.C.S.-Charger-RUN 3 :

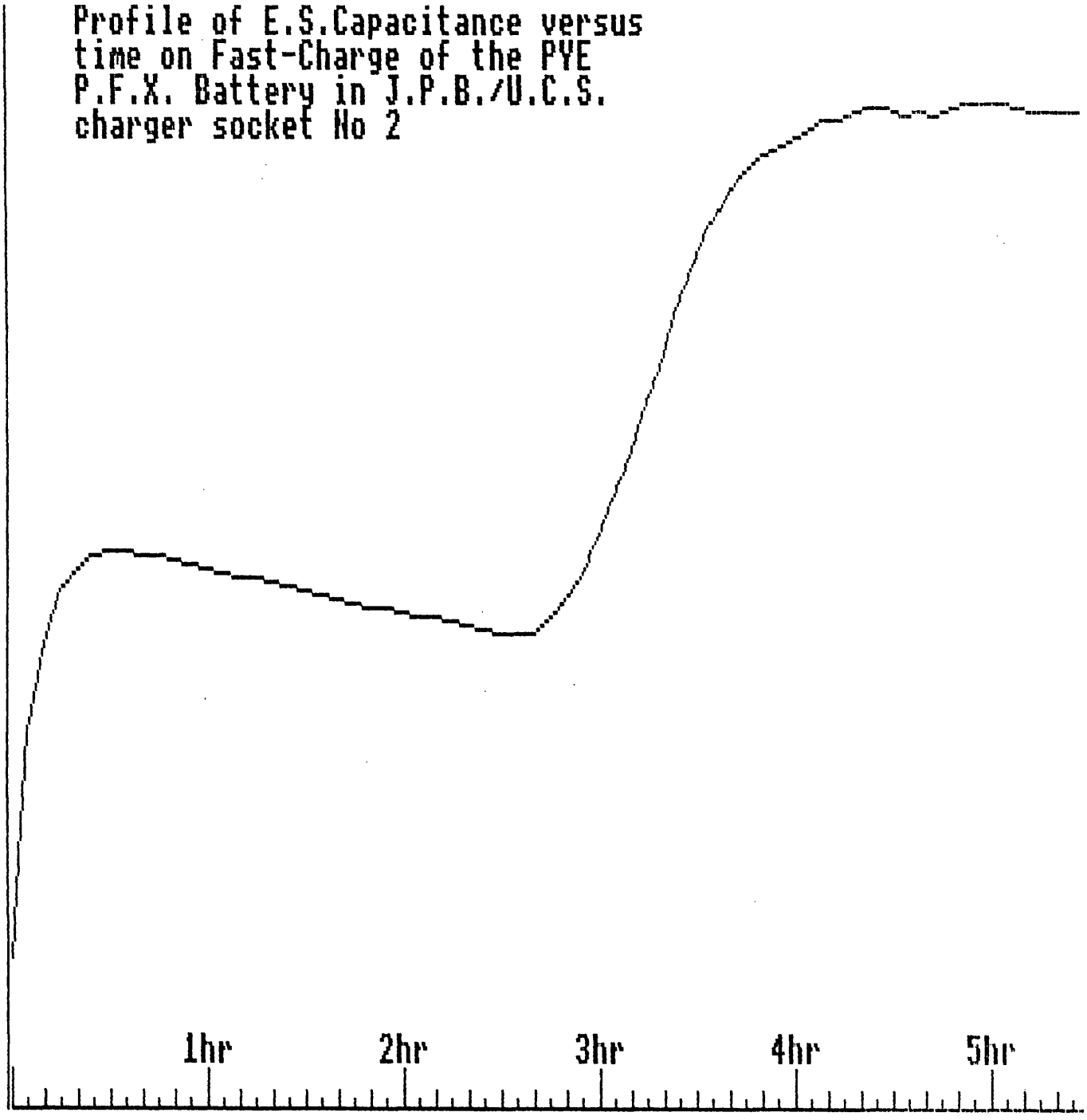


Note:- The y axis represents 2Hz E.S.C. but is uncalibrated.

Phases:- *(i)* = rise, *(ii)* = peak (may be vague), *(iii)* = approximate plateau (may be rising), *(iv)* = trough (may be vague or absent), *(v)* = final rise, *(vi)* = final plateau.

Graph 101(b)

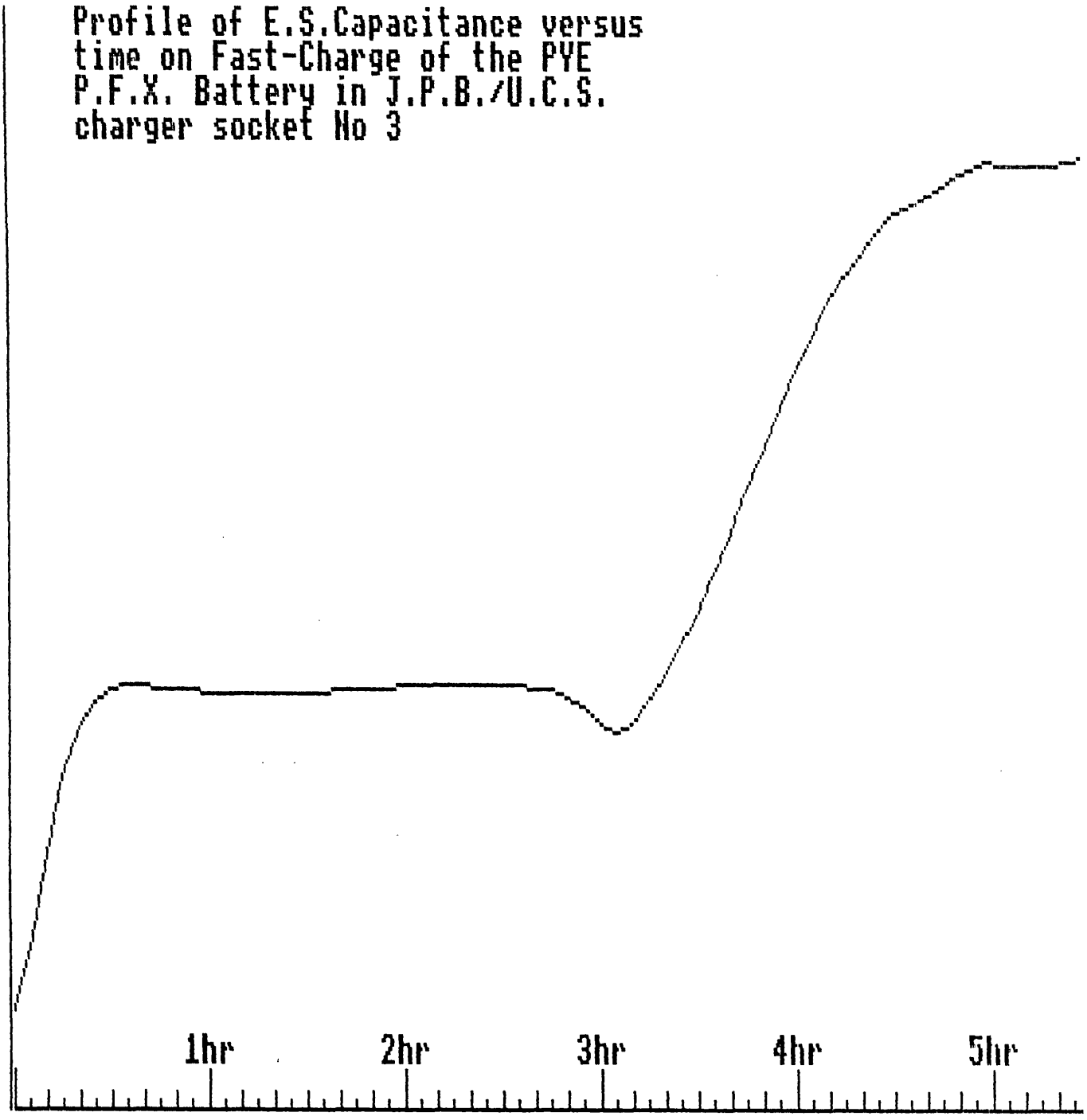
Result for J.P.B./U.C.S.-Charger-RUN 3 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 101(c)

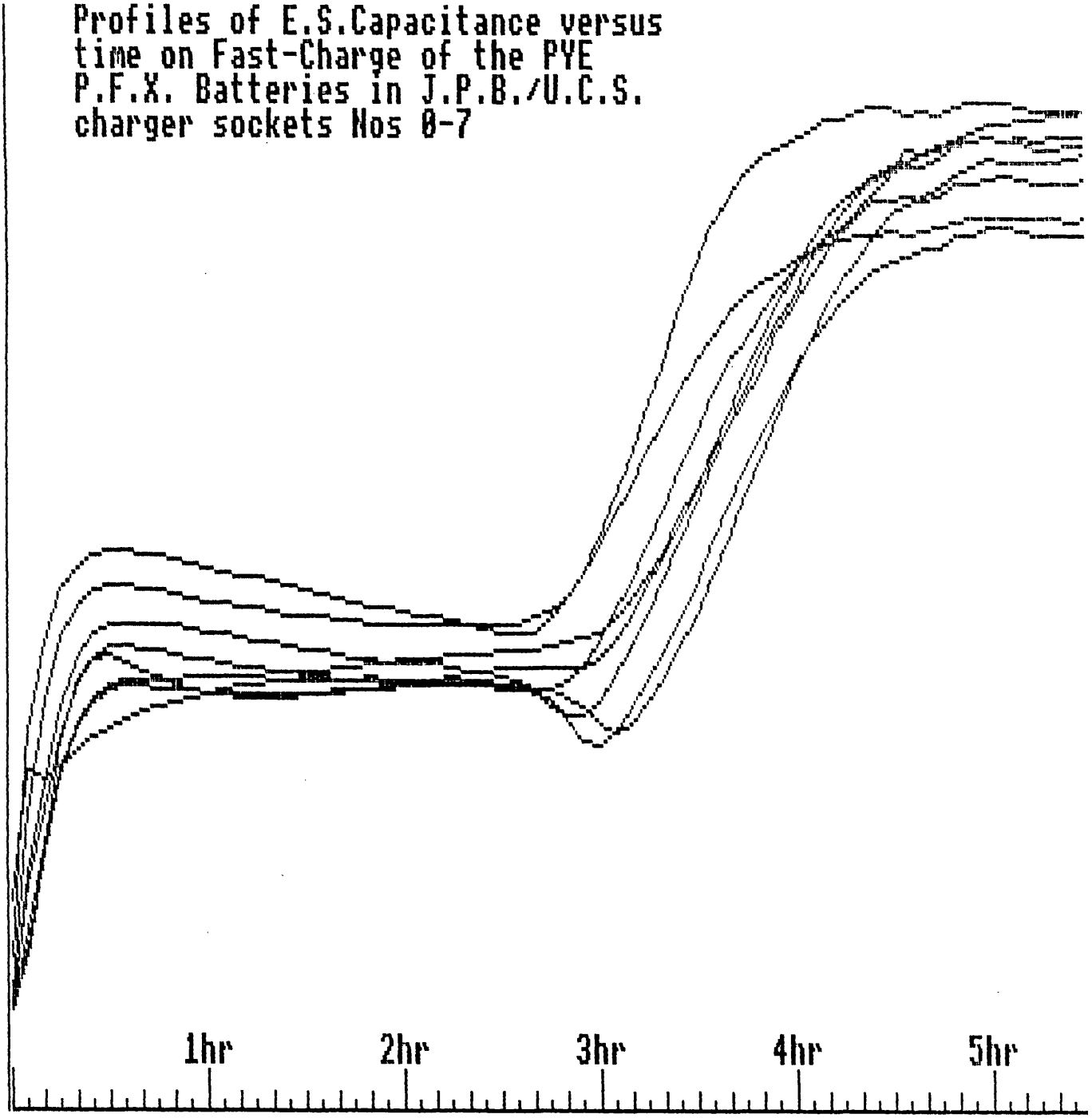
Result for J.P.B./U.C.S.-Charger-RUN 3 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 101(d)

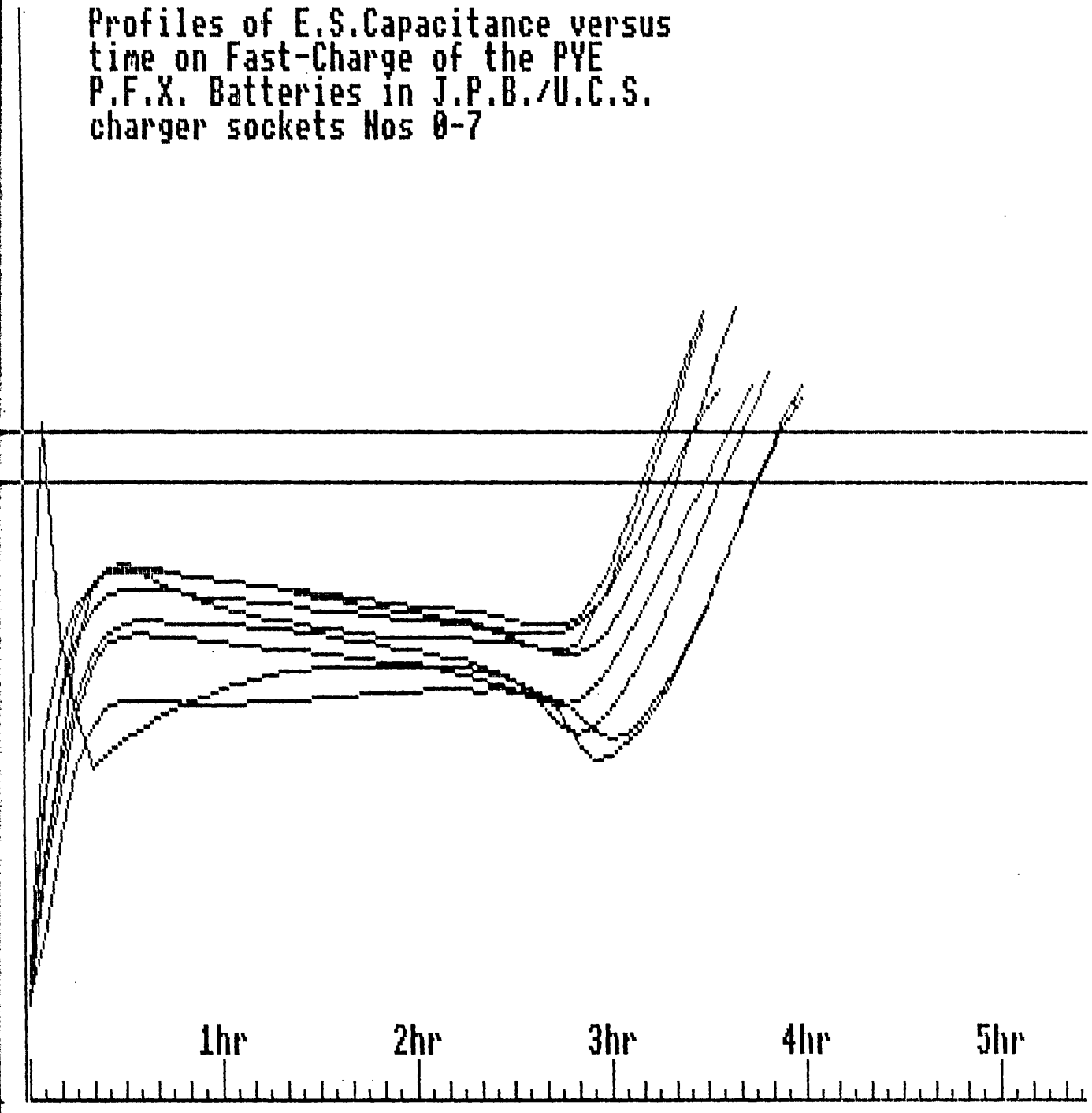
Results for J.P.B./U.C.S.-Charger-RUN 3 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 102(a)

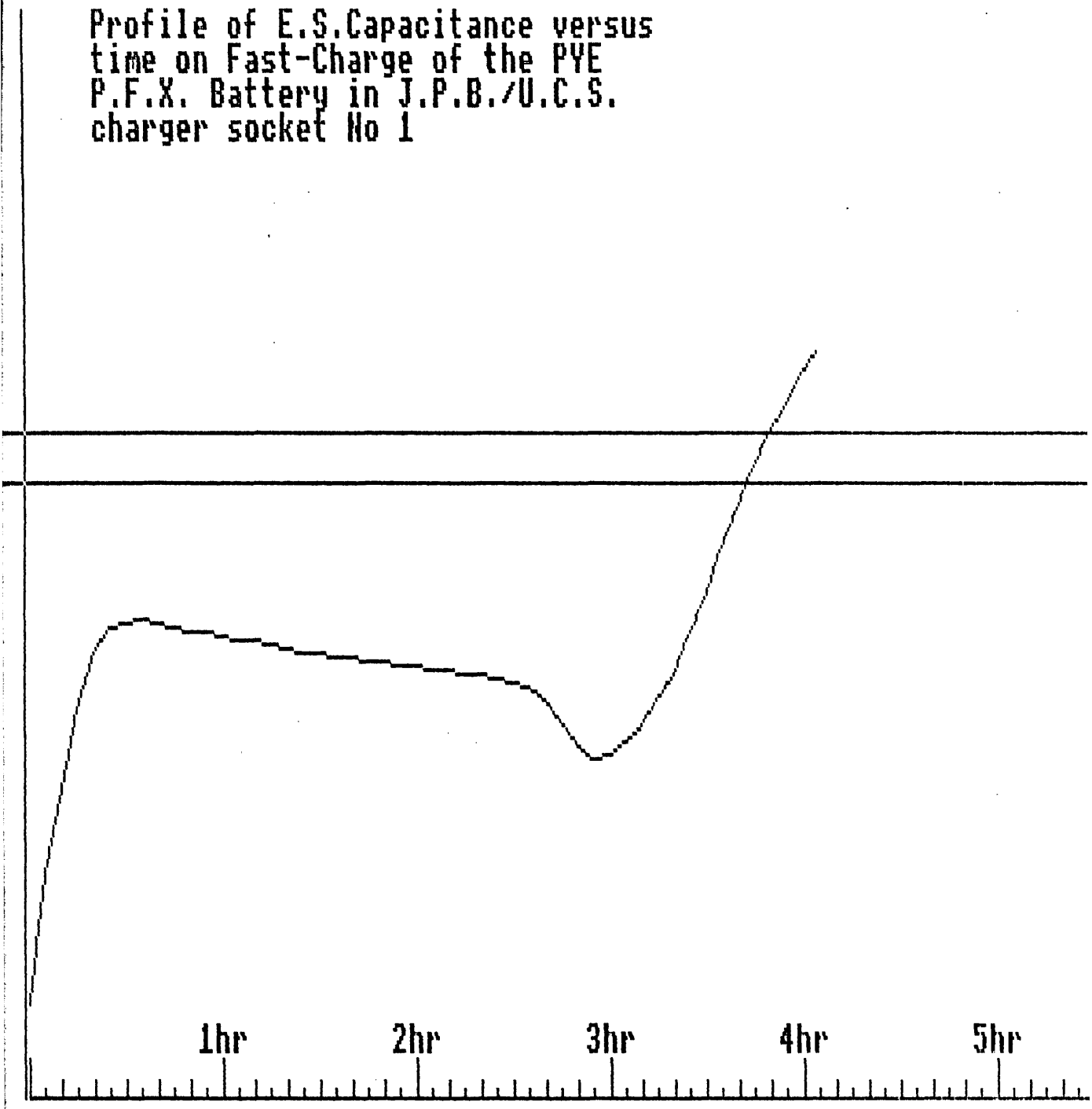
Results for J.P.B./U.C.S.-Charger-RUN 5 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 102(b)

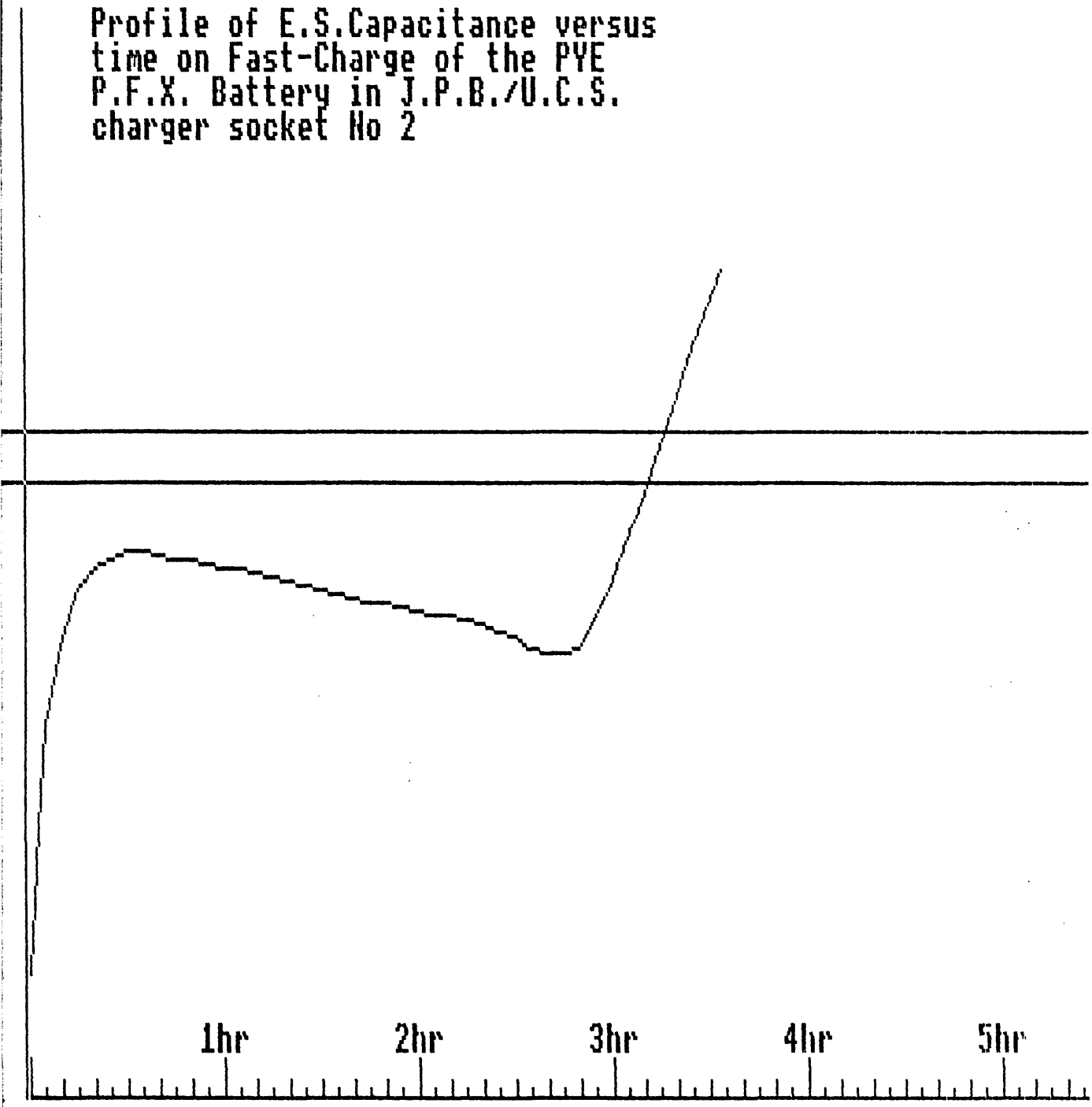
Result for J.P.B./U.C.S.-Charger-RUN 6 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 102(c)

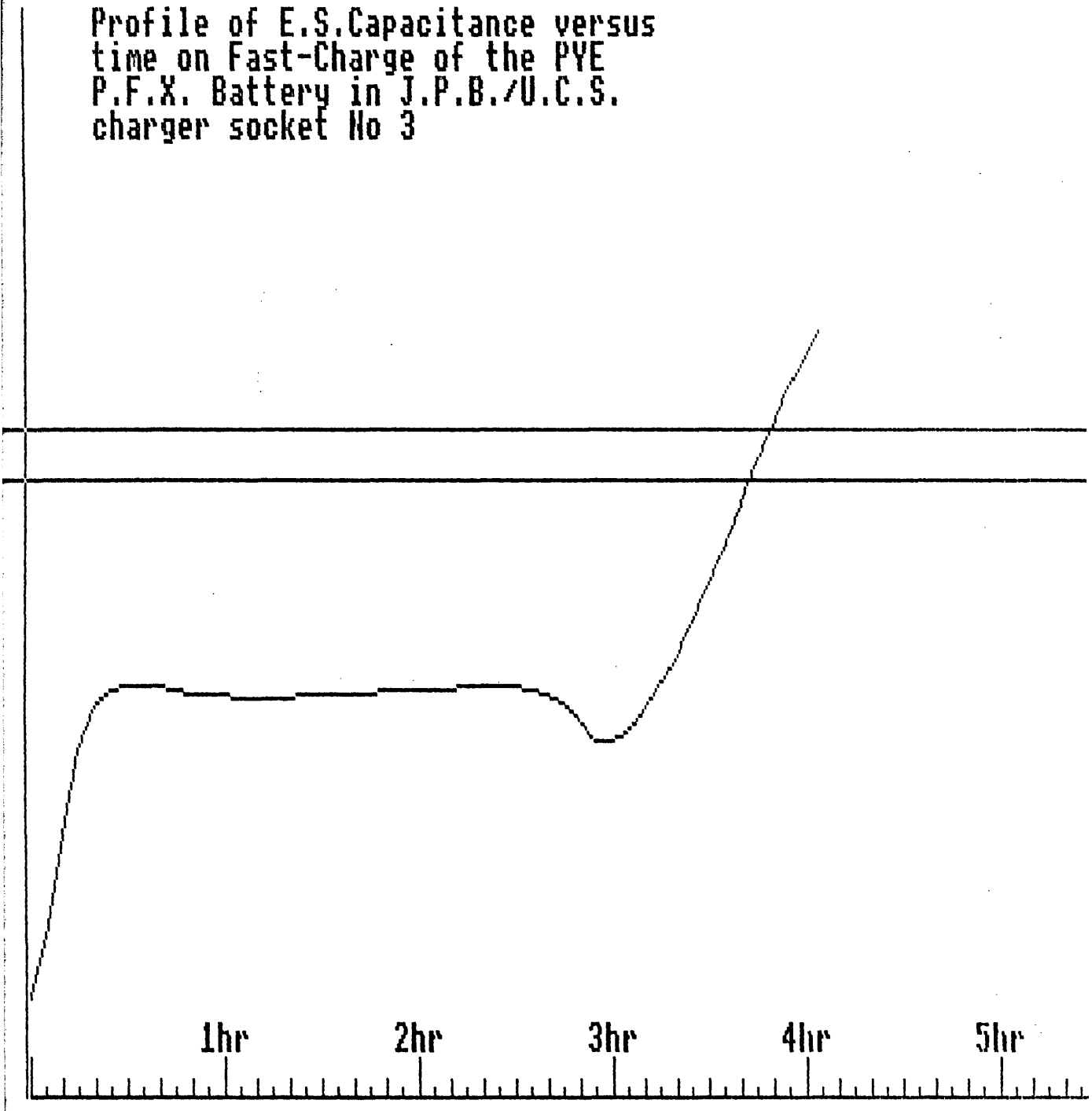
Result for J.P.B./U.C.S.-Charger-RUN 6 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 102(d)

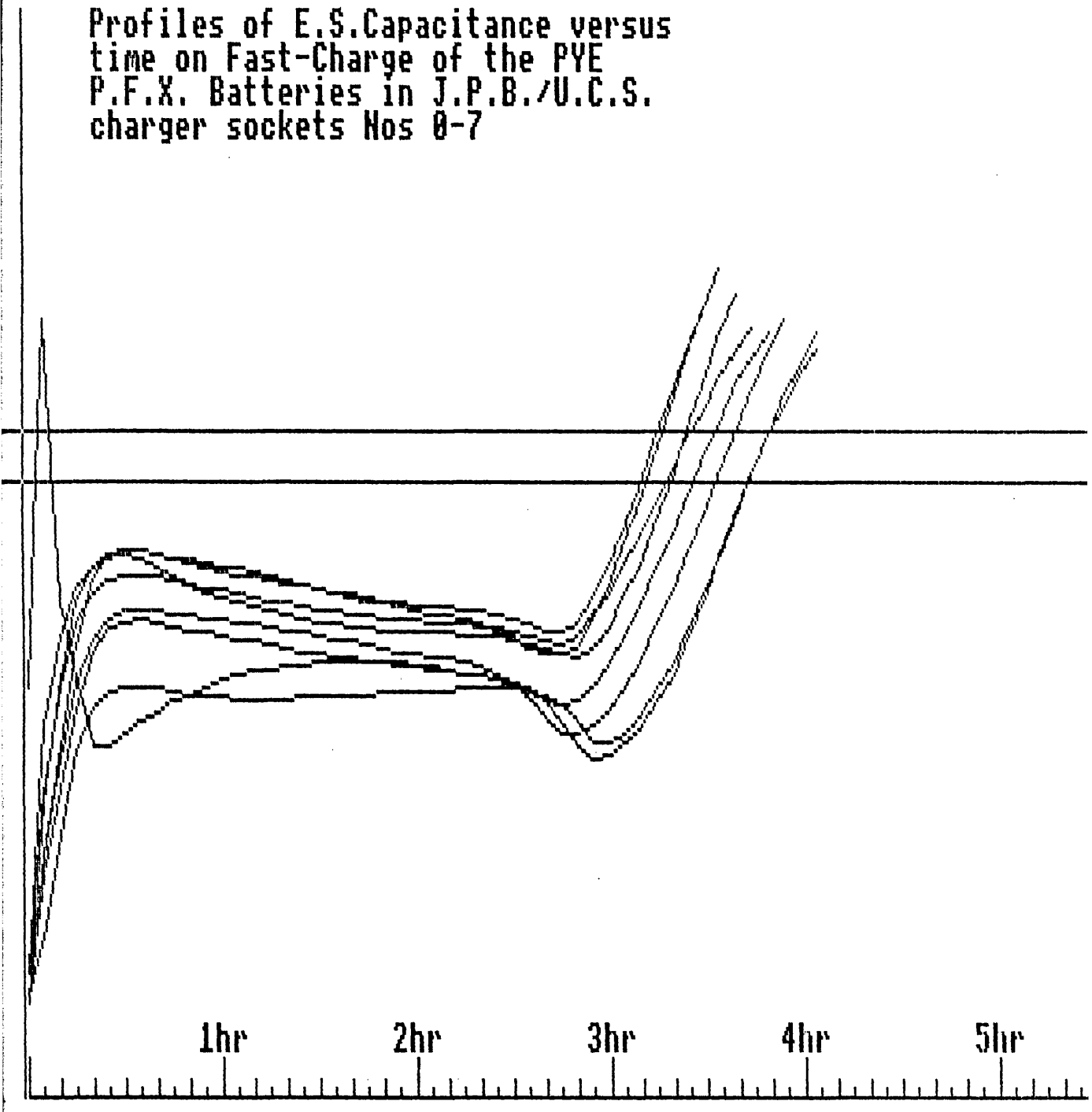
Result for J.P.B./U.C.S.-Charger-RUN 6 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 102(e)

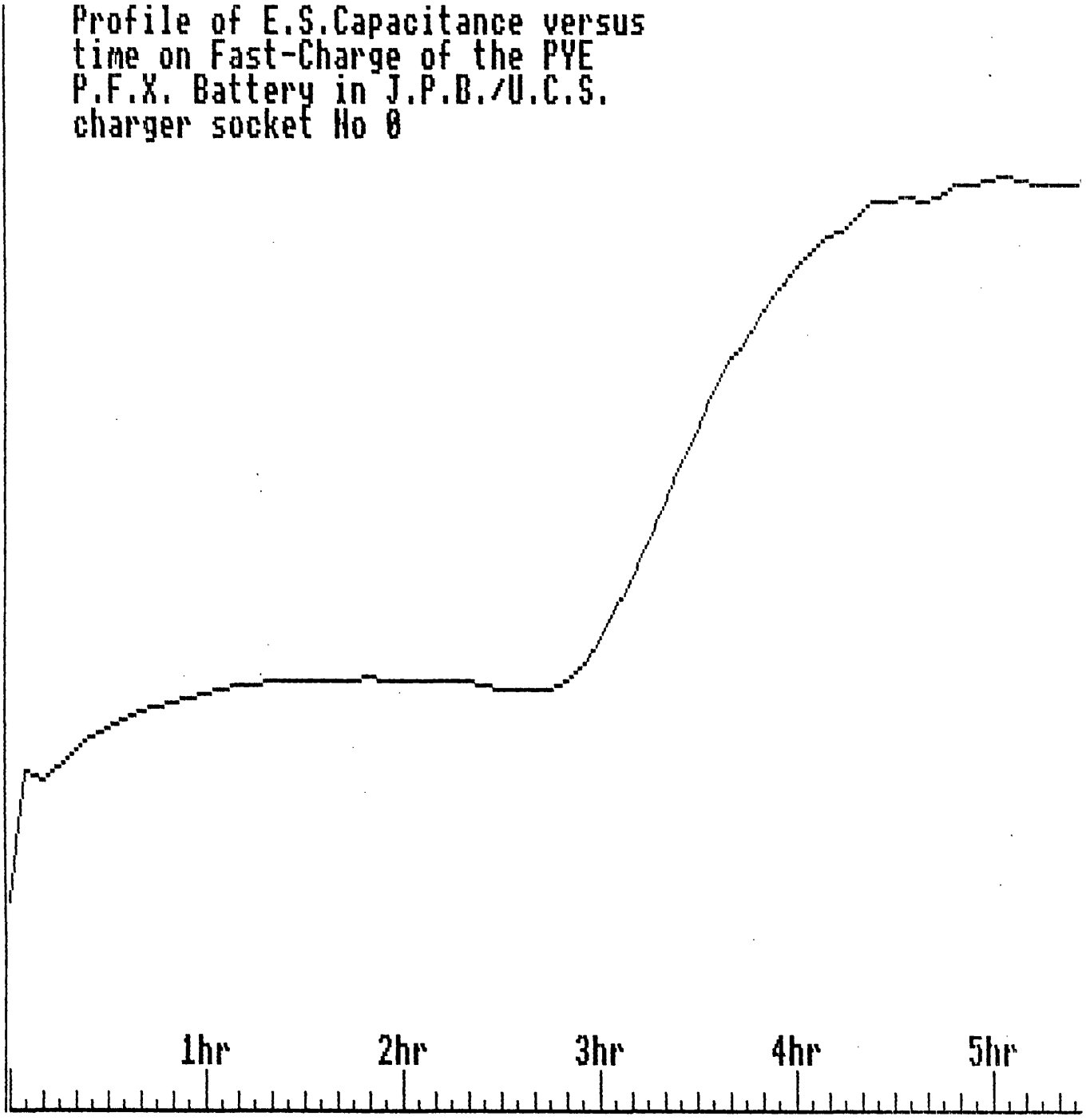
Results for J.P.B./U.C.S.-Charger-RUN 6 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

Graph 103

Result for J.P.B./U.C.S.-Charger-RUN 3 :



Note: The y (E.S.C.) axis is uncalibrated but is constant amongst graphs

APPENDIX 1(a)

Terminology and Definitions Associated with Batteries and Special Measurements (specific to this document and general)

- "Battery" : An electrochemical device for purposes of generating external electrical currents. A rigorous definition of a battery demands that it should contain two or more electrochemical cells but in practice the term is commonly applied to single-cell devices also.
- "Bias" (when used in association with measurements on cells/batteries) : A d.c. current applied in a specified direction during measurement (a definition specific to this document).
- "C" (other than to represent Capacitance) : "C" may be used to represent the nominal capacity of a cell/battery (in milliampere-hours) or, more generally, the quantity of charge equivalent to this capacity (Note that the use of "C" to represent an unquantified capacitance is generally avoided by the Author in this document).
- "Cell" : An electrochemical device comprising a single electrode-electrolyte-electrode unit. Note that in the case of the Ni-Cd system a cell has a nominal terminal voltage of 1.25 volts.
- "Cell Reversal" : A reversal of terminal voltage polarity of an individual cell (possibly within a multi-cell battery) resulting from overdischarge. The magnitude of the reversed voltage depends on the (over)discharge rate and the duration of overdischarge. Note that cell reversal may be extremely damaging to Ni-Cd cells/batteries.
- "Charge" (as in a charging process) : The process of increasing the charge stored in a cell/battery by applying a current into the positive terminal of the battery.

- "Charge Efficiency" : The value (Charge delivered to a cell/battery)/(Charge deliverable from a cell/battery) as measured by giving a cell/battery a charge from a discharged state (defined by means of a specified cutoff on a preceding discharge) followed by a discharge to the specified cutoff. Note that for an initially discharged cell/battery the charge efficiency effectively varies with overcharge factor.
- "Ch-D" : Charge-Discharge (a non-conventional term specific to this document).
- "Cutoff (Voltage)" : A minimum voltage, or voltage-per-cell of a series-multi-cell battery, to which the terminal voltage of a cell/battery may be allowed to fall during a discharge process. Note that for Ni-Cd devices values of 0.8-1.0 volt-per-cell are common.
- "C/X (-rate)" where X = <number> : A charge/discharge rate (in milliamps) obtained by dividing the nominal capacity of the cell/battery (in milliampere-hours) by the number (X) given. Note that the number (X) is equivalent to the nominal period (in hours) for which an initially fully charged cell/battery can deliver a discharge current of the magnitude defined by "C/X".
- "Discharge" : The process of decreasing the charge stored in a cell/battery by extracting a current from the positive terminal of the battery.
- "E.S.C." : The Effective Series Capacitance of an electrical device as measured at its terminals.
- "E.S.Con." : Effective Series Conductance, equivalent to 1/(E.S.R.) (a fairly non-conventional term).
- "E.S.R" : The Effective Series Resistance of an electrical device as measured at its terminals.
- "Full Charge/Fully Charged" : These descriptive terms relating to the charge state of a battery are open to a degree of interpretation. However,

a sensible interpretation is as follows: a cell/battery can be described as having reached full charge or being fully charged when it has received sufficient charging such that continued charging would not cause an appreciable increase in the charge extractable from that cell/battery upon a test discharge to a predetermined cutoff voltage.

- "Life Expectancy/Lifetime (of Cell/Battery)" : The (expected or average or true, as appropriate) working lifetime of a cell/battery. Lifetime may be expressed in terms of number of charge-discharge cycles or in terms of time periods (usually years). In practice, definitions of lifetime vary since cells/batteries have several failure modes and since tolerance of faults is generally application-dependent. In a general sense, a cell/battery is said to have reached the end of its life when it fails to perform to a specified satisfactory degree in its intended application. To take a simple case, a battery might be considered to have reached the end of its life when its charge-storing capacity has fallen to 75% of its nominal value.

- "Memory Effect" : A popular name for a form of reversible loss of usable cell/battery capacity arising from repeated non-full discharges of a cell/battery. The effect usually manifests itself not as a loss of total coulombic capacity but as a depression of cell/battery terminal voltage (possibly to below useful levels) during the latter part of discharge.

- "Nominal Capacity" : The nominal charge-storing capacity (usually given in milliampere-hours) of a cell/battery as specified by its manufacturer.

- "Overcharge" : The process of passing charge through a cell/battery in the charge direction additional to the "C"-quantity charge needed to fully charge an ideal (i.e. 100% efficient/reversible) cell/battery. Since Ni-Cd devices are not ideal then some degree of overcharge is necessary to achieve full charging. Greatly extended overcharge, however, does not contribute significantly to the charge stored in a cell/battery. In

practice, if a cell is subjected to a complicated charge-discharge regime then occurrences of overcharge are not always easy to predict theoretically though can often be identified by means of experimental observations.

- "Overcharge Factor" : The value ((Charge given to a cell/battery) DIVIDED BY (Nominal capacity of the cell/battery)) expressed either as percentage or a fraction. Note that a charge at a C/10 rate with a 1.4-1.6 (140%-160%) overcharge factor is a typical "standard" charge for Ni-Cd cells/batteries.

- "Overdischarge" : The process of passing charge through a cell/battery in the discharge direction additional to that required to discharge the battery to a specified cutoff. On overdischarge the terminal voltage of a cell/battery will continue to fall and will eventually pass through zero and reverse in polarity.

- "Reversible Capacity Loss" : A reduction (perhaps serious) of usable cell/battery charge-storing capacity which is capable of being reversed by means of special processing of the cell/battery.

- "Second Plateau" : The depressed terminal voltage plateau present during the latter part of discharge of cells/batteries suffering the memory effect.

- (n^{th}-Harmonic-)"Transcapacitance" : (see Appendix 2) (a non-conventional term specific to this document).

- (n^{th}-Harmonic-)"Transconductance" : (see Appendix 2) (a non-conventional term specific to this document).

- "True Capacity" : The true charge-storing capacity of an individual cell/battery as measured for that particular battery under specified conditions. Typical conditions for Ni-Cd devices involve a discharge at the C/5 rate to a 1-volt-per-cell cutoff.

- "+Ve (direction) current" : In this document a current through a

cell/battery is defined as being positive if it is in the charge direction (This is contrary to convention and arises since the Author chose to consider currents from the viewpoint of current-generating hardware rather than from the viewpoint of cells/batteries).

- "-Ve (direction) current" : In this document a current through a cell/battery is defined as being negative if it is in the discharge direction (This is contrary to convention and arises since the Author chose to consider currents from the viewpoint of current-generating hardware rather than from the viewpoint of cells/batteries).

APPENDIX 1(b)

Abbreviations Used in This Document

- A : Amp(ere)
- a.c. (or A.C.) : alternating current
- A.D.A.M. : Analogue Data Acquisition Module
- A.D.C. : Analogue-to-Digital Converter
- AF : Amplitude-Factor
- Ah : Ampere-hour
- A-to-D : Analogue-to-Digital
- B.B.C. : British Broadcasting Corporation
- ^{o}C : degree Centigrade
- Ch-D : Charge-Discharge
- CMOS : Complementary Metal Oxide Semiconductor
- CPB : Cell-Programming-Byte
- DAC : Digital-to-Analogue Converter
- dB : decibel
- d.c. (or D.C.) : direct current
- d.o.d. : depth-of-discharge
- D.P.D.T. : Double-Pole-Double-Throw
- D-to-A : Digital-to-Analogue
- e.m.f. : electromotive force
- EPROM : Erasable Programmable Read-Only Memory
- E.S.C. : Effective Series Capacitance
- E.S.Con. : Effective Series Conductance
- E.S.R. : Effective Series Resistance
- F : Farad
- ^{o}F : degree Fahrenheit

- F.E.T. : Field Effect Transistor
- f.s.d. : full-scale deflection
- FSF : Frequency-Setting-Factor
- g.r.p. : glass-(fibre-)reinforced plastic
- H : Henry
- hr : hour
- Hz : Hertz
- i.c. : integrated circuit
- J.P.B. : (Author's initials)
- g : gram
- l.e.d. : light-emitting diode
- LSB : Least Significant Bit
- MOSFET : Metal Oxide Semiconductor Field Effect Transistor
- MSB : Most Significant Bit
- Ni-Cd : Nickel-Cadmium
- op-amp : operational-amplifier
- Pa : Pascal
- p.c.b. : printed circuit board
- p.p.m. : part(s) per million
- p.s.d. : phase-sensitive detection
- p.s.i. : pounds per square inch
- R.A.M. or RAM : Random-Access Memory
- R.O.M. or ROM : Read-Only Memory
- s : second
- S : Siemen
- S.P.S.T. : Single-Pole-Single-Throw
- tempco : temperature coefficient (usually of resistance)
- U.C.S. : University College (of) Swansea
- U.S.A. : United States of America

- U.K. : United Kingdom
- V : Volt
- +ve : positive
- -ve : negative
- V-I : Voltage-to-Current
- Wh : Watt-hour
- Ω : Ohm

APPENDIX 2

Important Aspects of the Theory of a Simple Current-Excitation Complex Impedance Meter Based on Phase-Sensitive Detection Techniques

Consider an arbitrary two-terminal electrical device (described hereafter as the "D(evice).-U(nder).-T(est)." and quite possibly an electrochemical cell/battery) upon which complex a.c. impedance measurements are to be done then, regardless of the nature of component parts and their connections internal to the D.U.T., at any chosen measurement frequency the D.U.T. will display a complex impedance which can be split into a real (resistive) component and an imaginary (reactive) component. Depending on the sign of the reactive part of impedance, the D.U.T. may exhibit inductive or capacitive behaviour. For convenience, (and particularly since Nickel-Cadmium cells/batteries generally exhibit capacitive reactance at useful measurement frequencies) any reactance of the D.U.T. will be described in this discussion in terms of a capacitance. If, at a selected frequency a well-defined sinewave current is passed through the D.U.T. (by external means) then a sinusoidal voltage will be developed across it in accordance with the complex form of Ohm's law ...

$$V_t = I_t(R - j/(\omega C))$$

where: t represents time

: ω = excitation/measurement angular frequency (equal to $2\pi f$ where f is frequency)

: R = effective-series-resistance of D.U.T.

: C = effective-series-capacitance of D.U.T.

Let the D.U.T. be excited with a waveform ...

$$I_t = I_{pk} \sin(\omega t)$$

where: t represents time

: I_{pk} = peak value of I_t

then the response voltage is of the form ...

$$V_t = I_{pk}\{R \sin(\omega t) - (1/\omega C)\cos(\omega t)\}$$

such that the resistive part of D.U.T. impedance generates a component of response voltage in phase with the excitation current sinewave and the capacitive part of D.U.T. impedance generates a component of response voltage in quadrature with the excitation current sinewave.

The method of impedance-component measurement by phase-sensitive detection involves multiplying the response signal (a voltage in this case) by a waveform of defined shape which is of the same frequency as the excitation signal (a current in this case) and of a defined phase relation to it. The resulting product signal is then integrated over a defined number of cycles of the excitation signal. The simplest method (used by the Author) involves multiplying the response voltage by a square-wave. It can easily be shown (analytically or graphically) that by multiplying the response voltage by a square-wave in phase with the excitation signal and integrating over a time period corresponding to an integer number of waveform cycles then a result is obtained which is proportional to the real part only of D.U.T. impedance. Similarly, by multiplying the response voltage by a square-wave in quadrature with the excitation signal and integrating over a time period corresponding to an integer number of waveform cycles then a result is obtained which is proportional to the imaginary part only of D.U.T. impedance. Subsequent to these integrations, by considering the value of I_{pk} and the number of waveform cycles over which the integrations were performed then the values of R and $(1/\omega C)$ (and hence C since f is known) can be calculated. It should be noted that any constant d.c. component in the response signal is totally ignored by a phase-sensitive detection/integration process since the integral of its

product with any symmetrical a.c. waveform over an integer number of cycles of the waveform will always be zero.

The above case considers sinewave excitation combined with a square-wave multiplication signal (which were used in the Author's apparatus) and considers the D.U.T. to behave in a linear manner such that the response signal is a true sinewave. The D.U.T. may exhibit a degree of nonlinearity (most electrochemical devices do) such that some response voltage may appear in the form of harmonics of the excitation frequency. It should be noted that a phase-sensitive-detection process involving square-wave multiplication is sensitive, though to a reduced degree compared with the fundamental, to odd harmonic components in the response voltage. It can easily be shown that the sensitivity to the third harmonic is a third of that of the to the fundamental, that the sensitivity to the fifth harmonic is a fifth of that to the fundamental, and so on. However, provided that the nonlinearity of the D.U.T. is relatively small then reasonably accurate impedance component measurements may be made using the square-wave multiplication method (An alternative method involving multiplication by a sinewave eliminates sensitivity to harmonics but is more difficult to implement.

The phase-sensitive-detection method may be used to explicitly investigate any harmonic response component by multiplying the response signal with quadrature square-waves at the frequency of the harmonic being investigated. Integration of the products over an integer number of cycles of the fundamental leads to values proportional to the in-phase-harmonic and quadrature-phase-harmonic components of harmonic-component response. These values may subsequently be used to quantitatively define parameters of the D.U.T., in a manner analagous to the definitions of effective-series-resistance and effective-series-capacitance, that give a measure of the degree of nonlinearity of the D.U.T. These parameters could, perhaps,

be called the n^{th}-Harmonic-"Transconductance" and n^{th}-Harmonic-"Transcapacitance" where n is the number of the harmonic involved.

APPENDIX 3

A Discussion of Sine-Burst Measurements as Applied to Real Cells/Batteries Rather Than to Series-RC Battery Models

For simplicity the Author has often considered cells/batteries to be modellable at any given measurement frequency for purposes of a.c. measurements (with d.c. aspects of behaviour ignored) as a series R-C combination. If a measurement is done on such a cell/battery using techniques involving continuous sinewave excitation (current or voltage) at a defined frequency then the exact nature of R-C networks within the cell/battery is immaterial. A cell/battery subject to continuous excitation can generally be regarded as being in an a.c.-steady-state condition and by applying phase-sensitive-detection/integration over an integer number of cycles of the excitation waveform then the effective impedance components of the cell/battery may be measured accurately. However, in practice, the Author was forced by timing considerations to excite cells/batteries for each measurement by a well-defined burst of sinewave current with current prior to and post to the burst being defined as zero. Furthermore, the phase-sensitive integration was carried out over the same period as the excitation burst with no time explicitly allowed for an a.c.-steady-state condition to be reached. If a cell/battery under test has, in reality characteristics of a parallel-R-C combination then these circumstances can cause problems relating to the validity of measurement results.

The cases of the application of sine-burst measurements to series-R-C and parallel-R-C two-terminal combinations will be treated separately as follows. It should be remembered that a high quality current generator

(such as was used by the Author to produce excitation current sinewaves) has an extremely high output impedance and that the current-generator is assumed to produce a sinewave with no d.c.-current offset.

Considering the case of a cell/battery behaving as a true series-R-C combination, only one loop (the generator, R and C in a series loop) is involved in the measurement-setup network and since the current generator may be regarded as having an effectively infinite impedance then the time-constant of the generator-R-C loop is effectively infinite. Consequently, the average d.c. voltage across the capacitor prior to excitation is undefined and if the introduction of an excitation waveform causes a perturbation in the average d.c. voltage across the capacitor then the perturbation will not decay but will persist for the duration of the excitation.

Considering the case of a cell/battery behaving as a true parallel-R-C combination, only two nodes are involved in the measurement-setup network (the generator, R and C all effectively in parallel) and the network has an obvious time constant of RC. Provided that the cell/battery has not been subject to excitation waveforms for a sufficient time then the average d.c. voltage across the capacitor (and other components) prior to excitation can be regarded as being zero. If, as is possible, the introduction of an excitation current waveform to the parallel-R-C device causes an initial perturbation in the average d.c. voltage across the capacitor (and other components) then the perturbation will decay exponentially with time at a rate determined by the product RC. This exponential component will appear as a component in the response voltage. It can be shown easily (very easily graphically) that an exponential response component is not ignored by the phase-sensitive detection process and will cause errors in results.

As a simple proof that the introduction of a sinewave excitation

signal to a two-terminal R-C combination (series or parallel) may cause an initial perturbation in the average d.c. across the capacitive element (and hence across the terminals of the combination), consider the R-C combination to be excited with a continuous sinewave current and let the average d.c. voltage across the two terminals be zero. Using exponential notation, if the excitation current is of form ...

$$I_t = I_{pk}\, e^{j(\omega t+\alpha)}$$

where: t represents time

: ω = angular frequency (equal to $2\pi f$ where f is frequency)

: α is an absolute phase angle

then the response voltage will be of form ...

$$V_t = I_{pk}.Z\, e^{j(\omega t+\alpha+\phi)}$$

where: Z = impedance (magnitude) of R-C combination

: ϕ = (constant) phase angle between voltage and current.

It can be seen that for each value of I_t there exists a distinct value of V_t and that if t=0 is regarded as an origin (with excitation having begun at negative values of t such that a.c.-steady-state conditions exist at t=0) then ...

(a) $I_0 = I_{pk}\, e^{j(\alpha)}$, $V_0 = I_{pk}.Ze^{j(\alpha+\phi)}$

where the subscript 0 indicates t=0.

Suppose now that the two-terminal R-C combination is excited by a burst of sinewave current commencing at t=0 and having (starting) phase factor Θ. If the value of Θ is such that at t=0 the conditions (a) exist then at times t>0 then the situation existing will be indistinguishable from the continuous-excitation case. If however, Θ is not specially selected then the value of the starting voltage (V_0) across the R-C

combination will generally not be appropriate to the value of the starting current (I_0). If the R-C combination is regarded as having linear behaviour then the voltage discrepancy may be regarded as an additive voltage term and as such represents a shift in the average d.c. voltage across the R-C combination. If in the burst-excitation case the voltage across the terminals of the R-C combination prior to excitation is constrained to zero (which is generally realistic) then ...

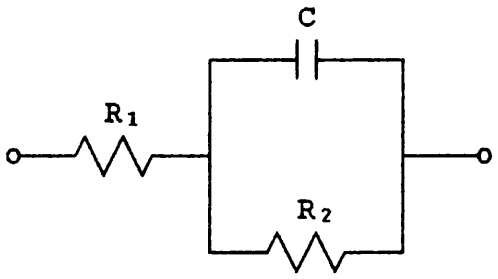
$$(V_0=0) = I_{pk}.Ze^{j(\Theta-\phi)} + V_{offset} : (t=0)$$

so that ...

$$V_{offset(t=0)} = I_{pk}.Ze^{j(\Theta-\phi)} : (t=0)$$

It is obvious in the above case that V_{offset} at (t=0) is zero only if $\Theta = \phi$. A practical measurement strategy may require that Θ be fixed in which case V_{offset} will generally be non-zero (In the case of the Author's measurements a value Θ=0 was used to eliminate high current slew rates).

A more rigorous treatment involves solving differential equations for the two-terminal series-parallel R-C-R network shown below.



It can be calculated that for the case of sine-burst excitation where I_t = 0 AND V_t = 0 prior to excitation AND if α = 0 then solutions for V_t:(t>=0) exist in special cases as follows:-

If R_2 = infinite then ...

$$V_t = I_t.Ze^{j(\omega t+\phi)} + V_{offset}$$

where: V_{offset} = constant

If $R_1 = 0$ then ...

$$V_t = I_t.Ze^{j(\omega t+\phi)} + V_{offset}.e^{-(t/R_1C)}$$

where: V_{offset} = constant

In both of the above special cases the value of V_{offset} is calculable if R_x and C are known.

In the case of the pure-series R-C combination the offset persists indefinitely whilst in the case of the pure-parallel combination the offset decays with time. It can be shown easily that in the pure-series case the creation of an average d.c. voltage offset may result in inefficient usage of the input voltage range of a practical detector.

For the pure-parallel case the introduction of an exponential (transient) term interferes with a phase-sensitive detection process and a value calculated for C via such a method will have some dependence on the value of R_1. Furthermore, if the parallel-R-C combination is not in a true steady-state condition at the onset of excitation (i.e. if not $V_0 = 0$) then the values calculated for both C and R_1 may be influenced.

In reality, an electrochemical cell/battery displays a combination of series-R-C and parallel-R-C characteristics. A rigorous treatment of cells/batteries is made very difficult since a multitude of electrochemical time constants are effectively present and since nonlinear (probably 'lopsided') behaviour is quite possible, especially in situations where d.c. currents have been in use prior to measurements. The inexactitudes of measurement methods using burst-excitation should be borne in mind but provided that transient effects are limited in magnitude and measurements waveforms are well-defined then the method should still provide useful information in a repeatable manner. It should be noted that

consecutive measurements on a single cell/battery may interact to a degree by means of perturbing voltage levels involved in internal equivalent R-C networks.

APPENDIX 4(a)

Usage of B.B.C. Microcomputer Memory

In zero-page, memory is allocated (within a block 0070-008F reserved for the user by B.B.C. BASIC II) as follows:-

- 0070-0077 (8 bytes) - Machine-code workspace
- 0078-007F (8 bytes) - (unused)
- 0080-0084 (5 bytes) - Machine-code workspace
- 0085-0087 (3 bytes) - (unused)
- 0088-008B (4 bytes) - Machine-code workspace

Program memory is as follows ("PAGE" is a machine-dependent pseudovariable, generally 0E00 or 1900) :-

- PAGE-62FF (variable) - BASIC programs

In memory reserved by the user between program and screen memory, allocations are as follows:-

- 6300-69FF (1.75kbyte) - Machine-code routines
- 6A00-6A17 (24 bytes) - "FSF" table "0"
- 6A18-6A2F (24 bytes) - "FSF" table "1"
- 6A30-6A47 (24 bytes) - "FSF" table "2"
- 6A47-6A5F (24 bytes) - "FSF" table "3"
- 6A60-6A77 (24 bytes) - "AF" table "0"
- 6A78-6A8F (24 bytes) - "AF" table "1"
- 6A90-6AA7 (24 bytes) - "AF" table "2"
- 6AA8-6ABF (24 bytes) - "AF" table "3"
- 6AC0-6AEF (48 bytes) - "CTF" table
- 6AF0-6AFF (16 bytes) - (unused)

- 6B00-6B2F (48 bytes) - "CPB" table

- 6B30-6B5F (48 bytes) - "PCR" table

- 6B60-6BEF (144 bytes) - "Compacted-Sinewave" table

- 6BF0-6BF7 (8 bytes) - p.s.d. results

- 6BF8 (1 byte) - Sinegenerator (latch) programming byte

- 6BF9 (1 byte) - Detector (latch) programming byte

- 6BFA,6BFB (2 bytes) - (D.c.)-Nulling-DAC programming byte

- 6BFC,6BFD (2 bytes) - "autonul" (routine) result

- 6BFE,6BFF (2 bytes) - (unused)

- 6C00-73FF (2048bytes) - "Low-Byte-Sinewave" table

- 7400-7BFF (2048bytes) - "High-Byte-Sinewave" table

Computer screen memory (MODE7) is as follows:-

- 7C00-7FE7 (1 kbyte) - MODE7 microcomputer screen memory

In page FC (which is associated with the B.B.C. Microcomputer 1MHz bus), allocations for memory-mapped I/O devices as follows:-

- FC00-FC8F (144 bytes) - (unused)

- FC90-FCEF (96 bytes) - Charge-Discharge modules

- FCF0-FCFB (12 bytes) - Measurement hardware devices

- FCFC,FCFD (2 bytes) - (unused)

- FCFE (1 byte) - Charge-Discharge system reset address

- FCFF (1 byte) - (unused)

APPENDIX 4(b)

A Listing of the 6502 Machine Code

Notes:-

- The listing given is of the B.B.C. BASIC source program for the 6502 machine code. The machine code is contained in assembler mnemonic form between program lines 100 to 8700 inclusive.

```
10REM "C.MC+OS_C"
20
30DIM MC% 1750
40OSBYTE=&FFF4
50FOR opt%=0 TO 3 STEP 3
60P%=MC%
70dest%=&6300
80assemb%=P%:os%=dest%-assemb%
90[
100          OPT opt%
110.dcmeas%  JSR autonul%+os%  <Do d.c. null>
120.oneshot% LDA &6BF9         Load A with Detector-Programming byte
130          AND #&DF          Set BIT3 low
140          TAY               Program Detector latch with result (so
150          LDA #&93          that a conversion is initiated)
160          LDX #251          .
170          JSR OSBYTE        .
180          JSR timlopA%+os%  Wait for conversion to finish
190          LDA #&92          <Put conversion result into (0076,0077)>
200          LDX #243          .
210          JSR OSBYTE        .
220          TYA               .
230          AND #&3F          .
240          STA &77           .
250          LDA #&92          .
260          LDX #242          .
270          JSR OSBYTE        .
280          STY &76           .
290          LDA &6BF9         Load A with Detector-Programming byte
300          ORA #&20          Set BIT3 high
310          TAY               Program Detector latch with result
320          LDA #&93          .
330          LDX #251          .
340          JSR OSBYTE        .
350          RTS               Exit
360         NOP
370         NOP
380.autonul% LDA &6BF9         Load A with Detector-Programming byte
390          AND #&BF          Set BIT2 low (for d.c. mode)
400          ORA #&20          Set BIT3 high
410          STA &6BF9         Store result as new Det-Prog. byte
420          TAY               Program Detector latch with result
430          LDA #&93          .
440          LDX #251          .
450          JSR OSBYTE        .
460          JSR timlopB%+os%  Wait for hardware settling
470          LDA &6BF9         Load A with Detector-Programming byte
480          AND #&DF          Set BIT3 low
490          TAY               Program Detector latch with result (so
500          LDA #&93          that a conversion is initiated)
510          LDX #251          .
520          JSR OSBYTE        .
530          JSR timlopA%+os%  Wait for conversion to finish
540          LDA #&92          <Put conversion result into (6BFC,6BFD)
550          LDX #243          and put result divided by two into
560          JSR OSBYTE        (6BFA,6BFB) and program voltage-nulling
570          TYA               D-to-A converter with result>
580          AND #&3F          .
```

```
 590          STA &6BFD          .
 600          LSR A              .
 610          PHP                .
 620          STA &6BFB          .
 630          TAY                .
 640          LDA #&93           .
 650          LDX #241           .
 660          JSR OSBYTE         .
 670          LDA #&92           .
 680          LDX #242           .
 690          JSR OSBYTE         .
 700          STY &6BFC          .
 710          PLP                .
 720          TYA                .
 730          ROR A              .
 740          STA &6BFA          .
 750          TAY                .
 760          LDA #&93           .
 770          LDX #240           .
 780          JSR OSBYTE         .
 790          LDX #246           .
 800          JSR OSBYTE         .
 810          LDA &6BF9          Load A with Detector-Programming byte
 820          ORA #&20           Set BIT3 high
 830          TAY                Program Detector latch with result
 840          LDA #&93           .
 850          LDX #251           .
 860          JSR OSBYTE         .
 870          JSR timlopB%+os%   Wait for d.c.-voltage-null settling
 880          RTS                Exit
 890        NOP
 900        NOP
 910.acprep%  LDA &6BF9          Load A with Detector-Programming byte
 920          ORA #&40           Set BIT2 high (for a.c. mode)
 930          STA &6BF9          Store result as new Det-Prog. byte
 940          TAY                Program Detector latch with result
 950          LDA #&93           .
 960          LDX #251           .
 970          JSR OSBYTE         .
 980          JSR timlopB%+os%   Wait for Detector reed-relays to settle
 990          RTS                Exit
1000        NOP
1010        NOP
1020.trimdwn% LDA &6BFA         <Take value from (6BFA,6BFB), deduct one,
1030          SEC               put result back in (6BFA,6BFB) and
1040          SBC #1            program voltage-nulling D-to-A converter
1050          PHP               with result>
1060          STA &6BFA         .
1070          TAY               .
1080          LDA #&93          .
1090          LDX #240          .
1100          JSR OSBYTE        .
1110          PLP               .
1120          LDA &6BFB         .
1130          SBC #0            .
1140          STA &6BFB         .
1150          TAY               .
1160          LDA #&93          .
```

```
1170          LDX #241          .
1180          JSR OSBYTE        .
1190          LDX #246          .
1200          JSR OSBYTE        .
1210          JSR timlopB%+os%  Wait for d.c.-voltage-null settling
1220          RTS               Exit
1230         NOP
1240.trimup%  LDA &6BFA         <Take value from (6BFA,6BFB), add one,
1250          CLC               put result back in (6BFA,6BFB) and
1260          ADC #1            program voltage-nulling D-to-A converter
1270          PHP               with result>
1280          STA &6BFA         .
1290          TAY               .
1300          LDA #&93          .
1310          LDX #240          .
1320          JSR OSBYTE        .
1330          PLP               .
1340          LDA &6BFB         .
1350          ADC #0            .
1360          STA &6BFB         .
1370          TAY               .
1380          LDA #&93          .
1390          LDX #241          .
1400          JSR OSBYTE        .
1410          LDX #246          .
1420          JSR OSBYTE        .
1430          JSR timlopB%+os%  Wait for d.c.-voltage-null settling
1440          RTS               Exit
1450         NOP
1460         NOP
1470.timlopA% LDY #0            <Wait approx. 100 microseconds (via a
1480.back1%   CPY #22           mechanism involving a software counter)>
1490          BEQ exit1%        .
1500          INY               .
1510          JMP back1%+os%    .
1520.exit1%   RTS               Exit
1530         NOP
1540         NOP
1550.timlopB% LDX #0            <Wait approx. 22 milliseconds (via a
1560.backo1%  LDY #&0           mechanism involving two nested software
1570.backi1%  CPY #&FF          counters)>
1580          BEQ exi1%         .
1590          INY               .
1600          JMP backi1%+os%   .
1610.exi1%    CPX #18           .
1620          BEQ exo1%         .
1630          INX               .
1640          JMP backo1%+os%   .
1650.exo1%    RTS               Exit
1660         NOP
1670         NOP
1680.acmeas%  LDA #&93          Program Sinegenerator with
1690          LDX #249          Sinegenerator-Programming byte
1700          LDY &6BF8         .
1710          JSR OSBYTE        .
1720          JSR timlopB%+os%  Wait for Sinegen. reed-relays to settle
1730          LDX #250          Trigger Sinegenerator
1740          JSR OSBYTE        .
```

```
1750          LDX #0            <Wait approx. 50 milliseconds (via a
1760.backo3%  LDY #&0           mechanism involving two nested software
1770.backi3%  CPY #&FF          counters)>
1780          BEQ exi3%         .
1790          INY               .
1800          JMP backi3%+os%   .
1810.exi3%    CPX #40           .
1820          BEQ exo3%         .
1830          INX               .
1840          JMP backo3%+os%   .
1850.exo3%    NOP               .
1860.back4%   LDA #&92          Read Hi-byte Bus-Interface
1870          LDX #241          .
1880          JSR OSBYTE        .
1890          TYA               <If BIT7 is low then return to back4%>
1900          ROL A             .
1910          BCC back4%        .
1920          NOP               .
1930          RTS               Exit
1940        NOP
1950        NOP
1960.sinread% LDX #0            <Initialise counters to zero>
1970          STX &82           .
1980          STX &83           .
1990          STX &72           .
2000          STX &71           .
2010          STX &74           .
2020          STX &88           .
2030          STX &8A           .
2040          STX &84           .
2050.Stselct% LDA #&78          <Select and call one of routines St8%,
2060          AND &6BF8         St16%, St32%, St64% according to
2070          STA &75           measurement frequency information held in
2080          LDY #24           BITS2,3,4,5 of the Sinegenerator-
2090          CLC               Programming Byte (6BF8)>
2100          CPY &75           .
2110          BCC jsr8%         .
2120          BEQ jsr16%        .
2130          LDY #8            .
2140          CLC               .
2150          CPY &75           .
2160          BCC jsr32%        .
2170          JSR St64%+os%     .
2180          RTS               Exit
2190.jsr8%    JSR St8%+os%      .
2200          RTS               Alternative Exit
2210.jsr16%   JSR St16%+os%     .
2220          RTS               Alternative Exit
2230.jsr32%   JSR St32%+os%     .
2240          RTS               Alternative Exit
2250        NOP
2260.St8%     STX &70           <Routine reading in 1-cycle format data
2270          STX &72           utilising a call of storehv% for each
2280          LDA #&6C          sample read>
2290          CLC               .
2300          ADC &70           .
2310          STA &89           .
2320          LDA #&74          .
```

```
2330          CLC                .
2340          ADC &70            .
2350          STA &8B            .
2360.loopi8%  LDA #0             .
2370          STA &73            .
2380          JSR storehv%+os%   .
2390          INC &74            .
2400          INC &71            .
2410          BEQ exiti8%        .
2420          JMP loopi8%+os%    .
2430.exiti8%  LDX &70            .
2440          INX                .
2450          CPX #8             .
2460          BEQ exito8%        .
2470          JMP St8%+os%       .
2480.exito8%  RTS                Exit
2490        NOP
2500.St16%    STX &70            <Routine reading in and sorting 2-cycle
2510          STX &72            format data utilising a call of storehv%
2520          LSR &72            for each sample read>
2530          LDA #&6C           .
2540          CLC                .
2550          ADC &70            .
2560          STA &89            .
2570          LDA #&74           .
2580          CLC                .
2590          ADC &70            .
2600          STA &8B            .
2610.loopi16% LDA #0             .
2620          STA &73            .
2630          JSR storehv%+os%   .
2640          INC &71            .
2650          LDA #4             .
2660          STA &73            .
2670          JSR storehv%+os%   .
2680          INC &74            .
2690          INC &71            .
2700          BEQ exiti16%       .
2710          JMP loopi16%+os%   .
2720.exiti16% LDX &70            .
2730          INX                .
2740          CPX #8             .
2750          BEQ exito16%       .
2760          JMP St16%+os%      .
2770.exito16% RTS                Exit
2780        NOP
2790.St32%    STX &70            <Routine reading in and sorting 4-cycle
2800          STX &72            format data utilising a call of storehv%
2810          LSR &72            for each sample read>
2820          LSR &72            .
2830          LDA #&6C           .
2840          CLC                .
2850          ADC &70            .
2860          STA &89            .
2870          LDA #&74           .
2880          CLC                .
2890          ADC &70            .
2900          STA &8B            .
```

```
2910.loopi32% LDA #0            .
2920          STA &73           .
2930          JSR storehv%+os%  .
2940          INC &71           .
2950          LDA #2            .
2960          STA &73           .
2970          JSR storehv%+os%  .
2980          INC &71           .
2990          LDA #4            .
3000          STA &73           .
3010          JSR storehv%+os%  .
3020          INC &71           .
3030          LDA #6            .
3040          STA &73           .
3050          JSR storehv%+os%  .
3060          INC &74           .
3070          INC &71           .
3080          BEQ exiti32%      .
3090          JMP loopi32%+os%  .
3100.exiti32% LDX &70           .
3110          INX               .
3120          CPX #8            .
3130          BEQ exito32%      .
3140          JMP St32%+os%     .
3150.exito32% RTS               Exit
3160         NOP
3170.St64%    STX &70           <Routine reading in and sorting 8-cycle
3180          LDA #&6C          format data utilising a call of storehv%
3190          CLC               for each sample read>
3200          ADC &70           .
3210          STA &89           .
3220          LDA #&74          .
3230          CLC               .
3240          ADC &70           .
3250          STA &8B           .
3260.loopi64% LDA #0            .
3270          STA &73           .
3280          JSR storehv%+os%  .
3290          INC &71           .
3300          LDA #1            .
3310          STA &73           .
3320          JSR storehv%+os%  .
3330          INC &71           .
3340          LDA #2            .
3350          STA &73           .
3360          JSR storehv%+os%  .
3370          INC &71           .
3380          LDA #3            .
3390          STA &73           .
3400          JSR storehv%+os%  .
3410          INC &71           .
3420          LDA #4            .
3430          STA &73           .
3440          JSR storehv%+os%  .
3450          INC &71           .
3460          LDA #5            .
3470          STA &73           .
3480          JSR storehv%+os%  .
```

```
3490          INC &71           .
3500          LDA #6            .
3510          STA &73           .
3520          JSR storehv%+os%  .
3530          INC &71           .
3540          LDA #7            .
3550          STA &73           .
3560          JSR storehv%+os%  .
3570          INC &74           .
3580          INC &71           .
3590          BEQ exiti64%      .
3600          JMP loopi64%+os%  .
3610.exiti64% LDX &70           .
3620          INX               .
3630          CPX #8            .
3640          BEQ exito64%      .
3650          JMP St64%+os%     .
3660.exito64% RTS               Exit
3670        NOP
3680.storehv% LDA &72           <Calculate hardware address for sample to
3690          CLC               be read from external R.A.M. and program
3700          ADC &73           RAM-Address counter accordingly>
3710          TAY               .
3720          LDA #&93          .
3730          LDX #248          .
3740          JSR OSBYTE        .
3750          LDY &74           .
3760          LDX #247          .
3770          JSR OSBYTE        .
3780          LDA #&92          Read sample hi-byte from external R.A.M.
3790          LDX #245          .
3800          JSR OSBYTE        .
3810          TYA               Mask out redundant bits BITS1,2
3820          AND #&3F          .
3830          STA &81           Store result in 0081
3840          LDY &71           Store result also in a selected location
3850          STA (&8A),Y       of the hi-byte Primary-Sinewave table
3860          LDA #&92          Read sample lo-byte from external R.A.M.
3870          LDX #244          .
3880          JSR OSBYTE        .
3890          STY &80           Store value in 0080
3900          TYA               Store result also in a selected location
3910          LDY &71           of the lo-byte Primary-Sinewave table
3920          STA (&88),Y       .
3930          CLC               <Compare contents of (0080,0081) with
3940          LDA &81           contents of (0082,0083). If greater then
3950          CMP &83           replace contents of (0082,0083) with
3960          BCC exitp%        contents of (0080,0081)>
3970          BNE branch%       .
3980          CLC               .
3990          LDA &80           .
4000          CMP &82           .
4010          BCC exitp%        .
4020          BEQ exitp%        .
4030.branch%  LDA &81           .
4040          STA &83           .
4050          LDA &80           .
4060          STA &82           .
```

```
4070.exitp%   LDA &81            <Compare contents of (0080,0081) with
4080          CMP #0             zero. If equal then set contents of 0084
4090          BNE exitp2%        to 1>
4100          LDA &80            .
4110          CMP #0             .
4120          BNE exitp2%        .
4130          LDA #1             .
4140          STA &84            .
4150.exitp2%  RTS                Exit
4160         NOP
4170         NOP
4180.compact% JSR clrcomp%+os%   <Clear Compacted-Sinewave table>
4190.xcompct% STA &88            Do further initialisations
4200          STA &8A            .
4210          STA &71            .
4220          STA &73            .
4230.loopoc%  STA &70            <Code converting data from raw format in
4240          JSR pagcalc%+os%   the Primary-Sinewave table to compacted
4250.bacc1%   JSR adstor%+os%    format in the Compacted-Sinewave table
4260          INC &71            utilising calls of pagcalc%, adstor% and
4270          LDY &71            csateX%>
4280          CPY #43            .
4290          BNE bacc1%         .
4300          JSR csateA%+os%    .
4310          INC &73            .
4320          INC &73            .
4330          INC &73            .
4340.bacc2%   JSR adstor%+os%    .
4350          INC &71            .
4360          LDY &71            .
4370          CPY #85            .
4380          BNE bacc2%         .
4390          JSR csateB%+os%    .
4400          INC &73            .
4410          INC &73            .
4420          INC &73            .
4430.bacc3%   JSR adstor%+os%    .
4440          INC &71            .
4450          LDY &71            .
4460          CPY #128           .
4470          BNE bacc3%         .
4480          INC &73            .
4490          INC &73            .
4500          INC &73            .
4510.bacc4%   JSR adstor%+os%    .
4520          INC &71            .
4530          LDY &71            .
4540          CPY #171           .
4550          BNE bacc4%         .
4560          JSR csateA%+os%    .
4570          INC &73            .
4580          INC &73            .
4590          INC &73            .
4600.bacc5%   JSR adstor%+os%    .
4610          INC &71            .
4620          LDY &71            .
4630          CPY #213           .
4640          BNE bacc5%         .
```

```
4650          JSR csateB%+os%   .
4660          INC &73           .
4670          INC &73           .
4680          INC &73           .
4690.bacc6%   JSR adstor%+os%   .
4700          INC &71           .
4710          LDY &71           .
4720          BNE bacc6%        .
4730          INC &73           .
4740          INC &73           .
4750          INC &73           .
4760          INC &70           .
4770          LDA &70           .
4780          CMP #8            .
4790          BNE loopoc%       .
4800          RTS               Exit
4810         NOP
4820.clrcomp% LDY #0            <Routine clearing the Compacted-Sinewave
4830          TYA               table>
4840.back3%   STA &6B60,Y       .
4850          INY               .
4860          CPY #144          .
4870          BNE back3%        .
4880          RTS               Exit
4890         NOP
4900.pagcalc% LDA #&6C          <Routine calculating page numbers for
4910          CLC               use in indirect,Y addressing>
4920          ADC &70           .
4930          STA &89           .
4940          LDA #&74          .
4950          CLC               .
4960          ADC &70           .
4970          STA &8B           .
4980          RTS               Exit
4990         NOP
5000.adstor%  LDA (&8A),Y       <Routine performing an immediate function
5010          TAX               of data transfer and addition utilising
5020          LDA (&88),Y       indirect,Y addressing for data fetch and
5030          LDY &73           storage>
5040          CLC               .
5050          ADC &6B60,Y       .
5060          STA &6B60,Y       .
5070          INY               .
5080          TXA               .
5090          ADC &6B60,Y       .
5100          STA &6B60,Y       .
5110          INY               .
5120          LDA #0            .
5130          ADC &6B60,Y       .
5140          STA &6B60,Y       .
5150          RTS               Exit
5160         NOP
5170.csateA%  LDY &71           <Compensation routine dealing with
5180          LDA (&88),Y       part-samples (using same addressing
5190          STA &80           methods as adstor%)>
5200          LDA (&8A),Y       .
5210          STA &81           .
5220          JSR divSby3%+os%  .
```

```
5230          LDY &73           .
5240          LDA &6B60,Y       .
5250          SEC               .
5260          SBC &74           .
5270          STA &6B60,Y       .
5280          INY               .
5290          LDA &6B60,Y       .
5300          SBC &75           .
5310          STA &6B60,Y       .
5320          INY               .
5330          LDA &6B60,Y       .
5340          SBC #0            .
5350          STA &6B60,Y       .
5360          NOP               .
5370          INY               .
5380          LDA &74           .
5390          CLC               .
5400          ADC &6B60,Y       .
5410          STA &6B60,Y       .
5420          INY               .
5430          LDA &75           .
5440          ADC &6B60,Y       .
5450          STA &6B60,Y       .
5460          INY               .
5470          LDA #0            .
5480          ADC &6B60,Y       .
5490          STA &6B60,Y       .
5500          LDY &71           .
5510          RTS               .
5520        NOP
5530.csateB%  LDY &71           <Compensation routine dealing with
5540          INY               part-samples (using same addressing
5550          LDA (&88),Y       methods as adstor%)>
5560          STA &80           .
5570          LDA (&8A),Y       .
5580          STA &81           .
5590          JSR divSby3%+os%  .
5600          LDY &73           .
5610          LDA &74           .
5620          CLC               .
5630          ADC &6B60,Y       .
5640          STA &6B60,Y       .
5650          INY               .
5660          LDA &75           .
5670          ADC &6B60,Y       .
5680          STA &6B60,Y       .
5690          INY               .
5700          LDA #0            .
5710          ADC &6B60,Y       .
5720          STA &6B60,Y       .
5730          NOP               .
5740          INY               .
5750          LDA &6B60,Y       .
5760          SEC               .
5770          SBC &74           .
5780          STA &6B60,Y       .
5790          INY               .
5800          LDA &6B60,Y       .
```

```
5810          SBC &75           .
5820          STA &6B60,Y       .
5830          INY               .
5840          LDA &6B60,Y       .
5850          SBC #0            .
5860          STA &6B60,Y       .
5870          LDY &71           .
5880          RTS               Exit
5890         NOP
5900.divSby3% LSR &81           <Divide contents of (0080,0081) by 3 and
5910          ROR &80           put result into (0074,0075)>
5920          LSR &81           .
5930          ROR &80           .
5940          LDA &80           .
5950          STA &74           .
5960          LDA &81           .
5970          STA &75           .
5980          LSR &81           .
5990          ROR &80           .
6000          LSR &81           .
6010          ROR &80           .
6020          LDA &80           .
6030          CLC               .
6040          ADC &74           .
6050          STA &74           .
6060          LDA &81           .
6070          ADC &75           .
6080          STA &75           .
6090          LSR &81           .
6100          ROR &80           .
6110          LSR &81           .
6120          ROR &80           .
6130          LDA &80           .
6140          CLC               .
6150          ADC &74           .
6160          STA &74           .
6170          LDA #0            .
6180          ADC &75           .
6190          STA &75           .
6200          LSR &80           .
6210          LSR &80           .
6220          LDA &80           .
6230          CLC               .
6240          ADC &74           .
6250          STA &74           .
6260          LDA #0            .
6270          ADC &75           .
6280          STA &75           .
6290          LSR &80           .
6300          LSR &80           .
6310          LDA &80           .
6320          CLC               .
6330          ADC &74           .
6340          STA &74           .
6350          LDA #0            .
6360          ADC &75           .
6370          STA &75           .
6380          LSR &80           .
```

```
6390          LSR &80           .
6400          LDA &80           .
6410          CLC               .
6420          ADC &74           .
6430          STA &74           .
6440          LDA #0            .
6450          ADC &75           .
6460          STA &75           .
6470          LSR &80           .
6480          LDA &80           .
6490          CLC               .
6500          ADC &74           .
6510          STA &74           .
6520          LDA #0            .
6530          ADC &75           .
6540          STA &75           .
6550          RTS               Exit
6560         NOP
6570         NOP
6580.average% JSR prepint%+os%  Initialise output locations
6590          STA &70           Further initialisation
6600.back5%   JSR tORfR%+os%    Add 1 sample to Real component total
6610          JSR addRorI%+os%  .
6620          INC &70           Increment sample address counter
6630          INC &70           .
6640          INC &70           .
6650          LDA &70           .
6660          CMP #144          If counter value is not equal to 3*48 =
6670          BNE back5%        144 then return to loop start
6680          JSR divby4%+os%   Divide output results by 4
6690          RTS               Exit
6700         NOP
6710         NOP
6720.psdsoft% JSR prepint%+os%  Initialise output locations
6730          STA &70           Further initialisation
6740.phase0%  LDX #0            Initialisation
6750.toPId2%  JSR tORfR%+os%    Add 1 sample to Real component total
6760          JSR addRorI%+os%  .
6770          JSR tORfI%+os%    Subtract 1 sample from Imag. comp. total
6780          JSR subRorI%+os%  .
6790          INC &70           Increment sample address counter
6800          INC &70           .
6810          INC &70           .
6820          INX               Return to "toPId2" loop start if still in
6830          CPX &75           first quadrant
6840          BNE toPId2%       .
6850          LDX #0            Initialisation
6860.toPI%    JSR tORfR%+os%    Add 1 sample to Real component total
6870          JSR addRorI%+os%  .
6880          JSR tORfI%+os%    Add 1 sample to Imag. component total
6890          JSR addRorI%+os%  .
6900          INC &70           Increment sample address counter
6910          INC &70           .
6920          INC &70           .
6930          INX               Return to "toPI%" loop start if still in
6940          CPX &75           second quadrant
6950          BNE toPI%         .
6960          LDX #0            Initialisation
```

```
6970.to3PId2% JSR tORfR%+os%    Subtract 1 sample from Real comp. total
6980          JSR subRorI%+os%  .
6990          JSR tORfI%+os%    Add 1 sample to Imag. component total
7000          JSR addRorI%+os%  .
7010          INC &70           Increment sample address counter
7020          INC &70           .
7030          INC &70           .
7040          INX               Return to "to3PId2%" loop start if still
7050          CPX &75           in third quadrant
7060          BNE to3PId2%      .
7070          LDX #0            Initialisation
7080.to2PI%   JSR tORfR%+os%    Subtract 1 sample from Real comp. total
7090          JSR subRorI%+os%  .
7100          JSR tORfI%+os%    Subtract 1 sample from Imag. comp. total
7110          JSR subRorI%+os%  .
7120          INC &70           Increment sample address counter
7130          INC &70           .
7140          INC &70           .
7150          INX               Return to "toPI%" loop start if still in
7160          CPX &75           fourth quadrant
7170          BNE to2PI%        .
7180          LDA &70           Return to "phase0%" loop start if last
7190          CMP #144          sample not reached
7200          BNE phase0%       .
7210          JSR divby4%+os%   Divide output results by four
7220          RTS               Exit
7230         NOP
7240.divby4%  LSR &6BF3         <Divide contents of (6BF0-6BF3) by 4>
7250          ROR &6BF2         .
7260          ROR &6BF1         .
7270          ROR &6BF0         .
7280          LSR &6BF7         .
7290          ROR &6BF6         .
7300          ROR &6BF5         .
7310          ROR &6BF4         .
7320          LSR &6BF3         .
7330          ROR &6BF2         .
7340          ROR &6BF1         .
7350          ROR &6BF0         .
7360          LSR &6BF7         .
7370          ROR &6BF6         .
7380          ROR &6BF5         .
7390          ROR &6BF4         .
7400          RTS               Exit
7410         NOP
7420.tORfR%    LDA #&F0         <Initialisation routine>
7430          STA &8A           .
7440          RTS               Exit
7450         NOP
7460.tORfI%    LDA #&F4         <Initialisation routine>
7470          STA &8A           .
7480          RTS               Exit
7490         NOP
7500.addRorI% LDY &70           <Addition routine for 3-byte samples>
7510          LDA (&88),Y       .
7520          STY &71           .
7530          LDY #0            .
7540          CLC               .
```

```
7550          ADC (&8A),Y       .
7560          STA (&8A),Y       .
7570          LDY &71           .
7580          INY               .
7590          LDA (&88),Y       .
7600          STY &71           .
7610          LDY #1            .
7620          ADC (&8A),Y       .
7630          STA (&8A),Y       .
7640          LDY &71           .
7650          INY               .
7660          LDA (&88),Y       .
7670          LDY #2            .
7680          ADC (&8A),Y       .
7690          STA (&8A),Y       .
7700          LDA #0            .
7710          LDY #3            .
7720          ADC (&8A),Y       .
7730          STA (&8A),Y       .
7740          RTS               Exit
7750        NOP
7760.subRorI% LDY #0            <Subtraction routine for 3-byte samples>
7770          LDA (&8A),Y       .
7780          LDY &70           .
7790          SEC               .
7800          SBC (&88),Y       .
7810          STY &71           .
7820          LDY #0            .
7830          STA (&8A),Y       .
7840          LDY #1            .
7850          LDA (&8A),Y       .
7860          LDY &71           .
7870          INY               .
7880          SBC (&88),Y       .
7890          STY &71           .
7900          LDY #1            .
7910          STA (&8A),Y       .
7920          LDY #2            .
7930          LDA (&8A),Y       .
7940          LDY &71           .
7950          INY               .
7960          SBC (&88),Y       .
7970          LDY #2            .
7980          STA (&8A),Y       .
7990          LDY #3            .
8000          LDA (&8A),Y       .
8010          SBC #0            .
8020          STA (&8A),Y       .
8030          RTS               Exit.
8040        NOP
8050.prepint% LDA #&60          <Initialisation routine>
8060          STA &88           .
8070          LDA #&6B          .
8080          STA &89           .
8090          STA &8B           .
8100          LDA #2            .
8110          STA &6BF3         .
8120          STA &6BF7         .
```

```
8130          LDA #0              .
8140          STA &6BF0           .
8150          STA &6BF1           .
8160          STA &6BF2           .
8170          STA &6BF4           .
8180          STA &6BF5           .
8190          STA &6BF6           .
8200          RTS                 Exit
8210         NOP
8220         NOP
8230.busline% LDA &70             <Routine calculating a Charge-Discharge
8240          AND #&F8            module hardware address offset. Module
8250          ASL A               number is supplied via 0070 and
8260          STA &71             calculated address offset is put into
8270          LDA &70             0071>
8280          AND #&3             .
8290          ASL A               .
8300          ASL A               .
8310          CLC                 .
8320          ADC &71             .
8330          STA &71             .
8340          LDA &70             .
8350          AND #&4             .
8360          LSR A               .
8370          LSR A               .
8380          CLC                 .
8390          ADC &71             .
8400          STA &71             .
8410          RTS                 Exit
8420         NOP
8430         NOP
8440.access%  JSR busline%+os%    Calculate address offset of Ch-D module
8450          LDA &71             Add 146 decimal (base address) to address
8460          CLC                 offset
8470          ADC #146            .
8480          STA &71             Put result in 0071 (optional)
8490          TAX                 Write arbitrary value to calculated
8500          LDA #&93            address (to close 4-pole relay of
8510          JSR OSBYTE          selected Ch-D module).
8520          RTS                 Exit
8530         NOP
8540         NOP
8550.delatch% LDX #254            Write arbitrary value to hardware Reset
8560          LDA #&93            address (to reset hardware)
8570          JSR OSBYTE          .
8580          RTS                 .
8590         NOP
8600         NOP
8610.chdpro%  JSR busline%+os%    Calculate address offset of Ch-D module
8620          LDA &71             Add 144 decimal (base address) to address
8630          CLC                 offset
8640          ADC #144            .
8650          STA &71             Put result in 0071 (optional)
8660          TAX                 Write contents of 0075 to calculated
8670          LDY &75             address (to program selected Ch-D module
8680          LDA #&93            for output current)
8690          JSR OSBYTE          .
8700.rts%     RTS                 Exit
```

```
 8710]
 8720NEXT
 8730asendpll%=P%
 8740PRINT "dcmeas% ] &";~dcmeas%+os%
 8750PRINT "oneshot% ] &";~oneshot%+os%
 8760PRINT "autonul% ] &";~autonul%+os%
 8770PRINT "trimup% ] &";~trimup%+os%
 8780PRINT "trimdwn% ] &";~trimdwn%+os%
 8790PRINT "acmeas% ] &";~acmeas%+os%
 8800PRINT "acprep% ] &";~acprep%+os%
 8810PRINT "sinread% ] &";~sinread%+os%
 8820PRINT "compact% ] &";~compact%+os%
 8830PRINT "xcompct% ] &";~xcompct%+os%
 8840PRINT "psdsoft% ] &";~psdsoft%+os%
 8850PRINT "average% ] &";~average%+os%
 8860PRINT "access% ] &";~access%+os%
 8870PRINT "delatch% ] &";~delatch%+os%
 8880PRINT "chdpro% ] &";~chdpro%+os%
 8890PRINT "assemb% = &";~assemb%
 8900PRINT "asendpll% = &";~asendpll%
 8910PRINT "assemb%+os% = &";~assemb%+os%
 8920PRINT "asendpll%+os% = &";~asendpll
%+os%
 8930PRINT"dcmeas%=&";~dcmeas%+os%;":one
shot%=&";~oneshot%+os%;":autonul%=&";~au
tonul%+os%;":trimup%=&";~trimup%+os%;":t
rimdwn%=&";~trimdwn%+os%;":acmeas%=&";~a
cmeas%+os%;":acprep%=&";~acprep%+os%;":s
inread%=&";~sinread%+os%
 8940PRINT"lcompact%=&";~compact%+os%;":
xcompct%=&";~xcompct%+os%;":psdsoft%=&";
~psdsoft%+os%;":average%=&";~average%+os
%;":access%=&";~access%+os%;":delatch%=&
";~delatch%+os%;":chdpro%=&";~chdpro%+os
%;":rts%=&";~rts%+os%
```

APPENDIX 5(a)

Sinegenerator Latch and Detector Latch Programming

Sinegenerator latch programming is as follows:-

BIT	Purpose
B7	Frequency select (M.S.B.)
B6	Frequency select
B5	Frequency select
B4	Frequency select
B3	Frequency select (L.S.B.)
B2	Amplitude select (M.S.B.)
B1	Amplitude select
B0	Amplitude select (L.S.B.)

Detector latch programming is as follows:-

BIT	Purpose
B7	2V/14-range select (low for 9V)
B6	D.c./A.c.-mode select (low for D.c.)
B5	Sample-Hold/Trigger control
B4	Sinegenerator polarity select
B0 - B3	(Unused)

Notes:-

- A positive-then-negative-going sinewave is produced for BIT4 low. An inverted sinewave is produced for BIT4 high.

APPENDIX 5(b)

A Table of FSF's Versus Frequencies

Main Series		Intermediate Series	
FSF	Frequency	FSF	Frequency
0	128	128	$85\frac{1}{3}$
8	64	136	$42\frac{2}{3}$
16	32	144	$21\frac{1}{3}$
24	16	152	$10\frac{2}{3}$
32	8	160	$5\frac{1}{3}$
40	4	168	$2\frac{1}{3}$
48	2	176	$1\frac{1}{3}$
56	1	184	$\frac{2}{3}$
64	$\frac{1}{2}$	192	$\frac{1}{3}$
72	$\frac{1}{4}$	200	$\frac{1}{6}$
80	$\frac{1}{8}$	208	$\frac{1}{3}$

Notes:-

- "FSF" represents "Frequency-Setting-Factor".

- Two interleaved binary-weighted frequency sequences.

are available and are shown above in separate tables. Note that the top bit of an FSF (assuming a binary representation) effectively selects between sequences.

APPENDIX 5(c)

A Table of ASF's Versus Amplitude Settings

ASF	Relative Excitation Amplitude	Optimum Load Impedance
0	128	~10mΩ
1	64	~20mΩ
2	32	~39mΩ
3	16	~78mΩ
4	8	~156mΩ
5	4	~312mΩ
6	2	~624mΩ
7	1	~1.25Ω

Notes:-

- "ASF" represents "Amplitude-Setting-Factor".

- An ASF of 0 causes the Sinegenerator to produce an excitation current at maximum amplitude (the value of which is determined by hardware). Other ASF's result in smaller excitation currents, the values of which are in a binary-weighted sequence.

- Approximate optimum load (cell/battery) impedances are given based on an estimated peak response voltage of {(3000/8192) = 0.37} of the Detector f.s.d. which allows a overload safety margin of {1/0.37 = 2.7}.

APPENDIX 5(d)

The AEF and CTF Formulas

The AEF formula is ...

$$(\text{Scaling Factor}) = 2^{((\text{AEF} - 128)/32)}$$

The inverse of the AEF formula is ...

$$\text{AEF} = \{(16/\log(2)) * \log(\text{Scaling Factor})\} + 128$$

Notes:-

- "AEF" represents "Amplitude-Estimation-Factor".
- AEF's are used to generate scaling factors in the range $^1/_{16}$ to 16 for use in measurement amplitude estimation process.

The CTF formula is ...

CTF = 0 for single-cell batteries AND measurement sequence "0"

CTF = 64 for single-cell batteries AND meas. sequence "1"

CTF = 128 for multi-cell batteries AND meas. sequence "2"

CTF = 192 for multi-cell batteries AND meas. sequence "3"

Notes:-

- "CTF" represents "Cell-Type-Factor".
- CTF's are used to program the Detector for battery type (single- or multi-cell) and to select one of two FSF/AF blocks for each battery type.

APPENDIX 5(e)

A Table of CPB's Versus Charge-Discharge Currents

Notes:-

- "CPB" refers to "Cell-Programming-Byte".
- "LO OPT", "MED OPT", "HI OPT" refer respectively to the low-current, medium-current and high-current options of Charge-Discharge (Ch-D) modules which are selected by means of hardware links on individual modules.
- The least significant bit of a CPB (assuming a binary representation) is irrelevant.
- A CPB of 254 is special in that it programs a Ch-D module such that the (cell/battery) load is isolated from the current-generation circuitry by means of a reed relay. Note that a Ch-D module in the isolated-zero-current mode has its yellow L.E.D. indicator extinguished as an indicator of the mode.

CPB	HI OPT	MED OPT	LO OPT
126	630	315	157.5
124	620	310	155
122	610	305	152.5
120	600	300	150
118	590	295	147.5
116	580	290	145
114	570	285	142.5
112	560	280	140
110	550	275	137.5
108	540	270	135
106	530	265	132.5
104	520	260	130
102	510	255	127.5
100	500	250	125
98	490	245	122.5
96	480	240	120
94	470	235	117.5
92	460	230	115
90	450	225	112.5
88	440	220	110
86	430	215	107.5
84	420	210	105
82	410	205	102.5
80	400	200	100
78	390	195	97.5
76	380	190	95
74	370	185	92.5
72	360	180	90
70	350	175	87.5
68	340	170	85
66	330	165	82.5
64	320	160	80
62	310	155	77.5
60	300	150	75
58	290	145	72.5
56	280	140	70
54	270	135	67.5
52	260	130	65
50	250	125	62.5
48	240	120	60
46	230	115	57.5
44	220	110	55
42	210	105	52.5
40	200	100	50
38	190	95	47.5
36	180	90	45
34	170	85	42.5
32	160	80	40
30	150	75	37.5
28	140	70	35
26	130	65	32.5
24	120	60	30
22	110	55	27.5

20	100	50	25
18	90	45	22.5
16	80	40	20
14	70	35	17.5
12	60	30	15
10	50	25	12.5
8	40	20	10
6	30	15	7.5
4	20	10	5
2	10	5	2.5

CPB	HI OPT	MED OPT	LO OPT
0	0	0	0
254	(Ch-D output relay open - ISOLATED)		
252	-20	-10	-5
250	-30	-15	-7.5
248	-40	-20	-10
246	-50	-25	-12.5
244	-60	-30	-15
242	-70	-35	-17.5
240	-80	-40	-20
238	-90	-45	-22.5
236	-100	-50	-25
234	-110	-55	-27.5
232	-120	-60	-30
230	-130	-65	-32.5
228	-140	-70	-35
226	-150	-75	-37.5
224	-160	-80	-40
222	-170	-85	-42.5
220	-180	-90	-45
218	-190	-95	-47.5
216	-200	-100	-50
214	-210	-105	-52.5
212	-220	-110	-55
210	-230	-115	-57.5
208	-240	-120	-60
206	-250	-125	-62.5
204	-260	-130	-65
202	-270	-135	-67.5
200	-280	-140	-70
198	-290	-145	-72.5
196	-300	-150	-75
194	-310	-155	-77.5
192	-320	-160	-80
190	-330	-165	-82.5
188	-340	-170	-85
186	-350	-175	-87.5
184	-360	-180	-90
182	-370	-185	-92.5
180	-380	-190	-95
178	-390	-195	-97.5
176	-400	-200	-100
174	-410	-205	-102.5
172	-420	-210	-105
170	-430	-215	-107.5
168	-440	-220	-110
166	-450	-225	-112.5
164	-460	-230	-115
162	-470	-235	-117.5
160	-480	-240	-120
158	-490	-245	-122.5
156	-500	-250	-125
154	-510	-255	-127.5
152	-520	-260	-130

150	-530	-265	-132.5
148	-540	-270	-135
146	-550	-275	-137.5
144	-560	-280	-140
142	-570	-285	-142.5
140	-580	-290	-145
138	-590	-295	-147.5
136	-600	-300	-150
134	-610	-305	-152.5
132	-620	-310	-155
130	-630	-315	-157.5
128	-640	-320	-160

APPENDIX 6(a)

A Listing of Example BASIC Program "dCELRUN"

Notes:-

- The program operates in B.B.C. BASIC MODE7 (Teletext mode).

- The program contains embedded Teletext graphics codes. For purposes of printability these have been replaced with "£" characters.

```
   10REM "dCELRUN"
   20
   30REM uses an integral DATA table for cell/Ch-D-routine data
   40MODE7
   50HIMEM=&62FF:VDU15
   60R%=J%:J%=0
   70REM WARNING:- a printer is required if this program is not to hang!
   80DIM order$(100):FOR Z%=0 TO 99:order$(Z%)="        ":NEXT:order$(100)="X"
   90dcmeas%=&6300:oneshot%=&6303:autonul%=&6338:trimup%=&63EA:trimdwn%=&63BD:ac
meas%=&643C:acprep%=&63A7:sinread%=&6472
  100compact%=&662A:xcompct%=&662D:psdsoft%=&6825:average%=&6808:access%=&6984:d
elatch%=&6997:chdpro%=&69A1:rts%=&69B3
  110CPB%=&6B00:PCR%=&6B30:CTF%=&6AC0:FSF%=&6A00:AEF%=&6A60
  120*FX3,8
  130PRINT" ***** MAIN PROGRAM *****":*FX3,0
  140REM================================
  150REM (No of cells/batteries on test - 1) (LCEL%<48) :-
  160LCEL%=47:REM 48 cells !!!
  170REM manual meas prog name:-  180mpro$=":0.$.MANMEAS"
  190REM safe voltage limits (DAC codes):-  200over1%=7000:under1%=-
10:over9%=8000:under9%=4681
  210REM================================
  220PROCPCRclr:REM PCRs always cleared on entry to "dCELRUN"
  230IF R%>999000000 dp%=R%-999000000:PROCreentry:GOTO390 ELSE dp%=1
  240*LOAD :0.U.celCODE 6300
  250PROCrhardw:PROCCPBclr
  260CLS:PRINT TAB(0,23);"":*LOAD :0.U.SCREEN1 7C00
  270*FX15,1
  280X$=GET$
  290CLS:PRINT TAB(0,22);"":*LOAD :0.U.SCREEN2 7C00
  300PROCsetendt
  310ON ERROR PROCERROR
  320CLS:VDU10,10:PRINT" If starting the system using internal   DATA table init
ial data PRESS£";CHR$(162);"I";CHR$(162):VDU10
  330PRINT" ELSE if wishing to manually amend/set   system start data PRESS£";CH
R$(162);"M";CHR$(162):VDU10,10
  340VDU23,1,0;0;0;0;
  350*FX15,1
  360REPEAT:PROCtdisp:X$=INKEY$(0):UNTIL (X$="I" OR X$="M")
  370VDU23,1,1;0;0;0;:IF X$="I" PROCstartdata ELSE CLS:PROCsyntdescr(0):PROCinpu
tlines:PROCwaittorep:PROCstartdata
  380REM================================
  390PROCCPBstochds
  400*FX15,1
  410CLS:VDU23,1,0;0;0;0;
  420PRINT"£";STRING$(38,"*"):PRINT"£Ch-D SYSTEM IS IN NORMAL/RUN MODE AND":PRIN
T"£IS MONITORING FOR OVERCHARGE/DISCH":PRINT"£";STRING$(38,"*"):VDU10
  430PRINT"£PRESS ";CHR$(162);"S";CHR$(162);" TO SUSPEND PROGRAM":VDU10
  440PRINT"£PRESS ";CHR$(162);"R";CHR$(162);" TO MANUALLY REPROGRAM WITH   £NEW
DATA":VDU10
  450PRINT" To show the last <filename>/<cell No>   list again for inspection PR
ESS£";CHR$(162);"L";CHR$(162):VDU10
  460PRINT" To show (operational) CPB's PRESS£";CHR$(162);"B";CHR$(162):VDU10
  470PRINT" To reset the system clock to a new time PRESS£";CHR$(162);"K";CHR$(1
62):VDU10
  480PRINT" To inspect or change the manual end-of- program time PRESS£";CHR$(16
2);"E";CHR$(162):VDU10,10
  490Z%=TIME:PRINT"  £PROGRAM ACTIVE TIME > ";TIME DIV 100;" SEC";TAB(39);"":VDU
```

```
11
  500FOR C%=0 TO LCEL%:PROCsafe(C%):NEXT
  510REPEAT:PROCtdisp:X$=INKEY$(0):UNTIL (TIME>=Z%+1000 OR TIME>=(data%*100) OR
TIME>=(endt%*100) OR X$="S" OR X$="L" OR X$="E" OR X$="B" OR X$="K" OR X$="R")
  520IF TIME>=(endt%*100) PROCendt
  530IF TIME>=(data%*100) VDU7:PROCusedata ELSE GOTO560
  540IF TIME>=(data%*100) VDU7:PROCusedata:GOTO540:REM test again in case the da
ta pointer is positioned too early
  550IF chn$<>"" VDU10,10,10:PROCrhardw:PROCCHAINM(chn$) ELSE GOTO390
  560IF X$="" GOTO490:REM this condition if true implies that TIME>=Z%+1000
  570VDU23,1,1;0;0;0;
  580IF X$="S" PROCsuspend ELSE IF X$="L" PROCc_clist ELSE IF X$="E" PROCreseten
dt ELSE IF X$="B" PROCCPBlist ELSE IF X$="K" PROCresetime ELSE CLS:PROCsyntdescr
(1):PROCinputlines:PROCwaittorep:GOTO390
  590GOTO400
  600REM*******************************
  610DEF PROCtdisp:VDU11:PRINT"£";STRING$(38,CHR$(255)):PRINT"£";CHR$(255);"£PRO
GRAM ACTIVE TIME = ";TIME DIV 100;" SEC£";TAB(38);CHR$(255):PRINT"£";STRING$(38,
CHR$(255)):VDU11,11:ENDPROC
  620
  630DEF PROCc_clist:LOCALcount%,X$
  640CLS:count%=0:VDU23,1,0;0;0;0;
  650REPEAT:PRINT order$(count%);",";:count%=count%+1:UNTIL order$(count%-1)="X"
:VDU127,10,10,13
  660PRINT" PRESS£";CHR$(162);"P";CHR$(162);"£FOR A PRINTER LISTING":PRINT"£PRES
S ";CHR$(162);"C";CHR$(162);" TO CONTINUE":VDU10,10
  670*FX15,1
  680C%=0:REPEAT:PROCtdisp:PROCsafe(C%):C%=(C%+1) MOD (LCEL%+1):X$=INKEY$(0)
  690UNTIL (X$="C" OR X$="P"):VDU15:VDU23,1,1;0;0;0;
  700*FX3,0
  710IF X$="C" GOTO750
  720*FX3,10
  730count%=0:REPEAT:PRINT order$(count%);",";:count%=count%+1:UNTIL order$(coun
t%-1)="X":VDU127,13,13
  740*FX3,0
  750ENDPROC
  760
  770DEF FN14BOB(L%,H%)=(256*H%+L%-8192)
  780
  790DEF FNnerr(num$):IF INSTR(num$,"E")<>0 THEN =-1 ELSE =(STR$(VAL(num$))<>num
$)
  800
  810DEF PROCrhardw:LOCAL Z%:CALLdelatch%:?&75=254:FOR Z%=0 TO 47:?&70=Z%:CALLch
dpro%:NEXT:ENDPROC
  820
  830DEF PROCCPBclr:LOCAL Z%:FOR Z%=0 TO 47:?(CPB%+Z%)=254:NEXT:ENDPROC
  840
  850DEF PROCPCRclr:LOCAL Z%:FOR Z%=0 TO 47:?(PCR%+Z%)=0:NEXT:ENDPROC
  860
  870DEF PROCsafe(C%):LOCAL DC%,X%
  880?&70=C%:CALLaccess%:X%=TIME:REPEAT UNTIL TIME>=X%+8
  890?&6BF9=?(CTF%+C%):CALLautonul%:CALLautonul%:CALLoneshot%:DC%=FN14BOB(?&76,?
&77)
  900IF (?(CPB%+C%)=0 OR ?(CPB%+C%)=254) THEN ?(PCR%+C%)=0:GOTO1030:REM zero cur
rent is always safe
  910IF ?(CTF%+C%)>127 GOTO940
  920IF DC%>over9% ?(PCR%+C%)=1 ELSE IF DC%<under9% ?(PCR%+C%)=2
  930GOTO950
```

```
  940IF DC%>over1% ?(PCR%+C%)=1 ELSE IF DC%<under1% ?(PCR%+C%)=2
  950IF (?(PCR%+C%)=1 AND ?(CPB%+C%)>=128) ?(PCR%+C%)=0:REM a disch current is a
llowed if overcharged
  960IF (?(PCR%+C%)=2 AND ?(CPB%+C%)<128) ?(PCR%+C%)=0:REM a charging current is
 allowed if overdischarged
  970IF ?(PCR%+C%)=0 GOTO1030
  980?(CPB%+C%)=254:?&70=C%:?&75=?(CPB%+C%):CALLchdpro%
  990VDU7
 1000*FX3,10
 1010PRINT CHR$(223);CHR$(223);CHR$(223);CHR$(223);" safe(";C%;") at ";TIME DIV
100;" SEC"
 1020*FX3,0
 1030CALLdelatch%:X%=TIME:REPEAT UNTIL TIME>=X%+8
 1040ENDPROC
 1050
 1060DEF PROCsuspend:LOCAL Z%,W%,Z$
 1070Z%=TIME:TIME=0
 1080PROCrhardw
 1090*FX3,10
 1100PRINT"SUSPENDED AT TIME = ";Z% DIV 100;" SEC"
 1110*FX3,0
 1120CLS:VDU10,10:PRINT"£££PROGRAM IN SUSPENSION":PRINT"£££WITH CLOCK FROZEN AT ";
Z% DIV 100;" SEC":VDU10,10
 1130PRINT"£££NTER ";CHR$(162);"M";CHR$(162);" TO CHAIN ";CHR$(162);" ";mpro$;CH
R$(162):VDU10:PRINT"£££NTER ";CHR$(162);"C";CHR$(162);" TO CONTINUE PROGRAM":VDU
10:PRINT"£££NTER ";CHR$(162);"ABORT!";CHR$(162);" TO ABORT£":VDU10
 1140*FX15,1
 1150INPUT Z$:VDU10
 1160IF Z$="C" GOTO 1250
 1170IF Z$="M" THEN TIME=Z%:PROCCHAINM(mpro$)
 1180IF Z$<>"ABORT!" VDU7,11,13:PRINT STRING$(40," ");:VDU11,11:GOTO1130
 1190VDU129
 1200*FX3,8
 1210PRINT" PROGRAM ABORTED AT TIME = ";Z% DIV 100;" SEC":VDU10:PRINT" DATA PTR
(NEXT DATA) = ";dp%
 1220*FX3,0
 1230END
 1240
 1250PROCCPBstochds
 1260susT%=TIME:TIME=Z%
 1270*FX3,10
 1280PRINT"SUSPENSION DURATION = ";susT% DIV 100;" SEC"
 1290*FX3,0
 1300ENDPROC
 1310
 1320DEF PROCwaittorep
 1330VDU23,1,0;0;0;0;
 1340CLS:PRINT"£";STRING$(38,"*"):PRINT"£££Ch-D SYSTEM IS IN WAIT-TO-REPROGRAM":P
RINT"£££MODE USING LAST REPROGRAMMING DATA":PRINT"£";STRING$(38,"*"):VDU10
 1350PRINT" To show the last <filename>/<cell No>   list sequentially for inspec
tion        PRESS£";CHR$(162);"L";CHR$(162):VDU10
 1360VDU132:PRINT"PRESS  ";:VDU157,131:PRINT"SHIFT ";:VDU132,156,157,131:PRINT"#
 ";:VDU132,156:PRINT" TO PROGRAM AND £SIMULTANEOUSLY RESET THE SYSTEM-ACTIVE £CL
OCK AND THE PCR TABLE TO ZERO":VDU10
 1370PRINT"£PRESS£";CHR$(162);"D";CHR$(162);"£TO DO Ch-D REPROGRAMMING":VDU10
 1380PRINT"£PRESS£";CHR$(162);"A";CHR$(162);"£TO ABORT CURRENT REPROGRAMM- £ING
OPERATION AND RE-ENTER DATA":VDU10,10
 1390*FX15,1
```

```
 1400C%=0:REPEAT:PROCtdisp:PROCsafe(C%):C%=(C%+1) MOD (LCEL%+1):X$=INKEY$(0):UNT
IL (X$="L" OR X$="#" OR X$="D" OR X$="A")
 1410VDU23,1,1;0;0;0;
 1420IF X$="L" PROCc_clist:GOTO1330 ELSE IF X$="A" CLS:PROCsyntdescr(1):PROCinpu
tlines:GOTO1330
 1430IF X$="#" FOR X%=0 TO LCEL%:?(PCR%+X%)=0:NEXT:TIME=0
 1440*FX3,10
 1450PRINT"MANUAL REPROGRAM AT ";TIME DIV 100;" SEC":VDU13
 1460*FX3,0
 1470PROCdatatoCPBs
 1480ENDPROC
 1490
 1500DEF PROCsyntdescr(Z%):LOCAL X%
 1510IF Z%>0 GOTO1540
 1520PRINT" Enter required Ch-D currents followed   by identity-numbers of cells
 to be      programmed with those current values"
 1530PRINT" and finally an instruction£";CHR$(162);"X";CHR$(162):VDU10
 1540PRINT" Use syntax £";CHR$(162);"I";CHR$(162);"<current>,<Cell No>,<Ce £ll N
o>,....,";CHR$(162);"I";CHR$(162);"<current>,<Cell No>,<Ce £ll No>,......£ending
 with a£......,";CHR$(162);"X";CHR$(162);"  to terminate data acceptance":VDU10
 1550PRINT" Data may be entered as a sequence of    short strings rather than as
 one long   string; i.e.£";:VDU157:PRINT"£RETURN £";:VDU156:PRINT"can be pressed
"
 1560PRINT" as often as desired though note that a  comma should never be includ
ed at the   end of a data line":VDU10
 1570PRINT" To reduce typing for groups of cells in sequence use the syntax form
          £...,<First Cell No>-<Last Cell No>,...":VDU10
 1580IF Z%>0 PRINT"££WARNING - While waiting for data input££the program is unab
le to monitor for  ££cell overcharge/discharge!":VDU10
 1590ENDPROC
 1600
 1610DEF PROCinputlines:LOCAL line$,W$,ptr%,mid$,count%,remc%,T%,Z%,Q%
 1620count%=0
 1630*FX15,1
 1640remc%=count%:ptr%=1:INPUT LINE line$
 1650IF (count%=0 AND LEFT$(line$,1)<>"I" AND LEFT$(line$,1)<>"X") PRINT"£Start
with I (or X) - Do line again!":VDU7,10:GOTO1630
 1660IF RIGHT$(line$,1)="/" line$=LEFT$(line$,(LEN(line$)-1))
 1670IF (INSTR(line$," ")<>0 OR INSTR(line$,"E")<>0 OR RIGHT$(line$,1)="," OR RI
GHT$(line$,1)="-") PRINT"£PUNCTUATION/E ERROR - Do line again!":VDU7,10:GOTO1630
 1680W$="":REPEAT
 1690W$=W$+MID$(line$,ptr%,1):ptr%=ptr%+1
 1700UNTIL (MID$(line$,ptr%,1)="," OR MID$(line$,ptr%,1)="/" OR MID$(line$,ptr%,
1)="-" OR ptr%>LEN(line$))
 1710IF MID$(line$,ptr%,1)="-" GOTO1740
 1720mid$=MID$(W$,2,4):IF((LEFT$(W$,1)="I" AND VAL(mid$)>=0 AND VAL(mid$)<=255 A
ND NOT FNnerr(mid$)) OR (NOT FNnerr(W$) AND VAL(W$)>=0 AND VAL(W$)<48) OR W$="X"
) THEN order$(count%)=W$:count%=count%+1:GOTO1790
 1730PRINT"£SYNTAX ERROR (I/cell) - Do line again!":VDU7,10:count%=remc%:GOTO163
0
 1740Z%=VAL(W$):ptr%=ptr%+1:IF (Z%<0 OR Z%>47 OR FNnerr(W$)) THEN PRINT"£SYNTAX
ERROR (c-c) - Do line again!":VDU7,10:count%=remc%:GOTO1630
 1750W$="":REPEAT:W$=W$+MID$(line$,ptr%,1):ptr%=ptr%+1
 1760UNTIL (MID$(line$,ptr%,1)="," OR MID$(line$,ptr%,1)="/" OR ptr%>LEN(line$))
 1770T%=VAL(W$):IF (T%<0 OR T%>47 OR FNnerr(W$)) THEN PRINT"£SYNTAX ERROR (c-c)
- Do line again!":VDU7,10:count%=remc%:GOTO1630
 1780REPEAT:order$(count%)=STR$(Z%):Z%=Z%+1:count%=count%+1:UNTIL (Z%>T% OR coun
t%>100)
```

```
 1790IF W$="X" VDU10 ELSE IF count%>100 PRINT"£TOO MANY ITEMS - Do line again!":
VDU7,10:count%=remc%:GOTO1630 ELSE IF ptr%>=LEN(line$) GOTO1630 ELSE ptr%=ptr%+1
:GOTO1680
 1800ENDPROC
 1810
 1820DEF PROCdatatoCPBs:LOCAL count%,I%,C%,num$
 1830count%=0
 1840IF order$(count%)="X" GOTO1890
 1850num$=MID$(order$(count%),2,4):I%=VAL(num$):count%=count%+1
 1860IF (VAL(order$(count%))=0 AND order$(count%)<>"0"):GOTO1840
 1870REPEAT:num$=(order$(count%)):C%=VAL(num$):?(CPB%+C%)=I%:count%=count%+1
 1880UNTIL (VAL(order$(count%))=0 AND order$(count%)<>"0"):GOTO1840
 1890ENDPROC
 1900
 1910DEF PROCCPBstochds:LOCAL C%:FOR C%=0 TO LCEL%:?&70=C%:?&75=?(CPB%+C%):CALLc
hdpro%:NEXT:ENDPROC
 1920
 1930DEF PROCendt:VDU23,1,1;0;0;0;:PROCrhardw:VDU7,7:PRINT"£";CHR$(255);" £END-T
IME REACHED =    ";TIME DIV 100:VDU10:END
 1940
 1950DEF PROCresetime:LOCAL time$,Z$,C%
 1960CLS:VDU10,10,10:PRINT" ENTER New value of time in seconds      ELSE PRESS "
;:VDU132,157,131:PRINT"RETURN ";:VDU135,156:PRINT" to maintain     present clock
 status":VDU10
 1970PRINT"££WARNING - While waiting for data input££the program is unable to mo
nitor for  ££cell overcharge/discharge!":VDU10
 1980*FX15,1
 1990INPUT time$:IF time$="" GOTO2050 ELSE IF (LEN(time$)>7 OR FNnerr(time$)) VD
U7:GOTO1960
 2000VDU10:PRINT" The new value will be£";VAL(time$):VDU10:PRINT"£PRESS£";CHR$(1
62);"D";CHR$(162);"£TO DO THE OPERATION":VDU10:PRINT"£PRESS£";CHR$(162);"A";CHR$
(162);"£TO ABORT AND RE-ENTER DATA":VDU10,10
 2010VDU23,1,0;0;0;0;
 2020*FX15,1
 2030C%=0:REPEAT:PROCtdisp:PROCsafe(C%):C%=(C%+1) MOD (LCEL%+1):Z$=INKEY$(0):UNT
IL (Z$="D" OR Z$="A")
 2040VDU23,1,1;0;0;0;:IF Z$="D" THEN TIME=VAL(time$)*100 ELSE GOTO1960
 2050ENDPROC
 2060
 2070DEF PROCsetendt:LOCAL X$
 2080*FX15,1
 2090INPUT X$:IF X$="" THEN endt%=9999999:GOTO2110
 2100IF (LEN(X$)>7 OR FNnerr(X$)) VDU7,11:PRINT STRING$(38," ");:VDU13:GOTO2090
ELSE endt%=VAL(X$)
 2110ENDPROC
 2120
 2130DEF PROCresetendt:LOCAL endt$,Z$,C%
 2140CLS:VDU10,10,10:PRINT" The current time for manual program end is£";endt%:V
DU10
 2150PRINT" ENTER New value for the manual end-of-  -program time  ELSE PRESS ";
:VDU132,157,131:PRINT"RETURN ";:VDU135,156:PRINT"  to maintain the present value
":VDU10
 2160PRINT"££WARNING - While waiting for data input££the program is unable to mo
nitor for  ££cell overcharge/discharge!":VDU10
 2170*FX15,1
 2180INPUT endt$:IF endt$="" GOTO2260
 2190IF (LEN(endt$)>7 OR FNnerr(endt$)) VDU7:GOTO2140
 2200CLS:VDU10:PRINT" The current value is£";endt%:VDU10
```

```
 2210PRINT" THE new value will be£";VAL(endt$);"£(?)":VDU10:PRINT"£PRESS£";CHR$(
162);"D";CHR$(162);"£TO DO THE OPERATION":VDU10:PRINT"£PRESS£";CHR$(162);"A";CHR
$(162);"£TO ABORT AND RE-ENTER DATA":VDU10,10
 2220VDU23,1,0;0;0;0;
 2230*FX15,1
 2240C%=0:REPEAT:PROCtdisp:PROCsafe(C%):C%=(C%+1) MOD (LCEL%+1):Z$=INKEY$(0):UNT
IL (Z$="D" OR Z$="A")
 2250VDU23,1,1;0;0;0;:IF Z$="A" GOTO2140 ELSE endt%=VAL(endt$)
 2260ENDPROC
 2270
 2280DEF PROCCPBlist:LOCAL C%,tab%,Z$:CLS:VDU23,1,0;0;0;0;
 2290FOR C%=0 TO (LCEL%-1) STEP 2:IF C%>9 tab%=-1 ELSE tab%=0
 2300PRINT TAB(9+tab%);"£";C%;"£";?(CPB%+C%),TAB(24+tab%);"£";C%+1;"£";?(CPB%+C%
+1):NEXT
 2310PRINT"£PRESS ";CHR$(162);"C";CHR$(162);" TO CONTINUE "
 2320*FX15,1
 2330C%=0:REPEAT:PROCsafe(C%):C%=(C%+1) MOD (LCEL%+1):Z$=INKEY$(0):UNTIL Z$="C":
VDU23,1,1;0;0;0;:ENDPROC
 2340
 2350DEF PROCstartdata:LOCAL data$
 2360READ data$:dp%=dp%+1:IF data$="#?" GOTO2390
 2370num$=(MID$(data$,2,8))
 2380IF (LEFT$(data$,1)<>"#" OR LEN(num$)>7 OR FNnerr(num$)) THEN PROCrhardw:VDU
10,10,10:PRINT"££ABORTED! - DATA error (#)":VDU10:PRINT" D.P. = ";dp%;"  TIME =
";TIME DIV 100;" SEC":STOP:ELSE TIME=100*VAL(num$)
 2390PROCusedata:ENDPROC
 2400
 2410DEF PROCusedata:LOCAL data$,Z$,T$,I%,C%,dash%:READ data$:dp%=dp%+1
 2420IF LEFT$(data$,1)="M" chn$=(MID$(data$,2,14)):GOTO2560 ELSE chn$=""
 2430IF data$="X" GOTO2560
 2440IF LEFT$(data$,1)="E" PROCendt
 2450num$=(MID$(data$,2,4)):I%=VAL(num$)
 2460IF (LEFT$(data$,1)<>"I" OR I%<0 OR I%>255 OR FNnerr(num$)) THEN PROCrhardw:
VDU10,10,10:PRINT"££ABORTED! - DATA error (I)":VDU10:PRINT" D.P. = ";dp%;"  TIME
 = ";TIME DIV 100;" SEC":STOP ELSE READ data$:dp%=dp%+1
 2470IF LEFT$(data$,1)="I" GOTO2450 ELSE IF data$="X" GOTO2560
 2480dash%=INSTR(data$,"-"):IF dash%<>0 GOTO2520
 2490REPEAT:num$=data$:C%=VAL(num$)
 2500IF (C%<0 OR C%>47 OR FNnerr(num$)) THEN PROCrhardw:VDU10,10,10:PRINT"££ABOR
TED! - DATA error (cell No)":VDU10:PRINT" D.P. = ";dp%;"  TIME = ";TIME DIV 100;
" SEC":STOP ELSE ?(CPB%+C%)=I%:READ data$:dp%=dp%+1
 2510IF (VAL(LEFT$(data$,1))=0 AND LEFT$(data$,1)<>"0") GOTO2430 ELSE GOTO2480
 2520Z$=LEFT$(data$,(dash%-1)):T$=MID$(data$,(dash%+1),3)
 2530IF (VAL(Z$)<0 OR VAL(T$)<0 OR VAL(Z$)>47 OR VAL(T$)>47 OR FNnerr(Z$) OR FNn
err(T$)) THEN PROCrhardw:VDU10,10,10:PRINT"££ABORTED! - DATA error (cell-cell)":
VDU10:PRINT" D.P. = ";dp%;"  TIME = ";TIME DIV 100;" SEC":STOP
 2540FOR C%=VAL(Z$) TO VAL(T$):?(CPB%+C%)=I%:NEXT:READ data$:dp%=dp%+1
 2550IF (VAL(LEFT$(data$,1))=0 AND LEFT$(data$,1)<>"0") GOTO2430 ELSE GOTO2480
 2560READ data$:dp%=dp%+1:num$=(MID$(data$,2,8))
 2570IF (LEFT$(data$,1)<>"T" OR LEN(num$)>7 OR FNnerr(num$)) THEN PROCrhardw:VDU
10,10,10:PRINT"££ABORTED! - DATA error (T)":VDU10:PRINT" D.P. = ";dp%;"  TIME =
";TIME DIV 100;" SEC":STOP
 2580data%=VAL(num$)
 2590ENDPROC
 2600
 2610DEF PROCreentry:LOCAL data$,num$,Z%:ON ERROR PROCERROR
 2620FOR Z%=1 TO (dp%-1):READ data$:NEXT:num$=(MID$(data$,2,8))
 2630IF (LEFT$(data$,1)<>"T" OR LEN(num$)>7 OR FNnerr(num$)) THEN PROCrhardw:VDU
```

```
10,10,10:PRINT"££ABORTED! - DATA error (T on reentry)":STOP
 2640data%=VAL(num$):TIME=K%:endt%=L%:ENDPROC
 2650
 2660DEF PROCCHAINM(X$):CLS:PRINT" NOW CHAINing ";CHR$(162);X$;CHR$(162):PRINT"
and preparing for re-entry into this    program upon its completion":VDU10
 2670PRINT" Setting £J%=";999000000+dp%:PRINT"          £K%=";TIME:PRINT"
 £L%=";endt%:PRINT"          £M%=";LCEL%:VDU10
 2680J%=999000000+dp%:K%=TIME:L%=endt%:M%=LCEL%:CHAIN X$
 2690
 2700DEF PROCERROR:PROCrhardw:VDU7,7,7,7:VDU23,1,0;0;0;0;:VDU10,10:REPORT:VDU10,
10,13:PRINT"£FOR SPECIAL RESTART SET:-":VDU10:PRINT" J%=";999000000+dp%;":K%=";T
IME;":L%=";endt%:VDU10:END
 2710REM*******************************
 2720REM DATA TABLE starts here
 2730DATA#?,X,T9999999,E:REM NULL DATA!
```

APPENDIX 6(b)

A Listing of Example BASIC Program "MAF"

Notes:-

- The program operates in B.B.C. BASIC MODE7 (Teletext mode).

- The program contains embedded Teletext graphics codes. For purposes of printability these have been replaced with "£" characters.

```
   10progname$="MAF":REM name given here determines the data-out option (3rd cha
r)
   30REM================================
   40REM a measurement program for use with a RUN-control program saved as "DUMM
Y"
   50REM this program uses data currently in the FSF/CTF table to select measure
ments
   60REM WARNING:- this program outputs data to a disk file which should have al
ready been opened manually using an OPENOUT command and its channel number place
d in integer variable N% !
   70REM WARNING:- if the "BREAK" key is ever used to abort this program or a sy
stem program which CHAINs this program then the previously chosen output file ma
y be corrupted or made unavailable for further output!
   80REM WARNING:- an on-line printer is required and user machine code must be
present in main memory!
   90MODE7
  100HIMEM=&62FF:VDU15
  110REM disable ESCAPE key:-
  120*FX229,1
  130ON ERROR PROCERRORN
  140dcmeas%=&6300:oneshot%=&6303:autonul%=&6338:trimup%=&63EA:trimdwn%=&63BD:ac
meas%=&643C:acprep%=&63A7:sinread%=&6472
  150compact%=&662A:xcompct%=&662D:psdsoft%=&6825:average%=&6808:access%=&6984:d
elatch%=&6997:chdpro%=&69A1:rts%=&69B3
  160CPB%=&6B00:PCR%=&6B30:CTF%=&6AC0:FSF%=&6A00:AEF%=&6A60
  170REM================================
  180REM No's of cells on test (0-LCEL%) where LCEL%="LAST CELL":-
  190REM (value may be transferred from "DUMMY" in variable M%)
  200LCEL%=M%
  210REM================================
  220REM autonulling trim time (1/100th's SEC) :-
  230atrimT%=10
  240REM================================
  250REM optimum a.c. meas amplitude (14-bit DAC LSB's) :-
  260alampl%=3000:REM!!!!!
  270REM================================
  280REM scaling factors for deriving exact d.c. voltages ( = meas system input
voltage in Volts for 1 DAC LSB) :-
  290REM for 1.5V cells
  300dcscal1=2.44141E-4:REM!!!!!
  310REM for 9V cells
  320dcscal9=(2.44141E-4)*7:REM!!!!!
  330REM================================
  340REM scaling factors for deriving exact impedance components:-
  350REM for 1.5V cells
  360scale1=5.13192954E-6:REM!!!!!
  370REM for 9V cells
  380scale9=(5.13192954E-6)*7:REM!!!!!
  390REM================================
  400REM data-out option is coded into the program name
  410REM items to be outputted to disk ("F" fundamental, "H" harmonics, "B" both
 ):-
  420dataout$=MID$(progname$,3,1)
  430REM================================
  440*FX3,8
  450PRINT STRING$(20,"=");" TIME ";TIME DIV 100;TAB(40);progname$;" ";STRING$((
38-LEN(progname$)),"="):*FX3,0
  460FOR C%=0 TO LCEL%
```

```
  470PRINT"£CELL No ";C%;" MEASUREMENTS:-":
  480?&70=C%:CALLaccess%:?&6BF9=?(CTF%+C%):Z%=TIME:REPEAT:UNTIL TIME>=Z%+8
  490PROCacN
  500CALLdelatch%:Z%=TIME:REPEAT:UNTIL TIME>=Z%+8
  510NEXT
  520*FX229,0
  530REM return to main program by CHAINing it:-
  540CHAIN"DUMMY"
  550REM*******************************
  560DEF PROCmsqN:LOCAL M%,Q%,Z%,T%,AV%,PKA%,HIVAL%,EST%,term%,scale
  570T%=(?(CTF%+C%) DIV 64):IF (T%=2 OR T%=3) scale=scale1 ELSE scale=scale9
  580T%=24*T%
  590REM a pre-meas cell-inspection (using a set low amplitude) to roughly gauge
 cell impedance for setting sinegen-ampl for the first main measurement:-
  600?&6BF8=(?(FSF%+T%) OR ?(AEF%+T%))
  610CALLacmeas%:CALLsinread%:CALLcompact%:CALLaverage%
  620AV%=(256*?&6BF2+?&6BF1)/2-24576:PRINT"£INSP MEAS AV DC = ";AV%
  630REM now the main a.c. measurement series using a method to estimate optimum
 sinegen-ampl settings:-
  640M%=1
  650term%=0
  660HIVAL%=(256*?&83+?&82)-8192
  670AV%=(256*?&6BF2+?&6BF1)/2-24576
  680PKA%=HIVAL%-AV%
  690REM choose a value to estimate amplitude in the event of a detector overloa
d or if somehow PKA%<=0 :-
  700over1%=0:IF (HIVAL%=8191 OR ?&84=1 OR PKA%<=0) PKA%=16384:over1%=-1
  710PRINT"£**£AV";AV%;
  720PRINT TAB(11);:IF over1%=-1 PRINT"£OVERLOAD!"; ELSE PRINT"£**£PKA";PKA%;
  730IF over1%=-1 BPUT#N%,255:BPUT#N%,255 ELSE BPUT#N%,(PKA% MOD 256):BPUT#N%,(P
KA% DIV 256):REM put PKA% to disk in two bytes
  740IF term% GOTO1100
  750REM estimate amplitude at detector for next measurement assuming singen-amp
l to be unchanged:-
  760EST%=PKA%*2^((?(AEF%+T%+M%)-128)/32)
  770REM adjust sinegen-amplitude as necessary (by powers of 2) and set sinegen-
freq:-
  780Q%=alampl% DIV 256:Z%=-8:REPEAT:Q%=Q%*2:Z%=Z%+1:UNTIL EST%<=Q%
  790Z%=Z%+(?&6BF8 AND 7):IF Z%<0 THEN Z%=0 ELSE IF Z%>7 THEN Z%=7
  800?&6BF8=(?(FSF%+T%+M%) OR Z%)
  810PRINT TAB(22);"£***£";?(FSF%+T%+M%);TAB(30);"+";Z%;TAB(33);"=";?&6BF8;TAB(3
7);"£**";
  820BPUT#N%,?(FSF%+T%+M%):BPUT#N%,Z%:REM put sinegen freq- and ampl- factors se
perately to disk in one byte each
  830REM do measurement:-
  840CALLacmeas%:CALLsinread%:CALLcompact%
  850REM analyze a.c. measurement result looking at harmonics No's 1,2,3,4,6 - N
OTE THAT THIS PROGRAM SECTION MAY BE MODIFIED AS DESIRED !!!
  860IF (?(FSF%+T%+M%) MOD 128)=0 Ncyc1%=2 ELSE Ncyc1%=1
  870?&75=12 DIV Ncyc1%:CALL psdsoft%
  880@%=&20210A:PRINT FNREAL,FNIMAG;"   £(AMPL=";SQR(FNREAL^2+FNIMAG^2)*SQR2;")"
  890BPUT#N%,?&6BF0:BPUT#N%,?&6BF1:BPUT#N%,?&6BF2:BPUT#N%,?&6BF4:BPUT#N%,?&6BF5:
BPUT#N%,?&6BF6:REM put REAL and IMAGINARY parts to disk in three bytes each (in
an offset binary code)
  900IF FNREAL=0 THEN PHA=PI/2:PRINT"£PHASE ANGLE 90 DEG - SYSTEM FAULT?" ELSE P
HA=DEG ATN(FNIMAG/FNREAL)
  910Z=SQR(FNIMAG^2+FNREAL^2)*2^Z%*scale
  920R=FNREAL*2^Z%*scale:X=-FNIMAG*2^Z%*scale
```

```
  930L=X*1E6/(2*PI*FNFREQ(?(FSF%+T%+M%)))
  940IF X=0 THEN C=999999999 ELSE C=-1/(2*PI*FNFREQ(?(FSF%+T%+M%))*X)
  950@%=&10508:PRINT"£Z=";Z;"R=";R;"X=";X;
  960PRINT TAB(40);"£C(ser)=";C;"F";TAB(61);"£(";L;"uH)":@%=10
  970@%=&2020A
  980?&75=6 DIV Ncycl%:CALLpsdsoft%
  990PRINT FNREAL,FNIMAG;"";
 1000IF dataout$="H" BPUT#N%,?&6BF0:BPUT#N%,?&6BF1:BPUT#N%,?&6BF2:BPUT#N%,?&6BF4
:BPUT#N%,?&6BF5:BPUT#N%,?&6BF6:REM to disk
 1010?&75=4 DIV Ncycl%:CALLpsdsoft%
 1020PRINT FNREAL,FNIMAG;"";
 1030IF dataout$="H" BPUT#N%,?&6BF0:BPUT#N%,?&6BF1:BPUT#N%,?&6BF2:BPUT#N%,?&6BF4
:BPUT#N%,?&6BF5:BPUT#N%,?&6BF6:REM to disk
 1040?&75=3 DIV Ncycl%:CALLpsdsoft%
 1050PRINT FNREAL,FNIMAG:@%=10
 1060IF dataout$="H" BPUT#N%,?&6BF0:BPUT#N%,?&6BF1:BPUT#N%,?&6BF2:BPUT#N%,?&6BF4
:BPUT#N%,?&6BF5:BPUT#N%,?&6BF6:REM to disk
 1070CALLaverage%:M%=M%+1
 1080IF ?(FSF%+T%+M%)=255 term%=-1
 1090GOTO660:REM loop back
 1100PRINT TAB(22);"£***£(TERMINATE)"
 1110ENDPROC
 1120REM*********************************
 1130DEF FNREAL=((256*256*?&6BF2+256*?&6BF1+?&6BF0)/512)-16384
 1140REM*********************************
 1150DEF FNIMAG=((256*256*?&6BF6+256*?&6BF5+?&6BF4)/512)-16384
 1160REM*********************************
 1170DEF FNFREQ(F%)=2^(7-(F% AND 127)/8)/(1+(F% AND 128)/256)
 1180REM*********************************
 1190DEF FN14BOB(L%,H%)=256*H%+L%-8192
 1200REM*********************************
 1210DEF PROCatrim(Z%):LOCAL T%,aLO%,aHI%
 1220T%=TIME:CALLoneshot%
 1230IF FN14BOB(?&76,?&77)<0 THEN trim%=trimdwn% ELSE IF FN14BOB(?&76,?&77)>0 TH
EN trim%=trimup% ELSE trim%=rts%
 1240REPEAT:aLO%=?&76:aHI%=?&77:CALLtrim%:CALLoneshot%:UNTIL ABS FN14BOB(?&76,?&
77) > ABS FN14BOB(aLO%,aHI%) OR TIME>=T%+Z%
 1250IF trim%=trimdwn% THEN CALLtrimup% ELSE IF trim%=trimup% THEN CALLtrimdwn%
ELSE CALLrts%
 1260REPEAT:UNTIL TIME>=T%+Z%:ENDPROC
 1270REM*********************************
 1280DEF PROCacN:LOCAL T%,dcscal
 1290T%=(?(CTF%+C%) DIV 64):IF (T%=2 OR T%=3) dcscal=dcscal1 ELSE dcscal=dcscal9
 1300CALLautonul%:CALLautonul%:CALLoneshot%
 1310PRINT"£DC = ";FN14BOB(?&76,?&77);" LSB";:@%=&2040A:PRINT TAB(15);" (";dcsca
l*FN14BOB(?&76,?&77);" Volts)":@%=10
 1320BPUT#N%,?&76:BPUT#N%,?&77:REM put d.c. meas value to disk in two bytes (in
an offset binary form)
 1330CALLacprep%:PROCatrim(atrimT%):PROCmsqN:CALLautonul%:ENDPROC
 1340REM*********************************
 1350DEF PROCERRORN
 1360PROCrhardw:*FX229,0
 1370VDU10:PRINT"££********** ERROR! **********":REPORT:PRINT" at line ";
ERL:VDU10:PRINT"££ABORTED AT£TIME = ";TIME DIV 100;" SEC":VDU10:PRINT" £(Note:-
DISK O/P FILE IS NOT CLOSED)":END
 1380REM*********************************
 1390DEF PROCrhardw:LOCAL Z%:CALLdelatch%:?&75=254:FOR Z%=0 TO 47:?&70=Z%:CALLch
dpro%:NEXT:ENDPROC:REM resets all Ch-D modules to the inactive state
```

APPENDIX 6(c)

The Text of Screenload File "U.SCREEN1"

```
^A UTILITY TO AUTOMATICALLY OR MANUALLY
^PROGRAM Ch-D MODULES (i.e. cell charge
^-discharge currents) AND ALSO TO TAKE
^AUTOMATIC OR MANUAL MEASUREMENTS ON THE
^CELLS UNDERGOING DUTY CYCLING

^Note:-^This program requires a valid
  auto-programming instruction sequence
 to be present in an integral DATA table
 (program lines approx. 3000 onwards)
 Notes on DATA table syntax are provided
 in REM lines within program ^valDATA^

 This program^always^obeys^all^commands
 contained in its DATA table but allows
 manual reprogramming of any Ch-D module
 or taking of measurements at any time

 If purely manual Ch-D system control is
 desired then the DATA table must hold
 an instruction sequence such as:-
^?,X,T9999999,E^

^PRESS A KEY TO CONTINUE
```

Notes:-

- "U.SCREEN1" is intended as a screenload file for B.B.C. BASIC MODE7 (Teletext).

- The file contains embedded Teletext graphics control codes. For purposes of printability these have been replaced with "^" characters.

APPENDIX 6(d)

The Text of Screenload File "U.SCREEN2"

```
^Note:-^This program uses the BASIC TIME
 clock fairly directly for auto-program-
 ming and end-of-program functions so to
 assist the user a display of (TIME DIV
 100) is provided wherever possible
^Note:-^The only time that the system
 clock is stopped is whilst a program is
 formally SUSPENDED
 From the viewpoint of a user of this
 program the TIME clock is effectively
 frozen during any  period of suspension
^Note:-^If using pure manual programming
 it is not essential to reset TIME to
 zero at the start of a run
^**************************************
 PRESS ^^^RETURN ^^ to set the program-
 end-time according to the value stored
 in this program's DATA table ELSE enter
 a value in seconds to terminate this
 program at any EARLIER time
^Note:-^The DATA end-time value has
 equal priority to a value entered here!
```

Notes:-

- "U.SCREEN2" is intended as a screenload file for B.B.C. BASIC MODE7 (Teletext mode).

- The file contains embedded Teletext graphics control codes. For purposes of printability these have been replaced with "^" characters.

APPENDIX 6(e)

A Listing of Example BASIC Program "valDATA"

Notes:-

- The program operates in B.B.C. BASIC MODE7 (Teletext mode).

- The program contains embedded Teletext graphics codes. For purposes of printability these have been replaced with "£" characters.

```
   10REM "valDATA"
   20
   30MODE7:VDU15
   40HIMEM=&62FF
   50CLS:PRINT"£A UTILITY FOR CHECKING THE VALIDITY OF £ITEMS IN A BASIC DATA TE
XT FILE (in the£format as produced by ";CHR$(162);"P.genDATA";CHR$(162);") FOR £
PURPOSES OF Ch-D SYSTEM CONTROL":VDU10
   60PRINT"£Important:-£The DATA text file must be  ";CHR$(42);"EXEC'ed onto the
 end of this program   before use":VDU10
   70PRINT"£Note:-£This program does not check that timing increments are sensib
le - poor   timings may result in data items being  ignored by charge/discharge
programs":VDU10
   75PRINT"£Note:-£An 'Out of DATA' error will      result if the required charg
e/discharge sequence terminator ";CHR$(162);"E";CHR$(162);" is missing":VDU10
   80PRINT"£";STRING$(39,"*")
   90PRINT" PRESS£";CHR$(162);"P";CHR$(162);"£to check/display DATA using   page
d mode":VDU10:PRINT" PRESS£";CHR$(162);"N";CHR$(162);"£to check/display DATA usi
ng   normal screen scrolling"
  100REPEAT:X$=INKEY$(0):UNTIL (X$="P" OR X$="N")
  110IF X$="P" VDU14
  120REM==============================
  130CLS:item%=0
  140READ data$:item%=item%+1:PRINT item%;TAB(16);"£";data$
  150IF data$="#?" GOTO180
  160num$=(MID$(data$,2,8))
  170IF (LEFT$(data$,1)<>"#" OR LEN(num$)>7 OR FNnerr(num$)) THEN PRINT"£DATA er
ror in item ";item%;"  (#)":END
  180REPEAT:PROCtestdata:UNTIL FALSE
  190REM**********************************
  200REM Full data checking is used
  210DEF PROCtestdata:LOCAL data$,Z$,T$,I%,C%,dash%
  220READ data$:item%=item%+1:PRINT item%;TAB(16);:IF (LEFT$(data$,1))="M" PRINT
"£";data$:GOTO390
  230IF LEFT$(data$,1)="E" PRINT"£";data$:PRINT"£DATA TABLE IS OK":END
  240IF data$="X" PRINT"£";data$:GOTO390 ELSE PRINT "£";data$;
  250IF (LEFT$(data$,1))="T" THEN :PRINT"":PRINT"£DATA error in item ";item%;"
(missing X?)":END
  260num$=(MID$(data$,2,4)):I%=VAL(num$)
  270IF (LEFT$(data$,1)<>"I" OR I%<0 OR I%>255 OR FNnerr(num$)) THEN :PRINT"":PR
INT"£DATA error in item ";item%;"  (I?)":END
  280READ data$:item%=item%+1
  290IF LEFT$(data$,1)="I" PRINT"£(Redundant)":PRINT item%;TAB(16);"£";data$;:GO
TO250 ELSE IF data$="X" PRINT"£(Redundant)":PRINT item%;TAB(16);"£";data$:GOTO39
0 ELSE PRINT"":PRINT item%;TAB(16);"£";data$
  300dash%=INSTR(data$,"-"):IF dash%<>0 GOTO340
  310num$=data$:C%=VAL(num$):IF (C%<0 OR C%>47 OR FNnerr(num$)) THEN PRINT"£DATA
 error in item ";item%;"  (cell No?)":END
  320READ data$:item%=item%+1
  330IF (VAL(LEFT$(data$,1))=0 AND LEFT$(data$,1)<>"0") PRINT item%;TAB(16);:GOT
O230 ELSE PRINT item%;TAB(16);"£";data$:GOTO300
  340Z$=LEFT$(data$,(dash%-1)):T$=MID$(data$,(dash%+1),3)
  350IF (VAL(Z$)<0 OR VAL(T$)<0 OR VAL(Z$)>47 OR VAL(T$)>47 OR FNnerr(Z$) OR FNn
err(T$)) THEN PRINT"£DATA error in item ";item%;"  (cell-cell)":END
  360READ data$:item%=item%+1
  370IF (VAL(LEFT$(data$,1))=0 AND LEFT$(data$,1)<>"0") PRINT item%;TAB(16);:GOT
O230 ELSE PRINT item%;TAB(16);"£";data$:GOTO300
  380REM This DATA element gives timing info
  390READ data$:item%=item%+1:PRINT item%;TAB(16);"£";data$
```

```
  400num$=(MID$(data$,2,8)):IF (LEFT$(data$,1)<>"T" OR LEN(num$)>7 OR FNnerr(num
$)) THEN PRINT"£DATA error in item ";item%;"  (T)":END
  410ENDPROC
  420REM*********************************
  430DEF FNnerr(num$):IF INSTR(num$,"E")<>0 THEN =-1 ELSE =(STR$(VAL(num$))<>num
$)
  440REM*********************************
  450REM notes on AUTO-RUN-CONTROL INSTRUCTION syntax held in a BASIC DATA table
  460
  470REM It is important to note that an applications program will essentially m
ake use of this type of DATA in a logical sequential manner
  480REM The first instruction has syntax "#<time in seconds>" - At the applicat
ions program start the BASIC TIME clock is set to <time>*100 - An alternative fo
rm is "#?" in which case the BASIC clock is not interfered with
  490REM The "#" instruction is followed by an initial instruction sequence
  500REM Auto-reprogram instruction blocks should follow and comprise a "T" inst
ruction followed immediately by an instruction sequence - A "T" instruction has
syntax "T<time in seconds>"
  510REM At the program start and whenever the BASIC clock reaches a time held i
n a "T" instruction the applications program performs the instruction or instruc
tions which follow
  520REM Commas are generally used as separators in instruction sequences and th
e default instruction sequence is "X" (which does nothing)
  530REM The applications program will perform Ch-D system reprogramming on enco
untering a (Ch-D current)/(cell No) instruction
  540REM (Ch-D current)/(cell No) instructions have syntax - ".....,I<current>,<
cell No>,<cell No>,<cell No>,.....,I<current>,<cell No>,<cell No>,.....e.t.c....
.....,X"
  550REM An alternative syntax is ".....,<start cell No>-<end cell No>,....."
and the syntax forms can be mixed
  560REM Cases of (Ch-D current) instructions NOT followed by (cell No) instruct
ions are tolerated - applications programs will ignore these incomplete instruct
ion combinations
  570REM The applications program shuts down the Ch-D system on encountering an
end-of-program instruction - this has syntax "E" and should directly follow a "T
" instruction "T<end-time>"
  580REM The applications program will request an auto-measurement (by CHAIN'ing
 an appropriate BASIC program) upon encountering a measurement instruction
  590REM A measurement instruction has syntax "M<program name>" and must reside
between two "T" instructions
  600REM*********************************
  610REM DATA TABLE starts here
  620
  630REM example DATA appended below !!!!!
  640
  650DATA #0,I20,0,1,2,3,4,5,6,7,8,9,X
  660DATA T600,I0,0,1,2,3,4,5,6,7,8,9,X
  670DATA T1200,MMAF
  680DATA T1800,I236,0-9,X
  690DATA T2400,X
  700DATA T2800,MMAF,T2800,I216,0-4,X
  710DATA T3000,E
```

APPENDIX 6(f)

A Listing of Example BASIC Program : "DC_C_K"

Notes:-

- The program operates in B.B.C. BASIC MODE7 (Teletext mode).

- The program contains embedded Teletext graphics codes. For purposes of printability these have been replaced with "£" characters.

```
   10REM================================
   20prog$="DC_C_K":run$="RUN300"
   30REM================================
   40
   50MODE7:VDU15
   60
   70REM this is a controller program for graph-printer programs
   80
   90REM this program acts upon information held in its integral DATA table - th
is DATA must be sensibly set by the user before engaging on a graph-printing seq
uence
  100
  110REM this program uses resident variables I%,P% as program-consistency check
 parameters; J% as a control-prog./printer-prog. position-indicator and K%,L%,M%
,N%,O%,Q%,R%,S%,T%,U% to transfer parameters to graph-printer programs
  120
  130REM this program uses blocks &70-&87 and &88-&8F in zero-page to transfer t
wo text strings to printer-programs (of 24 and 8 characters max. respectively an
d comprising characters with ASC codes of 32-126)
  140
  150REM NOTE:- before engaging on a graph-printing sequence I% must be set to t
he RUN No and J% must be set to a sensible value (may be negative) BY THE USER!
  160
  170REM NOTE:- if I% is set to zero then this program will CHAIN itself repeate
dly as a method of checking its DATA table for item type
  180
  190REM NOTE:- the value of J% on entry to this program determines the start po
sition in the control-program/printer-program sequence
  200
  210REM================================
  220ON ERROR GOTO760
  230DIM data$(13):FOR X%=0 TO 5:data$(X%)="XXXXXXXXXXX":NEXT:data$(6)=STRING$(2
55,"X"):FOR X%=7 TO 12:data$(X%)="XXXXXXXXXXX":NEXT:data$(13)=STRING$(255,"X")
  240FOR X%=&70 TO &8F:?X%=0:NEXT:REM set zero-page locations &70-&8F to zeroes
(0 is the ASC null code)
  250IF (I%<>VAL(MID$(run$,4,10)) AND I%<>0) VDU7:PRINT"£ERROR:- program RUN num
ber inconsistent£with set value of I% !":VDU10:END
  260noteJ%=J%:REM note op-counter value on entry in case of program error
  270REM================================
  280header$=run$+STRING$((7-LEN(run$))," ")+CHR$(34)+prog$+CHR$(34)+STRING$((8-
LEN(prog$))," ")+"(last pos'n "+STR$(J%)+")"
  290CLS:VDU132,157,141:PRINT"£";header$
  300VDU132,157,141:PRINT"£";header$:VDU10
  310PRINT "£CURRENT PROGRAM CUSTOMIZATION LIST:-":PRINT"£(Hold SPACE BAR down n
ow to inspect)":VDU10
  320FOR X%=1 TO 6:READ data$(X%):NEXT:REM read the first 6 items in the DATA ta
ble into data$(1-6)
  330REPEAT:READ data$(0):FOR X%=7 TO 13:READ data$(X%):NEXT:UNTIL VAL(data$(0))
>J%:REM move to required block of DATA and store it in the rest of array data$
  340REM================================
  350REM check data$(0-13) for validity
  360FOR X%=0 TO 5:IF FNnerr(data$(X%)) VDU7:PRINT"££ERROR:- faulty fixed numeri
c DATA item":PRINT"££(may be due to missed/extra items)":VDU10:END ELSE NEXT
  370FOR X%=1 TO LEN(data$(6)):Z%=ASC(MID$(data$(6),X%,1)):IF (Z%<32 OR Z%>126)
VDU7:PRINT"££ERROR:- bad permanent-text DATA item":PRINT"££(only ASC codes 32-12
6 allowed)":VDU10:END ELSE NEXT
  380FOR X%=7 TO 12:IF FNnerr(data$(X%)) VDU7:PRINT"££ERROR:- faulty vari. numer
ic DATA item":PRINT"££(may be due to missed/extra items)":VDU10:END ELSE NEXT
```

```
  390FOR X%=1 TO LEN(data$(13)):Z%=ASC(MID$(data$(13),X%,1)):IF (Z%<32 OR Z%>126
) VDU7:PRINT"££ERROR:- bad variable-text DATA item":PRINT"££(only ASC codes 32-1
26 allowed)":VDU10:END ELSE NEXT
  400REM==============================
  410REM set the resident variables I%-U% and zero-page data block &80-&8F accor
ding to data$(0-11) and display their values
  420PRINT"£I%=";I%;TAB(15);"RUN No (as above)"
  430J%=VAL(data$(0)):PRINT" J%=";J%;TAB(15);"pos'n for current op'n"
  440VDU10
  450K%=VAL(data$(1)):PRINT"£K%=";K%;TAB(15);"fixed param. (numcels)"
  460L%=VAL(data$(2)):PRINT" L%=";L%;TAB(15);"fixed param. (celbloc)"
  470M%=VAL(data$(3)):PRINT"£M%=";M%;TAB(15);"fixed param. (acbloc)"
  480N%=VAL(data$(4)):PRINT" N%=";N%;TAB(15);"fixed param. (nummeas)"
  490O%=VAL(data$(5)):PRINT"£O%=";O%;TAB(15);"fixed param. (repeats)"
  500VDU10
  510IF LEN(data$(6))>24 THEN X%=24 ELSE X%=LEN(data$(6))
  520FOR Z%=1 TO X%:?(&6F+Z%)=ASC(MID$(data$(6),Z%,1)):NEXT
  530P%=VAL(data$(7)):PRINT" P%=";P%;TAB(15);"printer program type"
  540VDU10
  550Q%=VAL(data$(8)):PRINT"£Q%=";Q%;TAB(15);"vari. param. (cell No)"
  560R%=VAL(data$(9)):PRINT" R%=";R%;TAB(15);"vari. param. (repeat No)"
  570S%=VAL(data$(10)):PRINT"£S%=";S%;TAB(15);"vari. param. (?)"
  580T%=VAL(data$(11)):PRINT" T%=";T%;TAB(15);"vari. param. (?)"
  590U%=VAL(data$(12)):PRINT"£U%=";U%;TAB(15);"vari. param. (?)"
  600IF LEN(data$(13))>8 THEN X%=8 ELSE X%=LEN(data$(13))
  610FOR Z%=1 TO X%:?(&87+Z%)=ASC(MID$(data$(13),Z%,1)):NEXT
  620VDU10
  630PRINT"£";LEFT$((data$(6)+STRING$(24," ")),24);" / ";LEFT$((data$(13)+STRING
$(8," ")),8)
  640REM==============================
  650REM the program may be paused here by pressing and holding down the space b
ar in order to inspect the text just printed
  660*FX15,1
  670REPEAT:UNTIL NOT INKEY(-99)
  680REM==============================
  690IF I%=0 THEN CHAIN "DRIVER":REM I%=0 sets this program into a self-checking
 mode
  700REM CHAIN a selected graph-printer program (any printer-program may be sele
cted by the following routine but note that every one should CHAIN this controll
er-program upon termination)
  710IF P%=0 THEN CHAIN "ALPHA" ELSE IF P%=1 THEN CHAIN "BETA" ELSE IF P%=2 THEN
 CHAIN "GAMMA" ELSE IF P%=3 THEN CHAIN "DELTA" ELSE END
  720REM==============================
  730REM******************************
  740DEF FNnerr(num$):IF INSTR(num$,"E")<>0 THEN =-1 ELSE =(STR$(VAL(num$))<>num
$)
  750REM******************************
  760REM ERROR ROUTINE
  770VDU7:J%=noteJ%
  780IF ERR=15 PRINT"£ERROR:- too many DATA items per section£or missing section
 terminator ";CHR$(34);"E";CHR$(34);"?":VDU10 ELSE REPORT:PRINT" AT LINE ";ERL
  790END
  800REM******************************
  810REM DATA table starts here:-
  820
  830DATA 48,54,10,2,0,"(2,8Hz)"
  840
  850DATA   0,0,0,0,0,0,0,"S9"
```

```
 860DATA  10,0,1,0,0,0,0,"S10"
 870DATA  20,0,2,0,0,0,0,"S11"
 880DATA  30,0,3,0,0,0,0,"S12"
 890DATA  40,0,4,0,0,0,0,"S13"
 900DATA  50,0,5,0,0,0,0,"S14"
 910DATA  60,0,6,0,0,0,0,"S15"
 920DATA  70,0,7,0,0,0,0,"S16"
 930DATA  80,0,8,0,0,0,0,"S17"
 940DATA  90,0,9,0,0,0,0,"S18"
 950DATA  100,0,10,0,0,0,0,"S19"
 960DATA  110,0,11,0,0,0,0,"S20"
 970DATA  120,0,12,0,0,0,0,"S21"
 980DATA  130,0,13,0,0,0,0,"S22"
 990DATA  140,0,14,0,0,0,0,"S23"
1000DATA  150,0,15,0,0,0,0,"S24"
1010DATA  160,0,16,0,0,0,0,"S25"
1020DATA  170,0,17,0,0,0,0,"S26"
1030DATA  180,0,18,0,0,0,0,"S27"
1040DATA  190,0,19,0,0,0,0,"S28"
1050DATA  200,0,20,0,0,0,0,"S29"
1060DATA  210,0,21,0,0,0,0,"S30"
1070DATA  220,0,22,0,0,0,0,"S31"
1080DATA  230,0,23,0,0,0,0,"S32"
1090DATA  240,0,24,0,0,0,0,"S33"
1100DATA  250,0,25,0,0,0,0,"S34"
1110DATA  260,0,26,0,0,0,0,"S35"
1120DATA  270,0,27,0,0,0,0,"S36"
1130DATA  280,0,28,0,0,0,0,"S37"
1140DATA  290,0,29,0,0,0,0,"S38"
1150DATA  300,0,30,0,0,0,0,"S39"
1160DATA  310,0,31,0,0,0,0,"S40"
1170DATA  320,0,32,0,0,0,0,"S41"
1180DATA  330,0,33,0,0,0,0,"S42"
1190DATA  340,0,34,0,0,0,0,"S43"
1200DATA  350,0,35,0,0,0,0,"S44"
1210DATA  360,0,36,0,0,0,0,"S45"
1220DATA  370,0,37,0,0,0,0,"S46"
1230DATA  380,0,38,0,0,0,0,"PP18"
1240DATA  390,0,39,0,0,0,0,"PP12"
1250DATA  400,0,40,0,0,0,0,"PP5"
1260DATA  410,0,41,0,0,0,0,"PP3"
1270DATA  420,0,42,0,0,0,0,"PP2"
1280DATA  430,0,43,0,0,0,0,"PP13"
1290DATA  440,0,44,0,0,0,0,"PP7"
1300DATA  450,0,45,0,0,0,0,"PP15"
1310DATA  460,0,46,0,0,0,0,"PP4"
1320DATA  470,0,47,0,0,0,0,"PP16"
1330
1340
1350DATA  1000,2,0,0,0,0,0,"S9"
1370DATA  1010,2,0,0,0,0,0,"S10"
1380DATA  1020,2,2,0,0,0,0,"S11"
1390DATA  1030,2,3,0,0,0,0,"S12"
1400DATA  1040,2,4,0,0,0,0,"S13"
1410DATA  1050,2,5,0,0,0,0,"S14"
1420DATA  1060,2,6,0,0,0,0,"S15"
1430DATA  1070,2,7,0,0,0,0,"S16"
1440DATA  1080,2,8,0,0,0,0,"S17"
```

```
1450DATA  1090,2,9,0,0,0,0,"S18"
1460DATA  1100,2,10,0,0,0,0,"S19"
1470DATA  1110,2,11,0,0,0,0,"S20"
1480DATA  1120,2,12,0,0,0,0,"S21"
1490DATA  1130,2,13,0,0,0,0,"S22"
1500DATA  1140,2,14,0,0,0,0,"S23"
1510DATA  1150,2,15,0,0,0,0,"S24"
1520DATA  1160,2,16,0,0,0,0,"S25"
1530DATA  1170,2,17,0,0,0,0,"S26"
1540DATA  1180,2,18,0,0,0,0,"S27"
1550DATA  1190,2,19,0,0,0,0,"S28"
1560DATA  1200,2,20,0,0,0,0,"S29"
1570DATA  1210,2,21,0,0,0,0,"S30"
1580DATA  1220,2,22,0,0,0,0,"S31"
1590DATA  1230,2,23,0,0,0,0,"S32"
1600DATA  1240,2,24,0,0,0,0,"S33"
1610DATA  1250,2,25,0,0,0,0,"S34"
1620DATA  1260,2,26,0,0,0,0,"S35"
1630DATA  1270,2,27,0,0,0,0,"S36"
1640DATA  1280,2,28,0,0,0,0,"S37"
1650DATA  1290,2,29,0,0,0,0,"S38"
1660DATA  1300,2,30,0,0,0,0,"S39"
1670DATA  1310,2,31,0,0,0,0,"S40"
1680DATA  1320,2,32,0,0,0,0,"S41"
1690DATA  1330,2,33,0,0,0,0,"S42"
1700DATA  1340,2,34,0,0,0,0,"S43"
1710DATA  1350,2,35,0,0,0,0,"S44"
1720DATA  1360,2,36,0,0,0,0,"S45"
1730DATA  1370,2,37,0,0,0,0,"S46"
1740DATA  1380,2,38,0,0,0,0,"PP18"
1750DATA  1390,2,39,0,0,0,0,"PP12"
1760DATA  1400,2,40,0,0,0,0,"PP5"
1770DATA  1410,2,41,0,0,0,0,"PP3"
1780DATA  1420,2,42,0,0,0,0,"PP2"
1790DATA  1430,2,43,0,0,0,0,"PP13"
1800DATA  1440,2,44,0,0,0,0,"PP7"
1810DATA  1450,2,45,0,0,0,0,"PP15"
1820DATA  1460,2,46,0,0,0,0,"PP4"
1830DATA  1470,2,47,0,0,0,0,"PP16"
1840
1850
1860DATA  2000,3,0,0,0,0,0,"S9":
1871DATA  2010,3,1,0,0,0,0,"S10"
1890DATA  2020,3,2,0,0,0,0,"S11"
1900DATA  2030,3,3,0,0,0,0,"S12"
1910DATA  2040,3,4,0,0,0,0,"S13"
1920DATA  2050,3,5,0,0,0,0,"S14"
1930DATA  2060,3,6,0,0,0,0,"S15"
1940DATA  2070,3,7,0,0,0,0,"S16"
1950DATA  2080,3,8,0,0,0,0,"S17"
1960DATA  2090,3,9,0,0,0,0,"S18"
1970DATA  1100,3,10,0,0,0,0,"S19"
1980DATA  1110,3,11,0,0,0,0,"S20"
1990DATA  1120,3,12,0,0,0,0,"S21"
2000DATA  2130,3,13,0,0,0,0,"S22"
2010DATA  2140,3,14,0,0,0,0,"S23"
2020DATA  2150,3,15,0,0,0,0,"S24"
2030DATA  2160,3,16,0,0,0,0,"S25"
```

```
2040DATA  2170,3,17,0,0,0,0,"S26"
2050DATA  2180,3,18,0,0,0,0,"S27"
2060DATA  2190,3,19,0,0,0,0,"S28"
2070DATA  2200,3,20,0,0,0,0,"S29"
2080DATA  2210,3,21,0,0,0,0,"S30"
2090DATA  2220,3,22,0,0,0,0,"S31"
2100DATA  2230,3,23,0,0,0,0,"S32"
2110DATA  2240,3,24,0,0,0,0,"S33"
2120DATA  2250,3,25,0,0,0,0,"S34"
2130DATA  2260,3,26,0,0,0,0,"S35"
2140DATA  2270,3,27,0,0,0,0,"S36"
2150DATA  2280,3,28,0,0,0,0,"S37"
2160DATA  2290,3,29,0,0,0,0,"S38"
2170DATA  2300,3,30,0,0,0,0,"S39"
2180DATA  2310,3,31,0,0,0,0,"S40"
2190DATA  2320,3,32,0,0,0,0,"S41"
2200DATA  2330,3,33,0,0,0,0,"S42"
2210DATA  2340,3,34,0,0,0,0,"S43"
2220DATA  2350,3,35,0,0,0,0,"S44"
2230DATA  2360,3,36,0,0,0,0,"S45"
2240DATA  2370,3,37,0,0,0,0,"S46"
2250DATA  2380,3,38,0,0,0,0,"PP18"
2260DATA  2390,3,39,0,0,0,0,"PP12"
2270DATA  2400,3,40,0,0,0,0,"PP5"
2280DATA  2410,3,41,0,0,0,0,"PP3"
2290DATA  2420,3,42,0,0,0,0,"PP2"
2300DATA  2430,3,43,0,0,0,0,"PP13"
2310DATA  2440,3,44,0,0,0,0,"PP7"
2320DATA  2450,3,45,0,0,0,0,"PP15"
2330DATA  2460,3,46,0,0,0,0,"PP4"
2340DATA  2470,3,47,0,0,0,0,"PP16"
```

APPENDIX 6(g)

A Listing of Example BASIC Program "GAMMA"

Notes:-

- The program operates in B.B.C. BASIC MODE7 (Teletext mode).

- The program contains embedded Teletext graphics codes. For purposes of printability these have been replaced with "£" characters.

```
  10REM================================
  20prog$="GAMMA":prog%=2:axes$="TYPE4"
  30REM================================
  40
  50MODE7:VDU15
  60
  70REM this is a "CHOUND" program with graph axes of above type - this program
 CHAINs "DRIVER" upon termination or error
  80
  90REM NOTE:- this program requires data from a currently open file whose chan
nel number has been placed in resident variable E%
 100
 110REM THIS PROGRAM PLOTS A VERY HIGH RESOLUTION GRAPH USING A SUITABLE EPSON-
COMPATIBLE PRINTER (works with an EPSON LX-86)
 120
 130REM this program uses a "basic co-ordinate" system which simply comprises a
n X,Y dot count (of printer dots) from the printed graph origin - variables x% a
nd y% are used to keep track of print-head position in basic co-ords
 140
 150REM================================
 160IF P%<>prog% PRINT"£ERROR:- program type inconsistent with £set value of P%
 !":VDU10:FOR X%=0 TO 19:VDU7:Z%=TIME:REPEAT:UNTIL TIME>=Z%+75:NEXT:PROCEND:REM
check program type with that requested by the controller-program
 170ON ERROR GOTO1980
 180REM================================
 190::::::::::::::::::::::::::::::::::
 200REM SPECIAL INITIALISATIONS AND INSTRUCTIONS IN PARTICULAR PROGRAM CASES AR
E DONE HERE via "PROCinit"
 210::::::::::::::::::::::::::::::::::
 220PROCinit
 230REM================================
 240::::::::::::::::::::::::::::::::::
 250REM USER-SET PARAMETERS FOLLOW
 260::::::::::::::::::::::::::::::::::
 270REM printer graphics mode (0-6) :-
 280GRmode%=4:REM one-to-one mode
 290
 300REM usable width of paper in dots (depends on printer and mode) :-
 310GRwidth%=640
 320
 330REM AXIS-PRINTING INSTRUCTIONS (values in basic co-ords) .......
 340
 350REM (length),(interval between markers),(position of first marker) :-
 360REM (problems may occur if Xdiv%<7)
 370Yax%=600:Ydiv%=10:firstYmk%=0
 380Xax%=1467:Xdiv%=10:firstXmk%=0
 390
 400REM annotation points of axes (interval),(position of first) :-
 410REM (give firstAnnX% a large +ve value if X axis annotation is not desired)
 420REM (give firstAnnY% a negative value if Y axis annotation is not desired)
 430firstAnnX%=0:AnnXdiv%=30
 440firstAnnY%=0:AnnYdiv%=50
 450
 460REM left-hand margin size:-
 470Lmarg%=18
 480
 490REM offset (leftwards) for Y axis labels:-
 500Annofs%=7
```

```
  510
  520REM DATA ADJUSTMENT AND SCALING FACTORS.......
  530
  540REM data is obtained via functions FNXco and FNYco and is then adjusted usi
ng an algorithm (X case shown here) :-  Xco%=INT((FNXco+Xadj)*Xscale+Xoffs%+0.5)
  550
  560REM (real number) values to be added to raw (unscaled) data:-
  570Xadj=0
  580Yadj=0
  590
  600REM (real number) values to multiply data after additive adjustment:-
  610Xscale=1
  620Yscale=50
  630
  640REM values to be added to data after scaling (in integer basic co-ords) :-
  650Xoffs%=0
  660Yoffs%=0
  670REM==============================
  680REM initialise screen display
  690header$="printer "+CHR$(34)+prog$+CHR$(34)+" - "+axes$+" axes"
  700CLS:VDU132,157,141:PRINT"£"+header$:VDU132,157,141:PRINT"£"+header$:VDU10
  710PRINT" CURRENT GRAPH TITLE (truncated) :-":VDU10
  720PRINT"£";LEFT$(FNTITLESTRING,38):VDU10
  730PRINT" CURRENT (Xco%,Yco%) is £(      ,      )":VDU10
  740PRINT"£LOWEST  X co-ord found =":VDU10:PRINT"£HIGHEST X co-ord found =":VDU
10
  750PRINT"£LOWEST  Y co-ord found =":VDU10:PRINT"£HIGHEST Y co-ord found =":VDU
10
  760PRINT"£No OF -VE OVERLOADS    =":VDU10:PRINT"£No OF +VE OVERLOADS    =":VDU
10
  770PRINT"£No OF BAD X CO-ORDS    ="
  780VDU23,1,0;0;0;0;:REM cursor off
  790REM==============================
  800*FX3,10
  810VDU27,64,15:REM initialise printer and set condensed characters
  820REM set printer ignore character to 255:-
  830*FX6,255
  840REM essential initialisations
  850x%=0:Xmark%=firstXmk%:AnnX%=firstAnnX%:AnnY%=firstAnnY%
  860Xco%=0:REM required for the first use of the Xco% checking procedure
  870LOX%=999999999:LOY%=999999999:REM unlikely high values
  880HIX%=-999999999:HIY%=-999999999:REM unlikely low values
  890NLO%=0:NHI%=0:BADX%=0
  900REM==============================
  910PRINT FNTITLESTRING;:VDU10
  920REM==============================
  930VDU10:REM another linefeed (which will ensure that the printer takes up the
 paper feed properly in preparation for the graphics)
  940REM==============================
  950IF (AnnY%>=0 AND NOT INKEY(-69)) PROCAnnY ELSE VDU10:REM Y-axis annotation
(but will be skipped over if the "Y" key is depressed - this saves time when tes
ting programs)
  960REM==============================
  970REM plot Y axis with division markers at intervals and also plot an X marke
r at the origin if required
  980IF Yax%>(GRwidth%-1-8-Lmarg%) VDU7:Yax%=(GRwidth%-1-8-Lmarg%):REM ensure th
at the Y axis is not too long
  990code%=(Lmarg%+8+1+Yax%):PROCRESGB
```

```
 1000IF Lmarg%<>0 FOR Z%=1 TO Lmarg%:VDU0:NEXT:REM margin
 1010IF Xmark%=0 THEN byte%=2:Xmark%=Xmark%+Xdiv% ELSE byte%=0
 1020VDU0:FOR Z%=0 TO 4:VDU(byte%):NEXT:VDU0,0:REM possible X marker but leave a
 good space for clarity at the origin
 1030y%=0:IF (y%-firstYmk%) MOD Ydiv%=0 VDU(16+32+64+128) ELSE VDU0:REM possible
 Y marker but leave a good space at the origin for clarity
 1040FOR y%=1 TO Yax%
 1050IF (y%-firstYmk%) MOD Ydiv%=0 VDU(2+8+16+32+64+128) ELSE VDU2:REM Y axis/ma
rkers
 1060NEXT
 1070VDU27,65,0,10:REM 0-dot linefeed
 1080REM==============================
 1090REM get the next basic co-ordinate pair (and call it the "current" pair) an
d update the screen display as appropriate
 1100*FX3,0
 1110Z%=FNXADSC(FNXco):W%=FNYADSC(FNYco)
 1120IF Z%<LOX% LOX%=Z%:PRINT TAB(26,9);Z%;"           ";
 1130IF Z%>HIX% HIX%=Z%:PRINT TAB(26,11);Z%;"           ";
 1140IF W%<LOY% LOY%=W%:PRINT TAB(26,13);W%;"           ";
 1150IF W%>HIY% HIY%=W%:PRINT TAB(26,15);W%;"           ";
 1160IF Z%<Xco% VDU7:BADX%=BADX%+1:PRINT TAB(26,21);BADX%:GOTO1100 ELSE Xco%=Z%:
Yco%=W%:REM reject the co-ordinate pair if the current X co-ord is smaller than
the previous one
 1170IF Yco%<(-Lmarg%-8+1) VDU7:NLO%=NLO%+1:PRINT TAB(26,17);NLO%:Yco%=(-Lmarg%-
8+1):OVLD%=-1 ELSE OVLD%=0:REM act if Yco% is too low
 1180IF Yco%>(GRwidth%-1-Lmarg%-8-1) VDU7:NHI%=NHI%+1:PRINT TAB(26,19);NHI%:Yco%
=(GRwidth%-1-Lmarg%-8-1):OVLD%=1:REM act if Yco% is too high
 1190PRINT TAB(25,7);"(     ,     )     ";TAB(26,7);Xco%;TAB(32,7);Yco%;TAB(0,22
);
 1200*FX3,10
 1210REPEAT:UNTIL NOT INKEY(-99):REM holding down the SPACE-BAR pauses the progr
am here
 1220REM==============================
 1230REM the X axis is plotted in sections until less than 7 dots from the curre
nt X co-ordinate or until less than 4 dots from the current X-annotation point o
r until the end of the X axis
 1240IF x%>Xax% PROCEND
 1250IF NOT ((Xco%-x%)<7 OR (AnnX%-x%)<4) GOTO1270
 1260IF Xco%>=(AnnX%+3) THEN PROCAnnX:GOTO1240 ELSE GOTO1380
 1270REPEAT:VDU27,65,7,10:x%=x%+7:REM 7-dot linefeed
 1280code%=(Lmarg%+8+1):PROCRESGB
 1290IF Lmarg%<>0 FOR Z%=1 TO Lmarg%:VDU0:NEXT:REM margin
 1300IF Xmark%<=x% THEN byte%=2*2^(x%-Xmark%):Xmark%=Xmark%+Xdiv% ELSE byte%=0
 1310VDU0:FOR Z%=0 TO 5:VDU(byte%):NEXT:VDU0:REM possible X marker
 1320VDU(2+4+8+16+32+64+128):REM 7-dots of X axis
 1330UNTIL ((Xco%-x%)<7 OR (AnnX%-x%)<4 OR x%>Xax%)
 1340IF x%>Xax% PROCEND
 1350IF Xco%>=(AnnX%+3) THEN PROCAnnX:GOTO1240
 1360IF x%=Xco% GOTO1480:REM jump the next section from here if possible
 1370REM==============================
 1380REM plot the remaining bit of X axis up to the current point's X position
 1390Xtra%=(Xco%-x%)
 1400IF (Xtra%=0 AND Yco%>=(y%+1)) GOTO1500:REM if feasible then plot several po
ints having identical X co-ords without intervening linefeeds - check that the p
rinter hardware can cope with this method
 1410IF Xtra%=0 GOTO1480
 1420IF Xtra%<>0 VDU27,65,Xtra%,10:x%=Xco%:REM a calculated linefeed to achieve
the X position
```

```
1430code%=(Lmarg%+8+1):PROCRESGB
1440IF Lmarg%<>0 FOR Z%=1 TO Lmarg%:VDU0:NEXT:REM margin
1450IF Xmark%<=x% THEN byte%=2*2^(x%-Xmark%):Xmark%=Xmark%+Xdiv% ELSE byte%=0
1460VDU0:FOR Z%=0 TO 5:VDU(byte%):NEXT:VDU0:REM possible X marker
1470VDU2*((2^Xtra%)-1):REM extra X axis dots
1480VDU27,65,0,10:y%=(-Lmarg%-8):REM 0-dot linefeed and reset y%
1490REM==============================
1500REM now act upon the Y co-ordinate and plot the point
1510code%=(Yco%-y%+1+1):PROCRESGB
1520IF Yco%<>(y%+1) FOR Z%=1 TO (Yco%-y%-1):VDU0:NEXT:REM effectively a calcula
ted move in the Y direction
1530IF OVLD%<>0 PROCSQUARE ELSE PROCCROSS
1540y%=Yco%+2:REM print head Y position is now thus
1550REM==============================
1560GOTO1100:REM loop back
1570REM==============================
1580REM**********************************
1590DEF PROCRESGB:LOCAL lo%,hi%
1600lo%=(code% MOD 256):hi%=(code% DIV 256)
1610REM we must avoid the printer-ignore-character mechanism thus:-
1620IF (lo%<>255 AND hi%<>255) THEN GOTO1640 ELSE *FX6,254
1630IF (lo%<>254 AND hi%<>254) THEN GOTO1640 ELSE *FX6,253
1640VDU27,42,GRmode%,lo%,hi%:REM reserve graphics bytes
1650REM reset printer-ignore-char:-
1660*FX6,255
1670ENDPROC
1680REM**********************************
1690DEF PROCAnnY:LOCAL Z%
1700REPEAT:code%=(Lmarg%+8+1+AnnY%-Annofs%):PROCRESGB
1710IF code%<>0 THEN FOR Z%=1 TO code%:VDU0:NEXT
1720PRINT FNannY;:VDU27,65,0,10
1730AnnY%=AnnY%+AnnYdiv%
1740UNTIL AnnY%>=Yax%
1750VDU27,65,12,10:ENDPROC
1760REM**********************************
1770DEF PROCAnnX:LOCAL Z%
1780Xtra%=(AnnX%-x%+3)
1790VDU27,65,Xtra%,10:x%=(AnnX%+3)
1800code%=(Lmarg%+8+1):PROCRESGB
1810IF Lmarg%<>0 FOR Z%=1 TO Lmarg%:VDU0:NEXT
1820IF Xmark%<=x% THEN byte%=2*2^(x%-Xmark%):Xmark%=Xmark%+Xdiv% ELSE byte%=0
1830VDU0:FOR Z%=0 TO 5:VDU(16 AND byte%):NEXT:VDU0:REM annotation marker (using
a fixed print-head pin) and possibly a normal marker also
1840VDU2*((2^Xtra%)-1):REM extra X axis dots requred
1850VDU27,65,0,10:REM 0-dot linefeed
1860PRINT FNannX;:VDU27,65,0,10:y%=(-Lmarg%-8):REM must reset y%
1870AnnX%=AnnX%+AnnXdiv%:REM increment AnnX%
1880ENDPROC
1890REM**********************************
1900DEF FNXADSC(Z)=INT((Z+Xadj)*Xscale+Xoffs%+0.5)
1910REM**********************************
1920DEF FNYADSC(Z)=INT((Z+Yadj)*Yscale+Yoffs%+0.5)
1930REM**********************************
1940DEF PROCCROSS:VDU(2):VDU(1+2+4):VDU(2):ENDPROC:REM a small cross
1950REM**********************************
1960DEF PROCSQUARE:VDU(1+2+4):VDU(1+4):VDU(1+2+4):ENDPROC:REM a small square
1970REM**********************************
1980REM ERROR ROUTINE
```

```
 1990IF (ERR<>42 AND ERR<>223) GOTO2010 ELSE *FX3,10
 2000VDU7,7:Xco%=999999999:Yco%=999999999:GOTO1240:REM ignore "Out of DATA" or "
End of file" errors to allow graph axes to be fully printed even if the program
runs out of input data from a DATA TABLE or disk
 2010*FX3,0
 2020VDU7:IF ERR=214 VDU10:PRINT"ÉÉERROR:- ";CHR$(34);"DRIVER";CHR$(34);" not fo
und":END:REM "File not found" error which might occur in "PROCEND"
 2030REM disable ESCAPE key here:-
 2040*FX229,1
 2050REPORT:PRINT" at line ";ERL:PRINT TAB(0,24);CHR$(129);CHR$(157);"ÉÉ** WAIT:
- PRINTER BEING RESET! ** ";
 2060*FX3,10
 2070FOR Z%=0 TO 500:VDU0,0,0,0,0:NEXT:REM if the program has been interrupted a
nd the printer is currently expecting graphics bytes then this routine will in m
ost cases take the printer back into normal mode with no side-effects
 2080*FX3,0
 2090PRINT TAB(0,24);STRING$(39," ");:PRINT TAB(0,23);STRING$(39," ");:PRINT TAB
(0,22);
 2100REM re-enable ESCAPE key now:-
 2110*FX229,0
 2120PROCEND
 2130REM*********************************
 2140DEF PROCEND:*FX3,10
 2150VDU12,27,64:REM do a form-feed and then re-initialise the printer
 2160*FX3,0
 2170VDU23,1,1;0;0;0;
 2180*FX6,10
 2190*FX15,1
 2200CHAIN"DRIVER"
 2210REM*********************************
 2220:::::::::::::::::::::::::::::::::::
 2230REM USER-DEFINED AXIS-ANNOTATION ALGORITHMS (specific to this program) FOLL
OW (note that annotation points are always at constant spacings)
 2240:::::::::::::::::::::::::::::::::::
 2250DEF FNannX:LOCAL Z$
 2260IF AnnX%<=480 THEN Z$=STR$(AnnX%) ELSE IF AnnX%<=960 THEN Z$=STR$((AnnX%-48
0)/2+480) ELSE IF AnnX%<=1440 THEN Z$=STR$((AnnX%-960)+720) ELSE Z$=STR$((AnnX%-
1440)/2+1200)
 2270=STRING$(4-LEN(Z$)," ")+Z$
 2280REM.............................
 2290DEF FNannY:LOCAL Z$
 2300Z$=STR$(AnnY% DIV Yscale)+"F"
 2310IF LEN(Z$)=2 THEN =" "+Z$ ELSE =Z$
 2320REM*********************************
 2330:::::::::::::::::::::::::::::::::::
 2340REM USER-DEFINED FUNCTIONS (specific to this program type) FOLLOW
 2350:::::::::::::::::::::::::::::::::::
 2360DEF FNTITLESTRING:LOCAL X%,X$,Z$
 2370FOR X%=&70 TO &87:X$=X$+CHR$(?X%):NEXT
 2380X%=INSTR(X$,CHR$(0)):IF X%<>0 THEN X$=LEFT$(X$,X%-1)
 2390FOR X%=&88 TO &8F:Z$=Z$+CHR$(?X%):NEXT
 2400X%=INSTR(Z$,CHR$(0)):IF X%<>0 THEN Z$=LEFT$(Z$,X%-1)
 2410="RUN "+STR$(I%)+" CELL "+STR$(Q%)+" (CELL "+Z$+") CAPACITANCES AT FREQUENC
IES "+X$
 2420REM.............................
 2430DEF PROCinit:numcels%=K%:celbloc%=L%:acbloc%=M%:nummeas%=N%:repnum%=O%:user
ep%=R%
 2440DIM st%(celbloc%*numcels%-1):PTR#E%=0:A%=-1:scale=5.13192954E-6:ENDPROC
```

```
 2450REM.............................
 2460DEF FNXco:LOCAL Z%:A%=A%+1:IF (A% MOD nummeas%)=0 THEN FOR Z%=0 TO (celbloc
%*numcels%-1):st%(Z%)=BGET#E%:NEXT
 2470Z%=(A% DIV nummeas%):IF Z%<=48 THEN =10*Z% ELSE IF Z%<=72 THEN =20*(Z%-48)+
480 ELSE IF Z%<=120 THEN =10*(Z%-72)+960 ELSE =20*(Z%-120)+1440
 2480REM.............................
 2490DEF FNYco:LOCAL X,F%,ofs%:ofs%=(celbloc%*Q%)+acbloc%*(A% MOD nummeas%):X=sc
ale*2^st%(5+ofs%)*(((256*256*st%(11+ofs%)+256*st%(10+ofs%)+st%(9+ofs%))/512)-163
84)
 2500IF X=0 THEN =-9999/Yscale ELSE F%=st%(4+ofs%):=1/(2*PI*2^(7-(F% AND 127)/8)
/(1+(F% AND 128)/256)*X)
 2510REM.............................
```

APPENDIX 7

A Listing of the J.P.B./U.C.S. Charger Provisional User Manual (Version 1.0)

J.P.B./U.C.S. INTELLIGENT CHARGER FOR PYE PFX 600mAh BATTERIES

PROVISIONAL USER MANUAL (Version 1.0 - January 1990)

- containing full operational instructions and brief details of important charger characteristics.

Important note:- The prototype charger has charge current rates and internal thresholds set for use with 600mAh batteries only!

(A) NOTE ON CONTROL BUTTONS:-

The charger has a yellow "UPDATE" button and a red "RESET" button. In normal operation only the "UPDATE" button is used regularly - see (B) and (C). The "RESET" BUTTON may occasionally be required for purposes (D) and (E) but has additional functions for setting charger mode/status - see (G).

(B) HOW TO CHARGE OR TOP-UP A BATTERY:-

The charger will accept and charge in an automatically-controlled manner batteries of any initial charge state. Even batteries which are already 100 per cent charged will not be harmed if placed into the charger. Batteries may be placed individually into the charger at any time as each is treated independently (the charger is not a "batch"-type charger).

The following procedure (a)-(d) should be taught to and adopted by all general charger users. However, strictly speaking, it is permissable to insert any number of batteries at any time into the charger provided that no battery is ever inserted into a socket for which the associated charging-status LED (lamp) is lit. Note that the "RESET" button must not be depressed whilst choosing suitable sockets as it suppresses normal LED displays!

At 1-minute intervals the charger does an automatic operation similar to that produced when the "UPDATE" button is pressed. Hence, if a user omits to press the "UPDATE" button after inserting batteries then the batteries will be accepted (if not faulty) automatically by the charger within a minute period.

Often the charger will perform an automatic "Update" operation whilst a user is in the process of inserting a battery or batteries. The user should be advised that this is of no detrimental consequence. It should be noted that the yellow-flash sequence of LEDs during an "Update" operation (manual or automatic) should not be interpreted as indicating any LED to be "lit or flashing" for purposes of stage (b) of the insertion process.

(a) - FIRSTLY FIND AN EMPTY BATTERY CHARGING SOCKET (REMOVE ANY FULLY CHARGED BATTERY IF NECESSARY TO FREE A SOCKET)

(b) - IF THE SELECTED CHARGING SOCKET HAS ITS LED (LAMP) LIT OR FLASHING THEN PRESS THE "UPDATE" BUTTON AND WAIT UNTIL THE LED IS EXTINGUISHED. NEVER PLACE A BATTERY INTO AN EMPTY SOCKET WHILST IT DISPLAYS A LIT OR FLASHING LED!

(c) - THEN PLACE THE BATTERY TO BE CHARGED OR TOPPED-UP INTO THE SELECTED SOCKET. IT IS PERMISSABLE TO INSERT SEVERAL BATTERIES AT THIS STAGE PROVIDED THAT EACH BATTERY IS INSERTED INTO A SOCKET FOR WHICH THE ASSOCIATED LED IS EXTINGUISHED

(d) - THEN PRESS THE "UPDATE" BUTTON AGAIN AND CHECK THAT THE LED FOR THE SELECTED BATTERY SOCKET BECOMES LIT FLASHING-RED - IF IT DOES NOT LIGHT WITHIN A FEW MINUTES THEN THE BATTERY MAY BE FAULTY AND SHOULD BE REMOVED FOR EVALUATION

(C) WHEN TO REMOVE BATTERIES:-

The charge process is optimised for use with an 8-hour shift system of battery usage. Charging takes place in two phases which are timed independently for each battery present in the charger.

In the first phase (the "Fast-Charge" phase) each battery is supplied with a charge current at the "C/2.5" rate until the charger determines that the battery is nearing the fully-charged state; this stage may take between 20 minutes and 4 hours.

In the second charging phase (the "Top-Up" phase) each battery is supplied with a current at the "C/10" rate which "tops-up" remaining uncharged capacity. After a period of one hour from the start of the "Top-Up" phase the LED (lamp) associated with a battery is switched from flashing-red to continuous-green at which point the battery will generally be at least 90 per cent charged, which is adequate for most purposes. However, it is preferential to leave each battery on charge for as long as possible after its LED becomes green so that as much of the remaining uncharged capacity becomes charged (this may benefit the long-term performance of batteries as well as their immediate charge states).

It should be noted that the "Top-Up" phase is limited to a maximum of 3 hours after which any battery, if left in the charger, will be subjected to an indefinite "Maintenance" charge at the "C/40" rate which will maintain its fully-charged state for a very long period without causing significant deterioration of battery performance.

For practical purposes the following instructions should be taught to and observed by general charger users. It is not essential to press the "UPDATE" button after removing batteries but this operation will leave the charger LED display in a 'tidy' state.

- WHEN A BATTERY BECOMES SUFFICIENTLY CHARGED FOR USE THEN THE LED (LAMP) FOR ITS SOCKET BECOMES LIT CONTINUOUS-GREEN AND THE BATTERY MAY BE REMOVED. IT IS ADVISABLE THOUGH TO LEAVE BATTERIES IN THE CHARGER FOR AS LONG AS POSSIBLE (THEY WILL NOT BE DAMAGED). IT IS GOOD PRACTISE TO PRESS THE "UPDATE" BUTTON AFTER REMOVING A BATTERY OR GROUP OF BATTERIES!

(D) PRIMARY FUNCTION OF THE "RESET" BUTTON:-

On initial powerup and on startup after long periods during which mains power has not been supplied to the charger then the charger will enter "Unset" mode. In this mode the charger will produce a repetitive beep sound and repeatedly flash its "RESET" button as a warning and will supply an indefinite "C/10"-rate current to all battery sockets (which is sufficient to charge batteries in 14-16 hours and should not cause serious battery degradation even if continued for several weeks).

"Unset" mode is cancelled by pressing the "RESET" button for about half a second, whereupon the charger will enter its normal "Intelligent-Charge" mode.

For practical purposes the following instructions should be taught to and observed by general charger users.

UPON CONNECTION OF MAINS POWER TO THE CHARGER AFTER AN EXTENDED PERIOD THE CHARGER MAY REPEATEDLY BEEP AND FLASH ITS "RESET" BUTTON. TO CANCEL THE WARNING SIGNAL AND ALLOW NORMAL CHARGER OPERATION THE "RESET" BUTTON MUST BE PRESSED FOR ABOUT HALF A SECOND

(E) THE "BAD-BATTERY" LED. (LAMP):-

The charger has an ability to identify batteries suffering certain serious faults. The charging process involves monitoring of certain battery parameters (which may be extended in future charger versions) and includes on on-load battery voltage test. If any battery is determined by the charger to be faulty (which, as the charger is a prototype may not be a wholly accurate determination) then the "BAD-BATTERY" LED (lamp) will become lit flashing-red.

If the "BAD-BATTERY" LED is seen by a battery user to become lit then the situation should be reported to the system supervisor. The system supervisor (or any other person authorised to deal with "bad-battery" situations) should identify any suspect battery or batteries and remove them for testing.

The identification process involves pressing and continuously holding down the "RESET" button whilst the charger is in normal operation (with mains power applied). The charger will then operate in "IDENTIFY" mode in which any battery determined by the charger to be "BAD" will have its charging-status LED (lamp) lit rapid-flashing-yellow whilst every other battery will have its LED display suppressed. It must be noted, though that "IDENTIFY" mode is intermittent because, even with the "RESET" button continuously depressed, it conflicts with important once-per-minute charger internal operations. Some patience may therefore be required when identifying suspect batteries.

It should be noted that after a battery has been determined to be "BAD" it is placed on an indefinite, safe "C/40-rate" charge and its charging-status LED is set to flashing-red indefinitely so that it is most unlikely to be used in error.

The following instructions should be taught to and observed by general charger users. It must be stressed that (especially for this prototype, non-fully-evaluated charger) incidences of "BAD-BATTERY" response must be reported and recorded. Note that there exists a possibility that some batteries which are rejected by this charger may perform acceptably with conventional "batch"-type chargers.

IF ANY BATTERY IS SUSPECTED BY THE CHARGER TO BE FAULTY THEN THE "BAD BATTERY" LED (LAMP) BECOMES LIT FLASHING-RED - THE BATTERY MUST BE IDENTIFIED AND REMOVED FOR EVALUATION ("BAD" BATTERIES MAY BE IDENTIFIED BY HOLDING DOWN THE "RESET" BUTTON WHEREUPON AT INTERVALS THE LED FOR ANY "BAD" BATTERY WILL LIGHT RAPID-FLASHING-YELLOW)

(F) EFFECT OF MAINS FAILURES:-

The charger is equipped with a backup memory system which enables the charging-status of individual batteries to be remembered during power failures of up to several hours (or possibly more). On reconnection of mains power after a failure of acceptable duration then the charger will commence charging operations from the point at which they were broken off. Note that it is thus possible, whilst charging, to switch off the charger, unplug it, transfer it to a new location, reconnect it to a mains supply and switch on without disrupting the charging operation (except for the time lapse incurred whilst not powered-up).

During power failures the charger will also remember and restore its programmed operating mode ("Intelligent" or "C/10" - see (G)).

Whilst mains power is not supplied to the charger it is incapable of doing "Update" operations and of updating its internal memory of the charging-status of individual batteries. Therefore, batteries which are inserted into the charger when not powered-up may be treated by the charger as batteries which were present at the time of power-failure (or deliberate switch-off); hence, batteries inserted into the charger when not fully powered up are liable to be charged improperly. It is thus advised most strongly that no battery is ever inserted into the charger or exchanged with an already-present battery under such conditions. It is permissable, though, in an emergency such as an extended power-failure, to extract batteries from the charger for use but, of course, the charger's battery-status LED display will not be functional and the charging-state of batteries will not be indicated.

For practical purposes the following instructions and information should be taught to and observed by general charger users.

THE CHARGER WILL TOLERATE MAINS FAILURES OF AT LEAST A FEW HOURS WITHOUT FORGETTING CHARGING TASKS. IT IS INADVISABLE TO INSERT OR EXCHANGE BATTERIES IF THE CHARGER IS NOT RUNNING NORMALLY! (TEST FOR NORMAL OPERATION BY PRESSING THE "UPDATE" BUTTON AND NOTING IF THE CHARGER RESPONDS

(G) (a) "C/10-CHARGE" MODE:-
(b) "INTELLIGENT-CHARGE" MODE:-
(a) FORCED MEMORY CLEARANCE:-

(a) The charger can optionally be placed into a "C/10-Charge" operation mode in which every battery holder (regardless of whether it contains a battery or not) is programmed for an indefinite "C/10-rate" charging current. The "C/10-rate" current will charge batteries in 14-16 hours and batteries can generally be left on charge at this rate for at least several weeks without serious damage (though this is unlikely to occur in practice).

The primary use of "C/10-Charge" mode is that of "conditioning" virgin batteries or batteries that have undergone very long periods of disuse (several months or more) before use under a fast-charging regime (such as this charger's "Intelligent-Charge" mode). Most battery manufacturers specify that such batteries should be charged using a 14-16 hour "C/10-rate" charge for their first two or three cycles of usage and that the batteries should be discharged fully between the "conditioning" charges. In realistic situations it may be inconvenient to implement the full conditioning procedure but it should be noted that failure to do so may lower initial battery charge-capacity and can even lead to permanent battery degradation. It may be convenient to perform battery conditioning using an auxiliary or backup charger whilst a primary charger is used for conventional purposes.

In order to set the charger into "C/10-Charge" mode the charger should be switched off (preferably by means of the "Mains" switch), the "RESET" button pressed and held down and the charger switched on again. The "RESET" button must remain depressed for a period of at least eight seconds during which time a warble-tone will be generated and the "RESET" button will flicker. As soon as the warble-tone/"RESET"-button-flicker ends the "RESET" button may be released.

In "C/10-Charge" mode the "UPDATE" and "RESET" buttons serve no purpose and are inactive and all battery-status LEDs (lamps) flash simultaneously at 1-second intervals as an indicator of the set mode.

(b) Usually the charger will be required to operate in the fast-charging "Intelligent-Charge" mode (as outlined in (B),(C)) which is the default mode when powered-up after a long period of inactivity.

To restore the charger to "Intelligent-Charge" mode the charger must be switched off (preferably by means of the "Mains" switch), the "RESET" button pressed and held down and the charger switched on again. The "RESET" button must remain depressed until a warble-tone is generated and the "RESET" button flickers. However, the button must be released before the tone/flicker period ends. In practice, it is sensible to release the "RESET" button after the tone/flicker has been generated for about one second.

(c) The process for setting the charger into "Intelligent-Charge" mode may be used whilst the charger is already in "Intelligent-Charge" mode for purposes of clearing charger

memory. If this is done then the charger will abort all current charging operations and will treat any batteries present in its sockets as batteries recently inserted for charging. (The effect is the same as that produced by removing all batteries from the charger, pressing the "UPDATE" button and reinserting the same batteries). This facility is not expected to be used frequently in practice but may be a valuable short-cut correction method if it is suspected that batteries have been inserted improperly into the charger whilst not powered-up (e.g. during a power-cut or during charger transit).

(H) GENERAL MAINTENANCE CONSIDERATIONS:-

In common with general electrical equipment, the following points should be observed:-

- As the unit is provided with an earthing connection it should be earthed for safety reasons (though note that the output sockets are isolated from the case and from mains earth).

- Avoid contamination of the unit with water and other liquids.

- Avoid subjecting the unit to extremes of temperature (avoid placing in draughty locations, over radiators/heaters and in direct sunlight).

- Wipe the unit occasionally with a dry cloth.

Care should be taken to ensure that the battery holder contacts are kept reasonably clean and the following points should be observed:-

- Should battery holder contacts (including the socket frame) become contaminated with dirt or heavy grease then the performance of the charger may be reduced. The contacts (and battery contacts if necessary) can safely be cleaned using a lint-free cloth wetted with methylated spirits.

The unit contains three fuses of which one is accessible externally and the remaining two are internal. Replacement fuses, if ever required, must be of the following values for full charger protection and safety:-

- Mains input fuse (external):- 0.5A,"T" (anti-surge)

- Transformer o/p fuse (internal) :- 5A,"T" (anti-surge)

- Front-panel fuse (internal):- 160mA,"F" (fast-blow)

NOTES ON PHOTOGRAPHIC PLATES

Notes on **Plate 1** :-

- The central structure comprises six Charge-Discharge board carriers and associated parts mounted on a timber frame.
- The measurement hardware and Beeb-Interface box are visible in the lower left-hand corner.
- The ribbon-cable Charge-Discharge logic buses are clearly visible.
- The controller B.B.C. microcomputer and peripherals are not shown.

Notes on **Plate 2** :-

- The circuit board to left of centre is a Fuse/V_{REF} board.
- The circuit board on the right-hand side is a Charge-Discharge board.
- The ribbon-cable Charge-Discharge logic bus (which is normally plugged into the socket at the top right-hand corner of the Charge-Discharge module) has been removed for clarity.
- A VARTA "AA" cell is shown inserted into the on-board cell holder and is connected via extended tags for 4-terminal measurements.

Notes on **Plate 3** :-

- The box-like structure at the rear is the Beeb-Interface box.
- The structure at the front is the measurement hardware unit.
- The upper circuit board of the measurement unit is the Control Board.
- The lower circuit board visible in the measurement unit is the Sinegenerator board.
- The die-cast metal box which comprises the lower part of the measurement unit contains the Detector unit.

Plate Notes

PLATE 1

The Research Cell/Battery Test Rig

PLATE 2

The Fuse/V_{REF} and Charge-Discharge Boards

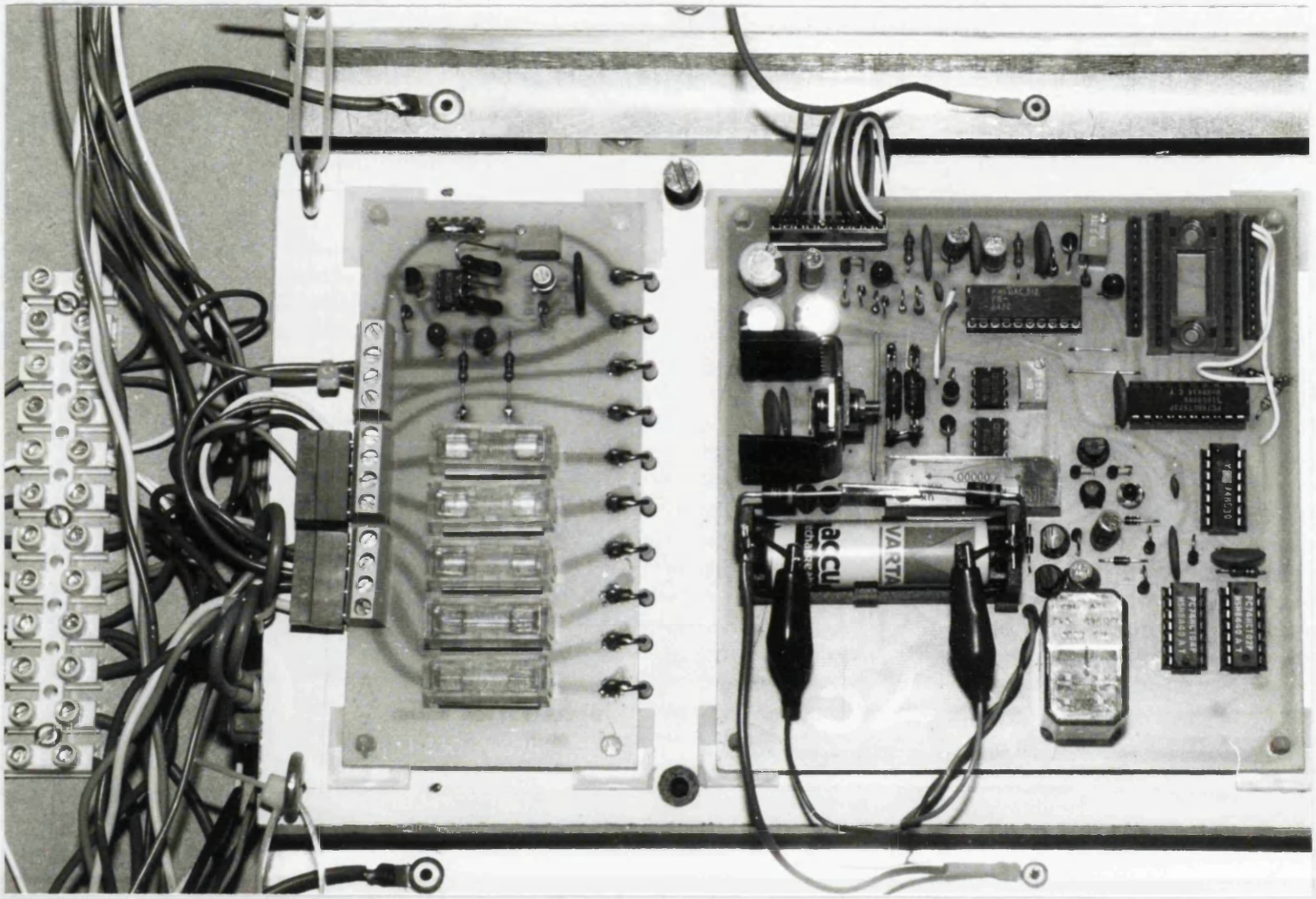
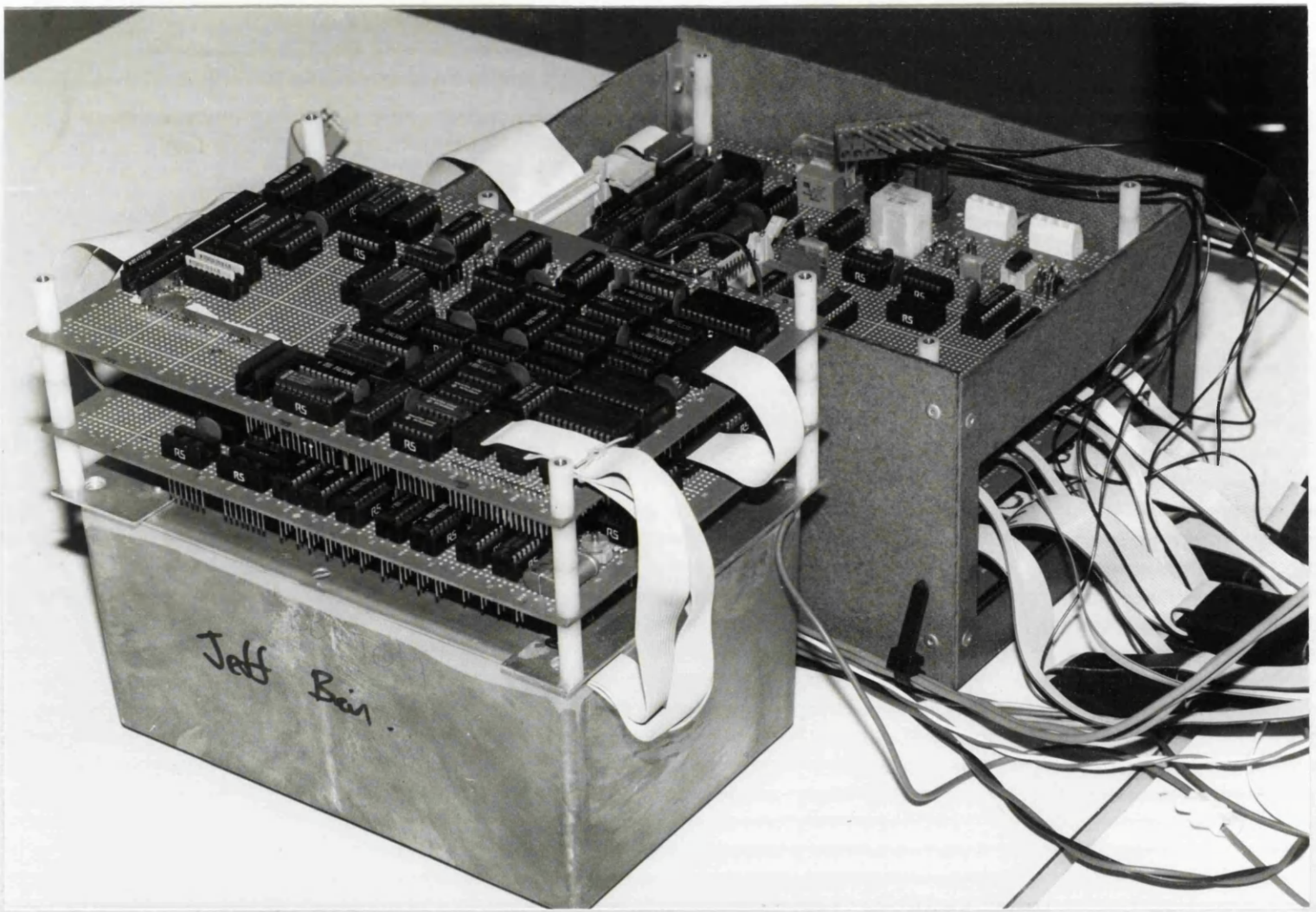


PLATE 3

The Control Board, Sinegenerator Board, Detector Unit and Beeb-Interface Box



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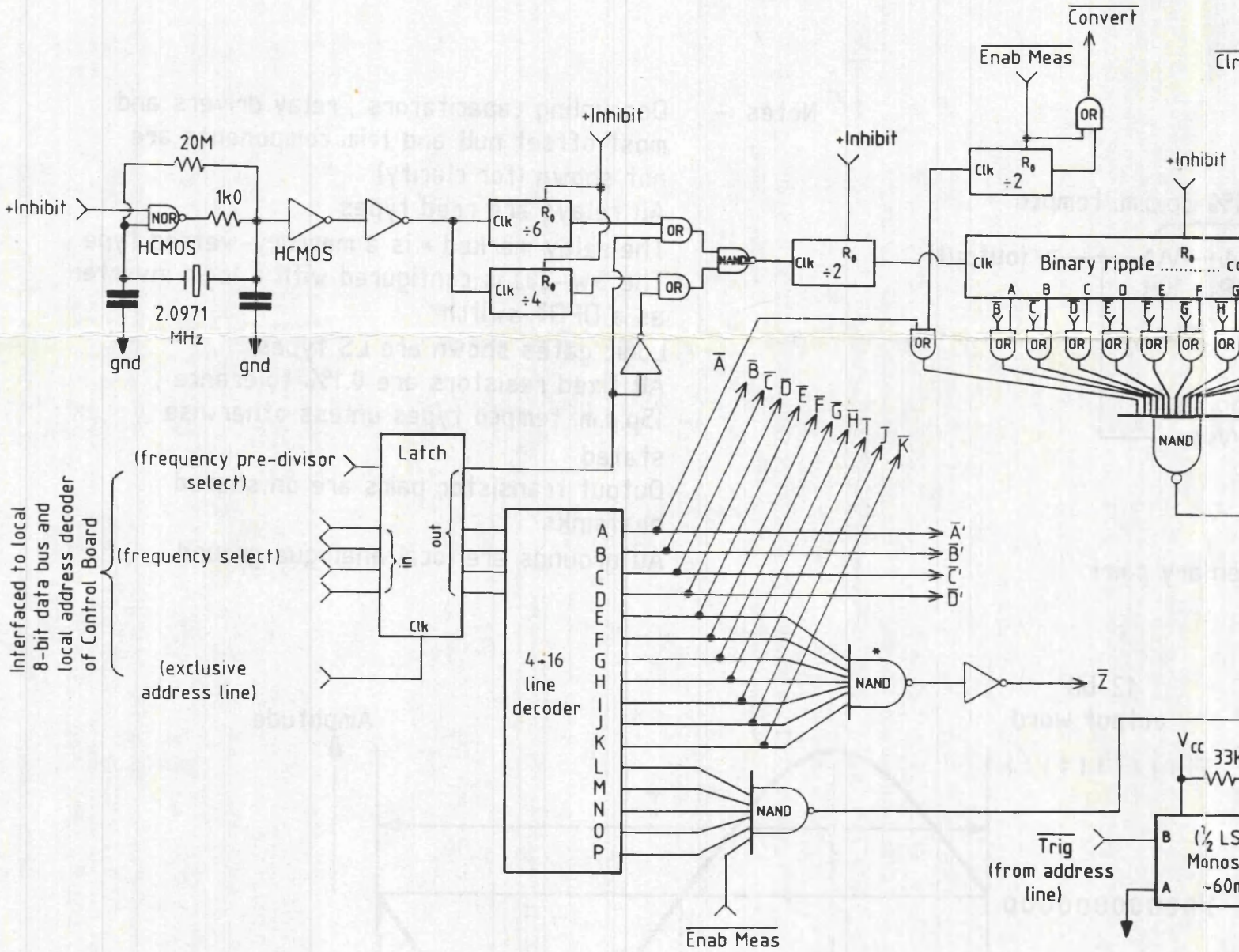
A NOTE ON USE OF THE RESEARCH TEST RIG

This thesis contains sufficient information on the Author's research cell/battery test rig to serve as an operating manual for the rig. The relevant information is contained primarily in Chapters 6 to 8 and some of the Appendices. Certain important points which may be easily overlooked are highlighted in Chapters 6 to 8 with a bracketted exclamation mark: "(!)".

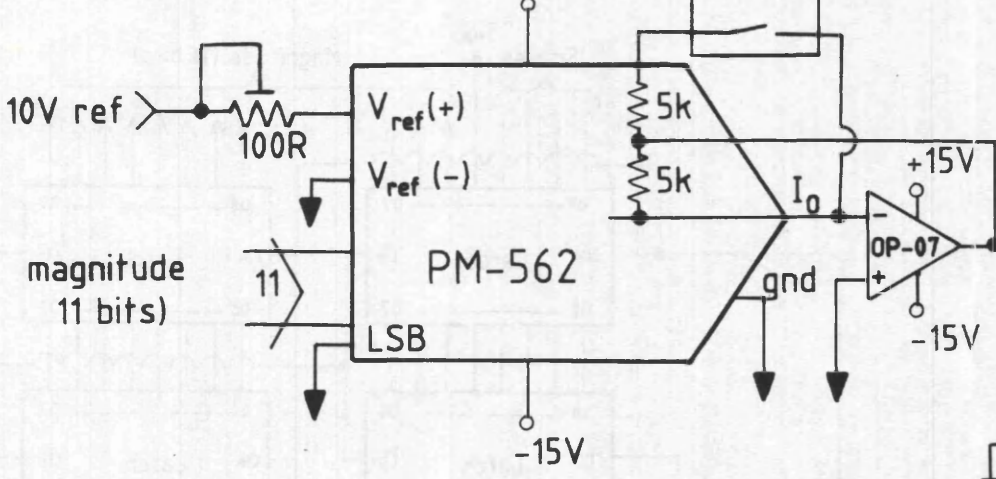
INTELLIGENT CHARGING/PROCESSING OF NICKEL CADMIUM BATTERIES VIA COMPLEX-IMPEDANCE MEASUREMENTS

J. P. Bain B.Sc. : Ph. D. Thesis : August 1990

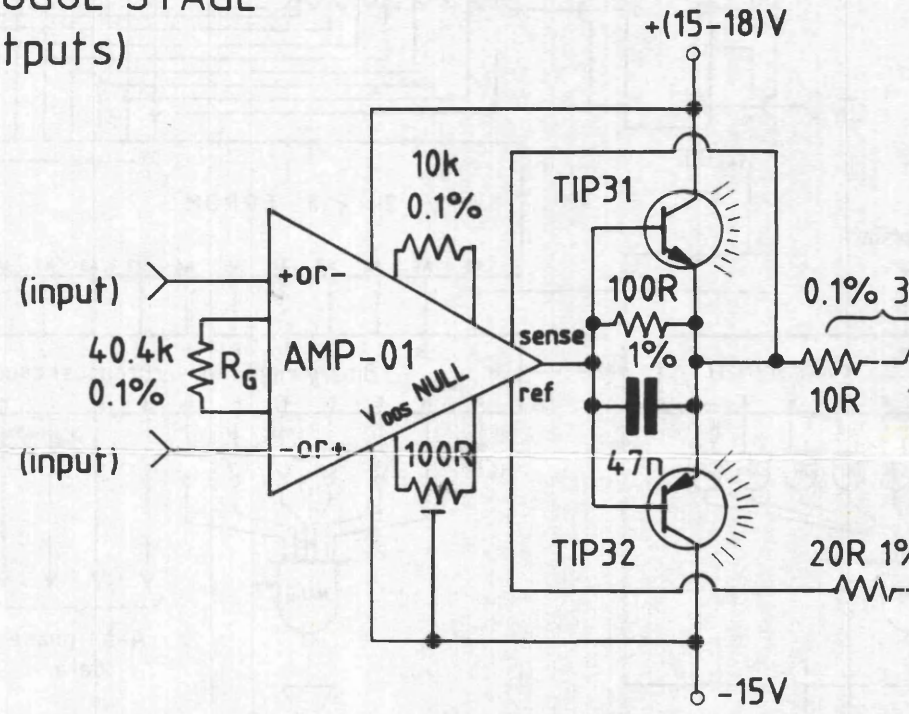
Notes :- EPROM address lines A0-A9 are used to select an output word
EPROM address line A10 is used to select the high/low byte of an output word
All logic gates are LS types unless otherwise specified
All grounds are local logic ground



SHEET 1(a) THE SINEGENERATO



THE SINEGENERATOR ANALOGUE STAGE
(complementary current outputs)



Current output buffer (one of a complementar

Sinewave EPROM coding

EPROM address (A_{10}--------A_0)	EPROM data (D_7------D_0)
00000000000	(00000000)*
00000000001	0000,(0000)*
00000000010	(word 1 lower 8 bits)
00000000011	0000,(word 1 top 4 bits)
00000000100	(word 2 lower 8 bits)
00000000101	0000,(word 2 top 4 bits)
.	.
.	.
.	.
11111111110	(word 1023 lower 8 bits)
11111111111	0000,(word 1023 top 4 bits)

*Note:- these are component parts of word 0

```
CHD_LEDLATCHBASE EQU 44H                        Charge-Discharge/LED latch base a

BACKUPRAMBASE    EQU  4000H                     Base address of external (Batter

*****************************************************************

* Reserve memory for various purposes:-

                 ORG  80H                       Reserve memory starting from the

BATTIMEWORDBASE RMB  20                         Battery-Memo time table (2-byte e
BATSTATWORDBASE RMB  20                         Battery-Status word table (2-byt
ACMEASNOTEBASE  RMB  20                         A.c.-Measurement-Note table (2-by
CHD_LEDBYTEBASE RMB  10                         Charge-Discharge/LED (Status) by
MEASERRCTRBASE  RMB  10                         Measurement-Error-Counter table
BATCOUNTER      RMB  2                          Battery counter and index genera
COUNTERTWO      RMB  2                          Double-step index generator (hig
ACMEASSTORE     RMB  2                          A.c.-Measurement store
GPMEMLOC1       RMB  2                          General-purpose memory 1 (can us
GPMEMLOC2       RMB  2                          General-purpose memory 2 (can us
GPMEMLOC3       RMB  2                          General-purpose memory 3 (can us
GPTIMER         RMB  2                          General-purpose (medium-term) re
SUPERCLOCK      RMB  2                          System time clock "Super" part
FLAG_POSN_WORD  RMB  2                          (System control) Flag byte and P
SUBCLOCK        RMB  1                          System time clock "Sub" part
FREQBYTE        RMB  1                          (Measurement) Frequency byte (BI

*****************************************************************

* Note useful fixed data values:-

ZEROCURRENT     EQU  00000001B                  To program Ch-D/LED latches for
DOUBLEZEROCURR  EQU  101H                       Two concatenated ZEROCURRENT byt

*                                               To program a Ch-D/LED latch for:
DISCHARGE       EQU  00000000B                   the Discharge current (and no L
FASTCHARGE      EQU  00000011B                   the Fast-charge current (and no
SLOWCHARGE      EQU  00000101B                   the Slow-charge current (and no
SUPERCHARGE     EQU  00000111B                   Combined-charge currents (and n
REDLED          EQU  00010000B                   the red LED lit (flashing) (and
GREENLED        EQU  00001000B                   the green LED lit (and Zero-cur
BOTHLEDS        EQU  00011000B                   both LEDs lit simultaneously (a

*                                               To program the Sine-Generator la
FREQ2HZ         EQU  00000000B                   excitation frequency 2Hz (and B
FREQ8HZ         EQU  00000001B                   excitation frequency 8Hz (and B
FREQ32HZ        EQU  00000010B                   excitation frequency 32Hz (and
BADBATTERYLAMP  EQU  10000000B                   the Bad-Battery LED lit (flashi

*                                               To program the Relay-Select latc
BEEPER_REDLAMP  EQU  00001111B                   Beeper/Red-Lamp operating (and
BPR_RLMP_NODISCH EQU 00011111B                   Beeper/Red-Lamp operating and b
*                                                (and no relay open)
ALLRELAYSOPEN   EQU  00001110B                   all relays open (and no other e
NODISCH_NORELAYS EQU 00011110B                   battery discharge inhibited and

ADCSATRESULT    EQU  0000111111111110B          The pure unsigned result derived

OCR1_HI         EQU  OCR1                       Output-Compare-Register-1 Hi-byt
OCR1_LO         EQU  (OCR1+1)                   Output-Compare-Register-1 Lo-byt
FLAGBYTE        EQU  FLAG_POSN_WORD             (System control) Flag byte
POSNBYTE        EQU  (FLAG_POSN_WORD+1)         (System control) Position-counte
BATTIMEHIBASE   EQU  BATTIMEWORDBASE            Battery-Memo time Hi-byte base a
BATTIMELOBASE   EQU  (BATTIMEWORDBASE+1)        Battery-Memo time Lo-byte base a
BATSTATHIBASE   EQU  BATSTATWORDBASE            Battery-Status word Hi-byte base
BATSTATLOBASE   EQU  (BATSTATWORDBASE+1)        Battery-Status word Lo-byte base
```

```
*                                                    8kByte (E)PROM is in use)

startup         LDS  #5FFFH                          ((The program start point) Immediate
*                                                    of external RAM) ...
                JSR  dohardreset                     then do a hardware reset to protect

nmilinetest0    LDAA PORT2                           (Test the state of the NMI line via
                ANDA #00001000B                      until it is high (This ensures that
                BEQ  nmilinetest0                    until the system is adequately power

                LDAA #00000010B                      Enable Serial Tx and disable all SCI
                STAA TRCSR                           .
                LDAA #00000101B                      Select SCI internal clock, asynchron
                STAA RMCR                            .
                LDAA #00001000B                      Select the Timer-1 Output-Compare in
                STAA TCSR1                           .

                LDAA #FREQ32HZ                       Program the Sine-Generator latch for
                STAA SINEGENPROGLATCH                .
                ORAA #00000100B                      (and set BIT2 of the Sine-Generator
                STAA SINEGENPROGLATCH                may possibly have been triggered alr

adcstathitest0  TIM  00000001B ADCREADBUF_LO         (Test the Status output of the ADC a
                BEQ  adcstathitest0                  until the output is found to be high
                ANDA #11111011B                      and end the trigger pulse by clearin
                STAA SINEGENPROGLATCH                .
                LDAB #01001111B                      then put 01001111 binary into B ...
                JSR  Txserialbyte                    and transmit the contents of B via s

adcstatlotest0  TIM  00000001B ADCREADBUF_LO         (Test the Status output of the ADC a
                BNE  adcstatlotest0                  is found to be low) ...
                LDX  #25                             and wait 2.5ms (> 10 ADC counts thou
                JSR  timedelay                       .

*****************************************************************
* POWERUP TESTS FOR CHARGE-MODE DETERMINATION FOLLOW:-
*****************************************************************

* This section determines the operating mode of the charger after powerup. This sect
* tests for system auto-resets. By depression of the Red-Button in a controlled mann
* the charger may be forced into specific operating modes.

                TIM  10000000B ADCREADBUF_HI         Test the Red-Button switch output
                BEQ  forcechargemode                 If low (button depressed) then branc
                JSR  validateramFB                   else check the Battery-Backed RAM fo
                BCS  CMpass0                         If a valid value was found (Carry fl
                OIM  00100000B FLAGBYTE              else set the "Unset-Mode" flag (FLAG
                JSR  dosoftreset                     then do a software reset ...
                JSR  unsetmode                       and enter Unset mode to request atte
                AIM  11111110B OCR1_LO               then clear OCR1 BIT0 (in use as a "v
                JMP  mainprogram                     and jump to the main program for ope

CMpass0         TIM  01000000B FLAGBYTE              Test the "C/10-Charge-Mode" flag bit
                BEQ  CMpass1                         If low (Intelligent-Charge mode) the
                AIM  11111110B OCR1_LO               else clear OCR1 BIT0 (in use as a "v
                JMP  auxprogram                      and jump to the auxiliary program fo

CMpass1         TIM  00100000B FLAGBYTE              Test the "Unset-Mode" flag bit (FLAG
                BEQ  CMpass2                         If low (Charger not registered as be
                JSR  dosoftreset                     else do a software reset ...
                JSR  unsetmode                       and enter Unset mode to request atte
                AIM  11111110B OCR1_LO               then clear OCR1 BIT0 (in use as a "v
                JMP  mainprogram                     and jump to the main program for ope

CMpass2         JSR  validateramdata                 (Check the Battery-Backed RAM to see
*
```

```
auxprogram      LDAA #SLOWCHARGE                Put into A the byte for Slow-charg

                LDX  #0                         (Program all Ch-D latches with the
auxPsetuploop   STAA CHD_LEDLATCHBASE,X         .
                INX                             .
                CPX  #9                         .
                BLS  auxPsetuploop              .

                LDAB #SLOWCHARGE                Put into B the byte for Slow-charg
                ORAB #BOTHLEDS                  .

auxPouterloop   LDX  #0                         Set IX to zero

auxPinnerloop0  STAB CHD_LEDLATCHBASE,X         Program the Ch-D/LED latch pointed
                INX                             then increment IX ...
                CPX  #9                         and compare IX with 9
                BLS  auxPinnerloop0             If lower or the same then return t
                LDX  #500                       else wait 50ms ...
                JSR  timedelay                  .
                LDX  #0                         and set IX to zero

auxPinnerloop1  STAA CHD_LEDLATCHBASE,X         Program the Ch-D/LED latch pointed
                INX                             then increment IX ...
                CPX  #9                         and compare IX with 9
                BLS  auxPinnerloop1             If lower or the same then return t
                LDX  #9500                      else wait 950ms ...
                JSR  timedelay                  .
                BRA  auxPouterloop              and return to the outer loop start

*****************************************************************
* SUBROUTINES FOLLOW:-
*****************************************************************

* A subroutine for charger "Unset" mode. In this mode all Ch-D latches are program
* regardless of the presence or absence of batteries and the charger produces a re
* as a warning to the charger user that attention is required. The routine repetit
* -User-Button. If the button is pressed and then released for 750ms then a Treme
* like a B.B.C. Micro) and the routine is exited.
* (Note that interrupts are best disabled in Unset mode!)

unsetmode       LDAA #SLOWCHARGE                (Program all Ch-D latches for Slow
                LDX  #0                         .
unsetMsetuploop STAA CHD_LEDLATCHBASE,X         .
                INX                             .
                CPX  #9                         .
                BLS  unsetMsetuploop            .

unsetbeeploop   TIM  10000000B ADCREADBUF_HI    Test the Red-Button switch output
                BEQ  umRBfreetest               If low (button depressed) then pas
                LDX  #2400                      else wait 240ms ...
                JSR  timedelay                  .
                TIM  10000000B ADCREADBUF_HI    Test the Red-Button switch output
                BEQ  umRBfreetest               If low (button depressed) then pas
                LDX  #12                        else give a 240ms Beep/Red_Lamp fl
                JSR  beep_RLflash               .
                BRA  unsetbeeploop              and return to the loop start

umRBfreetest    LDD  #750                       Load AB with 750 for a 750ms timed

umRBfreeloop    TIM  10000000B ADCREADBUF_HI    Test the Red-Button switch output
                BEQ  umRBfreetest               If low (button depressed) then res
                LDX  #10                        else wait for 1ms ...
                JSR  timedelay                  .
                SUBD #1                         and subtract one from AB
                BNE  umRBfreeloop               If AB is not equal to zero then re
                LDX  #25                        else give a 500ms tremelobeep ...
                JSR  timedelay                  .
```

```
* are evaluated via a call of "chargeneedtest" and appropriate action is taken.
* byte has BIT7 high is excluded from the test sequence. This routine may option
* byte via serial Tx !!!!!

dctestsequenceX LDAB GPMEMLOC1                    (Put the contents of GPMEMLOC1 i
*                                                 on entry must be 0,1,1 always))
                JSR  Txserialbyte                 then transmit the contents of B
                CLRA                              (and initialise BATCOUNTER/COUNT
                CLRB                              safety)) ...
                STD  BATCOUNTER                   .
                STD  COUNTERTWO                   .

dctsXloop       LDX  BATCOUNTER                   $
                TIM 10000000B CHD_LEDBYTEBASE,X   Test BIT7 of the relevant Ch-D/L
                BNE  dctsXpass                    If high (battery excluded from c
                JSR  doonedctest                  (else call the "Do-One-D.c.-Test
*                                                 holder) ...
                JSR  chargeneedtest               and call the "Charge-Need-Test"

dctsXpass       LDD  BATCOUNTER                   Put BATCOUNTER into AB (Hi-byte
                INCB                              then increment B ...
                CMPB #9                           and compare B with 9
                BHI  dctsXend                     If higher then pass to the routi
                STD  BATCOUNTER                   else put the result into BATCOUN
                ASLB                              then multiply B by two ...
                STD  COUNTERTWO                   and put the result into COUNTERT
                BRA  dctsXloop                    and return to the loop start ...

dctsXend        RTS

*****************************************************************

* A subroutine to program hardware to perform a d.c. test on the battery holder
* determine if a battery (of sufficient terminal voltage) is present in the hold
* current is applied to render the Battery-Presence comparator less susceptible
* The discharge is too brief to significantly affect battery charge state. This
* Present" bit) of the relevant Battery-Status word conditional on the result of
* request conditional output of d.c. measurement data in a selected format via s

doonedctest     LDX  BATCOUNTER                   $
                LDAA #DISCHARGE                   Set temporary Discharge with no
                STAA CHD_LEDLATCHBASE,X           .
                LDD  BATCOUNTER                   and close the measurement relay
                STAB RELAYSELECTLATCH             .
                LDX  #(RELAYSETTLETIME+100)       then wait for the relay and Batt
                JSR  timedelay                    .
                LDX  COUNTERTWO                   $$
                TIM  01000000B ADCREADBUF_HI      and test the Battery-Presence co
                BNE  dodctpass0                   If high (battery appears absent)
                OIM  10000000B BATSTATHIBASE,X    else (present) then set BIT15 of
                LDAA #10000001B                   then put 10000001 binary into GP
                STAA GPMEMLOC1                    .
                BRA  dodctpass1                   and pass ...

dodctpass0      AIM  01111111B BATSTATHIBASE,X    Clear BIT15 of the relevant Batt
                LDAA #10000000B                   and put 10000000 binary into GPM
                STAA GPMEMLOC1                    .

dodctpass1      LDX  BATCOUNTER                   $
                LDAA #ZEROCURRENT                 Set temporary Zero-current + bot
                ORAA #BOTHLEDS                    . (!!!!! the yellow LED flash pr
                STAA CHD_LEDLATCHBASE,X           . but is useful for test purpose
                LDAA #ALLRELAYSOPEN               and open the measurement relay (
                STAA RELAYSELECTLATCH             .
                LDX  #RELAYSETTLETIME             then wait for the relay to sett
                JSR  timedelay
```

```
                BHI   msXpass0                If higher or equal then pass ...
                BEQ   msXpass0                .
                BRA   msXinnerloop1           else return to the loop start

msXpass0        LDX   BATCOUNTER              $
                LDAA  GPMEMLOC3               (Restore the relevant Ch-D/LED by
                ANDA  #01111111B              ensuring that BIT7 is clear (BIT7
                STAA  CHD_LEDBYTEBASE,X       useful safeguard)) ...
                JSR   acmeasserver            (then call the A.c.-Measurement-S
*                                             measurements to be done on the re
                LDX   COUNTERTWO              $$
                LDD   BATSTATWORDBASE,X       and put the (possibly modified) r
                BEQ   msXpass2                (If zero (through battery having
*                                             then pass) ...
                JSR   chargealgorithm         else call the charging/end-of-cha

msXpass1        LDX   COUNTERTWO              $$
                LDD   BATSTATWORDBASE,X       Put the relevant Battery-Status w
                ANDA  #01110000B              and clear all bits of the Hi-byte
                CMPA  #01100000B              then compare A with o110oooo bina
                BNE   msXpass2                If not equal then pass ...
                JSR   topupalgorithm          (else (battery on charge and in t
*                                             algorithm) ...

msXpass2        LDD   BATCOUNTER              Put BATCOUNTER into AB ...
                ANDB  #00000001B              then mask out all bits of B other
                BNE   msXend                  (If the result is not zero (BATCO
*                                             end) ...
                LDD   BATCOUNTER              else put BATCOUNTER into AB ...
                INCB                          then increment AB by 1 ...
                STD   BATCOUNTER              and put AB to BATCOUNTER ...
                ASLB                          then multiply B by 2 ...
                STD   COUNTERTWO              and put AB to COUNTERTWO ...
                BRA   msXouterloop            and return to the (outer-loop) st

msXend          RTS

*****************************************************************

* A subroutine (the "A.c.-Measurement-Server" routine) which prepares the battery
* for a.c. measurements by appropriate (short-term) hardware programming and indi
* then restores the original hardware programming (defined by the relevant Ch-D/L

acmeasserver    LDX   BATCOUNTER              $
                LDAA  #ZEROCURRENT            Set temporary Zero-current with n
                STAA  CHD_LEDLATCHBASE,X      .
                LDD   BATCOUNTER              then close the measurement relay
                STAB  RELAYSELECTLATCH        .
                LDX   #RELAYSETTLETIME        and wait for the relay to settle
                JSR   timedelay               .
                LDX   BATCOUNTER              $
                LDAA  #ZEROCURRENT            then set Zero-current with both L
                ORAA  #BOTHLEDS               .
                STAA  CHD_LEDLATCHBASE,X      . (!!!!! the yellow LED flash pro
*                                             . but is useful for test purposes
                LDX   #1000                   and wait 100ms ...
                JSR   timedelay               .
                LDX   BATCOUNTER              $
                LDAA  CHD_LEDBYTEBASE,X       (then set Zero-current and restor
                ANDA  #BOTHLEDS               relevant battery) ...
                ORAA  #ZEROCURRENT            .
                STAA  CHD_LEDLATCHBASE,X      .
                LDX   #(IPCAPSETTLETIME-1000) (and wait a further period to gua
                JSR   timedelay               measurement-system capacitor-coup
```

```
                TAB                         then put the contents of A into B
                ANDB #00001111B             and clear all bits of B except BIT
                BEQ  decmeaserrctrB         If the result is zero (Measurement
                DECA                        else decrement A by 1 ...
                STAA MEASERRCTRBASE,X       and put the contents of A to the r

decmeaserrctrB  LDAA MEASERRCTRBASE,X       Put the relevant Measurement-Error
                TAB                         then put the contents of A into B
                ANDB #11110000B             and clear all bits of B except BIT
                BEQ  storetidyresult        If the result is zero (Measurement
                SUBA #00010000B             else subtract 00010000 binary from
                STAA MEASERRCTRBASE,X       then put the contents of A to the
                BEQ  storetidyresult        and pass

checkbatpresent JSR  doonedctest            (Call the "Do-one-D.c.-Test" subro
*                                           (holder)) ...
                JSR  chargeneedtest         then call the "Charge-Need-Test" s
                LDX  COUNTERTWO             $$
                TST  BATSTATHIBASE,X        Test the relevant Battery-Status w
                BEQ  acMehend               (If zero (through battery having b
*                                           pass to the routine end) ...
                LDD  #0FFFFH                else put the value FFFF hex (a non
                STD  ACMEASSTORE            then put AB into ACMEASSTORE
                BRA  acMehend               and pass to the routine end

storetidyresult LDD  ADCREADBUFFER          Put the ADC output result into AB
                ANDA #00001111B             ((then mask out BITS12-15 (in A) a
                ANDB #11111110B             but unsigned conversion result in
                STD  ACMEASSTORE            then put AB into ACMEASSTORE

acMehend        RTS

*****************************************************************

* A customised subroutine to initialise the Charge/End-of-Charge algorithm contain
* battery. The relevant battery is that pointed to by BATCOUNTER/COUNTERTWO. The i
* at any time irrespective of the timings of a.c. measurements. The routine must s
* the value of the system time clock at charge initialisation and may do other ope
* bytes and latches.

* This is Charge/End-of-Charge-Algorithm-Initialisation routine version 0.0
initiateChAlg   LDX  COUNTERTWO             $$
                LDD  SUPERCLOCK             Set the relevant Battery-Memo time
                STD  BATTIMEWORDBASE,X      .
                LDD  #ADCSATRESULT          and set the relevant A.c.-Meas.-No
                STD  ACMEASNOTEBASE,X       .
                LDX  BATCOUNTER             $
                CLR  MEASERRCTRBASE,X       then clear all bits of the relevan
                LDAA #FASTCHARGE            (and program for subsequent Fast-c
                ORAA #REDLED                relevant battery)
                STAA CHD_LEDBYTEBASE,X      .
                STAA CHD_LEDLATCHBASE,X     .
                RTS

*****************************************************************

* A customised subroutine containing the Charge/End-of-Charge algorithm for the Fa
* for application to a single battery at a time. The relevant battery is that poin
* routine first checks if a battery has been on Fast-Charge for the limiting perio
* procedure is complicated by the fact that the system clock undergoes wraparound
* than twice the Fast-Charge time limit then the solution is a simple one involvin
* carry/borrow ignored). The main section of the algorithm makes use of appropriat
* measurement results to control the charging process on the battery. On terminati
* relevant Battery-Memo time must be set to the value of the system clock at termi

* This is Charge/End-of-Charge Algorithm version 0.0 for which Fast-Charge is term
```

```
* Test (always!) if the contents of Charge-Algorithm-Counter-A are equal to or gr

testchalgctrA   LDAA BATSTATLOBASE,X            Put the relevant Battery-Status w
                ANDA #00001111B                 and clear all bits of A except BI
                CMPA #CHALGCTRACOMP             and compare A with the value #CHA
                BEQ  initiatetopup1             If equal or higher then pass (for
                BHI  initiatetopup1             .

* Put the current a.c.-measurement result into the relevant A.c.-Measurement-Note

                LDD  ACMEASSTORE                Put the a.c.-measurement result i
                STD  ACMEASNOTEBASE,X           then set the relevant A.c.-Meas.-
                BRA  caend                      and pass to the routine end

* Register the relevant battery as "Bad" and do all necessary operations to abort
* presence evident:-

registerbatbad1 LDX  COUNTERTWO                 $$
                OIM  00111100B BATSTATHIBASE,X  (Set BITS10,13,12,11 ("Battery-Ba
*                                               "Nominally-Charged" bits) of the
*                                               register the battery as "Bad", to
*                                               process and to bypass the Top-Up
                OIM  10000000B FREQBYTE         then set the "Bad-Battery" flag (
                LDAA FREQBYTE                   (and program the Sine-Generator l
                STAA SINEGENPROGLATCH           turn on the Bad-Battery LED whils
                LDX  BATCOUNTER                 $
                LDAA #ZEROCURRENT               (then program for subsequent Zero
                ORAA #REDLED                    battery) ...
                STAA CHD_LEDBYTEBASE,X          .
                STAA CHD_LEDLATCHBASE,X         .
                BRA  caend                      and pass to the routine end

* Initiate the Top-Up algorithm for the relevant battery:-

initiatetopup1  OIM  00100000B BATSTATHIBASE,X  Set BIT13 ("Fast-Charged" bit) of
                LDD  SUPERCLOCK                 then set the relevant Battery-Mem
                STD  BATTIMEWORDBASE,X          .
                LDX  BATCOUNTER                 $
                LDAA #SLOWCHARGE                (and program for subsequent Slow-
                ORAA #REDLED                    the red Status LED lit)
                STAA CHD_LEDBYTEBASE,X          .
                STAA CHD_LEDLATCHBASE,X         .

caend           RTS

*****************************************************************

* A customised subroutine containing the Top-Up charge algorithm for application
* relevant battery is that pointed to by BATCOUNTER/COUNTERTWO. The routine check
* charge (as a topping-up charge) for a limiting period (since Fast-Charge termin
* termination of Top-Up charge the relevant battery is programmed for subsequent
* Status LED lit. The routine controls the state of Battery-Status LEDs during th
* of the control of charging currents. For any battery in the Top-Up phase the as
* red for a period (since Fast-Charge termination) defined by #REDLEDHOLDTIME. Wh
* relevant LED is set to green and the battery is defined as being "Nominally-Cha
* Nominally-Charged state a subroutine "verifybattery" may be called to verify th
* battery is determined to fail verification then the topping-up process is abort
* subsequent Zero-current with the red Battery-Status LED lit.

* This is Top-Up-Algorithm version 0.0
topupalgorithm  LDD  SUPERCLOCK                 Put SUPERCLOCK into AB ...
                SUBD #TOPUPTIMELIMIT            and subtract #TOPUPTIMELIMIT from
                LDX  COUNTERTWO                 $$
                SUBD BATTIMEWORDBASE,X          then subtract the relevant Batter
                BMI  tuapass0                   If the result, as a two's complem
                OIM  00011000B BATSTATHIBASE,X  (also set BITS11,10 ("Nominally-C
```

```
                STAA CHD_LEDLATCHBASE,X          battery) ...
                BRA  rclpass5                    and pass

rclpass4        LDX  BATCOUNTER                  $
                LDAA #ZEROCURRENT                (Program for subsequent Zero-cur
                ORAA #GREENLED                   battery)
                STAA CHD_LEDBYTEBASE,X           .
                STAA CHD_LEDLATCHBASE,X          .

rclpass5        LDD  BATCOUNTER                  Put BATCOUNTER into AB (Hi-byte
                INCB                             then increment B ...
                CMPB #9                          and compare B with 9
                BHI  rclpass6                    If higher then pass ...
                STD  BATCOUNTER                  else put the result into BATCOUN
                ASLB                             then multiply B by two ...
                STD  COUNTERTWO                  and put the result into COUNTERT
                BRA  rclloop                     and return to the loop start ...

rclpass6        LDAA FREQBYTE                    (Program the Sine-Generator latc
                STAA SINEGENPROGLATCH            Battery LED is set to the approp
                RTS

*****************************************************************

* A subroutine used as part of a trickle- or "Maintenance-" charge generator. Th
* all Ch-D latches (but not bytes) which are originally programmed for Zero-curr
* state of Battery-Status LEDs.

settricklepulse LDX  #0                          Initialise IX to zero

stploop         LDAA CHD_LEDBYTEBASE,X           Load A with the ChD_LED byte for
                TAB                              and put the contents of A into B
                ANDA #00000111B                  then mask out all bits of A othe
                CMPA #00000001B                  and compare A with oooooo01B
                BNE  stppass                     If not equal then pass ...
                ORAB #00000100B                  else set BIT2 of B ...
                STAB CHD_LEDLATCHBASE,X          and program the relevant Ch-D/LE

stppass         INX                              Increment IX ...
                CPX  #9                          and compare IX with 9
                BLS  stploop                     If lower or the same then return
                RTS

*****************************************************************

* A subroutine to transmit a single data byte via (RS232) serial output. The rou
* byte to be transmitted in B.

Txserialbyte    LDAA TRCSR                       (Wait until the Transmit Data Re
                ANDA #00100000B                  .
                BEQ  Txserialbyte                .
                STAB TDR                         and put the contents of B into t
                RTS

*****************************************************************

* A subroutine primarily to check if the system's Battery-Backed RAM contains a
* system restart after a power failure though POSNBYTE is also dealt with simult
* locations reserved for holding copies of a FLAG_POSN_WORD value are checked fo
* consistent then the system FLAG_POSN_WORD is set to the common (positive-true)
* test is signalled on exit by the state of the Carry flag.
* (Note that this routine is best entered with maskable interrupts disabled!)

validateramFB   LDX  #(BACKUPRAMBASE+20)         (Read the first (2-byte) FLAG_PO
                LDD  0,X                         (whilst incrementing IX by two)
```

```
                CMPB 0,X                        .
                BNE  badramdata1                .
                INX                             .
                EORA #11111111B                 .
                EORB #11111111B                 .
                STX  GPMEMLOC2                  .
                LDX  GPMEMLOC1                  .
                STD  0,X                        .
                INX                             .
                INX                             .
                STX  GPMEMLOC1                  .
                LDX  GPMEMLOC2                  .
                CPX  #(BACKUPRAMBASE+159)       .
                BLS  readacMnoteloop            .

                LDD  #MEASERRCTRBASE            (Read, check and restore all (1-b
                STD  GPMEMLOC1                  from the primary table in Battery
readMerrctrloop LDAA 0,X                        an address generator for STAA ope
                INX                             10 bytes and GPMEMLOC2 forms part
                EORA #11111111B                 operations which increments by a
                CMPA 0,X                        is found in any stored value)
                BNE  badramdata1                .
                INX                             .
                EORA #11111111B                 .
                STX  GPMEMLOC2                  .
                LDX  GPMEMLOC1                  .
                STAA 0,X                        .
                INX                             .
                STX  GPMEMLOC1                  .
                LDX  GPMEMLOC2                  .
                CPX  #(BACKUPRAMBASE+179)       .
                BLS  readMerrctrloop            .

                LDX  #10                        Give a 200ms tremelobeep ...
                JSR  tremelobeep                .
                LDX  #500                       then wait 50ms ...
                JSR  timedelay                  .
                LDX  #10                        and give a 200ms Beep/Red-Lamp f
                JSR  beep_RLflash               .
                LDX  #500                       then wait 50ms ...
                JSR  timedelay                  .
                LDX  #10                        and give a 200ms tremelobeep ...
                JSR  tremelobeep                .
                LDX  #500                       then wait 50ms ...
                JSR  timedelay                  .
                LDX  #10                        and give a 200ms Beep/Red-Lamp f
                JSR  beep_RLflash               .
                AIM  11111110B OCR1_LO          then clear OCR1 BIT0 (in use as
                CLR  SUBCLOCK                   and initialise SUBCLOCK to zero
                SEC                             then set the Carry flag ...
                BRA  vrdend                     and pass to the routine end

badramdata1     CLC                             Clear the Carry flag

vrdend          RTS

*****************************************************************

* A subroutine to generate a modulated beep ("tremelobeep") of programmable lengt
* is effectively at half normal intensity and is not always clearly visible).
* Nominal length of tremelobeep = (Contents of IX on entry) * 20 milliseconds

tremelobeep     PSHX                            Push the counter value from IX to
                LDAB #BEEPER_REDLAMP            then give a 10ms beep/Red_Lamp fl
                STAB RELAYSELECTLATCH           .
                LDX  #100
```

```
                LDD  DOUBLEZEROCURR          (Set all Ch-D/LED Programming byt
                LDX  #0                      .
clrprogbyteloop STD  CHD_LEDBYTEBASE,X       .
                INX                          .
                INX                          .
                CPX  #9                      .
                BLS  clrprogbyteloop         .

                CLRA                         Initialise SUPERCLOCK to zero ...
                CLRB                         .
                STD  SUPERCLOCK              .
                AIM  00100000B FLAGBYTE      (then clear all bits of FLAGBYTE
*                                            "Unset-Mode" flag bit)) ...
                LDAA #5                      and initialise POSNBYTE to 5 (wil
                STAA POSNBYTE                .
                LDAA #FREQ2HZ                then put into FREQBYTE the byte f
                STAA FREQBYTE                .
                LDX  #12                     and give a 240ms Beep/Red-Lamp fl
                JSR  beep_RLflash            .
                RTS

*****************************************************************
* INTERRUPT ROUTINES FOLLOW:-
*****************************************************************

* The OCI routine is invoked every 1/9.375 second on Timer-1 Output-Compare inter
* provide system timekeeping by incrementing the (SUPERCLOCK-SUBCLOCK) system clo
* (1-byte) is reset immediately upon reaching 141 and so has a cycle time of (15
* is incremented upon each reset of SUBCLOCK and has a cycle time of about 274 ho
* bits of FLAGBYTE at timed intervals so as to inform the main program that hardw
* is convenient. This routine also increments the general-purpose resettable time
* time (subject to external resets) of approximately 6990 seconds . It should be
* effectively 0.26666% slow compared to conventional real time. The OCI routine a
* batteries. Any battery holder programmed for nominal Zero-current is in reality
* duty cycle. This charge regime is equivalent to a trickle-charge at the C/40 ra
* to maintain the charge state of charged batteries left in the charger for exten
* any totally exhausted batteries which might be placed in the charger (and which
* insufficient terminal voltage). The pulse charging is accomplished by selective
* not ChD_LED bytes) 15 seconds prior to each (once-per-minute) system measuremen
* are not generated whilst the Red-User-Button is depressed (to avoid interfering
* (Note that the 6303 processor is assumed to be operating with a 2.4576MHz oscil

ociroutine      LDAA TCSR1                   (Clear Output-Compare-Flag-1 by d
                LDAA #0                      followed by a write of 0 to the O
                STAA OCR1_HI                 .
                CLI                          (and enable maskable interrupts s
*                                            (via "irq1routine") to depression
                LDD  GPTIMER                 then put GPTIMER into AB ...
                ADDD #1                      and add 1 to AB ...
                STD  GPTIMER                 then put AB to GPTIMER ...
                LDAA SUBCLOCK                and put SUBCLOCK into A ...
                INCA                         then increment A by 1 ...
                CMPA #140                    and compare A with 140
                BHI  ocipass0                If higher then pass ...
                STAA SUBCLOCK                else put A into SUBCLOCK ...
                BRA  ociend                  and pass to the routine end

ocipass0        CLR  SUBCLOCK                Clear SUBCLOCK ...
                LDD  SUPERCLOCK              and put SUPERCLOCK into AB ...
                ADDD #1                      then add 1 to AB ...
                STD  SUPERCLOCK              and put AB to SUPERCLOCK ...
                ANDB #00000011B              then clear all bits of B to the l
                BNE  ocipass1                and pass if the result is not equ
                OIM  00000001B FLAGBYTE      else set the "Measurement-Request
                BRA  ociend                  and pass to the routine end
```

```
                CPX  #(BACKUPRAMBASE+39)          .
                BLS  saveNflagBloop              .

                LDD  #(BACKUPRAMBASE+40)         (Save all Battery-Memo times (2-b
                STD  GPMEMLOC2                   -true form) pairs (4-byte) to the
                LDX  #(BATTIMEWORDBASE)          forms part of an address generato
savebattimeloop LDD  0,X                         by a total of 20 bytes and GPMEML
                INX                              for STD operations which incremen
                INX                              .
                STX  GPMEMLOC1                   .
                LDX  GPMEMLOC2                   .
                STD  0,X                         .
                INX                              .
                INX                              .
                EORA #11111111B                  .
                EORB #11111111B                  .
                STD  0,X                         .
                INX                              .
                INX                              .
                STX  GPMEMLOC2                   .
                LDX  GPMEMLOC1                   .
                CPX  #(BATTIMEWORDBASE+19)       .
                BLS  savebattimeloop             .

                LDX  #(BATSTATWORDBASE)          (Save all Battery-Status words (2
savebatstatloop LDD  0,X                         (negative-true form) pairs (4-byt
                INX                              GPMEMLOC1 forms part of an addres
                INX                              increments by a total of 20 bytes
                STX  GPMEMLOC1                   address generator for STD operati
                LDX  GPMEMLOC2                   bytes))
                STD  0,X                         .
                INX                              .
                INX                              .
                EORA #11111111B                  .
                EORB #11111111B                  .
                STD  0,X                         .
                INX                              .
                INX                              .
                STX  GPMEMLOC2                   .
                LDX  GPMEMLOC1                   .
                CPX  #(BATSTATWORDBASE+19)       .
                BLS  savebatstatloop             .

                LDX  #(ACMEASNOTEBASE)           (Save all A.c.-Measurement-Note v
saveacMnoteloop LDD  0,X                         form),(negative-true form) pairs
                INX                              GPMEMLOC1 forms part of an addres
                INX                              increments by a total of 20 bytes
                STX  GPMEMLOC1                   address generator for STD operati
                LDX  GPMEMLOC2                   bytes))
                STD  0,X                         .
                INX                              .
                INX                              .
                EORA #11111111B                  .
                EORB #11111111B                  .
                STD  0,X                         .
                INX                              .
                INX                              .
                STX  GPMEMLOC2                   .
                LDX  GPMEMLOC1                   .
                CPX  #(ACMEASNOTEBASE+19)        .
                BLS  saveacMnoteloop             .

                LDX  #(MEASERRCTRBASE)           (Save all Measurement-Error-Count
saveMerrctrloop LDAA 0,X                         form),(negative-true form) pairs
                INX                              GPMEMLOC1 forms part of an addres
                STX  GPMEMLOC1                   increments by a total of 10 bytes
```

```
* effectively whilst raising the (ADC-code) algorithm thresholds - this may help
* 500mAh batteries more effectively (note that the ADC output result is inversely

* The charger could be given a "Dump-Charge" mode in which a timed discharge to a
* This mode could be used to perform a type of conditioning on batteries and poss
* have adequate chargeable capacities - though the latter function generally requ
* done which is impossible to fit into an 8-hour period. The mode would best be a
* could signal faulty batteries via the same mechanism as the "Intelligent-Charge
* Charge" mode could be a batch-charging mode or could operate in much the same m

* The 7109 integration capacitor ought to be ~1.25uF and not 2.2uF for best accur

* The dedicated-hardware sine-generator used could be replaced by a 6303-ROM-base
* the system interrupt clock to be paused during waveform generation which necess
* end of each waveform-generation phase and (b) the Yellow-User-Button service me
* mechanism using a hardware bistable which can be read and reset by the 6303

* The DG211 analogue switch ought to have power rails of at least +\-8V and the p
* from rails of +/-6V or higher - but ensure that the 7109 input is protected fro

* The main drawback of this program is that in order to output results (serial Tx
* is necessary to operate this program with a 5-minute cycle time which is perhap
* 4-minute cycle time)

**********************************************************************
THE END!
```

Sheet 3(a)

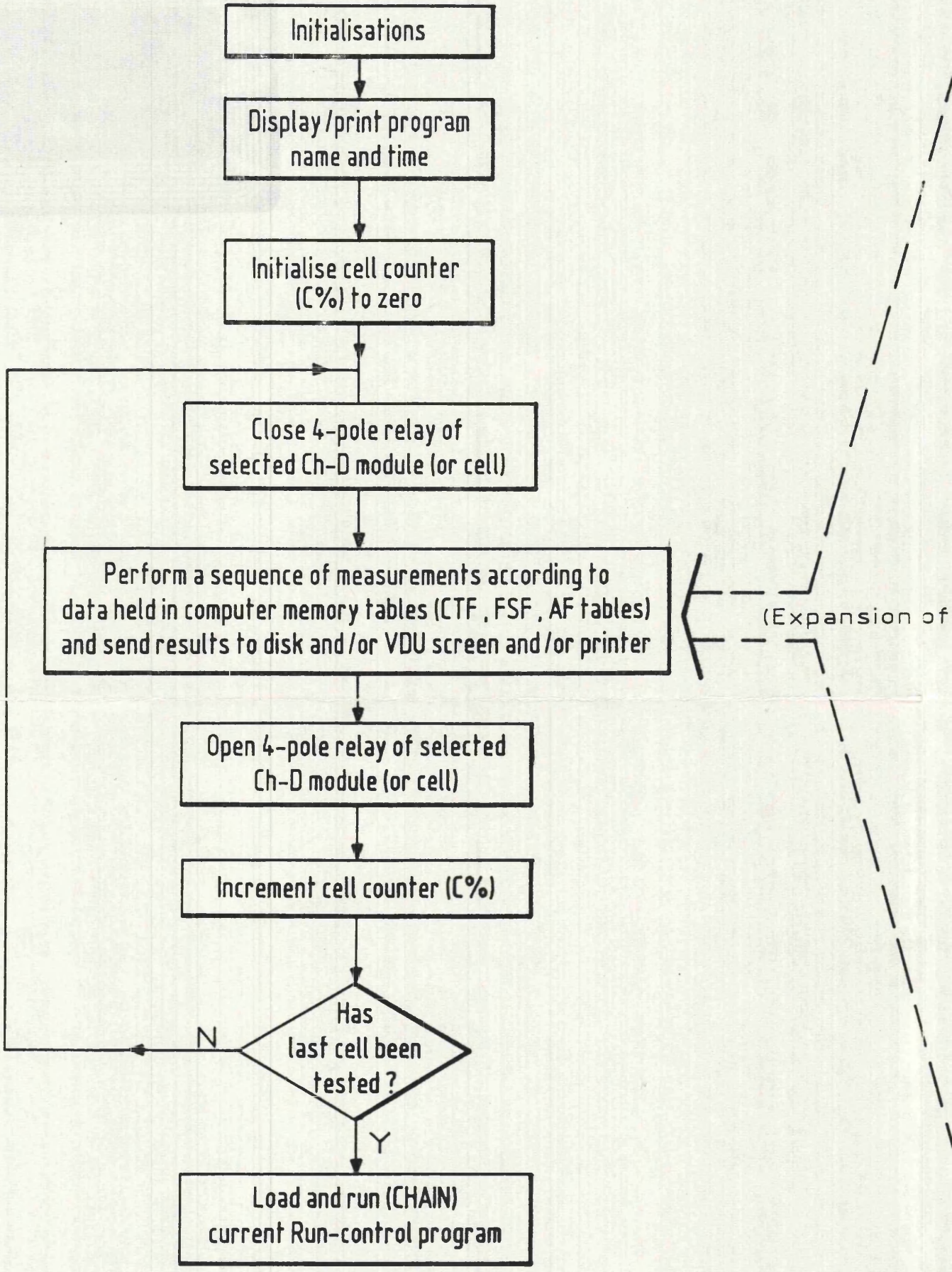
A flowchart for a typical R

SHEET 3(a) reverse

Notes:- (*)"Interpretation" of an instruction involves determining and recording its meaning for future usage. For any charge-discharge control instruction a relevant computer memory table (CPB table) is reprogrammed immediately according to the data contained in the instruction.

The true loop and timing structure for the "Display program time value" function, the "Do check for overcharge/overdischarge ..." function and the three tests (in lozenge boxes) which follow are omitted for reasons of simplicity. In practice, a nested loop structure is used in which overcharge/overdischarge checks and the three tests following are done at timed (typically 10 second) intervals whilst the program time value is updated as continuously as is possible.

Program "utilities and options" include facilities for manual program suspension, inspection of program and data parameters, manual modification (at run-time) of program and data parameters, and manual requests of special measurement utilities.



Sheet 3(b) A flowchart for a typical Measurement Program
(Notes on reverse side)

INTELLIGENT CHARGING/PROCESSING OF NICKEL CADMIUM BATTERIES VIA COMPLEX-IMPEDANCE MEASUREMENTS

J. P. Bain B.Sc. : Ph. D. Thesis : August 1990

SHEET 3(b) reverse

Notes:- A measurement program is normally entered automatically from a Run-control program; upon completion of the measurement program the Run-control program is automatically re-entered. The measurement program is invoked accoring to timing data available to and used by the Run-control program.

The left-hand flowchart shows program flow with the details of measurements omitted. The right-hand flowchart is an expanded view of the "Perform a sequence of measurements ..." block. It shows a typical measurement sequence involving a test of cell/batter d.c. terminal voltage followed by cell/battery d.c. nulling and a sequence of a.c. measurements. A calculated autoranging method is used for selecting optimum excitation amplitudes for individual a.c. measurements.