Optimisation of Lateral Super-Junction Multi-Gate MOSFET for High Drive Current and Low Specific On-Resistance in Sub-100 V Applications

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Abstract

The design and optimisation of a non-planar super-junction (SJ) Si MOSFET based on SOI technology for low voltage rating applications (below 100 V) is carried out with physically based commercial 3-D TCAD device simulations using Silvaco. We calibrate drift-diffusion simulations to experimental characteristics of the SJ multi-gate MOSFET (SJ-MGFET) aiming at improving drive current, breakdown voltage (BV), and specific on-resistance ($R_{on,sp}$). We investigate variations in the device architecture and improve device performance by optimizing doping profile under charge imbalance. The SJ-MGFET, using a folded alternating U-shaped n/p– SJ drift region pillar width of 0.3 μm with a trench depth of 2.7 μm achieves specific on-resistance ($R_{on,sp}$) of 0.21 mΩ.cm^2 at a BV of 65 V. In comparison with conventional planar gate SJ-LDMOSFETs, the optimised SJ-MGFET gives 68% reduction in $R_{on,sp}$ and 41% increase in a saturation drain current at a drain voltage of 5 V and a gate voltage of 10 V.

Keywords: Super-junction (SJ), multi-gate (MG), power MOSFETs, silicon-on-insulator (SOI), breakdown voltage (BV), specific on-resistance.

1. Introduction

The LDMOS (Lateral Double Diffused MOSFETs) technology based super-junction (SJ) design has been widely employed for various voltage applications such as domestic and office electronics appliances, automotive, military, and industrial control [1]. The super-junction (SJ) power MOSFET has

shown significant improvement in the trade-off relationship between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$) due to heavily doped alternating n– and p– pillars in the drift region because the SJ design benefits from charge-compensation between these n– and p– pillars. During the off-state when the n-pillars are fully depleted, the vertical electric field component is a function of lateral position in the drift region. In order to achieve a high breakdown voltage, the depths of the columns are increased without decreasing doping concentration [1, 2]. Considering that an optimal doping concentration is fixed for a specific breakdown voltage, the n-pillar doping concentration can be increased to be inversely proportional to the drift width resulting in a reduction of the on-resistance. This n-pillar doping concentration increase will subsequently lead to a linear relationship between the BV and $R_{on,sp}$ [2]. However, the implementation of lateral SJ transistor technology for low voltage (<200 V) applications has not been attractive due to the fact that the channel resistance becomes comparable to the drift region resistance at low voltage ratings. This is as a result of the minimum pillar width in the SJ drift region which becomes similar to the built-in depletion region. On-resistance of the minimum pillar width cannot be further reduced and design variations of the SJ transistor are thus very limited [3, 4].

In this work, we explore the potential of non-planar silicon MOSFET technology to be used as integrated power transistors with applications in power switching and amplifiers using physically based 3-D TCAD simulations [5]. We analyse experimental characteristics of the non-planar SJ multigate MOSFET (SJ-MGFET) fabricated within a silicon-on-insulator (SOI) technology [6] by reproducing its I-V characteristics and the BV. The simulations aim to improve major device figures-of-merit (FoM) including drive current, BV and specific on-resistance ($R_{on,sp}$). The structure of the paper is as follows: Section II describes the concept, structure and main characteristics of the SJ-MGFET devices, Section III the TCAD simulation methods and the calibration approach. Section IV discusses simulation results, device performance, and device design optimisation. Section V summarises the main conclusions of this work.

2. Device Structure of SJ-MGFET

The SJ-MGFETs studied here have relatively complex 3D design permitted by the application of non-planar SOI technology [6]. The transistor consists of a deep trench gate with a heavily doped alternating U-shaped n-type

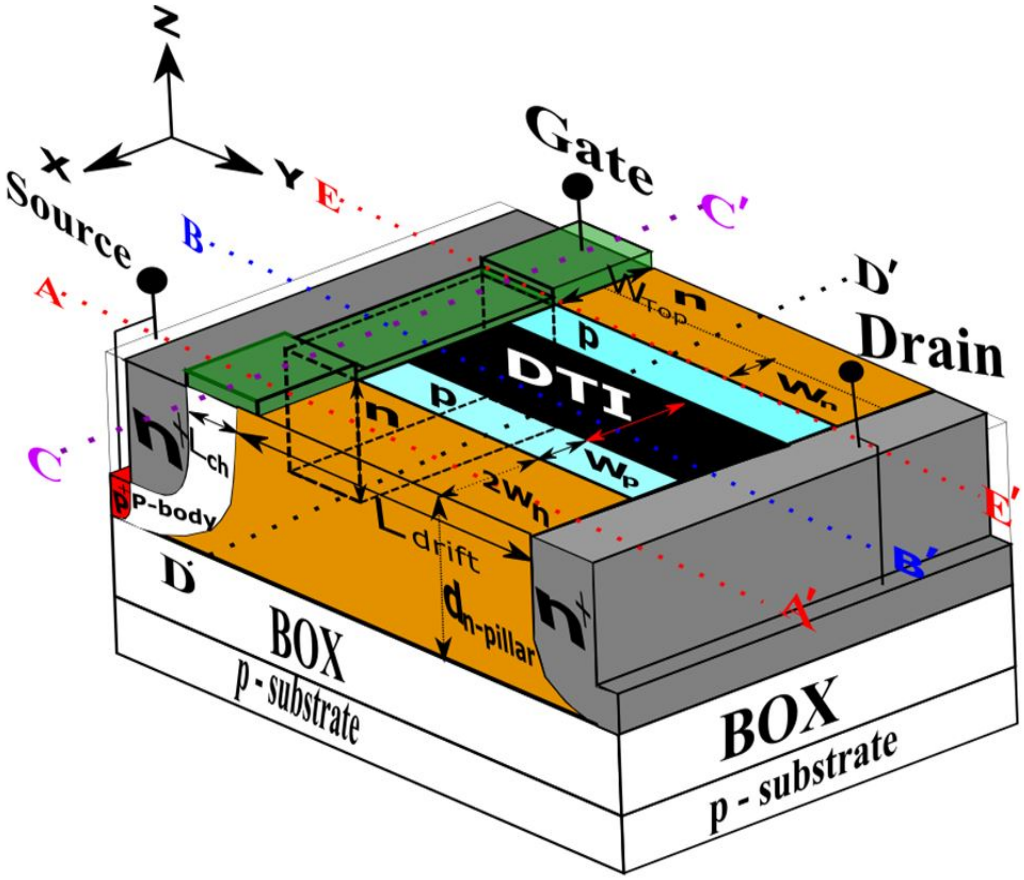
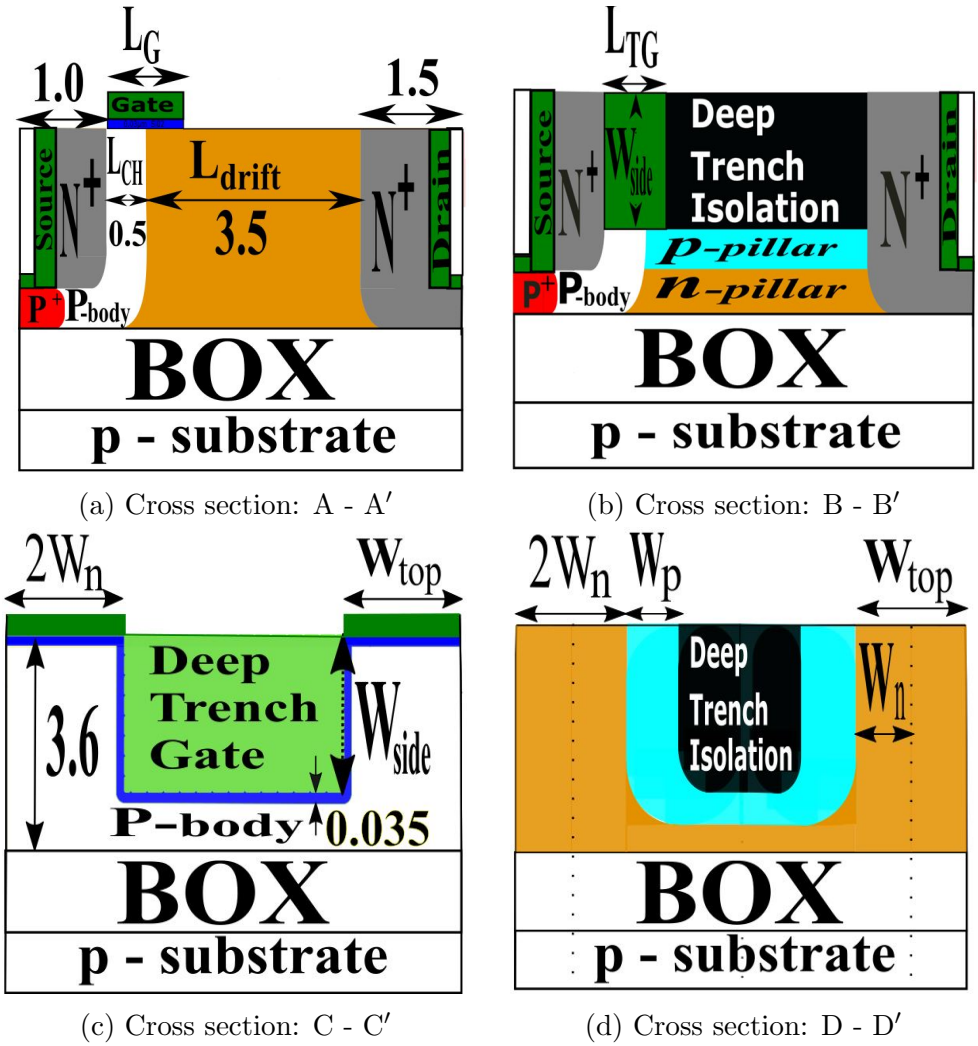


Figure 1: Schematic of the investigated 1μm gate length SJ-MGFET.

and p-type doping pillars forming a drift region. The schematic of the device simulation domain with cross-sectional views is illustrated in Fig. 1 and Fig. 2 (all measurements are in μm). This transistor design follows closely the architecture of SJ-MGFETs reported in [6, 7]. The whole transistor structure is grown on a buried oxide layer to mitigate the effect of substrate-assisted depletion (SAD) [8, 9, 10]. The SJ-MGFET has a 1 μm gate length trenched in the channel of 0.5 μm length, creating a top surface (W_{top}) and a side wall (W_{side}) enclosure in the channel (non-planar technology). This forms a multi-gate structure in the channel aiming at reducing the channel resistance and redistributing electron current crowding near the peak of the n-pillar in a SJ unit. We have carefully examined trench depths ranging from 1.5 μm - 3.0 μm in a step of 0.3 μm. We have observed that the difference



(a) Cross section: A - A′

(b) Cross section: B - B′

(c) Cross section: C - C′

(d) Cross section: D - D′

Figure 2: The cross-sectional views at the indicated locations in the investigated 1μm gate length SJ-MGFET.

in the doping concentration of the SJ n– and p–pillars becomes smaller as the trench depth is increased, also reported by [7]. For effective pathway to the SJ drift region, a trench depth of 2.7 μm (W_{side}) is chosen in this study. The deep trench source and drain contacts provide an effective 3D current density distribution in the structure that ensures uniform conducting flow with the deep trench isolation (DTI) separating each SJ unit. A different dimension of buried silicon dioxide ($Si0_2$) ranging from 0.5 μm to 5.0 μm has

been studied in order to minimise the effect of substrate-assisted depletion (SAD) [8, 11] and mitigate the degradation of current during self-heating. The self-heating management should ensure a good thermal conductive path for the dissipated heat in the active device region to the substrate (this is a result of the poor thermal conductivity of $Si0_2$ (1.4 W/m-K) compared to silicon (140 W/m-K)) [12, 13]. Thus, 2 μm was chosen as the depth of the buried oxide in this study. N_n and N_p are the doping concentration of n– and p–pillars with W_n and W_p their widths of 0.3 μm, respectively. The peak doping concentrations in p-type substrate and n-type source/drain contact are 1×10^{15} cm^3 and 1×10^{20} cm^3, respectively. Note that a design of this doping profile has to prevent a current leakage and a punch-through in the device.

3. 3-D TCAD Simulations of SJ-MGFET

The study is carried out with a 3-D commercial device simulator Atlas by Silvaco [5] using a drift-diffusion (DD) transport approach. In the DD transport approach, the carrier mobility model plays a central role. Since electrons are major carriers in the SJ-MGFET, we employ the Caughey-Thomas electron mobility model [14] which is given by:

$$\mu_e = \mu_1(\frac{T_L}{300K})^{\alpha_e} + \frac{\mu_2(\frac{T_L}{300K})^{\beta_e} - \mu_1(\frac{T_L}{300K})^{\alpha_e}}{1 + (\frac{T_L}{300K})^{\gamma_e}(\frac{N}{N_{\text{crit}}})^{\delta_e}} \quad (1)$$

where μ_e is the doping and temperature dependent low field electron mobility, while μ_1 and μ_2 are the first and second term mobility components, N_{crit} is the electron concentration between μ_1 and μ_2. N is the total impurity concentration, T_L is the lattice temperature, and α_e, β_e, γ_e, and δ_e are doping and temperature coefficients. We have used the following electron mobility parameters: μ_1= 55.24 cm^2/V.s, μ_2= 1429.23 cm^2/V.s, $N_{\text{crit}} = 1.072 \times 10^{17}$ cm^{-3}, α_e = 0.0, β_e = -2.3, γ_e = -3.8, δ_e = 0.73. All these parameters are default parameters for the Caughey-Thomas mobility model in Atlas [14].

Transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics of the SJ-MGFET at different voltage ratings will be compared with reported experimental data [6] including breakdown voltage (BV). In addition, the degradation of the current induced by self-heating (as a result of power dissipation and a low thermal conductivity of the buried oxide layer) is also investigated. Finally, the doping profile and 3-D geometry of the SJ-MGFET is optimised to increase the BV and to minimise device specific on-resistance ($R_{on,sp}$).

In 3-D electro-thermal simulations, we solve a heat transport equation given by:

$$C\frac{\delta T_L}{\delta t} = \nabla(K\ \nabla T_L) + H \tag{2}$$

where C is temperature-dependent heat capacitance per unit volume in real space, k is the temperature-dependent thermal conductivity in real space, H is the heat generation and T_L is the local lattice temperature. Placing of thermal contacts in the device along the x, y, and z axes has been carefully examined because the choice of thermal boundary conditions determines degree and distribution of temperature within the structure [15]. Thermal contacts are positioned at the bottom, and at the electrodes (source and drain), with all contacts set at 300 K in order to achieve a real time self-heating effect that has occurred in measurements [16, 17].

The switching performance of the SJ-MGFET is investigated with the aim of quantifying its capacitance (C) and conductance (G) effects respectively to allow further optimisation of the structure to meet different applications. The capacitive behaviour of the device is a function of the inversion, depletion and accumulation states [18, 19]. We studied the C-V curve in our simulation at a frequency of 1 MHz in order to quantify the junction capacitances and doping concentration of the substrate.We investigated the resultant effect of the Gate-drain capacitance ($\mathrm{C_{gd}}$) and Gate-source capacitance ($\mathrm{C_{gs}}$) on the Gate capacitance $\mathrm{C_g}$.

4. Structure Optimisation of SJ-MGFET

Figure 3 (a) compares the transfer characteristics ($\mathrm{I_D}$-$\mathrm{V_{GS}}$) of the experimental and the simulated transistor at a drain bias ($\mathrm{V_{DS}}$) of 0.1 V. The experimental transistor shows a linear dependence above a gate bias ($\mathrm{V_{GS}}$) of 4 V till a saturation on-set at about 12 V exhibiting a more resistive behaviour in the device body than observed in simulation. This increase in the resistivity of the channel occurring in experimental [6] $\mathrm{I_D}$-$\mathrm{V_{DS}}$ characteristics; is caused by the loss of gate control because the deep trench gate fabrication is technologically limited and does not fully encompass the p-body of the device (see Fig. 1). The simulations are in excellent agreement with experimental observations up to an elevated $\mathrm{V_{GS}}$ of 4 V. Above $\mathrm{V_{GS}} = 4$ V, the simulations show typical transistor switching characteristics when the drain current increases before reaching a saturation point ($\mathrm{V_{GS}} \sim 14$ V). Note here

that the drain current is normalised per width of the non-planar transistor in order to be able to make a fair comparison with planar SJ-MOSFET technology. A threshold voltage of approximately 1.8 V has been obtained by interpolating a linear region of the I_D-V_{GS} characteristics at a low drain bias of 0.1 V. Fig. 3 (b) shows the output characteristics (I_D-V_{DS}) with a maximum saturation drain current over 650 mA/mm at a V_{GS} of 10 V at $V_{DS} = 5$ V. Fig. 4 compares the previous electrical simulations with electro-thermal simulations which account for the effect of lattice temperature on I_D-V_{DS} characteristics. The heat-per-Joule effect exhibits itself by the reduction of conductance in the saturation region of the drain current which is more pronounced at high drain biases. The SOI transistor architecture suffers from enhanced self-heating issues because of the low thermal conductivity of silicon dioxide. Therefore, we have also studied a variation of the SOI based design when a fully deployed buried oxide (BOX) substrate in the partially depleted SOI SJ-MGFET is replaced by a partial BOX with opening under the drain as illustrated in Fig. 5(a). The partially buried oxide transistor architecture aims to provide an additional thermal conductive path for the dissipated heat to a substrate and enhance uniform distribution of electric field at breakdown.

This is because the thermal window alleviates the low thermal conductivity of BOX and limits the total temperature rise in the device by allowing the heat to dissipate through the opening in the thermal window. Fig. 5 (b) shows the I_D-V_{DS} characteristics of the SJ-MGFET with fully buried oxide (SOI technology) compared to the I_D-V_{DS} characteristics of the SJ-MGFET which uses only a partially buried oxide (thermal window) architecture. Both I-V characteristics are obtained from the electro-thermal simulations. At a gate bias of 10 V and a drain voltage of 50 V, the current decreases about 7.5% due to the self-heating when compared to the device with an ideal heat dissipation (the ideal heat dissipation means that a lattice temperature in the whole device would be at kept at room temperature of 300 K). When the SJ-MGFET is designed using a thermal window as shown in Fig. 5 (a); the current decrease seen in Fig. 5 (a) is less than 3% as a result of redistribution of temperature in the substrate through the additional heat conductive path. This current decrease is relatively very small suggesting a quite limited effect of the thermal window in the transistor architecture. The charge induced by the SJ n-and p-pillars should provide a mirror symmetry of each other in order to ensure charge compensation during the off-state. However, a cross-sectional area of the n-pillar (A_n) is larger than that of the p-pillar (A_p) as

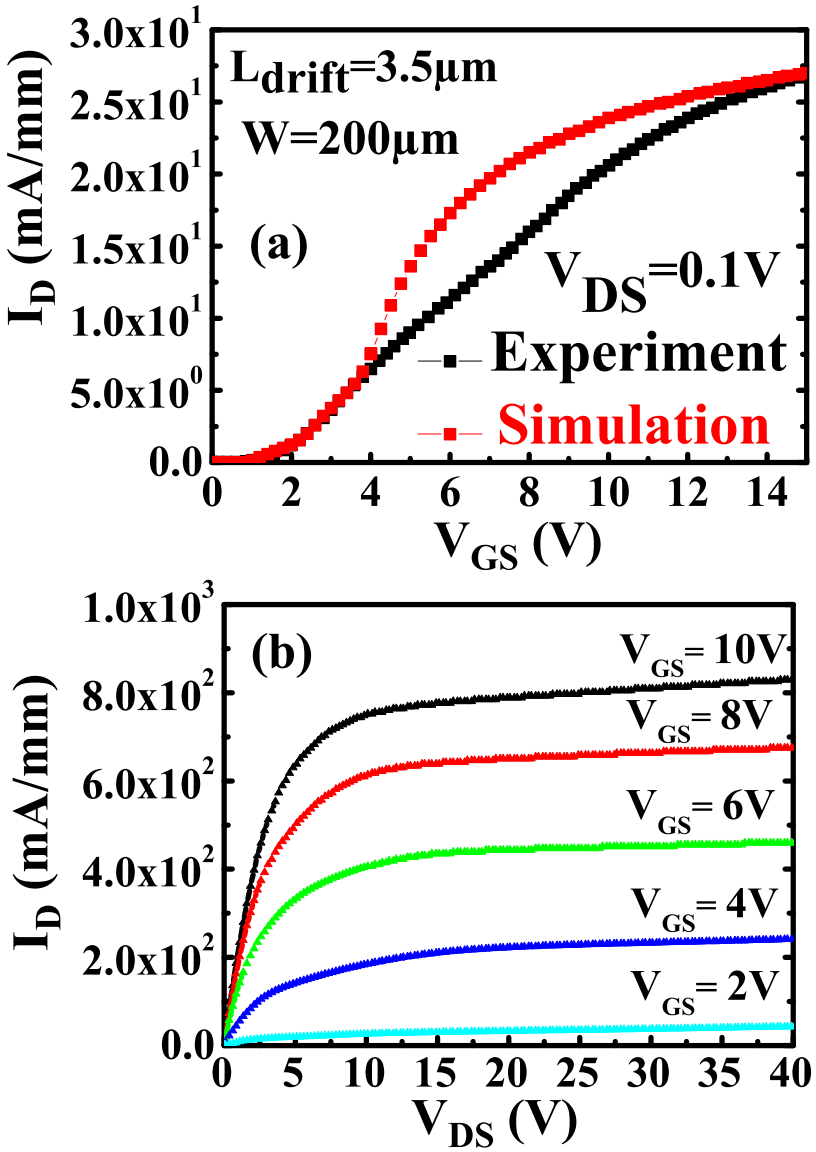


Figure 3: (a) Transfer (I_D-V_{GS}) characteristics of the SJ-MGFET showing the comparison between the experiment and the simulations at V_{DS} = 0.1 V with a trench depth (W_{side}) of 2.7 μm. (b) Output (I_D-V_{DS}) characteristics of the SJ-MGFET with L_{drift} = 3.5 μm, W_{side} = 2.7 μm , and W = 200 μm at indicated gate voltages in a step of 2.0 V.

shown in Fig. 1. This leads to asymmetry in a SJ unit and results in a charge imbalance in the drift region. In order for the SJ unit to sustain a maximum

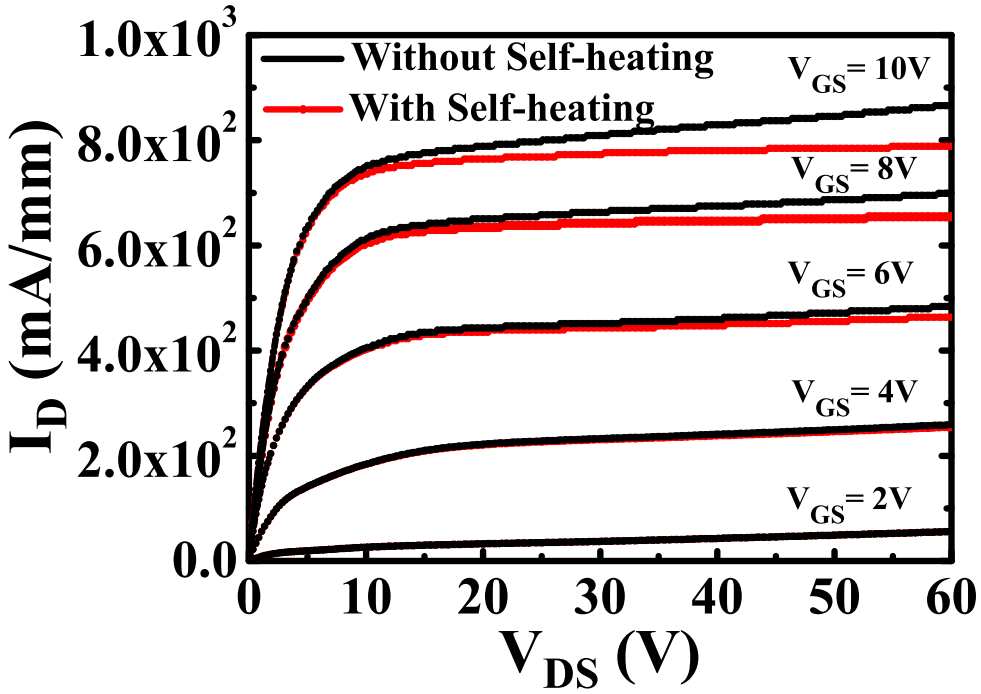


Figure 4: Output characteristics of the SJ-MGFET with $L_{drift} = 3.5$ μm and W = 200 μm obtained from the thermal simulations at indicated gate voltages in a step of 2.0 V comparing simulations when the self-heating is excluded and included.

voltage and achieve a fully depleted drift region before a breakdown, the total charge Q has to satisfy the relation [2]:

$$Q < \varepsilon_s(\frac{E_C}{q}), \tag{3}$$

where E_C is the critical electric field of silicon, ε_s is the permittivity of silicon and q is the elementary charge. In other words, the doping concentration of the p-pillar (N_p) should be greater than the n-pillar (N_n). This will ensure that the average charge in the depleted SJ unit tends toward zero. Fig. 6 depicts the effect of charge imbalance in the SJ unit on the BV. The variation along the drift region has no effect on the charge imbalance. This is due to the fixed ratio between cross-sectional areas of the two SJ pillars. It is also observed that the charge balance condition tends to shift toward the highly doped acceptor side for each dose variation in the p-pillar region. This is a result of substrate-assisted depletion effect and a volume difference between the p-pillar and the n-pillar in the SJ region.

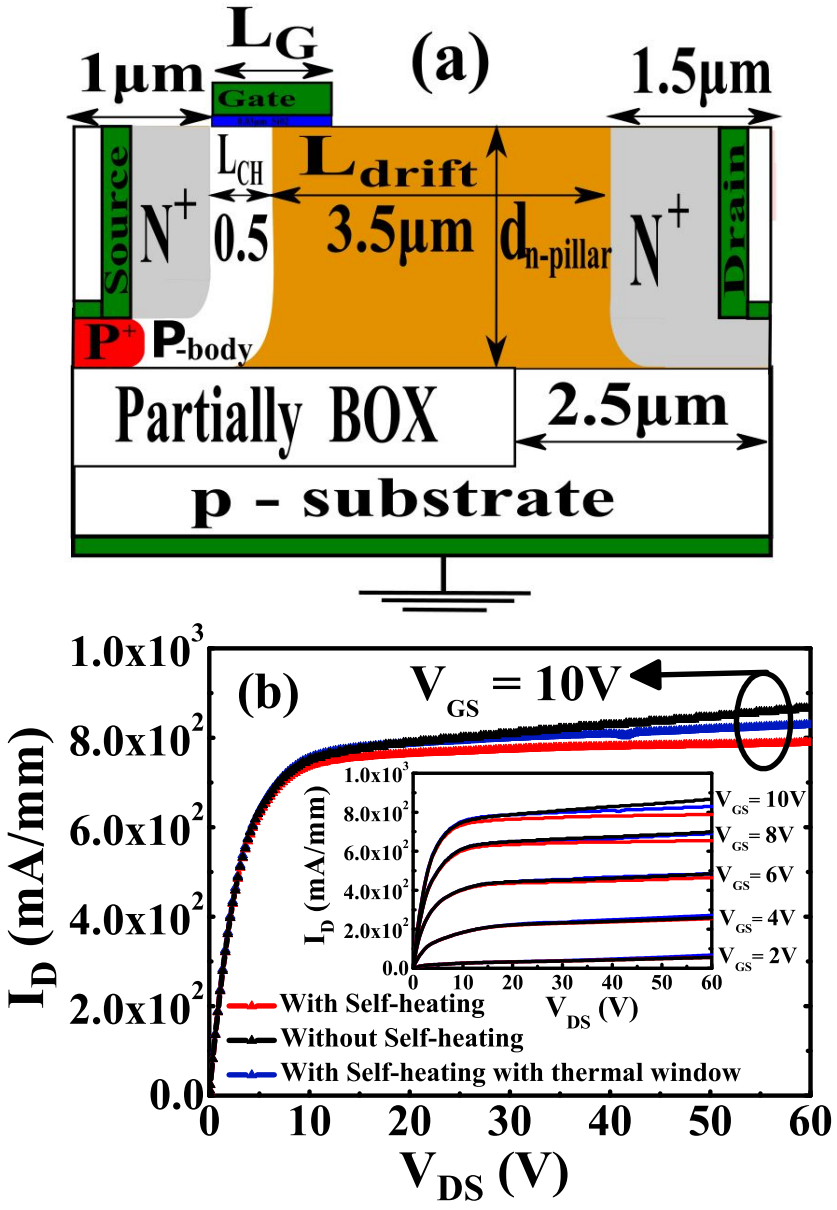


Figure 5: (a) 2D Schematic of the partially buried oxide with opening at the drain for L_{drift}= 3.5 μm, and W_{side} = 2.7 μm. (b) I_D-V_{DS} characteristics of the electro-thermal simulations comparing a transistor design with and without the thermal window at V_{GS} = 10 V and V_{DS} = 50 V for L_{drift}= 3.5 μm, W_{side} = 2.7 μm, and W= 200 μm.

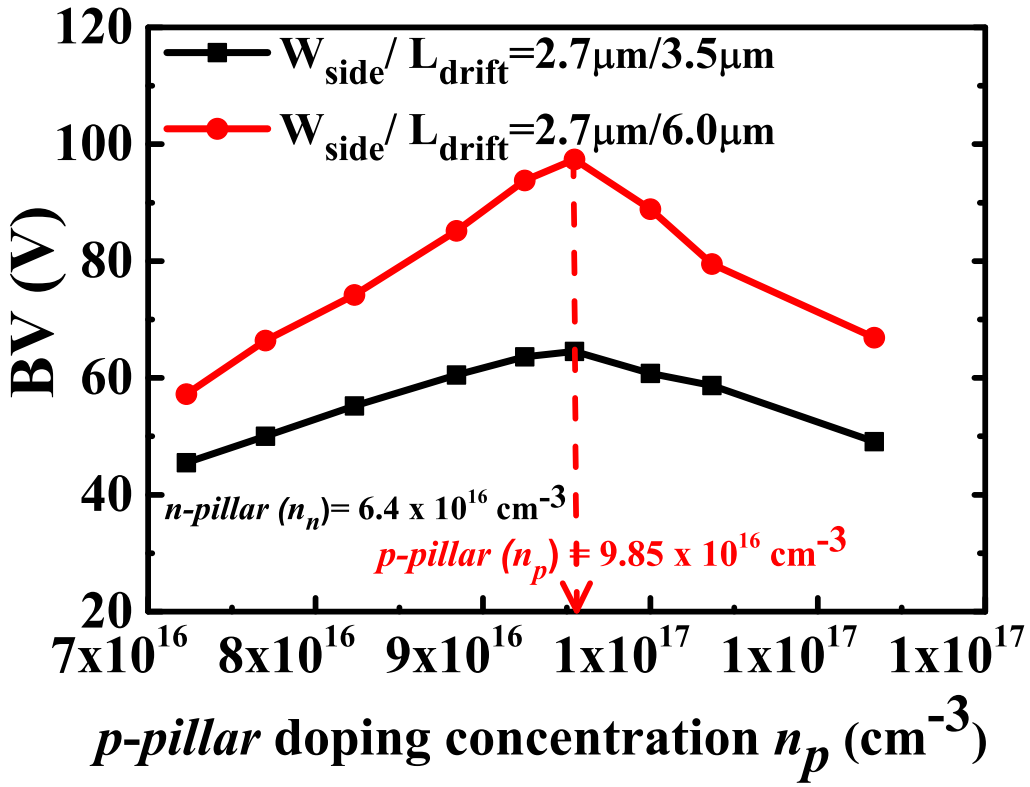


Figure 6: The effect of charge imbalance on BV in SJ-MGFET with W_{side} = 2.7 μm and W_n = W_p = 0.3 μm, comparing two device widths of L_{drift} = 3.5 μm and 6.0 μm during the off-state.

Fig. 7 (a) shows the contour plot of the electric field at the surface of the SJ-MGFET during the off-state under a charge balance with $W_n = W_p = 0.3$ μm. High electric field can be observed at the gate edge under W_{top}, with n– and p– pillars mutually depleted resulting in uniform distribution of electric field in the drift region. The SJ-MGFET will undergo avalanche breakdown at the junction between p-body and n-pillar when the electric field reaches a critical value, E_C of approximately 5.5×10^5 V/cm . Fig. 7 (b) shows the lateral electric field distribution at the surface during off-state under charge balance condition. The fully depleted SJ drift region shows two peak electric fields (PK_1 and PK_2) at the gate (W_{top} and W_{side}) edge and p-pillar/N+ drain junction respectively. The surface peak electric field at the edge of the gate electrode can be relaxed by using a metal field plate aiming at redistributing electron current crowding near the junction between p-body and n-pillar.

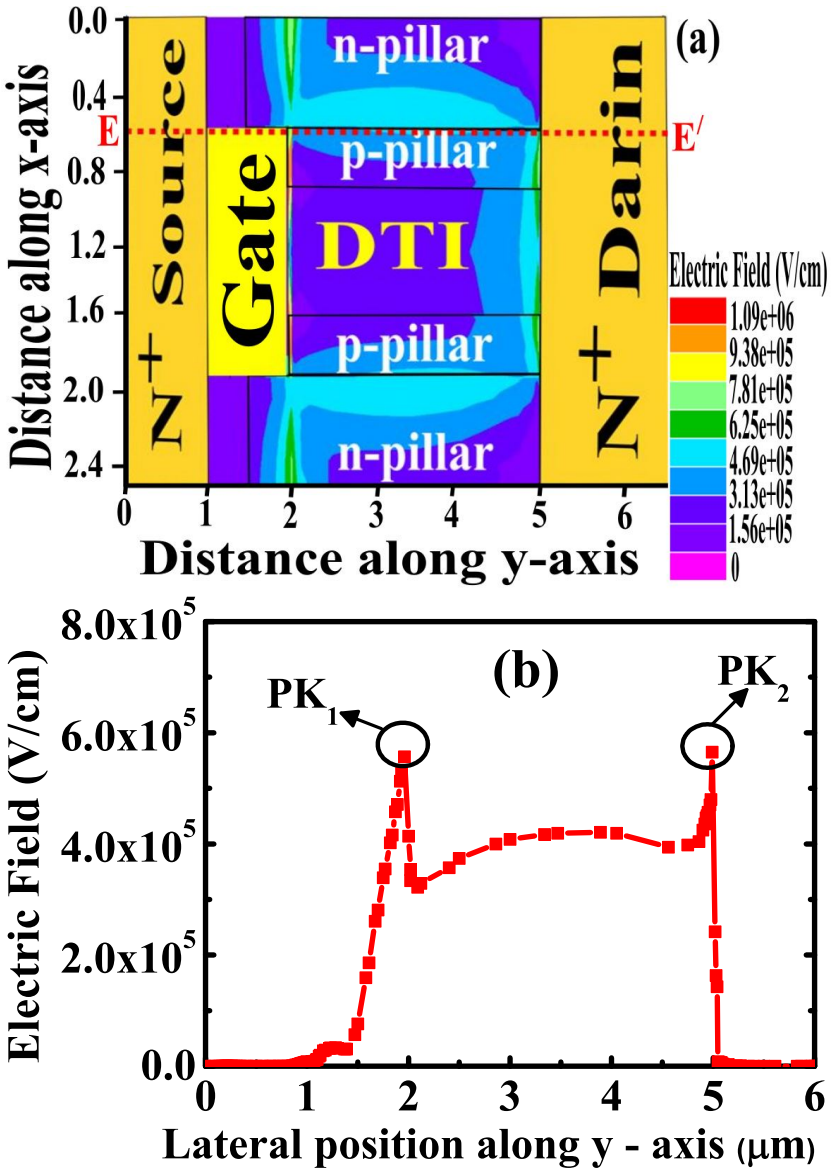


Figure 7: (a) Contour plot of the electric field distribution at the surface of the SJ-MGFET during the off-state with L_{drift}= 3.5 μm, and W_{side} = 2.7 μm under a charge balance condition. (b) Lateral electric field distribution at the surface of a drift region along the E-E′ cutline between the interface of n– and p–pillars during the off-state under the charge balance condition with W_{side} = 2.7 μm, L_{drift}= 3.5 μm, and $d_{n-pillar}$ = 3.6 μm.

Fig. 8 (a) shows the equi-potential distribution in the device along the A-A′ cut-line during the off-state under a charge balance near the edge of the drain, the slope of the potential verifies an horizontal increment at breakdown voltage in the SJ structure. A breakdown of 65 V was obtained for W_{side} = 2.7 μm, and L_{drift}= 3.5 μm which corresponds to an average lateral electric field of 18.6 V/μm. Fig. 8 (b) illustrates the specific on-resistance profile along A-A′ cut-line of the SJ-MGFET under the charge balance condition with W_{side} = 2.7 μm, and L_{drift}= 3.5 μm. In comparison with conventional SJ-LDMOSFET technology at the same voltage rating and channel length, the SJ-MGFET offers $R_{on,sp}$ of 8.9 $\mu\Omega.cm^2$ and 0.204 $m\Omega.cm^2$ at both channel and drift regions respectively; corresponding to 88% and 56% reduction [7].

Fig. 9 (a) shows the C_g and G_g of the device in the C-V simulation. In the on-state when the gate is reverse biased, the P-body area situated in the proximity of the gate is switched on to an accumulation state and the *n*-pillar is maintained in an inversion state; when the gate is forward biased, the P-body area changes to an inversion state and the *n*-pillar switches to an accumulation state. An overall C_g of approximately 0.01 pF was achieved, which is the summation of C_{gs} and C_{gd}. Fig. 9 (b) depicts the dependence of the output capacitance ($C_{oss} = (C_{ds} + C_{gd})$) on the drain source voltage (V_{ds}) during small-signal AC analysis at 1 Mhz. With drain biases of $V_{ds} < 22V$; drain-source capacitance (C_{ds}) is the dominant factor, in which the C_{oss} is directly proportional to it. However, as the drain voltage increases beyond $V_{ds} > 30V$; the gate-drain capacitance (C_{gd}) plays an active role in the total resultant effect of C_{oss} of the device. In the C_{oss} - V_{ds} curve, at $V_{ds} = 50V$, the SJ-MGFET exhibits $R_{on,sp}.C_{oss}$ = 445 $m\Omega$.pF which is approximately one-tenth and one-fifth of the D-MOSFET and FP-MOSFET respectively [20]. Fig. 10 (a)and Fig. 10 (b) show the gate turn-on transient simulation when the device is ramped to V_{gs} = 10V and V_{ds} = 50V neglecting the circuit resistance R_c and stray inductance L_s. A capacitance of 0.5pF is specified to emulate the gate drain interconnect and an external resistor of 1kΩ is used to simulate a load resistance between drain and drive. Hence, the SJ-MGFET offers a better switching turn-off time (t_{off}) of approximately 1.0ns compared with D-MOSFET (t_{off} = 18.5ns) and FP-MOSFET (t_{off} = 1.1ns) at the same voltage rating [20].

The trade-off between BV and $R_{on,sp}$ for the simulated SJ-MGFET, fabricated SJ-LDMOSFET and SJ-FinFET are compared with the ideal silicon limit and with several conventional LD-MOSFETs in Fig. 11. The simulations of the SJ-MGFET show a low $R_{on,sp}$ of 0.21 $m\Omega.cm^2$ at a BV_{dss} of

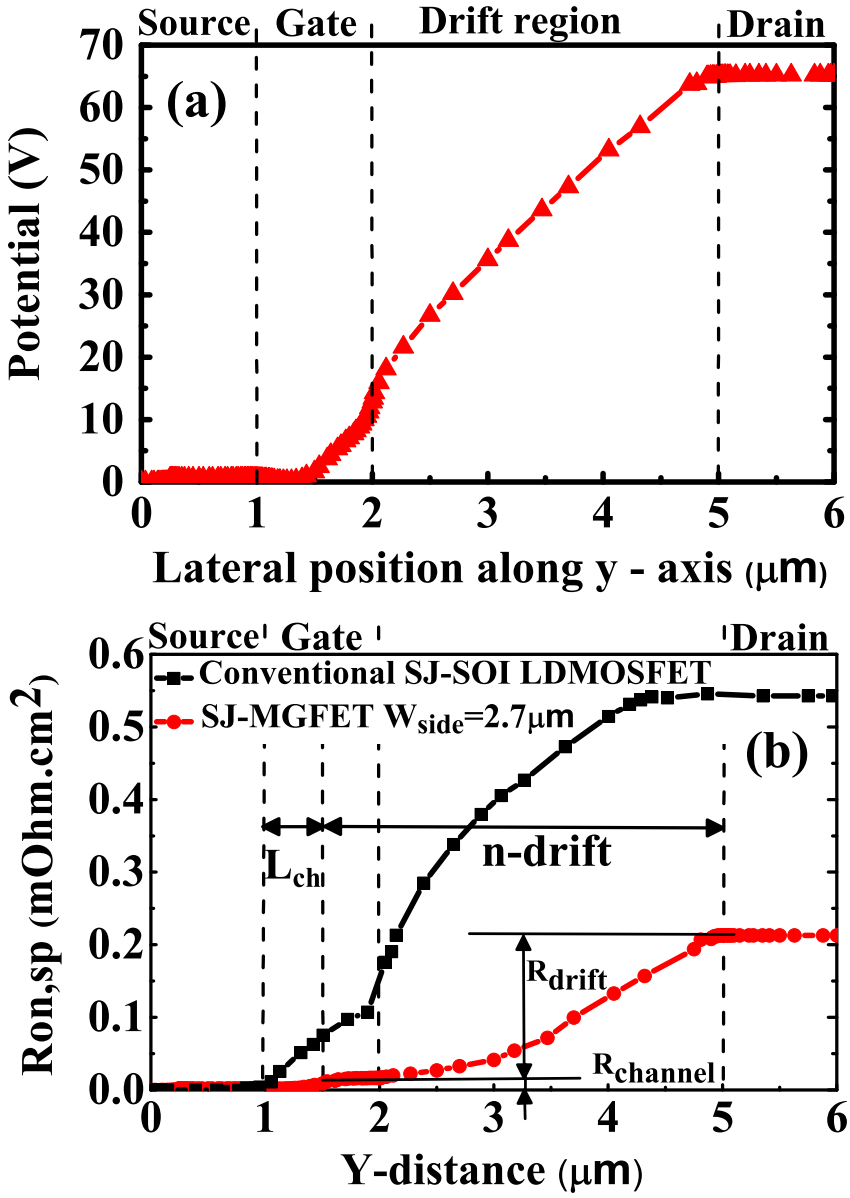


Figure 8: (a) Equi-potential distribution profile along the A-A′ cut-line in the off-state under a charge balance for the SJ-MGFET with L_{drift} of 3.5 μm, $W_n = W_p = 0.3$ μm, and $W_{side} = 2.7$ μm. (b) $R_{on,sp}$ profiles along the A-A′ cut-line in the on-state for the SJ-MGFET with L_{drift} of 3.5 μm, $W_n = W_p = 0.3$ μm, and $W_{side} = 2.7$ μm.

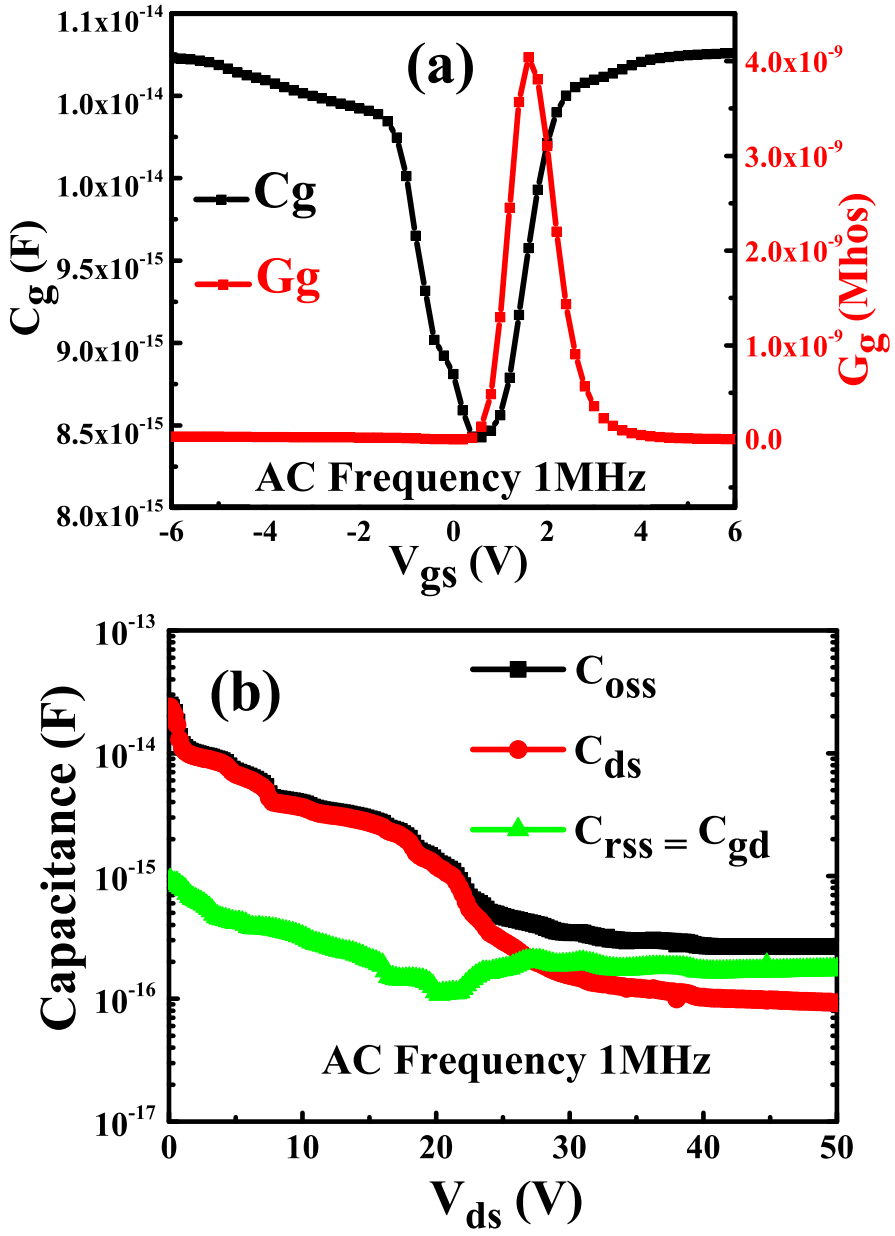


Figure 9: (a) Gate capacitance and conductance plotted as function of gate-source voltage V_{gs}, at AC 1 MHz with $L_{drift} = 3.5\ \mu$m, $W_{side} = 2.7\ \mu$m. (b) The dependence of the C_{oss}, C_{rss} and C_{ds} on the V_{ds} at small signal AC analysis of 1 Mhz.

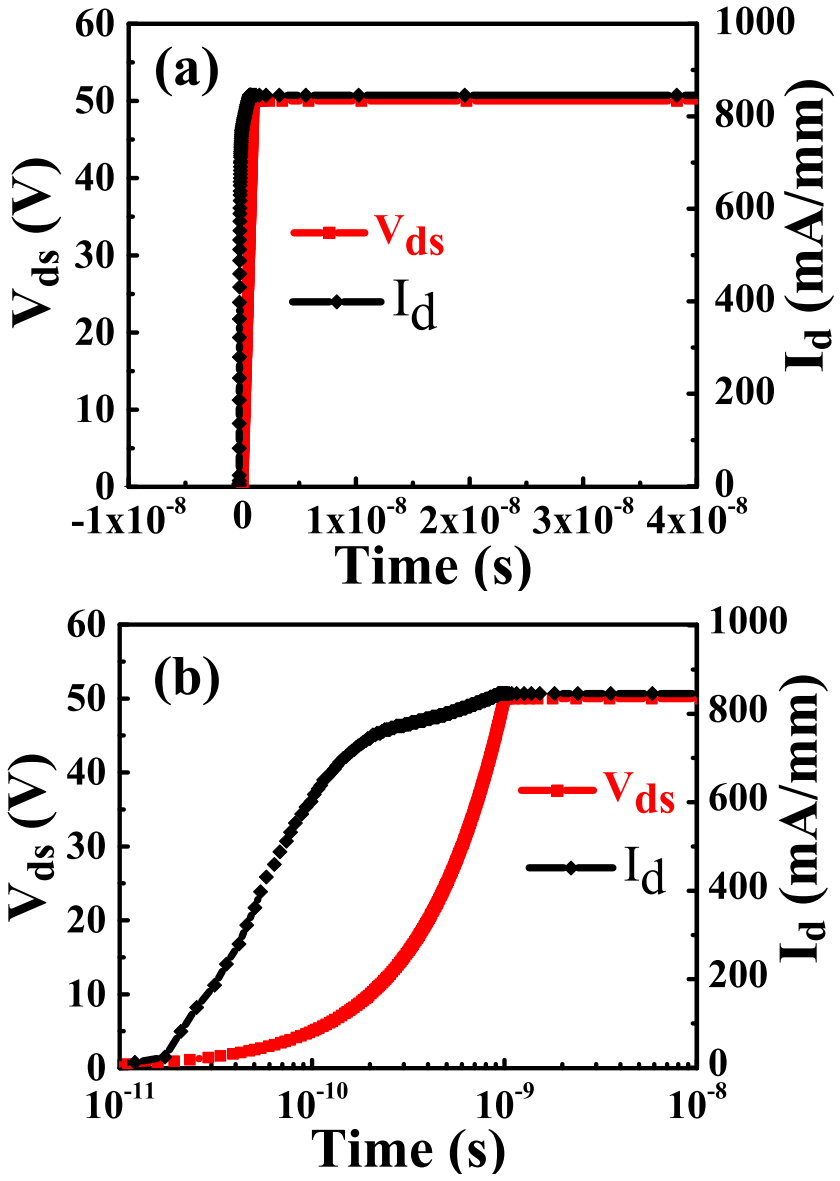


Figure 10: Switching waveforms from gate turn-on transient simulation with the device ramped to V_{gs} = 10V and V_{ds} = 50V (a) time in linear scale (b) time in log scale.

65 V with $d_{n-pillar}$ = 3.6 μm and L_{drift} = 3.5 μm. This leads to 68% and 52% reduction in $R_{on,sp}$ compared to the fabricated SJ-LDMOSFETs and SJ-FinFET at the same BV.

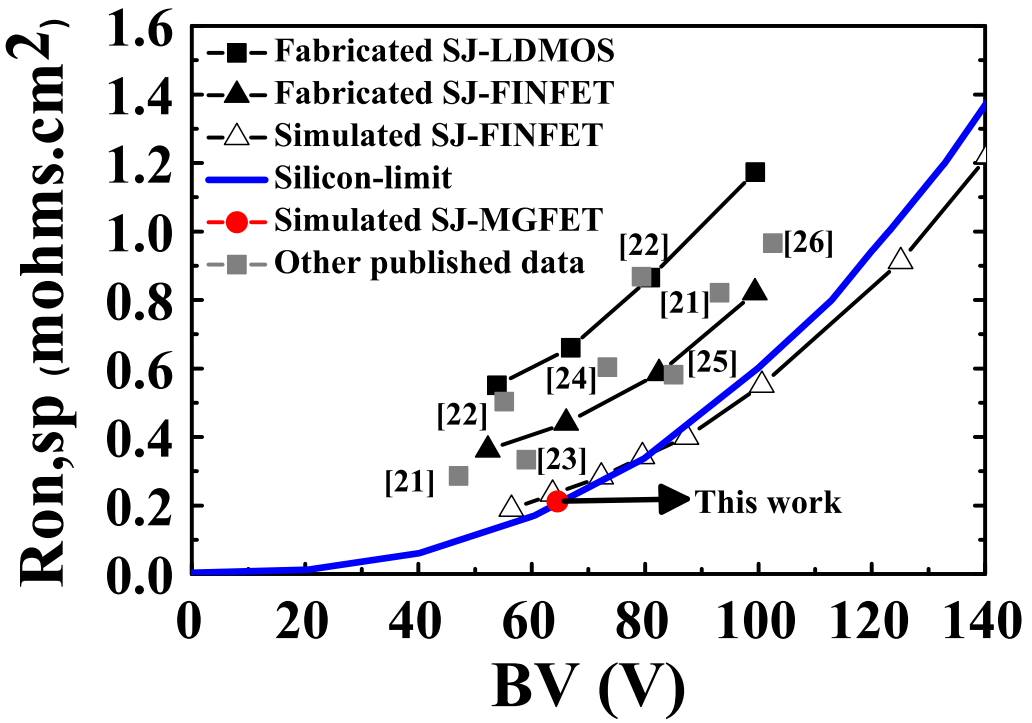


Figure 11: Specific on-resistance as a function of the breakdown voltage of the optimised SJ-MGFET compare with reported conventional LDMOSFETs [21, 22] and conventional SJ-LDMOSFETs [23, 24, 25, 26] devices.

5. Conclusion

The optimisation of doping profile of the 1 μm gate length SJ-MGFET using Silvaco TCAD simulations has shown that the FoM of this non-planar transistor can be substantially improved. The drive current has increased by 41% from 380 mA/mm to over 650 mA/mm, while the off-current decreased from 4×10^{-2} mA/mm to 2×10^{-4} mA/mm respectively [6], demonstrating a big advantage of the multi-gate device architecture to reduce leakage current. The optimisation of the SJ-MGFET doping profile gives an on-off ratio of 5×10^{6} with a saturation drain current of approximately 1000 mA/mm obtained at a drain voltage of 10 V and a gate voltage of 20 V. The application of 3-D TCAD simulations of the SJ-MGFET have been able to optimise the overall device design for a better trade-off between the BV and the $R_{on,sp}$ for a sub-100 V rating application. The optimised SJ-MGFET has achieved 15% reduction in $R_{on,sp}$ from 0.25 mΩ.cm^2 to 0.21 mΩ.cm^2 when compared

with a simulated SJ-FINFET at a BV_{dss} of 65 V [6]. With the trench gate and optimised fully-depleted SJ multi-gate architecture, the structure can offer a superior performance in achieving a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM.

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