Scaling and Optimisation of Lateral Super-Junction Multi-Gate MOSFET for High Drive Current and Low Specific On-Resistance in Sub – 50 V Applications

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Abstract

The scaling of a non-planar super-junction (SJ) Si MOSFET based on SOI technology for low voltage rating applications (below 50 V) requires a subsequent optimisation of SJ unit. The scaling and the SJ optimisation are carried out with physically based commercial TCAD device simulations by Silvaco. The study is based on a meticulous calibration of drift-diffusion simulations against experimental characteristics of a 1 μm gate length SJ multi-gate MOSFET (SJ-MGFET) aiming at improving density, switching speed, drive current, breakdown voltage (BV), and specific on-resistance ($R_{on,sp}$). We investigate scaling of the device architecture to improve the device performance by optimizing doping profile to achieve an avalanche-enabled device under a charge balanced condition. The optimised SJ-MGFETs scaled by a factor of 0.5 and 0.25, with a folded alternating U-shaped n/p-SJ drift region pillar of a width of 0.3 μm and a trench depth of 2.7 μm, achieve a low specific on-resistance ($R_{on,sp}$) of 7.68 $m\Omega.mm^2$ and 2.24 $m\Omega.\ mm^2$ ($V_{\mathrm{GS}} = 10\ V$) and BV of 48 V and 26 V, respectively. The scaled 0.5 μm and 0.25 μm gate length SJ-MGFETs offer a transconductance (g_m) of 20 mS/mm and 56 mS/mm at a drain voltage of 0.1 V, respectively, greatly improving the levels of integration in a CMOS architecture.

Keywords: Super-junction (SJ), silicon-on-insulator (SOI) power MOSFETs, short-channel effect (SCE), breakdown voltage (BV), specific on-resistance ($R_{on,sp}$).

1. Introduction

Technological improvement in the CMOS architecture design has resulted in the scaling of Power Integrated Circuit (PIC) devices aiming at improving physical density of transistors per chip area, switching speed and power capability. The dimension of VLSI chip is reduced by a factor of 0.7 in each technology generation, thereby ensuring more chips per wafer and greatly reduced overall cost of VLSI [1]. The complementary advantage of device dimension reduction ensures that the drive current increases linearly as channel length decreases, and switching losses decrease as the gate capacitance decreases. In order to sustain these two benefits simultaneously and not compromising other parameters, the overall device dimension has to be scaled down rather than the physical channel length only [2]. Scaling of LDMOS (Lateral Double Diffused MOSFETs) technology based on super-junction (SJ) concept has ensured a high transconductance with improved frequency response and a low specific on-resistance ($R_{on,sp}$) for applications such as power management, domestic and office electronics appliances, automotive, military, and industrial control [3]. The two dimensional (2-D) effects of scaling of the gate oxide thickness (t_{ox}), buried oxide (BOX) and silicon thickness in short-channel (SC) ultrathin SOI MOSFETs for better suppression of junction leakage current and power has been reported [4, 5]. However, the scaling theory applicable to bulk MOSFETs and single-gate MOSFETs cannot be fully implemented in SJ multi-gate SOI MOSFETs, because of the disparity in the distributions of electric field as a result of the asymmetric SJ device doping profile [6, 7, 8].

In this work, we examine the three dimensional (3-D) effects of transistor scaling by a factor S of non-planar SJ silicon MOSFET technology to be used as integrated power transistors with applications in power amplifiers and switching. We show that the scaling requires a subsequent optimisation of the SJ unit. The scaling and the SJ optimisation of a non-planar SJ silicon MOSFET is performed by physically based 3-D TCAD simulations [9]. We have reported the calibrated and optimised SJ-MGFET [10], based on the experimental characteristics of non-planar lateral SJ multi-gate MOSFET (SJ-MGFET) fabricated within a silicon-on-insulator (SOI) technology [11] by reproducing its I-V characteristics and the breakdown voltage (BV). The experimental characteristics are analysed with a different drift-diffusion (DD) transport approach in the simulation to achieve a better calibration aiming at reducing the device dimension and improve major de-

vice figures-of-merit (FoM) including drive current, switching capability, BV, and specific on-resistance ($R_{on,sp}$). The structure of the paper is as follows: Section II describes the concept, structure and main characteristics of the SJ-MGFET device, Section III the TCAD simulation methods. Section IV discusses scaling approach, results, device performance, and device design optimisation. Section V summarises the main conclusions of this work.

2. Device Structure of the SJ-MGFET

The investigated SJ-MGFETs have a complex 3-D design permitted by a non-planar technology [12] with an embedded deep trench gate and heavily doped alternating U-shaped n-type and p-type doping pillars forming a SJ drift region length of L_{drift} with a pillar height of $d_{n-pillar}$ [11]. The whole transistor structure is grown on a buried oxide layer to mitigate the effect of substrate-assisted depletion (SAD) [13, 14, 15]. This silicon-on-insulator (SOI) SJ-MGFET has a 1 μm gate length (L_{gate}) with a 0.5 μm channel (L_{ch}) length underneath. The gate is deep trenched to create a top surface with a width of W_{top} and a trench side wall of W_{side} width to enclosure the channel (non-planar technology). This embedded trench gate structure ensures reduction of the channel resistance and redistribution of electron current crowding under the gate, near the peak of the n-pillar in a SJ unit. We have carefully investigated the trench gate depths in the structure, ranging from 1.5 μm - 3.0 μm in a step of 0.3 μm, and observed that the difference in the doping concentration of the SJ n– and p–pillars becomes smaller as the trench depth is increased [16]. To have an effective conducting pathway to the SJ drift region, W_{top} and W_{side} of 0.6 μm and 2.7 μm are chosen in this study. Deep trenched source and drain contacts provide an effective 3-D uniform current density distribution in the n–pillar region with a deep trench isolation (DTI) separating each SJ unit. The doping concentration of n– and p–pillars are expressed as n_n and n_p, respectively, with their corresponding widths referred to as W_n and W_p.

The schematic of the device simulation domain is illustrated in Fig. 1 showing the 3-D geometry of the investigated $1\mu m$ gate length SJ-MGFET having a width of 200 μm and a drift length of 3.5 μm, respectively. Fig. 2 shows cross-sectional views defined in Fig. 1 as follows: (a) the 2-D structure of the 1 μm gate length SJ-MGFETs having $L_{\text{ch}} = 0.5\ \mu m$ and $L_{\text{drift}} = 3.5\ \mu m$ with source and drain contact lengths of 1.0 μm and 1.5 μm, respectively, along a A - A$'$ cutline at the middle of the n-pillar in the SJ unit; (b) the 2-D

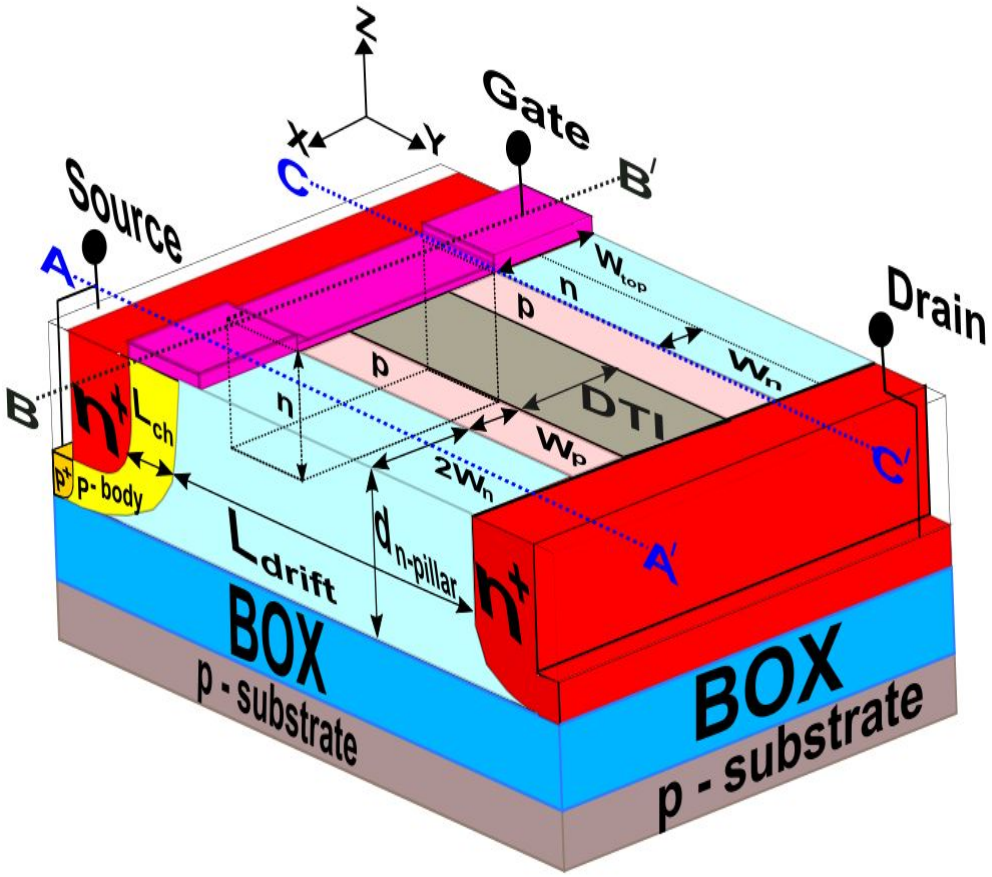
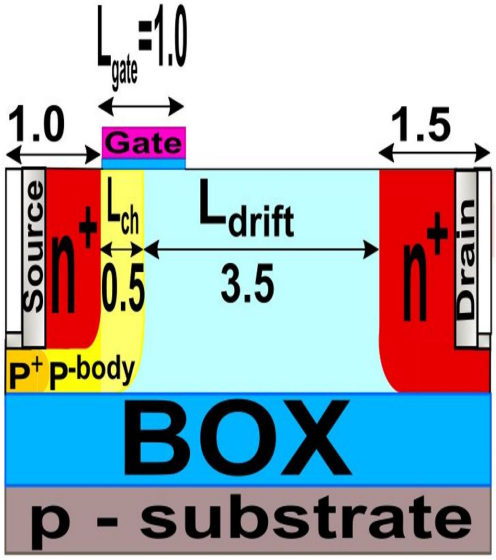
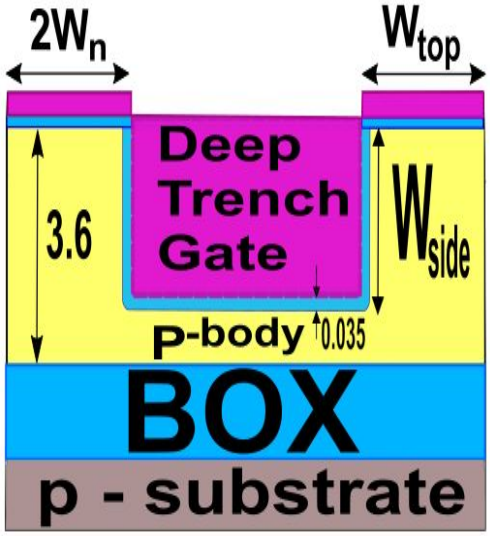


Figure 1: 3-D geometry of the investigated 1 μm gate length SJ-MGFET.

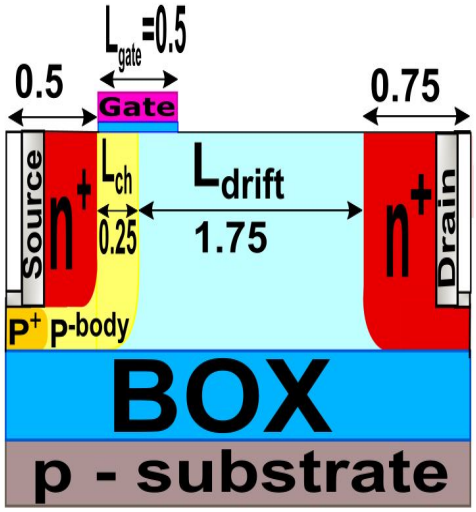
structure at a B - B′ cutline, midpoint of the gate length in Fig. 1 showing a formation of the W_{top} and W_{side} enclosure, with $W_{\text{top}} = 2W_n$, by the embedded deep trench gate structure in the p-body region of the device; (c) the 2-D structure of the scaled 0.5 μm gate length SJ-MGFET having $L_{\text{ch}} = 0.25$ μm, and $L_{\text{drift}} = 1.75$ μm with source and drain contact lengths of 0.5 μm and 0.75 μm, respectively, along a cutline at the middle of the n-pillar in the SJ unit; (d) the 2-D structure of the scaled 0.25 μm gate length SJ-MGFETs having $L_{\text{ch}} = 0.125$ μm, and $L_{\text{drift}} = 0.875$ μm with source and drain contact lengths of 0.25 μm and 0.375 μm, respectively, along a cutline at the centre of the n-pillar in the SJ unit.



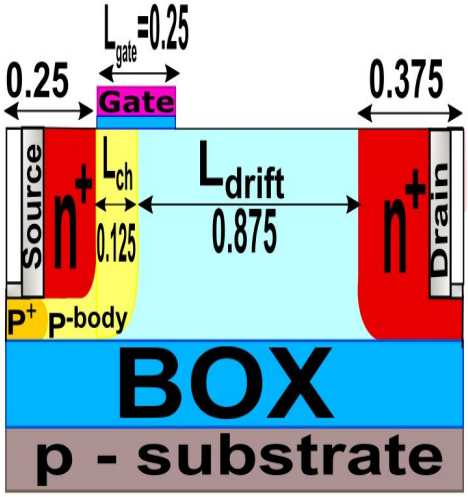
(a) Cross section: A - A′



(b) Cross section: B - B′



(c) 2-D lateral view of the 0.5 μm gate length SJ-MGFET.



(d) 2-D lateral view of the 0.25 μm gate length SJ-MGFET.

Figure 2: The cross-sectional views at the indicated locations in the investigated 1 μm gate length SJ-MGFET and pictorial view of the proposed 0.5 μm and 0.25 μm gate length SJ-MGFETs.

We have carefully examined different scaling approaches in all dimensions of the 3-D device structure. We observe that a scaling of the device vertically (along z-axis) will degrade its trench-gate design because W_{side} of the trench gate structure accounts for about 75% of the SOI body [16, 17]. A narrowing down the buried oxide (BOX) and the p-substrate thickness will induce a junction leakage current, degrade the current during self-heating, and increase the effect of substrate-assisted depletion (SAD) [13, 18]. Scaling the structure along x-axis will minimise the widths (W_n and W_p) of the SJ n– and p– pillars. However, the channel resistance, which play a crucial role in low voltage applications, becomes comparable to the drift resistance as a result of the minimum pillar width in the SJ drift region becoming similar to the built-in depletion region. This limits the reduction of the on-resistance due to a minimum pillar width/height ratio in the SJ unit [19]. Consequently, design variations of the SJ transistor n– and p– pillar widths are technologically limited [16, 20].

The scaling down of the 1.0 μm gate length SJ-MGFET structure laterally (along the y-axis) by scaling the channel length, the gate length, the gate oxide thickness, and the SJ drift unit length by a factor S to shrink the gate length of 1.0 μm to 0.5 μm and 0.25 μm is examined in our simulations. Here, we aim to improve a major device figures-of-merit (FoM) including drive current, switching capability, BV and specific on-resistance ($R_{on,sp}$). In the simulations, a large channel doping is employed in the scaled down structures in order to minimise the maximum depletion-layer width (W_{dm}) and suppress short-channel effects (SCE) [21, 22, 23]. However, this has an adverse effect on the input capacitance due to an increase in threshold voltage (V_{th}) associated with a high channel doping. To maintain electrostatic integrity of the channel potential by the gate, we reduce the gate oxide thickness by the same factor S of 0.5 and 0.25 to compensate for a loss of gate capacitance. The peak doping concentrations in p-type substrate and n-type source/drain contact are 1.0×10^{15} cm^{-3}, and 1.0×10^{20} cm^{-3}, while W_n and W_p are of equal widths of 0.3 μm, respectively.

3. 3-D TCAD Simulations of the SJ-MGFET

The study is carried out with a 3-D commercial device simulator Atlas by Silvaco [9] using a drift-diffusion (DD) transport model. We incorporated the classical DD model which includes Caughey-Thomas electron mobility (ANALYTIC) model, parallel electric field dependence (FLDMOB) model along with Shockley-Read-Hall (SRH) recombination. The Caughey-Thomas electron mobility model [24] is given by:

$$\mu_e = \left[\mu_1 \left(\frac{T_L}{300K} \right)^{\alpha_e} + \frac{\mu_2 \left(\frac{T_L}{300K} \right)^{\beta_e} - \mu_1 \left(\frac{T_L}{300K} \right)^{\alpha_e}}{1 + \left(\frac{T_L}{300K} \right)^{\gamma_e} \left(\frac{N}{N_{\text{crit}}} \right)^{\delta_e}} \right] \tag{1}$$

where μ_e is the doping and temperature dependent at a low field electron mobility, while μ_1 and μ_2 are the first and second term mobility components, N_{crit} is the electron concentration between μ_1 and μ_2. N is the total impurity concentration, T_L is the lattice temperature, and α_e, β_e, γ_e, and δ_e are doping and temperature coefficients. We have used the following electron mobility parameters: $\mu_1 = 55.24\ cm^2/V.s$, $\mu_2 = 1429.23\ cm^2/V.s$, $N_{\text{crit}} = 1.072 \times 10^{17}\ cm^{-3}$, $\alpha_e = 0.0$, $\beta_e = -2.3$, $\gamma_e = -3.8$, $\delta_e = 0.73$. All these are default parameters for the Caughey-Thomas mobility model in Atlas [24]. The parallel electric field dependence model [24] can be expressed as:

$$\mu_e(E) = \mu_1 \left[\frac{1}{1 + \left(\frac{\mu_1 E}{v_{SATn}} \right)^{\beta_{ex}}} \right]^{\frac{1}{\beta_{ex}}} \tag{2}$$

$$v_{\text{SATn}} = \left[\frac{\alpha_{ex}}{1 + \theta_{ex}^{\left(\frac{T_L}{T_{\text{NOMn}}} \right)}} \right] \tag{3}$$

where v_{SATn} is the saturation velocity for electron, μ_1 is the first term low-field electron mobility, E is the parallel electric field, T_L is the lattice temperature, while β_{ex}, α_{ex}, θ_{ex}, and T_{NOMn} are doping and temperature coefficient parameters specified as $\beta_{ex} = 2.0$, $\alpha_{ex} = 2.4 \times 10^7$, $\theta_{ex} = 0.8$, and $T_{\text{NOMn}} = 600$ [9]. Selberherr impact ionization model [25] used in our simulations examines the effect of charge imbalance of a doping concentration in n– and p– pillars of

the SJ unit on BV when the device is in off-state. The model is based on the expression given by:

$$\alpha_n = A_n \exp\left[-\left(\frac{B_n}{E}\right)^{\beta_n}\right] \tag{4}$$

where E is the electric field in the direction of current flow at a particular position in the device. A_n, B_n, and β_n are material parameters defined as $7.03 \times 10^5\ cm^{-1}$, $1.231 \times 10^6\ V/cm$ and 1.0 [9].

We analyse transfer (I_{D}-V_{GS}) and output (I_{D}-V_{DS}) characteristics of the SJ-MGFETs scaled down to 0.5 μm and 0.25 μm gate length. Finally, the doping profile and the 3-D geometry of the SJ-MGFET is optimised to improve the frequency response, drive current, BV, and specific on-resistance ($R_{on,sp}$).

4. Scaling Approach and Structure Optimisation of the Scaled down SJ-MGFET

Figure 3 (a) compares transfer characteristics (I_{D}-V_{GS}) of the experimental [11] and calibrated drift-diffusion simulations at a drain bias (V_{DS}) of 0.1 V. The simulation is in excellent agreement with experimental behaviour having a maximum error of approximately 0.5%, also exhibiting a typical transistor switching characteristics before reaching a saturation point. A threshold voltage of approximately 2.0 V was obtained at a drain bias of 0.1 V by interpolating the linear region of the I_{D}-V_{GS} characteristics with a drain current normalised per width of the non-planar transistor in order to be able to make a fair comparison with the planar SJ-MOSFET technology. Fig. 3 (b) shows the effect of charge imbalance in the SJ unit on the BV during off-state. The charge balance condition tends to shift toward the highly doped acceptor side for each dose variation in the p-pillar region [10]. This is a result of the volumetric difference between the p-pillar and the n-pillar in the SJ region and the substrate-assisted depletion (SAD) effect. A breakdown of 65 V is obtained for $W_{\mathrm{side}} = 2.7\ \mu m$, and L_{drift}= 3.5 μm which corresponds to an average lateral electric field of 18.6 $V/\mu m$. In order to prevent a weak electrostatic integrity in the 0.5 μm and 0.25 μm gate length (L_{gate}) SJ-MGFETs, we optimise the doping profile aiming at achieving a maximum drive current, a minimum leakage current and improve the avalanche capabilities of the scaled devices.

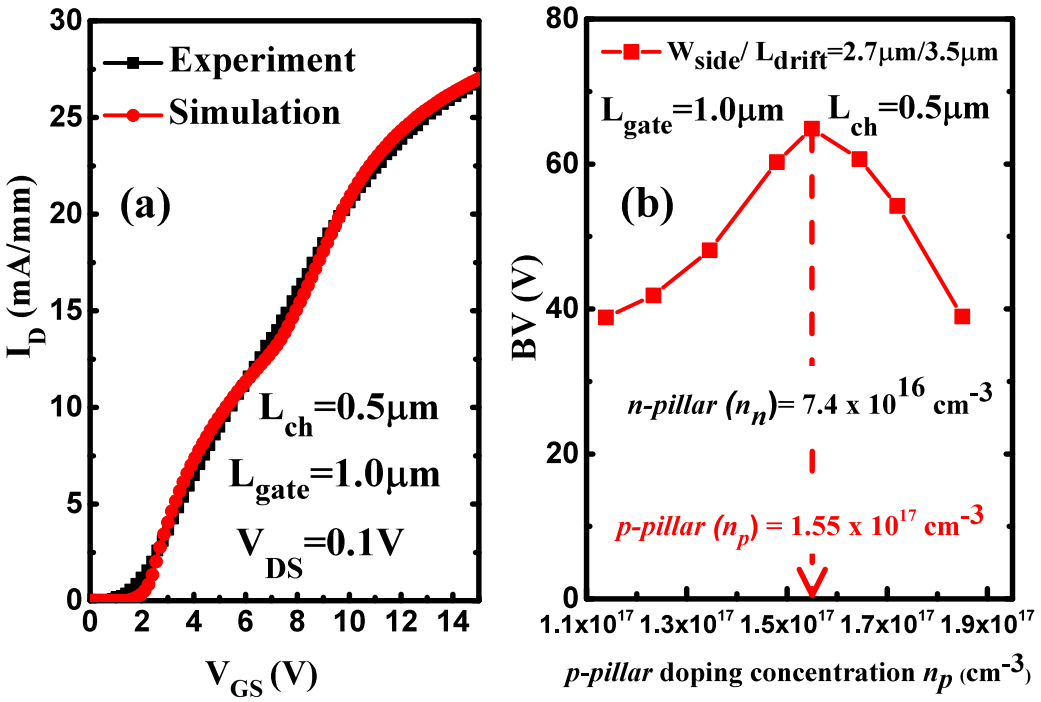


Figure 3: (a) Transfer ($I_{\rm D}$-$V_{\rm GS}$) characteristics of the SJ-MGFET showing a comparison between the experiment [11] and the simulations at $V_{\rm DS}$ = 0.1 V with $L_{\rm gate}$ = 1.0 μm, $L_{\rm drift}$ = 3.5 μm, $W_{\rm side}$ = 2.7 μm , and W = 200 μm. (b) The effect of charge imbalance on BV in SJ-MGFET with $W_{\rm side}$ = 2.7 μm, $L_{\rm drift}$ = 3.5 μm and W_n = W_p = 0.3 μm during the off-state.

Ideally, in transistor technology, the threshold voltage decreases with decreasing channel length. However, in order to offset this threshold voltage decrease and control SCE, the channel doping is increased from 2.5×10^{17} cm^{-3} to 1.0×10^{18} cm^{-3} in the 0.5 μm gate length SJ-MGFET. This doping increase will also improve avalanche capability of the depleted SJ drift region during off-state. The thickness of the gate oxide (t_{ox}) is also reduced from 35 nm to 18 nm to increase the input capacitance.

Figure 4 (a) shows transfer characteristics ($I_{\rm D}$-$V_{\rm GS}$) of the optimised 0.5 μm gate length SJ-MGFET at $V_{\rm DS}$ of 0.1 V with a threshold voltage of 2.0 V. At $V_{\rm GS}$ of 15.0 V with $V_{\rm DS}$ = 0.1 V, a saturation drain current of 38 mA/mm is obtained, resulting in 30% increase when compared with the current reported in an experimental device [11].

Figure 4 (b) shows the output characteristics (I_{D}-V_{DS}) of the 0.5 μm gate length SJ-MGFET. The device exhibits a good current saturation with flat output response at a large range of operational gate voltages. A saturation drain current over 740 mA/mm at V_{GS} of 10 V with $V_{\mathrm{DS}} = 20$ V is extracted.

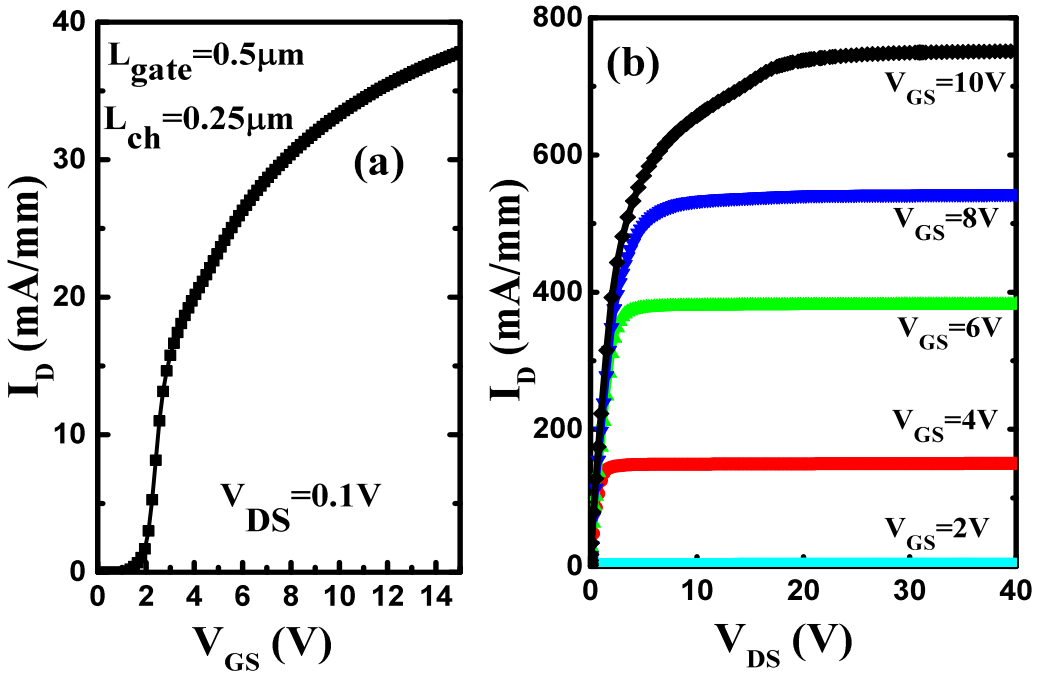


Figure 4: (a) Transfer (I_{D}-V_{GS}) characteristics of the optimised 0.5 μm gate length SJ-MGFET at $V_{\mathrm{DS}} = 0.1$ V with $L_{\mathrm{drift}} = 1.75$ μm and trench depth (W_{side}) of 2.7 μm. (b) Output (I_{D}-V_{DS}) characteristics of the 0.5 μm $L_{_{\mathrm{gate}}}$ SJ-MGFET with $L_{\mathrm{drift}} = 1.75$ μm, $W_{\mathrm{side}} = 2.7$ μm, and $W = 2.46$ μm at indicated gate voltages in a step of 2.0 V.

Figure 5 (a) illustrates the relationship between the BV and the p-pillar doping concentration during charge imbalance in the SJ unit of the 0.5 μm gate length SJ-MGFET when the device is in off-state. The asymmetry of the SJ unit, as a result of the cross-sectional area of the n-pillar (A_n) being larger than that of the p-pillar (A_p) Fig. 1; causes charge imbalance to occur in the device irrespective of the scaling factor. In order for the SJ unit to sustain a maximum voltage and achieve a fully depleted drift region before

a breakdown, the total charge (Q) has to satisfy the relation [19]:

$$Q < \varepsilon_s \left(\frac{E_C}{q} \right) \tag{5}$$

where E_C is the critical electric field of silicon, ε_s is the permittivity of silicon and q is the elementary charge. The SJ-MGFET scaled down to 0.5 μm L_{gate} will undergo avalanche breakdown at the junction between p-body and n-pillar with a breakdown of 48 V, which corresponds to an average lateral electric field of 27.5 $V/\mu m$ for $L_{\text{ch}} = 0.25$ μm, and $L_{drift} = 1.75$ μm. Figure 5 (b) shows I_{D}-V_{DS} characteristics used to determine a BV when the optimised SJ-MGFET scaled down to $L_{\text{gate}} = 0.5$ μm, and $L_{\text{ch}} = 0.25$ μm is off during impact ionisation.

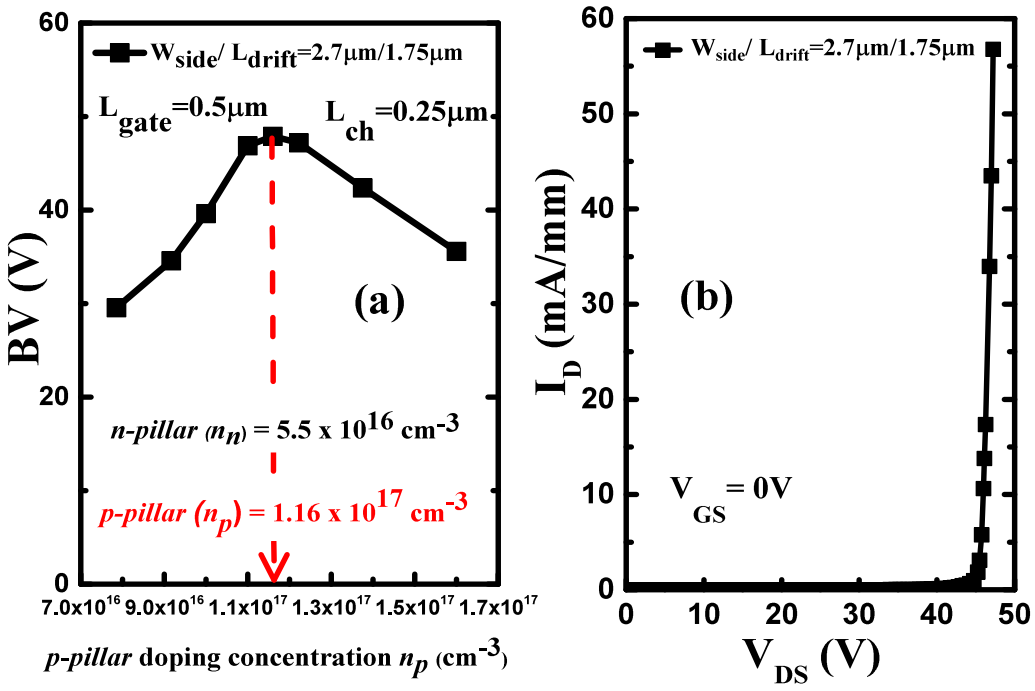


Figure 5: (a) The effect of charge imbalance on the BV in the SJ-MGFET scaled down to 0.5 μm L_{gate} with $W_{\text{side}} = 2.7$ μm, $L_{\text{drift}} = 1.75$ μm and $W_n = W_p = 0.3$ μm during the off-state. (b) The BV during off-state under a charge balance for the SJ-MGFET scaled down to $L_{\text{gate}} = 0.5$ μm, and $L_{\text{ch}} = 0.25$ μm.

The SJ-MGFET scaled by a factor S of 0.25 has a channel length of $L_{\text{ch}} = 0.125$ μm, a gate length of $L_{\text{gate}} = 0.25$ μm, and a length of the drift

region, $L_{\text{drift}} = 0.875\ \mu m$. An oxide thickness ($t_{ox}$) of 35 nm reduced by a factor $S = 0.25$ scales to 9 nm in order to maintain gate electrostatic integrity. This will also compensate for the effect of lowering V_{th} due to the narrowing of channel length and suppress the SCE. In addition, the channel doping is increased from $2.5{\times}10^{17}\ cm^{-3}$ to $1.0{\times}10^{19}\ cm^{-3}$ to prevent a punch-through in the structure.

Figure 6 (a) shows transfer characteristics (I_{D}-V_{GS}) of the optimised SJ-MGFET scaled down to 0.25 μm L_{gate} with an extracted threshold voltage of 3.9 V at V_{DS} of 0.1 V. A saturation drain current of 72 mA/mm is achieved at V_{GS} of 15.0 V and $V_{\text{DS}} = 0.1\ V$, which corresponds to 63% increase when compared with the current reported in experimental device [11]. Figure 6 (b)

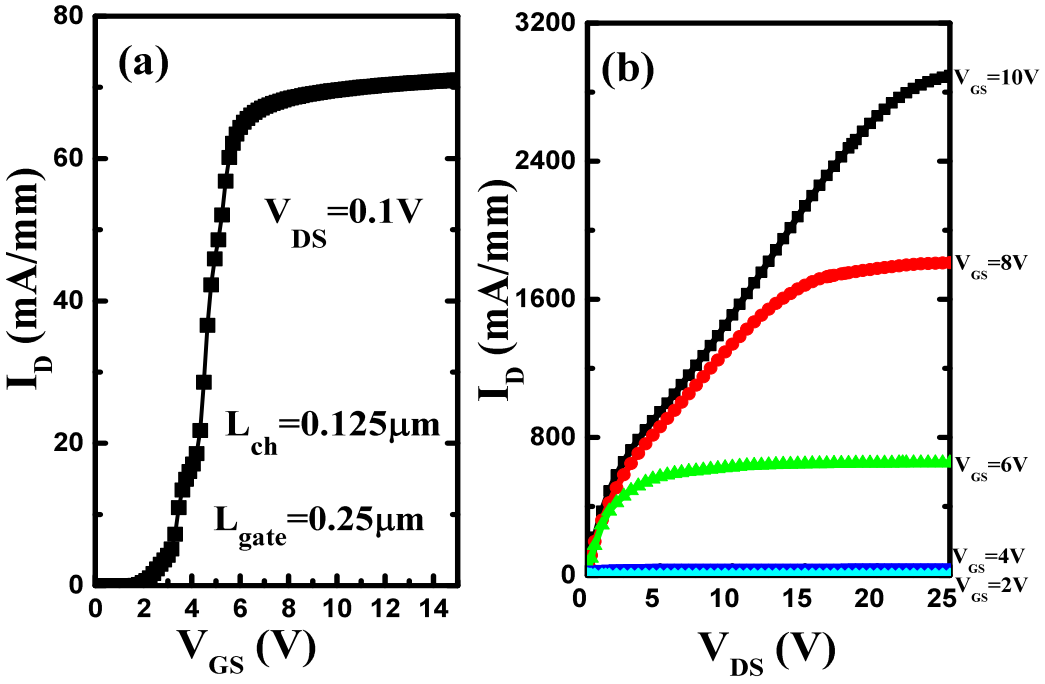


Figure 6: (a) Transfer (I_{D}-V_{GS}) characteristics of the optimised SJ-MGFET scaled down to 0.25 μm L_{gate} at $V_{\text{DS}} = 0.1\ V$ with $L_{\text{drift}} = 0.875\ \mu m$ and trench depth (W_{side}) of 2.7 μm. (b) Output (I_{D}-V_{DS}) characteristics of the SJ-MGFET scaled down to 0.25 μm L_{gate} with $L_{\text{drift}} = 0.875\ \mu m$, $W_{\text{side}} = 2.7\ \mu m$, and $W = 2.46\ \mu m$ at indicated gate voltages in a step of 2.0 V.

shows output characteristics (I_{D}-V_{DS}) of the 0.25 μm gate length SJ-MGFET at various gate voltages in a step of 2.0 V. The I_{D}-V_{DS} characteristics show

a current saturation up to an elevated $V_{\rm GS}$ of 6.0 V. Above $V_{\rm GS}$ = 6.0 V, the vertical electric field from the gate bias increases with the drain bias increase causing a channel resistance and a drain current to be strongly dependent on the drain voltage. This strong dependence is specific to a SJ structure because current flows only through the n-pillar. An elevated drain voltage will cause a voltage drop across a narrow depletion region between the channel end and the n-pillar resulting in a shortening of the channel length. This generates a high electric field in the shortened channel leading to the increase in the drain current with a higher drain voltage. We observe that the drain current increases in the $I_{\rm D}$-$V_{\rm DS}$ characteristics with increasing of $V_{\rm GS}$ compared to the 1 μm gate length device structure with a thicker oxide. However, despite a strengthening of a gate control by the oxide thickness reduction and aggressive doping in the channel, SCE occur in the scaled 0.25 μm gate length device, especially at higher $V_{\rm GS}$s. This is partially a result of increasing effect of the drain induced barrier lowering (DIBL) at very large applied drain voltages [26, 27, 28].

The dependence of BV on the p-pillar doping concentration during charge imbalance is plotted in Figure 7 (a) for the SJ-MGFET scaled down to the 0.25 μm gate length, when the device is in off-state. Figure 7 (b) illustrates determination of a BV of 26 V from $I_{\rm D}$-$V_{\rm DS}$ characteristics for the 0.25 μm gate length SJ-MGFET during the off-state. An average lateral electric field in a drift region (see Fig. 1) of the 0.25 μm gate length SJ-MGFET defined by L_{drift} = 0.875 μm is approximately 30 $V/\mu m$ at a BV of 26 V. We have observed that varying the doping concentration in the SJ unit has a less effect on the BV because there is an optimal doping concentration limit per unit volume upon which the device can be optimised. Figure 8 shows the lateral electric field distributions at the surfaces of the devices with $L_{\rm gate}$ of 1.0 μm, 0.5 μm, and 0.25 μm, respectively during the off-state under charge balance condition along the C - C$'$ cutline. The electric field distribution along the C - C$'$ cutline (the line defined along the junction between n– and p–pillars as defined in Fig. 1) is the field at 10 nm below the surface, from the source to the drain, during the off-state under the charge balance condition. The figure exhibits two peak electric fields at the gate edge and the $p-pillar/n^+$ drain junction in SJ-MGFETs with (a) $L_{\rm ch}$ = 0.125 μm, $L_{\rm gate}$ = 0.25 μm, and $L_{\rm drift}$ = 0.875 μm, (b) $L_{\rm ch}$ = 0.25 μm, $L_{\rm gate}$ = 0.5 μm, and $L_{\rm drift}$ = 1.75 μm, and (c) $L_{\rm ch}$ = 0.5 μm, $L_{\rm gate}$ = 1.0 μm, and $L_{\rm drift}$ = 3.5 μm.

The device avalanche breakdown occurred at the junction between the p-body and the n-pillar when electric field in all the three structures reaches

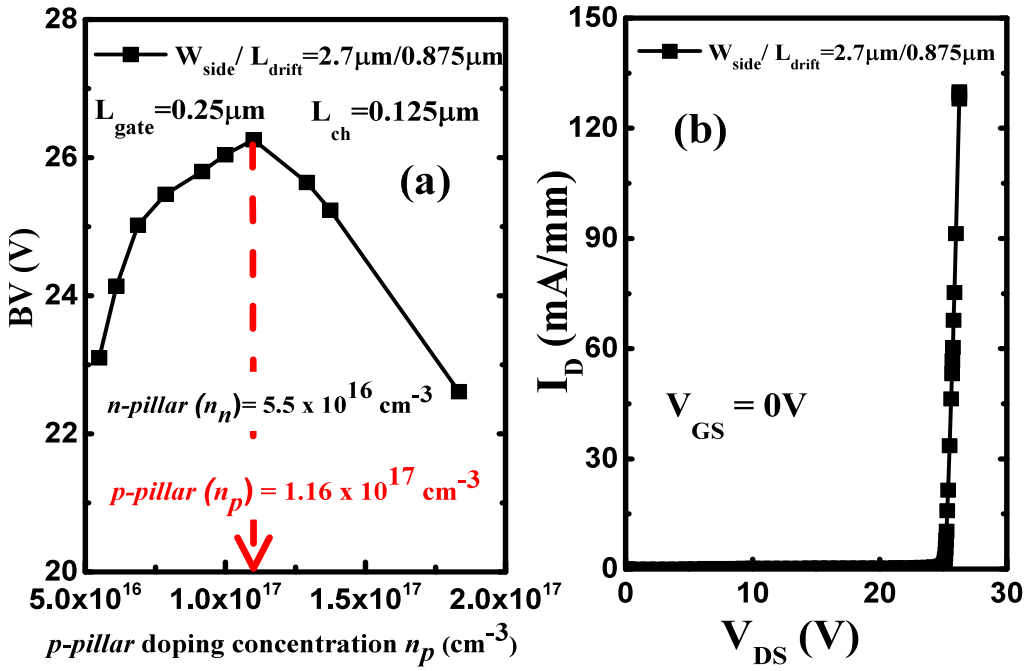


Figure 7: (a) A relationship between the BV and the p-pillar doping concentration during charge imbalance in the SJ unit when the device is scaled down to 0.25 μm L_{gate} with $W_{\text{side}} = 2.7\ \mu m$, $L_{\text{drift}} = 0.875\ \mu m$ and $W_n = W_p = 0.3\ \mu m$ during the off-state. (b) The BV during the off-state under a charge balance for the optimised SJ-MGFET scaled down to $L_{\text{gate}} = 0.25\ \mu m$, and $L_{\text{ch}} = 0.125\ \mu m$.

a critical value, E_C, of approximately $5.5{\times}10^5\ V/cm$. We have observed that surface electric field in the drift region (defined by the end of the channel and the beginning of the n-type drain doping) in each structure is relatively uniform and increases as the length of the drift region decreases. This implies that for an higher BV, more space is required for the electric field to be deployed.

A gate capacitance (C_{G}) as a function of the gate bias for the three scaled device structures is shown in Fig. 9. During the on-state, with the gate reverse biased, the *p-body* situated closer to the gate is switched on to accumulation mode which is the most pronounced in a structure with the thinnest gate oxide while at the same time maintains the n-pillar in inversion mode. When the gate is forward biased, the *p-body* area changes to inversion mode and the n-pillar switches to accumulation mode. We observe that the

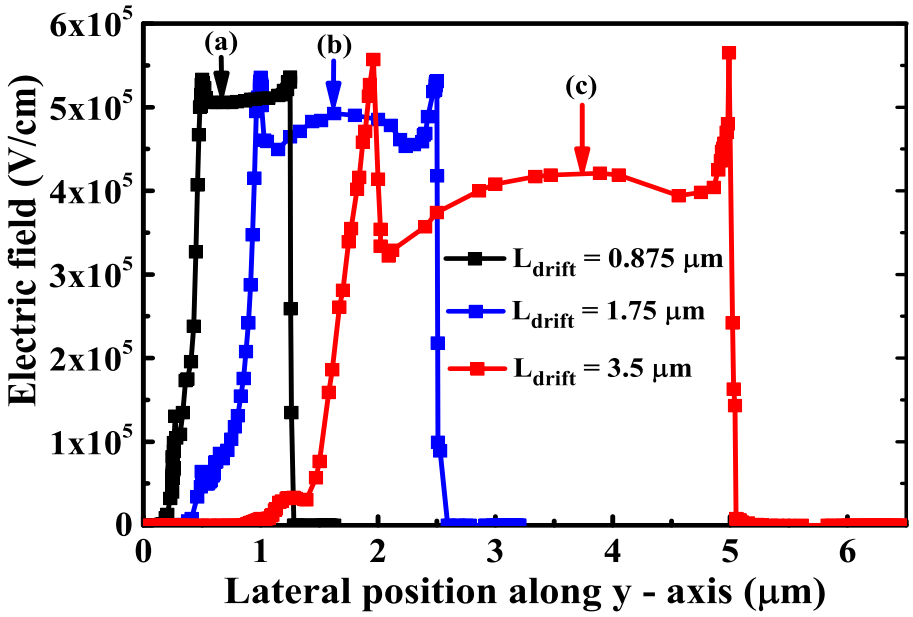


Figure 8: Lateral electric field distribution at the surface of the drift region along the $C-C'$ cutline defined along the junction between the n– and the p–pillars in Fig. 1 during the off-state under the charge balance condition (a) in the SJ-MGFET with $L_{\rm ch} = 0.125$ μm, $L_{\rm gate} = 0.25$ μm, and $L_{\rm drift} = 0.875$ μm at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 26$ V, (b) in the SJ-MGFET with $L_{\rm ch} = 0.25$ μm, $L_{\rm gate} = 0.5$ μm and $L_{\rm drift} = 1.75$ μm at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 48$ V, and (c) in the SJ-MGFET with $L_{\rm ch} = 0.5$ μm, $L_{\rm gate} = 1.0$ μm, and $L_{\rm drift} = 3.5$ μm at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 65$ V.

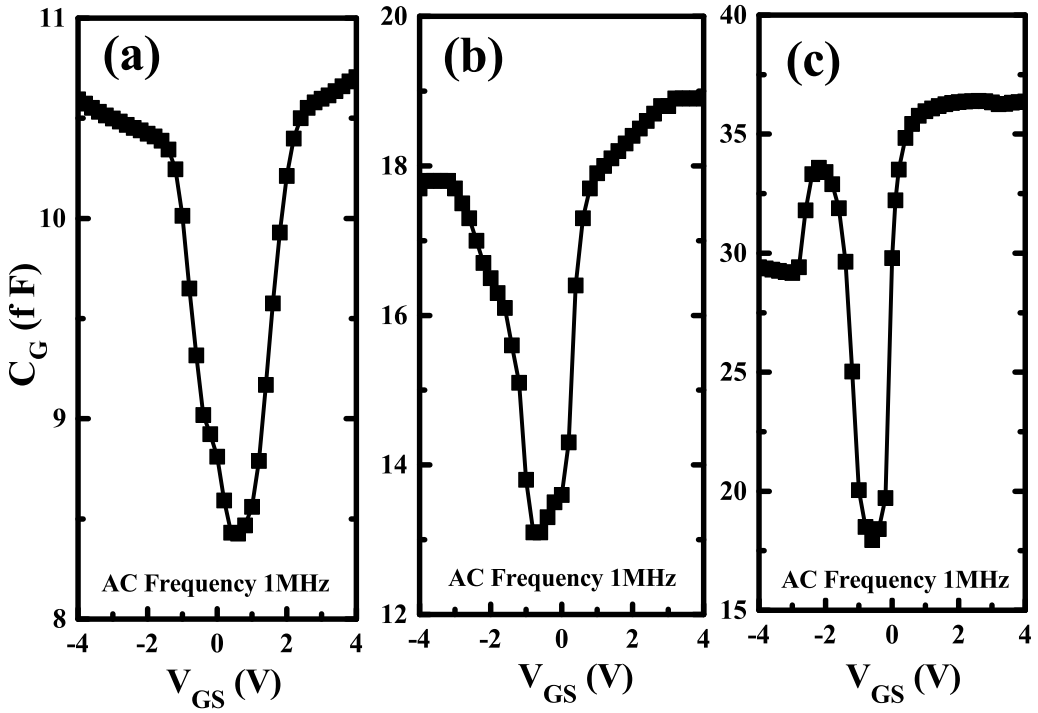


Figure 9: Gate capacitance plotted as a function of gate-source voltage $V_{\rm GS}$, at a small signal AC analysis of 1 MHz for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

0.25 μm gate length SJ-MGFET has the most elongated penetration of the drain-to-channel depletion layer under the gate because of the shortest $L_{\rm ch}$ and the thinnest t_{ox}. An overall $C_{\rm G}$ of approximately 0.01 pF, 0.02 pF, and 0.04 pF is achieved in conformity with the scaling ratio of 1 : 0.5 : 0.25, respectively. Fig. 10 depicts the dependence of output ($C_{\rm oss}$) and reverse transfer ($C_{\rm rs}$) capacitances on the drain voltage ($V_{\rm DS}$) by performing three-dimensional numerical simulations with an $A.C$ signal at 1 MHz. A non-linearity of the output and the reverse transfer capacitances ($C_{\rm oss}$ and $C_{\rm rs}$) can be seen as a result of their strong dependence on the depletion width, in which the drain voltage plays a dominant factor. We observe that, as the drain voltage increases in the three device structures, the gate-drain capacitance ($C_{\rm gd}$) plays a major role in a total effect of $C_{\rm oss}$ in the devices.

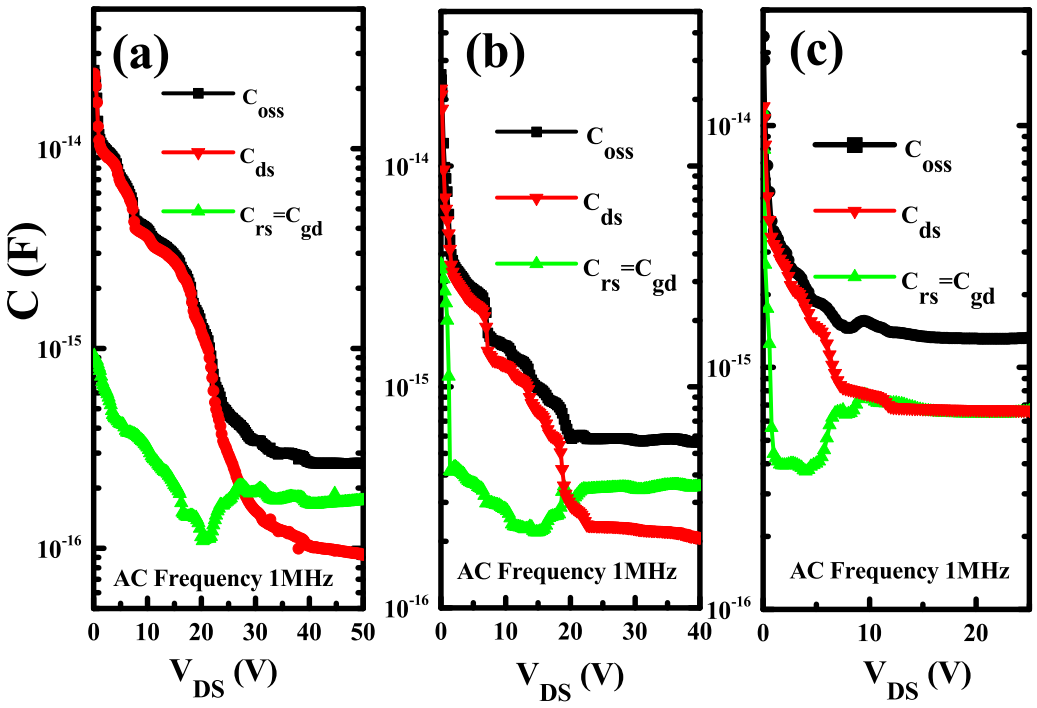


Figure 10: The dependence of $C_{\rm oss}$, $C_{\rm rss}$ and $C_{\rm ds}$ on $V_{\rm DS}$ at a small signal $A.C$ analysis of 1 MHz for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

Fig. 11 shows the dependence of transconductance (g_m) on the gate voltage in the three scaled device structures at $V_{\rm DS} = 0.1\ V$. The g_m per device width increases with shorter $L_{\rm ch}$ and thinner t_{ox}. The following maximum transconductances for three scales SJ-MGFETs have been extracted at $V_{\rm DS} = 0.1\ V$: (a) g_m of 5 mS/mm for the device with $L_{\rm ch} = 0.5\ \mu m$, $L_{\rm gate} = 1.0\ \mu m$ and $t_{ox} = 35\ nm$, (b) g_m of 20 mS/mm for the device with $L_{\rm ch} = 0.25\ \mu m$, $L_{\rm gate} = 0.5\ \mu m$ and $t_{ox} = 18\ nm$; and (c) g_m of 56 mS/mm for the device with $L_{\rm ch} = 0.125\ \mu m$, $L_{\rm gate} = 0.25\ \mu m$ and $t_{ox} = 9\ nm$. The SJ-MGFET scaled down to $L_{\rm gate} = 0.25\ \mu m$ with the thinnest t_{ox} shows the highest transconductance resulting in a larger RF gain having an intrinsic voltage gain (A_v) of 0.16 extracted at $V_{\rm GS} = 4.5\ V$ and $V_{\rm DS} = 0.1\ V$ [29, 30].

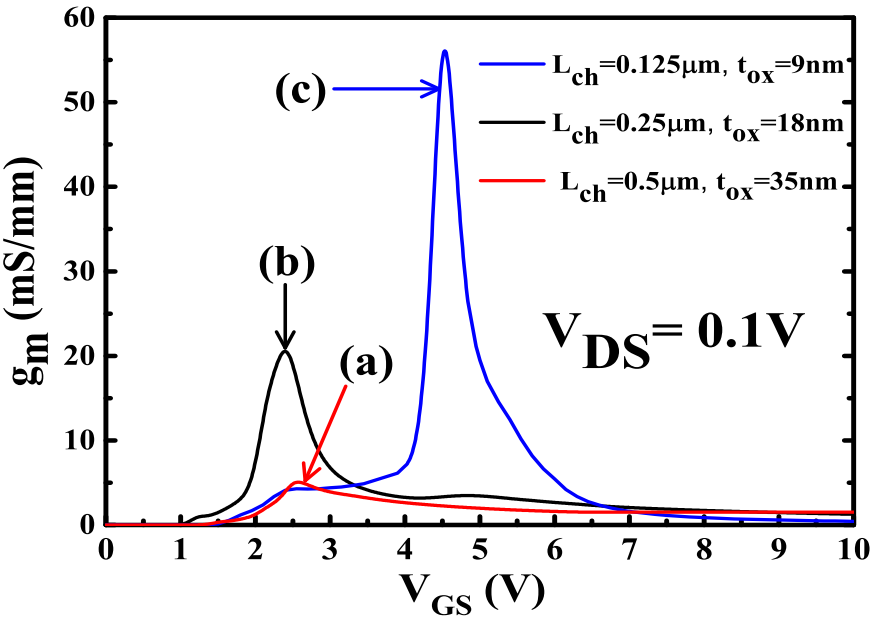


Figure 11: Transconductance of the three device structures for (a) the 1.0 μm gate length SJ-MGFET having a channel length of 0.5 μm and a drift region length of 3.5 μm, (b) the 0.5 μm gate length SJ-MGFET having a channel length of 0.25 μm and a drift region length of 1.75 μm, and (c) the 0.25 μm gate length SJ-MGFET having a channel length of 0.125 μm and a drift region length of 0.875 μm.

The cut-off frequency (f_T) [31, 32] can be obtained as 6:

$$f_T = \frac{g_m}{2 \cdot \pi \cdot (C_{\text{gs}} + C_{\text{gd}})} \tag{6}$$

The maximum operating frequency achieved at $V_{\text{DS}} = 0.1\ V$ are 0.2 GHz for the device with $L_{\text{gate}} = 1.0\ \mu m$, 0.6 GHz for the device with $L_{\text{gate}} = 0.5\ \mu m$, and 0.9 GHz for the device with $L_{\text{gate}} = 0.25\ \mu m$, respectively.

Fig. 12 shows a comparison of performance of the three scaled transistors during gate turn-on transient simulations when the devices are ramped to $V_{\text{DS}} = 10.0\ V$ at $V_{\text{GS}} = 10.0\ V$, neglecting a circuit resistance R_c and a stray inductance L_s. A capacitance of 0.5pF is specified to emulate the gate drain interconnect and an external resistor of $1k\Omega$ to simulate a load resistance between the drain and the drive. Hence, SJ-MGFETs with L_{gate} of 0.5 μm and 0.25 μm offer a switching turn-off time (t_{off}) of approximately 0.2 ns and 0.05 ns, respectively, compared with the 1 ns (t_{off}) in the SJ-MGFET with 1 μm gate length.

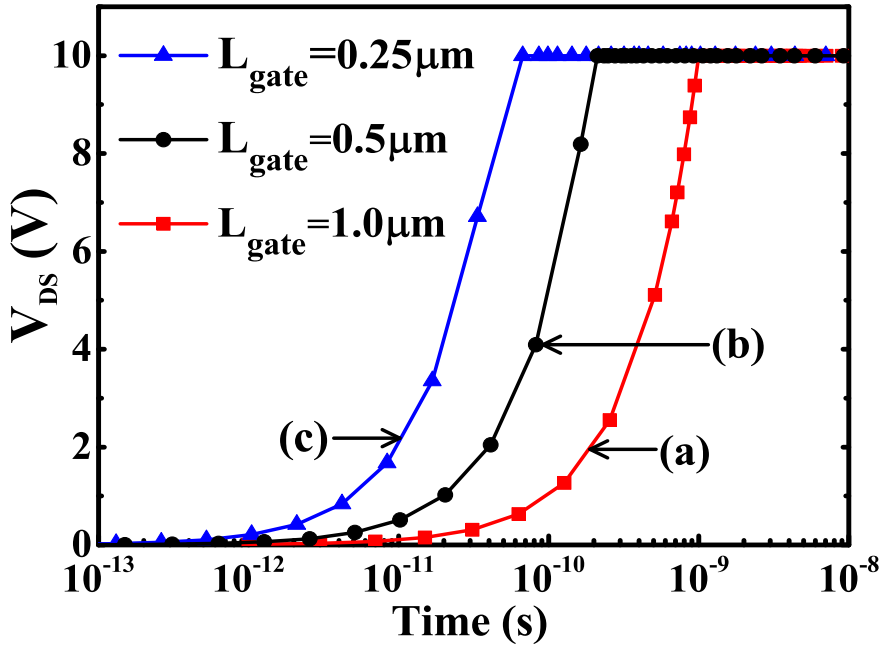


Figure 12: Switching waveforms from the gate turn-on transient simulations with a device ramped to $V_{\rm DS} = 10\ V$ and $V_{\rm DS} = 10\ V$ for (a) the device with $L_{\rm ch} = 0.5\ \mu m$, and $L_{\rm gate} = 1.0\ \mu m$; (b) the device with $L_{\rm ch} = 0.25\ \mu m$, and $L_{\rm gate} = 0.5\ \mu m$; and (c) the device with $L_{\rm ch} = 0.125\ \mu m$, and $L_{\rm gate} = 0.25\ \mu m$.

The trade-off between BV and $R_{on,sp}$ for the simulated SJ-MGFETs scaled down to 0.5 μm and 0.25 μm gate lengths are compared with the ideal silicon limit and with various conventional LD-MOSFETs in Fig. 13. The simulations show that the SJ-MGFET with 0.25 μm gate length achieves a low $R_{on,sp}$ ($V_{\rm GS} = 10\ V$) of 2.24 $m\Omega.mm^2$ and $BV = 26\ V$ with $L_{\rm drift} = 0.875\ \mu m$ and the SJ-MGFET with 0.5 μm gate length offers a $R_{on,sp}$ ($V_{\rm GS} = 10\ V$) of 7.68 $m\Omega.mm^2$ and $BV = 48\ V$ with $L_{\rm drift} = 1.75\ \mu m$, respectively. The SJ-MGFET scaled to the 0.5 μm gate length leads to 16% reduction in $R_{on,sp}$ compared to superjunction UMOSFET (SJ-UMOSFET) at the same BV rating [33], 73% reduction compared to Floating RESURF (FRESURF) at the same BV rating [34], 78% reduction compared to dual RESURF LDMOS at the same BV rating [35], and 85% reduction compared to isolated low NLDMOS at the same BV rating [36]. The SJ-MGFET scaled to the 0.25 μm gate length has $R_{on,sp}$ lower by 90% compared to isolated low NLDMOS [36] at the same breakdown voltage rating.

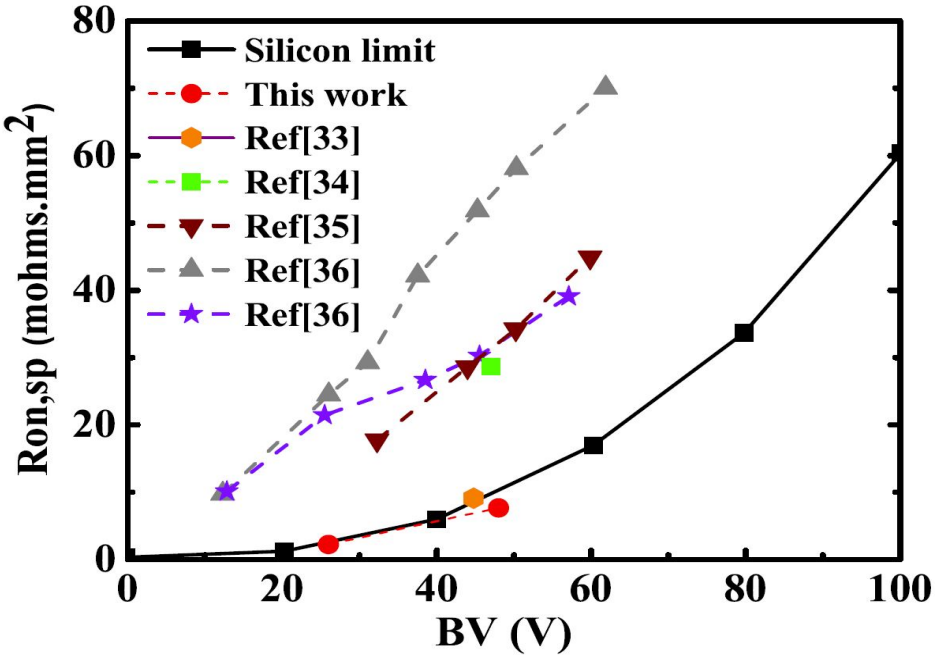


Figure 13: Specific on-resistance as a function of the breakdown voltage of the scaled down SJ-MGFET compare with the reported conventional LDMOSFETs and SJ-LDMOSFETs [33, 34, 35, 36] devices.

The SJ-MGFET scaled to 0.5 μm gate length offers superior performance in term of high drive current, switching speed, BV and $R_{on,sp}$ compared with the 1 μm gate length SJ-MGFET. The combination of these fourfold benefits with the reduction in device dimensions suggests a better architecture design in achieving a larger number of transistors per chip and a higher integration. Although, the SJ-MGFET scaled to the 0.25 μm gate length achieves the largest device dimension reduction with a vastly superior drive current and improved transconductance. However, the extreme scaling of the gate oxide thickness and decrease in the channel length limits the device voltage-sustaining capability. In addition, a fabrication of the aligned deep trenched gate structure with a small channel length within the non-planar SOI power technology is challenging, costly and technologically limited.

5. Conclusions

The scaling of non-planar SJ-MGFETs following conventional scaling rules [37, 38] requires a subsequent optimisation of their SJ unit. The lateral scaling and optimisation of the 1 μm gate length SJ-MGFET to gate lengths of 0.5 μm and 0.25 μm using Silvaco TCAD simulations has shown that the FoM of this non-planar transistor can be substantially improved including physical density, switching speed, drive current, breakdown voltage and specific on-resistance ($R_{on,sp}$). The scaling and optimisation of the overall device design have achieved a low specific on-resistance of 7.68 $m\Omega.mm^2$ and 2.24 $m\Omega.mm^2$ ($V_{\mathrm{GS}} = 10\ V$), and breakdown voltages of 48 V and 26 V for the 0.5 μm and 0.25 μm gate length SJ-MGFETs, respectively. Our investigations have also shown that excessive channel doping in the scaled SJ-MGFETs offers no significant improvement in the device avalanche capability during charge balanced condition. With the twofold benefits of device dimension reduction and optimised fully-depleted SJ multi-gate architecture, the transistor can offer a superior performance in achieving a higher levels of integration, a maximum breakdown voltage, a minimum specific on-resistance, and excellent FoM in sub-50 V applications.

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