

# Shuttling-Based Trapped-Ion Quantum Information Processing

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Moving trapped-ion qubits in a microstructured array of radiofrequency traps offers a route towards realizing scalable quantum processing nodes. Establishing such nodes, providing sufficient functionality to represent a building block for emerging quantum technologies, e.g. a quantum computer or quantum repeater, remains a formidable technological challenge. In this review, we present a holistic view on such an architecture, including the relevant components, their characterization and their impact on the overall system performance. We present a hardware architecture based on a uniform linear segmented multilayer trap, controlled by a custom-made fast multi-channel arbitrary waveform generator. The latter allows for conducting a set of different ion shuttling operations at sufficient speed and quality. We describe the relevant parameters and performance specifications for microstructured ion traps, waveform generators and additional circuitry, along with suitable measurement schemes to verify the system performance. Furthermore, a set of different basic shuttling operations for dynamic qubit register reconfiguration is described and characterized in detail.

## I. INTRODUCTION

The potentially disruptive applications of quantum information processing have stimulated an intensive effort towards realizing fault-tolerant large-scale quantum computers during the last two decades. Originally developed in academic research institutions, there is nowadays a variety of small-scale quantum processors that have served for proof-of-principle demonstrations<sup>[1]</sup>. In the last decade, we have witnessed an impressive progress in the performance of such small-scale quantum processing nodes. Currently, research efforts are partially shifting to world-leading technology companies. The most promising platforms are currently superconducting circuits and trapped atomic ions<sup>[2]</sup>. In this work, we focus on trapped-ion quantum computing (QC) platforms, which have been of paramount importance in the first demonstrations of some of the quantum algorithms that can potentially harness the power of quantum computers<sup>[3,5]</sup>.

Progress in trap technology allows for long and stable storage of long ion strings, and improved laser addressing optics allow for conducting gate operations across the entire register<sup>[4]</sup>. Fast entangling gates<sup>[6]</sup> allow for suppressing undesired couplings<sup>[7,8]</sup>, which opens up prospects for a scalable architecture based on multiple static ion registers<sup>[9]</sup>. The crucial remaining question is how to scale these devices towards large-scale quantum processors that can actually overcome the performance of their classical counterparts. Although noisy intermediate-scale quantum (NISQ) computing devices have reached a maturity allowing for proof-of-principle demonstration of quantum supremacy<sup>[10,12]</sup>, commercially

useful applications will still require substantial research and engineering efforts. In particular, the inherent fragility of quantum states ultimately requires the incorporation of quantum error correction (QEC)<sup>[13]</sup>, where trapped-ion platforms have also been used to demonstrate various methodological building blocks<sup>[21,4,15]</sup>. However, scaling such platforms to register sizes and circuit depths allowing for scientific or commercial applications remains a formidable challenge.

Trapped ion QC platforms face two major challenges when attempting to scale to a large number of qubits. On the one hand, the quantum information processing requires a very well controlled and extremely low-noise environment. This leads to the requirement of shielding and filtering, while sufficient access for control is to be maintained. Furthermore, scaling qubit registers is demanding as the number of required 'control lines', e.g. electrical wires, laser beams or microwave fields, scales unfavorably as compared to classical information processing devices.

For current trapped-ion based QC realizations, the qubit register is given by a linear Coulomb crystal of atomic ions confined in an ellipsoidal ponderomotive radio-frequency (rf) potential<sup>[16,17]</sup>. With typical ion spacings in the few-micrometer range, the ions can be individually addressed with tightly focused laser beams<sup>[18]</sup>, which allows for driving single- or multi-qubit gate operations on specific subsets of qubits. Multi-qubit entangling gates are the most demanding operations, which can be generated via radiation-induced coupling between the qubit states (internal electronic states of the atomic ions) and the collective vibrational motion of the Coulomb crystal<sup>[19]</sup>. Impressive results have been achieved using linear qubit registers, including entanglement of 14-qubits<sup>[20]</sup>, 20-qubit quantum simulations<sup>[21]</sup>, multi-species entanglement<sup>[22]</sup>, remote entanglement of ions in two setups<sup>[23]</sup>,

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demonstration of Groovers algorithm<sup>[24]</sup> and an 11-qubit trapped ion quantum computer<sup>[25]</sup>.

When increasing the number of ions in a linear Coulomb crystal, several challenges arise: Smaller inter-ion distances deteriorate laser addressing capabilities, an increasing number of motional modes leads to spectral crowding thwarting gate interactions, the ion crystal approaches the zig-zag structural instability<sup>[26]</sup>, and the overall difficulty of maintaining a large crystal stable in the presence of background gas collisions and electric noise increases.

These complications call for exploring alternative strategies to scale the trapped-ion quantum processor. To reach further scalability, the NIST group has proposed the *Quantum CCD* as a tentative solution for a scalable trapped-ion QC architecture<sup>[27]</sup>. Here, a *segmented* ion trap consists of an array of individually controllable electrodes. This allows for repositioning, commonly known as shuttling, of individual ions or small ion crystals between different regions of the trap, which can be processing zones allowing for qubit operations or mere storage regions. The degree of qubit connectivity can thus be adapted and optimized according to the requirements of the quantum algorithm to be executed. A recent theoretical analysis also shows that a quasi-1D qubit register topology with medium-range couplings, can be used to realize fault-tolerant operation at modest error-correction thresholds<sup>[28]</sup>. Such a quasi-1D register requires extensive use of shuttling operations.

Even with segmented traps, the achievable register sizes are subject to technological constraints. A possible route to further scalability is given by photonic interconnects, where light is used to transfer quantum information between different quantum processing nodes<sup>[29,35]</sup>. Establishing such interconnects based on free-space or cavity-enhanced coupling is currently subject to intensive research efforts. Note that other schemes to scale trapped-ion QC architectures are currently under investigation. In particular, a complete blueprint for a shuttling-based two-dimensional array of surface electrodes traps has been proposed<sup>[36]</sup>, which is based on laser-less gates<sup>[37,39]</sup>. The basic functionality has already been demonstrated on a static three-ion crystal<sup>[40]</sup>.

In this work, we present a thorough description of a promising scaling strategy that can be considered a natural evolution of the static string-based approach, by exploiting shuttling and combining the 1D quantum CCD approach with optical interconnects for scaling. This scheme can alleviate the discussed limitations and problems of large static ion strings at the cost of increased technical complexity and overhead given by shuttling operations. We focus on a single trapped-ion quantum processing node, and provide a complete and detailed description of the technological developments that are required to realize a shuttling-based quantum information processing toolbox, which offers basic scalable functionality. We will partially review recent advances in the field of trapped ion quantum computing and

provide references to seminal and recent work. Furthermore, our work contains a variety of recent and unpublished material serving as a summary of the current state-of-the-art concerning shuttling-based scalability and represents a road-map of technological advances required to further pursue this approach to scalable quantum information processing.

We start with a brief review of scalable trapped ion architectures with a focus on our approach in Sec. II and then describe the fabrication steps and properties of our linear segmented multilayer trap in Sec. III, our custom-made multi-channel arbitrary waveform generator in Sec. IV and the electrical wiring in Sec. V. The resulting system performance is presented in Sec. VI. We then outline the methodology for conducting different types of shuttling operations in Sec. VII. Finally, in Sec. VIII, we give a conclusion and brief discussion on future improvements, enhancements and developments towards a scalable trapped-ion quantum processing node.

## II. ARCHITECTURE

All presented trapped-ion quantum computing architectures are based on radiofrequency (Paul) traps. Two variations of such traps are commonly employed<sup>[41]</sup>, one known as surface electrodes traps<sup>[42,43]</sup>, where all rf and dc electrodes are arranged in one plane below the trapping center, and a second configuration known as symmetric or sandwich traps, which has at least two planes with electrodes placed symmetrically above and below the trapping zone<sup>[44,45]</sup>.

Architectures that allow scaling to large numbers of qubits without relying on optical interconnects make use of large electrode arrays connected using junctions<sup>[27,36]</sup> and naturally favor surface trap designs. Proposals making use of optical interconnects<sup>[31]</sup> rely on smaller trap arrays and a smaller number of ions stored in each trap. Here, large arrays or junction designs are not ultimately required and therefore symmetric traps are favored due to superior ion confinement and easier trap operation.

The centerpiece of the architecture presented in this work is a symmetric two-layer segmented rf trap. The trap features two metalized electrode layers, each layer forming a linear array of uniformly sized dc electrodes arranged along the trap slit on one side and a single rf electrode placed on the other side. Each dc electrode can be individually supplied with computer-controlled arbitrary voltage waveforms. The direction along the trap slit is termed *trap axis*, and the directions perpendicular to it are the *transverse directions*. Two electrode layers, with the sides of dc and rf electrodes reversed, are placed symmetrically around the trap axis, one above and one below. An example of such a trap is shown in Fig. I. In this design the confinement along the trap axis is of electrostatic nature, and can be controlled via the applied segment voltages. Application of a negative voltage to a given segment leads to an electrostatic potential well extending along the trap axis over the width of one segment, and a depth and potential curvature controlled by the voltage. The confinement along the transverse directions is of ponderomotive nature, and the

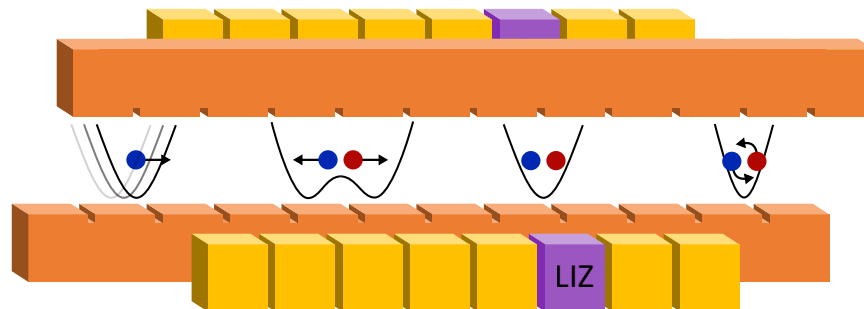


FIG. 1. 1D QCCD architecture: Trapped-ion qubits are arranged along the RF null axis of a uniformly segmented linear Paul trap. The lasers performing qubit operations are directed to a fixed segment, the laser interaction zone (LIZ). The qubits are kept in small groups of two to four ions, and rearranged via shuttling operations, which are carried out by changing the voltages applied to the trap electrodes. The rearrangement operations fall into different categories, from left to right: Linear transport, separation and merging and swapping via crystal rotation.

axial confinement leads to weakening along at least one transverse direction, according to Laplace’s law.

Typical operation parameters are rf trap drive frequencies on the order of  $2\pi \cdot 35$  MHz, rf voltages of about 200 V amplitude and dc trapping voltages around  $-6$  V. Such parameters lead to axial secular frequencies of  $2\pi \cdot 1.5$  MHz and transverse secular frequencies between  $2\pi \cdot 3.5$  MHz and  $2\pi \cdot 4.5$  MHz. These confinement parameters allow for stable linear ion strings of up to four ions to be stored in one segment potential. In total, we may operate on registers comprised of up to 20 ions.

Qubit register reconfigurations (i.e. shuttling operations) are carried out via temporal changes of the dc voltages, such that potential wells move along the trap axis. The fundamental challenge lies in realizing *fast* operation times, in order to stay significantly below the decoherence timescales, and to keep the overhead as low as possible. Generally, shuttling operations do not have detrimental effects on qubit coherence, as recently shown by the Siegen group<sup>[46]</sup>. However, *motional excitation* resulting from the shuttling operations is to be avoided, as it can deteriorate the fidelity of entangling gates or qubit readout operations. This directly implies a fundamental technological trade-off: On the one hand, fast operations require a large frequency bandwidth for the electrical waveforms to be applied to the dc electrodes, on the other hand, filtering of the dc lines is required to suppress technical noise. As a rule of thumb, we found that filtering at cut-off frequencies of 5-20% of the lowest secular frequency to lead to suitable operating conditions.

In order to realize computational sequences with interleaved entangling gate and shuttling reconfiguration, we conduct the entangling gates such that they are mediated by and therefore only sensitive to the transverse motion of the ions. As the register reconfiguration operations predominantly lead to residual excitation along the axial direction,

this scheme imposes much less stringent requirements on the reconfiguration operations. Note, that in actual experiments, we perform several hundreds of shuttling operations without the need for recoiling the qubit register. Therefore, fast shuttling and bearable calibration effort can be successfully combined with entangling gate operations at fidelities in the  $>99\%$  regime.

All laser beams for conducting the various operations on the qubits are directed to a fixed segment, which is termed *laser interaction zone* LIZ in the following. The computational sequences therefore consist of repeatedly regrouping the ions in a way such that gate operations or readout on a desired subset of the qubits can be carried out in the LIZ. We have demonstrated the basic functionality of the architecture by performing quantum-enhanced magnetic field sensing with separated, but entangled ions<sup>[47]</sup> and by generating a high-fidelity four-partite GHZ state<sup>[5]</sup>. So far, we have been working with two-ion crystals as the largest operational building block, however the extension to larger subsets is possible. Calculations indicate that the performance of a quasi-1D qubit register strongly increases with the maximum size of the subsets<sup>[28]</sup>.

The qubit type of our choice is the  $^{40}\text{Ca}^+$  spin qubit<sup>[48]</sup>, where the quantum information is stored in the spin of the valence electron, i.e. the  $|S_{1/2}, m_J = +\frac{1}{2}\rangle$  and  $|S_{1/2}, m_J = -\frac{1}{2}\rangle$  sublevels of the electronic groundstate, which are split in energy by about  $2\pi \times 10$  MHz by an external magnetic field. Our architecture is compatible with all trapped-ion qubit realizations, therefore this work does not elaborate on qubit-specific operations and restrictions. For more detail, the reader is referred to references<sup>[49][50]</sup>.

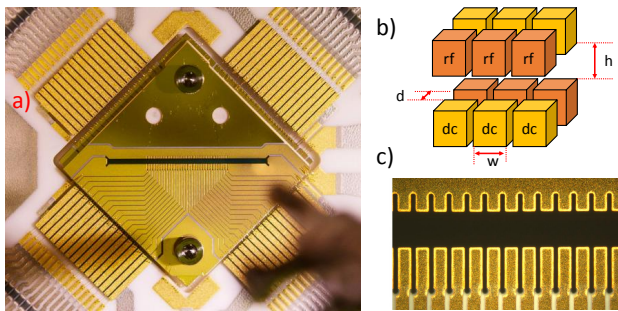


FIG. 2. **a)** Close-up photograph of the trap after assembly and wire-bonding. **b)** Sketch of the trap geometry, showing the relevant dimensions  $w = 150\ \mu\text{m}$ ,  $d = 254\ \mu\text{m}$  and  $h = 400\ \mu\text{m}$ . Note that these dimensions are reduced due to the electroplating of an  $8\ \mu\text{m}$  thick gold layer. The width of the isolation gaps between the dc electrodes is  $50\ \mu\text{m}$  before and on the order of  $34\ \mu\text{m}$  after plating. **c)** Microscope image of the trapping region. The exposed alumina between the electrodes serves as electrical isolation.

### III. SEGMENTED MICROTRAP FABRICATION

Ion traps can be manufactured using a variety of techniques, each having certain advantages depending on the dedicated purpose. For the storage of static linear strings of ions, large machined metal parts assembled to create a symmetric electrode configuration<sup>[51]</sup> still represent the most popular trap design. These traps are relatively easy to fabricate and operate. Shuttling ions in trap arrays requires a larger number of smaller electrode structures, leading to microfabrication techniques being a more suitable choice.

Microfabricated ion traps can incorporate many trap features, including microwave lines close to the ion<sup>[38,52]</sup>, magnetic field gradient generating structures<sup>[53,54]</sup>, micro-mirrors as part of the electrode surface<sup>[55]</sup>, on-chip detection<sup>[56]</sup>, complex electrode structures such as junctions<sup>[43]</sup>, and other useful features<sup>[57,58]</sup>. Fabrication techniques for such traps range from CMOS (Complementary Metal-Oxide-Semiconductor) compatible methods<sup>[59]</sup> to standard MEMS (Micro-Electro-Mechanical Systems) microfabrication techniques<sup>[41,43,60,62]</sup>.

Micromachined symmetric traps, consisting of laser-machined and metal-coated alumina wafers, are designed and fabricated to accommodate many dc electrodes<sup>[45,63,64]</sup>, while some advantages of macroscopic linear rf traps retained, i.e. deep and symmetric ion confinement. Micromachined symmetric traps can be fabricated with minimal use of cleanroom fabrication techniques. The machining can be realized by employing commercially available laser cutting services, and near-perfect shielding of dielectrics can be achieved.

For the experiments presented in this work a linear micro-machined symmetric trap with 64 dc electrodes was used, which is depicted in Fig. 2(a). The trap is made up of two electrode layers, which are stacked together using an additional spacer layer. The electrode configuration is shown in Fig. 2(b).

Fabrication of the electrode layers starts with polished alumina (Coors ADS996-polished /  $\text{Al}_2\text{O}_3$  99,6%) as base ma-

terial to achieve a low surface roughness. Individual parts are laser-cut from 2 inch alumina wafers forming the electrodes, trap slit and mounting holes. Cutting is performed using a high-power femto-second laser (Mitreon GmbH, Hannover), which ablates material and provides clean cuts, allowing for structures down to the  $10\ \mu\text{m}$  scale. After cutting, the wafers are cleaned using the following procedures: i) Ultrasonic cleaning in isopropyl alcohol at  $40^\circ\text{C}$  for 20 minutes, ii) rinsing with distilled water, iii) submerging in piranha solution, 98%  $\text{H}_2\text{SO}_4$  to one part  $\text{H}_2\text{O}_2$  (30% dilution), at room temperature for 10 minutes, to remove organic and other reactive materials, iv) rinsing with distilled water followed by isopropyl alcohol and v) drying in air for 1 hour.

Next, the chips are coated with a titanium adhesion layer of 50 nm, followed by a 500 nm layer of gold using an e-beam evaporator (Universität Ulm, Institut für Optoelektronik) creating an oxide free and conducting surface for subsequent electroplating. To ensure homogeneous coating of all electrodes, the wafers are rotated during the coating process and the wafer normal is tilted by  $20^\circ$  with respect to the direction of incidence of the atomic beam.

In a subsequent laser cutting step at lower optical power, gold is removed from the alumina surface to create the electrode structures. In this step only the metals are ablated, while the alumina surface is retained. To ensure that no shorts appear at the intersection of electrode fingers and unstructured alumina, shown in Fig. 2(c) an additional laser ablation step drills a hole at this intersection point, removing any metals deposited due to the angled evaporation and also alumina. At the top and left side of the trap, the electrodes remain fully connected along two edges of the trap, which is required for the following step.

Our trap design and fabrication process is inspired by similar traps operated by the NIST group and the ETH Zürich group, where thick gold layers have been deposited via electroplating, and low heating rates were observed at room temperature. Thick electrode layers are desirable as the shielding of the trapped ions from the dielectric wafers is improved, and the ohmic resistance of the dc and more importantly rf electrodes is reduced. Furthermore, the electroplated gold layer might exhibit more beneficial surface characteristics as compared to an evaporated layer. However, the dependence of heating rates on the trap surface characteristics is not yet fully understood. For instance, heating rates of below 10 quanta/s at secular frequencies in the 1 MHz range have also been observed in a trap with an evaporated surface of about  $1\ \mu\text{m}$  thickness by the Berkeley group<sup>[65]</sup>.

To achieve a thick gold layer covering the electrodes, the structured - but still connected - metal layers are gold electroplated to a thickness of about  $8\ \mu\text{m}$ . The electroplating procedure is similar to the one established by the NIST group<sup>[66]</sup>. The solution used for the gold deposition is a sulphite-based gold bath Gold-SF (Metakem GmbH). Before the electroplating, the chips are cleaned in an ultrasonic bath of isopropyl alcohol (purity grade 99.8%) at  $40^\circ\text{C}$  for 15 minutes. We observed that if the chips are not cleaned within a few days after the last laser machining step, gold is more likely to be deposited on the electrically isolated parts during electroplating.



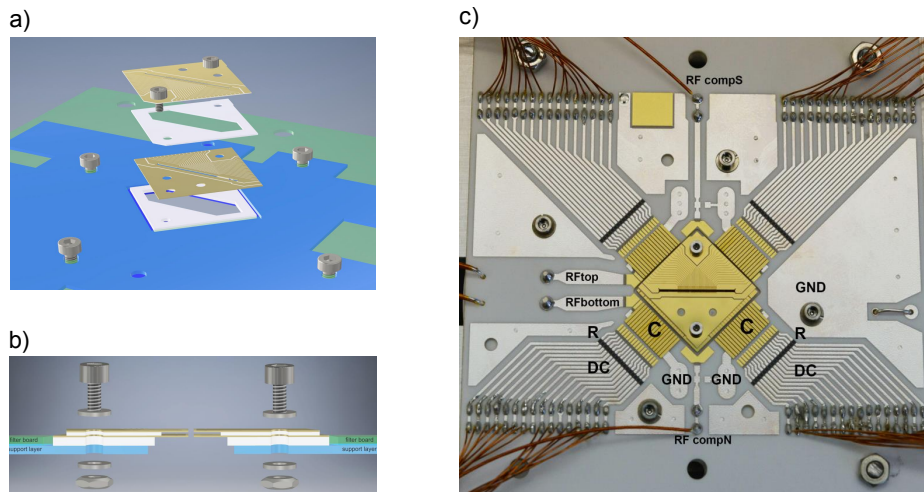


FIG. 3. Trap assembly. **a)** and **b)** depict the assembly of the trap stack. The transparent green structure is the filter board, below which the support layer (blue) is mounted. Onto the latter, the following elements are mounted from bottom to top: Bottom spacer, metalized trap bottom layer, central spacer, metalized trap top layer. The stack is held together with M1 titanium screws. **(c)** shows a photograph of the complete electrical assembly. The outer dimensions of the board are 79.9 mm x 78.3 mm. Each trap dc electrodes is connected to a single layer capacitor *C* using wirebonds. Another set of wirebonds makes contact to printed metallized tracks followed by printed resistors *R*. Connections between the end of the tracks and vacuum feedthrough is made by soldering on Kapton insulated wires with a crimped on D-Sub connector. The rf electrodes of the trap top and bottom layers are wired individually with cables of the the same length.

This is likely caused by small particles of gold which are released during the laser ablation process and can then redeposit on gold-free areas if not cleaned in time. We also found that this problem can be avoided by submerging the traps in diluted iodine for a few seconds to dissolve these undesired gold particles without removing significant amounts of gold from the electrodes. After the electroplating, the trap chips are cleaned in distilled ionized water, isopropyl alcohol and acetone and inspected under a microscope.

In the last step, chips are cut out using a saw blade to remove the electrical connections between electrodes, which were required during the plating process. Cutting these shorts was achieved using a 200  $\mu\text{m}$  diameter diamond wire saw (Model 3500, Diamond WireTec GmbH). To perform the cutting process chips have to be glued onto the surface of a plastic mount using acetone soluble wax (Crystalbond, Type 509). It is important that the trap surfaces are fully covered with the wax during cutting to prevent the wire saw from dragging gold across isolating parts of the alumina wafer which could otherwise electrically shorten the electrodes. Finally, the trap chips are removed from the plastic slab by dissolving the wax in acetone and then cleaned in an ultrasonic bath with distilled water followed by isopropyl alcohol.

After completing the individual trap chips, the symmetric ion trap is assembled using two trap chips and a mechanical spacer made of alumina. Traps chips and spacers are placed on a ceramic trap mount and aligned making use of an optical microscope, and fixated using two titanium M1 screws, as can be seen in Fig. 3. This procedure achieves an alignment accuracy between the top and bottom trap chip of up to 10  $\mu\text{m}$ <sup>67</sup>. Besides holding the trap in place and providing mounting structures to fixate the assembly inside a vacuum

system, the ceramic mount is also used to establish electrical connections and provide low-pass filters.

The trap mount is made of a polished alumina plate and has electrical tracks and resistors printed on it using conductive paste (made by Technische Universität Dresden, Fakultät Elektrotechnik und Informationstechnik), which is afterwards sintered, shown in Fig. 3(c). To provide a low rf impedance path to ground for the dc electrodes and to create a simple low-pass rc filter, single layer ceramic capacitor arrays (Complex row capacitor, CR/CM series: CR16-200-344.2X178X10-3-G-202-Z) marked with C in Fig. 3(c) are soldered onto the printed metal tracks. Both the top of the capacitor arrays and the electrical tracks of the trap chips are connected using wirebonds. Kapton insulated ultra-high vacuum compatible wires are soldered onto the end of the tracks on the trap mount and are connected to voltage waveform generators outside the vacuum apparatus, which will be described in the following chapters.

#### IV. FAST MULTI-CHANNEL ARBITRARY WAVEFORM GENERATOR

Shuttling-based trapped-ion quantum processing requires freely programmable time-dependent voltage waveforms supplied to the individual trap electrodes. Therefore, a required key technological component is a fast multi-channel arbitrary waveform generator (mAWG), operating in real time, at sufficient channel count, memory depth and update rate. Moreover, stringent requirements are imposed on the electrical output characteristics.

Such mAWGs have been developed by several ion trapping

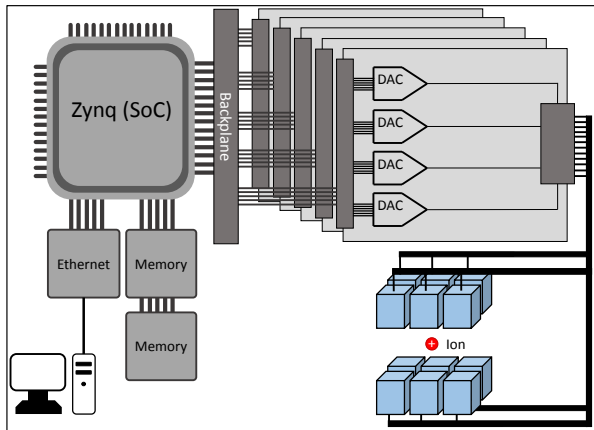


FIG. 4. System overview showing connections between individual modules of the mAWG and also critical parts of the experiment, ranging from control computer to ion trap electrodes.

groups and have been successfully employed to drive shuttling operations. These devices essentially consist of digital hardware receiving voltage waveform data from a control computer, storing these into a buffer memory and feeding them forward to digital-to-analog converters (DACs). The DACs and their subsequent output stages have the most significant impact on the performance of the system. Devices using parallel DACs have been developed by the NIST ion trapping and storage group<sup>[68]</sup> and the University of Siegen<sup>[69]</sup>, other groups employ home-built<sup>[70]</sup> or commercial systems using parallel or serial DACs.

The mAWG developed in Mainz is described in this work and makes use of serial DACs. It is optimized for individual control of a large number of channels and employs a centralized *Zynq* System-on-a-chip (SoC) device, which supplies digital waveform data to up to 80 DACs in real-time. It stores voltage waveform data on its on-board memory and supplies 24 additional digital I/O channels which can be used e.g. for laser control. A schematic showing the interplay of SoC, analog and digital modules and other essential components is presented in Fig. 4.

The mAWG is controlled and supplied with waveform data by a host computer using an Ethernet connection. The host computer sends data to CPU cores on the Zynq, which is stored in on-board dynamic random access memory (RAM) chips with a total storage capacity of 1 gigabyte. After receiving a trigger command from the host PC, the SoC streams the stored data to the connected DAC and digital output modules via the SoCs digital I/O pins. The DAC modules convert the digital signals to voltage waveforms. An overview of the general specifications achieved by the mAWG is given in Table I. More detailed specifications for the individual modules currently in use with the mAWG are given in the following sections.

Characteristic	Value	Unit
Max. data transfer rate	730	MBit/s
Sequence memory	900	MB
Max. internal clock rate	400	MHz
Signal clock rate	50	MHz
Sample hold time resolution	20	ns
Min. analog sample update time	360	ns
Max. number of analog channels	80	
Output voltage range	$\pm 40$	V
Min. analog resolution	1.2	mV
Slew rate	$\sim 20$	V/ $\mu$ s
Noise floor	$< 100$	$\mu$ V/ $\sqrt{Hz}$

TABLE I. Important performance specifications of the Mainz mAWG.

### A. Digital hardware

We employ a Xilinx Zynq-7000 SoC ZC702 Evaluation Kit, which provides the Zynq SoC, memory and Ethernet interface, as the central control unit. It is based on the XC7Z020 Zynq chip, which combines a dual core ARM Cortex A9 667 MHz CPU and an Artix-7 FPGA with 85000 programmable logic cells. The SoC ZC702 board, illustrated in Fig 5 (a), features a total of 1 GB DDR3 memory, a 1 Gb/s Ethernet connector and corresponding controllers, a total of 200 digital in/outputs, on-board flash memory and other components.

Communication between Zynq and host computer is established using an Ethernet-based TCP/IP connection utilizing the on-board Ethernet controller, managed by an ARM CPU core. The available USB connections are used to upload the drivers and software running on the ARM core and also to program the FPGA logic cells. During operation, data sequences are sent to the Zynq using the 1 Gb/s Ethernet connection, which is optimized for low latency ( $< 1$  ms) and high throughput ( $> 750$  Mb/s). This ensures that experiments requiring long data sequences, exceeding the 1 GB on-board memory, can be run in an efficient way.

On the host PC, a custom control software interfaces to all connected devices, including the mAWG. The control software converts voltage sample sequences into a binary format and sends them to the Zynq, which outputs these using a buffer system from the memory to the connected modules. The binary data is converted by the DACs to produce analog voltages. Additional execution control commands allow for interruption of the output by a predetermined duration, looping of a sequence and wait-for-trigger events.

Harnessing the versatility of the Zynq, future developments will focus on implementing a more advanced storage and control system for the experimental sequences. These will be split into sub-sequences, and the selection and streaming will be initialized by an execution control logic running on the SoC. This will make it possible to perform autonomous branching of sequences, conditioned on measurement results processed by the mAWG. Additionally, the mAWG will be interfaced with rf waveform generators for laser pulse control, therefore

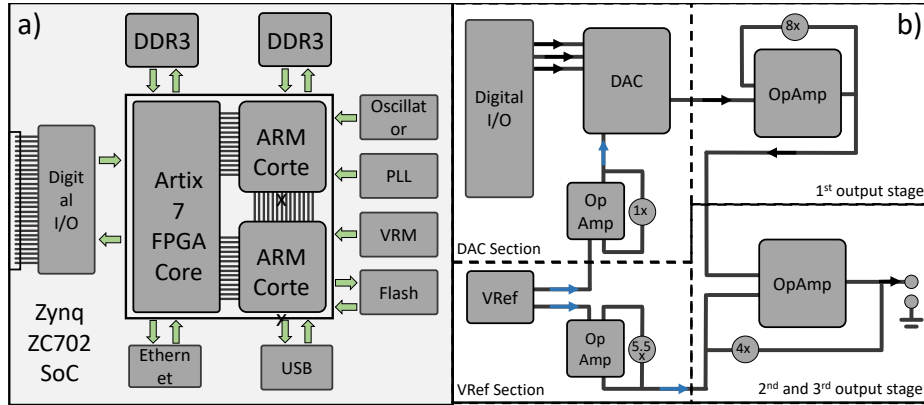


FIG. 5. (a) Simplified overview of the Zynq ZC702 SoC evaluation kit showing the relevant on-board controllers and components. The connections between the SoC and external on-board components are illustrated. (b) Essential components of a single analog output channel. The DAC section features an AD5541 DAC supplied with data by the digital hardware and a reference voltage supplied by the VRef section, buffered by an OpAmp close to the DAC. The 1st output stage yields an 8x voltage amplification, followed by the 2nd and 3rd output stage which amplify the voltage further by a factor of 4 and perform a level shift.

realizing an autonomous real-time system capable of shuttling and gate operations conditioned on in-sequence measurement results - a cornerstone for quantum error correction protocols running on a scalable QC platform.

## B. Digital signal routing

Routing of the binary data buffered on the Zynq is handled by a custom-developed back-plane. The Zynq I/O connections are directly connected to the back-plane, which distributes these to various digital I/O and analog output modules.

For the signals supplying the digital I/O modules, the signal conditioning takes place directly on the back-plane. Digital I/O modules are connected to the I/Os of the SoC via the back-plane and to the front-panel outputs via level translation buffers (TI SN74LVC06A and SPC BSX20). The I/Os of the digital modules are used to control laser pulses and control of other experimental components. Each module features 20 digital outputs and four inputs with a maximum update rate of 50 MHz.

Analog output modules do not feature processing or conditioning of the digital input signals, therefore the back-plane is engineered to process digital and clock signals to a format usable by the DACs. To that end, the data and clock signal timings are adjusted to ensure that the stringent timing requirements of the DACs are met. Buffering clock drivers (TI CDC328AD) are used to distribute the main clock to all connected analog modules and their DACs. The issue of clock timing errors is addressed using a clock delay circuit (using a variable capacitor and ON 74ACT74D flip-flop), which can be manually adjusted to achieve the required clock timings with respect to the digital data. The digital signals are also buffered (ON 74ACT541SC-ND), which helps to correct for timing mismatches and maintains the required logic voltage levels.

In addition, the DACs require a chip select signal, which initializes the shift of received binary data to the output stages. To reduce the amount of required digital I/Os, four DACs per module are supplied using a common chip select signal, which is buffered and distributed (ON 74ACT541SC-ND). While each DAC of a group can be updated independently, the update timings have to be the same, and also each DAC of a given group has to be updated even if the same voltage is to be maintained. The chip select, data and clock signals run through digital isolators (BCM HCPL-900J) in order to separate the grounds of the Zynq I/Os and the DACs. Galvanic isolation helps to prevent ground loops and reduces noise leakage from the digital signal processing and Zynq to the analog output modules.

## C. Analog output modules

Analog output modules are equipped with DACs followed by output stages. Design choices for the used components are based on the requirements of performing fast shuttling operations: Voltage update rate of  $\geq 2$  million samples per second (MSPS), voltage range of  $\pm 40$  V, a resolution of 16 bit, stability of at least one least significant bit (80 V/16 bit), sufficient bandwidth and slew rate ( $\geq 20$  V/ $\mu$ s) at low noise levels. Fig. 5(b) gives a schematic overview of the individual components used for the analog output modules.

For the most crucial component - the DACs - Analog Devices model AD5541 was chosen based on its update rate of 2.5 MSPS using a serial data interface, its low output noise of  $11$  nV/ $\sqrt{Hz}$  and 16 bit resolution, with a relative accuracy of  $\pm 0.5$  least significant bits (LSB). Significantly faster DACs are available, however these require a parallel data interface with 16 times more data lines per DAC. Other mAWGs used for control of trapped ions<sup>[68,69]</sup> feature parallel DACs, allowing for higher update rates, but require multiple FPGA controllers. For the intended operations being performed with this

mAWG, the 2.5 MSPS update rate of the *AD5541* is sufficient.

Each analog output module is equipped with 16 *AD5541* DACs and receives 16 identical clock signals, 16 independent serial data and four chip select lines from the back-plane. The output range of the DACs is set to 0 - 2.5 V by a voltage reference (ADR441). Output voltages of the DACs require further amplification and the unipolar range needs to be converted to a bipolar  $\pm 40$  V range. In addition, a low output impedance is required to guarantee a sufficient bandwidth.

The output circuit consist of two stages:

1. Pre-amplification with a gain factor of 8: An AD8510 op-amp and a resistor array are employed to achieve a stable gain factor, while ensuring that sufficiently low current is drawn from the DAC outputs. Despite the high gain of 8, this amplification stage maintains a large bandwidth of more than 3 MHz, while also reaching a slew rate of  $\geq 20$  V/ $\mu$ s. The AD8510 op-amps add further  $8 \text{ nV}/\sqrt{\text{Hz}}$  noise to the signal generated by the DAC. The total noise, which will also include noise from clock signal bleed-through and Johnson noise from the used resistors will then be amplified by a factor of 8, putting the lower noise limit of the signal to  $\sim 160 \text{ nV}/\sqrt{\text{Hz}}$  at this stage.
2. Level shifting and final voltage amplification with a gain factor of 4: The second stage uses an op-amp LTC6090, which features a maximum voltage output range of up to  $\pm 70$  V. Besides amplifying the input signal further by a factor of 4, a level shift from 0-20 V to  $\pm 40$  V is performed. This is accomplished using the on-board voltage reference, ensuring a symmetric bipolar output. The slew rate of  $\sim 20$  V/ $\mu$ s at the chosen gain sets the limit of a full voltage swing ( $+40 \text{ V} \leftrightarrow -40 \text{ V}$ ) time to about 4  $\mu$ s. Input voltage noise of the LTC6090 is specified to be  $14 \text{ nV}/\sqrt{\text{Hz}}$ , which adds to the minimum noise of  $\sim 160 \text{ nV}/\sqrt{\text{Hz}}$  on the signal after the first amplification stage. Total noise after the entire amplification stage will be characterized in more detail in the following section, but a lower limit is set by the  $\sim 160 + 14 \text{ nV}/\sqrt{\text{Hz}}$  input noise, which is multiplied by the gain (4) to  $\sim 700 \text{ nV}/\sqrt{\text{Hz}}$ .

Each analog output module features 16 output channels accessible via a D-sub 37 pin connector.

#### D. Noise characteristics

In this section, we present a detailed analysis of the analog voltage output performance of the mAWG, i.e. the noise characteristics in the frequency ranges particularly relevant for trapped ions, the long term voltage stability of the system, the inherent glitches and full voltage range pulse response.

Noise spectra were recorded using an Anritsu MS2781B spectrum analyzer in combination with an active probe Agilent 41800A. Displayed minimum noise of the spectrum analyzer is -167 dBm at 0.1 Hz RBW. The active probe (3 pF input capacitance and 100 k $\Omega$  input resistance) ensures that the

measurement instrument load does not significantly affect the measurement results. Its frequency response was measured flat across the range 5 Hz to 500 MHz.

To establish a reference noise spectrum, the input noise floor was recorded with the bare active probe connected to the spectrum analyzer input. Then, spectra were recorded for 0 V voltage output from the mAWG with and without sending (constant) digital updates, as shown in Fig. 6(a). At 0 V the DACs and first amplification stage are at half scale output and are not expected to perform better or worse compared to other output voltages. Generating a static voltage without digital updates, see Fig. 6(a), represents an ideal case for low noise performance corresponding to the scenario when ions are statically confined in the trap. Outputting static voltages with constant digital updates of the same digital data is a common case when some voltages are kept constant and others need to be switched for shuttling, see Fig. 6(b). Digital updates need to be sent even if the voltage is kept static, since multiple DACs share a chip select channel. A noise spectrum for this case is presented in Fig. 6(b).

The measured noise exhibits a significant increase towards lower frequencies, which is expected due to flicker noise, following a  $1/f$  behavior, combined with Johnson noise stemming from the input resistances. Johnson noise is frequency independent, but a  $1/f$  behavior is expected taking into account the passive RC load given by the active probe. Furthermore, the noise peaks visible at 100 kHz and 200 kHz can be explained by the presence of active switching power supplies in the vicinity of the measurement setup.

The output noise spectra shown in Fig. 6 display a noise floor on the order of  $\sim 3 \mu\text{V}/\sqrt{\text{Hz}}$  in the frequency range below 1 MHz, which is significantly higher than the noise floor of the measurement equipment. In the frequency range around 1 MHz the noise converges towards the level of the equipment noise floor and becomes indistinguishable at about 10 MHz.

The DACs in combination with op-amps are expected to contribute at least  $\sim 700 \text{ nV}/\sqrt{\text{Hz}}$  of noise within the bandwidth of the amplification stages (2 MHz). At low frequencies (1 kHz) the reference voltage circuit will increase the minimum noise floor to  $\gtrsim 2 \mu\text{V}/\sqrt{\text{Hz}}$ .

The observed voltage noise spectral densities  $S_V(\omega_j)$  would result in motional heating rates  $\Gamma_h$  for a given mode  $j = x, y, z$  at secular frequency  $\omega_\xi$  in quanta per second via the relation<sup>[71]</sup>

$$\Gamma_h = \frac{e^2}{4m\hbar\omega_j} \xi_j^2 S_V(\omega_j). \quad (1)$$

Here, the  $\xi_j \approx 1000 \dots 2000 \text{ m}^{-1}$  are geometric factors characterizing the electric field generated by the neighboring trap electrodes at the ion location, pointing along direction  $j$ . We therefore estimate axial heating rates of up to  $10^4$  quanta per second, which is much higher than acceptable. We employ additional passive filters to reduce the voltage noise spectral densities by several orders of magnitude and will be discussed in chapter V.

When digital updates corresponding to the same voltage are sent to the DAC, the noise, depicted in Fig. 6(b), shows a clear increase to  $\sim 10 \mu\text{V}/\sqrt{\text{Hz}}$  at the update frequency of



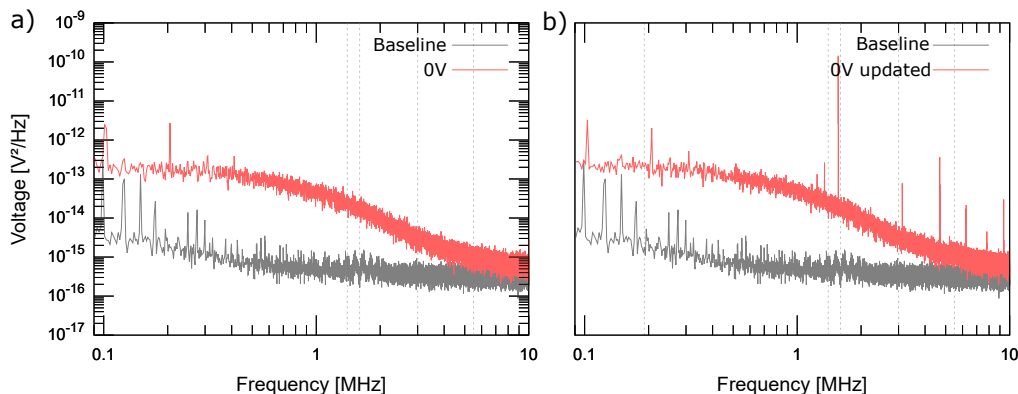


FIG. 6. Spectra showing a baseline measurement and noise measurement for 0 V output without updates (a) and (b) with updates. The spectra display the expected  $1/f$  dependence with additional pickup signals, originating from switch mode power supplies (100 kHz and 200 kHz). The spectrum with updates (b) also shows the update frequency close to 1.7 MHz and its higher harmonics. The vertical dashed lines indicate typical secular trap frequencies at about  $2\pi \times 1.5$  MHz,  $2\pi \times 3.5$  MHz and  $2\pi \times 4.5$  MHz.

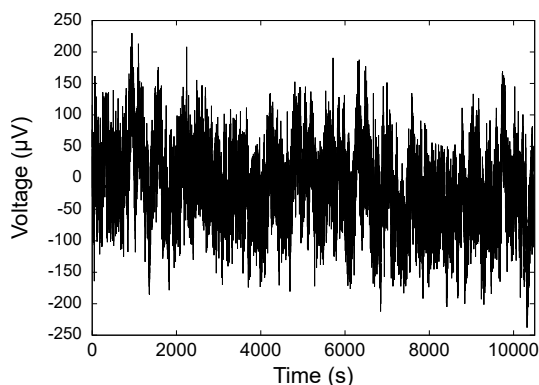


FIG. 7. Voltage stability recording showing slow and fast voltage fluctuations measured each second over a time period of 10000 seconds. Slow drifts, even over this large time period, are significantly smaller ( $\sim 50$   $\mu\text{V}$ ) than faster drifts ( $\pm 200$   $\mu\text{V}$ ).

$\sim 1.7$  MHz and its higher harmonics. By appropriate choice of the secular frequencies, update-noise induced excitation can be avoided.

Long term voltage stability and output voltage accuracy were characterized using an Agilent 34411A 6.5 digital multimeter. The output voltage was set to 0 V in order to use the smallest measurement range  $\pm 100$  mV with the lowest measurement noise floor of 3 nV and best measurement accuracy of 100 nV, which is well below the LSB of the mAWG of  $\sim 1.2$  mV. Voltage samples were recorded over a period of more than 160 min at a sampling rate of 1/s, the result is shown in Fig. 7. The rms voltage deviation of about  $140$   $\mu\text{V}$  on timescales beyond 1 s is smaller by a factor of 10 compared to 1 LSB of the mAWG. Voltage drifts will detrimentally affect entangling gates due to a mismatch between the preset and actual secular frequencies<sup>[72]</sup> and motional dephasing, see Sec. VI 2

An important parameter of the system is the *slew rate*,

Characteristic	Value	Unit
Noise level static output @ 1 MHz	$5 \times 10^{-14}$	$\text{V}^2/\text{Hz}$
Max. glitch impulse area	3(1)	nV·s
Max. slew rate	20	$\text{V}/\mu\text{s}$
rms voltage stability	$\pm 140$	$\mu\text{V}$

TABLE II. Electrical performance characteristics of the mAWG.

which characterizes a limit on how fast the output voltage can be changed without causing a non-linear response. A full output voltage swing  $-40$  V  $\rightarrow$   $+40$  V was recorded using a MSOX3104A mixed-signal oscilloscope and is shown in Fig. 8(a). The maximum achieved slew rate is determined to be  $\sim 20$   $\text{V}/\mu\text{s}$ , consistent with the specified value for the LTC6090 operational amplifier used in the second amplification stage. As can be seen in Fig. 8(a), the beginning and end of a full voltage swing display low-pass characteristics due to charging of additional trim capacitors. These trim capacitors (6.5 to 30 pF range) are placed between the negative input and output of the LTC6090 to prevent ringing at this amplification stage.

Glitches, i.e. undesired voltage spikes, occur when the DAC switches to a different output voltage. Due to their short duration, they cover a wide frequency range and can lead to spurious motional excitation of the trapped ions upon propagation to the trap electrodes. Glitches are commonly characterized in terms of glitch impulse area, which is proportional to the number of bits flipped throughout the update. The measured glitch signal shown in Fig. 8(b) occurs during a programmed voltage change of one LSB at the mid-scale voltage output (0 V), which causes *all bits* of the DAC to flip. This produces the worst-case glitch with an impulse area of 3(1) nV·s. Even if the static noise level of the mAWG would be sufficiently low to yield satisfactory heating rates, the presence of glitches makes additional low-pass filters a necessity. The glitch impulse area has also been measured using a MSOX3104A mixed-signal oscilloscope with a mea-

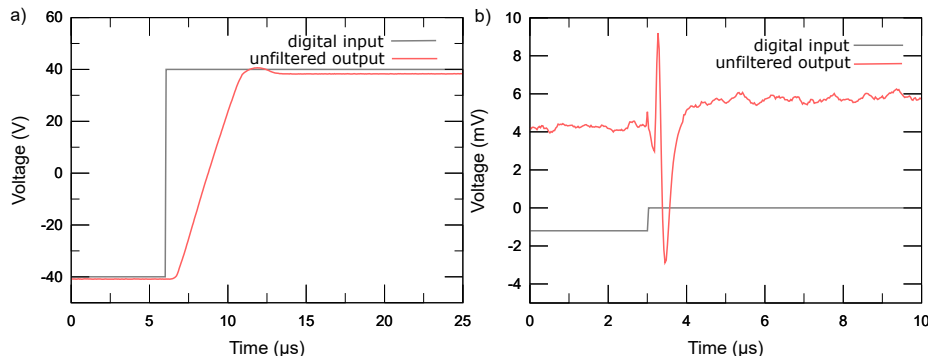


FIG. 8. (a) Recorded full voltage swing from -40 V to 40 V. The initial and final settling behavior is due to trim capacitors that are employed to prevent overshooting and ringing at the output of the amplification stage. (b) Recording of a voltage glitch on the order of  $\sim 10$  mV occurring when the DAC switches all 16 output bits (1000 0000 0000 0000 0000 to 0111 1111 1111 1111).

surement bandwidth of 1 GHz and a resolution of 12 bits upon averaging.

Based on the measurements discussed above, a performance summary of the analog output modules is given in Tab.

**II**. In the following chapter **V**, the performance specifications will be analyzed in more detail, when the system is characterized in combination with an ion trap setup, including external filter stages and wiring.

## V. ROUTING OF RF AND DC SIGNALS TO ION TRAP APPARATUS

Trapping ions in a segmented Paul trap requires large rf voltage amplitudes to provide confinement in the transverse directions and lower dc voltages to provide electrostatic confinement and control in the axial direction. In the following section we will discuss how large rf voltages, (e.g. 200 V amplitude at  $\sim 35$  MHz) are generated and applied to trap electrodes and how dc voltages generated by the previously discussed mAWG, section **IV** are filtered and connected to dc electrodes inside a UHV chamber. Furthermore we will discuss effects of inadequate DC and RF grounding and an additional noise analysis will be presented for a realistic experimental setup including all cables and filters.

### A. Trap Drive Routing and Stabilization

Generating large rf voltages for the operation of a Paul trap commonly requires the use of a resonant circuit. Different resonator types depending on the ion trap type and ion species are employed. Low atomic mass ions are commonly trapped at higher trap drive frequencies on the order of up to 150 MHz, making a quarter-wave coaxial resonator a favorable choice<sup>[73]</sup>. Operating a cryogenic ion trap apparatus close to liquid helium temperatures requires the resonator to be placed inside the vacuum chamber near the trap. This has led to the development of superconducting helical resonators<sup>[74]</sup> and discrete component resonators using copper coils or superconducting coils<sup>[75][76]</sup>. The most widely used resonator is the heli-

cal resonator<sup>[77]</sup>, which can be used for a variety of frequencies and achieves a high quality factor at room temperature ensuring a large rf voltage gain and high signal-to-noise ratio.

The resonator is typically supplied by an rf signal generator via a low noise rf amplifier, often including an active amplitude stabilization circuit. For the microfabricated ion trap presented in Sec. **III**, a low noise signal generator (R & S SMB100), which is further amplified by a high-gain (46 dB) high-power (5 W) rf amplifier (minicircuits ZHL-5W-1) is connected to a home-built helical resonator.

Temperature drifts, and drifting stray capacitances will cause trap drive amplitude fluctuations and therefore instabilities of the confining electric potential. As a result, the transverse secular frequencies will be unstable, which negatively effects the fidelity of gate operations, especially if two-qubit gates are implemented using the transverse modes, see Sec. **III**. To mitigate these fluctuations, an active stabilization system was developed, which employs a capacitive divider at the resonator output sampling the current rf amplitude. The signal is fed, via a rectifier, to a proportional-integral (PI) servo, which adjusts the signal generator output in real time, similar to the system described in<sup>[78]</sup>.

The challenge in active stabilization of the rf output amplitude lies in the high-impedance of the signal obtained from the capacitive divider, making the loop prone to electric noise pickup. Our present design makes use of a capacitive divider, consisting of a 1 pF pickup capacitor and a 60-90 pF dividing capacitor, directly followed by an active rf buffer (TI BUF634). A schematic of this circuit is shown in Fig **9**. The buffer transforms the signal from the divider to a low impedance and prevents noise pickup within the stabilization loop. Fluctuations of the transverse secular frequencies due to the amplitude instabilities are on the order of  $\sim 2\pi \times 6$  kHz without stabilization and as low as  $\sim 2\pi \times 20$  Hz ( $\sim 4 \times 10^{-6}$  long-term stability) with active stabilization. Therefore, transverse mode secular frequency drifts do not represent a bottleneck for the fidelity of entangling gate operations.

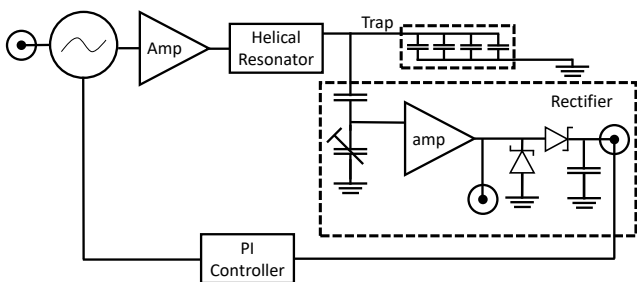


FIG. 9. Diagram showing the rf stabilization system, which uses a BNC connector to attach an adjustable capacitive divider to the resonant circuit. The operational amplifier buffers the picked up rf signal and decouples the stabilization circuit from the resonant circuit. The signal is then rectified and fed to a PI controller.

## B. Segment Voltage Filtering and Wiring

Technical noise, inherent to all electrical components, will have a detrimental effect on the system performance. Voltage noise at the secular frequencies leads to heating of the ions, and noise at lower frequencies will lead to motional decoherence, deteriorating the fidelity of entangling gate operations<sup>[79]</sup>. A lower bound for the heating rates is given by electric field noise generated by thermally activated processes at the trap surfaces<sup>[65,71,80,82]</sup>.

Technical noise can be suppressed below the limit imposed by surface noise<sup>[83]</sup> by suitable filtering, however the shuttling-based quantum computing approach requires a sufficient bandwidth for fast operations, such that the heating rates are typically given by technical noise.

A combination of low-pass filters is employed to reduce electric noise at frequencies below typical secular frequencies ( $2\pi \times 1 - 7$  MHz) as much as possible. The cut-off frequency was chosen for sufficient suppression of noise at the secular frequencies, while still allowing for shuttling operations on timescales between 10 and 100  $\mu$ s. Throughout separation and merging operations (see Sec. [V I C](#)), the axial secular frequency transiently drops to a few 100 kHz, therefore a good rule of thumb is to choose the filter cut-off to be below the minimum secular frequency obtained throughout these operations. In our case, the minimal secular frequency during ion separation was determined to be 275 kHz and the cut-off frequency of the main RLC low pass filters was thus chosen to be 100 kHz.

Three filter stages are employed in our system. First, a set of high frequency LC filters are placed at the outputs of the mAWG and used to prevent bleed-through of digital clock signals and other higher frequency noise from reaching the ion trap electrodes. These filters make use of a commercial LC electromagnetic interference (EMI) filter (NFE61PT472C1H9L) with a cut-off frequency of 400 kHz using a ferrite core based inductance and a capacitor. Ferrite cores are lossy at high frequencies and lead to dissipation of high-frequency signals. As shown in the schematic in Fig [10](#) (a), the filter can be effectively represented by two inductors, both sharing a common ferrite core, and a central capacitor of

4.7 nF. A total of 16 LC filters, shown in Fig [10](#) (a) with additional resistor are placed in a custom made D-Sub connector, which provides shielding and allows for small diameter RG178 coaxial cables to be directly soldered to the outputs of the high frequency filters.

The second filter stage, possessing the lowest cut-off frequency, consists of PCB mounted PI-type filters in shielded metal boxes using D-sub connectors at the in and output. This makes it possible to easily exchange filters for a different cut-off frequency. The filters are directly plugged into the feedthroughs of the vacuum apparatus, see Fig [10](#) (b). The filters consist of two 22 nF capacitors, a 150  $\mu$ H inductor and a 69.8  $\Omega$  resistor per channel. The 3rd order filter is designed for a cut-off of 100 kHz. The inductors are shielded to reduce inductive coupling and thus cross-talk between neighboring channels.

As a third and final filter stage, in-vacuum RC filters near the trap are used to reduce potential noise pick up inside the vacuum chamber and to help provide a low impedance path to ground for dc electrodes at the rf drive frequencies.

The capacitances of these filters ensure a low impedance path to ground for the dc electrodes of the ion trap, which are capacitively coupled to the rf electrodes. If the filter capacitance would not be present, a significant rf voltage would drop at the resistive impedance of the dc supply lines. This would yield an increased effective load of the rf resonator, deteriorating its performance by decreasing the voltage gain and increasing its linewidth. Due to the reduced signal-to-noise ratio heating rates due to noise on the rf signal, at frequencies offset from the trap drive frequency by the secular frequencies would increase. Furthermore, without a low impedance path to ground for the rf, the capacitively coupled dc electrodes would show a significant rf potential, instead of rf ground, compromising the confinement potential of the trap.

In-vacuum RC filters are placed on the trap mount made from alumina and are shown in Fig [10](#) (c). The ultra-high vacuum environment requires careful choice of the filter components. The trap mount is made of alumina, and tracks are printed on it using sintered metal paste. The 10  $\Omega$  filter resistors are directly printed onto the alumina. Ultra-high vacuum compatible single layer ceramic capacitors arrays (2 nF) are soldered onto the metal tracks of the PCB for grounding and connected directly to the trap and signal tracks using wire bonding. These filters feature a cut-off frequency of 8 MHz, which only removes high frequency noise close to the drive frequency and above.

Coaxial cables (RG178), are soldered to each output pin of the high frequency filters at the mAWG output and connected to the input pins of the PI-filters. They are bundled together and placed inside an additional metal mesh shielding shroud to further reduce noise pickup. Inside the vacuum chamber, space restrictions require the use of simple single-stranded wires without shielding to make a connection between the feedthrough and the RC filter board.

Careful design of the grounding topology can have a significant impact on the system performance in terms of heating rates and motional dephasing. Possible ground loops, i.e. spurious electrical potentials between circuit points intended

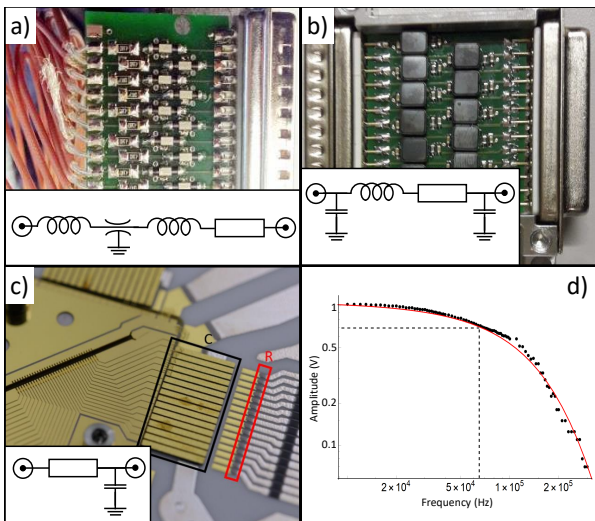


FIG. 10. Pictures showing the three filters placed between the mAWG and the ion trap electrode. The high frequency LC filter is shown in **a**), made up of two ferrite core inductors and a 4.7 nF capacitor, followed by the main  $\Pi$  filter shown in **b**). These filters are made up of two 22 nF capacitors, a 150  $\mu$ H inductor and a 69.8  $\Omega$  resistor. The last, in-vacuum filter stage is shown in **c**). It is placed next to the trap and is comprised of a 10  $\Omega$  printed resistor and a 2 nF capacitor. **d**) Shows the filter response curve of the combined filters and wiring system. Dashed lines indicate the 3db point of the filter response curve.

to be ground, result in additional noise due to current flow between these points. The mAWG is equipped with an isolating transformer separating the mains ground from the ground of the power supplies. Analog grounds of the mAWG output modules are carefully routed to a common ground of the vacuum apparatus. The analog ground pins of the output modules are connected to the shielding of the coaxial cables between output filters and PI-filters, which have a common ground for all channels. An additional shielding metal mesh is wrapped around the coaxial cables making contact between analog output ground and filter ground. Filter ground is directly connected to the vacuum chamber via the D-Sub connectors of the vacuum feedthroughs. Vacuum apparatus ground is finally connected to the laboratory ground using low resistance connections.

Filter responses and cut-off frequencies of individual filters are only of limited use since a filter or even the cables can influence the behavior of the consecutive filter and therefore the entire system. We have thus measured a filter response curve of the combined filters and wiring system placed between the mAWG and ion trap. The results of this measurement are shown in Fig. 10(d). The combined filter and wiring setup has a significantly lower cut-off as compared to the dominating PI-filter. This is due to the 50  $\Omega$  resistor after the first LC filter, which is in series with the 69.8  $\Omega$  resistor of the PI-filter.

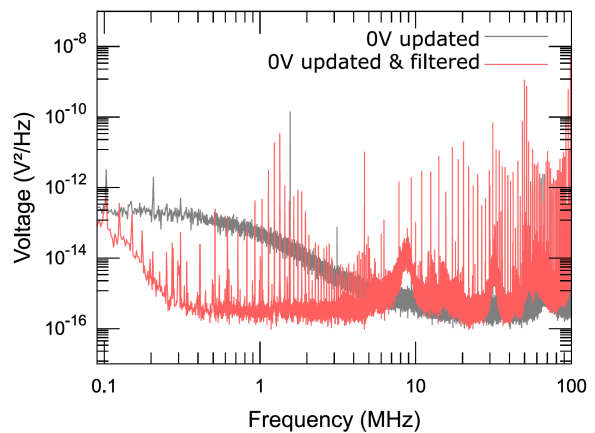


FIG. 11. Measured noise spectral densities for 0 V output at continuous DAC updates. The gray curve is also shown in Fig. 6 and corresponds to measurement at the mAWG output, and the red curve corresponds to measurement at the PI-filter output. As the measurement is performed on the bare filter output pins without proper shielding, noise pickup occurs and manifests in sharp peaks. The filtered signal reaches the measurement noise floor between 300 kHz and 5 MHz, compare to Fig. 6. The actual noise suppression by the PI-filters is presumably better.

### C. Filter Response and Technical Performance Analysis of the Setup

In this section, we discuss the effect of the main PI-filter stage on the static noise on the dc lines and the glitches occurring upon DAC updates.

Measurements of the mAWG output noise shown in Sec. IV D indicate that additional filtering is required to achieve sufficiently low heating rates. Noise spectral densities measured at the output of the PI-filter stage are shown in Fig. 11. The measurement has been performed identically to the noise measurements shown in Sec. IV D. The output channel has been set to 0 V, and output noise with continuous DAC updates is shown in comparison to the measurement directly at the mAWG output. In the range between 100 kHz and about 5 MHz, noise suppression by the filters is clearly visible. However, the measurement is limited by the noise floor of the used spectrum analyzer of about  $10 \times 10^{-16} \text{ V}^2/\text{Hz}$ , this measurement scheme does therefore not allow for a quantitative prediction of the technical noise contribution to ion heating rates, see Sec. VI I. Spurious peaks can be seen in the spectrum, these presumably occur because the measurement is prone to electromagnetic pickup, such that the noise peaks do not necessarily occur in the trap setup. The broad peak slightly below 10 MHz corresponds to the self resonance of the inductor used for the PI-filters.

The voltage glitches observed when switching DAC bits are of broadband nature, see Sec. IV D and will therefore be mitigated by the low pass filters. Significant suppression of the glitches can be seen in Fig. 12 in comparison to Fig. 8. Glitch energy can not be entirely removed from the system since the low pass filters charge up during filtering and slowly dissipate



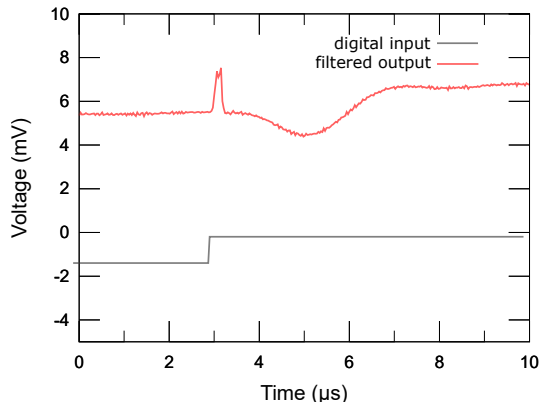


FIG. 12. Voltage glitch occurring when the DAC switches all 16 output bits (1000 0000 0000 0000 0000 to 0111 1111 1111 1111), affected by the filter system. The glitch amplitude is reduced by a factor of  $\sim 4$  and significant smearing compared to unfiltered glitches can be observed.

the energy after the glitch has passed, a phenomenon commonly called glitch smearing.

## VI. SYSTEM CHARACTERIZATION

The electric field noise affecting the trapped-ion qubits is a key limitation to the performance of the architecture. It stems from molecular processes on the trap surfaces<sup>65,84</sup> and from the electrical circuitry supplying the dc and rf trapping voltages. While the latter -technical- noise can in principle be filtered, the shuttling-based trapped-ion QC approach requires supplying a bandwidth sufficient for fast shuttling operations to the dc electrodes, such that technical noise will typically limit the system performance. Electric field noise manifests in two detrimental effects: First, noise at the secular frequencies causes heating of the stored ions<sup>71</sup>, resulting in thermal population of the secular modes, which leads to decreased entangling gate fidelities. Second, noise ranging from slowly varying secular frequency offsets to secular frequency modulation at up to a few 100 kHz leads to decoherence of transient motional superposition states during gate operations, which also represents an error source.

Therefore, our architecture requires sufficiently low noise on the trap electrodes across the entire range up to the secular frequencies, and in addition a suitable tradeoff has to be made between the bandwidth of the dc signals allowing for fast shuttling operations and the overall noise level suppression. Here, we present the resulting performance figures in terms of heating rates and motional coherence.

### 1. Ion heating

The heating rates on all three secular modes are measured for a single ion in the laser interaction zone (LIZ), i.e. the trap segment to which all laser beams are directed. The mea-

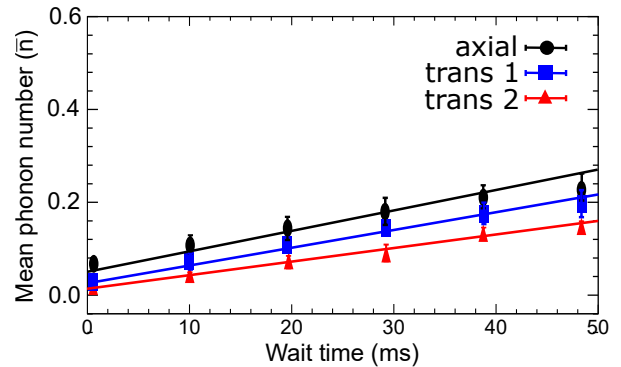


FIG. 13. Heating rates: Measured mean thermal phonon numbers on all secular modes of a single ion with variable wait times after sideband cooling are shown with an external low-pass filters at a cut-off frequency 100kHz. Heating rates are 5.5(3) phonons per second for the axial mode, 4.8(2) for the transverse mode 1 and 3.6(1) for transverse mode 2.

surements utilize the Rabi flopping method as described in Sec. VII A. Here, a variable wait time is introduced between sideband cooling close to the ground state of all modes and the probe pulse. The inferred mean thermal phonon numbers versus wait time are shown in Fig. 13. On the dc lines, PI-type low-pass filters at a cut-off frequency of 100kHz were employed, see Sec. V. The resulting heating rates are 5.5(3) phonons per second for the axial mode at  $2\pi \times 1.49$  MHz, 4.8(2) for the transverse mode 1 at  $2\pi \times 3.88$  MHz and 3.6(1) for transverse mode 2 at  $2\pi \times 4.66$  MHz. More sets of heating data have been acquired for different trap voltages, i.e. different secular frequencies. It was found that the dependence of the heating rates on the secular frequencies is not consistent with a proper power-law behavior, as would be expected for anomalous heating originating from surface heating<sup>85</sup>. This indicates that at least the transverse modes are predominantly affected by technical noise. This is supported by the measured noise spectrum at the output of the  $\Pi$  filter, Fig. 11, which exhibits many resonances in the range of typical secular frequencies.

This unusual behavior can be explained by the significant voltage noise peaks observed when the PI-type low-pass filters is connected to the mAWG show in Fig. 11 and discussed in section V. These noise peaks can overlap with the secular frequency or a combination of the secular frequency and drive frequency. This will lead to a significant increase in technical noise, which can dominate the anomalous heating for that mode.

### 2. Motional dephasing

Noisy dc and rf trap voltages lead to fluctuating secular trap frequencies, which in turn lead to dephasing of motional superposition states occurring during entangling gate operations<sup>72,79</sup>. White secular frequency noise leads to exponential decay of motional coherences at a rate  $\gamma_m$ . We measure these rates on the transverse secular modes of a single ion in

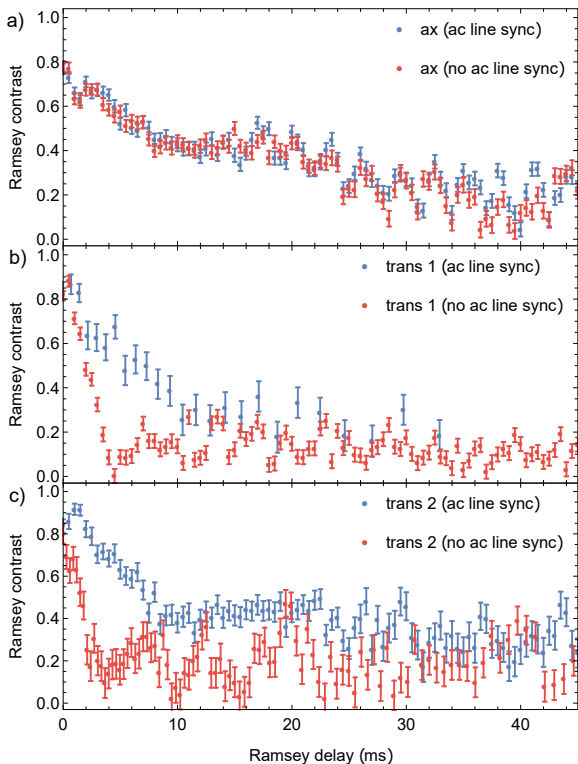


FIG. 14. Motional coherence decay. We measure the decay of superposition state coherence for all three secular modes of a single ion (see text). Data is shown for the cases with (without) triggering the measurement to the ac mains in blue (red), for the axial secular mode in **a**), the lower-frequency transverse mode in **b**) and the higher-frequency transverse mode in **c**).

the motional ground state in the LIZ by means of a motional Ramsey scheme. We proceed in the following steps: i) A qubit superposition  $(|\uparrow\rangle + |\downarrow\rangle)|0\rangle$  is created by a resonant  $\pi/2$  qubit rotation, ii) a  $\pi$  rotation on the red sideband of the mode of interest creates the superposition  $|\uparrow\rangle(|0\rangle + |1\rangle)$ , iii) dephasing takes place during a variable wait time  $T$ , iv) another  $\pi$  rotation maps the motional superposition back into a spin superposition, and v) a concluding  $\pi/2$  spin rotation with (without)  $\pi/2$  phase shift serve for measurement of the spin  $\hat{\sigma}_X$  ( $\hat{\sigma}_Y$ ) operators. The resulting measured Ramsey contrast is then obtained from  $\mathcal{C}(T) = \sqrt{\langle \hat{\sigma}_X \rangle^2 + \langle \hat{\sigma}_Y \rangle^2}$  and decreases with  $T$ . The results are shown in Fig. 14.

In order to verify the presence of 50 Hz ac line pickup on the trap electrodes, the measurements were carried out with and without triggering to the ac mains signal. While no difference is observed for the axial mode, ac line triggering yields substantially longer coherence times on both transverse modes. This result indicates either ac mains pickup in the rf system or ac mains common-mode noise on the dc lines. Entangling gates will suffer errors from motional dephasing of magnitude  $\lesssim t_g \gamma_m$ , where  $t_g$  is the gate duration<sup>72</sup>. We estimate the error contribution from this effect to be smaller than 0.25% for gate of  $t_g = 50 \mu\text{s}$  driven on the higher-frequency transverse mode. This shows that this gate error source -which is often

disregarded- can contribute significantly to gate error budgets. We emphasize the importance of measuring motional dephasing rates along with heating rates when the performance of a trap setup is to be characterized.

## VII. SHUTTTLING

Shuttling operations are executed by applying varying voltage potentials to the dc electrodes, leading to a change of trapping potentials along the axial direction over time. For example, we consider a single ion confined in a harmonic electrostatic potential well generated by a negative trapping voltage applied to segment  $n$  while all other segments are kept at 0 V. Ramping the voltage at segment  $n$  to 0 V while simultaneously ramping the neighboring segment  $n+1$  to a negative voltage, the electrostatic potential well will shift along the trap axis, from segment  $n$  to  $n+1$ . The ion confined within this well will move along with respect to the center of the potential well. This corresponds to a pendulum with dragged support, which can lead to oscillatory excitation along the direction of transport, increasing at short process times.

As explained in Sec. III, shuttling operations should take place as fast as possible, while motional excitation is to be avoided. In our architecture, entangling gates and readout are only sensitive to transverse motion, see Sec. II. Therefore, the predominantly axial excitation can be tolerated to some extent. However, excessive axial excitation amplitudes are to be avoided, as there is i) residual coupling to axial motion throughout gates and readout, ii) anharmonic coupling between axial and radial collective modes, iii) large axial excitation can render separation/merging operations unreliable and iv) oscillation amplitudes comparable to laser focus size lead to undesired intensity modulation during gate operations. Importantly, as the trap geometry is non-ideal, i.e. not entirely uniform and symmetric. Therefore, shuttling along the trap axis also leads to parasitic transverse excitation.

In order to realize the desired operational principle of the quantum processing node, sequences for reconfiguration of the qubit register have to be carried out, which consist of three elementary shuttling operations, see Fig. 1.

- **Linear transport:** Movement of single ions or small ion crystals along the trap axis.
- **Separation/merging:** Ion crystals are split into single ions and/or smaller crystals, or the reverse process is carried out.
- **Swapping:** Physical swapping through rotation of ion crystals, equivalent to a logical SWAP gate.

In the following, we describe the measurement methods employed for characterizing the performance of the shuttling operations in Sec. VII A then we cover the operational building blocks linear transport (Sec. VII B), separation / merging (Sec. VII C) and ion crystal rotation (Sec. VII D).

### A. Excitation measurement

In order to verify and optimize shuttling operations, suitable measurement schemes for characterizing the state of a given motional mode of a single ion or ion crystal is required. A well-established method consists of recording Rabi flops on a coherently driven transition between long-lived internal states of the ions, which feature a suitable coupling to the motional mode(s) of interest<sup>[17,86]</sup>. In our case, we utilize stimulated Raman transitions<sup>[87]</sup> between the Zeeman sublevels of the  $S_{1/2}$  ground state of  $^{40}\text{Ca}^+$ , i.e.  $|m_J = -1/2\rangle \equiv |\downarrow\rangle$  and  $|m_J = +1/2\rangle \equiv |\uparrow\rangle$ . These are driven by laser beam pairs, which are directed such that the effective wavevectors point either along the axial direction or along the transverse directions. The resulting Lamb-Dicke factors, characterizing the coupling to the motion, range from about 0.05 for the lower-frequency transverse center-of-mass mode of a two-ion crystal, up to about 0.24 for the axial vibration of a single ion. Note that such measurements can also be performed by coherently driving electronic transitions which are dipole-forbidden, such as the  $S_{1/2} \leftrightarrow D_{5/2}$  electric quadrupole transition in alkaline-earth ions<sup>[88]</sup>.

The shuttling operations predominantly cause coherent oscillatory motion, therefore one is not interested in full quantum state reconstruction, but rather in obtaining the mean phonon number  $\bar{n} = |\alpha|^2$  pertaining to the displacement parameter  $\alpha$ . Resonantly driving Rabi flops on a sideband transition where a  $\pi$  rotation (a spin flip in our case) is accompanied by a change of  $\delta n$  phonons, starting with a single ion in  $|\downarrow\rangle$ , the probability to find the ion in  $|\uparrow\rangle$  after exposure time  $t$  is given by

$$P_{|\uparrow\rangle}^{(\delta n)}(t) = \sum_{n=0}^{n_{\max}} p_n(\alpha) \frac{1}{2} (1 - \cos(\Omega_{n,n+\delta n} t)) \quad (2)$$

Here,  $p_n(\alpha) = e^{-|\alpha|^2} \frac{|\alpha|^{2n}}{n!}$  is the Poissonian phonon number distribution pertaining to oscillatory excitation, and Rabi frequencies  $\Omega_{n,n+\delta n}$  depend on the phonon number via<sup>[87]</sup>

$$\begin{aligned} |\Omega_{n,n+\delta n}| &= \Omega_0 \eta^{\delta n} e^{-\eta^2/2} \sqrt{\frac{n_{<}!}{n_{>}!}} L_{n_{<}}^{\delta n}(\eta^2) \\ &\approx \begin{cases} \eta\sqrt{n} & \delta n = -1 \\ 1 - \eta^2 n & \delta n = 0 \\ \eta\sqrt{n+1} & \delta n = +1 \end{cases}, \end{aligned} \quad (3)$$

where  $\Omega_0$  is the base Rabi frequency,  $\eta$  is the Lamb-Dicke factor,  $n_{<}$  ( $n_{>}$ ) is the smaller (larger) number of  $\{n, n + \delta n\}$  and  $L_n^m(x)$  are the generalized Laguerre polynomials. The approximation in the second line holds within the Lamb-Dicke regime  $\eta n \ll 1$ , where the spatial extent of the wavefunction is much smaller than the wavelength of the driving radiation. The three most common cases are the first red sideband ( $\delta n = -1$ ), the first blue sideband ( $\delta n = +1$ ) and the carrier transition ( $\delta n = 0$ ). For the characterization of heating rates, as shown in Fig. 13, the Poissonian phonon number distribution in Eq. 2 has to be replaced with a thermal distribution

$p_n(\bar{n}) = \bar{n}^n / (\bar{n} + 1)^{n+1}$ , with the mean thermal phonon number  $\bar{n}$ .

In order to increase the accuracy of such measurements, Rabi flops can be recorded on several sidebands, which also serves for fixing parameters such as the base Rabi frequency  $\Omega_0$  or the Lamb-Dicke factor. The model Eq. 2 can be straightforwardly extended to the presence of spectator modes<sup>[89]</sup>, which is required e.g. for two-ion crystals or for characterizing the state of transverse secular modes, where both modes for a single ion feature nonzero Lamb-Dicke parameters. Moreover, the model can be extended to include thermal excitation as well, which is required to characterize separation processes at long durations<sup>[90]</sup>.

Precise measurement of motional amplitudes using the method described above requires taking large amounts of data - typically  $10^4 - 10^5$  individual measurements are required to infer motional excitation at a resolution down to 0.1 phonons. Therefore, for efficient calibration of the shuttling operations, a more convenient method is needed. In<sup>[91]</sup>, a suitable metric coined *pseudo-energy* was introduced, which has the following properties: i) It should scale monotonously with the mean phonon number up to an upper limit, ii) it should assume zero for  $\bar{n} = 0$  and iii) should exhibit an almost constant slope with respect to  $\bar{n}$  across the region of validity. Such metric can be constructed as the weighted sum of a set of spin readout results pertaining to different sideband transitions  $\delta n^{(i)}$  and probe times  $t_i$ . With the parameters being tailored for a specific purpose, such a measure can serve e.g. to efficiently minimize shuttling-induced excitation with respect to given control parameters.

#### 1. Simplified measurement scheme

A rather simple and robust measurement scheme can be applied for small excitations, i.e. values of  $\bar{n}$  for which  $p_0(\alpha) \gg 0$  holds. Probing a red sideband for a range of time values  $t$  and averaging the resulting values  $P_{|\uparrow\rangle}^{(\delta n)}(t)$  is equivalent to averaging Eq. 2 over time. For all terms except  $n = 0$ , the right-hand-side of Eq. 2 yields a constant:

$$\begin{aligned} \overline{P_{|\uparrow\rangle}^{(\delta n)}} &= \frac{1}{2} \sum_{n=1}^{n_{\max}} p_n(\alpha) \approx \frac{1}{2} (1 - p_0(\alpha)) \\ \Rightarrow \bar{n} &= -\ln \left( 1 - 2\overline{P_{|\uparrow\rangle}^{(\delta n)}} \right). \end{aligned} \quad (4)$$

Therefore, sufficiently small values for  $\bar{n}$  pertaining to a Poissonian phonon number distribution can be estimated from averaging recorded red sideband excitation probabilities over time. Eq. 4 also holds for the case of coupling to multiple motional modes and in the presence of additional dephasing, and can therefore conveniently be applied for characterizing oscillatory excitation on multi-ion crystals.

## B. Linear transport

The first demonstration of transport in a segmented trap was reported in [92]. In [45], it has been shown that qubit states are preserved during transport, and in [93], adiabatic transport retaining the ground state of axial motion has been demonstrated. In [91,94], *diabatic* transport has been shown: Due to the (coherent) oscillatory nature of the transport-induced excitation, it is possible to control the residual excitation either by choosing 'sweet-spot' transport times or by removing the excitation with a 'kick' voltage impulse. However, these approaches are of limited use for a scalable quantum processing node, as both require precise calibration of parameters such as a kick voltage amplitude, which might vary with the location of the transport and even drift with time.

Several control strategies have been proposed for robust control of transport induced excitation, such as optimal control [95] or invariant-based inverse engineering [96,97]. It has been shown in [98] that in the limit of infinite resources such as segment voltage range and bandwidth, the control strategies yield a straight-forward bang-bang type solution.

If we move the center of a harmonic potential well  $z_0$  pertaining to constant axial secular frequency  $\omega$  along the trap ( $z$ ) axis such that it follows the trajectory  $z_0(t)$ , the resulting displacement for a single ion of mass  $m$  after the transport of duration  $T$  can be calculated [94]

$$\alpha(T) = -e^{-i\omega T} \sqrt{\frac{m\omega}{2\hbar}} \int_0^T \dot{z}_0(t') e^{i\omega t'} dt'. \quad (5)$$

This means that the magnitude of the residual excitation is given by the Fourier component of the trap center's velocity at the trap frequency. As our architecture allows for performing probing and readout only at the LIZ, we characterize the residual axial excitation by means of a round-trip scheme: A single ion is cooled close to the ground state of its axial motion. It is then shuttled from the LIZ to a neighboring segment, where it is kept idle for a variable dwell time, after which it is shuttled back to the LIZ. There, the state of its axial motion is probed via the Rabi flopping method described in Sec. VII A. The employed voltage ramps are shown in Fig. 15 (a), and the measured axial excitation for different shuttling durations is shown in Fig. 15 (b). The voltage ramps are chosen such that a smooth acceleration and deceleration is ensured, minimizing the Fourier component of the well center's velocity  $\dot{z}_0$ , and to keep the axial secular frequency  $\omega \approx 2\pi \times 1.5\text{MHz}$  roughly constant. During the dwell time  $t_D$ , the oscillatory motion leads to accumulation of a phase  $t_D\omega$ , and the transport back to the LIZ leads to displacement of the same magnitude as the transport forth, but at reversed phase. The dwell time phase thus affects the magnitude of the final displacement, leading its oscillatory behavior with respect to  $t_D$ . The maximum excitation values therefore pertain to addition of the oscillatory excitation resulting from the back and forth transports, while the minimum values indicate a mismatch of these magnitudes: Because of filter-induced voltage waveform distortions, the voltage ramps for the two transport operations are not exactly symmetric, such that the excitation from the trans-

port back cannot exactly null the excitation from the transport forth.

The resulting values in the few-phonon range for transport durations of a few ten microseconds are tolerable, as all relevant laser-driven operations are only sensitive to transverse motion, see Sec. II. We probe the transverse excitation with the same scheme as described above, however we probe Rabi oscillation on sidebands pertaining to the lower- and higher-frequency transverse modes. The results are shown in Fig. 16. Residual transverse excitation can occur due to technical imperfections, i.e. if slightly different filtering characteristics on the dc lines pertaining to two adjacent dc segments lead to spurious transient transverse electric fields, if trap geometry imperfections lead to slightly tilted confining potentials. As can be seen, rather small residual excitations varying with the transverse secular period are observed on the lower-frequency transverse mode, while the residual excitation is consistent with zero -irrespective of the dwell time- on the higher-frequency transverse mode.

## C. Separation and merging

Ion crystal separation constitutes the transfer of two ions stored in one common axial potential well into two separate individual wells at distinct trap segments, and merging is the reverse process. These operations require the transform of a harmonic potential well into a double-well potential, which necessarily involves a transient situation where the ions experience a strongly reduced axial confinement, see Fig. 17. This makes it the most challenging shuttling operation, as the low confinement exposes the ions to increased heating and improperly controlled potentials. The process requires driving the ions through a quasi-singularity in terms of equilibrium distance versus time. As pointed out in [99], this makes it impossible to attaining adiabatic shuttling conditions and leads to finite axial excitation even at slow process times. Separation operations have been demonstrated and analyzed in more detail in Refs. [90,92,94].

The residual confinement at the critical point, where the harmonic confinement at the symmetry center of the axial electrostatic potential vanishes, is caused by the fact that the Coulomb repulsion pushes the ions away from it, where the anharmonicity of the emerging double-well leads to nonzero potential curvature. Therefore, small trap geometries with large anharmonicity parameters are beneficial for conducting such operations. For optimum excitation values, it is crucial to drive the ions slowly through the critical point, which in turn requires precise control over the harmonic confinement generated by the involved control electrodes. To that end, a precise calibration of the dependence of the axial secular frequency on the control voltages is obtained from resolved sideband spectroscopy. This way, tolerable axial excitations in the range of 1-10 phonons per ion and per operation are achieved. However, the spectroscopic calibration requires optical access to the site where the separation/merge operations take place, therefore these operations are so far restricted to



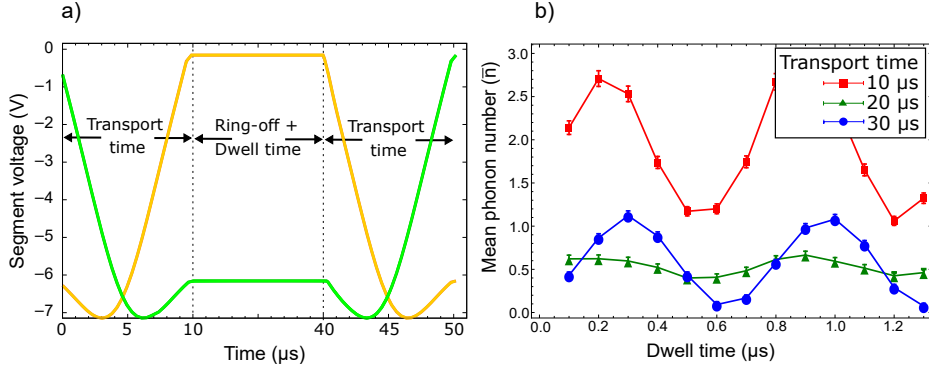


FIG. 15. Linear transport. **a)** shows the voltage ramps for shuttling an ion from the LIZ to a neighboring segment and back. The yellow (green) curve shows voltage applied to the initial (destination) electrodes during the transport time. The ion is kept at the destination segment for a ring-off time of  $30\mu\text{s}$  and a variable dwell time. **b)** shows the measured motional excitation on the axial mode resulting from this round-trip transport, versus the dwell time at the destination for multiple transport times. The coherent oscillatory nature of the excitation is revealed by the oscillations of the excitation with respect to the dwell time. It can be seen that excitations in the few-phonon range occur.

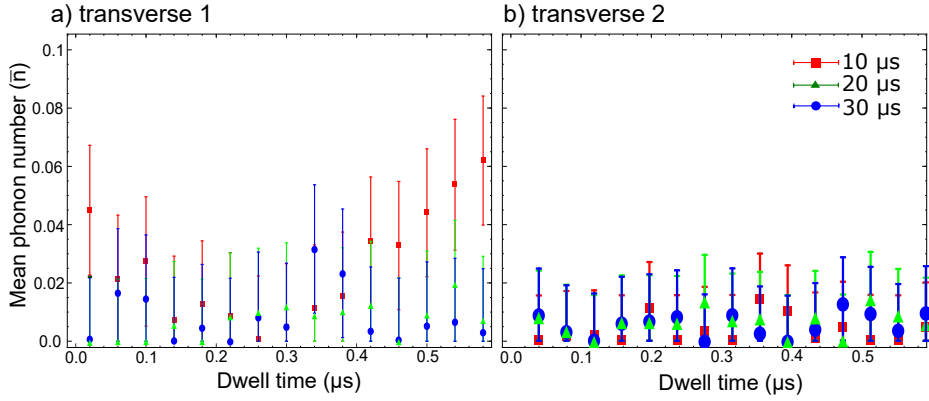


FIG. 16. Transport-induced transverse excitation. **a)** shows the excitation on the lower-frequency transverse mode after a round trip transport, and **b)** shows similar data for the higher-frequency transverse mode. Data for various single-trip transport times is shown for varying dwell times. Small transverse excitation only occurs on the lower-frequency transverse mode.

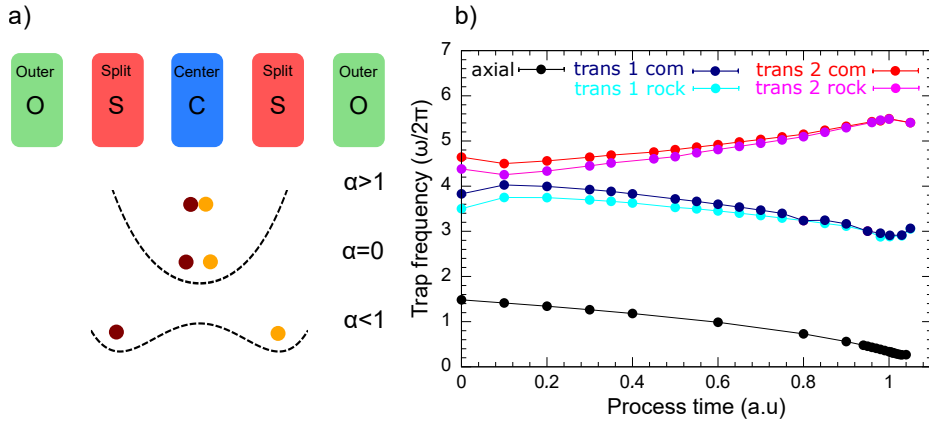


FIG. 17. **a)** shows a cartoon of the separation process, where a single harmonic axial potential well is transformed into a double well. The involved electrodes are the outer electrodes  $O$  serving for increasing the critical confinement, the split electrodes  $S$  generating the double well and the center electrode  $C$ , where the ions are stored initially. **b)** shows how the secular frequencies vary up to slightly beyond the critical point. The axial confinement decreases down to about  $2\pi \times 200\text{kHz}$ , while the transverse frequencies persist at values in the few-MHz range. It can also be seen how the transverse center-of-mass (com) and out-of-phase (rocking) modes become degenerate at the critical point, as the Coulomb coupling between the ions becomes weak at increasing distance.

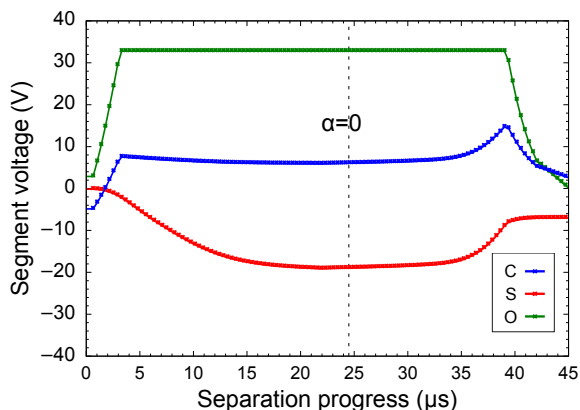


FIG. 18. Separation voltage ramps. The blue/red/green curves correspond to the voltages applied to the  $C/S/O$  segments. The first part consists of a rapid decrease of the harmonic confinement. The middle part, featuring rather slow variation of the voltages, corresponds to slow driving of the ion crystal through the critical point. In the final part, the separated ions are shuttled to the destination positions at the  $S$  electrodes, which basically corresponds to simple linear transport.

the LIZ. Suitable control voltage ramps are shown in Fig. 18

A detailed account on how to obtain voltage ramps for good separation/merge performance and a characterization of the resulting axial excitation can be found in<sup>90</sup>. In this work, we present more recent results from an improved apparatus and an additional characterization of the transverse excitation induced by this process.

The resulting axial excitation versus process time is displayed in Fig. 19(a). Strong excitation towards shorter process times can be observed, and for long times the excitation saturates due to the fact that the ions spend more time at low confinement and therefore are prone to increased anomalous heating. The more relevant parameter is the resulting transverse excitation, shown in Fig. 19(b), as it is affecting the entangling gate fidelities. For sufficiently long times beyond  $70\mu\text{s}$ , no significant excitation is observed on both transverse modes of the singled ions, i.e. the measured values are consistent with the baseline values after sideband cooling. For shorter times, also the transverse excitations show a strong increase, and the process is ultimately failing for times shorter than  $50\mu\text{s}$  due to ion loss. The presumed reason is that the voltage waveforms are distorted by the low-pass filters, see Sec. VB. Faster separation/merging can thus eventually be achieved by compensating the filter-induced distortions and/or increasing the filter cutoff while simultaneously improving the noise characteristics of the waveform generator.

As pointed out in<sup>90</sup>, separation/merge processes are extremely sensitive to uncompensated axial background forces, which can be of electrostatic or ponderomotive nature. A suitable axial compensation field can be generated by applying a differential voltage to the  $S$  or  $O$  segments, see Fig. 17(a). Its value is determined by determining the window of successful separation versus the differential ‘tilt’ voltage, and choosing the center of this window as the value yielding the best results.

In the context of multi-qubit operations, care has to be taken to not generate undesired background fields from additional wells storing spectator ions. Possible solutions for this are to either determine the tilt voltage for each separation/merge operation in the sequence, or to conduct these operations with spectator wells created at fixed positions. The tilt voltage also serves as a control parameter for separation/merging operations on larger ion crystals. In Ref.<sup>94</sup>, it has been demonstrated that  $M$  ions can be separated from an  $N$  ion crystal, in a controlled manner, via tuning of the tilt voltage.

#### D. Swapping

Physical rotation of ion crystals, termed ion swapping, enables reordering of the qubit arrangement along the trap axis. This has first been demonstrated in<sup>100</sup> and used in conjunction with quantum logic operations in<sup>89</sup>. The underlying mechanism is as follows: Upon increasing the axial secular frequency above the lower transverse one, a two-ion crystal will undergo a structural transition to vertical alignment, along the direction of the weaker transverse confinement. Transient application of a diagonal potential via the neighboring electrodes tilts the ion crystal before and after crossing the structural transition, and therefore turns this process into a controlled rotation. For identical qubit ions, the physical rotation is equivalent to a logical SWAP gate. Therefore, the capability to perform fast swap operations can improve the effective connectivity of our 1D architecture, which has a beneficial impact on the overall resource requirements for conducting a given quantum algorithm. Furthermore, swapping can mitigate the requirement of shuttling ions through trap junctions, and facilitate the operation of multi-species registers.

Unlike the linear transport and separation/merge operations, swapping necessarily involves motion along the transverse directions, and therefore leads to transverse excitation even in the ideal case without technical imperfections. However, in contrast to the separation/merge processes, it is possible to maintain high secular frequencies along all directions throughout the entire process, therefore it can be performed fast and at tolerable transverse excitations. The resulting coherent oscillatory excitation in the ideal case will predominantly affect the axial out-of-phase mode, originating from the centrifugal force, and the transverse out-of-phase mode pertaining the weaker confinement direction, originating directly from the rotation movement. We verify low motional excitation by performing a single rotation on a two-ion crystal, which is cooled close to the ground state on all six secular modes before the rotation. Determining mean phonon number from fitting Rabi oscillations is more complicated in the two-ion case, therefore the simplified scheme described in Sec. VII A 1 has been employed. The resulting values for the motional excitation on all six secular modes of a two-ion crystal after swapping are shown in Table III. These values pertain to a swap duration of  $18\mu\text{s}$ .

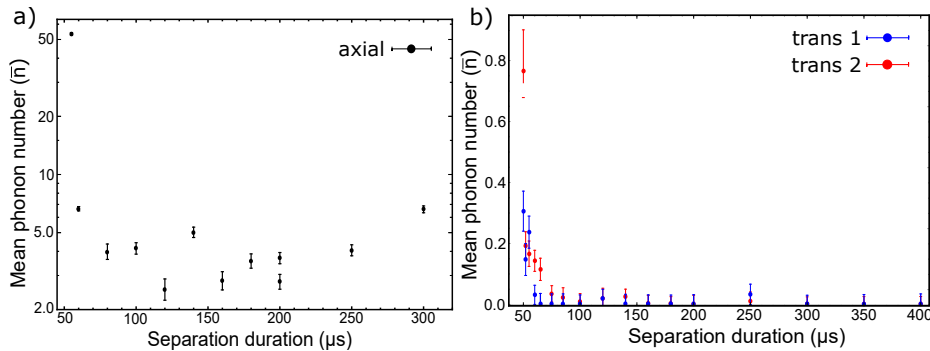


FIG. 19. Separation induced excitation: **a)** shows the mean axial excitation per ion in terms of mean phonon number after separation. It can be seen that excitations in the few-phonon regime cannot be avoided. **b)** shows the transverse excitations per ion in terms of mean phonon number after separation on both modes. For sufficiently slow separation, the separation-induced excitation drops below the residual thermal excitation after sideband cooling.

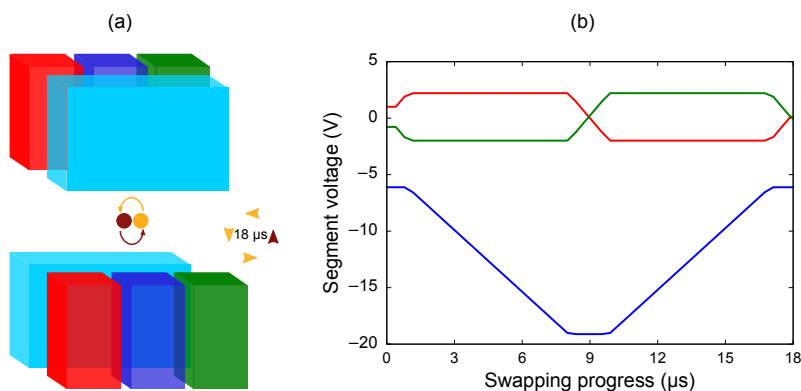


FIG. 20. Ion crystal rotation. **a)** shows the trap electrodes controlling the rotation process: The center segment (blue) providing the axial confinement, the electrodes generating the tilt field (red/green) and the rf electrodes providing transverse confinement (light blue). **b)** shows the applied voltage ramps: First, the tilt field is ramped up by applying voltages of opposite polarity to the tilt electrodes. Then, the axial confinement is increased by increasing the negative bias on the center segment. After crossing the structural transition to vertical alignment of the ion crystal, the polarity of the tilt is reversed, and the crystal is restored to horizontal alignment.

The arbitrary waveform generator described in Sec. IV allows for negative bias voltages of up to  $-40\text{V}$  at the center segment, therefore it is possible to conduct this process while maintaining high transverse secular frequencies in the few-MHz range. The fully independent control of all trap electrodes allows for swap operations at any trap site, and even for conducting multiple swap operations simultaneously. As all secular trap frequencies remain high during the process, a precise calibration as in the case of separate / merge operations is not required. Therefore, the process is not restricted to the LIZ. We have shown swapping of a two-ion crystal across the entire trap, the results are displayed in Fig. 21. Here, a two-ion crystal is separated, and the ions are consecutively moved to the LIZ, where ion 1 is prepared in  $|\uparrow\rangle$  and ion 2 in  $|\downarrow\rangle$ . The ions are merged again and jointly shuttled to a given destination segment. There, the swap operation is performed. Then, the crystal is again separated at the LIZ, and both ions are consecutively moved to the LIZ for spin readout. It can be seen that, within the given readout fidelity, the spin configuration is indeed reversed for all destination segments, if the

swap operation was actually carried out.

Based on these results, we also demonstrate simultaneous swapping: Here, a four-qubit register is prepared in the spin configuration  $|\downarrow_1\uparrow_2\downarrow_3\uparrow_4\rangle$ . The ions are then separated into two-ion crystals consisting of ions 1,2 and 3,4. These pairs are moved to distinct segments at a distance of at least three segments. Measurements with different reconfiguration operations are performed: Ion swapping is attempted either on crystal one, crystal two or simultaneously on both. For comparison, a measurement is also performed with no ion swapping. Then, in each case, the ion crystals are separated into individual ions, which are consecutively read out. The results are shown in Fig. 22a). It can again be seen that the spin configuration is deterministically permuted based on which swap operations are actually driven, with the fluctuations being consistent with readout errors.

We also show that reordering via crystal rotation can be extended to larger crystals. In Fig. 22b), we show results for rotation of a three-ion crystal. Similar to the protocols above, the crystal is initialized to the three different spin configura-

Secular mode	Secular frequency/ $2\pi$ (MHz)	<i>Lamb-Dicke</i> ( $\eta$ )	$\bar{n}$ after swapping	increase
axial:com	1.49	0.16(1)	0.36(2)	0.10(3)
axial:str	2.58	0.11(1)	0.28(2)	0.08(2)
trans1:com	3.81	0.06(1)	0.34(2)	0.01(3)
trans1:rocking	3.49	0.06(1)	0.37(2)	0.12(3)
trans2:com	4.63	0.065(3)	0.25(2)	0.04(2)
trans2:rocking	4.37	0.065(3)	0.23(2)	0.01(2)

TABLE III. Motional excitation in mean phonon number induced by a single rotation operation on a two-ion crystal. The values are obtained from averaging red sideband excitation with respect to probe time, see Sec. VII A 1

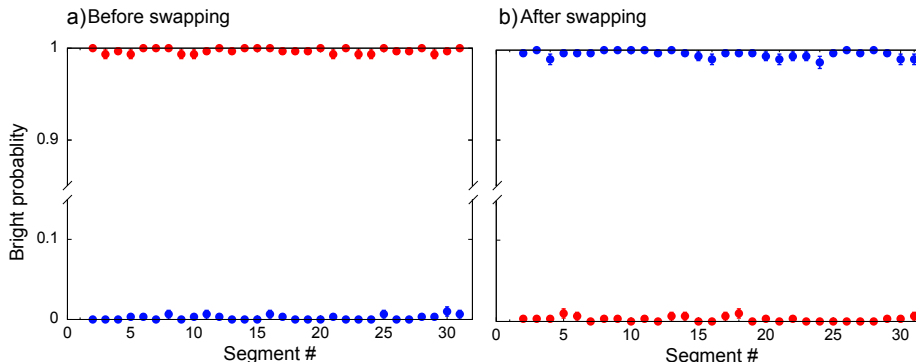


FIG. 21. Remote swapping: a swap operation on a two ion crystal is conducted at different segments, and is verified by measuring the spin configuration. Blue (red) dots correspond to the result for ion 1 (2). (a) shows the fluorescence result without swap, and (b) shows the fluorescence result with swap, where 'bright' ('dark') corresponds to  $|\downarrow\rangle(|\uparrow\rangle)$ . State preparation and measurement (SPAM) errors were characterized in [89] to be 0.4%.

tions  $|\downarrow_1\uparrow_2\uparrow_3\rangle$ ,  $|\uparrow_1\downarrow_2\uparrow_3\rangle$  or  $|\uparrow_1\uparrow_2\downarrow_3\rangle$ . The spin is read out in the original arrangement sequence, for the cases that the rotation is attempted or not. For the case with operation carried out, it can be seen that the spin population is predominantly in the expected state, i.e. the spin state of ions 1 and 3 is swapped. However, in this case the errors exceed the readout errors, presumably as increased transverse excitation deteriorates the spin readout fidelity. The three-ion rotation has been carried out using the same voltage ramps as for the two-ion rotation. Due to the increased axial extent of the three-ion crystal, the forces acting throughout the rotation are correspondingly increased. However, with a dedicated optimization of the ramps, it should be possible to carry out high-fidelity rotation operations on register building blocks comprised of three or more ions.

## VIII. OUTLOOK

In this review, we have given an overview of scalable trapped-ion quantum computer architectures based on shuttling operations. We have discussed the relevant technological components required to construct and operate such a node, in particular segmented microchip ion traps and fast multichannel arbitrary waveform generators. We have described the design, characterization and interplay of the relevant components and operations in detail, outlining how a fully functional few-qubit quantum processing node based on ion shuttling is

accomplished. In order to further boost the performance of such a platform, a number of well-defined technological and methodological building blocks is to be implemented. Most of these techniques have already been successfully demonstrated by different ion trapping groups, however mostly in a separate experiments.

Further improvements of the control hardware are required to allow for real-time conditional branching of computational sequences, based on the results of in-sequence measurements. A suitable execution control system will be able to conduct arbitrary branched sequences composed of shuttling and gate operations. Implementing such a system will make the node capable of autonomously performing a large number of error-correction cycles, rendering it to be fault tolerant. Other measures have to be implemented to improve the operational fidelities further, ranging from increased laser powers and composite pulse sequences to improve gate fidelities, to improvements of the qubit coherence times e.g by using hyperfine qubits, e.g.  $^{43}\text{Ca}^+$  [101], together with ultra-stable magnetic fields [50].

Adding at least one additional ion species will enable sympathetic cooling and selective readout of subsets of the qubit register. Both schemes are based on the fact that the auxiliary ion species allows for resonant driving with light which is far off-resonant to any relevant optical dipole transition of the qubit species. This has for example been successfully demonstrated by the groups at NIST, in Oxford and in Zurich [22, 102, 103]. However, adding an auxiliary species, which



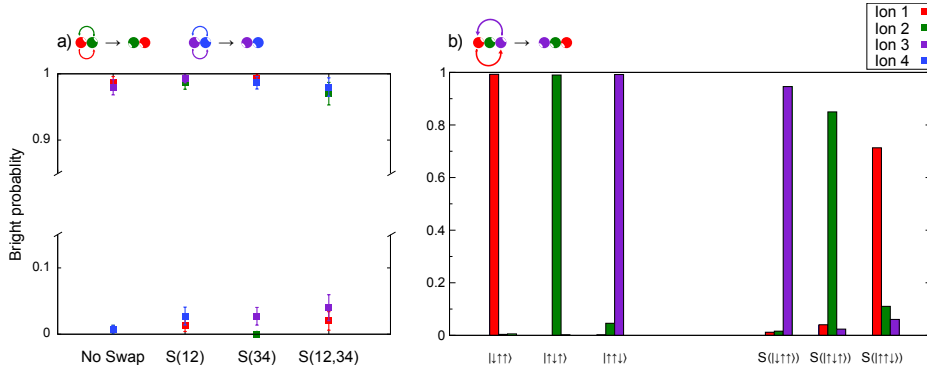


FIG. 22. Simultaneous three-ion crystal swapping:(a) shows the fluorescence results for no swapping, swapping of only ions 1,2, swapping of only ions 3,4 and swapping of 1,2 and 3,4 of a four ion register initialized to  $|\downarrow_1\uparrow_2\downarrow_3\uparrow_4\rangle$ . (b) shows the results for rotation of a three-ion crystal initialized in three different spin configurations.

was demonstrated in<sup>104</sup> will lead to an increase in controlling the shuttling operations.

Finally, to realize a scalable trapped-ion quantum computer capable of outperforming classical computers with useful tasks, requires an array of fully automated processing nodes, each consisting of one ion trap. Optical interfaces are a possible means for interconnecting the nodes within such an array, and could be based on free-space or cavity-enhanced coupling to optical radiation. Several research groups have realized free-space<sup>23,105,106</sup> optical interfaces, and work on cavity-based optical interfaces is ongoing<sup>33,107,108</sup>. Another approach could be to combine segmented linear traps with the extraction of single ions<sup>109</sup> from one trap and its injection<sup>110</sup> into a second ion trap. This scheme would be similar to a shuttling based approach<sup>36</sup>, however based on trap of modest complexity. In conclusion, shuttling-based trapped-ion QC has been shown to be a suitable approach to noisy intermediate-scale quantum computing. Methodological building blocks and the overall working principle have been demonstrated successfully, and further improvements based on existing technology could be accomplished in the foreseeable future.

While the steps outlined above and the integration into one platform are challenging, an optically connected network of 10 quantum processing nodes each bearing 10-100 trapped-ion qubits is within reach of today's technology. Such an apparatus could already allow for outperforming classical computing hardware on useful tasks such as computing molecular energy structures<sup>111</sup>.

As the operational timescales of such a platform will be dominated by the shuttling-induced overhead, which is in turn tied to the timescales imposed by the secular trap frequencies, such an architecture will not be competitive to e.g. superconducting platforms in terms of operational clock rate. However, the effective speed is also determined by the operation fidelities and the effective connectivity, moreover the performance advantage of a quantum computer is given by its intrinsic *quantum parallelism*. Therefore, it is promising to keep on pursuing the shuttling-based trapped-ion approach to scalable quantum computing.

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