Cronfa
Swansea University's Research Repository

Towards A Graphene Chip System For Blood Clotting Disease Diagnostics

Jacob John Mitchell

Submitted to Swansea University in fulfilment of the requirements for the Degree of Doctor of Philosophy in Nanotechnology.

Swansea University

24/02/2020

Towards A Graphene Chip System For Blood Clotting Disease Diagnostics © 2020 by Jacob J. Mitchell is licensed under a Creative Commons Attribution (CC BY) License.

Abstract

Point of care diagnostics (POCD) allows the rapid, accurate measurement of analytes near to a patient. This enables faster clinical decision making and can lead to earlier diagnosis and better patient monitoring and treatment. However, despite many prospective POCD devices being developed for a wide range of diseases this promised technology is yet to be translated to a clinical setting due to the lack of a cost-effective biosensing platform.

This thesis focuses on the development of a highly sensitive, low cost and scalable biosensor platform that combines graphene with semiconductor fabrication techniques to create graphene field-effect transistors biosensor. The key challenges of designing and fabricating a graphene-based biosensor are addressed. This work focuses on a specific platform for blood clotting disease diagnostics, but the platform has the capability of being applied to any disease with a detectable biomarker.

Multiple sensor designs were tested during this work that maximised sensor efficiency and costs for different applications. The multiplex design enabled different graphene channels on the same chip to be functionalised with unique chemistry. The Inverted MOSFET design was created, which allows for back gated measurements to be performed whilst keeping the graphene channel open for functionalisation. The Shared Source and Matrix design maximises the total number of sensing channels per chip, resulting in the most cost-effective fabrication approach for a graphene-based sensor (decreasing cost per channel from £9.72 to £4.11).

The challenge of integrating graphene into a semiconductor fabrication process is also addressed through the development of a novel vacuum transfer methodology that allows photoresist free transfer. The two main fabrication processes; graphene supplied on the wafer "Pre-Transfer" and graphene transferred after metallisation "Post-Transfer" were compared in terms of graphene channel resistance and graphene end quality (defect density and photoresist). The Post-Transfer process higher quality (less damage, residue and doping, confirmed by Raman spectroscopy).

Following sensor fabrication, the next stages of creating a sensor platform involve the passivation and packaging of the sensor chip. Different approaches using dielectric deposition approaches are compared for passivation. Molecular Vapour Deposition (MVD) deposited Al_2O_3 was shown to produce graphene channels with lower damage than unprocessed graphene, and also improves graphene doping bringing the Dirac point of the graphene close to 0 V. The packaging integration of microfluidics is investigated comparing traditional soft lithography approaches and the new 3D printed microfluidic approach. Specific microfluidic packaging for blood separation towards a blood sampling point of care sensor is examined to identify the laminar approach for lower blood cell count, as a method of pre-processing the blood sample before sensing.

To test the sensitivity of the Post-Transfer MVD passivated graphene sensor developed in this work, real-time IV measurements were performed to identify thrombin protein binding in real-time on the graphene surface. The sensor was functionalised using a thrombin specific aptamer solution and real-time IV measurements were performed on the functionalised graphene sensor with a range of biologically relevant protein concentrations. The resulting sensitivity of the graphene sensor was in the 1-100 pg/ml concentration range, producing a resistance change of 0.2% per pg/ml. Specificity was confirmed using a non-thrombin specific aptamer as the negative control. These results indicate that the graphene sensor platform developed in this thesis has the potential as a highly sensitive POCD. The processes developed here can be used to develop graphene sensors for multiple biomarkers in the future.

Declaration

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

Signed ... [redacted] ..... (candidate)

Date .....27/9/19.....

Statement 1

This thesis is the result of my own investigations, except where otherwise stated. Where correction services have been used, the extent and nature of the correction is clearly marked in a footnote(s).

Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

Signed ..... [redacted] ..... (candidate)

Date .....27/9/19.....

Statement 2

I hereby give consent for my thesis, if accepted, to be available for photocopying and for inter-library loans after expiry of a bar on access approved by the University.

Signed ..... [redacted] ..... (candidate)

Date .....27/9/19.....

Acknowledgements

During the past four years I have had a great deal of support and help from many people. I am sure that everyone of you will be as relieved as I am that I have finally finished writing up my thesis.

First I would like to thank Prof. Owen Guy for his continuous guidance, support, and patience throughout my research and writing of this thesis.

I would also like to thank all my academic colleagues Ryan, Anitha, Greg, Ehsaneh, Zari, Ffion, Hina, Olivia, Mo, Gareth, Jon and all the new members of our group and everyone else in Swansea, who have helped and advised me. All of whom have offered me encouragement, not only with writing this thesis but during my time at Swansea.

Sincere and Grateful thanks to my Mum, my Dad and my Nana, who have encouraged me, have been there for and me and given me endless support, both financial and moral, throughout my life and especially during past 4 years. Thank you.

A big thank you to all my friends who have supported me. Shout out to the D&D crew!

A very special thanks to my partner Cerys, who has helped and supported me, both at University, during my research, and also at home checking my thesis. She has kept me on track, whilst looking after me and our dogs and everything else! Her patience and advise has been truly invaluable. Without her I could not have done this... Especially not on time. Cerys Je t'aime.

Finally, Holly & Tasha. Who have been great conversationalists, keeping me company during the months of writing at home. And making sure I left the house for walkies.

Hec: Pretty majestical, aye?

Ricky Baker: I don't think that's a word.

Contents

List of Conferences & Publications

Conference BiosenseDementia 2017, Plymouth UK - Poster Presentation

Conference Graphene 2018, Dresden Germany - Poster Presentation

Conference Nanomaterials - Allied Academics 2018, London UK - Presentation Talk

Conference ISSC-22 2019, Swansea UK - Poster Presentation

Publication 2D Materials, Real-time detection of hepatitis B surface antigen using a hybrid graphene-gold nanoparticle biosensor.
https://doi.org/10.1088/2053-1583/ab734cu

Provisional Application for Patent NOVEL METHOD OF TRANSFERRING THIN FILMS TO ARBITRARY SUBSTRATES

List of Figures

List of Tables

List of Abbreviations

2D Two Dimensional

3D Three Dimensional

ABS Acrylonitrile Butadiene Styrene

AFM Atomic Force Microscopy

ALD Atomic Layer Deposition

Alumina Aluminium Oxide

Ambient Chips Graphene Dip Chips stored in ambient cleanroom conditions

APTES (3-Aminopropyl)triethoxysilane

aPTT activated Partial Thromboplastin Time

Bi-Layer A two layer photoresist system for lift-off processes

BNC Bayonet Neill-Concelman

BNP Brain Natriuretic Peptide

BOE Buffered Oxide Etch

BP Base Pair

CAD Computer Aided Design

CMOS Complimentary Metal-Oxide-Semiconductor

CNH Centre for NanoHealth

CNTs Carbon Nano Tubes

COC Cyclic Olefin Copolymer

CV Cyclic Voltammetry

CVD Chemical Vapour Deposition

D&D Dungeons and Dragons

DAN DiAminoNaphalene

Di Deionised

Dip Chip Inverted MOSFET Modified design of the Dip Chip with buried metal gate

Dip Chip Matrix Modified design of the Dip Chip with shared source and drain

electrodes, graphene channels increase to 9

Dip Chip Multiplex (Dip Chip M) Modified design of the Dip Chip with additional space between each

Dip Chip Shared Source Design Modified design of the Dip Chip with single shared source electrode, graphene channels increase to 5

Dip Chip (A design name for a chip that can be partially submerged in solution)

DNA Deoxyribonucleic Acid

DPV Differential Pulse Voltammetry

DQ Diazoquinones

DRAM Direct Random Access Memory

DTM Direct Transconductance Method

EDC/NHS 1-ethyl-3-3(3-dimethylaminopropyl)carbodiimide/N-hydroxysuccinimide

EDL Electric Double Layer

EDX Energy-dispersive X-Ray Spectrometer

FDM Fused Deposition Modelling

FET Field Effect Transistor

G-FET Graphene (based) Field Effect Transistor

GRC Graphene Resistor Chip

hBN hexagonal Boron Nitride

hCG Human Chorionic Gonadotropin protein

HOPG Highly Ordered Pyrolytic Graphite

i3DP Inkjet 3D Printing

ICP Inductively Coupled Plasma etching

ICs Integrated Circuits

IPA Propan-2-ol

IV Current Voltage

LDW Laser Direct Writing

LG-FET Liquid Gated Field Effect Transistor

LOR Lift-Off Resist

LPCVD Low Pressure Chemical Vapour Deposition

LT Nitride Low Temperature deposited silicon Nitride

mi-RNA micro Ribonucleic Acid

MI Myocardial Infarction

MJM Multi-Jet Modelling

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MVD Molecular Vapour Deposition

Nitride Silicon Nitride

NMP N-Methyl-2-pyrrolidone

Oxide Silicon Dioxide

PBS Phosphate Buffered Saline

PCB Printed Circuit Board

pDAN Polymerised Diaminonaphalene

PDMS Polydimethylsiloxane

PE Pulmonary Embolism

PECVD Plasma Enhanced Chemical Vapour Deposition

PEG Polyethylene Glycol

PFF Pinched Flow Fractionation

PIB Polyisobutylene

PMMA Poly Methyl Methscrylate

POCD Point of Care Diagnostics

Post-Transfer The majority of device is fabrication on base substrate occurs before CVD graphene transfer

PPP Platelet Poor Plasma

PR Photoresist

Pre-Transfer CVD graphene transferred onto base substrate prior to device fabrication

PT-MVD Post-Transfer process fabricated, Molecular Vapour Deposition passivated

PT-SPI Pre-Transfer process fabricated, Screen Printed Ink passivated

PT Prothrombin Time

PVA PolyVinyl Acetate

PVD Physical Vapour Deposition

RBC Platelet Rich Plasma

RBC Red Blood Cells

RIE Reactive Ion Etching

RNA Ribonucleic Acid

RSD Relative Standard Deviation

RTA Rapid Thermal Annealing

SC Solvent Cleaned

SD Secure Digital

SEM Scanning Electron Microscope

SLA Stereolithography

SMU Source Measurement Unit

SPE Screen Printed Electrode

ssDNA single stranded Deoxyribonucleic Acid

SWV Square Wave Voltammetry

TFA Tube Furnace Annealing

TMA TriMethylAluminium

TMAH TetraMethylAmmonium Hydroxide

TSP Test Script Processor

TSVVs Through Silicon Vacuum Vias

UV Ultra Violet

Vacuum Chips Graphene Dip Chips stored in vacuum desiccator

VDTs Vacuum Dicing Tracks

W/W Weight per Weight solution

WBC White Blood Cells

WCPC Welsh Centre for Printing and Coating

XPS X-ray Photoelectron Spectroscopy

ZF Zweifach-Fung

Chapter 1

Introduction

1.1 Background & Motivation

Point of care diagnostics (POCD) requires rapid detection of an analyte in close proximity of the patient. These analytes require quantification in some form for example their presence alone, a specific concentration range or the precise ratio of multiple biomarkers that are required to confirm a diagnosis. POCD can also aid in disease monitoring and long-term management and therapy. POCD is seen to be an area of growth and vital importance to the health care industry with a global value of $38.13 billion by 2022 rising from $23.71 billion in 2017 [1].

The biosensor is the most important component of the POCD as this supplies the high sensitivity required for analyte detection. Multiple new platforms are being developed for POCD using label-free biosensor platforms such as electrochemical, electrical, fluorescent and plasmon resonance systems [2]. These systems are also integrated with complementary technologies such as microfluidics and lab-on-a-chip to enable handheld/portable systems that can be delivered out of the lab environment.

Graphene is an ideal material to form the active surface for a biosensor platform due to its 2D structure, giving a large surface area to volume ratio and providing a surface for bio-receptors and signal enhancing molecules. Graphene also has unique electrical, physical and optical properties, such as its high carrier mobility. Graphene and carbon products have been researched and integrated into a diverse range of sensing platforms.

Out of the graphene sensing platforms, a G-FET sensor "Graphene-based field-effect transistor" was chosen for its high sensitivity and simple electronic measurement systems. G-FETs sense by monitoring surface modification by measuring

changes in transconductance. Any material that comes in contact with the graphene surface will effectively P-type or N-type dope the graphene [3]. This change in doping shifts the charge neutrality point (Dirac point) of the graphene. With a graphene channel-based sensor, this shift in Dirac point alters the conductance of the channel which can be measured using a two-terminal resistance measurement.

A G-FET sensor was chosen to be developed into a biosensor platform because it can be adapted for multiple disease diagnostics, providing the disease has a well-defined biomarker. Graphene has been shown as a highly sensitive and capable of detecting biomarkers that vary in physical size and nature, depending on the disease this can range from full cells to proteins and DNA and even single ions [4].

Blood clotting-based disorders are a large group of diseases which include cardiovascular disease (myocardial infarction and stroke), genetic disorders and acquired disorders from other medical conditions such as Cancer, Obesity, trauma, etc. Zion market research recently published a report stating the haemostasis diagnostic market would be valued on its own at $7.3 billion by 2024 [5]. Blood-clotting diagnostics was therefore the ideal target platform to test the G-FET sensor.

1.2 Aims & Objectives

The overall aim of this work is to develop a graphene biosensor platform that can be used for real-time studies of blood clotting biomarker detection. To achieve this aim key objectives were set out in this work across design, fabrication and testing phases of the devices.

Objective 1. Optimisation of the chip design. To allow for graphene submersion during functionalisation and sensing. Including connections to the sensor chip optimisation for repeatable measurements whilst taking the chip out of a probe station environment for liquid and chemical testing. Additionally design optimisation to reduce potential cost of graphene sensor the layout and fabrication flow, to maximise the number of sensing channels per chip with the lowest number of fabrication steps / lowest fabrication costs.

Objective 2. Fabrication optimisation. To reduce the total resistance of the graphene channel without applying additional strain or doping to graphene prior to functionalisation and sensing. As any doping of the graphene channel can effect the sensitivity of the graphene channel to the biomarker of interest. Fabrication materials such as contact metallisation and photoresist / cleaning chemicals were trialled and optimised based on best practices from literature around G-FET fabrication.

Objective 3. Packaging Optimisation. To develop an effective passivation solution for protection of the metal electrodes from the functionalisation and sensing solutions. Including development of fabrication process to protect the metal electrodes whilst keeping the graphene channel exposed. Additionally, development of a microfluidic package for the future translation of this technology to a point of care biosensor which can perform on chip sample preparation (blood fractionation) ready for the sensing step.

Objective 4. Device Testing. Electrical characterisation of G-FET performance and response of the graphene resistivity to aqueous environments. This needed to be established to isolate the response of the target biomarker during sensing. And functionalisation of the graphene surface to perform electrical measurements

in aqueous environments to determine the background noise an graphene response. G-FET sensor testing using the target biomarker to characterise the sensitivity and specificity of the device.

1.3 Thesis Outline

Chapter 2 Gives a general overview of the current literature surrounding graphene, graphene sensors, fabrication techniques, blood clotting diagnostics and microfluidic pre-processing.

Chapter 3 Covers the main equipment, materials and processes used throughout this work.

Chapter 4 Describes the optimisation of the chip design, comparing multiple designs for different potential applications. This includes a novel G-FET layout that allows the use of a microSD card connector to make direct connection the G-FET chip. This enables quick connection to G-FET chip and allows the chip to be submerged in solution during the electrical measurements.

These include a multiplex sensor design to allow for multiple chemical modifications on a single chip, a proof of concept design for gated field-effect measurements that can be performed using individual buried metal gates. This buried gate design employs an innovative fabrication process using metal filled vias through the dielectric layer. Another design was created through cost analyses of processing steps to produce the lowest cost graphene channel sensor. This chapter also gives detailed process flows for the main fabrication steps and cost analyses of each process flow.

This work also looks at the optimisation of the graphene sensor fabrication process. The development of a novel graphene transfer process which removes the use of polymer support layer, therefore eliminating polymer residues that result from the wet transfer process. Each process step for sensor fabrication was investigated, substrate, photoresist, metal, annealing and the stage of graphene integration. After fabrication of the functional graphene resistor. This microSD card connector is a step toward a handheld system and was implemented to improve the speed of data acquisition and provide a test setup for in-liquid measurements.

Chapter 5 Details the next stages of sensor development, this involved the passivation of the metal electrodes to aid with functionalisation and future sensor testing. Multiple materials including polymers and dielectric layers were developed and compared to find the optimum material. The development of a novel application for molecular vapour deposition technology as a graphene passivation process. This technique could be applied to any G-FET type system due to the nature of the Al_2O_3 deposition environment.

With successful passivation, the packaging of the sensor was then developed, integrating microfluidic channels onto the graphene sensor to achieve reliable functionalisation of individual channels. Multiple materials were tested including An innovative use of 3D printing technology directly onto a graphene based sensor to implement create a microfluidic cartridge for functionalisation and testing of the sensor. This technique was used to produce the first microfluidic multiplex functionalisation process used for a graphene based sensor. For a blood clotting biosensor platform all key biomarkers are found in the circulating blood. Microfluidics was investigated for sample pre-processing; a blood separation system was developed to isolate a blood plasma sample from whole blood. As plasma is the standard sample preparation used for blood sample detection assays.

Chapter 6 Investigates the sensor performance and was then tested in a real-time measurement setup. The device's response to ambient conditions and different liquid environments were investigated, these measurements established the sensors baseline response. Testing of a G-FET sensor in a submerged aqueous environment has not previously been achieved for extended time periods as performed in these experiments. The sensor was then tested against a range of protein concentrations from pg/ml to μg/ml. The sensor produced a linear response to protein concentration compared to a negative control which did not respond to the protein concentrations.

Chapter 7 Summarises the main findings of this work and looking forward at the potential for future research projects based on this work.

Bibliography

[1] Samiksha Nayak, Nicole R Blumenfeld, Tassaneewan Laksanasopin, and Samuel K Sia. Point-of-care diagnostics: Recent developments in a connected age. *Analytical chemistry*, 89(1):102–123, 2016.

[2] Sandeep Kumar Vashist, Peter B Luppa, Leslie Y Yeo, Aydogan Ozcan, and John HT Luong. Emerging technologies for next-generation point-of-care testing. *Trends in biotechnology*, 33(11):692–705, 2015.

[3] Jinglei Ping, Ramya Vishnubhotla, Amey Vrudhula, and AT Charlie Johnson. Scalable production of high-sensitivity, label-free dna biosensors based on back-gated graphene field effect transistors. *ACS nano*, 10(9):8700–8704, 2016.

[4] Janire Peña-Bahamonde, Hang N Nguyen, Sofia K Fanourakis, and Debora F Rodrigues. Recent advances in graphene-based biosensor technology with applications in life sciences. *Journal of nanobiotechnology*, 16(1):75, 2018.

[5] Marcus D Lancé. A general review of major global coagulation assays: thrombelastography, thrombin generation test and clot waveform analysis. *Thrombosis journal*, 13(1):1, 2015.

Chapter 2

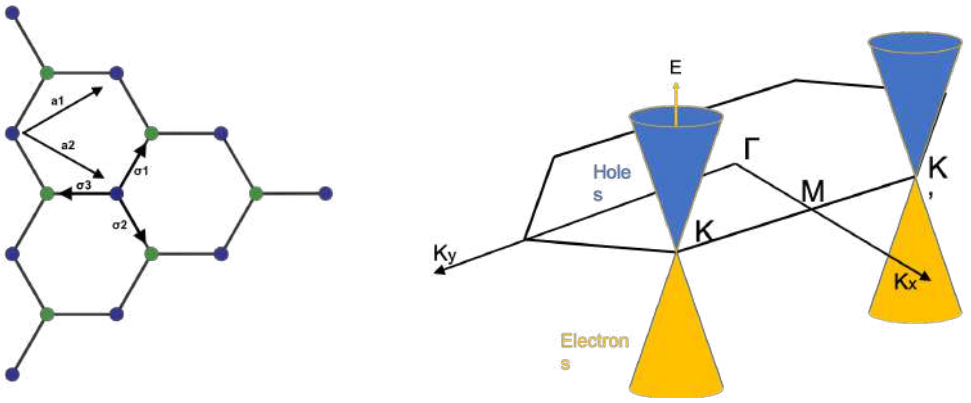
Literature Review

2.1 A Brief Introduction To Graphene

Graphene is an allotrope of carbon. It consists of a single layer of atoms organised in a hexagonal lattice. This honeycomb structure is the basic building block for other carbon allotropes such as a 3D stack which forms graphite, the rolled-up form carbon nanotubes (CNTs) and the wrapped up form fullerenes [1] [2].

In 2004 the first graphene sheet was isolated using the micro-mechanical cleavage method, it was also observed that it has probably been isolated every-time someone writes with a pencil [3] [4]. Graphene is optically transparent but has unique optical properties which means that it can be seen when prepared on silicon wafer substrates with a specific thicknesses of SiO_2 (90 and 280-291 nm) [5] [6]. It has also been observed that graphene produces a strong Raman response due to its unique geometric structure. This Raman signature enables the distinction between monolayer, bi-layer and many-layer graphene [7].

Graphene's geometric structure is based on each carbon atom being bonded to a further three carbon atoms in a single plane lattice. Figure 2.1 shows the graphene crystal structure containing the triangular Bravais lattice and the Brillouin zone reciprocal lattice. The electronic properties of graphene are a result of the SP^2 hybridisation between one s orbital and two p orbitals, these orbital structure results in the triangular planar structure of carbon-carbon σ bonds and a half-filled π bond. Due to this SP^2 hybridised bonding structure graphene has both remarkable thermal and mechanical properties [4].



(a) (b)

Figure 2.1: (a) The honeycomb lattice structure of graphene with two coloured sub-lattices, a1 and a2 are the lattice unit vectors, and sigma i=1,2,3 are the nearest-neighbour vectors. (b) Reciprocal view showing Brillouin zone (a particular choice of the unit cell of the reciprocal lattice) of the graphene with representatives of the Dirac points near the K and K' points.

The electronic band theory of solids describes the quantum states that electrons can occupy inside a solid. The energy states an electron may occupy are called energy bands. The energy states forbidden to the electron represent the band gap. When two atomic electron orbitals overlap, they both split into two energy quantum states relating to the radial distance between the two atoms. The lower energy orbitals are the bonding orbitals. Higher energy unoccupied orbitals are called anti-bonding orbitals. Figure 2.2 shows the orbitals of a single atom and the formation of band structure when bonding is extended to multiple atoms. This example uses the element Sodium (Na) a conducting material with a valence band is only partially filled with discrete energy levels for electrons. The collection of Na atoms have a band structure with discrete energy levels.

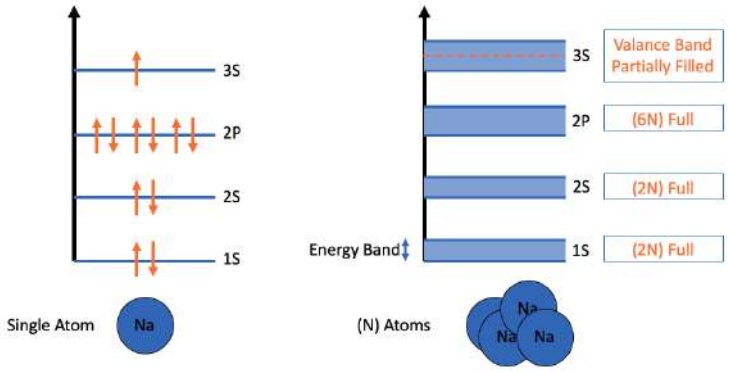


Figure 2.2: Band theory of solids, discrete energy levels of electrons in a single atom become a band in solids.

The electronic band dispersion of graphene was calculated in 1947 long before graphene's isolation [8]. Due to graphene's unique structure, its conduction and valence band intersect making it a zero bandgap material. Figure 2.3 shows the standard bandgap structure of normal conductors, insulators, semiconductors and graphene.

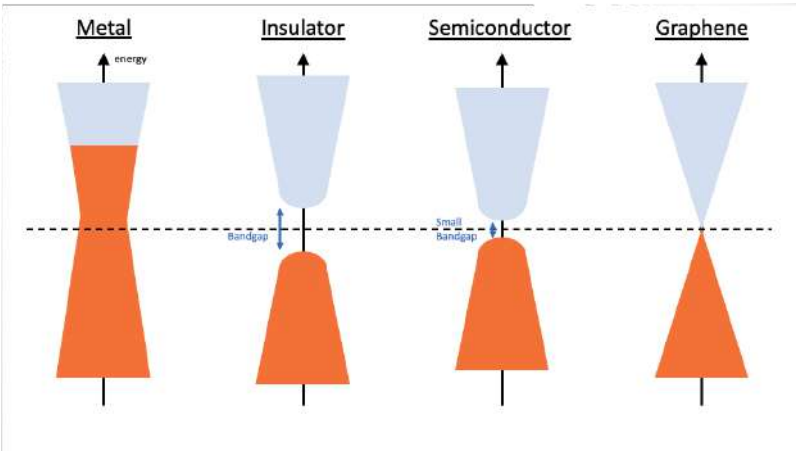


Figure 2.3: Valence and conduction bands of metals, insulators, semiconductors and graphene. The Fermi level is the name given to the highest energy occupied electron orbital at absolute zero (0 K).

In hypothetical perfect conditions, without other material interactions on the

graphene sheet, graphene has equal carrier concentrations of both electrons and holes. Depending on the Fermi energy with respect to the Dirac point, either holes or electrons can be the majority charge carriers. Figure 2.4 shows the effect of hole (P-type) doping and electron (N-type) doping moving the Fermi level with respect to the Dirac point.

This shifting in Fermi level (doping shift), is used in electrical G-FET sensing, as the doping shift results in a change in current through a graphene channel. This change in current is calculated as a change in resistance which is used for quantifying the sensing result [9].

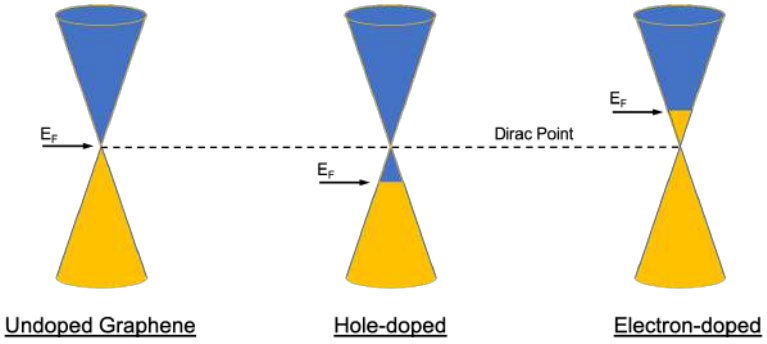


Figure 2.4: Representation of the electronic band linear dispersion in graphene (Dirac Cone). Electron transfer from the graphene causes P-type (Hole) doping, Electron transfer to the graphene causes N-type (electron) doping. Doping displaces the Fermi level above or below the Dirac point. Figure adapted from [9]

Graphene when transferred onto a supporting substrate forms folds/ripples and other defects that mean a perfect planar structure is not maintained. These folds, as well as interactions with the base substrate, induce the formation of charge puddles. These are regions of enriched electrons or holes on the substrate graphene interface, in the case of oxides the oxygen rich open-shell/dangling bond defects strongly hole-dope the graphene sheet [10].

Graphene as a 0 bandgap semiconductor can be used for high-speed analogue electronics and has uses in transparent conductive films, but is not suitable for logic applications, where a complete switch-off of the G-FET would be required. This zero

bandgap originates from the identical carbon lattice structure, to introduce a large enough bandgap for graphene to be used in semiconductor applications this planar symmetry would need to be disrupted. Atom substitutions in the graphene lattice as well as the use of crystal substrates with lattice mismatch have been suggested for bandgap opening [11] [12].

When a contact between a metal and a semiconductor is created there are two main types of electrical junction that can form:
1) An ohmic contact, an ohmic contact (a system that follows Ohms law), is a contact commonly between metal and semiconductor or metal and metal that has a linear current–voltage (IV) curve. This can be obtained by choosing metals (M) with specific work functions relative to the work function of the semiconductor (S). Such as ϕM $<$ ϕS for metal to n-type semiconductor junctions or metals with high work functions so that ϕM $>$ ϕS for metal to p-type semiconductor junctions.

Alternatively if the semiconductor surface is heavily doped near the contact to make the potential barrier incredibly small so that efficient quantum-mechanical tunnelling can take place.
2) A Schottky diode, where a potential energy barrier is formed at a metal–semiconductor interface. If the barrier is high enough that a depletion region forms in the semiconductor. This allows the formation of rectifying Schottky barrier which can allow the flow of electrons only in one direction. These junctions are formed with low levels of semiconductor doping.

When fabricating metal-graphene contacts the standard metal-metal or metal-semiconductor theory no longer applies. This is because graphene is a 0 bandgap material (No bandgap semiconductor) and that the density of states for graphene dissipates at the Dirac point Figure 2.5 shows this process in an energy level diagram.

The fact that no energy gap forms also prevents the formation of depletion region and therefore the formation of a rectifying Schottky barrier. As graphene is a 2D material with large surface area to volume ratio it is highly sensitive to environment, its electrical properties can be altered when creating a the metal-

graphene contact. The work function of the metal used can cause a charge transfer through the interface, this can cause the graphene to become doped highly.

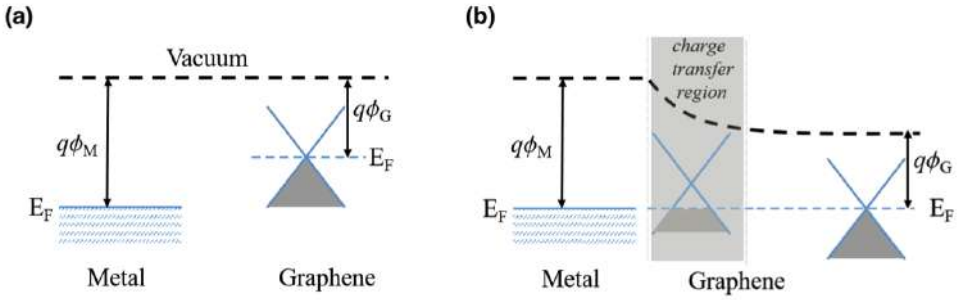


Figure 2.5: (a) Representation of separated metal and graphene (graphene with its Dirac cone). (b) A metal-graphene contact, at the interface the Fermi levels are aligned. Further away from from the metal-graphene contact the Dirac point of graphene approaches the Fermi energy. This figure was adapted from energy level diagram by Filippo Giubileoa and Antonio Di Bartolomeo [9].

The small density of states in graphene near the Dirac point can cause the Fermi level of the graphene to shift, even with a small transfer of charge. The energy shift of the Fermi level can be upwards electrons transferring from metal to graphene (n-type doping), or downwards when holes move from metal to graphene (p-type doping).

The work function difference of the metal used for contacts is just one factor to consider, it is not the only factor that can alter the doping of graphene. As previously mentioned graphene is incredibly reactive to its environment. Chemical interaction at the interface surface (metal physisorption or chemisorption) can substantially effect the doping. The incredible sensitivity of graphene to its environment and how these surface changes can modify its electrical behaviour are part of the reason this material has so many potential applications.

Graphene can also be deliberately doped to change the majority charge carriers. This can be done by applying an electric field to the graphene sheet (similar to a metal oxide capacitor system), or by introducing chemical dopants [13].

When applying a voltage using a conductive layer separated from the graphene by a thin insulator, the resulting electrical field modifies the electron density that can carry electrical current. When applying a negative potential, electrons are added to the system, N-type doping the graphene. When a positive potential is applied electrons are removed from the system, P-type doping the graphene [14].

Dopants can also be introduced into the lattice structure of the graphene, similar to semiconductor doping where impurities are introduced to form "extrinsic semiconductors". This form of doping is often introduced during the graphene growth process (gases introduced into the growth chamber). Introducing Nitrogen into the graphene results in N-type doping of the graphene [15], whilst introducing of Boron atoms into the lattice produce a P-type doping effect [16].

Graphene is quite stable due to its structure of interconnected σ-bonds and network of π orbitals that assist the carbon-carbon bond strength. Even so, graphene can be chemically modified using multiple processes post-graphene-growth. This involves vacancy filling using by deliberately introducing damage into the sheet and filling these "vacancies" with other atoms, in a similar process to doping during synthesis.

Edge defects occur in all graphene synthesis and graphene channel fabrication. depending on the orientation of the graphene sheet. Either "armchairs" or "zig-zag" edges (Figure 2.6) will be produced, most likely a combination of the two. The graphene structure at the edge produces dangling σ-bonds, these can develop radial groups forming covalent bonds with molecules in the environment, making the graphene edge relatively reactive compared to the planar graphene sheet [17].

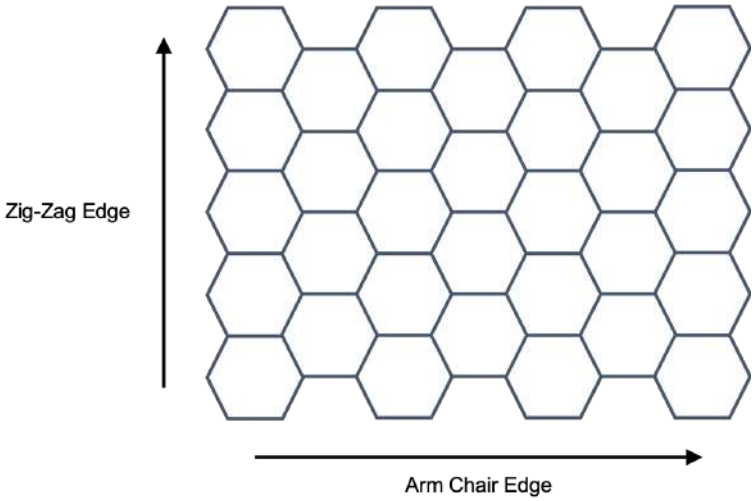


Figure 2.6: The two distinct edges of graphene depending on orientation of the lattice.

The most common method of graphene doping is chemical doping where molecules interact at the graphene surface, transferring or accepting electrons from the graphene sheet. This can involve gases such as NO_2 strong hole doping effect and NH_3 strong electron doping effect [18] [19], or organic molecules which π-π stack (non-covalent interactions with π-bonds in the graphene lattice) on the graphene surface and can hole or electron dope depending on the molecular structure (vanadyl phthalocyanine, 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane) [20]. These surface bonding doping interactions are the bases of graphene sensor chemical functionalisation and bio-receptor analyte interactions, that can be detected by monitoring the graphene's electrical properties.

2.2 Graphene Growth

There are three primary methods of synthesising graphene; exfoliation, epitaxial growth and chemical vapour deposition (CVD).

2.2.1 Graphene Exfoliation

The first isolation of graphene was performed by mechanical exfoliation [3]. This method involves micromechanical cleaving of graphene layers from bulk Highly Ordered Pyrolytic Graphite (HOPG). Minimal force is required to break the Van der Waals bonding between individual graphene sheets (2 eV/nm^2). Mechanical exfoliation can be achieved by a normal force, such as scotch tape method removing layers off the HOPG surface like in 2004 (approximately 300 nN of force per 1 μm^2 of graphite). Alternatively, using a shear force lathe-like process has also successfully produced graphene from HOPG [21].

Other methods for larger-scale production include the sonication of HOPG in a liquid-phase this is often accompanied by an electrochemical process, first oxidation of the the graphene layers using an applied potential connected to the HOPG. Sonication is then used to separate the graphene oxide sheets, followed by a chemical reduction to graphene [22]. A physical large scale approach is the use of ball-milling of graphite where a cylindrical container is rotated at 300 rpm containing 100 μm ZrO_2 ball bearings, these both cleave and fragment the graphite [23]. Both of these methods, although automated for large volume processing, suffer from the same small area flake size.

Exfoliation can produce high-quality crystal lattice graphene as small area graphene flakes. When large-area sheets are required. For whole wafer-scale fabrication of electrical graphene devices, exfoliated graphene is not a utilisable material.

2.2.2 Epitaxial Graphene

Epitaxial graphene is grown on silicon carbide (SiC) via a thermal decomposition process, first reported in 2004 [24]. The SiC wafer has two main crystal orientations a carbon facing (SiC000$\bar{1}$) and Si facing (SiC0001) orientation. The SiC0001 orientation is used for slower more controlled graphene growth. The process is performed at high temperature under vacuum (with argon flow) to avoid contamination. Due to carbon's low sublimation point compared to silicon, when SIC is heated at high

temperature (1650 °C) the Si atoms desorb leaving behind carbon atoms which can re-constitute into the hexagon sheet. This method was used to produce graphite-like layers and few-layered-graphene [25]. Approximately three bilayers of SIC desorb to produce a single graphene sheet.

Epitaxial graphene can be grown on large SiC wafer substrates (150 mm). Decreasing the Si evaporation rate resulted in lower levels of morphological change to the surface and larger graphene grain sizes 50 x 50 μm reported in 2013 [26]. The difficulty arises at surface steps on the SIC surface which can result in bi-layer or few-layer regions affecting the overall conductivity. For every 10 nm step height difference a resistance increase of 21 kΩ has been recorded [27].

More recently, larger grain sizes have been produced by controlling the nano step geometries on the SIC surface. Single grain graphene across full 2$''$ and even 100 mm wafers have been produced and are available commercially (Graphensic AB, Sweden). This graphene production method is of very high quality with large scale grain sizes for full wafer fabrication [28]. There are still issues regarding resistance variation across the surface (bi-layer patches), although this variability is being reduced with process optimisation. The main disadvantage of epitaxial graphene is processing costs. Starting with SiC wafers as the substrate material dramatically increases costs. As a comparison, using pricing from University Wafer Inc (USA). The unit price for 50.8 mm Silicon wafer with thermal SiO_2 surface (SiO_2, a standard graphene research substrate) is \$15.90 (£13.19), the unit price for a 50.8 mm 6H-SiC wafer is \$375.00 (£311.07). The SiC wafer is over 23 times more expensive as a starting substrate. The graphene growth process then adds further expense. The cost of a 50.8 mm epitaxial graphene wafer with monolayer graphene costs €6000 (£5358.34) (Graphensic AB, Sweden). In comparison, CVD grown graphene on a SiO_2/Si substrate costs €246 (£219.66) (Graphenea, Spain).

$Currency covetedusing XE.com (2019 - 09 - 03)$

2.2.3 Chemical Vapour Deposition Graphene

Chemical vapour deposition (CVD) is a method of depositing material from gaseous reactants onto a substrate in a reaction chamber. The substrate material is heated to achieve the desired chemical reaction. The chamber is pumped down to vacuum to reduce impurities. Reactant gas molecules CH_4/H_2 (in carrier gas Ar) combine and react to form graphene [29]. CVD graphene is grown in a two-step process. The first step is a precursor pyrolysis step, where carbon atoms are formed from the dissociated reactant gas at high temperature on the substrate to avoid clustering of the carbon atoms. Metal substrates are often used as catalysts to reduce the temperature required. The second step creates the graphene structure out of the dissociated carbon atoms, this step also requires high temperature and without a catalyst this would require a temperature of 2500 °C. Using a metal catalyst this temperature is reduced down to 1000 °C. Once cooled, the substrate is then removed from the growth chamber with the graphene film on the surface [30].

The problem with introducing a metal catalyst is the potential for contamination and the effect of reactions in the chamber. Metal single crystal substrates are used as CVD catalysts (and form the substrate) due to the metals closely packed hexagonal surface geometry which matches the graphene carbon geometry. The distance between the surface metal atoms also determines the arrangement of carbon atoms during the graphene structure step. Different metals and orientations have been researched. The most common metals that are used for growth and have weak interactions with the graphene include Cu, Ag, Ir, Pt, Pd and Au. Metals that are used for growth and have a strong interaction include Ni, Co, Ru, Rh, Re (strong interaction defined by separation distance above or below 0.3 nm) [31]. CVD growth results in multiple nucleation sites so different grain sizes are produced across the metal substrate. However, the advantage of CVD growth is the large scale of production available up to 30 inch Cu foil, m^2 growth has been demonstrated [32].

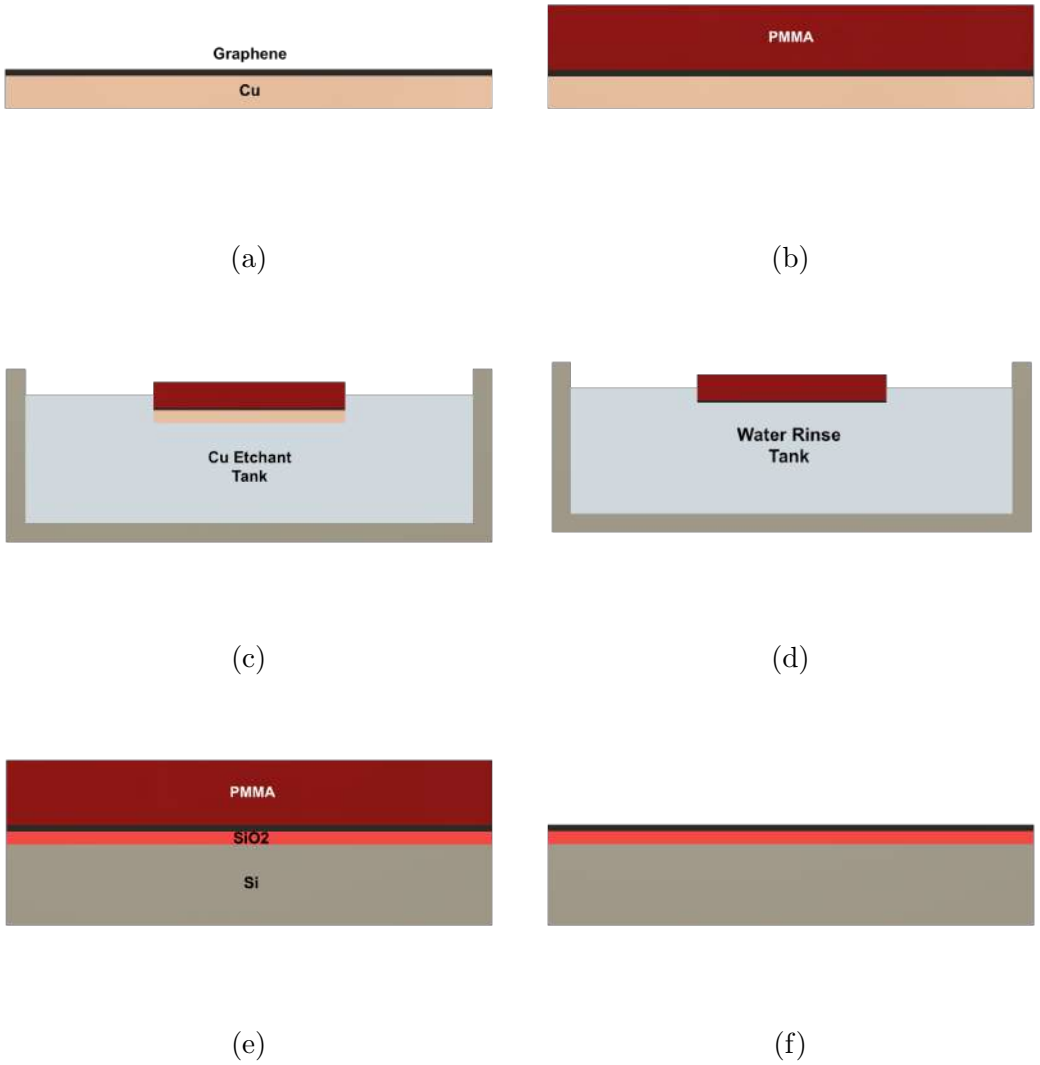
Among all the CVD growth substrates Cu and Ni foil is most common. It has an advantage in terms of material cost and its low carbon solubility, making etching

and transfer of graphene easy and relatively low-cost [33].

The process of CVD growth on metal foil substrates requires a transfer step for wafer fabrication. The common method is the use of a wet transfer method. Figure 2.7 outlines the main steps of this method. Metal foil is used as CVD catalyst with the etch solution determined by the metal used [34]. The wet transfer method is used in commercial fabrication and can produce a full 100 mm ($572) and 150 mm ($936) monolayer graphene on wafer substrates (Graphenea, Spain).

The wet transfer method using both Poly(methyl methacrylate) (PMMA) or alternative positive photoresists is the most common method of graphene transfer. Some issues include cracking of the graphene layer during the solvent cleaning stages where the graphene had not conformally made contact with the substrate. A secondary spin coating of PMMA on the transferred graphene PMMA was shown to improve transfer and reduce total breaks in the graphene sheet [35].

The primary issue with graphene transfer is the use of a polymer support layer. Acetone is primarily used as the cleaning agent for PMMA but inevitably there are residues left behind. PMMA residues post solvent clean have been shown to cause charged impurity scattering, changing the doping of the graphene sheet, and causing the carrier mobility to decrease [36] [37].



(a) (b)

(c) (d)

(e) (f)

Figure 2.7: (a) CVD monolayer graphene growth on Cu(111) foil. (b) Polymer (e.g. Poly methyl methacrylate) coated onto the graphene surface. (c) PMMA used as support material to float graphene on Cu foil in wet etch tank. (d) Cu foil etched away, followed by transferring to di H_2O rinse tanks to remove etchant residue. (e) Graphene and PMMA "Scooped" from solution using silicon wafer (SiO_2 coated), vacuum baking used to promote adhesion and remove graphene PMMA wrinkles. (f) Solvent cleaning steps used to remove PMMA from graphene surface.

2.2.4 Reducing Residue From CVD Graphene Transfer

The use of deep UV curing (20 mins 50 W 254 nm wavelength) of the PMMA layer prior to solvent cleaning has been shown to reduce residues and improve graphene's electrical performance [38]. Resist removal decreased the graphene channel's electrical resistance and reducing doping and increasing stability.

Alternative methods have been put forward to reduce residue from the graphene's surface, including using alternatives to PMMA/Photoresist. Polymer polyisobutylene (PIB) has also been used as part of the supporting layer, used as a release layer between the graphene and polydimethylsiloxane (PDMS). The removal solvent decane was then used post-transfer to remove the PIB layer, this process was shown to reduce total residue from the support layer [39].

A recent method shows some promise using a paraffin spin-coated as the support layer. The metal layer is etched as normal followed by transfer to a 40 °C water bath. The warm water bath enables the paraffin to remain in its solid-state but expands thermally and removes graphene wrinkles. In the expanded state, the floating paraffin-graphene is transferred to substrate silica and baked. The paraffin is removed (peeling) whilst at 40 °C leaving pristine graphene with lower levels of residue compared to PMMA. This method yielded decreased sheet resistance variability and increased carrier mobility by 2.6 times. The cause of this has been investigated and it is thought that the paraffin molecule has a lower likelihood of forming bonds with carbon radicals and graphene defects [40].

True "polymer-free" methods do not use a support structure during the transfer method so no polymer compounds come into contact with the graphene sheet. The primary difficulty of this process is promoting graphene substrate adhesion during the metal etch process. It was shown that hydrophilic substrates are likely to have an interface layer of the etchant solution between the graphene and the substrate, leading to delamination [41]. Using surface treatments to create a hydrophobic surface for transfer, polymer-free transfer was achieved using a frame to support the graphene edges during transfer. As the Cu foil was etched away, the graphene

made contact with the hydrophobic substrate beneath [42]. This process was limited to small substrate sizes and resulted in some breakage points as the Cu layer was etched.

Other polymer-free methods include a direct growth on the final substrate. Fe deposited directly onto a SiO_2 coated substrate was used to catalyse by CVD graphene growth on the Fe layer. Graphene channels were patterned and etched and metal contacts deposited onto the surface securing the graphene. HCl wet etching solution was then used to undercut etch the Fe layer under the graphene, producing suspended graphene channels. Atomic layer deposition of HfO_2 was then used to fill the recess [43]. However, the graphene channels suffered from delamination issues during the under etch process, resulting in low yields.

Additionally direct growth on dielectric substrates such as GaN, Ge and Si has been shown to be possible but these processes are still limited in terms of surface growth and graphene grain size [44].

2.3 Graphene Sensors

Graphene has been researched as a biosensor platform using multiple techniques due to its electrical, optical and physical properties being suitable for biosensing applications. Graphene biosensors range from purely electrical FET-based measurements, using the graphene as a conductive channel; to electrochemical sensors (using the graphene as an working electrode); optical processes such as surface-enhanced Raman spectroscopy (using the graphene as an enhancing substrate); optoelectronic sensors based on labelled receptor molecules and even force-based AFM imaging sensors using graphene bound receptors and tip bound analytes [45].

For a handheld, lab-on-a-chip style, point of care system, the simplest (and smallest packaged) diagnostic tool would be an electrical measurement platform [46]. There are four electrical-based sensor configurations; chemiresistive, back-gated FET, liquid-gated FET and capacitance FET. Electrochemical graphene platform, using the primary electrochemical configuration of the three-Electrode system is

also reviewed. Table 2.1 & Table 2.2 lists some of the current electric graphene FET (G-FET) reported for biosensor applications.

A G-FET biosensor stripped down to it essential components includes a support substrate, (insulating layer), graphene sheet and metal electrodes to make electrical connections. The step that makes it a specific biosensor is the bio-receptor molecule used on the graphene surface. These molecules are used to bind the analyte (biomarker) target when presented in bio-fluid tissue or breath samples (Figure 2.8).

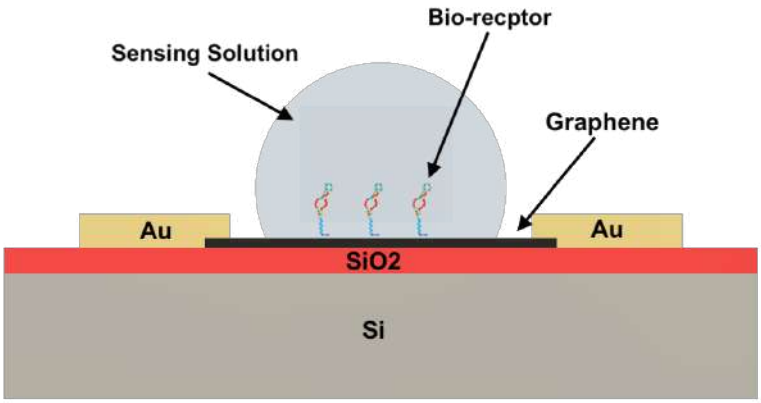


Figure 2.8: Basic components of a graphene biosensor.

Table 2.1: Table of graphene-based field effect transistor (G-FET) biosensors currently reported in the literature (Part I)

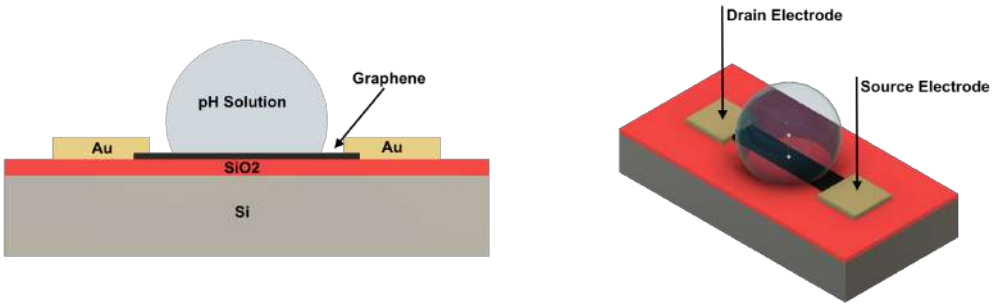
Type of Sensor	Bio-receptor	Application	Substrate	Sensitivity	Ref.
Chemiresistive	Antibody Human Chorionic Gonadotropin (hCG)	Pregnancy	Epitaxial on SiC Ti/Au contacts	16.7 pM	[47]
Chemiresistive	Antibody 8-hydroxydeoxyguanosine	Cancer	Epitaxial on SiC Ti/Au contacts	0.35 nM	[48]
Back-Gated FET	22 base pair (BP) DNA Aptamer	Proof of concept	CVD on SiO−2 Cr/Au contacts	100 pM	[49]
Back-Gated FET	DNA Aptamer Kanamycin A	Antibiotic detection	CVD on HfO_2 Ti/Pt contacts	11.5 pM	[50]

Table 2.2: Table of graphene-based field effect transistor (G-FET) biosensors currently reported in the literature (Part II)

Type of Sensor	Bio-receptor	Application	Substrate	Sensitivity	Ref.
Liquid-Gated FET	20 BP DNA Aptamer	Proof of concept	CVD on SiO_2 Ti/Au contacts	10 pM	[51]
Liquid-Gated FET	22 BO miRNA	Cancer	CVD on SiO_2 Cr/Au/Cr contacts	100 fM	[52]
Liquid-Gated FET	Antibody Carcinoembryonic	Cancer	CVD on SiO_2 Ti/Au contacts	0.5 pM	[53]
Capacitance FET	Antibody E. coli O157:H7	Bacterial detection	CVD on SiO_2 Au contacts	10 cells/ml	[54]
Capacitance FET	Antibody Zika Viral antigen (ZIKV)	Virus detection	CVD on SiO_2 Ti/Pt	450 pM	[55]

2.3.1 Chemiresistive Sensor

Chemiresistive sensors are based on a simple IV measurement performed across a graphene resistor [48]. IV measurements can be performed dry or in solution, when an analyte interacts with the graphene channel it produces a change in the IV (resistance/conductivity) characteristics of the graphene channel. Figure 2.9 shows a simple graphene resistor made up of core components substrate, insulator, graphene and metal contacts, this simple graphene resistor was used as a pH sensor, applying a constant 10 μA current and measuring voltage to calculate graphene channel resistance. The graphene channel resistance in the air was measured as 86 kΩ initially but displayed a dramatic drop to 56 kΩ on submersion in liquid (pH 4). A resistance change was then measured for each pH solution applied with a resistance change of approximately -3.48 kΩ/pH unit average from both acid and alkali pH direction [56].



(a) (b)

Figure 2.9: (a) Cross-section view of graphene pH resistor sensor. (b) 3D view showing resistance measurement setup for pH sensing.

Even though this method of sensing does not measure the charge neutrality point (Dirac Point, the resistance maxima where the charge carrier density is negligible), it was assumed that the graphene was hole-doped due to the substrate being SiO_2 and the graphene being annealed in air. As the resistance decreased with increasing pH. This suggests a hole doping shift with increasing pH, this result was backed up

by similar pH FET style graphene sensor measurements which confirmed the p-type doping shift of the Dirac point with increasing pH [57] [58]. Figure 2.10 shows a simplified Dirac point shift due to hole doping with pH increase.

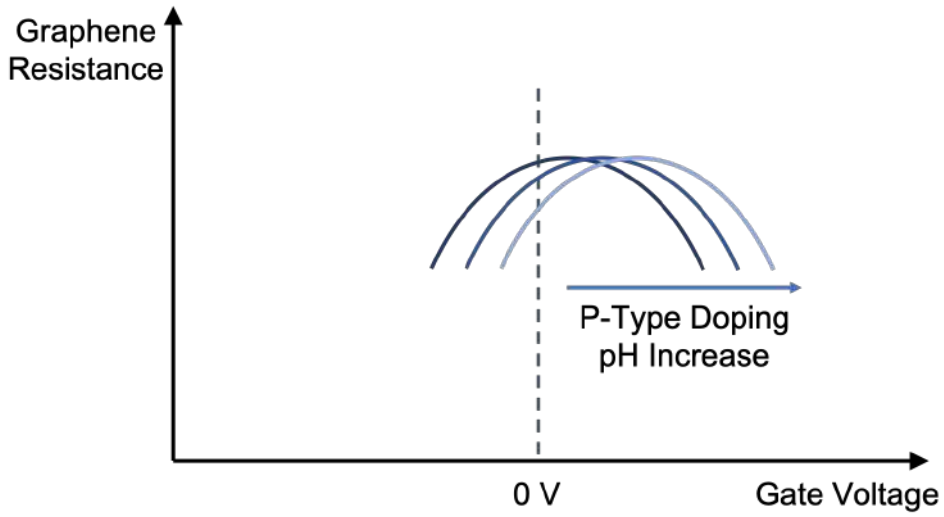


Figure 2.10: Illustration of decrease in resistance for resistor (0V) pH sensor. Hole doping shift with increasing pH. Adapted from ([56])

The mechanism for the change in resistance (Dirac point shift) due to water and pH change is still debated. It is commonly agreed that the water molecules and ionic molecules adsorb onto the graphene surface, causing changes in conductivity. It has been recently reported that capacitative charging [59], not surface transfer doping [60], is the cause of the doping shift seen in graphene electrical sensors. Figure 2.11 shows the capacitative model, the adsorption of OH^- and H_3O^+ ions on the graphene surface forming an electric double layer (EDL). Due to the charging effect of the EDL, the capacitance changes the carrier concentration of the graphene and is responsible for the change in doping. This model was confirmed using a back gated graphene FET measurement which removes the potential charge effects of the liquid gating electrode [61].

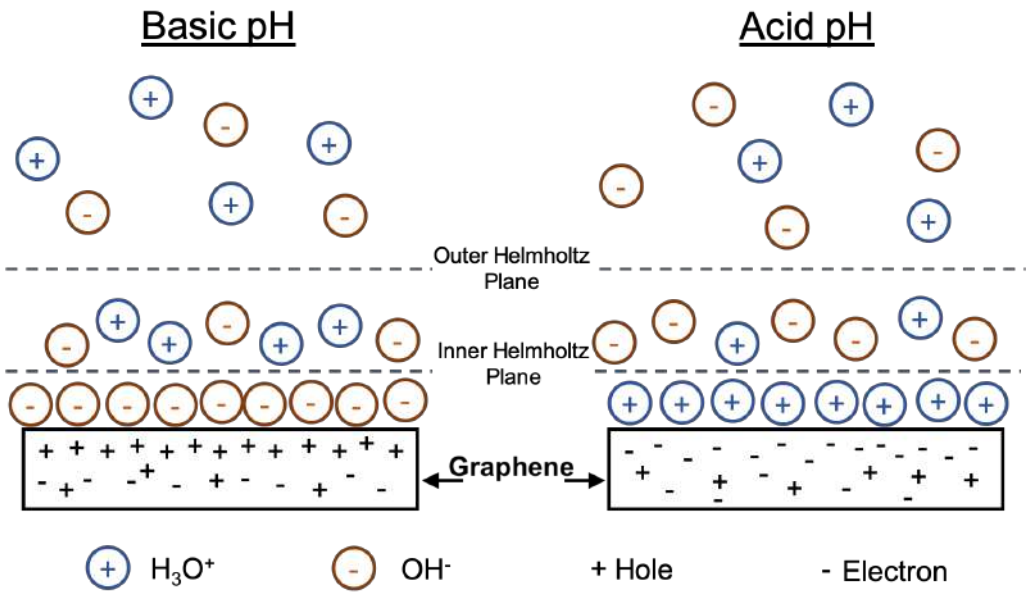


Figure 2.11: Electric double layer schematic with inner and outer Helmholtz planes. The formation of a dielectric-like layer produces a capacitance effect on the graphene channel, changing its carrier concentrations and doping the graphene. (Adapted from [62]).

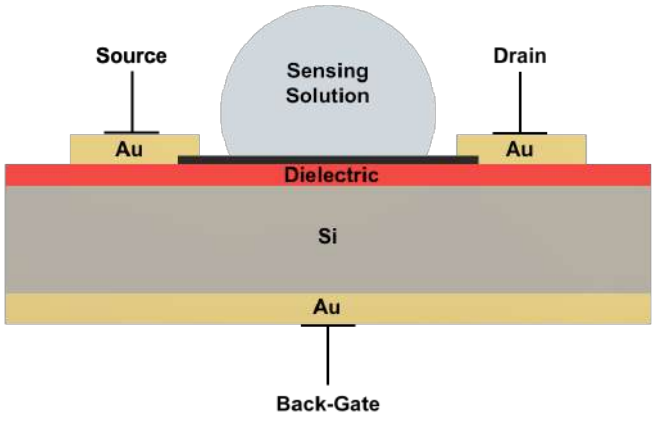
Chemiresistive graphene sensors have also been employed in biosensor applications using bio-receptors bound to the graphene surface [47] [48].

2.3.2 Back Gated FET Sensor

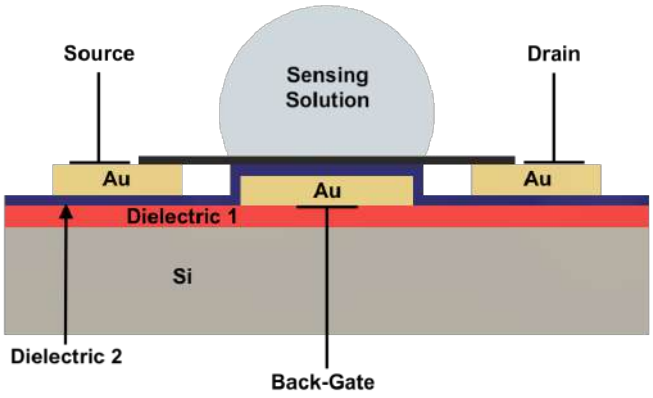
The back gated sensor design has advantages over other gated sensors due to its solid metal/silicon gate which enables a high level of integration for different applications. This includes in vivo measurements and handheld point-of-care measurements. Additionally, the gate dielectric is isolated from a sample solution. This removes errors caused by the liquid gate charging and allows for wet and dry diagnostic measurements. Figure 2.12 shows the two main configurations of the back gated graphene FET: (a) the silicon gated FET design, where doped silicon is used as the substrate wafer and a metal electrode applies the gate bias, whilst the dielectric film acts as the insulating capacitive layer. (b) The buried metal FET design, which uses

an additional dielectric layer on top of a buried metal gate electrode produce the capacitor under the graphene.

The use of the high κ dielectric materials (Hafnium Oxide) in graphene FETS has been shown to provide high specific capacitance, producing a high transconductance and allowing the device to operate at low gate voltages [61].



(a)



(b)

Figure 2.12: (a) Cross-section view of silicon back gated graphene FET sensor. (b) Cross-section view of buried metal back gated graphene FET sensor.

Back gated FET sensors can be used to perform Dirac point measurements by holding a continuous bias across the graphene channel measuring the current across the channel, whilst performing a bias sweep across the back gate. The electric field produced by the charge stored in the capacitor transfers electrons to the graphene in one bias direction and transfer electrons away from the graphene in the other bias direction. Effectively this gating effect can change the primary charge carrier in the graphene channel. When the carrier concentrations of both holes and electrons are equal, the "Dirac point", the resistance of the graphene channel is at a maximum. The location of the Dirac point at a negative or positive bias gate voltage indicates the doping of the graphene channel as either N-type or P-type (Figure 2.13). Gated FET sensors measure the change in Dirac point as target molecules bind to the surface changing the surface charge and therefore doping of the graphene channel.

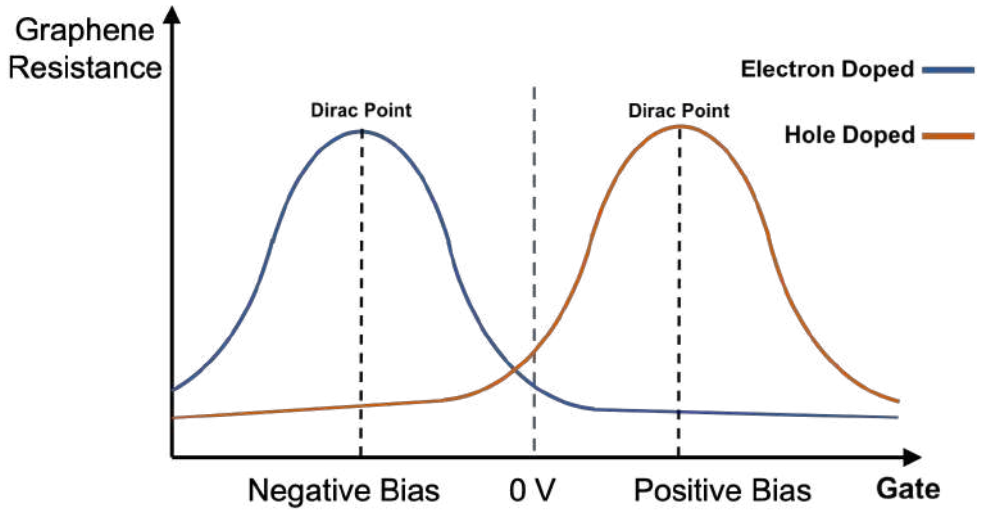


Figure 2.13: Dirac point measurement using gated graphene FET device with an electron (N-type) doped graphene channel and a Hole (P-type) doped graphene channel.

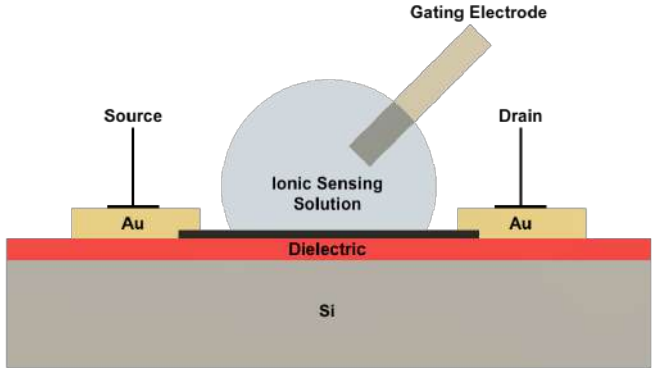
Back gated graphene FETs have been used for both liquid-based sensing, liquid analyte (measured dry) sensing and dry gas sensing [63] [50] [49]. But requires more complex fabrication process flows which can increase average cost per sensor.

2.3.3 Liquid Gated FET Sensor

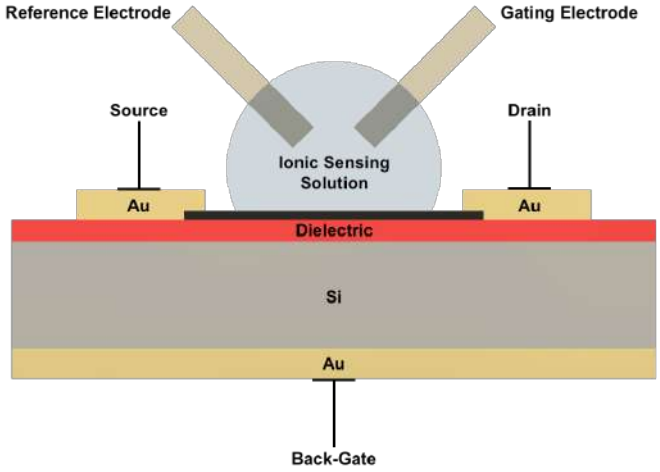
In a liquid gated graphene FET (LGFET) the solid gate used in the back gated FET is replaced by an ionic liquid and an external electrode. The electric double layer formed at the graphene surface acts as a quasi dielectric layer. The external gate electrode is still required to apply a bias to the ionic liquid. This is routinely performed using an external electrode made of Pt wire or Ag/AgCl [64]. However, devices can be fabricated with the gating electrode directly patterned onto the G-FET chip as part of a full lab-on-a-chip style sensor [65].

Figure 2.14 shows the layout of a standard liquid gated set up and modified setups that are common in the literature [53] [52]. To monitor the gate voltage more accurately an electrochemical three-electrode system is used, where the gate electrode (or working electrode) applies the gating bias and the reference electrode monitors the voltage in the ionic solution. This has been shown to provide greater accuracy in terms of measuring the voltage in the ionic solution [66].

Materials used for the gating electrode have been compared in the literature, Pt, Pd etc. It was shown that a Pt metal gate electrodes produced the lowest current variations [67]. Similarly, the type of ionic solution and pH used has been investigated. It has been shown that the makeup of the ionic solution is not as important to the sensing capability of the graphene when using a reference electrode to measure the potential of the ionic solution [68]. Some sensors have been tested using blood serum as the sensing liquid, which for many biosensors would be the end goal for a point of care sensing system [69].



(a)



(b)

Figure 2.14: (a) Cross-section view gating electrode connected to ionic liquid. (b) Cross-section view LGFET modified using three electrode set up and back gating connection.

Similar to a back-gated graphene FET the liquid gated FET can be used to for Dirac point measurements of the graphene channel. Although this sensing method has to exclusively be performed in a wet environment due to the ionic liquid solution, there have been recent developments using ionic hydrogel gates to maintain the ionic makeup when bringing the analyte solution into contact with the sensor [70]. LGFET systems have also been implemented as gas-based sensors where the gases

diffuse through the liquid/gel membrane and absorb onto the bio-receptor modified graphene surface.

2.3.4 Capacitive FET Sensor

Capacitive sensing often relies on similar G-FET systems such as back-gated and liquid gated FET designs, measuring capacitance changes instead of resistance changes of the graphene channel (Figure 2.15) [71]. ALD deposited dielectrics are used to to insulate the gate electrode. In some cases, encapsulation techniques such as ALD deposited dielectrics or 2D material layer transfer such as hexagonal boron nitride have been used as a permanent dielectric layer encapsulating the graphene channel. The capcitance is then measured between the ionic liquid and encapsulated graphene. Bio-receptors are then bound to the dielectric layer instead of the graphene layer. The graphene's sensitivity to electric field changes can be detected through the thin encapsulating film [72].

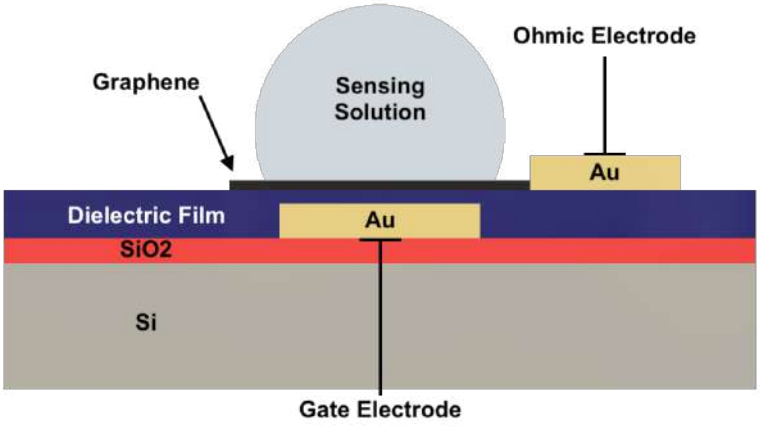


Figure 2.15: (a) Cross-section view capacitance measured between graphene electrode and gate electrode.

2.3.5 Graphene Electrochemical Sensor

Electrochemical sensors function differently to a G-FET electrical resistance sensor. The measurement is not based on the flow of charge carriers across the graphene

channel. Most electrochemical sensors do not use a graphene channel structure, but the graphene is used as a single electrode submerged in an ionic solution. The electrons flow between a "counter" electrode and the graphene "working" electrode. Electrochemistry is the study of this flow of electrons due to chemical processes occurring on the working electrode surface [73]. The most common electrochemical setups require 3 electrodes, a working electrode (graphene), a counter electrode and a reference electrode.

The process of oxidation and reduction (redox) caused by chemical or voltage changes can be measured using the three-electrode system. The reference electrode acts as a reference when measuring electron transfer processes between the working electrode and the counter electrode. The reference electrode is also used for controlling the working electrode potential (without producing current). The reference electrode should have constant electrochemical potential e.g. an Ag/AgCl aqueous reference electrode. In the three-electrode system, the reference potential is much more stable, and there is compensation for the voltage drop that occurs across the solution.

If the graphene surface is oxidised/reduced through an analyte binding to a bio-receptor on the surface, this causes electrons to either be gained or lost by the working electrode. The first application of carbon nanotubes in electrochemistry was for the oxidation of dopamine [74]. Graphene-based devices show excellent electrocatalytic activity towards the reduction and oxidation of paracetamol, showing that the Graphene surface can be electrochemically modified [75]. It was later shown that the responsiveness of graphene and carbon nanotubes to electrochemical change is due to the graphene edges, where heterogeneous electron transfer is much faster than through the planar region. Pristine graphene without impurities has a lower electron transfer rate compared to graphite-based materials [76].

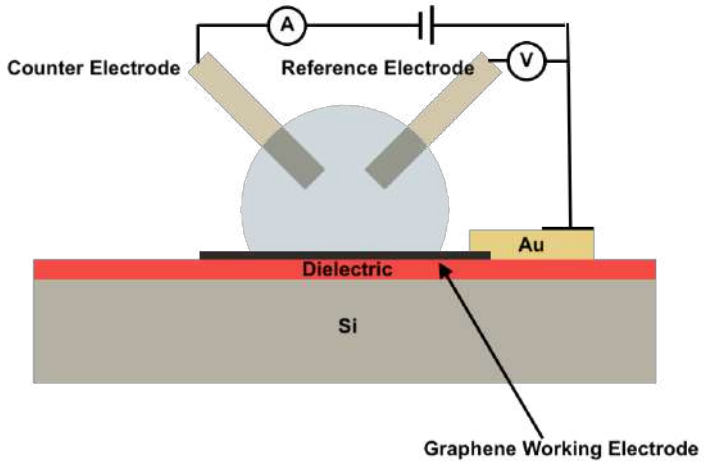


Figure 2.16: Three electrode setup of graphene FET for electrochemical sensing.

2.3.6 Functionalisation & Bio-receptors

Biosensor functionalisation is the process of chemically modifying the surface/edges of the graphene with a bio-receptor. Biosensors are used for the detection of target analytes (biomarkers), to create a sensor with high specificity; the bio-receptor immobilised on the graphene must only bind the target analyte. The type of bio-receptors used vary depending on the target molecule. They can include amino acids, enzymes, antibodies (whole/fragmented) and aptamers/nucleic acids [77].

Bio-receptors often require a linker molecule to enable immobilisation onto the graphene surface. These linkers require there own functionalisation process to immobilise the linker prior to the bio-receptor attachment [78].

In certain cases, the bio-receptor can be synthesised with the linker molecule pre-conjugated directly onto it. The conjugation of the linker molecule and bio-receptor on the graphene surface was compared to pre-conjugated bio-receptors, it was shown that the pre-conjugated system produces higher yields of bio-receptors immobilised on the graphene surface and greater sensitivity to the target analyte [79].

The functionalisation of the graphene surface is also employed to deliberately dope the graphene and modify the sensor's electronic properties (e.g. tetrathiafulvalene). Traditionally band-gap engineering aims to bring the Dirac point close to

midpoint 0 V, reducing the need for high voltage equipment to monitor the Dirac point shift [80].

The functionalisation of graphene can be performed through covalent bonding to the carbon atoms in the graphene lattice, or by non-covalent binding to the graphene by electrostatic and/or weak Van der Waals bonding (Figure 2.17).

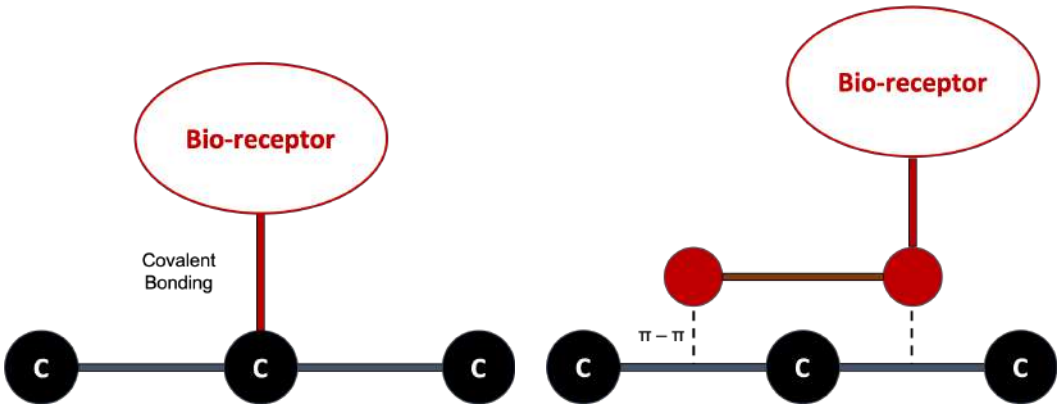
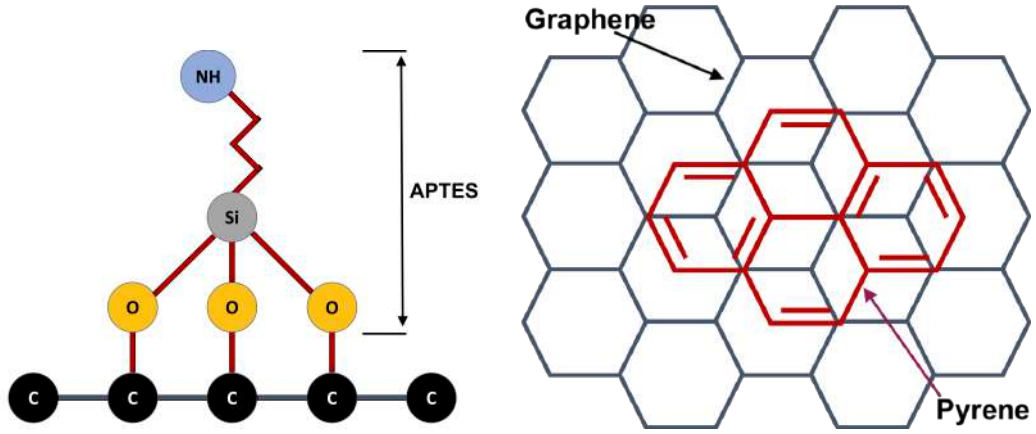


Figure 2.17: (a) Covalent bonding bio-receptor to carbon atom. (b) Non-covalent π-π stacking of bio-receptor on graphene sheet.

Covalent bonding methods including (3-Aminopropyl)triethoxysilane (APTES) which links to the graphene surface through three oxygen molecules that form C-O bonds with the carbon in the graphene lattice [81]. Non-covalent bonding is preferred as the structural and electrical properties of the graphene sheet are then maintained [82]. Non-covalent functionalisation often occurs through an interaction between the π-electron cloud of the graphene and the functional molecule (pyrene, acridine, fluorenylmethyl ect.), otherwise known as π–π stacking (Figure 2.18) [83].



(a) (b)

Figure 2.18: (a) APTES linker molecule used for covalent bonding to oxidised graphene surface. (b) Top-Down view of Pyrene molecule π-π stacking with graphene sheet.

Bio-receptors are the molecules/proteins that are responsible for binding the target bio-marker, these bio-receptors are generally categorized into Aptamers(DNA and RNA), Oligonucleotides, antibodies and enzymes.

Aptamers Aptamers are short-chain peptides or single-stranded nucleic acids designed to fold into a three-dimensional (3D) structure specifically for binding to target analytes. Aptamers have attracted considerable attention due to their ease of synthesis, high binding efficiency and affinity, specificity, and high stability to target biomarkers. Most of all, aptamers have been extensively researched due to their small size (sub 5 nm) and ability to reorientate close to the sensor surface, which is a desirable trait to combat the issues faced with Debye screening (sub 1 nm).

In G-FET biosensors, aptamers have two main processes that cause doping/resistance changes that enable in analyte sensing (Figure 2.19). The first process involves the aptamers reorientating closer to the graphene surface hole doping (e.g. for detection of dopamine, glucose). The second process involves the aptamers stem-loops reorientating away from the graphene surface electron doping the graphene surface

(e.g. for detection of serotonin, S1P) [84].

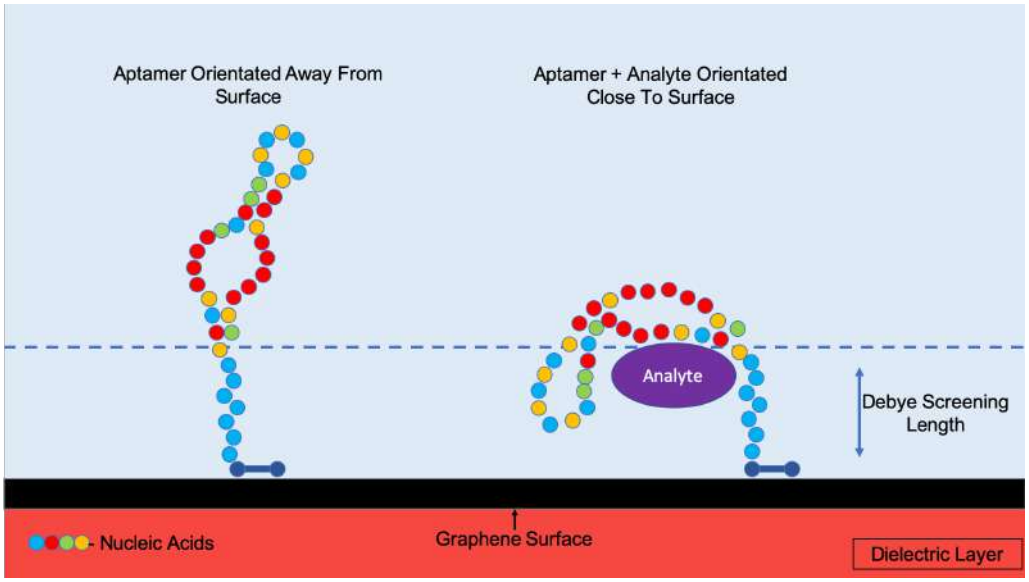


Figure 2.19: Aptamer functionalisation of graphene surface showing orientation away from surface and analyte binding causing reorientation close to the surface.

Debye length screening is a dependent on the ionic strength of the solution which forms the electric double layer above the graphene surface. It is defined as the length at which surface charges of molecules no longer affect the mobile charges of the graphene [85] [86].

Oligonucleotides Oligonucleotides are short (normally 6-25 nucleotides) DNA and RNA molecules. They are most commonly used for detection of specific DNA or RNA sequences, a single stranded oligonucleotide (bio-receptor) is attached to the graphene surface, when a complementary sequence (the analyte) comes into contact with the bio-receptor strong Van der Waals forces (Hydrogen bonds) bond the two sequences together (Figure). As DNA/RNA sequences have strong negative charges present in their phosphate structure, this creates a charge close to the graphene surface that alters the charges, present in the electric double layer and can be detected as a change in resistance/doping of the graphene surface. This can be used for multiple disease diagnostics or genetic testing, a system based on ssDNA

has been used for detection of viral HIV-1 by binding a specific sequence of the viral DNA [87].

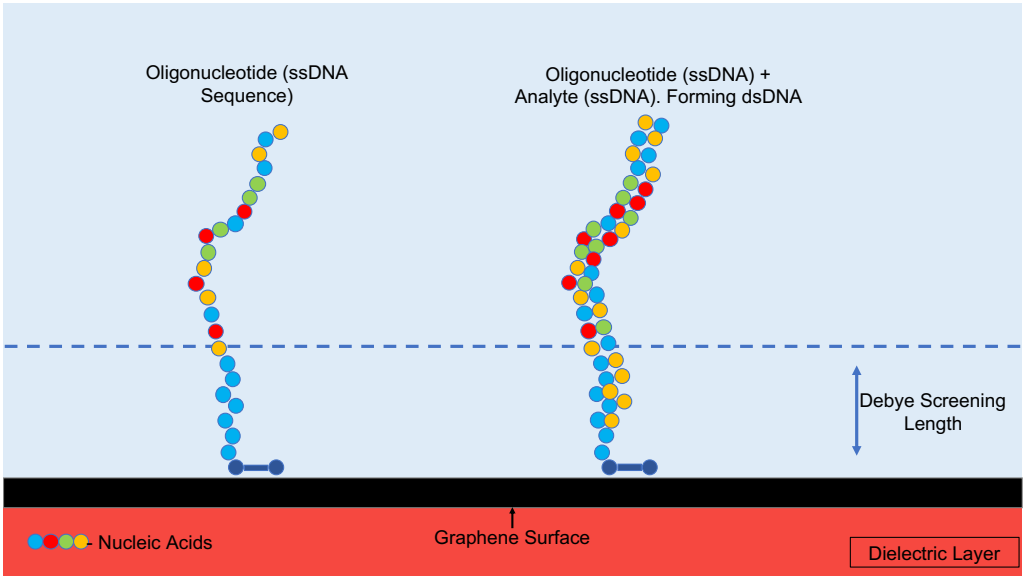


Figure 2.20: ssDNA functionalisation of graphene surface before and after binding of target ssDNA molecule

Antibodies The other main bio-rector used for biosensor assays are antibodies, these are the proteins produced by the body to detect/bind the analytes in vivo. Antibodies vary in size but generally are larger than aptamers (approximate 10-15 nm in length), and do not reorientate themselves closer to the graphene surface during analyte binding. This length is outside the graphene's Debye length so has little effect on the graphene doping. In some cases, truncated antibodies have been used as a way of reducing the distance at which the analyte binds on the graphene surface [88].

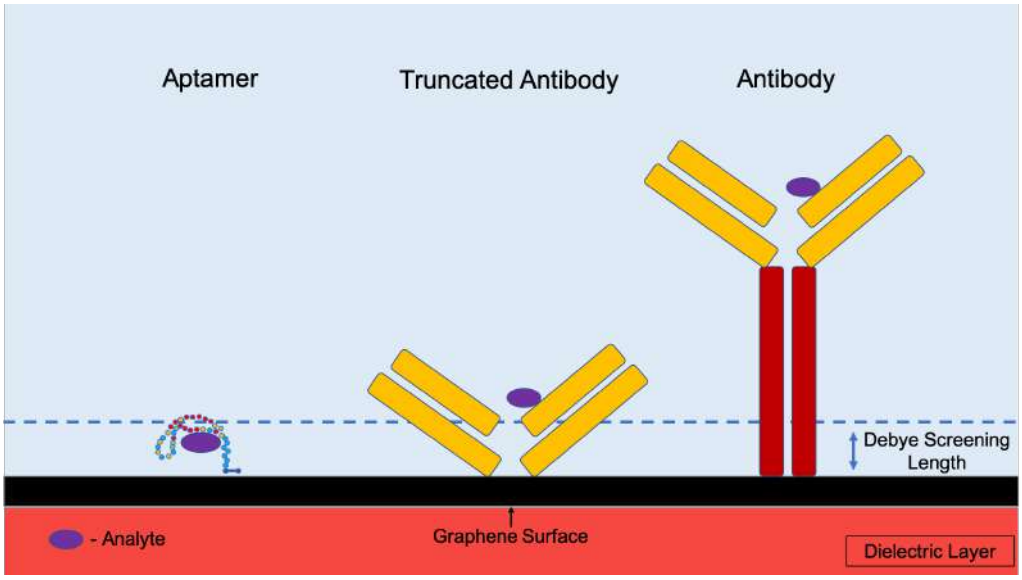


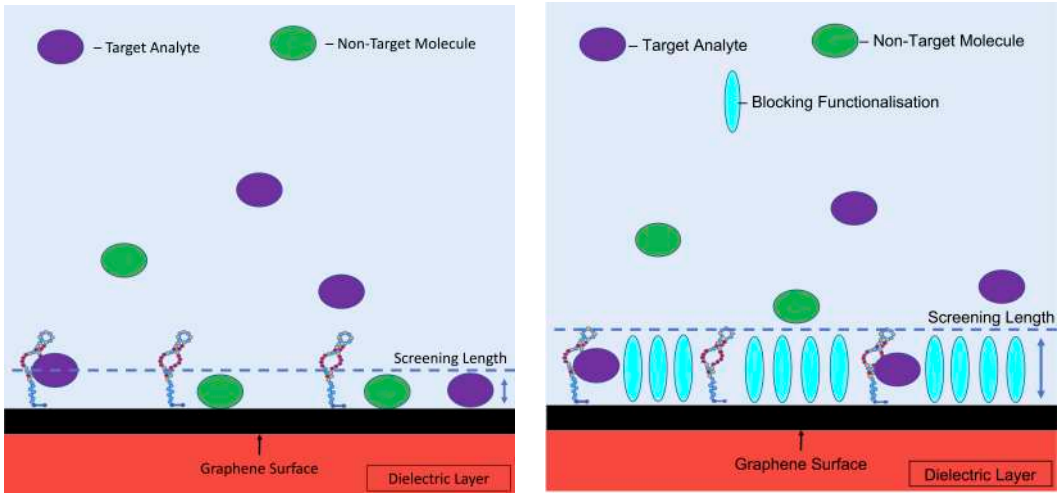
Figure 2.21: Bio-receptor molecules and their approximate sizes when bound to analyte, compared to debye screening length.

Enzymes Enzymes are proteins found in the body which perform a multitude of functions broadly they are used for cleaving (breaking) of larger molecules into smaller ones (Amylase converts starches into sugars). Or for boding smaller molecules to form larger molecules (RNA polymerase constructs DNA sequences). Enzymes are often referred to as biological catalysts as they reduce the energy required for these biological functions. The enzyme glucose oxidase was implemented as the bio-receptor for an diabetes glucose monitoring test in 1962, considered the original biosensor. Graphene electrochemical sensors can use the oxidation/reduction of the target analyte by the surface bound enzyme and monitor the current change (direct electron transfer) in the electrochemical system. This can be used for various analyte detection, pathogens, proteins for disease detection [89] [90].

Blocking Chemistry

Additional to the bio-receptor, other functional layers/molecules can be attached onto the graphene surface. Most commonly, "blocking" molecules are used to increase sensor performance, as they can perform multiple roles simultaneously. The

primary use of blocking molecules is to saturate the graphene surface after immobilisation of the bio-receptor. In this role the blocking molecule will prevent physisorption (or potential bonding) of molecules to the graphene surface. Without the use of a blocker, other analytes/molecules could physically adsorb onto the surface within the debye length and cause a mobile charge change (Figure 2.22). The use of blocking molecules has been shown to increase sensor sensitivity by up to 10-fold [91]. The use of large blocking molecules such as 10-kDa polyethylene glycol has been shown to both saturate the graphene surface, and also increase sensitivity by increasing the effective debye screening length of the graphene surface (extending the double electric layer to the length of the blocking molecule) [86].



(a) (b)

Figure 2.22: (a) Graphene sensor operation without blocking functionalisation. Non-specific physisorption of target and non target proteins/molecules. (b) Operation with blocking functionalisation on graphene surface, preventing physisorption of molecules/proteins.

2.4 Graphene Sensor Fabrication

2.4.1 Substrate Choice

CVD growth graphene, pre-transferred onto SiO_2 wafers can be purchased in wafer sizes of up to 150 mm diameter. The current aim for graphene technology is fabrication at CMOS foundry level processing for full scale commercialisation (European Graphene Flagship Roadmap 2019). Therefore, the substrate choice is based around Silicon technology and the dielectrics that can be deposited onto the silicon surface.

SiO_2 has been the primary dielectric of choice since it was first used to isolate graphene in 2004 [3]. The commercially available monolayer graphene on SiO_2 comes in both 90 nm and 300 nm SiO_2 thickness (Graphenea, Spain). This thickness also corresponds to the thicknesses at which graphene produces the highest contrast and can be seen optically [5]. The effect of charge puddles on the oxygen terminated surface in contact with the graphene, it is believed these dangling bonds have a strong hole-doping effect removing electrons from the graphene channel. [92].

Silicon Nitride is also available from Graphenea but limited to 10 x 10 mm substrate dimensions. The sheet resistance of monolayer graphene and the electron mobility differs depending on substrate choice. Some gate oxides such as Al_2O_3 and HfO_2 have been tested as part of graphene FET development [93]. New 2D materials such as hexagonal boron nitride (hBN) have been shown to produce the highest carrier mobility in graphene. Table 2.3 gives the commercially available and literature derived properties of graphene varies on dielectric substrates.

Table 2.3: Table of graphene electronic properties on different dielectric substrates.

Substrate	Carrier Mobility ($cm^2/V\ s$)	Sheet Resistance (Ω/sq cm)	Reference
SiO_2	3760	450 ±40	[94]
Si_3N_4	1432 ±428	576 ±172	Graphenea
hBN	127500 ±25000	Not Found	[95]
Al_2O_3 Encapsulated	6900	Not Found	[96]
HfO_2 Encapsulated	20000	Not Found	[93]

On SiO_2, variation from the 300 nm oxide thickness even within 10 % change can result in the contrast of the graphene layer on the SiO_2 becoming less observable [5]. This creates problems during photolithography, specifically during alignment and optical quality checking as the graphene layer becomes practically invisible and therefore much more difficult to align using the optical microscopes of a mask aligner tool.

It is well documented that the interaction of SiO_2 on graphene's electrical transport properties [97]. However, it has also been shown that Silicon Nitride as a graphene substrate can produce similar peak conductivity levels under atmospheric conditions to that of SiO_2, but due to impurities in the Nitride films the carrier mobility is lower the SiO_2 [98] [99]. hBN has been shown to produce the highest carrier mobility of all substrates and encapsulation methods, this is due to its matching single layer smooth sheet with hexagonal lattice which prevents charge puddles and trapped charges normally encountered with wafer substrates [95]. However, hBN is still a research-focused material and cannot be purchased as a standard wafer substrate.

2.4.2 Pre-Process (Conditional) Annealing Step

It has been previously established by the Swansea University research group that pre-process annealing is required for top contact graphene fabrication, to improve adhesion and produce yields above 50 % [100]. Graphene annealing is used extensively in the literature to increase graphene substrate adhesion [101] [102].

Vacuum annealing can lead to the formation of C-O and C=O bonds. This bonding could be due to reactive O^- groups from the SiO_2 substrate created during the annealing process bonding to the graphene [101].

The source of yield reduction for non-annealed samples is due to graphene delamination during photolithography steps, specifically during exposure to developer and during photoresist removal steps. The process of graphene annealing via Rapid Thermal Annealing is a short-term process which can also release the induced strain in the graphene lattice and create dangling bonds at the SiO_2 interface [103]. Predominantly this results in physical bonds such as Van der Waal bonding between the SiO_2 and graphene layer. Longer duration vacuum annealing has been shown to produce greater adhesion between the graphene and SiO_2 surface which is thought to be due to both physical and chemical bonds formed between the SiO groups and the graphene [104]. SiO_x exhibits an O^- terminated surface as well as a Si^+ surface, which is highly reactive at high temperature during the annealing process. However, it is thought that the C atoms interact more strongly with electronegative O^- ions than the electropositive Si+ ions, thus, C-O and C=O bond formation is more likely [101].

Another explanation for increased adhesion from annealing is the removal of interfacial water layer between the graphene and substrate, decreasing H_2O^- assisted hole doping and thus bringing the graphene layer closer to the substrate [104]. This removal of inter-facial water and subsequently the reduction of this inter-facial water layer over time fits with previous findings from Swansea University.

2.4.3 Photolithography For Graphene Etch Mask

Photolithography is a lithographic technique that is used to change the properties of photoactive polymers, known as photoresists, using UV light [105]. Photoresists compose of four key substances, the polymer, solvents, sensitizers and additives. The polymer is the solid organic material that changes its solubility following UV exposure. This polymer is diluted in solvents to thin the resist. Sensitizers and additives are used to control the reaction of the photoresist to UV light, to achieve the desired process result. The most common chemical base for positive photoresists are the Diazoquinones (DQ). UV light breaks of nitrogen molecules of the DQs decomposing them into an carboxylic acid product (elimination of Nitrogen and binding of H_2O). This acidic derivative of the photoresist is then soluble in a basic developer solution [106].

The first photolithography process is used to produce an etch mask for the final geometry of the graphene channel. A thin positive photoresist layer is employed in this process, as it is easier to clean and remove from the graphene surface with less time spent in organic solvents [107].

2.4.4 Graphene Etch

The graphene etch process is performed using an oxygen plasma etch process. The Oxygen (O_2) plasma removes organic matter including the exposed graphene layer and other carbon oxides and trapped water vapour. The removed carbon is pumped out of the chamber by the vacuum system. This method of etching graphene is the same as an oxygen plasma ashing process to clean organic contaminants off of a surface [108].

Other processes have been explored to replace the use of photoresist etch mask. This includes using a metal etch masks such as Ni (Ni has low carbon solubility) which can be etched without causing graphene damage [109]. Targeted etch processes that do not require an etch mask have also been explored, the use of laser direct writing (LDW) has been explored for graphene removal in ambient conditions

directly on the insulator coated wafer. This method produced sub-micron features but required a Ni evaporated coating oil immersion layer for writing [110]. Other approaches without coatings, using a Ti sapphire 50 fs pulsed laser, have been used for fabricating a residue-free graphene device process on SiC epitaxial graphene wafer [111].

2.4.5 Photoresist Cleaning

For G-FET fabrication (with graphene pre-transferred onto the SiO_2 substrate), there are three photoresist processes required, all of which coat the graphene surface: (1) the photoresist used for CVD transfer; (2) the photoresist etch mask for graphene channel etching; (3) the photoresist mask used for metal contact pads. Each of these steps is likely to leave dispersed residues across the graphene surface when performing a standard solvent clean with Acetone and isopropanol (IPA).

Photoresist removal is important for improving graphene FET performance, as resists have been shown to reduce carrier mobility from 3410 cm^2/Vs to 1125 cm^2/Vs. Resist residue also result in higher levels of hole doping, shifting the Dirac point from 5.2 V to 11.6 V when FET devices on SiO_2 were fabricated with and without a sacrificial barrier layer [112]. The cause of these changes is thought to be charge scattering due to the photoresist residues closely bonding (π-π stacking) to the graphene surface. Charge scattering (Colomb scattering) is caused by impurities on or underneath the transferred graphene, creating non-uniform electric fields across the graphene sheet and interfering with the charge carriers, reducing the carrier mobility [113].

Negative photoresists are more likely to produce non-removable photoresist residue, as UV exposure and baking causes cross-linking reactions producing non soluble polymer coatings. Even the use of positive photoresists such as PMMA and S1813 has been shown to produce photoresist contamination [114]. Additional solvent cleaning steps have been shown to reduce, but can cause photoresist residue causing delamination or damage to the graphene channel. These include solvent (NMP) and

(DMSO) cleaning steps.

High-temperature vacuum annealing has been shown to remove photoresist residues and improve graphene electrical performance. A 3-hour annealing process at 350 °C was shown as the most effective treatment for removing PMMA residues. Long duration high-temperature annealing has been shown to induce doping changes in graphene as well as band structure changes due to defects already present forming new covalent bonds during the anneal process [115].

Ultraviolet ozone (UVO) treatment has been shown to reduce PMMA residue post graphene transfer. FETs fabricated using a UVO treatment for 10 mins showed higher carrier mobility 3264 cm^2/Vs compared to non treated 1725 cm^2/Vs. Increasing UVO to 16 minutes starts to degraded the graphene and the carrier mobility reduces [116].

Additional cleaning mechanisms such as UV cleaning can also be introduced to reduce photoresist residue on the graphene surface. Particularly when using positive photoresists and deep UV cleaning [38].

Introducing sacrificial layers such as e-beam evaporated yttrium (Y), deposited before photolithography and removed by dilute HCl etching after device fabrication, has been shown to reduce photoresist residue. AFM analyses confirmed graphene FETs made with the Y sacrificial layer had lower levels of roughness (photoresist residues). Electrical measurements showed a reduction in device resistance [117]. Similarly, Aluminium (Al) evaporation has been used to produce an Al sacrificial layer to reduce photoresist residues on graphene, increasing electrical performance [118].

2.4.6 Metal Electrode Deposition

Graphene FET sensors require interconnects to make electrical/electrochemical measurements on the graphene surface. These interconnects are fabricated using metal deposition onto the graphene and SiO_2/Si surface.

Graphene device contact resistance at the metal-Graphene interface has been

investigated with several adhesion metals used. A Ni/Au bilayer metal stack was shown to have the lowest contact resistance 500 $\Omega\mu$m. The contact resistance for both Cr/Au and Ti/Au samples is significantly higher than that of the Ni/Au. However, contact resistance measured in the literature varies for the same metals and Ni is not always reported as having the lowest contact resistance [119] [120] [121] [122] [123] [124]. The explanation given for the unreliable reporting of contact resistance is that the graphene device fabrication highly variable, the contact resistance is also dependent on other factors such as photoresist residue, graphene grain size and lattice defects.

A two-layer metal stack is often used for fabrication of metal contacts and was previously developed as a standard process at Swansea [100]. First, the adhesion metal layer chromium (Cr) 20 nm which naturally forms chromium oxide at the interface with the SiO_2 substrate creates a physical type bond (Van der Waal bonding). The Cr also makes contact with the graphene forming both side and edge contacts with the graphene due to sputtering damage (chromium carbide formation) [125]. The second layer is the capping metal which is fabricated using palladium (Pd) 80 nm, a noble metal which doesn't oxidise in the atmosphere and is chemical unreactive to most acids and bases.

Pd fits into the same category as Nickel in that it changes the graphene's electronic structure and bonds to the graphene through chemisorption, the lattice structure reduces the physical distance between the graphene and metal layer altering the electrical behaviour of the interconnect. [126] [9] [127]. For graphene transfer performed on a wafer after metal deposition, the Pd capping metal acts as the graphene adhesion metal. Chromium is not used as the capping layer as it the surface oxide would increase interconnect resistance over time.

2.4.7 Passivation of Graphene

Passivation films are primarily used as protective coatings to protect semiconductor devices from electrical and chemical contamination. Passivation films are also used

as inter-layers to separate metal tracks in multilayer integrated circuits (ICs) during semiconductor fabrication [128]. In the case of G-FET devices, passivation materials are used to protect the metal contacts connecting to the graphene channel but a "passivation window" allows the graphene surface to be open to the environment (Figure 2.23).

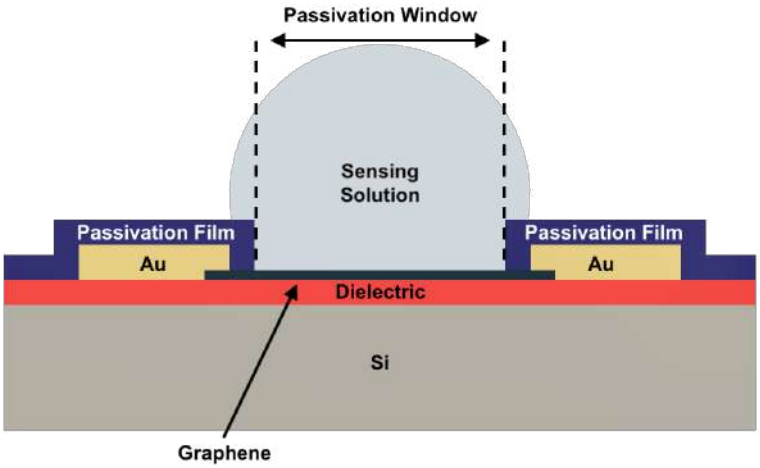


Figure 2.23: Passivation film isolating the metal contacts and substrate from the environment. Passivation window allows the sensing solution direct contact with the graphene surface.

Passivation of G-FET devices is a requirement for measurements in highly ionic solutions such as for liquid gated G-FETs, to eliminate parasitic current between metal contacts in solution. The gate voltage could short circuit via the metal contacts through the ionic solution if exposed to the sensing solution. Even chemiresistive sensors can suffer from excessive leakage currents through the exposed source-drain contacts [129]. For functionalisation, amine linker molecules preferentially bind to Au surfaces and are often used as part of Au nanoparticle conjugate systems [130]. Having exposed contact electrodes means a non-uniform functionalisation of the graphene surface. This will lead to reduced sensitivity as the target analytes can bind to bio-receptors bound to the metal tracks and to the graphene channel.

For G-FET fabrication, passivation using dielectric films has also been shown to

improve carrier mobility and electron doping to bring the Dirac point closer to 0 V. G-FETs fabricated on SiO_2 in ambient conditions are generally hole-doped by the SiO_2 and Oxygen atmosphere can have Dirac point voltages above 50 V [96].

Table 2.4 lists several current materials used for G-FET passivation reported in the literature, as well as materials used for top gated G-FET devices (as the dielectric material can double as the gate oxide and passivation film). For G-FET fabrication, passivation films are required to be deposited and enable revealing of the passivation window, without causing damage to the graphene lattice; minimal doping or deliberate doping to bring the Dirac point close to 0 V; and no residue/-modifications that would reduce the carrier mobility of the graphene.

Table 2.4: Table of passivation materials for (G-FET) biosensors currently reported in the literature.

Graphene Source	G-FET Type	Passivation Material	Deposition Technique	Passivation Window	Effect On Graphene	Reference
CVD grown	Electrolyte-Gated LGFET	SU-8	Spin Coating	Direct Photolithography	Increase in yield resistance	[129]
CVD grown	BGFET	PVA PDMS	Spin Coating	Not Found	Electron Doping	[131]
CVD grown	BGFET	Al_2O_3	ALD	Not Found	Reduced doping Increased carrier mobility	[96]
CVD grown	BGFET	Al_2O_3	ALD	Wet etch	Carrier mobility increase	[132]
CVD grown	LGFET	Si_3N_4	PE-CVD	RIE	Not Found	[65]
CVD grown	LGFET	SiO_2	PE-CVD	Lift-Off	Not Found	[133]
CVD grown	LGFET	SiO_2	ALD	Wet etch	Not Found	[134]
CVD grown	LGFET	Si_3N_4	PE-CVD	Lift-Off	Not Found	[51]
SiC Epitaxial grown	Hall Bar Resistor	Parylene	Vaporised & Pyrolysed	Not Found	Higher carrier mobility & reduced sheet resistance	[135]

Polymeric Passivation Films

The most common polymer passivation material used for G-FET fabrication is the permanent photoresist SU-8. This is the simplest of the passivation options as it only requires a single photolithography process to both deposit the material and pattern the passivation window [129]. However, this is another photolithography step that brings photoresist in direct contact with the graphene surface. SU-8 as with other photoresist residues has been shown to reduce carrier mobility / increase the resistance of graphene channels [136].

Other polymers such as paralene have been shown to preserve high carrier mobility and reduce sheet resistance. Paralene is a two component system evaporated onto the surface at 175 °C and 160 °C, followed by polymerisation at higher temperature 690 °C and 650 6°C. This process was used for full encapsulation so a passivation window was not fabricated onto the device [135].

Dielectric Passivation Films

Dielectric passivation is widely reports in the literature, often using SiO_2, Si_3N_4 and Al_2O_3. Additional to these dielectrics other materials have been able to be directly applied to the graphene surface without damaging the lattice structure, most of which have been tested as gate dielectrics for graphene top gated FETs and CMOS like devices. Materials include Y_2O_3, TiO_2, HfO_2 and 2D materials such as hBN [137] [138] [139].

There are two main approaches to fabricating the passivation window to expose the graphene surface: (1) Plasma enhanced chemical vapour deposition (PE-CVD) of SiO_2 and Si_3N_4, due to the more directional deposition and low temperatures a photoresist lift-off method can be used, this requires the use of photoresist patterning onto the graphene surface. (2) Alternatively, the use of atomic layer deposition (ALD) results in more conformal dielectric films reducing the effectiveness of a photoresist lift-off process. For material deposited by ALD, an etch process and etch mask are required to create the passivation window, Al_2O_3 can be etched using wet

enchants e.g. (TMAH) based which do not damage the graphene surface. Similarly, SiO_2 can be wet etched with HF acid.

Al_2O_3 passivation has other advantages such as the reported "healing" effect of ALD deposition on the graphene surface. Atomic defects (grain boundaries and dislocations) were removed after ALD deposition and etch. The first Al_2O_3 layer bonds to graphene oxide (C-O) defects. During the etch process all O bonds are reduced leaving behind a pure carbon layer. This is due to the nucleation sights of the ALD deposition targeting the graphene defects during films growth. Graphene healing has been shown to decrease sheet resistance and increase stability in ambient conditions [140]. The disadvantage of ALD films is there slow deposition rate (<1nm/minute) compared to PECVD (30-50nm/minute).

2.4.8 Microfluidic Packaging

Graphene FET sensors require packaging to integrate with a functionalisation/sampling mechanism for the sensing measurement. More basic forms of packaging involve fabrication of a reservoir region for the sensing solution to be held during the gated FET measurement. Figure 2.24 shows an example of this involving an epoxy ring used to encompass the graphene surface region and gating electrodes of the LGFET biosensor [65]. Without the use of the reservoir, the liquid would be free to spread across the hydrophilic surface and even leave the chip surface.

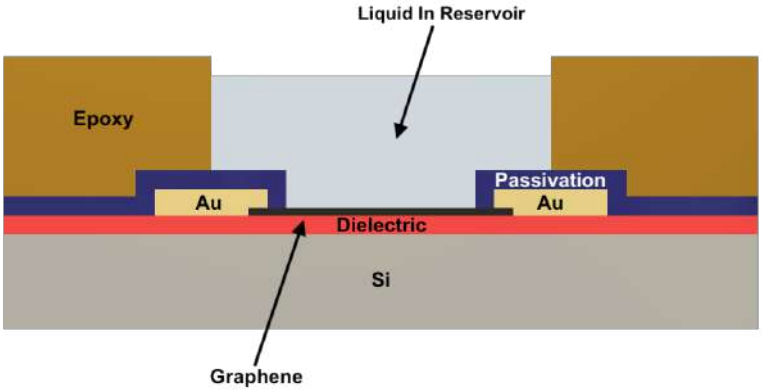


Figure 2.24: Cross section of LGFET with epoxy packaging forming liquid reservoir.

Packaging can also be used to integrate microfluidics onto the biosensor platform. Using microfluidic channels can greatly reduce chemical volumes for both the functionalisation stages and also the sensing measurement when the sample volume is limited. Integrated microfluidics can be used for advanced sample pre-processing techniques including fluid transport, multiplexing, separation/filtering, immobilisation (trapping) and combination/mixing [141].

Microfluidics can be broadly categorized into three main classes: (1) continuous-flow; (2) droplet-based; (3) digital microfluidics. The advantages and disadvantages of each are summarised in Table 2.5. The first of these continuous flow systems were the first developed microfluidics and have the simplest operation, using a continuous flow of liquid either self-drawing or using external pressure. These are often integrated into graphene biosensor systems to allow for small, well-defined sample volumes to be tested on the biosensor platform [51].

Table 2.5: Comparison between three types of microfluidics, adapted from [142]

	Continous-Flow Microfluidics	**Droplet-Based Microfluidics**	**Digital Microfluidics**
Operating Method	Continuous fluid flow through microchannels	Motion of droplets in microchannels, producing using controlled flows of immiscible fluids	Motion of discrete droplets on an array of planar electrodes
Flow Actuation	capillary action, mechanical pumping, electrokinetic	Mechanical (syringe) pumps, (pressure) pumps pumping	Electro-wetting, dielectric (capacitance) control of electric fields
Advantages	Ease of fabrication, simple microfluidic design and operation, top down integration for current screening / sensing platforms, portability (capillary action)	Ease of fabrication, suitable for isolation reactions, high throughput	Low sample consumption, scalable with FET design, reconfigurable, portability
Disadvantages	High sample volume consumption (mechanical pumping system)	Minimal control over individual droplets, limited droplet size changing using same configuration	Complex fabrication, and complex integration with established sensor platforms

Microfluidic Fabrication Methodologies

The most common fabrication technique for microfluidics uses a moulding (soft lithography) process based on a silicone elastomer polydimethylsiloxane (PDMS). This methodology has been in practice since 1998 and is most widely used for microfluidic devices in research [143]. This requires the fabrication of a master mould often using a harder more permanent material compared to the PDMS. The master mould is often fabricated by photolithography using a silicon wafer and patterned photoresist as the microchannels. PDMS microfluidics can be bonded directly to silicon and glass using a plasma surface treatment of both surfaces and subsequently bringing them together. Moulding-based microfluidic fabrication can also be done using a hot embossing approach. Flexdyme "soft-embossing" (Eden labs, USA) requires 10-12 minutes at 105 °C embossing on master mould template. The advantage of Flexdyme sheets is that they are inherently adhesive so do not require surface treatment like its PDMS counterpart. Flexdyme is also more hydrophilic compared to PDMS making liquid filling much easier [144]. Another moulding approach is injection moulded microfluidics. This is standard for the final stages of process development when a microfluidic product needs to be made in large volumes in large volumes as a commercial product [145].

Laminate based microfluidics are produced by stacking individually cut layers bonded together. Simple devices can even be created out of layers of adhesive tape [146]. The most common materials include polycarbonate, PMMA, glass and Cyclic olefin copolymer (COC). The feature size is dependent on the cutting system used to create the layers (knife plotter, CO_2 laser etcher ect.), the vertical height of the channels is dependent on the thickness of the polymer sheets [147]. Unlike moulded systems, each design is cut individually which provides more reconfiguration and ability to rapidly prototype microfluidic devices. The method of bonding the layers together depends on the material used. Adhesives and thermal bonding are most common [148]. This methodology is faster for prototyping but more limited in terms of integrating with FET style devices due to the bonding requirement adhesives and

alignment.

3D printing can be used in the fabrication of microfluidic devices. It is widely used as a method of producing the master-mould for PDMS moulding, replacing the photolithography process by printing the inverted microfluidic channels [149]. True 3D printed microfluidics, by direct writing of the full microfluidic systems with an additive manufacturing process have also been fabricated, although initially larger channels mm scale were created [150]. The three main 3D printing technologies fused deposition modelling (FDM), laser stereolithography (SLA) and multi-jet modelling (MJM) have all been used for direct printing of microfluidic devices [151]. Through advances in 3D printer technology, true "micro" devices and even sub-micron fabrication has been achieved using 2 photon 3D printer systems, these direct laser writing (DLW) systems require piezoelectric actuators for XYZ stage direction. These systems have been used to produce 1 μm 3D features inside standard microfluidic channels [152].

2.5 Blood-Based Diagnostics

The aim of this project is to develop a biosensor for a point-of-care diagnostic system. Blood clotting disorders effect millions of people around the globe. This section gives details about the process of blood clotting and the multiple diseases arise from it, and the potential benefits for a rapid blood-clotting diagnostic sensors.

Blood clotting (coagulation) is the process by which blood transitions from liquid to a gel. It is part of the body's natural defence mechanism, to prevent excessive bleeding when a blood vessel is damaged. Platelets are one of the three main cell types found in the circulatory systems, and along with proteins found in the bloodstream are the primary components that form a blood clot. Normally after the vessel/injury has healed, the blood clot is broken down and the proteins are either recycled or removed as waste [153]. If a blood clot forms inside a vessel and the cause is not due to damage, or the clot breaks off an existing clot, this called thrombosis. Thrombosis can have serious negative health impacts leading to other medical con-

ditions. Clots that are not broken down will travel through the circulatory system until their diameter is greater than the elastic diameter of the blood vessel they are travelling in. They can then prevent blood flow to the surrounding tissue and down flow of the blockage. This can lead to cell and tissue death. If this blockage occurred in the heart it would be known as a "myocardial infarction" (MI). If the blockage occurs in the lungs it is a "pulmonary embolism" (PE) and in the brain, a "stroke".

Coagulation is the third step of the haemostasis mechanism (the blood vessel repair response). The process of coagulation can be activated by two chemical pathways depending on the initial trigger; the tissue factor pathway, which results from tissue damage and the contact activation pathway, which is mainly associated with inflammation. Both lead to the cleaving of fibrinogen to fibrin, which in turn forms the fibre mesh throughout the clot structure. This mesh acts like a net and captures platelets and other blood cells to form a clot [154].

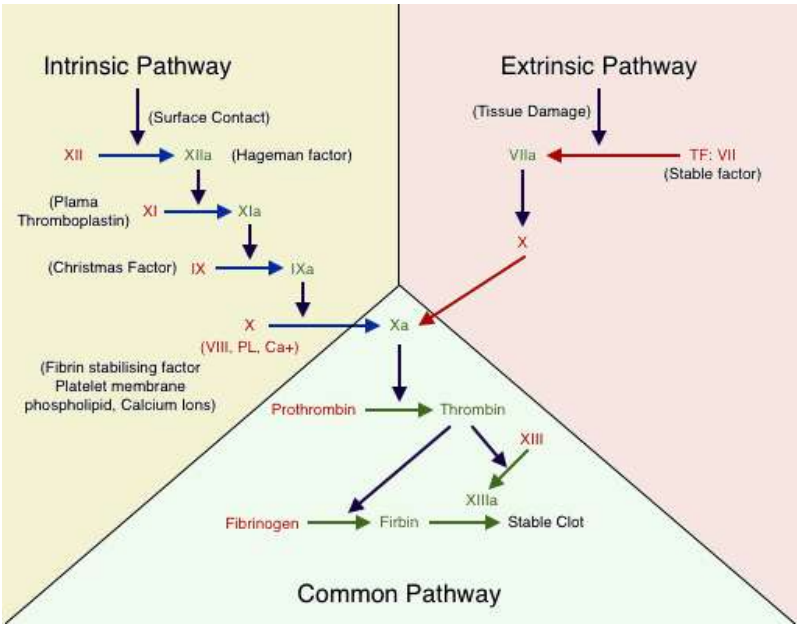


Figure 2.25: The coagulation cascade initially divided into two starting points. The Intrinsic pathway starting with the activation of the hangman factor and the Extrinsic pathway starting with tissue derived factors. Adapted from [155]

Each of these proteins (factors) are required for healthy blood clotting. Each

protein is coded in the human genome by a gene or collection of genes. Genetic blood clotting disorders are due to a mutation in one of the genes which encode a protein in this cascade, such as haemophilia (haemophilia A) which is caused by a mutation in the gene for Factor VIII [156]. Diseases which cause disruption in the coagulation cascade, which limit the formation/effectiveness of a blood clot, are known as coagulopathies (hypo-coagulation disorders). Acquired versions of the disorder include overuse use of the drugs heparin and aspirin. Other linked diseases include vitamin K deficiency, liver failure and Uremia. Coagulopathy can also be attributed to infectious diseases such as meningococcemia, Ebola and Dengue [157].

The other main class of blood clotting diseases fit into the category of hyper-coagulation disorders. These diseases increase the risk of thrombosis and therefore increase the likelihood of life-threatening conditions related to blocked blood vessels. Hyper-coagulation disorders can be both inherited (genetic) conditions and acquired through environmental factors or other diseases [158]. The most common of the genetic conditions is Factor V Leiden thrombophilia which causes an increased risk of thrombosis and clot detachment [159]. Acquired conditions can be caused by a wide array of conditions from lifestyle, low exercise/high blood pressure, or can be a result of other diseases e.g. bowel cancer [160] [161].

For a sensor a sensor to be used as a blood clotting based diagnostic device, the packaging must be designed on the understanding of the current operational requirements of clotting diagnostics testing. Current NHS coagulation screening includes three essential clotting tests: (1) Prothrombin Time (PT) the time taken for the blood to begin to clot, performed by mechanical actuation or an opacity-based test. The PT test measures the extrinsic coagulation pathway due to the addition of tissue factor at the start of the measurement [162].

(2) Activated Partial Thromboplastin Time (aPTT) also measures the time taken to for the blood to begin to clot. This is paired with the PT as it measures the intrinsic pathway due to the addition of a surface activator (silica, celite etc.). So with both the PT and aPTT tests, any times outside of the healthy range can indicate which route of the coagulation cascade has the problem [162].

(3) The third core element of the panel is the measurement of the fibrinogen protein directly. This is quantitatively performed by detection of the fibrinogen molecule (Clauss fibrinogen test) [163]. The levels of the fibrinogen in circulation are used to identify if you have a deficiency or abnormality.

Other tests are often performed with the standard coagulation screen including measurement of D-Dimer peptide, a bi-product of clotting itself, which can be used to determine clotting events (MI, PE, stroke). Both of these molecule detection based tests can help diagnose multiple clotting disorders [164].

Thrombin is the protein at the end of the coagulation cascade which is responsible for cleaving the fibrinogen molecule into fibrin. Direct monitoring for PT and aPTT using micro-volumes of blood could speed up the coagulation screening process and allow it to become more mobile, bringing the test directly to patients [165].

Successful detection of thrombin, the cardiovascular biomarker, has been shown using an aptamer-based graphene electrode approach [166]. When the thrombin protein binds to the aptamers, the aptamer re-orientates hole-doping the graphene and reducing resistance [167]. This makes it the ideal target as the sequence is well documented and has been used previously as a model system for aptamer-based sensors.

2.5.1 Blood Separation Microfluidics

Sample preparation is important for medical laboratory tests making it possible to transport the sample and selectively test for certain biomarkers. For the coagulation screen, blood is collected from a patient in a tube containing sodium citrate (calcium leaching agent) which acts as anticoagulant, preventing blood from clotting in the tube. For the PT and aPTT test calcium is later added and mixed along with the specific proteins for the coagulation cascade to start the clotting procedure once the blood has been transported to the lab, ready for testing.

For protein assays, blood is often centrifuged and separated into the blood plasma liquid phase and the blood cells (Leukocytes, Thrombocytes and Erythrocytes). The

total volume of whole blood taken up by red blood cells is approximately 40 - 45 % [168]. The plasma, containing the circulating proteins, can then be analysed. The advantages of analysing plasma include the lack of interference off blood cells with analyte detection, and improving the sensitivity and selectivity by removing a large proportion of non-target mass from the system [169].

Microfluidic systems have been researched for blood separation, trying to miniaturise the sample preparation step towards a full lab-on-a-chip biosensor system. There are two main categories of blood separation microfluidics Active systems and Passive systems, additionally, a hybrid of the two is sometimes used; Active systems rely on external forces; acoustic wave forces [170], dielectrophoretic force [171], magnetic force [172] and combinations of these methods. In general active systems allow for fast and high throughput systems which are highly accurate. However, the additional complexity increases fabrication costs with more moving components which can make operation more complicated.

Passive systems do not require external forces and are traditionally created as continuous-flow microfluidic devices. These devices are simpler to fabricate, depending on the geometry of the channel to separate the blood cells. This results in lower fabrication costs and simpler operation. In some cases, a pushing force is required to move the blood through the device and the flow is linked to the separation capability. In other devices, a pulling/vacuum force and slow flow rates are used for separation. Table 2.6 reviews the current passive microfluidic systems for lab-on-a-chip blood separation.

- Platelet Poor Plasma = <10 x$10^3/\mu$l
- Platelet Rich Plasma = >10 x$10^3/\mu$l
- White Blood Cell = 1.3 - 35.8 x10^9/L
- Red Blood Cell = 0.03 - 4.7 x10^9/L

Table 2.6: A summary of passive microfluidic devices for blood separation currently in the literature, adapted from [173].

Mechanism	Injected Sample	Sample Throughput Max	Device Target	Reported Performance	Reference
Sedimentation	Whole blood	5 μL in 10 mins	Plasma	99.9–100% blood cell retention	[174]
Hydrodynamic	Whole blood	0.4 μL/min	Plasma	100% blood cell removal	[175]
Hydrodynamic	Diluted whole blood 7–62% Hct.	500 μL/min	Plasma	99.5% blood cell removal	[176]
Hydrodynamic	diluted whole blood 5% Hct.	100 μL/min	Plasma	17.8 % plasma extraction	[177]
Hydrodynamic	Whole blood	0.16 μL/min	Plasma	100% plasma purity 15–25% plasma extraction	[178]
Hydrodynamic	Whole blood	0.33 μL/min	WBC	96.9% WBC purity 97.2% WBC recovery rate	[179]

Single-layer devices are the cheapest to fabricate and can be integrated onto the sensor surface most easily. Sedimentation systems requiring slow flow rates have been effectively integrated into G-FET sensors for analyses [180]. A higher flow rate device should be investigated for a higher throughput system.

Bibliography

[1] S Ergun. Structure of graphite. *Nature physical science*, 241(107):65, 1973.

[2] Harold W Kroto, James R Heath, Sean C O'Brien, Robert F Curl, and Richard E Smalley. C60: Buckminsterfullerene. *Nature*, 318(6042):162, 1985.

[3] Kostya S Novoselov, Andre K Geim, Sergei V Morozov, D Jiang, Y_ Zhang, Sergey V Dubonos, Irina V Grigorieva, and Alexandr A Firsov. Electric field effect in atomically thin carbon films. *science*, 306(5696):666–669, 2004.

[4] AH Castro Neto, Francisco Guinea, Nuno MR Peres, Kostya S Novoselov, and Andre K Geim. The electronic properties of graphene. *Reviews of modern physics*, 81(1):109, 2009.

[5] P Blake, EW Hill, AH Castro Neto, KS Novoselov, D Jiang, R Yang, TJ Booth, and AK Geim. Making graphene visible. *Applied physics letters*, 91(6):063124, 2007.

[6] Matteo Bruna and SJAPL Borini. Optical constants of graphene layers in the visible range. *Applied Physics Letters*, 94(3):031901, 2009.

[7] Andrea C Ferrari, JC Meyer, V Scardaci, C Casiraghi, Michele Lazzeri, Francesco Mauri, S Piscanec, Da Jiang, KS Novoselov, S Roth, et al. Raman spectrum of graphene and graphene layers. *Physical review letters*, 97(18):187401, 2006.

[8] Philip Richard Wallace. The band theory of graphite. *Physical Review*, 71(9):622, 1947.

[9] Filippo Giubileo and Antonio Di Bartolomeo. The role of contact resistance in graphene field-effect devices. *Progress in Surface Science*, 92(3):143–175, 2017.

[10] Annalisa Fasolino, JH Los, and Mikhail I Katsnelson. Intrinsic ripples in graphene. *Nature materials*, 6(11):858, 2007.

[11] Xavier Blase, Angel Rubio, Steven G Louie, and Marvin L Cohen. Quasiparticle band structure of bulk hexagonal boron nitride and related systems. *Physical review B*, 51(11):6868, 1995.

[12] S Yi Zhou, G-H Gweon, AV Fedorov, de First, PN, WA De Heer, D-H Lee, F Guinea, AH Castro Neto, and A Lanzara. Substrate-induced bandgap opening in epitaxial graphene. *Nature materials*, 6(10):770–775, 2007.

[13] Hugo Pinto and Alexander Markevich. Electronic and electrochemical doping of graphene by surface adsorbates. *Beilstein journal of nanotechnology*, 5(1):1842–1848, 2014.

[14] Young-Jun Yu, Yue Zhao, Sunmin Ryu, Louis E Brus, Kwang S Kim, and Philip Kim. Tuning the graphene work function by electric field effect. *Nano letters*, 9(10):3430–3434, 2009.

[15] Yu-Fen Lu, Shun-Tsung Lo, Jheng-Cyuan Lin, Wenjing Zhang, Jing-Yu Lu, Fan-Hung Liu, Chuan-Ming Tseng, Yi-Hsien Lee, Chi-Te Liang, and Lain-Jong Li. Nitrogen-doped graphene sheets grown by chemical vapor deposition: synthesis and influence of nitrogen impurities on carrier transport. *ACS nano*, 7(8):6522–6532, 2013.

[16] Pooja Rani and VK Jindal. Designing band gap of graphene by b and n dopant atoms. *Rsc Advances*, 3(3):802–812, 2013.

[17] Amedeo Bellunato, Hadi Arjmandi Tash, Yanina Cesa, and Grégory F Schneider. Chemistry at the edge of graphene. *ChemPhysChem*, 17(6):785–801, 2016.

[18] Hongtao Liu, Yunqi Liu, and Daoben Zhu. Chemical doping of graphene. *Journal of materials chemistry*, 21(10):3335–3345, 2011.

[19] Kumar Vikrant, Vanish Kumar, and Ki-Hyun Kim. Graphene materials as a superior platform for advanced sensing strategies against gaseous ammonia. *Journal of Materials Chemistry A*, 6(45):22391–22410, 2018.

[20] Xiaomu Wang, Jian-Bin Xu, Weiguang Xie, and Jun Du. Quantitative analysis of graphene doping by organic molecular charge transfer. *The Journal of Physical Chemistry C*, 115(15):7596–7602, 2011.

[21] Min Yi and Zhigang Shen. A review on mechanical exfoliation for the scalable production of graphene. *Journal of Materials Chemistry A*, 3(22):11700–11715, 2015.

[22] Yenny Hernandez, Valeria Nicolosi, Mustafa Lotya, Fiona M Blighe, Zhenyu Sun, Sukanta De, IT McGovern, Brendan Holland, Michele Byrne, Yurii K Gun'Ko, et al. High-yield production of graphene by liquid-phase exfoliation of graphite. *Nature nanotechnology*, 3(9):563, 2008.

[23] Weifeng Zhao, Ming Fang, Furong Wu, Hang Wu, Liwei Wang, and Guohua Chen. Preparation of graphene by exfoliation of graphite using wet ball milling. *Journal of materials chemistry*, 20(28):5817–5819, 2010.

[24] Claire Berger, Zhimin Song, Tianbo Li, Xuebin Li, Asmerom Y Ogbazghi, Rui Feng, Zhenting Dai, Alexei N Marchenkov, Edward H Conrad, Phillip N First, et al. Ultrathin epitaxial graphite: 2d electron gas properties and a route toward graphene-based nanoelectronics. *The Journal of Physical Chemistry B*, 108(52):19912–19916, 2004.

[25] J Hass, WA De Heer, and EH Conrad. The growth and morphology of epitaxial multilayer graphene. *Journal of Physics: Condensed Matter*, 20(32):323202, 2008.

[26] G Reza Yazdi, Remigijus Vasiliauskas, Tihomir Iakimov, Alexei Zakharov, Mikael Syväjärvi, and Rositza Yakimova. Growth of large area monolayer

graphene on 3c-sic and a comparison with other sic polytypes. *Carbon*, 57:477–484, 2013.

[27] Yu-Ming Lin, Damon B Farmer, Keith A Jenkins, Yanqing Wu, Joseph L Tedesco, Rachael L Myers-Ward, Charles R Myers-Ward, D Kurt Gaskill, Christos Dimitrakopoulos, and Phaedon Avouris. Enhanced performance in epitaxial graphene fets with optimized channel morphology. *IEEE Electron Device Letters*, 32(10):1343–1345, 2011.

[28] Mikael Karlsson, Carl Strandqvist, Johnny Jussi, Olof Öberg, Ingemar Petermann, Louise Elmlund, Simon Dunne, Ying Fu, and Qin Wang. Chemical sensors generated on wafer-scale epitaxial graphene for application to frontline drug detection. *Sensors*, 19(10):2214, 2019.

[29] Zhen-Yu Juang, Chih-Yu Wu, Ang-Yu Lu, Ching-Yuan Su, Keh-Chyang Leou, Fu-Rong Chen, and Chuen-Horng Tsai. Graphene synthesis by chemical vapor deposition and transfer by a roll-to-roll process. *Carbon*, 48(11):3169–3174, 2010.

[30] Jesus De La Fuente. Cvd graphene-creating graphene via chemical vapour deposition. *Graphenea. com. Retrieved*, 1, 2015.

[31] Matthias Batzill. The surface science of graphene: Metal interfaces, cvd synthesis, nanoribbons, chemical modifications, and defects. *Surface Science Reports*, 67(3-4):83–115, 2012.

[32] LaiPeng Ma, WenCai Ren, ZaiLi Dong, LianQing Liu, and HuiMing Cheng. Progress of graphene growth on copper by chemical vapor deposition: Growth behavior and controlled synthesis. *Chinese science bulletin*, 57(23):2995–2999, 2012.

[33] Wencai Ren and Hui-Ming Cheng. The global growth of graphene. *Nature nanotechnology*, 9(10):726, 2014.

[34] Seonyeong Kim, Somyeong Shin, Taekwang Kim, Hyewon Du, Minho Song, ChangWon Lee, Kisoo Kim, Seungmin Cho, David H Seo, and Sunae Seo. Robust graphene wet transfer process through low molecular weight polymethylmethacrylate. *Carbon*, 98:352–357, 2016.

[35] Xuelei Liang, Brent A Sperling, Irene Calizo, Guangjun Cheng, Christina Ann Hacker, Qin Zhang, Yaw Obeng, Kai Yan, Hailin Peng, Qiliang Li, et al. Toward clean and crackless transfer of graphene. *ACS nano*, 5(11):9144–9153, 2011.

[36] Ji Won Suk, Wi Hyoung Lee, Jongho Lee, Harry Chou, Richard D Piner, Yufeng Hao, Deji Akinwande, and Rodney S Ruoff. Enhancement of the electrical properties of graphene grown by chemical vapor deposition via controlling the effects of polymer residue. *Nano letters*, 13(4):1462–1467, 2013.

[37] Jian-Hao Chen, Chaun Jang, Shudong Xiao, Masa Ishigami, and Michael S Fuhrer. Intrinsic and extrinsic performance limits of graphene devices on sio2. *Nature nanotechnology*, 3(4):206, 2008.

[38] A Suhail, K Islam, B Li, D Jenkins, and G Pan. Reduction of polymer residue on wet-transferred cvd graphene surface by deep uv exposure. *Applied Physics Letters*, 110(18):183103, 2017.

[39] Jie Song, Fong-Yu Kam, Rui-Qi Png, Wei-Ling Seah, Jing-Mei Zhuo, Geok-Kieng Lim, Peter KH Ho, and Lay-Lay Chua. A general method for transferring graphene onto soft surfaces. *Nature nanotechnology*, 8(5):356, 2013.

[40] Wei Sun Leong, Haozhe Wang, Jingjie Yeo, Francisco J Martin-Martinez, Ahmad Zubair, Pin-Chun Shen, Yunwei Mao, Tomas Palacios, Markus J Buehler, Jin-Yong Hong, et al. Paraffin-enabled graphene transfer. *Nature communications*, 10(1):867, 2019.

[41] Luiz Gustavo Pimenta, Yi Song, Tingying Zeng, Mildred Dresselhaus, Jing Kong, and Paulo Araujo. Direct transfer of graphene onto flexible substrates. In *APS Meeting Abstracts*, 2014.

[42] Wei-Hsiang Lin, Ting-Hui Chen, Jan-Kai Chang, Jieh-I Taur, Yuan-Yen Lo, Wei-Li Lee, Chia-Seng Chang, Wei-Bin Su, and Chih-I Wu. A direct and polymer-free method for transferring graphene grown by chemical vapor deposition to any substrate. *ACS nano*, 8(2):1784–1791, 2014.

[43] Daiyu Kondo, Shintaro Sato, Katsunori Yagi, Naoki Harada, Motonobu Sato, Mizuhisa Nihei, and Naoki Yokoyama. Low-temperature synthesis of graphene and fabrication of top-gated field effect transistors without using transfer processes. *Applied physics express*, 3(2):025102, 2010.

[44] Afzal Khan, Sk Masiul Islam, Shahzad Ahmed, Rishi R Kumar, Mohammad R Habib, Kun Huang, Ming Hu, Xuegong Yu, and Deren Yang. Direct cvd growth of graphene on technologically important dielectric and semiconducting substrates. *Advanced Science*, 5(11):1800050, 2018.

[45] Li Wang, Aiguo Wu, and Gang Wei. Graphene-based aptasensors: from molecule interface interactions to sensor design and biomedical diagnostics. *Analyst*, 143(7):1526–1543, 2018.

[46] Samadhan B Patil, Dharmendra S Dheeman, Mohammed A Al-Rawhani, Srinivas Velugotla, Bence Nagy, Boon Chong Cheah, James P Grant, Claudio Accarino, Michael P Barrett, and David RS Cumming. An integrated portable system for single chip simultaneous measurement of multiple disease associated metabolites. *Biosensors and Bioelectronics*, 122:88–94, 2018.

[47] Sofia Teixeira, G Burwell, A Castaing, D Gonzalez, RS Conlan, and OJ Guy. Epitaxial graphene immunosensor for human chorionic gonadotropin. *Sensors and Actuators B: Chemical*, 190:723–729, 2014.

[48] Z Tehrani, G Burwell, MA Mohd Azmi, A Castaing, R Rickman, J Almarashi, P Dunstan, A Miran Beigi, SH Doak, and OJ Guy. Generic epitaxial graphene biosensors for ultrasensitive detection of cancer risk biomarker. *2D Materials*, 1(2):025004, 2014.

[49] Jinglei Ping, Ramya Vishnubhotla, Amey Vrudhula, and AT Charlie Johnson. Scalable production of high-sensitivity, label-free dna biosensors based on back-gated graphene field effect transistors. *ACS nano*, 10(9):8700–8704, 2016.

[50] Cheng Wang, Yijun Li, Yibo Zhu, Xiaohong Zhou, Qiao Lin, and Miao He. High-κ solid-gate transistor configured graphene biosensor with fully integrated structure and enhanced sensitivity. *Advanced Functional Materials*, 26(42):7668–7678, 2016.

[51] Shicai Xu, Jian Zhan, Baoyuan Man, Shouzhen Jiang, Weiwei Yue, Shoubao Gao, Chengang Guo, Hanping Liu, Zhenhua Li, Jihua Wang, et al. Real-time reliable determination of binding kinetics of dna hybridization using a multi-channel graphene biosensor. *Nature communications*, 8:14902, 2017.

[52] Gaurav Singh, Anshul Choudhary, D Haranath, Amish G Joshi, Nahar Singh, Sukhvir Singh, and Renu Pasricha. Zno decorated luminescent graphene as a potential gas sensor at room temperature. *Carbon*, 50(2):385–394, 2012.

[53] Lin Zhou, Hongju Mao, Chunyan Wu, Lin Tang, Zhenhua Wu, Hao Sun, Honglian Zhang, Hongbo Zhou, Chunping Jia, Qinghui Jin, et al. Label-free graphene biosensor targeting cancer molecules based on non-covalent modification. *Biosensors and Bioelectronics*, 87:701–707, 2017.

[54] Ashish Pandey, Yasar Gurbuz, Volkan Ozguz, Javed H Niazi, and Anjum Qureshi. Graphene-interfaced electrical biosensor for label-free and sensitive detection of foodborne pathogenic e. coli o157:h7. *Biosensors and Bioelectronics*, 91:225–231, 2017.

[55] Savannah Afsahi, Mitchell B Lerner, Jason M Goldstein, Joo Lee, Xiaoling Tang, Dennis A Bagarozzi Jr, Deng Pan, Lauren Locascio, Amy Walker, Francie Barron, et al. Novel graphene-based biosensor for early detection of zika virus infection. *Biosensors and Bioelectronics*, 100:85–88, 2018.

[56] Nan Lei, Pengfei Li, Wei Xue, and Jie Xu. Simple graphene chemiresistors as ph sensors: fabrication and characterization. *Measurement science and technology*, 22(10):107002, 2011.

[57] Priscilla Kailian Ang, Wei Chen, Andrew Thye Shen Wee, and Kian Ping Loh. Solution-gated epitaxial graphene as ph sensor. *Journal of the American Chemical Society*, 130(44):14392–14393, 2008.

[58] Yasuhide Ohno, Kenzo Maehashi, Yusuke Yamashiro, and Kazuhiko Matsumoto. Electrolyte-gated graphene field-effect transistors for detecting ph and protein adsorption. *Nano letters*, 9(9):3318–3322, 2009.

[59] Benjamin Mailly-Giacchetti, Allen Hsu, Han Wang, Vincenzo Vinciguerra, Francesco Pappalardo, Luigi Occhipinti, Elio Guidetti, Salvatore Coffa, Jing Kong, and Tomás Palacios. ph sensing properties of graphene solution-gated field-effect transistors. *Journal of Applied Physics*, 114(8):084505, 2013.

[60] J-H Chen, Ci Jang, Shaffique Adam, MS Fuhrer, Ellen D Williams, and Masa Ishigami. Charged-impurity scattering in graphene. *Nature physics*, 4(5):377, 2008.

[61] Yibo Zhu, Cheng Wang, Nicholas Petrone, Jaeeun Yu, Colin Nuckolls, James Hone, and Qiao Lin. A solid-gated graphene fet sensor for ph measurements. In *2015 28th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, pages 869–872. IEEE, 2015.

[62] Pietro Salvo, Bernardo Melai, Nicola Calisi, Clara Paoletti, Francesca Bellagambi, Arno Kirchhain, Maria Giovanna Trivella, Roger Fuoco, and Fabio

Di Francesco. Graphene-based devices for measuring ph. *Sensors and Actuators B: Chemical*, 256:976–991, 2018.

[63] Wenjing Yuan and Gaoquan Shi. Graphene-based gas sensors. *Journal of Materials Chemistry A*, 1(35):10078–10091, 2013.

[64] Ciril Reiner-Rozman, Melanie Larisika, Christoph Nowak, and Wolfgang Knoll. Graphene-based liquid-gated field effect transistor for biosensing: Theory and experiments. *Biosensors and Bioelectronics*, 70:21–27, 2015.

[65] Brett R Goldsmith, Lauren Locascio, Yingning Gao, Mitchell Lerner, Amy Walker, Jeremy Lerner, Jayla Kyaw, Angela Shue, Savannah Afsahi, Deng Pan, et al. Digital biosensing by foundry-fabricated graphene sensors. *Scientific reports*, 9(1):434, 2019.

[66] Hediyeh Karimi, Rasoul Rahmani, Reza Mashayekhi, Leyla Ranjbari, Amir H Shirdel, Niloofar Haghighian, Parisa Movahedi, Moein Hadiyan, and Razali Ismail. Analytical development and optimization of a graphene–solution interface capacitance model. *Beilstein journal of nanotechnology*, 5(1):603–609, 2014.

[67] Giuseppe Tarabella, Clara Santato, Sang Yoon Yang, Salvatore Iannotta, George G Malliaras, and Fabio Cicoira. Effect of the gate electrode on the response of organic electrochemical transistors. *Applied Physics Letters*, 97(12):205, 2010.

[68] Wangyang Fu, Cornelia Nef, Alexey Tarasov, Mathias Wipf, Ralph Stoop, Oren Knopfmacher, Markus Weiss, Michel Calame, and Christian Schönenberger. Sensing with liquid-gated graphene field-effect transistors. In *2012 12th IEEE International Conference on Nanotechnology (IEEE-NANO)*, pages 1–2. IEEE, 2012.

[69] Haizhou Huang, Shi Su, Nan Wu, Hao Wan, Shu Wan, Hengchang Bi, and Litao Sun. Graphene-based sensors for human health monitoring. *Frontiers in Chemistry*, 7, 2019.

[70] Hamed Hosseini Bay, Richard Vo, Xiaochuan Dai, Huan-Hsuan Hsu, Zhiming Mo, Siran Cao, Wenyi Li, Fiorenzo G Omenetto, and Xiaocheng Jiang. Hydrogel gate graphene field-effect transistors as multiplexed biosensors. *Nano letters*, 19(4):2620–2626, 2019.

[71] Yao Zhang, Rui Ma, Xue V Zhen, Yogish C Kudva, Philippe Bühlmann, and Steven J Koester. Capacitive sensing of glucose in electrolytes using graphene quantum capacitance varactors. *ACS applied materials & interfaces*, 9(44):38863–38869, 2017.

[72] Jack Allen Alexander-Webber, Abhay Abhimanyu Sagade, Adrianus I Aria, Zenas A Van Veldhoven, Philipp Braeuninger-Weimer, Ruizhi Wang, Andrea Cabrero-Vilatela, Marie-Blandine Martin, Jinggao Sui, Malcolm R Connolly, et al. Encapsulation of graphene transistors and vertical device integration by interface engineering with atomic layer deposited oxide. *2D Materials*, 2017.

[73] Yuyan Shao, Jun Wang, Hong Wu, Jun Liu, Ilhan A Aksay, and Yuehe Lin. Graphene based electrochemical sensors and biosensors: a review. *Electroanalysis: An International Journal Devoted to Fundamental and Practical Aspects of Electroanalysis*, 22(10):1027–1036, 2010.

[74] PJ Britto, KSV Santhanam, and PM Ajayan. Carbon nanotube electrode for oxidation of dopamine. *Bioelectrochemistry and Bioenergetics*, 41(1):121–125, 1996.

[75] Xinhuang Kang, Jun Wang, Hong Wu, Jun Liu, Ilhan A Aksay, and Yuehe Lin. A graphene-based electrochemical sensor for sensitive detection of paracetamol. *Talanta*, 81(3):754–759, 2010.

[76] Martin Pumera, Adriano Ambrosi, Alessandra Bonanni, Elaine Lay Khim Chng, and Hwee Ling Poh. Graphene for electrochemical sensing and biosensing. *TrAC Trends in Analytical Chemistry*, 29(9):954–965, 2010.

[77] Ying Wang, Zhaohui Li, Jun Wang, Jinghong Li, and Yuehe Lin. Graphene and graphene oxide: biofunctionalization and applications in biotechnology. *Trends in biotechnology*, 29(5):205–212, 2011.

[78] Carrie Haslam, Samar Damiati, Toby Whitley, Paul Davey, Emmanuel Ifeachor, and Shakil Awan. Label-free sensors based on graphene field-effect transistors for the detection of human chorionic gonadotropin cancer risk biomarker. *Diagnostics*, 8(1):5, 2018.

[79] Nathaniel S Green and Michael L Norton. Interactions of dna with graphene and sensing applications of graphene field-effect transistor devices: A review. *Analytica chimica acta*, 853:127–142, 2015.

[80] Liping Chen, Linjun Wang, Zhigang Shuai, and David Beljonne. Energy level alignment and charge carrier mobility in noncovalently functionalized graphene. *The Journal of Physical Chemistry Letters*, 4(13):2158–2165, 2013.

[81] Tibor Pasinszki, Melinda Krebsz, Thanh Tran Tung, and Dusan Losic. Carbon nanomaterial based biosensors for non-invasive detection of cancer and disease biomarkers for clinical diagnosis. *Sensors*, 17(8):1919, 2017.

[82] Hong Ying Mao, Yun Hao Lu, Jia Dan Lin, Shu Zhong, Andrew Thye Shen Wee, and Wei Chen. Manipulating the electronic and chemical properties of graphene via molecular functionalization. *Progress in Surface Science*, 88(2):132–159, 2013.

[83] Vasilios Georgakilas, Michal Otyepka, Athanasios B Bourlinos, Vimlesh Chandra, Namdong Kim, K Christian Kemp, Pavel Hobza, Radek Zboril, and Kwang S Kim. Functionalization of graphene: covalent and non-covalent ap-

proaches, derivatives and applications. *Chemical reviews*, 112(11):6156–6214, 2012.

[84] Nako Nakatsuka, Kyung-Ae Yang, John M Abendroth, Kevin M Cheung, Xiaobin Xu, Hongyan Yang, Chuanzhen Zhao, Bowen Zhu, You Seung Rim, Yang Yang, et al. Aptamer field-effect-transistors overcome debye length limitations for small-molecule sensing. *Science*, 362(6412):319–324, 2018.

[85] Wenhu Zhou, Po-Jung Jimmy Huang, Jinsong Ding, and Juewen Liu. Aptamer-based biosensors for biomedical diagnostics. *Analyst*, 139(11):2627–2640, 2014.

[86] Ning Gao, Teng Gao, Xiao Yang, Xiaochuan Dai, Wei Zhou, Anqi Zhang, and Charles M Lieber. Specific detection of biomolecules in physiological solutions using graphene transistor biosensors. *Proceedings of the National Academy of Sciences*, 113(51):14633–14638, 2016.

[87] Qiaojuan Gong, Haixia Han, Haiying Yang, Meiling Zhang, Xiaoling Sun, Yunxia Liang, Zhaorong Liu, Wenchan Zhang, and Jinli Qiao. Sensitive electrochemical dna sensor for the detection of hiv based on a polyaniline/graphene nanocomposite. *Journal of Materiomics*, 5(2):313–319, 2019.

[88] Roey Elnathan, Moria Kwiat, Alexander Pevzner, Yoni Engel, Larisa Burstein, Artium Khatchtourints, Amir Lichtenstein, Raisa Kantaev, and Fernando Patolsky. Biorecognition layer engineering: overcoming screening limitations of nanowire-based fet devices. *Nano letters*, 12(10):5245–5254, 2012.

[89] Siva Kumar Krishnan, Eric Singh, Pragya Singh, Meyya Meyyappan, and Hari Singh Nalwa. A review on graphene-based nanocomposites for electrochemical and fluorescent biosensors. *RSC advances*, 9(16):8778–8881, 2019.

[90] Shuaihui Li, Yashen Ma, Yongkang Liu, Gu Xin, Minghua Wang, Zhihong Zhang, and Zhongyi Liu. Electrochemical sensor based on a three dimensional nanostructured mos2 nanosphere-pani/reduced graphene oxide composite for

simultaneous detection of ascorbic acid, dopamine, and uric acid. *RSC advances*, 9(6):2997–3003, 2019.

[91] Biwu Liu, Po-Jung Jimmy Huang, Erin Y Kelly, and Juewen Liu. Graphene oxide surface blocking agents can increase the dna biosensor sensitivity. *Biotechnology journal*, 11(6):780–787, 2016.

[92] Maria F Pantano, Erica Iacob, Antonino Picciotto, Benno Margesin, Alba Centeno, Amaia Zurutuza, Costas Galiotis, Nicola M Pugno, and Giorgio Speranza. Investigation of charges-driven interaction between graphene and different sio2 surfaces. *Carbon*, 2019.

[93] Ke Zou, Xia Hong, Derek Keefer, and Jun Zhu. Deposition of high-quality hfo2 on graphene and the effect of remote oxide phonon scattering. *Physical review letters*, 105(12):126601, 2010.

[94] Timothy J Lyon, Jonas Sichau, August Dorn, Alba Centeno, Amaia Pesquera, Amaia Zurutuza, and Robert H Blick. Probing electron spin resonance in monolayer graphene. *Physical review letters*, 119(6):066802, 2017.

[95] Luca Banszerus, Michael Schmitz, Stephan Engels, Jan Dauber, Martin Oellers, Federica Haupt, Kenji Watanabe, Takashi Taniguchi, Bernd Beschoten, and Christoph Stampfer. Ultrahigh-mobility graphene devices from chemical vapor deposition on reusable copper. *Science advances*, 1(6):e1500222, 2015.

[96] Sana Mzali, Alberto Montanaro, Stéphane Xavier, Bernard Servet, Jean-Paul Mazellier, Odile Bezencenet, Pierre Legagneux, Maëlis Piquemal-Banci, Regina Galceran, Bruno Dlubak, et al. Stabilizing a graphene platform toward discrete components. *Applied Physics Letters*, 109(25):253110, 2016.

[97] K Nagashio, T Yamashita, T Nishimura, K Kita, and A Toriumi. Electrical transport properties of graphene on sio2 with specific surface structures. *Journal of Applied Physics*, 110(2):024513, 2011.

[98] Wenjuan Zhu, Deborah Neumayer, Vasili Perebeinos, and Phaedon Avouris. Silicon nitride gate dielectrics and band gap engineering in graphene layers. *Nano letters*, 10(9):3572–3576, 2010.

[99] Sung Kyu Jang, Jaeho Jeon, Su Min Jeon, Young Jae Song, and Sungjoo Lee. Effects of dielectric material properties on graphene transistor performance. *Solid-State Electronics*, 109:8–11, 2015.

[100] Ryan Michael Bigham. Development of process technology for silicon and graphene biosensor devices. Technical report, Swansea University, 2019.

[101] Santanu Das, Debrupa Lahiri, Arvind Agarwal, and Wonbong Choi. Interfacial bonding characteristics between graphene and dielectric substrates. *Nanotechnology*, 25(4):045707, 2014.

[102] Wonsuk Jung, Joonkyu Park, Taeshik Yoon, Taek-Soo Kim, Soohyun Kim, and Chang-Soo Han. Prevention of water permeation by strong adhesion between graphene and sio2 substrate. *Small*, 10(9):1704–1711, 2014.

[103] XF Fan, WT Zheng, Viorel Chihaia, ZX Shen, and Jer-Lai Kuo. Interaction between graphene and the surface of sio2. *Journal of Physics: Condensed Matter*, 24(30):305004, 2012.

[104] Zengguang Cheng, Qiaoyu Zhou, Chenxuan Wang, Qiang Li, Chen Wang, and Ying Fang. Toward intrinsic graphene surfaces: a systematic study on thermal annealing and wet-chemical treatment of sio2-supported graphene devices. *Nano letters*, 11(2):767–771, 2011.

[105] Marc D Levenson, NS Viswanathan, and Robert A Simpson. Improving resolution in photolithography with a phase-shifting mask. *IEEE Transactions on electron devices*, 29(12):1828–1836, 1982.

[106] Joseph L Lenhart, Daniel A Fischer, Sharadha Sambasivan, Eric K Lin, Ronald L Jones, Christopher L Soles, Wen-li Wu, Dario L Goldfarb, and

Marie Angelopoulos. X-ray absorption spectroscopy to probe surface composition and surface deprotection in photoresist films. *Langmuir*, 21(9):4007–4015, 2005.

[107] Bing Li, Genhua Pan, Ahmed Suhail, Kamrul Islam, Neil Avent, and Paul Davey. Deep uv hardening of photoresist for shaping of graphene and lift-off fabrication of back-gated field effect biosensors by ion-milling and sputter deposition. *Carbon*, 118:43–49, 2017.

[108] Mariana C Prado, Deep Jariwala, Tobin J Marks, and Mark C Hersam. Optimization of graphene dry etching conditions via combined microscopic and spectroscopic analysis. *Applied Physics Letters*, 102(19):193111, 2013.

[109] Yixuan Wu, Haihua Tao, Shubin Su, Huan Yue, Hao Li, Ziyu Zhang, Zhenhua Ni, and Xianfeng Chen. Patterning graphene film by magnetic-assisted uv ozonation. *Scientific reports*, 7:46583, 2017.

[110] Wei Xiong, Yun Shen Zhou, Wen Jia Hou, Li Jia Jiang, Yang Gao, Li Sha Fan, Lan Jiang, Jean Francois Silvain, and Yong Feng Lu. Direct writing of graphene patterns on insulating substrates under ambient conditions. *Scientific Reports*, 4(1), May 2014.

[111] A Nath, M Currie, VD Wheeler, MJ Tadjer, AD Koehler, ZR Robinson, K Sridhara, SC Hernandez, JA Wollmershauser, JT Robinson, et al. Towards pristine graphene-metal interface and microstructures: Laser assisted direct patterning on epitaxial graphene. *arXiv preprint arXiv:1411.5114*, 2014.

[112] Zhaoli Gao, Hojin Kang, Carl H Naylor, Frank Streller, Pedro Ducos, Madeline D Serrano, Jinglei Ping, Jonathan Zauberman, Robert W Carpick, Ying-Jun Wang, et al. Scalable production of sensor arrays based on high-mobility hybrid graphene field effect transistors. *ACS applied materials & interfaces*, 8(41):27546–27552, 2016.

[113] V Vyurkov and V Ryzhii. Effect of the coulomb scattering on graphene conductivity. *JETP letters*, 88(5):322–325, 2008.

[114] Behiye Boyarbay Kantar, Muhittin Ozturk, and Hidayet Cetin. The effects of lithographic residues and humidity on graphene field effect devices. *Bulletin of Materials Science*, 40(1):239–245, 2017.

[115] Yung-Chang Lin, Chun-Chieh Lu, Chao-Huei Yeh, Chuanhong Jin, Kazu Suenaga, and Po-Wen Chiu. Graphene annealing: how clean can it be? *Nano letters*, 12(1):414–419, 2011.

[116] Wei Li, Yiran Liang, Dangmin Yu, Lianmao Peng, Kurt P Pernstich, Tian Shen, AR Hight Walker, Guangjun Cheng, Christina A Hacker, Curt A Richter, et al. Ultraviolet/ozone treatment to reduce metal-graphene contact resistance. *Applied Physics Letters*, 102(18):183110, 2013.

[117] Ning C. Wang, Enrique A. Carrion, Maryann C. Tung, and Eric Pop. Reducing graphene device variability with yttrium sacrificial layers. *Applied Physics Letters*, 110(22):223106, May 2017.

[118] Zhangfu Chen, Yiru Li, Bo Wang, Bin Wei, and Lianqiao Yang. Enhanced photolithography with al film insertion for large-scale patterning of cvd graphene. *Optical Materials Express*, 8(8):2403–2414, 2018.

[119] Hongmei Liu, Hisashi Kondo, and Takahisa Ohno. Contact effects of nickel and copper on electron transport through graphene. *Physical Review B*, 86(15):155434, 2012.

[120] Zhihong Chen and Joerg Appenzeller. Gate modulation of graphene contacts-on the scaling of graphene fets. In *2009 Symposium on VLSI Technology*, pages 128–129. IEEE, 2009.

[121] Seyoung Kim, Junghyo Nah, Insun Jo, Davood Shahrjerdi, Luigi Colombo, Zhen Yao, Emanuel Tutuc, and Sanjay K Banerjee. Realization of a high mo-

bility dual-gated graphene field-effect transistor with al2o 3 dielectric. *Applied Physics Letters*, 94(6):062107, 2009.

[122] Tao Chu and Zhihong Chen. Understanding the electrical impact of edge contacts in few-layer graphene. *Acs Nano*, 8(4):3584–3589, 2014.

[123] Aaron D Franklin, Shu-Jen Han, Ageeth A Bol, and Vasili Perebeinos. Double contacts for improved performance of graphene transistors. *IEEE Electron Device Letters*, 33(1):17–19, 2011.

[124] Cheng Gong, Stephen McDonnell, Xiaoye Qin, Angelica Azcatl, Hong Dong, Yves J Chabal, Kyeongjae Cho, and Robert M Wallace. Realistic metal–graphene contact structures. *ACS nano*, 8(1):642–649, 2013.

[125] DW Yue, CH Ra, XC Liu, DY Lee, and Won Jong Yoo. Edge contacts of graphene formed by using a controlled plasma treatment. *Nanoscale*, 7(2):825–831, 2015.

[126] Teresa Cusati, Gianluca Fiori, Amit Gahoi, Vikram Passi, Max C Lemme, Alessandro Fortunelli, and Giuseppe Iannaccone. Electrical properties of graphene-metal contacts. *Scientific reports*, 7(1):5109, 2017.

[127] GAKPA Giovannetti, PA Khomyakov, G Brocks, VM vd Karpan, J Van den Brink, and Paul J Kelly. Doping graphene with metal contacts. *Physical review letters*, 101(2):026803, 2008.

[128] CX Li and PT Lai. Wide-bandgap high-k y2o3 as passivating interlayer for enhancing the electrical properties and high-field reliability of n-ge metal-oxide-semiconductor capacitors with high-k hftio gate dielectric. *Applied Physics Letters*, 95(2):022910, 2009.

[129] Charles Mackin, Lucas H Hess, Allen Hsu, Yi Song, Jing Kong, Jose Antonio Garrido, and Tomás Palacios. A current-voltage model for graphene electrolyte-gated field-effect transistors. *IEEE Transactions on Electron Devices*, 61(12):3971–3977, 2014.

[130] Mir Hadi Jazayeri, Hamed Amani, Ali Akbar Pourfatollah, Hamidreza Pazoki-Toroudi, and Bijan Sedighimoghaddam. Various methods of gold nanoparticles (gnps) conjugation to antibodies. *Sensing and bio-sensing research*, 9:17–22, 2016.

[131] Geunsoo Jang, Woongbin Yim, YH Ahn, Soonil Lee, and Ji-Yong Park. Control of device characteristics by passivation of graphene field effect transistors with polymers. *Current Applied Physics*, 16(11):1506–1510, 2016.

[132] Chang Goo Kang, Young Gon Lee, Sang Kyung Lee, Eunji Park, Chunhum Cho, Sung Kwan Lim, Hyeon Jun Hwang, and Byoung Hun Lee. Mechanism of the effects of low temperature al2o3 passivation on graphene field effect transistors. *Carbon*, 53:182–187, 2013.

[133] Jiawei Tu, Ying Gan, Tao Liang, Qiongwen Hu, Qian Wang, Tianling Ren, Qiyong Sun, Hao Wan, and Ping Wang. Graphene fet array biosensor based on ssdna aptamer for ultrasensitive hg^{2+} detection in environmental pollutants. *Frontiers in chemistry*, 6, 2018.

[134] Jeffrey Abbott, Donhee Ham, and Guangyu Xu. All-electrical graphene dna sensor array. In *Biosensors and Biodetection*, pages 169–187. Springer, 2017.

[135] Albert F Rigosi, Chieh-I Liu, Bi Yi Wu, Hsin-Yen Lee, Mattias Kruskopf, Yanfei Yang, Heather M Hill, Jiuning Hu, Emily G Bittle, Jan Obrzut, et al. Examining epitaxial graphene surface conductivity and quantum hall device stability with parylene passivation. *Microelectronic engineering*, 194:51–55, 2018.

[136] Sunwoo Lee, Changyao Chen, Vikram V Deshpande, Gwan-Hyoung Lee, Ilkyu Lee, Michael Lekas, Alexander Gondarenko, Young-Jun Yu, Kenneth Shepard, Philip Kim, et al. Su-8 clamped cvd graphene drum resonators. *arXiv preprint arXiv:1612.04279*, 2016.

[137] David A Deen, James G Champlain, and Steven J Koester. Multilayer hfo2/tio2 gate dielectric engineering of graphene field effect transistors. *Applied Physics Letters*, 103(7):073504, 2013.

[138] Ting Ting Song, Ming Yang, Martin Callsen, Qing Yun Wu, Jun Zhou, Shao Feng Wang, Shi Jie Wang, and Yuan Ping Feng. Graphene stabilized high-κ dielectric y2o3 (111) monolayers and their interfacial properties. *RSC Advances*, 5(102):83588–83593, 2015.

[139] Inanc Meric, Cory R Dean, Nicholas Petrone, Lei Wang, James Hone, Philip Kim, and Kenneth L Shepard. Graphene field-effect transistors based on boron-nitride dielectrics. *Proceedings of the IEEE*, 101(7):1609–1619, 2013.

[140] Sang-Min Kim, Youngji Cho, Jae-Hyun Kim, Hak-Joo Lee, Jun-Mo Yang, Seung-Mo Lee, et al. Healing defective cvd-graphene through vapor phase treatment. *Nanoscale*, 6(11):5639–5644, 2014.

[141] Mukul Sonker, Vishal Sahore, and Adam T Woolley. Recent advances in microfluidic sample preparation and separation techniques for molecular biomarker analysis: A critical review. *Analytica chimica acta*, 986:1–11, 2017.

[142] Georgia-Paraskevi Nikoleli, Christina G Siontorou, Dimitrios P Nikolelis, Spyridoula Bratakou, Stephanos Karapetis, and Nikolaos Tzamtzis. Biosensors based on microfluidic devices lab-on-a-chip and microfluidic technology. In *Nanotechnology and Biosensors*, pages 375–394. Elsevier, 2018.

[143] Younan Xia and George M Whitesides. Soft lithography. *Annual review of materials science*, 28(1):153–184, 1998.

[144] Hoang-Tuan Nguyen, Ha Thach, Emmanuel Roy, Khon Huynh, and Cecile Perrault. Low-cost, accessible fabrication methods for microfluidics research in low-resource settings. *Micromachines*, 9(9):461, 2018.

[145] Usama M Attia, Silvia Marson, and Jeffrey R Alcock. Micro-injection moulding of polymer microfluidic devices. *Microfluidics and nanofluidics*, 7(1):1, 2009.

[146] Pulak Nath, Derek Fung, Yuliya A Kunde, Ahmet Zeytun, Brittany Branch, and Greg Goddard. Rapid prototyping of robust and versatile microfluidic components using adhesive transfer tapes. *Lab on a Chip*, 10(17):2286–2291, 2010.

[147] David I Walsh III, David S Kong, Shashi K Murthy, and Peter A Carr. Enabling microfluidics: from clean rooms to makerspaces. *Trends in biotechnology*, 35(5):383–392, 2017.

[148] David J Kinahan, Lourdes AN Julius, Cor Schoen, Tanja Dreo, and Jens Ducrée. Automated dna purification and multiplexed lamp assay preparation on a centrifugal microfluidic "lab-on-a-disc" platform. In *2018 IEEE Micro Electro Mechanical Systems (MEMS)*, pages 1134–1137. IEEE, 2018.

[149] Jiquan Yang, Kelou Li, Li Zhu, Wencheng Tang, et al. Fabrication of pdms microfluidic devices with 3d wax jetting. *Rsc Advances*, 7(6):3313–3320, 2017.

[150] Stephanie Knowlton, Chu Hsiang Yu, Fulya Ersoy, Sharareh Emadi, Ali Khademhosseini, and Savas Tasoglu. 3d-printed microfluidic chips with patterned, cell-laden hydrogel constructs. *Biofabrication*, 8(2):025019, 2016.

[151] Niall P Macdonald, Joan M Cabot, Petr Smejkal, Rosanne M Guijt, Brett Paull, and Michael C Breadmore. Comparing microfluidic performance of three-dimensional (3d) printing platforms. *Analytical chemistry*, 89(7):3858–3866, 2017.

[152] Koji Sugioka, Jian Xu, Dong Wu, Yasutaka Hanada, Zhongke Wang, Ya Cheng, and Katsumi Midorikawa. Femtosecond laser 3d micromachining: a powerful tool for the fabrication of microfluidic, optofluidic, and electrofluidic devices based on glass. *Lab on a Chip*, 14(18):3447–3458, 2014.

[153] James L Tullis. *Blood cells and plasma proteins: their state in nature*. Elsevier, 2013.

[154] Walter H Seegers. *Blood clotting enzymology*. Academic Press, 2013.

[155] Shibnath Ghatak, Edward V Maytin, Judith A Mack, Vincent C Hascall, Ilia Atanelishvili, Ricardo Moreno Rodriguez, Roger R Markwald, and Suniti Misra. Roles of proteoglycans and glycosaminoglycans in wound healing and fibrosis. *International journal of cell biology*, 2015, 2015.

[156] Karin Fijnvandraat, Marjon H Cnossen, Frank WG Leebeek, and Marjolein Peters. Diagnosis and management of haemophilia. *Bmj*, 344:e2707, 2012.

[157] ECM Van Gorp, Catharina Suharti, H Ten Cate, WMV Dolmans, Jos WM van der Meer, JW Ten Cate, and DPM Brandjes. Infectious diseases and coagulation disorders. *The Journal of infectious diseases*, 180(1):176–186, 1999.

[158] Colleen M Johnson, Leila Mureebe, and Donald Silver. Hypercoagulable states: a review. *Vascular and endovascular surgery*, 39(2):123–133, 2005.

[159] Kenneth Bauer. Hypercoagulable states. *Hematology*, 10(sup1):39–39, 2005.

[160] Charalampos Seretis, Haney Youssef, and Mark Chapman. Hypercoagulation in colorectal cancer: what can platelet indices tell us? *Platelets*, 26(2):114–118, 2015.

[161] Anna Falanga. Mechanisms of hypercoagulation in malignancy and during chemotherapy. *Pathophysiology of Haemostasis and Thrombosis*, 28(Suppl. 3):50–60, 1998.

[162] Glenn P Gravlee, Sunil Arora, Sidney W Lavender, Stephen A Mills, Allen S Hudspeth, A Robert Cordell, Robert L James, Joni K Brockschmidt, and John J Stuart. Predictive value of blood clotting tests in cardiac surgical patients. *The Annals of thoracic surgery*, 58(1):216–221, 1994.

[163] W Miesbach, J Schenk, S Alesci, and E Lindhoff-Last. Comparison of the fibrinogen clauss assay and the fibrinogen pt derived method in patients with dysfibrinogenemia. *Thrombosis research*, 126(6):e428–e433, 2010.

[164] B Boneu, G Bes, H Pelzer, P Sie, and H Boccalon. D-dimers, thrombin antithrombin iii complexes and prothrombin fragments 1+ 2: diagnostic value in clinically suspected deep vein thrombosis. *Thrombosis and haemostasis*, 65(01):028–032, 1991.

[165] Oliver Königsbrügge, Silvia Koder, Julia Riedl, Simon Panzer, Ingrid Pabinger, and Cihan Ay. A new measure for in vivo thrombin activity in comparison with in vitro thrombin generation potential in patients with hyper-and hypocoagulability. *Clinical and experimental medicine*, 17(2):251–256, 2017.

[166] Grant Saltzgaber, Peter M Wojcik, Tal Sharf, Matthew R Leyden, Jenna L Wardini, Christopher A Heist, Adeniyi A Adenuga, Vincent T Remcho, and Ethan D Minot. Scalable graphene field-effect sensors for specific protein detection. *Nanotechnology*, 24(35):355502, 2013.

[167] Yanping Wang, Yinghong Xiao, Xiaoling Ma, Na Li, and Xiaodi Yang. Label-free and sensitive thrombin sensing on a molecularly grafted aptamer on graphene. *Chemical Communications*, 48(5):738–740, 2012.

[168] Jennie Z Ma, Jim Ebben, Hong Xia, and Allan J Collins. Hematocrit level and associated mortality in hemodialysis patients. *Journal of the American Society of Nephrology*, 10(3):610–619, 1999.

[169] Witold Szymon Mielczarek, EA Obaje, TT Bachmann, and Maïwenn Kersaudy-Kerhoas. Microfluidic blood plasma separation for medical diagnostics: is it worth it? *Lab on a Chip*, 16(18):3441–3448, 2016.

[170] Yuchao Chen, Mengxi Wu, Liqiang Ren, Jiayang Liu, Pamela H Whitley, Lin Wang, and Tony Jun Huang. High-throughput acoustic separation of platelets from whole blood. *Lab on a Chip*, 16(18):3466–3472, 2016.

[171] Crispin Szydzik, Khashayar Khoshmanesh, Arnan Mitchell, and Christian Karnutsch. Microfluidic platform for separation and extraction of plasma from whole blood using dielectrophoresis. *Biomicrofluidics*, 9(6):064120, 2015.

[172] Ki-Ho Han and A Bruno Frazier. Paramagnetic capture mode magnetophoretic microseparator for high efficiency blood cell separations. *Lab on a Chip*, 6(2):265–273, 2006.

[173] Da-Han Kuan, Chia-Chien Wu, Wei-Yu Su, and Nien-Tsu Huang. A microfluidic device for simultaneous extraction of plasma, red blood cells, and on-chip white blood cell trapping. *Scientific reports*, 8(1):15345, 2018.

[174] Ivan K Dimov, Lourdes Basabe-Desmonts, Jose L Garcia-Cordero, Benjamin M Ross, Antonio J Ricco, and Luke P Lee. Stand-alone self-powered integrated microfluidic blood analysis system (simbas). *Lab on a Chip*, 11(5):845–850, 2011.

[175] John A Davis, David W Inglis, Keith J Morton, David A Lawrence, Lotien R Huang, Stephen Y Chou, James C Sturm, and Robert H Austin. Deterministic hydrodynamics: taking blood apart. *Proceedings of the National Academy of Sciences*, 103(40):14779–14784, 2006.

[176] Siddhartha Tripathi, YV BalaVarun Kumar, Amit Agrawal, Amit Prabhakar, and Suhas S Joshi. Microdevice for plasma separation from whole human blood using bio-physical and geometrical effects. *Scientific reports*, 6:26749, 2016.

[177] Elodie Sollier, Myriam Cubizolles, Yves Fouillet, and Jean-Luc Achard. Fast and continuous plasma extraction from whole human blood based on expanding cell-free layer devices. *Biomedical microdevices*, 12(3):485–497, 2010.

[178] Sung Yang, Akif Ündar, and Jeffrey D Zahn. A microfluidic device for continuous, real time blood plasma separation. *Lab on a Chip*, 6(7):871–880, 2006.

[179] Myounggon Kim, Seung Mo Jung, Kyeong-Hwan Lee, Yang Jun Kang, and Sung Yang. A microfluidic device for continuous white blood cell separation and lysis from whole blood. *Artificial organs*, 34(11):996–1002, 2010.

[180] Sowmya Viswanathan, Tharangattu N Narayanan, Kiana Aran, Kathryn D Fink, Jacobo Paredes, Pulickel M Ajayan, Slawomir Filipek, Przemyslaw Miszta, H Cumhur Tekin, Fatih Inci, et al. Graphene protein field effect biosensors: glucose sensing. *Materials Today*, 18(9):513–522, 2015.

Chapter 3

Materials & Methods

3.1 Graphene Sensor Fabrication & Optimisation

The following chapter will describe the main materials and methods used within this work. Where appropriate, further details of equipment functionality can be found in the Appendix.

The device fabrication focused on two main process routes:

- "Pre-Transfer", graphene is grown and transferred onto the base substrate before device fabrication.

- "Post-Transfer", the device fabricated on the base substrate followed by graphene transfer onto the surface.

3.1.1 Graphene Growth & Transfer

For Pre-Transfer device fabrication, monolayer graphene grown by chemical vapour deposition (CVD) and transferred to a circular 100 mm diameter substrate of SiO_2 (300 nm) on Si (525 μm) by a wet transfer process was purchased from Graphenea Inc (Spain).

For Post-Transfer device fabrication, monolayer graphene CVD grown and transferred onto 100 mm wafer of fabricated devices, in 10 mm x 10 mm patches or 10 mm x 60 mm strips by wet transfer process was purchased from HexagonFab Ltd (UK).

3.1.2 Base Substrate

Silicon wafers with thin-film coatings and oxides were purchased from Si-Mat Silicon Materials GmbH. Bulk Silicon; 100 mm diameter, orientation <100>, Single Side Polished, 525 μm thickness.

SiO_2 coating: wet thermal growth 300 nm thickness.

Si_3N_4 coating: Low pressure chemical vapour deposition (LPCVD) growth 100 nm

3.1.3 Sensor Design

The design of each sensor and corresponding photomasks within this work were designed using "AutoCAD" software, from the Autodesk Inc. under an education license. A single block was created for a single sensor-based chip. This chip can then be arrayed to fill up any corresponding wafer size (100 mm).

3.1.4 Photomask Purchase

Photomasks were purchased from JD PhotoData UK. Soda Lime 127 mm substrate with chrome pattern resolution of 1 μm and polymer film with chrome ink emulsion achieving 10 μm resolution photomasks were purchased.

Film masks purchased 229 mm x 305 mm film photomasks comprising of 4x designs were cut using a guillotine to 110 mm x 110 mm individual film masks. the film masks were attached to blank 127 mm (5 inch) Soda Lime glass pieces for support using polyamide tape.

3.2 Sample Preparation

The substrate cleaning protocol will depend on the initial surface materials present as well as the intended fabrication process. e.g. if graphene is present on the surface cleaning processes are restricted to solvent-based cleaning as well as thermal

annealing. Compared to a SiO_2 coated Si wafer where full Piranha cleaning as well as O_2 plasma cleaning are available without damaging the substrate.

3.2.1 Solvent Clean

All cleaning steps are vitally important in micro-fabrication to obtain uniform and defect-free microstructures. Cleaning is done to return a sample surface to a known state. This is important when doing any process on the sample. A standard clean-room clean consists of a solvent clean followed by Piranha and HF treatments. solvent clean can be used to strip resist, remove organics and particulates.

The solvent clean process is as follows: The sample is submerged in Acetone (Fisher Scientific, UK) and placed in an ultrasonic sonic bath for 10 minutes. The sample is then submerged in isopropanol (IPA) (Fisher Scientific, UK) placed in an ultrasonic bath for 5 minutes. After 5 minutes The sample is dried with compressed air to remove excess liquid. Finally, the sample is then dehydrated on a hotplate at 150 °C for 20 minutes.

3.2.2 Piranha Clean

Standard Piranha solution is made up of 70% concentrated sulphuric acid (H_2SO_4) to 30% hydrogen peroxide (H_2O_2). This clean is used for removing organics via strong oxidation reactions. It also ensures the removal of any larger particulates such as silicon dust.

The sulphuric acid reduces the organics to carbon and the hydrogen peroxide oxidises the carbon to carbon dioxide (CO_2). The solution can be heated or additional H_2O_2 can be added every 5 minutes over a 20 minute clean period, this additional H_2O_2 causes an exothermic self-heating effect. This clean can form a thin oxide layer on the surface of silicon wafers, the oxide can then be removed in the HF clean. The piranha clean reacts with metals on the surface forming sulphates but this clean is not specifically a metal etching process.

3.2.3 Oxide Removal

Immersing the silicon wafer in hydrofluoric Acid (HF) removes the thin native silicon dioxide (SiO_2) layer and any oxide grown during the Piranha clean. The etch reaction can be seen in equation,

$$SiO_2(s) + 4HF(aq) \rightarrow SiF_4(g) + 2H_2O(l) \tag{3.2.1}$$

Once the oxide is removed, the wafer is removed and rinsed in deionised water (di water). This process is also used for etching thermal and deposited SiO_2.

3.3 Photoresist Removal

3.3.1 AZ Photoresist Removal

The sample is submerged in Acetone for 10 minutes. Followed by submersion in IPA for 5 minutes. The sample surface is then dried with compressed air gun. The sample is then submerged in AZ 100 Remover (Microchemicals GmbH, Germany) for 10 minutes followed by a di H_2O rinse bath and submersion in a second di H_2O bath for 10 minutes. The sample is then removed and the surface is dried with compressed air.

3.3.2 LOR Photoresist Removal & or Lift-Off Solution

The sample is submerged in D-350 remover (Microchemicals GmbH) for 30 minutes on a hot plate with a set temperature of 80 °C. The sample is removed and immediately placed in a secondary bath of D-350 at 80 °C. The wafer is then removed and placed in di H_2O rinse bath followed quickly by submersion in a second di H_2O bath for 10 minutes.

3.4 Annealing

3.4.1 Tube Furnace Annealing

Tube furnace annealing (TFA): PyroTHERM Furnace CES, PyroTHERM (UK). Target annealing temperature between 400 - 500 °C. The furnace tube has an inner diameter of 2 ", samples are loaded onto quartz carrier boats. Each boat can carry 1 " x 2 " sample. The tube was sealed at both ends before argon was flown through the tube at 100 sccm. Once under a vacuum pressure of 10 mTorr, the filament was turned on. Once the set temperature was reached the samples were annealed for 4 hours before the filament was switched off the temperature remained above 300 °C for a further 4 hours during the cool-down process.

3.4.2 Rapid Thermal Annealing

Rapid thermal annealing (RTA): Jipelec Jetfirst RTA, Jipelec ECM USA (USA). Target temperature set at 400 °C. Ramp up rate set at maximum (10 °C/s) with argon flown through the chamber 10 sccm flow rate. The graphene was RTA annealed for 10 minutes, followed by 3 minute ramp-down period.

3.5 Photolithography

3.5.1 Spin Coating

Photoresist spin coating performed using Laurell Spin Coater 200 mm, Laurell (USA)

3.5.2 UV Exposure & Mask Alignment

UV exposure and mask alignment were performed using SUSS MicroTec MA8 mask aligner, SUSS GmbH (Germany). The process of photolithography is explained

further in Appendix 10.1.2. Photolithography is performed using 100 mm wafer vacuum chuck and 127 mm quartz photomask.

3.5.3 Positive Photoresist Protocols

The standard Pre-Transfer fabrication process developed at Swansea University originally used AZ 6632 (Microchemicals GmbH, Germany) photoresist. This product line has been removed by Microchemcals GmbH, recommended replacement AZ 5214E h-line (310 - 420 nm) multi-tone photoresist. Some test devices were also fabricated using Microposit S1813 (DOW) the top layer of the bi-layer photoresist system used for metal lift-off procedure.

A combination of LOR 5A (MicroChem Corp., USA) and Microposit S1813 is used as a bi-layer photoresist system for metal lift-off. An explanation of the bi-layer metal lift-off system can be found in the appendix section 10.1.3.

Protocol for AZ 6632

1. Dehydrate Step: Graphene coated wafer placed on a hot plate at 130 °C for 15 minutes.

2. Spin Coat Step: Two-step spin 1st step 500 rpm 250 rpm s^{-1} 10 s, 2nd step 3000 rpm 1000 rpm s^{-1} 10 s.

3. Homogenization Step: 5 minutes rest

4. Soft Bake Step: 3 minutes 100 °C

5. Rehydration Step: 15 minutes rest

6. Mask Alignment Exposure Step: Expose Dose 200 mJ/cm^2

7. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1-2 minutes, followed by 2x di water rinse baths

Protocol for AZ 5214 E

1. Dehydrate Step: Graphene coated wafer placed on a hot plate at 130 °C for 15 minutes.
2. Spin Coat Step: Two-step spin 1st step 500 rpm 250 rpm s^{-1} 10 s, 2nd step 3600 rpm 1000 rpm s^{-1} 10 s.
3. Homogenization Step: 5 minutes rest
4. Soft Bake Step: 1 minute 100 °C
5. Rehydration Step: 15 minutes rest
6. Mask Alignment Exposure Step: Expose Dose 150 mJ/cm^2
7. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1-2 minutes, followed by 2x di water rinse baths

Protocol for Microposit S1813, Single Layer Process

1. Dehydrate Step: Graphene coated wafer placed on a hot plate at 130 °C for 15 minutes.
2. Spin Coat Step: Two-step spin 1st step 500 rpm 250 rpm s^{-1} 10 s, 2nd step 3000 rpm 10000 rpm s^{-1} 10 s.
3. Homogenization Step: 5 minutes rest
4. Soft Bake Step: 1 minute 115 °C
5. Rehydration Step: 15 minutes rest
6. Mask Alignment Exposure Step: Expose Dose 150 mJ/cm^2
7. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1 minute, followed by 2x di H_2O rinse baths

Protocol for LOR 5A and Microposit S1813, Bi-Layer Process

1. Dehydrate Step: Graphene coated wafer placed on a hot plate at 130 °C for 15 minutes.

2. Spin Coat Step: Two-step spin 1st step 500 rpm 250 rpm s^{-1} 10 s, 2nd step 3000 rpm 10000 rpm s^{-1} 10 s.

3. Homogenization Step: 5 minutes rest

4. Soft Bake Step: 2 minutes 180 °C

5. Spin Coat Step: Two-step spin 1st step 500 rpm 250 rpm s^{-1} 10 s, 2nd step 3000 rpm 10000 rpm s^{-1} 10 s.

6. Homogenization Step: 5 minutes rest

7. Soft Bake Step: 1 minute 115 °C

8. Rehydration Step: 15 minutes rest

9. Mask Alignment Step: Expose Dose of 150 mJ/cm^2

10. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1 minute, followed by 2x di H_2O rinse baths

3.5.4 Negative Photoresist Protocols

Negative photoresist AZ 125 nXT and AZ nLOF 2070 (MicroChemicals GmbH, Germany) are used as temporary etch masks, as they can be removed using solvent cleaning. Other negative photoresists and photo-active polymers are used to fabricate permanent passivation layers, including SU-8 2025 (MicroChem Corp. USA), EpoClad5 (MicroResist Technologies, Germany) and Ostemer 220 Litho (Mercene Labs, Sweden). AZ nLOF is also hard-baked with an additional baking step to produce permanent features.

Protocol for AZ 125 nXT

1. Wafer Dehydration Step: Wafer is placed on a hot plate 15 minutes at 130 °C
2. Photoresist Spin Step: 45 s 2500 rpm 500 rpm/s
3. Homogenization Step: 5 minutes rest
4. Soft Bake Step: 13 minutes 130 °C
5. Rehydration Step: 15 minutes rest
6. Mask Alignment Exposure Step: Expose Dose 1500 mJ/cm^2
7. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 2-3 minutes, followed by 2x di water rinse baths

AZ 125 nXT is also used for creating the master moulds for microfluidic soft lithography. The "AZ 125 nXT Microfluidic" protocol is modified to produce a thicker photoresist film: Spin speed decreased to 1000 rpm, soft bake time increased to 18 minutes, development time increased to 4 - 5 minutes.

Protocol for AZ nLOF 2070 photoresist passivation mask

1. Wafer Dehydration Step: Wafer is placed on a hot plate 15 minutes at 130 °C
2. Photoresist Spin Step: (Step 1) 10 s 500 rpm 250 rpm/s, (Step 2) 30 s 3000 rpm 1000 rpm/s
3. Homogenization Step: 5 minutes rest
4. Soft Bake Step: 7 minutes 100 °C
5. Rehydration Step: 15 minutes rest
6. Mask Alignment Exposure Step: Expose Dose 300 mJ/cm^2
7. Post Exposure Bake Step: 3 minutes 110 °C

8. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1-2 minutes, followed by 2x di water rinse baths

9. Hard Bake Step: Tube Furnace 200 °C for 30 minutes (plus heat-up and cool-down time)

Protocol for SU-8 2025 Photoresist Passivation Mask

1. Wafer Dehydration Step: Wafer is placed on a hot plate 15 minutes at 130 °C

2. Photoresist Spin Step: (Step 1) 10 s 500 rpm 250 rpm/s, (Step 2) 30 s 3000 rpm 1000 rpm/s

3. Homogenization Step: 5 minute rest

4. Soft Bake Step: 3 minutes 65 °C, increase to 95 °C for 5 minutes

5. Rehydration Step: 15 minutes rest

6. Mask Alignment Exposure Step: Expose Dose 150 mJ/cm^2

7. Post Exposure Bake Step: 1 minutes 65 °C, increase to 95 °C for 5 minutes

8. Developer Step: Develop in AZ 726 (Microchemicals GmbH) for 1-2 minutes, followed by 2x di water rinse baths

Protocol for EpoClad5 photoresist passivation mask

1. Wafer Dehydration Step: Wafer is placed on a hot plate 15 minutes at 130 °C (recommended 200 °C)

2. Photoresist Spin Step: (Step 1) 10 s 500 rpm 250 rpm/s, (Step 2) 30 s 3000 rpm 1000 rpm/s

3. Homogenization Step: 5 minute rest

4. Soft Bake Step: 5 minutes 120 °C

5. Rehydration Step: 15 minutes rest

6. Mask Alignment Exposure Step: Expose Dose 350 mJ/cm^2

7. Post Exposure Bake Step: 3 minutes 120 °C

8. Developer Step: Develop in acetone 1-2 minutes, followed by IPA bath 5 minutes

9. Hard Bake Step: Hot plate 120 °C for 30 minute

Ostemer 220 Litho Protocol

1. Coating, 1 ml of resist per 25 mm substrate diameter

2. Spin, 500 rpm for 40 seconds with acceleration of 100 rpm/second. (estimated unknown μm thick)

3. Expose Non Contact mode, 1200 mJ/cm2

4. Develop, Acetone, (Alternatively Butyl Acetate)

5. Clean, IPA 5 minutes

6. Dry, Compressed air

7. Hard bake, Not required, optional 90 °C 60 mins increase stiffness

Additionally to improve adhesion further 1 % W/W Dynasylan MTMO was mixed with methanol or ethanol. A clean wafer is submerged into the solution for at least 10 minutes at RT. The wafer is taken out of the bath and blown dry with compressed gas (air or nitrogen). The wafer is placed in an oven or on a hotplate set at 100-110 deg C for 10 minutes.

Ostemer 220 Litho

Ostemer 220 Litho is part of the ostemer range of UV curable resins (Mercene Labs). This product is adapted from the standard range for high contrast ratio patterning using a photomask. The surface of the ostemer product rang have active thiol group groups that would allow for further bonding of PDMS microfluidic packaging to be directly bonded to the passivation film. Ostemer 220 Litho requires mixing of two components 1.86 : 1 ratio of A to B. Optimally both components are stored at 5 °C this creates crystals in the solution. Therefore, both components require heating at 60 °C to dissolve the crystal compounds back in the solution. The two components are mixed thoroughly and then vacuum dedicated to removing trapped air from the solution before photolithography.

3.6 Etching Processes

3.6.1 Plasma Graphene Etch Process

Protocol for Reactive Ion Etching (RIE) Oxford Plasmalab 80 Plus (Oxford Instruments, UK) graphene etch process, prior to the graphene etch step the chamber is cleaned using an (O_2) plasma for 15 minutes. The parameters for O_2 plasma; 75 mtorr chamber pressure, 50 W RF power 50 sccm O_2 flow rate. The sample is then inserted into the chamber and pumped down to vacuum. The same O_2 plasma parameters are used for the graphene etch process but with a process time of 30 s.

Protocol for Inductively Coupled Plasma etching (ICP) SPTS ICP (SPTS Technologies, UK) graphene etch process, the ICP user protocol requires a 30 minute O_2 plasma clean 500 W after each process run to clean the chamber. An additional cleaning step is not required prior to the graphene etch process. The coil power is set to 200 W and platen power set to 50 W, O_2 flow rate 100 sccm and chamber pressure 100 mtorr. The process time set for 10 s any increase in plasma time resulted in further photoresist hard baking and photoresist.

3.6.2 Silicon Etch Process

Deep silicon etching was performed using ICP (SPTS Technologies, UK) using the deep silicon "Bosch process", also known as time-multiplexed etching where the process alternates repeatedly between two different gas recipes passivation and etching.

The parameters for the deposition phase; octafluorocyclobutane (C_4 F_8) gas flow rate 100 sccm, coil RF generator set to 600 W.

The parameters for the etch phase; Sulphur hexafluoride (SF_6) gas 200 sccm, coil RF power set to 800 W.

3.6.3 SiO_2 Etch Process

Protocol for RIE (Oxford Instruments, UK) SiO_2 etch process recipe; gases 100 sccm CF_6 and 4 sccm O_2, power 150 W, chamber pressure 70 mTorr.

3.6.4 Yttrium Etch Process

Yttrium layer (10 nm thickness) is wet etched by submersion in 100 ml 0.2 M HCl for 30 s followed by 2x Di H_2O rinse steps.

3.6.5 Al_2O_3 Etch Process

To etch Al_2O_3 thin films a wet etch process using AZ 726 photo-developer (Microchemicals GmbH, UK). Sample is submerged in 100 ml AZ 726 (50 nm/minute etch rate), followed by 2x di H_2O rinse steps.

3.7 Metal Deposition

3.7.1 Physical Vapour Deposition

Metal deposition for metal electrodes is done using physical vapour deposition (PVD) system (Lesker 75 PVD System). The samples (pieces) are fixed into place

on the sample holder using polyamide tape covering the edge regions (approximately 1 mm) the sample holder is then fixed into position inside the vacuum chamber. The metal targets for metal deposition are inserted into the sputtering guns at the base of the vacuum chamber.

The chamber is pumped down to vacuum 10^{-5} torr. Cr is deposited with plasma parameters, flow rate of 30 sccm Argon and power increased to 80 W. Pd is deposited with plasma parameters, flow rate 60 sccm Argon and power increased to 50 W.

3.7.2 Metal Evaporation

Metal evaporation of Yttrium and Copper was performed using Quorum Q150TE Sputter Coater (Quorum Technologies, UK). Using Tungsten baskets (Quorum Technologies) Yttrium or Copper pieces $<$ 12 mm (Kurt J.Lesker Company, USA) are loaded into the basket and inserted into Sputter Coater. Turbo pump down process is used to reach base pressure 10^{-4} Torr. The current required is preset based on the material required copper 20 μA, Yttrium 30μA. The thickness is measured using crystal monitor, once the required thickness is achieved the current is turned off.

3.8 Graphene Sensor Passivating Films: Dielectric Materials

3.8.1 Magnetron Sputtered Silicon Dioxide

First trials of dielectrics deposition were performed using the PVD 75 (Kurt J. Lesker, USA) to sputter the dielectric material. This method allowed a photoresist lift-off procedure to produce the passivation window around the graphene channels. The bi-layer photoresist combination LOR and S1813 were used with the same parameters as the metal lift-off process.

To sputter SiO_2 in PVD system an RF plasma (13.56 MHz) is generated instead of a DC plasma. The alternating current prevents a charge build-up within the

dielectric materials which could eventually arc into the plasma.

The parameters for RF sputtering require the PVD chamber to be pumped down to 10^{-5} torr for 1 hour before deposition. During the deposition, Ar plasma is flown into the chamber at 80 sccm. RF power is ramped up 10 W at a time to avoid sudden charge/heat build-up in the SiO_2 target. the power is raised to 50 W. After 1 minute of deposition the plasma will be stable and the target surface will be cleaned of surface contamination. The dep rate at this power setting produces 0.001-0.005 nm/s. To produce a substantial dielectric film e.g. 30 nm the deposition took over 2 hours of deposition during this time the dep rate reduced, potentially due to the build-up of positive ions on the target. Depositions of this thickness are not regularly done using PVD sputtered dielectrics with 2 inch diameter target material. However, for the overall limited damage to the graphene due to the lift-off method, this was investigated preliminarily.

Initial tests were performed on Cu coated chips to check resistance to Sulphuric acid (used during functionalization processes Au dep). Lift-off was then tested on fabricated Dip Chip Origin devices.

3.8.2 Plasma Enhanced Chemical Vapour deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD) SPTS PECVD (SPTS Technologies, UK) is a process which uses the energy within the plasma to induce reactions at the wafer surface that would otherwise require higher temperatures associated with conventional CVD. Energetic ion bombardment during deposition can also improve the film's electrical and mechanical properties. The routine operating temperature of the PECVD are separated into substrate platen 300 °C, chamber 75 °C and shower head 250 °C.

Silicon Dioxide Standard Process

Silicon dioxide (SiO_2) is produced by the combination of silicon-based gas silane (SiH_4) 105 sccm, and oxygen gas (N_2O) 3000 sccm.

Silicon Nitride Standard Process

Silicon nitride (Si_3N_4) is produced by combining silicon-based gas SiH_4 40 sccm, and nitrogen-based gas ammonia (NH_3) 55 sccm and an N_2 flow of 1960 sccm.

SIlicon Dioxide Low Temperature

The power and gas flow rates for the deposition of SiO_2 were kept the program recipe was kept the same. However, the temperature settings for the three main temperature components were set to 35 °C so that the temperature could be maintained by the system controller.

SIlicon Nitride Low Temperature

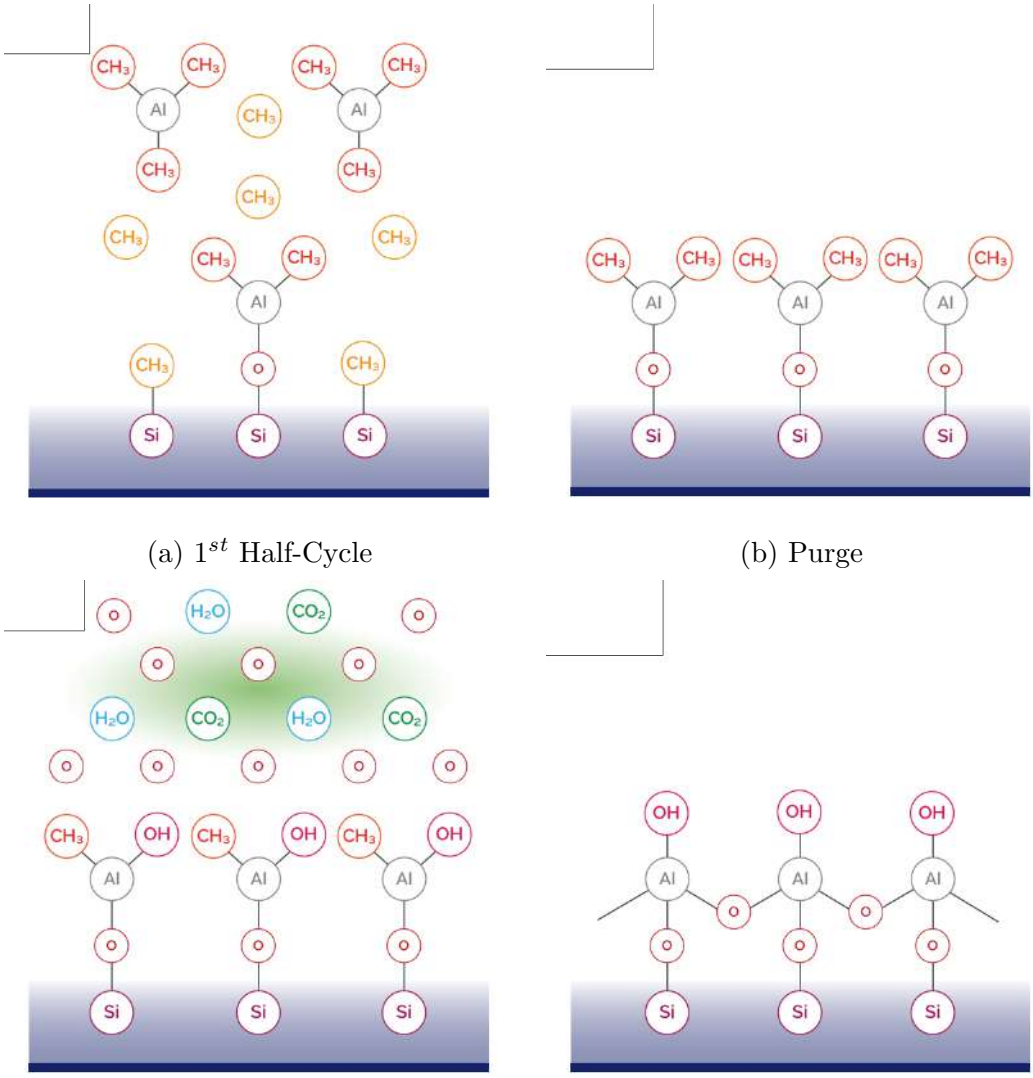
The power and gas flow rates for the deposition of Si_3N_4 were kept the program recipe was kept the same. However, the temperature settings for the three main temperature components were set to 35 °C so that the temperature could be maintained by the system controller.

3.8.3 Molecular Vapour Depsoition: Aluminium Oxide

The molecular vapour deposition tool (MVD) has atomic layer deposition (ALD) capability. Aluminium Oxide (Al_2O_3) is deposited using precursors kept under vacuum. Each cycle is represented by a volume (defined by pressure) collected into an expansion chamber then released into the main sample chamber (Under higher vacuum) for each subsequent precursor of the deposition. Al_2O_3 is deposited using two precursors: 1. Trimethylaluminium (TMA) deposited first to react with native hydroxyl groups. Followed by precursor 2 di H_2O which reacts with the methyl groups releasing CH_4. Resulting in further hydroxyl groups on the remaining Al-O to repeat the TMA. These steps (half cycles) compromise a full cycle, the chemical reaction of each precursor step can be seen in Figure3.1.

The resulting films are deposited at approximately 0.1 nm per cycle, as the thickness of the deposition increases in thickness beyond 5 - 10 nm the deposition

rate is closer to 0.09 nm per cycle. So to achieve a thickness of 30 nm requires approximately 340 cycles (1 cycle = 50 s).



(a) 1^{st} Half-Cycle

(b) Purge

(c) 2^{nd} Half-Cycle

(d) Purge

Figure 3.1: MVD Al_2O_3 process for a single deposition cycle. (a) TMA is released into the chamber and reacts with native hydroxyl (oxygen) groups on the surface. (b) The excess TMA and reacted CH_3 groups are purged from the chamber. (c) Di H_2O is released into the chamber and reacts with the CH_3 groups of the TMA molecule. (d) The remaining H_2O and reaction products are purged from the chamber. This figure was adapted from Oxford Instruments Atomic Layer Deposition.

3.9 Microfluidic Packaging

3.9.1 Polydimenthysiloxane

PDMS is used for creation of microfluidic channels / packaging.

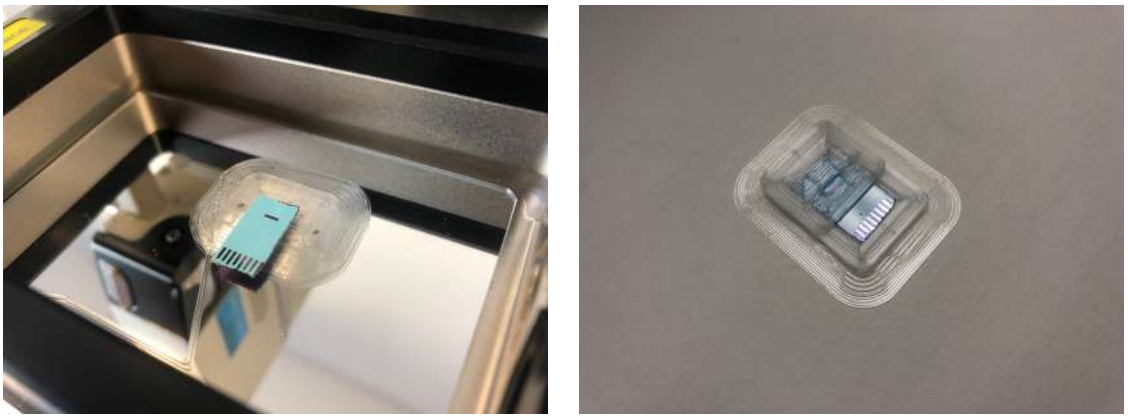
The PDMS comes as a two-part system and is mixed by weight at 10:1 siloxane to curing agent. The extra curing agent can be added to decrease the setting time. The PDMS is then degassed for up to one hour using a vacuum desiccator to remove air bubbles from the liquid. The template wafer is placed inside a wafer holder or Petri dish to allow for PDMS overflow. The PDMS is then poured onto the template wafer. The minimum volume required to cover the surface of the wafer is used; a volume of 10 ml PDMS is required. The wafer and PDMS are placed inside a 50 °C oven for four hours to complete the process of cross-linking the siloxane chains. After cross-linking or hardening, the PDMS is removed from the template wafer. The depth of the inlets and outlets of the device are the same as the microfluidic channels. The PDMS is punctured with a 0.5 mm diameter boring tool in the inlet and outlet region. Metal syringes and tubing (Darwin Microfluidics).

To bond PDMS pieces directly to the graphene Dip Chips. The PDSM bonding surface is exposed to an O_2 plasma (RIE for 30 s) which creates negatively charged molecules and free radicals on the surface. The PDMS piece is then brought into contact with the graphene Dip Chip. The reactive groups on the PDMS surface bond to the Oxygen groups of the SiO_2 surface. The radical groups rapidly return to a more stable state the two surfaces need to be introduced to each other within a 2 - 3 minute window to ensure liquid tight bonding. Once brought into contact the PDMS and Si chips are heated on a hot plate at 80 °C for 30 minutes to finalise the bonding process.

3.9.2 3D Printed Microfluidics

Microfluidic 3D designs were created using Fusion360 (AutoDesk) imported through Fluidic Factory software (Dolomite Microfluidics) to create a proprietary 3D print

file which can be loaded onto the Dolomite Fluidic Factory 3D printer. This specialist 3D printer designed to compress the fused filaments whilst extruding to produce liquid-tight seals even single filament thick. This method can be used to print microfluidic channels directly on the graphene Dip Chips. Using a file pause function the base of the microfluidic cartridge, the graphene Dip Chip is then fixed into its final position using epoxy-based adhesive. The second half of the file then continues to print encapsulating the region of the Dip Chip and printing a microfluidic channel intersecting with the graphene channel this can be seen in Figure 3.2.



(a) Graphene device cross section view (b) Dip Chip iso view

Figure 3.2: (a) Microfluidic cartridge print paused after stage 1 pf printing. Graphene Dip Chip bonded into specific notch using epoxy based adhesive. (b) Microfluidic cartridge removed from printer after stage 2 of printing encapsulating the graphene region of the Dip Chip.

3.9.3 Blood Separation Testing

Blood Samples

Samples of whole blood were obtained under full ethical approval (REC Ref No. 13/WA/0190) by venipuncture from healthy individuals, who had not taken any medication that is known to interfere with coagulation that is the anticoagulants or antiplatelet therapy (e.g. aspirin). Each donor declared that they had no personal

or family history of coagulopathies or thromboembolic disease. A qualified phlebotomist collected the blood samples slowly and carefully from the median cubital or cephalic vein, using a 21-gauge butterfly line (Greiner Bio-One: Safety Blood Col. Set + Holder 21GX19 cm SP Sterile - Cat.-No: 450085).

Microfluidic Set Up

Single Microfluidic Syringe Pump (World Precision Instruments, USA) was used with $1/16^{th}$ HPLC tubing. Connected to 5 ml Luer Lock syringes (BD, USA) via PEEK Micro-Fitting connectors (Sigma Aldrich, UK).

Haematology Analyser

For blood cell counting a 400 μl sample of blood plasma was required to be for use with the Abbott Cell-Dyn Ruby Haematology analyser (Abbott, USA). The wash steps and analyses are performed automatically by the analyser and csv files are produced containing the total cell counts and standard deviation.

3.10 Chemical and Biochemical Functionalisation

Functionalisation the graphene Dip Chip platforms, with an amine-terminated surface. The PGSTAT302 AutoLAB (Metrohm Ltd UK) was used to electrochemically functionalise graphene devices. To protect the metal contact electrodes of Graphene devices from functionalisation solutions photoresist or dielectric passivation material was used in place of the screen printed passivation.

3.10.1 Drop-cast Functionalisation

The drop-cast functionalisation method requires a pi-pi stacking molecule. Pyrene is used extensively in the literature to bio-functionalised graphene surfaces [1]. Bio-receptors pre-conjugated to pyrene is an example of a functionalisation method that can be carried out using a drop-casting process. The solution is applied directly to

the graphene surface. And following a 2-hour incubation, samples are washed with di H_2O, leaving behind the functionalised surface.

Thrombin Aptamer Pyrene Conjugate

Thrombin being a target biomarker for blood clotting the general aim of the biosensor under design, optimisation and testing. Also the thrombin aptamer sequence has been in public domain since 1992 [2] the 15 base pair sequence $5'-GGTTGGTGTGGTTGG-3'$. This sequence was purchased from Base Pair Bio with additional modifications a spacer T section as well as the pyrene end conjugation to allow for π-π stacking 5'-pyrene – 10T Spacer - Aptamer – 3'. For dropcast functionalisation 1 μg of the thrombin aptamer was dissolved in $MgCl_2$ 0.1 M concentration. This was made up to a 10 μl solution and dropcast onto the graphene channel surface incubated in a sealed container for 2 hours

For the scramble sequence control an aptamer for Brain natriuretic peptide (BNP) was also purchased from Base Pair Bio from their commercial aptamer selection with the same 5'-pyrene – 10T Spacer - Aptamer – 3' molecular layout. The functionalisation procedure for the control channel was kept the same as the thrombin aptamer

The aptamers were reconstituted using the reconstitution buffers provided by Base Pair Bio. And made diluted to 5 mM using the application buffer (Application Buffer 200ml = 10 mM TrisHCl(pH 7.4), 150 mM NaCl, 1 mM MgCl, Tween20 0.05%)

Sensing experiments were performed using alpha thrombin protein (Sigma Aldrich) in a dilution series from 1 pg to 1 μg per ml in 0.1 M PBS. The protein concentrations were applied sequentially with a 45 minute incubation period for each protein and PBD wash steps in between.

Poly(ethylene glycol) Blocking Molecule

Poly(ethylene glycol) (PEG) pyrene conjugate 2 kDa (Sigma Aldrich) diluted to 0.1 M concentration in PBS. 10 μl of the solution is dropcast onto the graphene channel and incubated for 2 hours in a sealed container. Excess solution was then washed off with di H_2O.

3.10.2 Electrochemical Functionalisation

Electrochemical functionalisation was performed using PGSTAT302 AutoLAB (Metrohm Ltd UK) to individually functionalise the graphene channel. Electrochemistry involves the movement of electrons from one element to another, caused by chemical processes. The transfer of electrons is known as a redox reaction. A standard 3 electrode system was used to electrochemically functionalise the graphene channel see Figure 3.3 for set up. The graphene surface acts as the working electrode, Pt was used as the counter electrode and Ag/AgCl was used at the reference electrode. The electrodes are submerged in an electrolyte solution (PBS 0.1 M). The AutoLAB is used to apply a potential to the working and reference electrode and measures the current between the counter and working electrode.

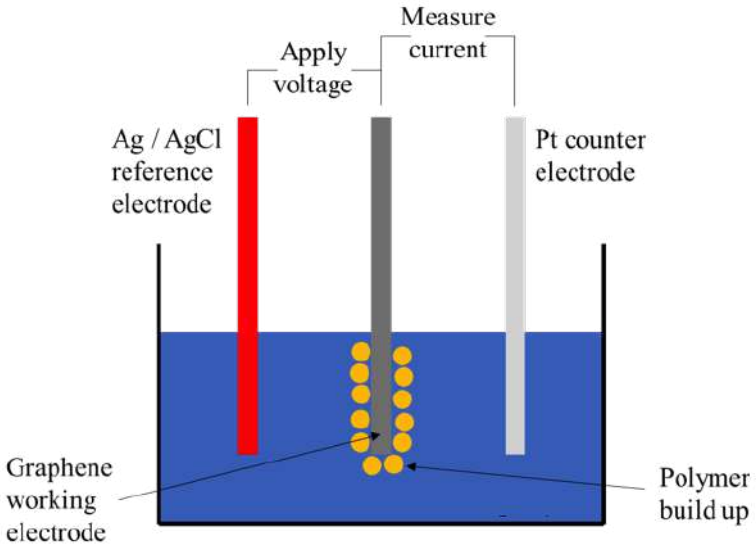


Figure 3.3: Diagram showing electrochemical set up of a three electrode system for polymerisation reaction, adapted from [3].

Chemical functionalisation by polymerization of Diamino

The devices were functionalised with pDAN using the method detailed below. 10 mM DAN was prepared in 0.25 M H_2SO_4. Graphene devices, Pt counter electrode and Ag / AgCl reference electrode are added to the solution. The potential scan is applied from 0.3 V to 0.9 V for 25 cycles and current is measured to produce a cyclic voltammetry (CV) graph of current against applied potential.

3.10.3 Gold Nanoparticle Functionalisation

0.01 M $HAuCl_4$.xH2O was prepared in di H2O. Graphene channel, Pt counter electrode and Ag / AgCl reference electrode are added to the solution. A constant potential of – 0.1 V was applied to the working electrode for 60 s. A potential of – 0.1 V was applied to the working electrode as it is the potential required to oxidise Au, from previous work by the group.

3.11 Electrical Testing & Analyses

3.11.1 IV Probe Station

The Semiprobe lab (Inseto) and IV lab (Everbeing) probe station were used to measure the resistance of each Graphene device throughout both fabrication and functionalisation processes. Devices were placed on the sample stage, which can hold substrates up to 100 mm in diameter. The device contact pads were probed using Gold (Au) plated Tungsten (W) probes. A sweeping voltage was applied across the device, the current was measured, and resistance was calculated.

The Inseto IV probe station with two micromanipulators and probes connected via BNC (Bayonet Neill–Concelman) cable and connected to the terminal blocks of Keithley 2602A source measurement unit for two-terminal IV measurements this is standard practice. The Inseto unit uses a sheared BNC cable with the guard cable grounded through the terminal blocks on the back of the Keithley 2602A.

The Everbeing IV probe station with four micromanipulators and internal inserted probes connected to tri-axle cabling directly connected to triaxle ports of the Keithley 2636B source measurement unit. For 2 - 4 terminal IV and gated measurements.

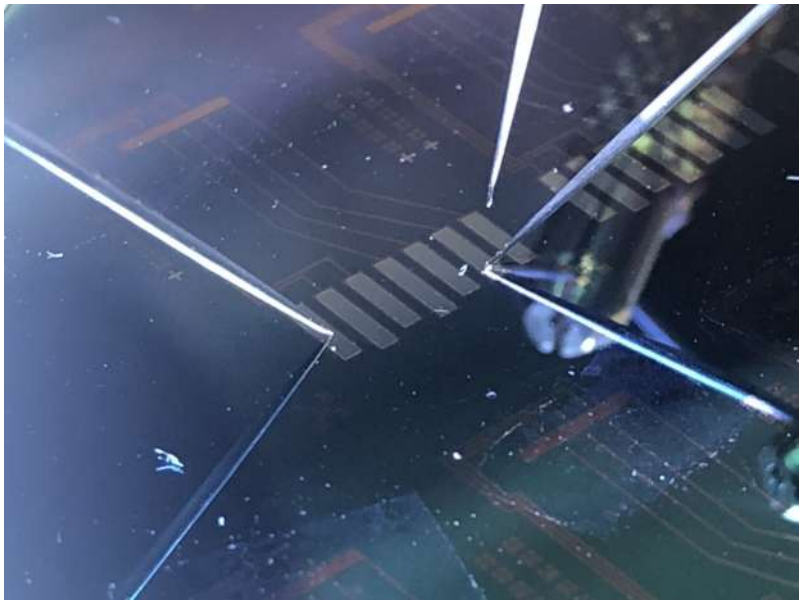
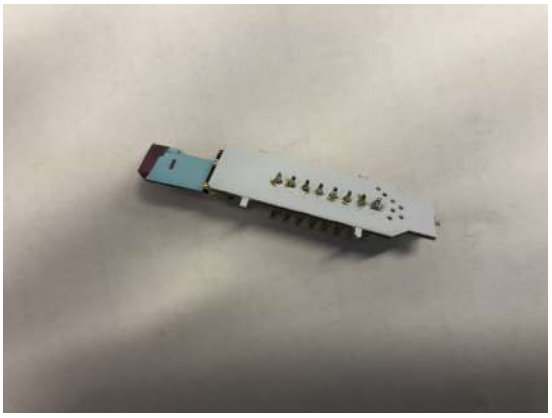


Figure 3.4: Gated measurement of Dip Chip based graphene channel. Full 100 mm wafer scale production and analyses

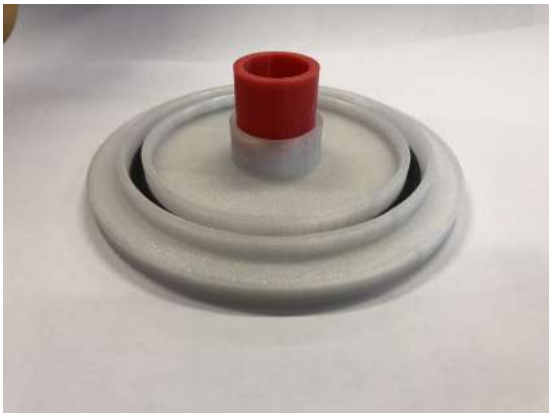
The Keithley 2600 series source meter unit has a built-in graphical user interface "Keithley TSP Express" of their standard TSP (Test Script Processor). This enables basic bias, sweep and step control of one or more probes. For a standard IV sweep to calculate

Each Keithley 2600 series source measurement unit has two channels / SMUs. With the use of cat5 ethernet cable multiple Keithley 2600 series source measurement units can be connected. This enables more than two SMUs to operated during a single measurement.

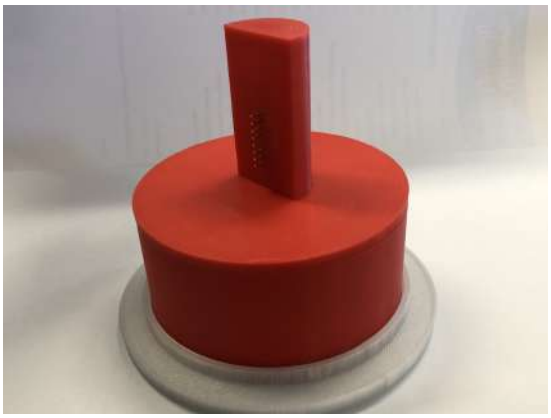
An SD card connector was integrated into a custom made PCB with soldered header pins. The header pins can be connected via BNC hook clip cables that can connect to the triaxle ports of the 2636B Keithley unit. This allows for PCB connector dip measured for in solution measurements (measurement container 5 ml volume). See Optimisation Chapter for more details on the Dip Chip design.



(a) Graphene device cross section view



(b) Dip Chip iso view



(c) Dip Chip iso view

Figure 3.5: (a) Dip Chip Graphene channel chip inserted into SD card connector PCB. (b) Dip Station base with changeable solution pot in centre region aligning with suspended Dip Chip. (c) Dip Station top with header pins from SD car connector exposed to enable BNC clip cables to make connection with Kietheley SMU's.

3.11.2 Keithley Scripts

Using the graphic user interface "Keithley TSP Express" the default current detection range when set to Auto is set to 100 mA with a step time of 200 ms. For the most accurate data the detection range should be set to lowest possible as to not dampen the signal by measuring in the larger obsolete region. This can be done by manually setting the range lower and lower until the linear signal no longer fits within the given axis. In setting the range manually instead of Auto the step time

can also be adjusted.

Two Terminal Resistance Measurement, Silicon not connected to the system (Floating Gate)

A voltage sweep performed using a single Keithley SMU from -1 V to 1 V and the resulting current is measured. The sweep is performed over 101 points in 0.02 V increments. The data is then exported containing three main data columns time-stamp, input voltage, measured current.

Two Terminal Resistance Measurement, (Grounded Gate)

Sweep parameter are as above for the two-terminal resistance measurement. Additionally to the source and drain, a probe is connected to the bulk silicon and grounded to the Keithley instrument. Either by contacting a dedicated gate electrode or applied to silicon exposed via scratching through the thin dielectric SiO_2 layer using a diamond tipped scribe. Alternatively, the bulk silicon can have the voltage set to 0 V relative to the system.

Three Terminal Gated Sweep Measurement

The set up involves holding a constant bias at either 10 mV or 100 mV and current measured across the Source-Drain electrodes of the graphene channel on SMU-A. The gate electrode connected to SMU-B is set to sweep gate from -50 V to 50 V, with 201 data points (0.5 V intervals). The data is then exported containing 5 main data columns time-stamp, input voltage channel, input voltage gate, measured current channel and measured current gate.

Continuous Measurements, Two terminal resistance

A point measurement taken over a set number of power line cycles (25) drain bias set at 0.1 V and the resulting drain current is measured. The maximum number of points that can be measured using the Keithley instruments with TSP Express is

1000 points. A time interval between point measurements was set at 72 s to produce a 20 hour monitoring period to make continuous measurements of the graphene channel under different conditions. Using the SD connector PCB and Dip Station. Multiple solvents wetting and drying effects the graphene could be measured.

The time length is adjusted for specific measurements, the total number of measurement points (1000) is kept constant and the interval is automatically calculated. The data is then exported containing three main data columns time-stamp, input voltage, measured current.

3.11.3 Electrochemical Analyses

Square Wave Voltammetry

Square wave voltammetry (SWV) is widely used in electrochemical based sensing applications [4].

SWV is a form of voltammetry whereby the current at the working electrode is measured between the working electrode whilst the reference electrode undergoes a linear sweep. This is a modified version of staircase voltammetry (Linear measurement). The current is measured at twice, after the forward potential pulse and then after the reverse potential pulse.

SWV performed using PGSTAT302 AutoLAB (Metrohm, Switzerland) sweep Range set from -0.2 - 0. 5 V current measurement range set to automatic. csv files produced containing the input bias and output current this data was then plotted as line graphs using Excel.

Differential Pulse Voltammetry

Differential Pulse Voltammetry (DPV) is another voltammetry method used for electrochemical measurements, it is also a modification of normal staircase voltammetry [5]. A series of voltage pulses are superimposed on a normal staircase linear sweep. The current is measured immediately before each pulse and then plotted against the potential applied.

DPV performed using PGSTAT302 AutoLAB (Metrohm, Switzerland), sweep Range set from -0.2 - 0. 5 V current measurement range set to automatic. csv files produced containing the input bias and output current this data was then plotted as line graphs using Excel.

3.12 Material Characterization Techniques

3.12.1 Scanning Electron Microscope

The primary SEM used in this work was the Hitachi S-4800 field emission scanning electron microscope. The highest resolution achieved with this microscope is 1 nm. The microscope has a variable accelerating voltage from 0.5 - 30 kV and a variable current 1 - 20 μA. lower accelerating voltages for low-density samples and high accelerating voltages for high-density samples. To image graphene, an acceleration voltage of 10 kV and measuring current of 5 μA is used. There is a top and bottom backscatter detector which can operate separately or combined. For this work, the detectors were set to "combined".

3.12.2 Energy-dispersive X-ray Spectroscopy

The Oxford instruments EDX detector has two main operating modes for performing EDX on a sample. EDX analysis can be performed as a single point, single line or over an area. The scan determines the elementary components as percentages of a single point or averaged over an area. A line scan can be used to identify elementary changes across border regions in samples.

An EDX map takes the SEM image captured using SEM settings, and displays the elements identified overlay with the original image. This method is useful when identifying layers in a cross-section of a substrate.

3.12.3 Raman Spectrometer

Structural damages due to annealing were characterized via Raman spectroscopy. An InVia Raman microspectrometer (Renishaw, UK) was used to collect Raman spectroscopic data within this thesis. The spectrometer was equipped with a 100x NPlan microscope objective (Leica, USA). Spectral data were acquired using a 532 nm laser with a 2400 l/mm spectral grating. Spectral data were acquired with the following parameters:

Laser power: 50% (60 mW at sample). Spectral range 1200-3000 cm^{-1}. Exposure 10 s. Accumulations 1. Spectral maps were collected in a square array with 5 μm spacing within 50 μm^2 area.

Spectral mapping data were analysed using the Renishaw Wire 5.1 software package to generate mapping images. Raw spectra for mapping analysis and average peak ratio values were calculated via exporting to MATLAB and analysed via in house software.

532 nm laser, 100x objective (N-plan 0.85 na), 1200 - 3000 cm-1, 50 % laser power (60 - 70 mW).

25 - 25 micron maps, in 5 micron even steps, raster format

Data Processing

Graphene was baseline subtracted with polynomial within the Wire software. Cosmic ray removal procedure is done within wire software using the automated program.

Mapping measurements were created using wire's mapping review software. Exported map data as .txt for analyses in mat lab (Math Works). Peak centres were chosen visually using the Wire 5.1 software

Graphenea Tube Furnace D = 1345 G = 1598 2D = 2696

Graphenea RTA D = 1349 G = 1600 2D = 2693

Graphenea Annealed Acetone IPA D = 1349 G = 1600 2D = 2696

Graphenea Annealed microposit Acetone IPA D = 1349 G = 1601 2D = 2696

Graphenea Annealed microposit Acetone IPA Remover D = 1349 G = 1598 2D = 2693

Graphenea Annealed microposit LOR Remover Acetone IPA D = 1349 G = 1597 2D = 2693

Graphenea Annealed Yttrium HCl D = 1346 G = 1601 2D = 2695

Bottom Contact blank D = 1346 G = 1588 2D = 2679 pixel saturated

Bottom Contact 5214E acetone IPA remover D = 1346 G = 1590 2D = 2685

Graphenea Epo D = 1346 G = 1591 2D = 2693

Graphenea Ytt RIE HCl D = 1348 G = 1601 2D = 2698

Bottom Contact MVD D = 1346 G =1596 2D = 2684

Different parameters were used for transfer rig scans, extended exposure 1100 - 3200, 100 % power, 50x objective 50 % 50x static scan centre at 1800.
Appendix map scan 8.1.10.

3.12.4 Atomic Force Microscopy

The Nanowizard II AFM (JPK Germany) used for imaging and surface roughness, morphology and step height measurements in the with sub nm resolution. Scanning area of 100 x 100 μm^2 with the gain set 150, setpoint 0.45 V and a line frequency of 0.3 Hz. (Bruker silicon cantilever)

Bibliography

[1] Guangfu Wu, Ziwen Dai, Xin Tang, Zihong Lin, Pik Kwan Lo, Meyya Meyyappan, and King Wai Chiu Lai. Graphene field-effect transistors for the sensitive and selective detection of escherichia coli using pyrene-tagged dna aptamer. *Advanced healthcare materials*, 6(19):1700736, 2017.

[2] Louis C Bock, Linda C Griffin, John A Latham, Eric H Vermaas, and John J Toole. Selection of single-stranded dna molecules that bind and inhibit human thrombin. *Nature*, 355(6360):564, 1992.

[3] Ryan Michael Bigham. Development of process technology for silicon and graphene biosensor devices. Technical report, Swansea University, 2019.

[4] Aicheng Chen and Badal Shah. Electrochemical sensing and biosensing based on square wave voltammetry. *Analytical Methods*, 5(9):2158–2173, 2013.

[5] Eduardo Laborda, Joaquín González, and Ángela Molina. Recent advances on the theory of pulse techniques: A mini review. *Electrochemistry Communications*, 43:25–30, 2014.

Chapter 4

Graphene Sensor Fabrication & Optimisation

4.1 Introduction

This chapter is broken down into 4 sub-chapters comprising of; "Designs & Fabrication" where the graphene sensor designs and associated fabrication process flows are described and evaluated; "Residue Free Graphene Transfer Process By Vacuum Via Transfer" a novel approach to wafer scale residue free graphene transfer process is tested; "Process Optimisation & Comparison" where the Pre-Transfer process flow is optimised in terms of fabrication materials and maintenance of graphene quality by minimising the introduction of defects from processing; "Device & Connector Testing" where the graphene devices are tested using a custom SD-Card PCB connector system.

Graphene devices have been fabricated using a number of different approaches. These include graphene Pre-Transfer process, where the graphene is supplied on a SiO_2/Si wafer and the graphene is thus present throughout the fabrication process; and graphene Post-Transfer process, where the device metal contacts are fabricated first, and the graphene layer is transferred toward the end of the fabrication process flow. Both methods have their merits and drawbacks.

Graphene Pre-Transfer process has been used to fabricate graphene resistors, graphene field-effect transistors (G-FET) and graphene electrochemical devices. Optimisation of graphene sensor processing has enabled development of antibody-based biosensors for future point of care sensors [1]. This work looks to optimise the Pre-Transfer process further and compare it to the alternative Post-Transfer process.

The process of fabricating a graphene field effect sensor involves multiple process steps similar to those used in the semiconductor industry. The advantages of using these process techniques, as outlined in the Literature Review, is that they are established techniques which allow for industrial level fabrication, using facilities that can be applied to sensor fabrication. The disadvantage is the overall cost, which is still relatively high compared to screen-printed sensors using graphene composites for fabrication of Screen Printed Electrodes (SPEs), which have an approximate cost £1.33 per SPE based on pricing from 3000 graphene SPEs £4000 (Zimmer & Peacock Ltd. 2019 pricing).

This compares to a graphene field-effect transistor (G-FET) sensors approximate cost of £350 per G-FET S-10 Sensor (Graphenea 2018 pricing), with 36 channels per sensor chip which equates to a price per channel of £9.70. The advantage of the G-FET sensor is the achievable sensitivity in the fM - pM range compared to graphene composite SPEs in the nM - μM [2] [3]. However, the semiconductor approach also has the potential for miniaturised graphene sensor chips, reducing device costs and increasing total sensors per chip [4]. The aim of this chapter is thus to develop and optimise G-FET sensors with the goal of producing a scalable, low-cost, high performance sensor.

4.2 Graphene Sensor Design & Fabrication

This section looks into the design of the graphene FET chip including the initial design criteria, the Dip Chip concept and the connector interface. Additionally, design improvements that increase functionality were also investigated: A "Multiplex Design", which allows for droplet-based analyses of different solutions on a single chip and individual functionalisation processes to be performed; An "Inverted MOSFET Design", which allows for individual gating of the graphene channel separate to gating of the silicon substrate which affects all channels; A "Matrix Design" which increases the total number of graphene channels per chip whilst keeping the contact electrode numbers the same, thus increasing the sensor yield per chip/wafer.

The fabrication process flows are broken down into the key fabrication steps and explained for the, (1) Pre-Transfer process flow, (2) Pre-Transfer Yttrium process flow which adds a sacrificial protective layer into the process flow, (3) Post-Transfer process flow, (4) Inverted MOSFET Design process flow, (5) Matrix Design process flow and (6) post-fabrication chip modification process flows.

Cost analyses of the main process flows were compared taking into account the resulting device yields and time scales. The number of working graphene channels per unit area is the determining factor for the cost for each sensor chip. The process costs are the same, regardless of the number of graphene channels patterned on the surface. In the longer term a PCB package would enable a smaller die size and therefore the highest yield of graphene channels. This must be balanced against packaging costs and graphene compatible processes.

Another key factor is the size of the substrate wafer. Some graphene suppliers such as Graphenea now offer 150 mm SiO_2 coated wafers with transferred monolayer graphene. This would not greatly increase processing costs, as industry has shown that an increase in wafer size can reduce cost per die [5]. Both of these aspects were not explored in this research due to restrictions in budgets and facilities but should be explored further in the future, as the best approaches for dramatically reducing costs and for scale up. Another approach to reducing cost is increasing the total

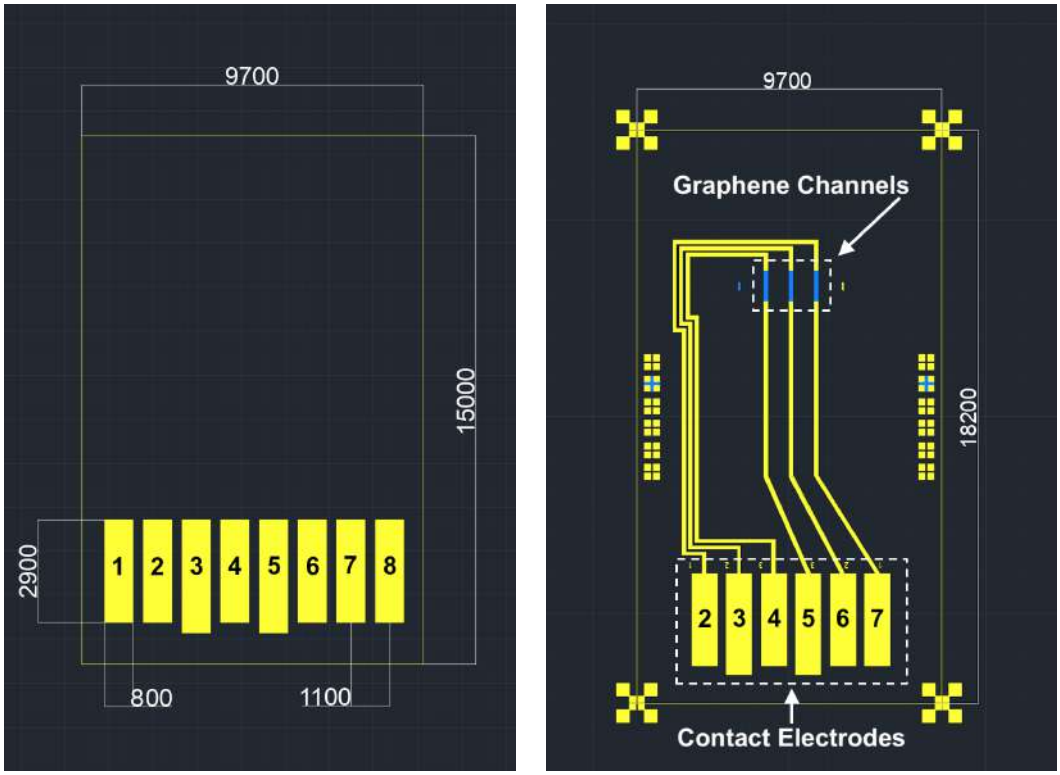
number of functioning graphene channels per chip. Keeping the die size the same and the number of electrical connections within the SD card PCB connector, keeping the process steps the same but changing the electrical layout to increase the total number of graphene channels. Alternative process flows will also be investigated, increasing the number of fabrication steps and increasing the total graphene channels per chip was also examined.

4.2.1 Device Design Criteria

Primary design criteria for the graphene sensor were: To be suitable for sensing experiments using liquid samples, to allow for repeat measurements per chip to improve reliability and to connect to an external electrical interconnect. A connector whereby the silicon chip could be inserted and held in place by friction with the device electrodes in contact with metal pins inside the connector. This was designed alleviate the use of electrical probing to the device electrodes. Electrical IV probing can cause damage to electrodes and is a source of reliability problems. If this biosensor is to move forward towards a commercial product it will need to be easy to handle, requiring a quick reliable connection system for inserting and removing replacement graphene chips.

A micro SD card (Secure Digital) connector was chosen as its widely available and cheap to purchase. The micro SD card has a height of 1 mm, which allows for standard wafer thickness of 525 μm to be inserted into the opening and held in place by the pressure of the connections pins. As the SD card design was developed by the SD card association and is not a proprietary technology, so it can be used and modified for research purposes and could potentially be developed in a commercial product.

A full blueprint of the micro SD card dimensions (9.7 x 15 mm), as well as the electrode dimensions (0.8 x 2.9 mm) and the pitch between the electrodes (1.1 mm) [6]. This was used to recreate the dimensions in AutoCAD format and the first "Dip Chip" design layout (Figure 4.1).



(a) (b)

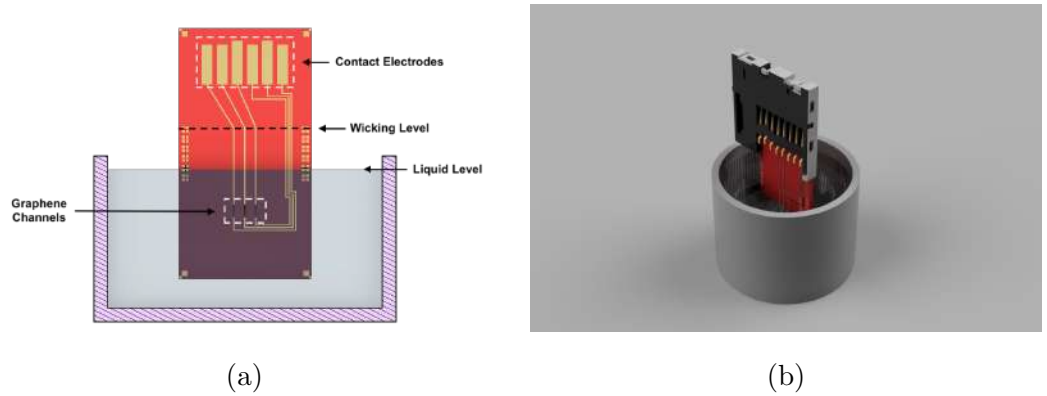
Figure 4.1: AutoCAD schematic dimensions in (μm) (a) Layout of SD Card electrodes (yellow) obtained from literature schematic [6]. With numbering of SD card connector pins. (b) AutoCAD layout of Dip Chip design with mirrored electrode dimensions. Centre connection electrodes used (2-7).

The source and drain electrodes are separate for each graphene channel in this design, which increases the flexibility of the end device. Keeping each of the electrodes separate enables individual functionalisation of each graphene channel when using electrochemical methods. If the graphene channels shared a common ground electrode then the total number of graphene channels could increase, (discussed further in this design section). However, this would mean that in a two/three electrode electrochemical system, a potential applied to any graphene channel would mean that all graphene channels would share the applied potential.

The width of the chip (die) was kept at 9.7 mm in order to align its surface electrodes with the connector pins of the SD Card reader. The graphene Dip Chip

length was finalised at 18.2 mm after wetting experiments were conducted on plain SiO_2/Si chips to determine the distance required to prevent the liquid drawing upwards onto the metal contacts, further details can be found in the Appendix section 8.2.1.

The second key design criterion was that the graphene channels could be submerged in liquid solution whilst connected to the IV characterisation unit, so that resistance and sensing measurements can be performed both wet and dry. Using a micro SD card connector and extending the graphene channels to the opposite end of the chip allowed the graphene channels to be submerged without risk to the metal metal pin in the connector (Figure 4.2). This allowed for submerged and dry IV measurements to be performed.



(a) (b)

Figure 4.2: (a) Infographic of Dip Chip submerged in liquid container. (b) Graphic of Dip Chip Graphene sensor connected via a micro SD card connector, with the graphene channels submerged in a liquid ready to perform IV or electrochemical based measurements.

The graphene channel dimensions were kept constant for all of the Dip Chip based sensors. The length was 900 μm and width 100 μm giving a total exposed area of 90000 μm^2 for each channel. The metal contact area for each electrode connected to the graphene channel covers an area of 6000 μm^2 including castellation for aided metal adhesion see CAD schematic (Figure 4.3). Variation of graphene resistance and fabrication feasibility on graphene channel dimensions was previously addressed

[1]. For the purpose of this research project the graphene channel dimensions chosen were to facilitate easier handling and alignment of graphene channels in the SD card PCB connector. These chip dimension were also chosen to be compatible with microfluidic integration, giving physical surface area surrounding the graphene channels to allow for microfluidic bonding.

Figure 4.3: Dimensions of graphene channel pattern, with end based castellations to aid with adhesion to metal contact electrodes.

The graphene channels were located in the same region of the chip with a region either side of the graphene channels devoid of metal tracks (Figure 4.4). This region allows for a microfluidic channel to be introduced into the final packaging which does not expose any metal region. If a passivation material can be introduced that protects all the metal track regions from solution the microfluidic channel can be much larger or may not be required.

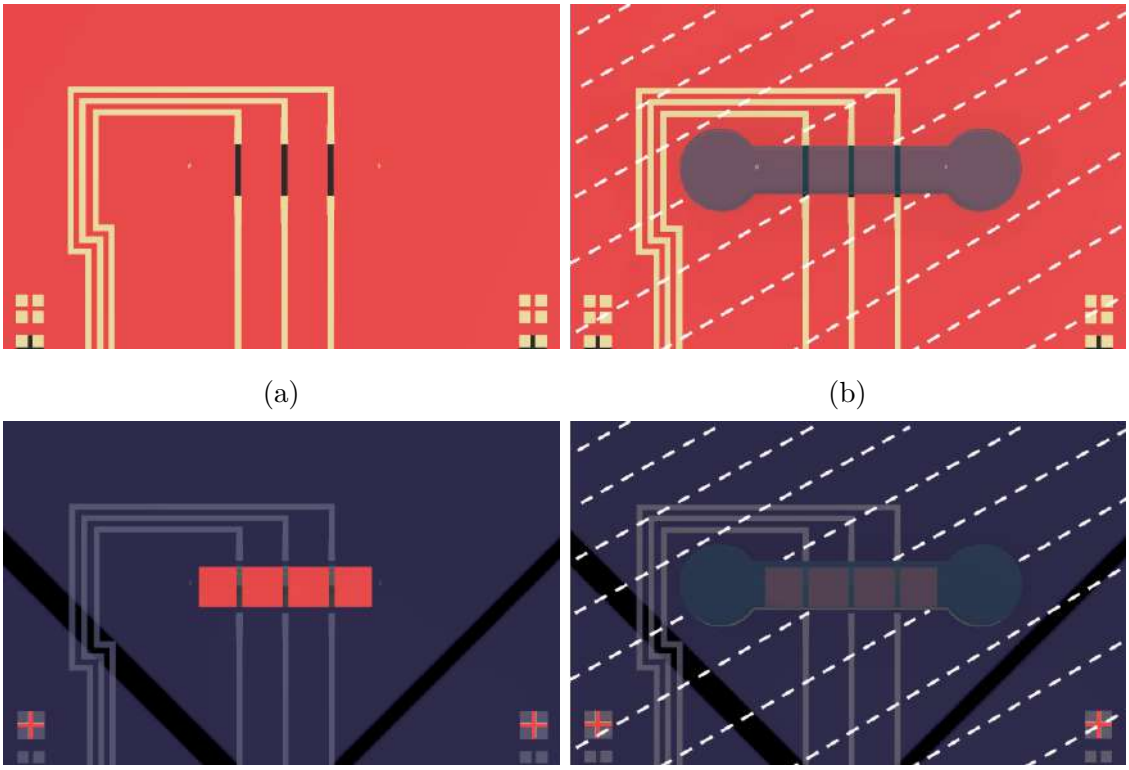


Figure 4.4: Infographic of the graphene region from the Dip Chip Design. The red background represents the SiO_2 substrate, the yellow tracks represent metal tracks and the black rectangles represent the graphene channels. (a) shows a non passivated metal tracks; (b) shows a microfluidic channel applied over the three graphene channels, the microfluidic packaging makes contact with the metal tracks and surrounding SiO_2. (c) shows the metal tracks covered with a passivation layer and a window exposing the graphene surface. (d) shows a microfluidic channel applied to the passivated Dip Chip, the microfluidic packaging only makes contact with the passivation layer.

The asymmetry of the metal track layout will create unequal metal track length for each graphene channel. Based on a metal stack of adhesion metal (20 nm Chromium) and capping metal (100 nm Palladium), the cross sectional area (A) can be calculated. The resistance (R) was calculated from the length (l) of the metal tracks, with a specific resistivity (ρ) for the particular metal. For each graphene

channel the metal track resistance was calculated using the resistance equation $R = \rho\frac{l}{A}$. The combined resistance of the adhesion and cap metals as a parallel resistor was calculated using the equation $R = \frac{R_1 \cdot R_2}{R_1 + R_2}$. Table 4.1 shows the calculated resistances of the metal tracks. The maximum variation between graphene channel 1 and graphene channel 3 is approximately 12 Ohms. This additional resistance can be figured into final resistance changes when performing IV measurements across the graphene channels.

With Dip Chip device IV measurements producing resistances on average 8-9 kΩ, the difference of 12 Ω between the metal represents approximately 0.1-0.2 % of total device resistance.

Table 4.1: The resistance of the metal tracks from contact pad to graphene channel calculated for each graphene channel on Dip Chip Design.

	Total Track Length (μm)	Total Resistance (Ω)
Channel 1	26100	235.39
Channel 2	25559	230.52
Channel 3	24772	223.42

4.2.2 Design Efficiency: Graphene Channels Per Chip

When investigating the graphene sensor chip fabrication, the first issue when analysing the efficiency of the process is to look at the number of individual steps in the process and the machine run time dedicated to this process. Next is the material costs associated with each step of the process, the number of process steps and associated machine time costs for the Pre-Transfer process (7 steps, 693.5£) and Post-Transfer process (7 steps, 693.5£). Both use the same machine time and total process steps, just arranged in a different order.

When looking at the material cost the most expensive process step is the graphene growth and transfer. As of 05/01/2019 the price for monolayer graphene on a 100

mm wafer ranges between £450 - £550 (Graphenea Spain, HexagonFab Ltd UK). The obvious way to reduce cost per chip is to miniaturise the die size of the finished chip and therefore increase the total number of chips produced per wafer. The Dip Chip dimensions 9.7 mm by 18.2 mm allow for a total of 32 die per 100 mm silicon wafer. Each Dip Chip has 3 graphene totalling 96 graphene channels per 100 mm silicon wafer. Even using the lower cost (£450) for monolayer graphene growth and transfer, this equates to £4.69 per graphene channel in graphene material alone.

To increase the total number of graphene channels with the same number of contact pads the connection layout needed to be altered. As mentioned in the initial device design of Dip Chip, each graphene channel has an individual source and drain contact pad to give the option for electrochemical functionalisation. Removing the ability for individual functionalisation enables the graphene channels to share a source contact pad, which allows the total number of graphene channels to be increased to 5 per chip. This increases the total number of graphene channels per wafer to 160 reducing cost per channel by 40%.

FET arrays have been used to increase the total number of measurable resistors whilst keeping the contact electrodes the same [7]. Using the six contact electrodes of the Dip Chip a matrix of 3 by 3 could be created with additional process steps. This would also remove the ability to individually functionalise the graphene channels with electrochemistry methods. However, this methodology would lead to a total of 9 graphene channels per chip. Figure 4.5 shows both the shared source and matrix contact concepts. This increases the total number of graphene channels per wafer to 288 reducing cost be channel by 66.6%.

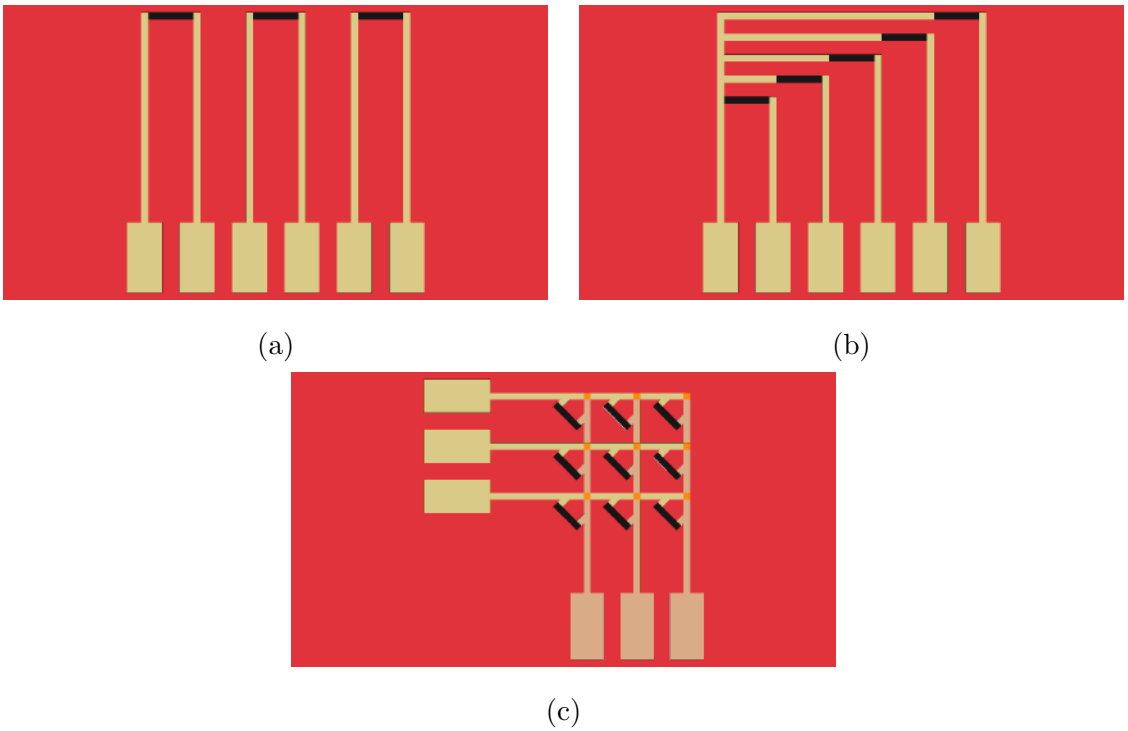


Figure 4.5: Different electrical (source-drain) measurement setups. (a) Each graphene channel has an individual source & drain contact pad. (b) Using 1 shared source contact pad 5 graphene can be measured with 5 individual drains contacts. (c) Using a matrix of 3 source contacts and 3 drain contacts. Providing the metal tracks can be electrically isolated in 3D space a total of 9 graphene channels can be individually measured.

4.2.3 Device Designs Used In This Work

The inner six electrodes (SD card connector pins 2 - 7) were chosen to be used as contacts for the graphene channels. This allowed for processing of smaller sample pieces (sub wafer-scale fabrication) and hand cleaving of the individual chips with little risk of breaking the metal tracks or graphene channels. For the modified Dip Chip designs the 2 available connector pins were incorporated to increase functionality (e.g. gating electrode). Figure 4.6 shows the modified Dip Chip; Multiplex, Inverted MOSFET, Matrix and Graphene Resistor Chip designs.

Figure 4.6a shows the Dip Chip Multiplex design the metal layer (yellow) and graphene channels (blue). The original Dip Chip design had the graphene channels arrayed in close proximity to each other (Figure 4.1), the graphene channels have a width of 100 μm and a pitch of 800 μm. This small distance between each graphene channel proved challenging when trying to functionalise to create a multiplex sensor, even with the use of microfluidic channels. Dip Chip Multiplex design has much wider spacing between each of the graphene channels. The average distance between the graphene channels was increased to 4.75 mm. All channels were moved as far apart as possible without encroaching on the 9 mm of clearance between the electrodes and graphene channel. Some of the space above the graphene channels that had been reserved for chip handling and additional electrodes has been reduced from 5 mm to approximately 2 mm to the centre graphene channel.

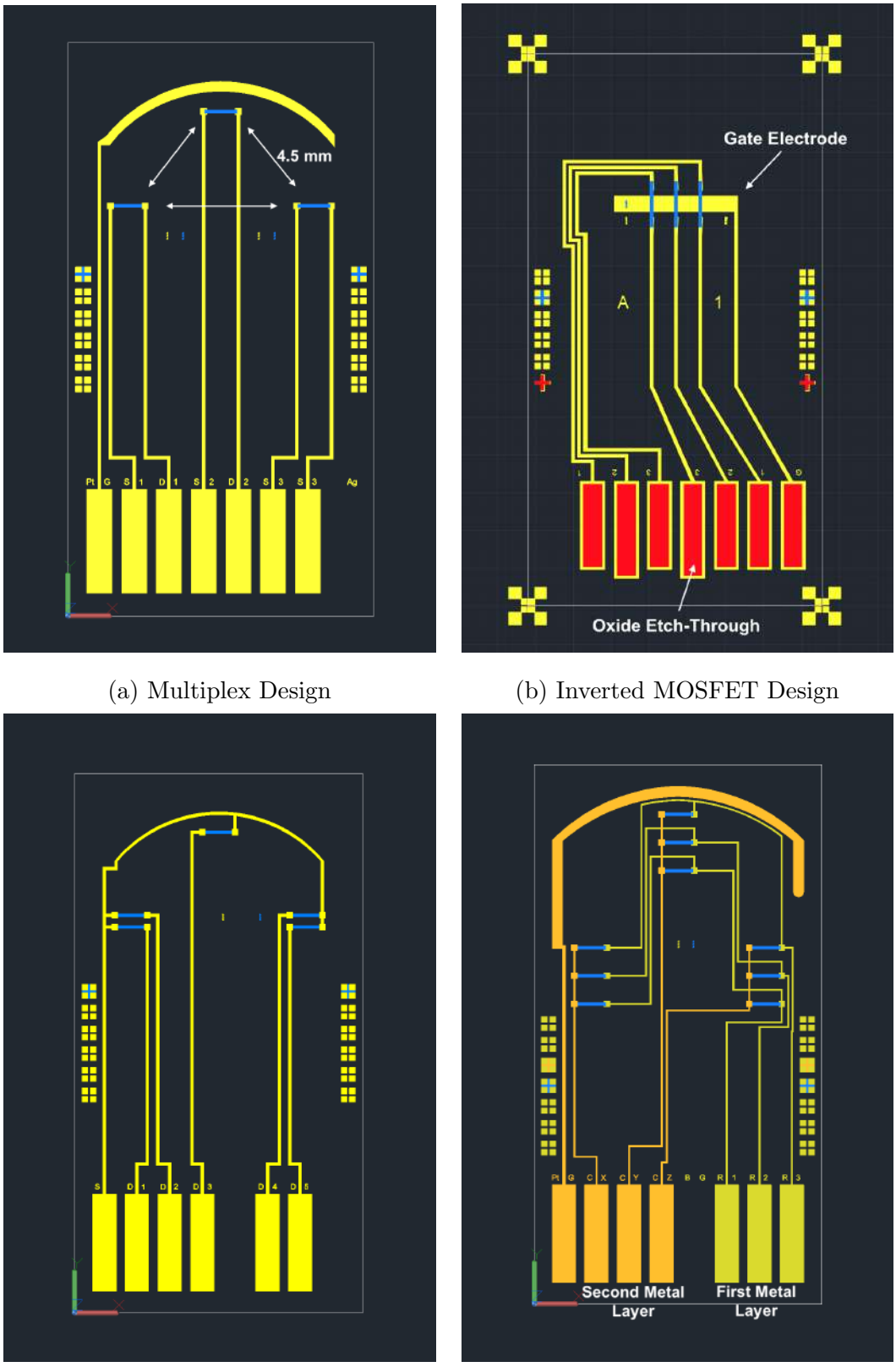
Figure 4.6b shows the Dip Chip Inverted MOSFET design, the first metal layer (yellow) is fabricated first, secondly a dielectric material (dielectric materials SiO_2 and Al_2O_3 investigated later in this chapter) is deposited on top of the first metal layer. With a second mask for dielectric etch (red) and metal filling up to the surface of the dielectric surface, The graphene is then transferred and etched to form graphene channels (blue), for the original Dip Chip design, gating of the silicon is equivalent of the metal gate in a metal-oxide-semiconductor-field-effect-transistor (a MOSFET-like device) used for producing an electric field altering the conductance of the graphene channel. This means that the electric field generated is applied to the

entire chip so with the original Dip Chip all three graphene channels will be gated simultaneously. In order to gate and measure each channel as an individual FET each channel would need its own individual gate. With a traditional MOSFET a layer of dielectric (oxide) would be deposited/grown on top of the conducting channel, with a metal gate electrode deposited on-top of the dielectric layer. However, with a G-FET sensor the device parameters require the graphene layer to be exposed to the environment or within the debye length of the detectable analyte [8], this means an oxide and metal layer cannot be deposited on top of the graphene surface.

Figure 4.6c shows the Dip Chip Shared Source design the metal layer (yellow) and graphene channels (blue). The design, similar to the Multiplex Design has the graphene channel regions spread out in a triangular geometry, which increases the distance between each region to aid with multiplex functionalisation. As the source electrode spans all 5 graphene channels the total number of channels has increased. This allows for individual graphene channel measurements but would require small time delays between measuring each graphene channel. The disadvantage of a shared source design is that the electrochemical functionalisation and sensing would measure all graphene channels simultaneously and limit the electrochemical measurements to 1 per chip. The advantage of this design is the total number of measurements per chip increases from 3 to 5 increasing the accuracy of each sensing experiment.

Figure 4.6d shows the Dip Chip Matrix design, The yellow layer represents the electrodes and metal tracks (Source) and is the first metal layer patterned and deposited. The Orange layer represents the electrodes and metal tracks (Drain) and is patterned and is the second deposited metal layer, after the deposition of a dielectric layer ($Al{-}2O_3$). This is followed by graphene transfer and patterning into channels (blue). The Matrix design concept is to maximise the total graphene channels per chip without electrode redesign. Similar to the Multiplex and Shared Source design, the graphene channels are spread out to aid with multiplex functionalisation. This design increases the number of channels per chip to 9. As with the Shared Source design, electrochemical measurements would be limited in this design to 1. However,

for electrical measurements each graphene channel can be measured individually increasing the measurements per chip to 9.



(a) Multiplex Design

(b) Inverted MOSFET Design

(c) Shared Source Design

(d) Matrix Design

Figure 4.6: AutoCad Dip Chip sensor designs.

Figure 4.7 shows the Graphene Resistor Chip design, a simple source drain graphene resistor occupying a 4 x 4 mm die. Increasing the total graphene channel output per mm^2 for fabrication optimisation testing.

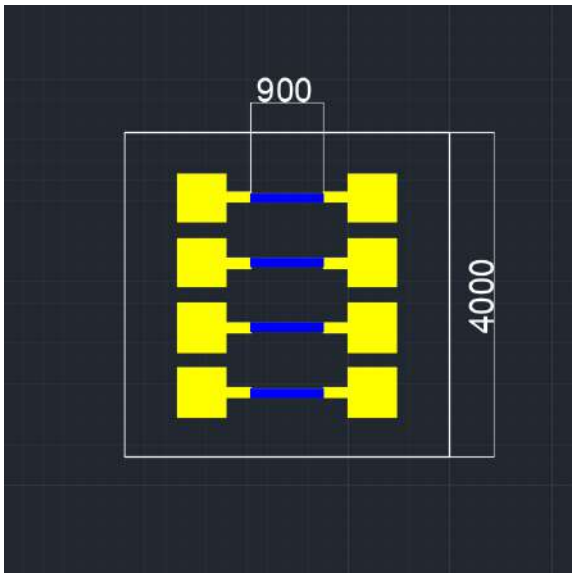


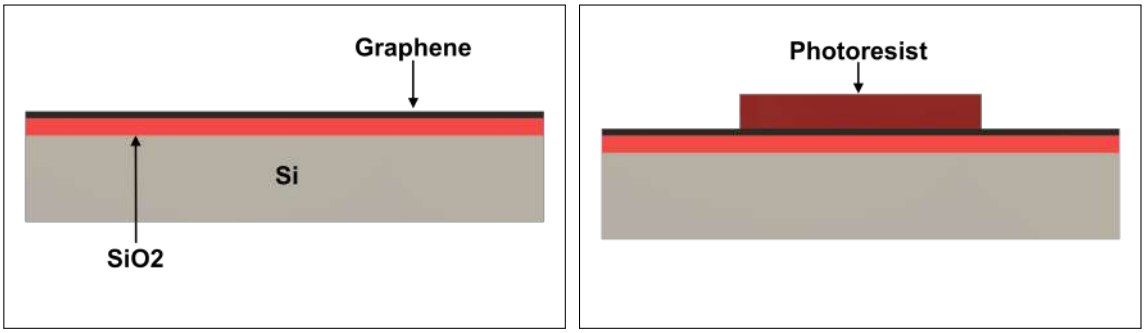
Figure 4.7: AutoCAD design for Graphene Resistor Chip (GRC).

4.2.4 Graphene Sensor Fabrication Process Flows

(1) Fabrication Process Flow: Pre-Transfer Process Flow

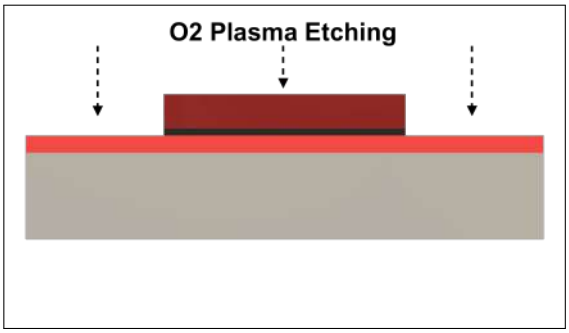
The Pre-Transfer process (standard process) was developed at Swansea University [1] and used to fabricate devices for chemical and sensor research. Figure 4.8 shows the fabrication process flow broken down into the main process steps. All protocols, processes and recipes can be found in the Materials & Methods Chapter.

Figure 4.8 (a) Graphene on SiO_2/Si supplied by Graphenea Inc. The wafer is annealed at 500 °C (Tube Furnace) followed by a "Solvent Clean" process (details of cleaning procedures found in Materials and Methods Chapter). Figure 4.8 (b) The Graphene surface is patterned with a photoresist etch-mask "AZ 5214 E" protocol. The etch photoresist etch-mask selectively protects the graphene of the graphene channel. Figure 4.8 (c) The exposed graphene surface is etched using an RIE O_2 plasma "Graphene Etch" recipe. The photoresist masked regions are protected from the O_2 plasma. Figure 4.8 (d) The photoresist etch mask is removed using a "AZ Photoresist Removal" process. Figure 4.8 (e) The SiO_2 and graphene surface is patterned with photoresist metal lift-off mask "Bi-Layer" protocol. Figure 4.8 (f) A dual metal structure (adhesion metal and contact metal) is PVD deposited sequentially over the entire surface, (Cr 20 nm Pd 100 nm). Figure 4.8 (g) The unwanted metal is removed by metal lift-off "LOR Photoresist Removal" process. Figure 4.8 (h) shows a completed Dip Chip from the Pre-Transfer process. After fabrication the metal tracks that connect the graphene channel to the contact pads would then be passivated using a screen printing passivation ink. New processes to passivate the graphene devices are examined in the Passivation & Microfluidic Packaging Chapter.

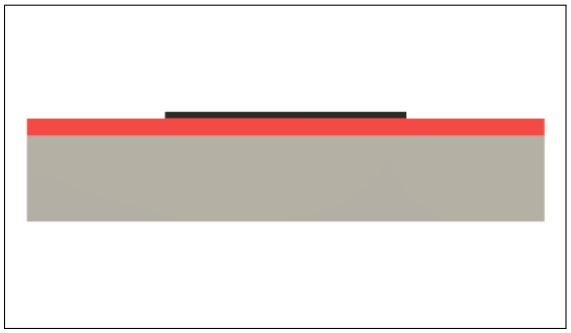


(a) Vacuum Annealing

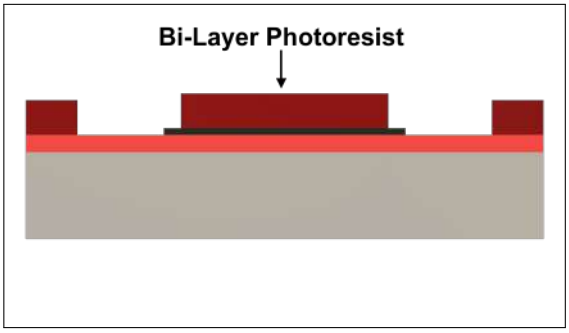
(b) Photoresist Etch-Mask



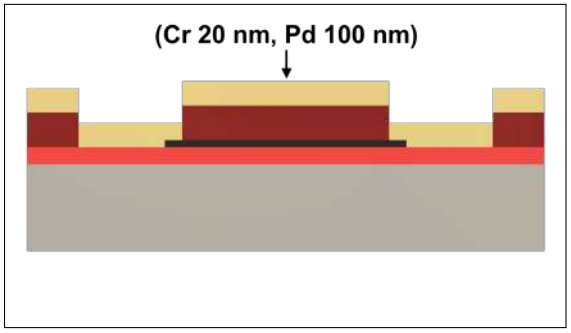
(c) Graphene Etch



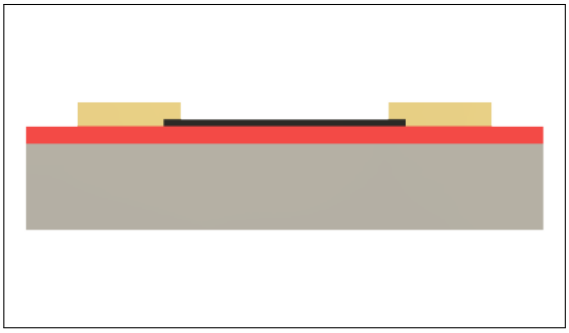
(d) Photoresist Removal



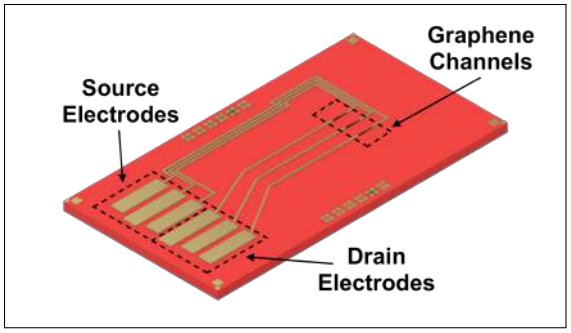
(e) Photoresist Metal Mask



(f) Metal Deposition



(g) Metal Lift-Off



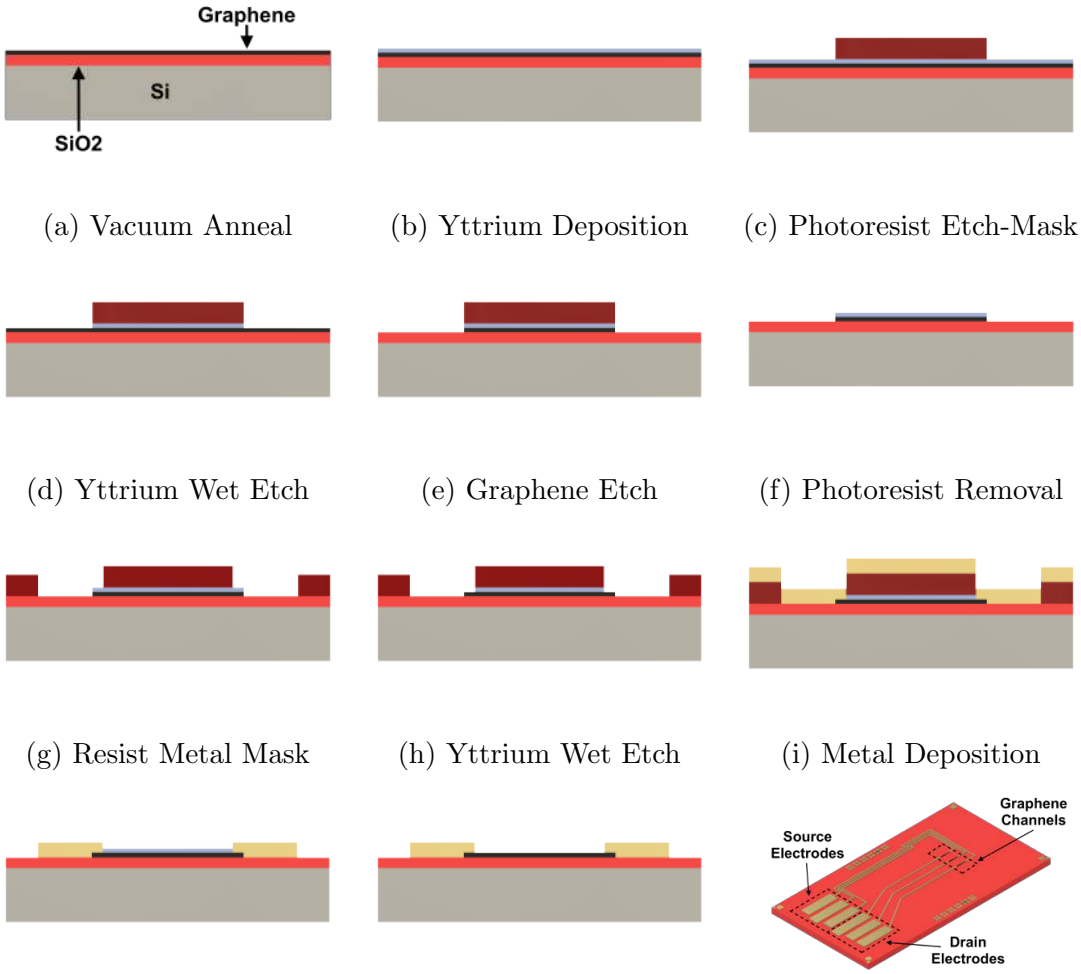
(h) Finished Dip Chip

Figure 4.8: Pre-Transfer process flow for graphene sensor fabrication.

(2) Fabrication Process Flow: Pre-Transfer Yttrium Process Flow

Based on the procedures developed to reduce graphene device variability by Wang et. al. [9], an yttrium sacrificial was introduced to the fabrication process after the first graphene annealing step. The yttrium sacrificial layer acts as a barrier between the graphene and the photoresist layer. Figure 4.9 shows the fabrication process flow broken down into the main process steps.

Steps (a, c, e, f, g, i and j) are identical to the Pre-Transfer process flow so are not explained a second time. Figure 4.9 (b) An yttrium 5 nm layer evaporated onto the graphene surface using Quorum Sputter Coater. Figure 4.9 (d) The exposed Yttrium layer is wet etched exposing the graphene layer for subsequent RIE etching. The wafer is submerged in 0.2 M HCl for 30 s followed by two di H_2O rinse steps. Figure 4.9 (h) The yttrium wet etch process is repeated to remove yttrium from graphene prior to metal deposition step (i). Figure 4.9 (k) Final yttrium wet etch step revealing graphene surface.



(a) Vacuum Anneal (b) Yttrium Deposition (c) Photoresist Etch-Mask

(d) Yttrium Wet Etch (e) Graphene Etch (f) Photoresist Removal

(g) Resist Metal Mask (h) Yttrium Wet Etch (i) Metal Deposition

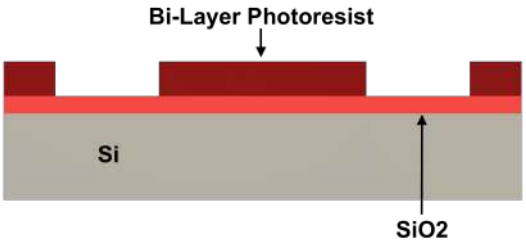
(j) Metal Lift-Off (k) Yttrium Wet Etch (l) Finished Dip Chip

Figure 4.9: Pre-Transfer Yttrium sacrificial layer process flow for graphene sensor fabrication.

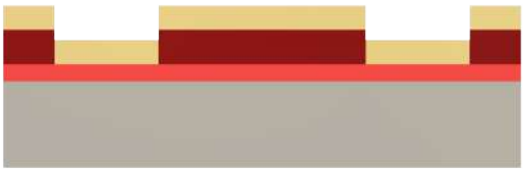
(3) Fabrication Process Flow: Post-Transfer Process Flow

The Post-Transfer process is also used in the literature for G-FET fabrication [10]. The process was developed here to be used with the Dip Chip design graphene sensor. The use of a vacuum annealing step is not required for the Post-Transfer process this is due to the single photolithography step for graphene channel etching and no aggressive lift-off solvents required for photoresist removal.

Figure 4.8 shows the fabrication process broken down into the main process steps. Before fabrication the SiO_2 substrate wafer is Solvent Cleaned to improve adhesion and uniformity during the photolithography step. Figure 4.10 (a) The SiO_2 is patterned with metal lift-off photoresist Bi-Layer process using the metal contacts photomask. Figure 4.10 (b) A dual metal structure (adhesion metal and contact metal) is PVD deposited sequentially over the entire surface, (Cr 20 nm Pd 100 nm). Figure 4.10 (c) The unwanted metal is removed by metal lift-off "LOR Photoresist Removal" process. Figure 4.10 (d) graphene transfer step performed by HexagonFab Ltd. Figure 4.10 (e) The Graphene surface is patterned with a photoresist etch-mask "AZ 5214 E" protocol. The etch-mask protects the graphene in the geometry of the graphene channel. Figure 4.10 (f) The exposed graphene surface is etched using an RIE O_2 plasma Graphene Etch recipe. The photoresist masked regions are protected from the O_2 plasma. Figure 4.10 (g) The photoresist etch mask is removed using a "AZ Photoresist Removal" recipe. Figure 4.10 (h) shows a completed Dip Chip from the Post-Transfer fabrication process.



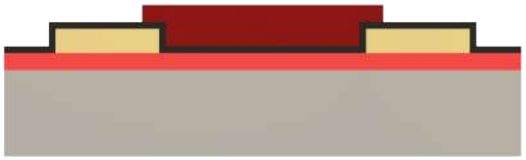
(a) Photoresist Metal Mask



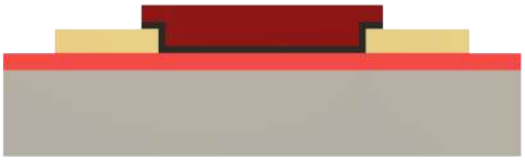
(b) Metal Deposition

(c) Metal Lift-Off

(d) Graphene Transfer

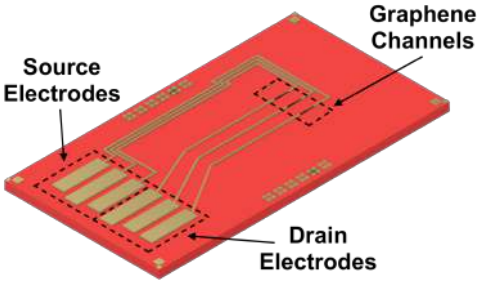


(e) Photoresist Etch-Mask



(f) Graphene Etch

(g) Photoresist Removal



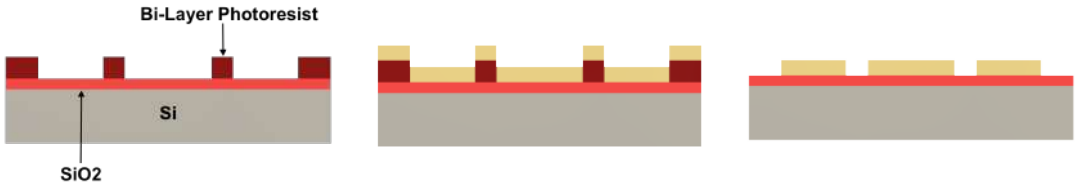
(h) Finished Dip Chip

Figure 4.10: Post-Transfer process flow for graphene sensor fabrication.

(4) Fabrication Process Flow: Inverted MOSFET Design Process Flow

The Inverted MOSFET Design shares some steps with the Post-Transfer process. The total number of process steps for the Inverted MOSFET design is greater than the standard Post-Transfer Dip Chip process and the graphene is transferred onto the wafer at step 9 of 12. As for the Post-Transfer process, tube furnace annealing is not required for graphene adhesion.

Figure 4.11 shows the fabrication process broken down into the main process steps. The final chip layout can be seen in Figure 4.12. Before fabrication the wafer was put through a Solvent clean procedure. Figure 4.11 (a) Photolithography step 1, SiO_2 is patterned with photoresist metal lift-off mask "Bi-Layer" protocol. Figure 4.11 (b) Metal deposition step, PVD sputtered; Chromium adhesion metal 20 nm Palladium capping metal 80 nm. Figure 4.11 (c) Metal lift off step, LOR Photoresist Remover protocol. Figure 4.11 (d) Dielectric deposition step, (Dielectric layers investigated later in this Chapter) Figure 4.11 (e) Photolithography step 2, photoresist etch-mask for dielectric etching, Negative photoresist nLOF 2070 protocol. Figure 4.11 (f) Dielectric etch step, etching process was investigated as part of fabrication optimisation. Figure 4.11 (g) Via filling metal deposition step, PVD sputtered metal stack, (Cr Pd)Figure 4.11 (h) Metal lift-off step, metal is removed by metal lift-off "LOR Photoresist Removal" process. Figure 4.11 (i) Graphene transfer step, performed by HexagonFab Ltd. Figure 4.11 (j) graphene etch mask step, The Graphene surface is patterned with a photoresist etch-mask "AZ 5214 E" protocol. Figure 4.11 (k) Graphene etch step, the exposed graphene surface is etched using an RIE O_2 plasma Graphene Etch recipe. Figure 4.11 (l) Photoresist removal step, the photoresist etch mask is removed using a "AZ Photoresist Removal" recipe.



(a) Resist Metal Mask (b) Metal Deposition (c) Metal Lift-Off

(d) Dielectric Deposition (e) Resist Etch-Mask (f) Dielectric Etch

(g) Metal Deposition (h) Metal Lift-Off (i) Graphene Transfer

(j) Resist Etch Mask (k) Graphene Etch (l) Photoresist Removal

Figure 4.11: Inverted MOSFET Design: process flow for graphene sensor fabrication.

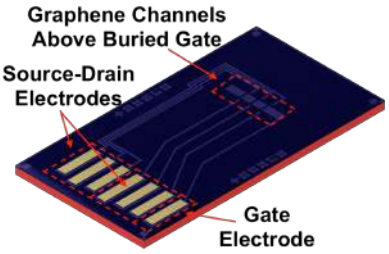
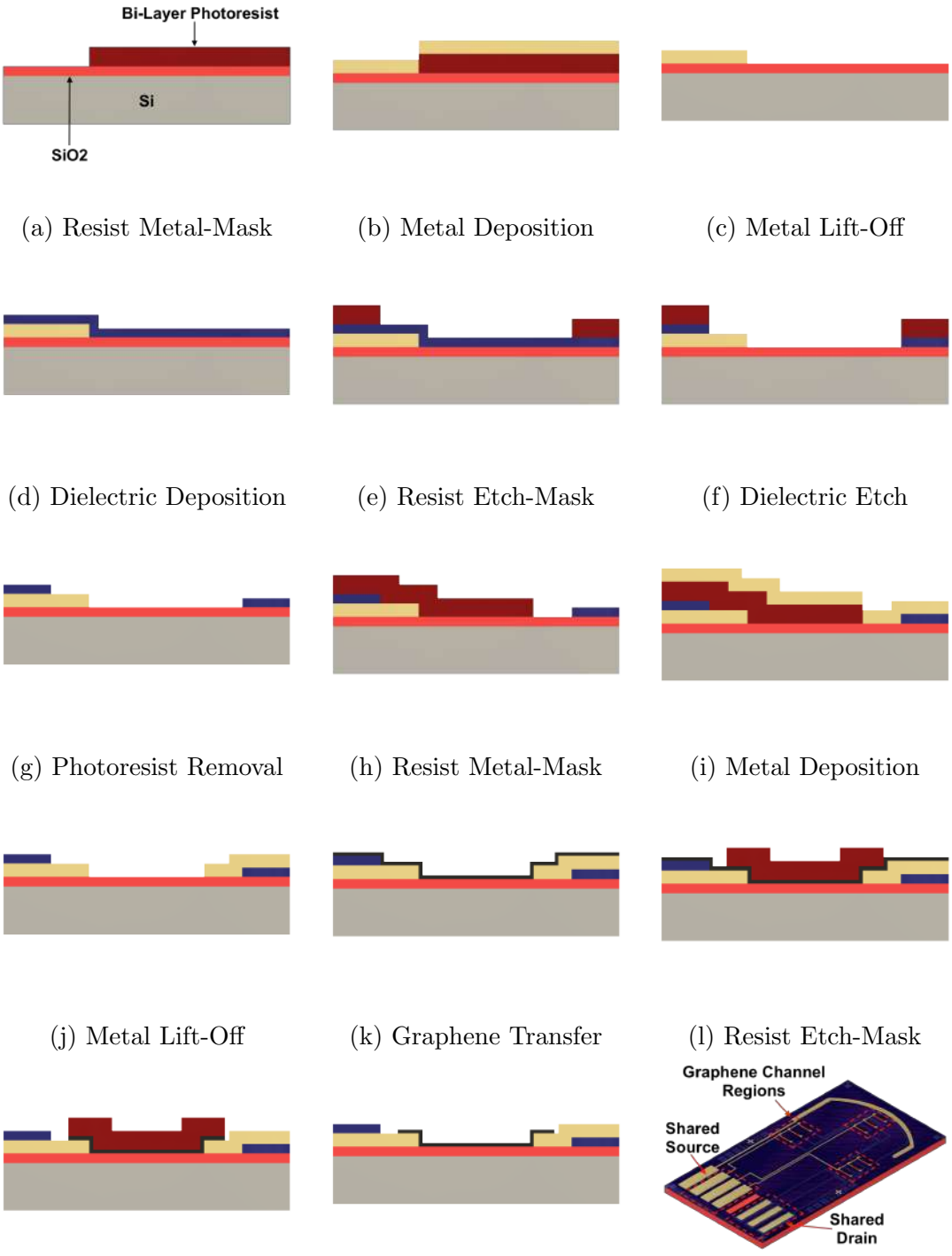


Figure 4.12: Completed Dip Chip Inverted MOSFET design Chip

(5) Fabrication Process Flow: Matrix Design Process Flow

The Dip Chip Matrix Design process flow shares similarities with the Post-Transfer process flow as the graphene is transferred onto patterned metal electrodes. The total number of process steps (14) is more for the Matrix Design than the Inverted MOSFET and Post-Transfer Dip Chip, the graphene is transferred at step 11 of 14. Similar to the Post-Transfer process annealing is not required for graphene adhesion through this process flow

Figure 4.13 shows the fabrication process broken down into the main process steps. Prior to fabrication the substrate wafer is cleaned using Solvent Clean process. Figure 4.13 (a) Photolithography step 1, Metal lift-off mask created using with Bi-Layer photoresist protocol. Figure 4.13 (b) Metal deposition 1, PVD sputtered metal stack; (Cr 20 nm, Pd 80 nm). Figure 4.13 (c) Metal lift-off 1, LOR Photoresist Removal protocol used to remove excess metal. Figure 4.13 (d) Dielectric deposition step, Molecular Vapour Deposition tool deposited Al_2O_3 layer 30 nm. Figure 4.13 (e) Photolithography step 2, nLOF 2070 protocol (photo-developer AZ 726 replaced with AZ 400K) used to produce photoresist etch-mask for dielectric vias and opening up the contact electrodes. Figure 4.13 (f) Dielectric etch step, the dielectric etch was performed using AZ 726 Al_2O_3 etch process. Figure 4.13 (g) Photoresist Removal step, The photoresist is removed using Solvent Clean process. Figure 4.13 (h) Photolithography step 2, Metal lift-off mask created using with Bi-Layer photoresist protocol (photo-developer AZ 726 replaced with AZ 400K). Figure 4.13 (i) Metal deposition 2, PVD sputtered metal stack; (Cr 20 nm, Pd 80 nm). Figure 4.13 (j) Metal lift-off 2, LOR Photoresist Removal protocol used to remove excess metal. Figure 4.13 (k). The remaining steps use the same processes as the Post-Transfer fabrication flow. The only modification to this process flow is the change in photo-developer from AZ 726 to AZ 400K at the graphene channel etch-mask step seen in Figure 4.13 (l).



(a) Resist Metal-Mask (b) Metal Deposition (c) Metal Lift-Off

(d) Dielectric Deposition (e) Resist Etch-Mask (f) Dielectric Etch

(g) Photoresist Removal (h) Resist Metal-Mask (i) Metal Deposition

(j) Metal Lift-Off (k) Graphene Transfer (l) Resist Etch-Mask

(m) Graphene Etch (n) Photoresist Removal (o) Finished Dip Chip

Figure 4.13: Inverted MOSFET Design: process flow for graphene sensor fabrication.

(6) Fabrication Process Flow: Silicon Gate Etch Reveal

For gating of the graphene channels the bulk silicon (P-type silicon substrate) is used as the gate electrode. As wafers are coated with a thermal SiO_2 layer which prevents electrical connection being made to the silicon. To allow electrical contact, a small window is etched through the SiO_2. To allow electrical contact to be made using the SD card PCB connector the SiO_2 window is etched in the location of an SD card connection pins (1 or 2).

The 1^{st} or 8^{th} SD card connector pins can also be used directly connect to the base substrate silicon. This can be achieved by additional fabrication steps. Figure 4.14 shows the process flow for silicon gate etch reveal, Figure 4.14 (b) the SiO_2 etch recipe found can be found in Materials & Methods Chapter section 3.6.3. This process flow follows on from a Pre-Transfer process Figure 4.8. Alternatively these steps could be introduced before the graphene transfer step if the Post-Transfer fabrication process.

Electrical grounding of the silicon, when performing graphene resistance based measurements, is recommended to reduce noise from built up capacitance between the silicon and graphene layer [11] [12].

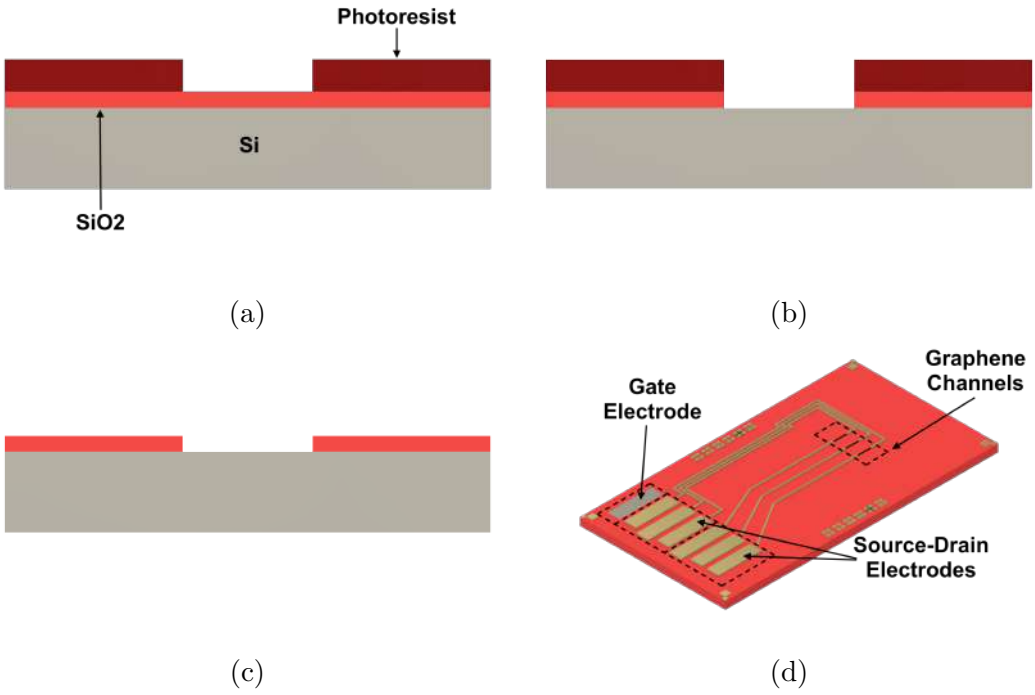


Figure 4.14: Additional process steps to produce silicon contact pad for SD card connector. (a) Photoresist etch mask patterned onto the surface of finished sensor. (b) SiO_2 etch performed using RIE process. (c) Photoresist removal and surface cleaning. (d) Finished Dip Chip with exposed Si window.

4.2.5 Fabrication Process Flow Cost Analyses

Pre-Transfer Process Flow

The Pre-Transfer process prior to passivation and functionalisation require a minimum of 7 process steps. Routinely it requires 9 process steps due to additional wafer annealing steps required for graphene adhesion. Table 4.2 shows the associated process steps and machine time cost estimates. Out of the 9 process steps only Step 1: Graphene Transfer is outsourced to external companies. The total cost excluding conditional Wafer Annealing steps was calculated as £693.5 (£933.5 including 2 furnace steps). Breaking this down further the cost per channel was calculated as £7.22 (£9.72 including annealing steps).

In the Pre-Transfer process, 8 of the 9 processes are performed with the graphene on the wafer surface. Each process step could lead to change/damage of SP^2 graphene bonding structure, or potentially have a doping effect on the graphene channel (e.g. photoresist caused hole-doping [13]).

Table 4.2: Machine cost estimates and external company costs based on 2017/2018 Centre for NanoHealth (CNH) (Swansea University) commercial services price list.

Process Step	**Process Description**	**Machine Time Cost Hourly rate x Time Duration (£)**
Step 1	Graphene Transfer, 100 mm wafer	450 - 500 (External Company)
Conditional Step 1	Wafer Annealing, Tube Furnace	120
Step 2	Photolithography Graphene Mask, Spin Coat and Mask Aligner	70
Step 3	Graphene Etch, Reactive Ion Etching	17.5
Step 4	Photoresist Removal, Photoresist Stripper	16
Step 5	Photolithography Metal Mask, Spin Coat and Mask Aligner	70
Conditional Step 2	Wafer Annealing, Tube Furnace	120
Step 6	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 7	Metal Lift Off, Photoresist Stripper	16
Total		**693.50** (With Annealing) **933.50**

Post-Transfer Process Flow

The Post-Transfer process flow requires a minimum of 7 process steps. Unlike the Pre-Transfer process, wafer annealing cannot be done at the same temperatures for Tube Furnace annealing as this would result in metal evaporation/flux on the wafer surface. A different graphene supplier (HexagonFab Ltd) is used for graphene transfer onto wafers with the metal previously fabricated. The reduced use of solvents (for photoresist removal steps) the graphene does not delaminate from the SiO_2/Si wafer surface. Table 4.3 shows the associated process steps and machine time cost estimates. The total processing cost was calculated as £693.50 which equals the cost of the Pre-Transfer process. The cost advantage of the Post-Transfer process is the lack of annealing steps, which means the cost decrease per wafer is £240 or 25.7 %. The cost per graphene channel was calculated as £7.22.

With the Post-Transfer process, 3 of the 6 processes are performed whilst the graphene is on the wafer surface. Additionally, the Post-Transfer process does not require the Bi-Layer photoresist resist process to be performed on the graphene surface (removing the 1 hour heated solvent cleaning step required to remove the Bi-Layer photoresist). This reduces the total photoresist processes and the total solvent solutions used on the graphene surface. This reduces the chance for of graphene structural damage and doping from resist residue (This will be investigated later in this chapter).

Table 4.3: Machine cost estimates and external company costs were based on 2017/2018 CNH (Swansea University) commercial services price list.

Process Step	**Process Description**	**Machine Time Cost Hourly rate x Time Duration (£)**
Step 1	Photolithography Metal Mask, Spin Coat and Mask Aligner	70
Step 2	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 3	Metal Lift Off, Photoresist Stripper	16
Step 4	Graphene Transfer, 100 mm wafer	450 - 500 (External Company)
Step 5	Photolithography Graphene Mask, Spin Coat and Mask Aligner	70
Step 6	Graphene Etch, Reactive Ion Etching	17.5
Step 7	Photoresist Removal, Photoresist Stripper	16
Total		**693.50**

Inverted MOSFET Design Process Flow

The Dip Chip Inverted MOSFET design requires a total of 12 process steps, increasing the total fabrication cost £1097.5, Table 4.4 shows the break down of the machine time costs. Due to the buried gate and metal filled vias the final stages of fabrication resemble the Post-Transfer process flow. The number of graphene channels for the Inverted MOSFET design is 3 per chip, with an estimated cost per channe calculated as £11.43.

The total cost is increased per graphene channel compared with the standard Dip Chip design. In future designs with individual buried metal gates the total graphene channels would decrease further, increasing the cost per channel even more. However, this design has large advantages (back gated Dirac point sensing measurements), and potential for studying individually gated graphene channels. As well as potential in other fields where different gate bias need to be applied to individual G-FETs (Optically transparent gated sensors). From a purely cost analyses the benefit to the sensing measurement would need to be evaluated to balance the additional cost per chip.

Table 4.4: Machine cost estimates and external company costs were based on 2017/2018 CNH (Swansea University) commercial services price list.

Process Step	**Process Description**	**Machine Time Cost (£)**
Step 1	Photolithography Metal Mask, Spin Coat and Mask Aligner	70
Step 2	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 3	Metal Lift Off, Photoresist Stripper	16
Step 4	Dielectric Deposition, Vapour Deposition	256
Step 5	Photolithography Etch Mask, Spin Coat and Mask Aligner	70
Step 6	Dielectric Etch, Wet Etch	8
Step 7	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 8	Metal Lift Off, Photoresist Stripper	16
Step 9	Graphene Transfer, 100 mm wafer	450 - 500 (External Company)
Step 10	Photolithography Graphene Mask, Spin Coat and Mask Aligner	70
Step 11	Graphene Etch, Reactive Ion Etching	17.5
Step 12	Photoresist Removal, Photoresist Stripper	16
Total		**1097.50**

Shared Source Design Process Flow

Pre-Transfer or Post-Transfer process can be used to fabricate the Shared Source Design chip (7 process steps). With a total cost of £693.5 for the 7-step Post-Transfer process for a 3 graphene channel Dip Chip (£7.22 per channel). Using a design which creates 5 graphene channels per chip the new cost per channel was calculated as £4.33, which reduces cost per channel by 40 %.

This design is more cost effective in terms of graphene channels per chip. The disadvantage is the limitation in terms of electrochemical functionalisation and analyses. However, if a purely drop-cast functionalisation approach is adopted and electrical measurements are used for sensing, this design is better suited and allows for more repeats per chip than the standard Dip Chip design.

Matrix Design Process Flow

Dip Chip Matrix Design requires a total of 14 process steps which, in turn, will increase total fabrication cost to £1007.5. Table 4.5 gives a break down of the steps and costs. Due to the buried metal layer and secondary metal layer this design can only be used with a Post-Transfer process flow. With 9 graphene channels per chip this gives a cost estimate of £4.11 per channel which reduces the cost from £7.22 by 43.1 %.

Table 4.5: The machine cost estimates and external company costs were based on 2017/2018 CNH (Swansea University) commercial services price list.

Process Step	**Process Description**	**Machine Time Cost (£)**
Step 1	Photolithography Metal Mask,	70
Step 2	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 3	Metal Lift Off, Photoresist Stripper	16
Step 4	Dielectric Deposition, Vapour Deposition	256
Step 5	Photolithography Etch Mask,	70
Step 6	Dielectric Etch, Liquid Etchant	8
Step 7	Photoresist Removal, Photoresist Stripper	16
Step 8	Photolithography Metal Mask 2,	70
Step 9	Metal Deposition, Adhesion and Cap Metal	54 (Plus Metal Cost)
Step 10	Metal Lift Off, Photoresist Stripper	16
Step 11	Graphene Transfer, 100 mm wafer	450 - 500 (External Company)
Step 12	Photolithography Graphene Mask,	70
Step 13	Graphene Etch, Reactive Ion Etching	17.5
Step 14	Photoresist Removal, Photoresist Stripper	16
Total		£1183.5

4.3 Residue Free Graphene Transfer Process

CVD graphene growth on Cu foil is a fast and cost effective process for producing high quality monolayer graphene and is the most practical approach for creating graphene based devices. The current wet transfer method for semiconductor integration has been shown to leave polymer/photoresist residue on the surface, this increases device variability and reduces graphene's carrier mobility [14]. Additionally, photoresist residues on the graphene surface effectively reduce the Debye length (screening length) for bio-receptors and target molecules for sensing [8].

Attempts have been made at producing a residue/photoresist free transfer method relying on non polymeric support structures and advanced surface treatments. This provides a hydrophobic surface to adhere the graphene to the surface during Cu etching [15]. These processed have yet to be upscaled to full wafer (100 mm +) and are currently tested on individual chips or small wafer pieces. The process developed here does not require a support material as the graphene Cu structure is held down onto the wafer surface by an applied vacuum through micro sized through silicon vias. This process has been designed for up scaling to any size substrate wafer. It requires pre-processing of the substrate, this allows for other chip structures (dicing channels) to be integrated into the wafer prior to graphene transfer.

4.3.1 Materials & Methods

Figure 4.15 shows the layout of the vacuum dicing tracks (VDTs) and through silicon vacuum vias (TSVVs) for whole wafer transfer. The process is designed for full wafer transfer of graphene and final graphene chip dicing. The design for the VDTs and TSVVs create the final die size of the graphene sensor chip. The VDTs also act as a dicing guide for saw or plasma based dicing of the individual finished chips.

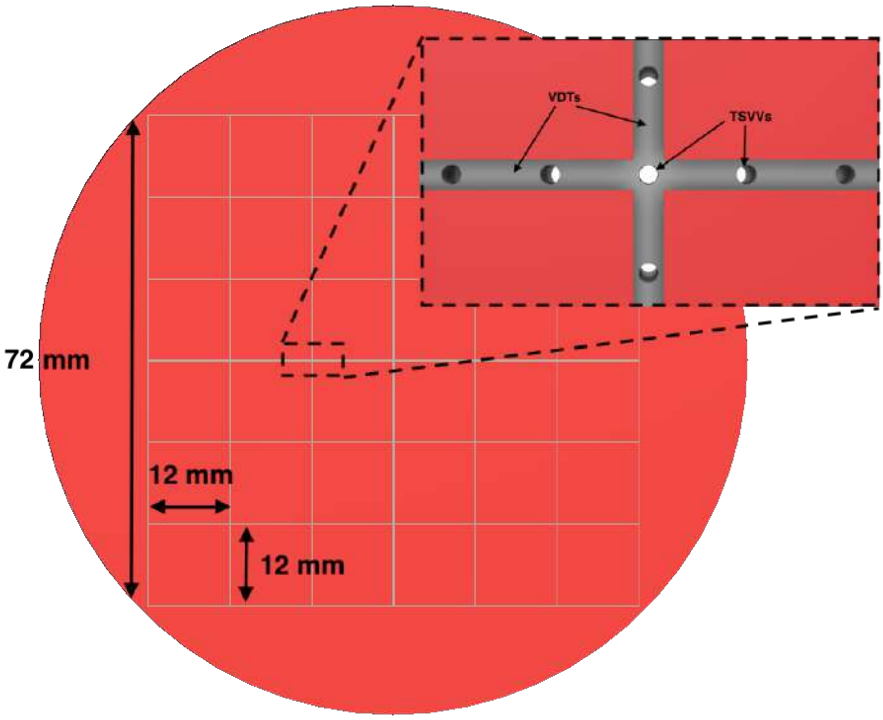
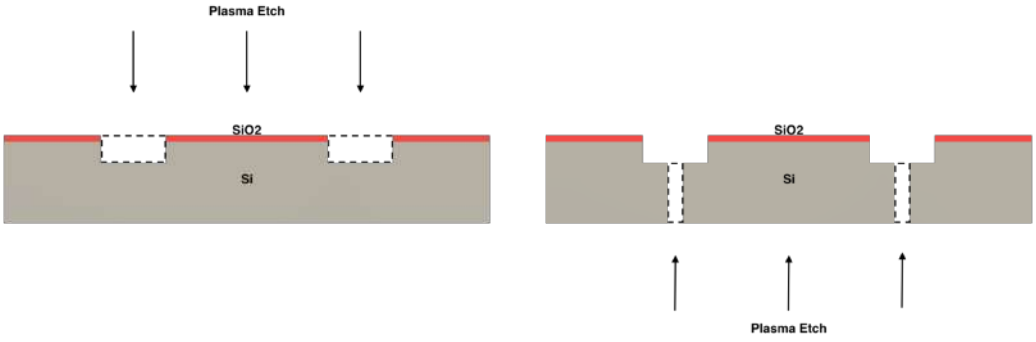


Figure 4.15: (a) Full wafer CAD view of graphene transfer wafer, including detailed view of VDTs and TSVVs.

The first stage of processing involves the etching of the SiO_2/Si substrate wafer to producing the VDTs and TSVVs. Figure 4.16 illustrates the two etching steps required for substrate wafer fabrication. The substrate wafer is patterned with the VDT photomask using a photoresist etch mask, using the photolithography process AZ 125 nXT protocol can be found in section 3.5.4. The thermal SiO_2 coating (300 nm film) is first etched using RIE SiO_2 etch recipe for 12 minute to etch through the full thickness of SiO_2 (protocol found in section 3.6.3). The VDTs are then etched out of the bulk silicon 200 μm deep using Bosch process deep silicon etching using ICP (SPTS Technologies), (protocol found in section 3.6.2). The photoresist is removed using Solvent Clean process.

The back side of the wafer is then patterned with the TSVVs photomask. A similar photolithography process and RIE etch process are used to reveal the bulk silicon. The wafer is bonded to a carrier wafer before a ICP Bosch process etching

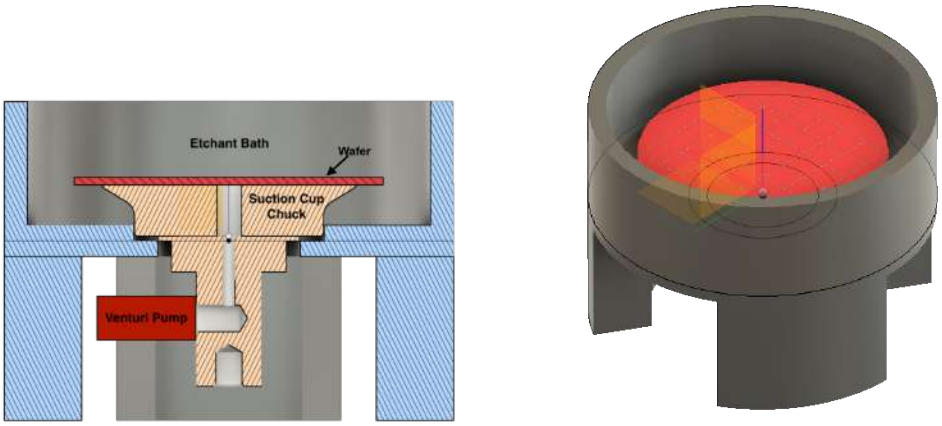
is performed to etch the remaining 300 μm depth of the wafer, (the carrier wafer is required to prevent gas flow in the ICP chamber after through silicon via penetration). The wafer was then de-bonded, the bonding agent (crystal bond, Agar Scientific) was removed and photoresist etch mask is also removed using Solvent Clean process.



(a) (b)

Figure 4.16: Etch steps required for graphene transfer substrate. (a) VDT etched on top side of substrate wafer. (b) TSVV etched through from back side of wafer.

A custom wet transfer rig was designed and printed to accommodate a vacuum chuck, venturi tube system and bath like structure to contain the wet etchant. Figure 4.17 outlines the components of the Transfer Rig, polymer alloy 910 (Taulman Ltd, UK) used to print the rig is etchant and solvent resistant, the suction cup chuck was purchased from RS components and has a 80 mm diameter cup. The Vacon venturi pump (PSI tech Ltd, UK) using set flow of rate of 3.2 scfm.

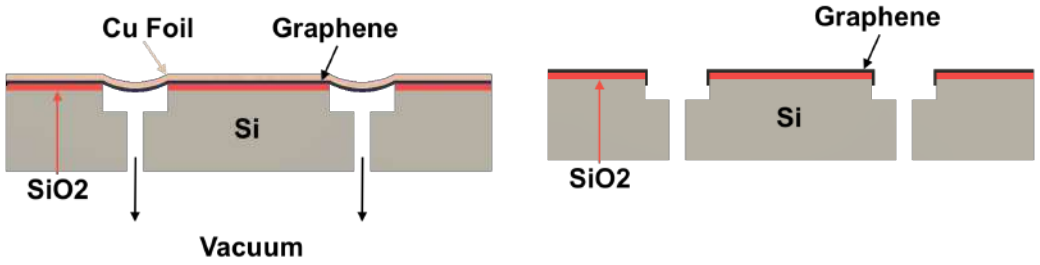


(a) (b)

Figure 4.17: (a) Cross Section of the Transfer Rig. (b) 3D view of Transfer Rig with substrate wafer connected to suction cup chuck.

The etched silica substrate wafer is then treated with a 10 minute RIE O_2 plasma clean O_2 plasma recipe found in section 3.6.1. The O_2 plasma treatment modifies the surface making it hydrophilic to improve graphene surface adhesion, by reducing trapped H_2O between the graphene and SIO_2 surface [16].

The graphene on Cu foil is applied to the substrate wafer, graphene-side down. A vacuum source is applied to the back side of the wafer which applies a stretching force to the Graphene on Cu foil (Monolayer graphene on Cu foil 100 mm Graphenea, Spain), The graphene and Cu foil is stretched across each individual die removing wrinkles from the Cu foil. The etchant bath is filled with 0.1 M ammonium persulfate (Sigma Aldrich, UK) whilst the vacuum is maintained on the wafer and graphene. Over a 4 - 5 hour period the Cu layer is etched away leaving the graphene layer on the SiO_2 surface. The etchant bath was emptied of remaining etchant and cycles of di H_2O were flowed through the bath to dilute and remove remaining ammonium persulfate. The wafer was then removed and vacuum dried at 120 °C to improve adhesion between the graphene and silica substrate. Figure 4.18 outlines the graphene stretching and Cu etching process.



(a) (b)

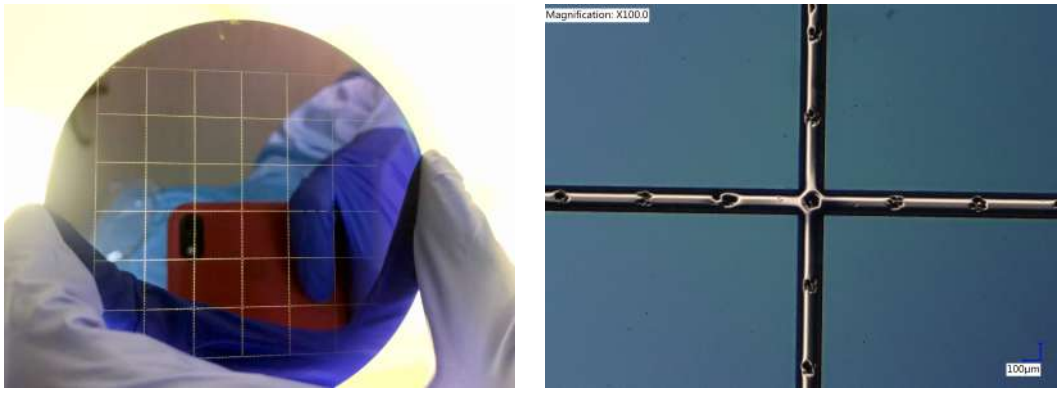
Figure 4.18: (a) Cross Section of vacuum stretching of graphene and Cu foil. (b) Cross section of graphene transfer post Cu etch and di H_2O rinse.

Raman Data Acquisition

Raman point measurements were performed on patches and regions of graphene found on the wafer surface. Single point measurement parameters can be found in section 3.12.3.

4.3.2 Results & Discussion

The substrate wafer was successfully prepared using a combination of RIE and ICP etching techniques. Figure 4.19 shows optical images which confirm the presence of TSVVs within the VDTs.



(a) (b)

Figure 4.19: (a) Full wafer VDT and TSVV etches complete. (b) Optical image of VDT corner section and TSVV at the base of the track.

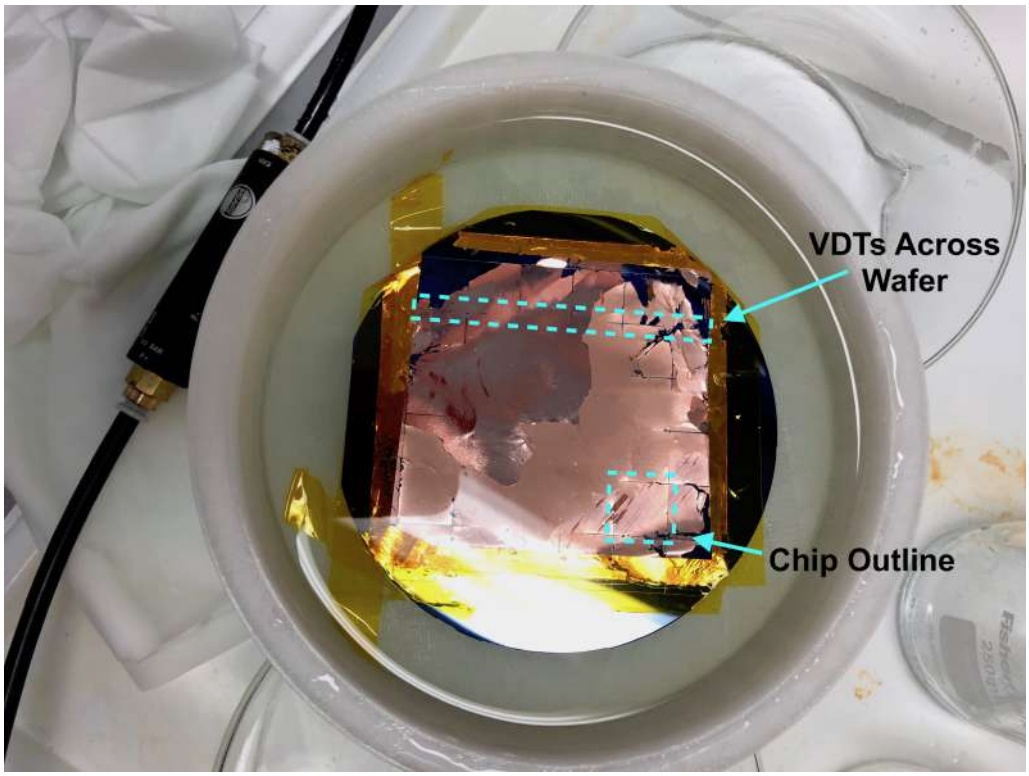


Figure 4.20: Vacuum graphene transfer process, 2 hours through Cu etch step.

Figure 4.20 shows the vacuum process was able to hold the graphene Cu foil tightly onto the substrate surface without visible wrinkles under solution. The graphene transfer process uses the ammonium persulfate to etch the Cu foil. The

VDTs can be seen clearly outlining the individual square chips.

Post Cu etch and di H_2O rinse cycles the surface was examined using Raman spectroscopy. Large regions of the graphene did not transfer successfully due to low surface adhesion between the graphene and SiO_2. Figure 4.21 shows Raman map of regions close to the VDTs showing concentrations of carbon but no monolayer graphene present. The peak at 1600 cm^{-1} represents amorphous carbon suggesting residue from delaminated and damaged graphene [17].

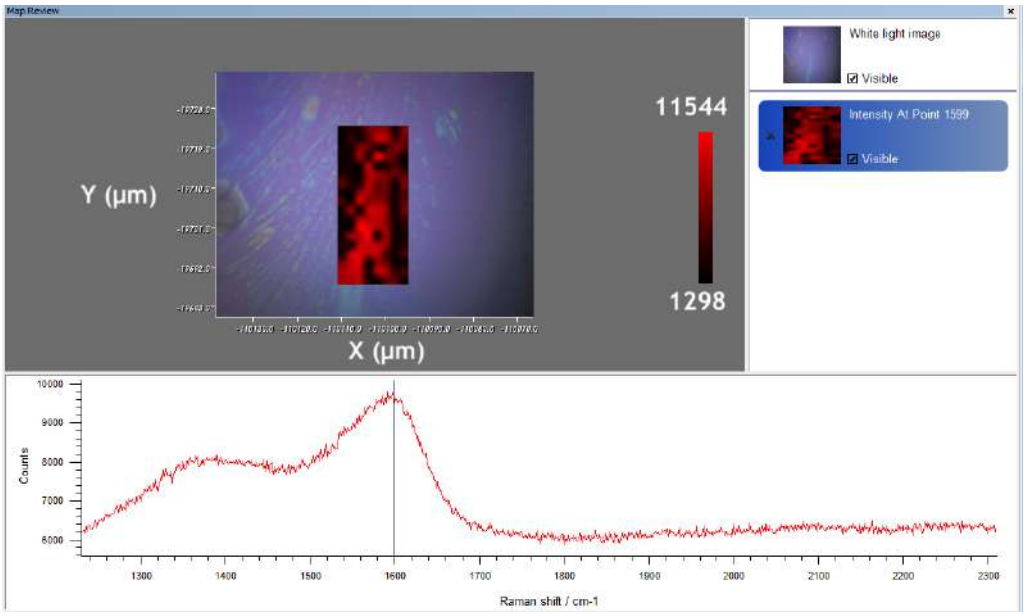
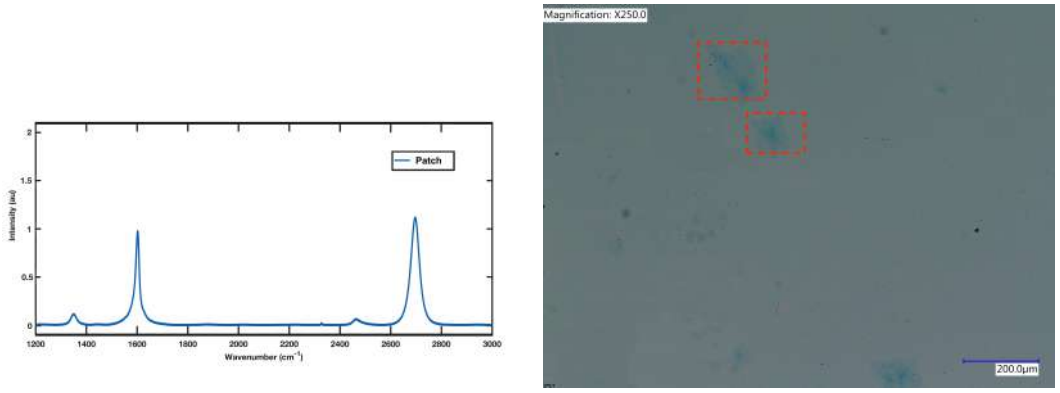


Figure 4.21: Raman map scan of carbon residue from graphene transfer region.

Looking at regions of discolouration on the SiO_2 a majority of areas show no signs of graphene, These discolourations are most likely caused by ammonium persulfate residue. However, specific spots of the wafer show signs of graphene being present (Figure 4.22). This suggests graphene transfer via the vacuum transfer process is possible. Graphene transfer onto semiconductor substrates without the use of photoresist/polymer support structures is thus achievable. This opens up the potential for larger scale graphene transfer onto commercial sized wafers (200 mm +).



(a) (b)

Figure 4.22: Single point measurement of graphene patch located on graphene transfer substrate.

4.4 Fabrication Process Optimisation

This high cost of graphene chips is related to graphene growth and the integration of the graphene layer (transfer step) into the wafer processing.

The Pre-Transfer process flow was reviewed at each main fabrication step, where possible alternative materials or techniques were compared. (1) The effect of pre-process vacuum annealing on graphene channel yield and the damage/doping of the graphene surface. (2) The photoresist steps were reviewed and the types of photoresist were compared for residues, damage and doping effects. (3) The device performance and yield were compared changing the types of metal deposited for contact electrodes. (4) The Pre-Transfer process was then compared to the Pre-Transfer Yttrium process in terms of yeild, device variance, damage and doping.

The Post-Transfer process flow was also reviewed at each key process step. The use of pre-process vacuum annealing and the effect on device yield. The metals used in the contact electrodes and the effect on yield as well as device performance. In order to assess the effect of fabrication processing on graphene quality. Blank graphene was compared directly to a fully fabricated device looking at the effect of the photoresist used on non-annealled graphene in terms of damage/doping. Additionally the effect of different substrates on electrical performance was investigated and the use of a buried contact process was compared to standard Post-Transfer process in terms of yield of devices.

The optimised fabricated devices for each process were then reviewed comparing the electrical performance, damage, doping and surface cleanliness.

4.4.1 Materials and Methods

Annealing Experiment Setup

Annealing procedure improves adhesion between the graphene and the SiO_2/Si substrate. This was apparent from devices fabricated where there was less delamination of graphene during device processes after annealing.

The effects of Vacuum tube furnace annealing (TFA) and rapid thermal annealing (RTA) on graphene damage/doping were compared. The operating procedure for the tube furnace and RTA can be found in the Materials & Methods Chapter section 3.4.

Vacuum oven annealing was performed using a Binder Vacuum Oven (Binder GmbH, Germany). Pumped to a pressure of 10^{-3} bar with a temperature set to 200 °C and 100 sccm Argon gas flow rate.

To investigate the longevity of the increased adhesion, three pieces of 20 x 20 mm graphene on SiO_2/Si were diced (allowing processing of 24 graphene channels Dense Design chip) from the same graphene wafer F55648 (Graphenea). Each piece was annealed by TFA at 400 °C followed by fabrication using the Pre-Transfer fabrication process within the following day, 2 days, 3 days, 4 days and 7 days.

Photoresist Comparison Experimental Setup

To compare the effect of photoresists used during the Pre-Transfer process fabrication on graphene damage, doping and surface residues 20 x 20 mm graphene on SiO_2/Si samples were prepared by TFA annealing and put through a Solvent Clean process. Sample 1 was left untreated as the control; sample 2 was coated with MicroPosit positive photoresist using the single layer Microposit protocol followed by a Solvent Clean; sample 3 was also coated with MicroPosit followed by a Solvent Clean and a LOR Remover clean and sample 4 was coated with Bi-Layer photoresist protocol followed by Solvent Clean and LOR Remover clean.

Adhesion Metal Comparison Experimental Setup

To asses the effect of metal adhesion to graphene on the final device resistance a quarter wafer of Graphene Resistor Chip (GRC) design two terminal resistors were fabricated using each candidate adhesion metal Cr, Ni and Ti. A thickness of 20 nm of adhesion metal with 80 nm of a capping noble metal Pd. Each test piece was used for each metal was approximately 50 mm x 25 mm graphene on SiO_2/Si

samples, each had a total of 112 graphene channels per adhesion metal. Wafer number F55537 from Graphenea was used to conduct this investigation, to reduce total error introduced from inter-wafer variability.

Resistance data processing: Outliers calculated based on 1.5 x the interquartile range (IQR) below IQR_1 and above IQR_3 were removed from the Box and Whisker plot

Dielectric Substrate Comparison Experimental Setup

When comparing substrate dielectrics on graphene channel resistance as part of the Post-Transfer fabrication process, two starting substrates were compared. SiO_2 300 nm on Si wafers (University Wafer Imc. USA). Silicon Nitride/Silicon wafers (University Wafer Inc. USA) With 100 nm Low Pressure Chemical Vapour Deposition LPCVD grown on bulk Si P type wafers. The Post-Transfer process was followed using Cr 20 nm Pd 80 nm metal stack for the metal electrodes using the Dip Chip Design.

Yttrium Deposition

For ytrrium sacrificial layer Pre-Transfer fabrication process, the first process step involves evaporating yttrium onto the graphene on SiO_2/Si wafer. The parameters for deposition of yttrium using the Quorum Sputter Coater set up as a thermal evaporator as described in the Materials & Methods Chapter section 3.7.2.

Yttrium Etch

For yttrium sacrificial layer Pre-Transfer fabrication process, there are three steps that involve removing the yttrium from the graphene surface; (1) prior to graphene etch step, (2) prior to metal deposition step, (3) final fabrication step removing yttrium from the graphene channel. The wet etch process was performed using 0.2 M HCl for 30 - 60 s. This was based on the methodology outlined by Wang et. al. [9].

RIE SiO_2 Etch

As part of the Inverted MOSFET design fabrication process flow, the dielectric layer (SiO_2) which is deposited onto the metal electrodes. This SO_2 layer requires etching to expose the metal for electrical contacts.

Additionally, for buried back contact process flow SiO_2 etching is required. Photoresist etch-masks are used to selectively etch the SiO_2 substrate.

Prior to SiO_2 etching the RIE chamber is cleaned using an O_2 plasma for 30 minutes (Materials & Methods Chapter, section 3.6.1). Once the SiO_2 sample is loaded into the RIE the surface is cleaned using an O_2 plasma (section 3.6.1) for 30 seconds. The sample is then removed from the RIE. The chamber is conditioned using SiO_2 etch recipe for 15 minutes. The sample is then loaded into the RIE for etching. The SiO_2 etch recipe can be found in Materials & Methods Chapter section 3.6.3.

Al_2O_3 Etching

For both the Inverted MOSFET and Matrix design process flows, Al_2O_3 is deposited as a dielectric insulation layer. For selective etching of the Al_2O_3 layer, photoresist etch-masks are patterned onto the wafer using AZ400K developer as the developing reagent during photolithography.

Al_2O_3 was then wet etched using AZ 726 developer (Microchemicals GmbH, Germany) etching protocol found in Materials & Methods Chapter section 3.6.5.

IV Measurement Data

IV measurements were performed using IV probe station and SD card PCB connector system. Standard IV sweep -1 to 1 V (measurement protocol found in Materials & Methods Chapter section 3.11.1).

IV Data Processing

The csv files were processed in Excel (Microsoft, USA). Voltage was plotted against current. The resistance was then calculated from inverse of the slope from the linear region of the I-V graph, (python software).

Resistance Data Processing

Resistance data calculated from IV measurements was then graphed using box and whisker plots (Prism 6 Software, GraphPad Ltd). Showing the mean, 25th to 75th percentiles and the upper and lower extremes of the resistance data range.

Relative standard deviation was calculated using standard deviation of the sample over the sample mean, multiplied by 100 to give the resulting percentage (Excel).

Comparisons of resistance data sets was performed using unpaired t-test with Welch's correction for non equal variance (Prism 6 Software, GraphPad Ltd).

Raman Data Acquisition

Acquisition settings for Raman map scans can be found in the Materials & Methods Chapter section 3.12.

Raman Data Processing

Structural damage due to annealing were characterized by Raman spectroscopy. The spectral ratio of the I_D/I_G can be used as a quantitative structural damage to the SP^2 bond structure with 0 resembling perfect bond structure and 1 representing SP^3. From ID/IG, one can then derive the average domain / grain size (L_a) of the resulting graphene layer using the following formula,

$$L_a(nm) = 2.4 \times 10^{-10}\,\lambda^4\,(I_D/I_G)^{-1} \tag{4.4.1}$$

Where λ is the wavelength of the laser (nm). The resulting graphene layer thickness and doping can also be characterised from the ratio 2D to G peak. In a pristine monolayer graphene the ratio I_{2D}/I_G should be close to 2 [18].

The spectral ratio of I_{2D}/I_G is used as an indicator of graphene layer thickness with 2 representing monolayer graphene. Changes to this ratio during fabrication can be an indicator of graphene doping.

In order to compare the amount of substrate-induced strain and doping in graphene, scatter plots were created by plotting the 2D peak position (ω2D) versus G peak position (ωG). This data was extracted from the Raman map scans and plotted based on the method created by [19], [20].

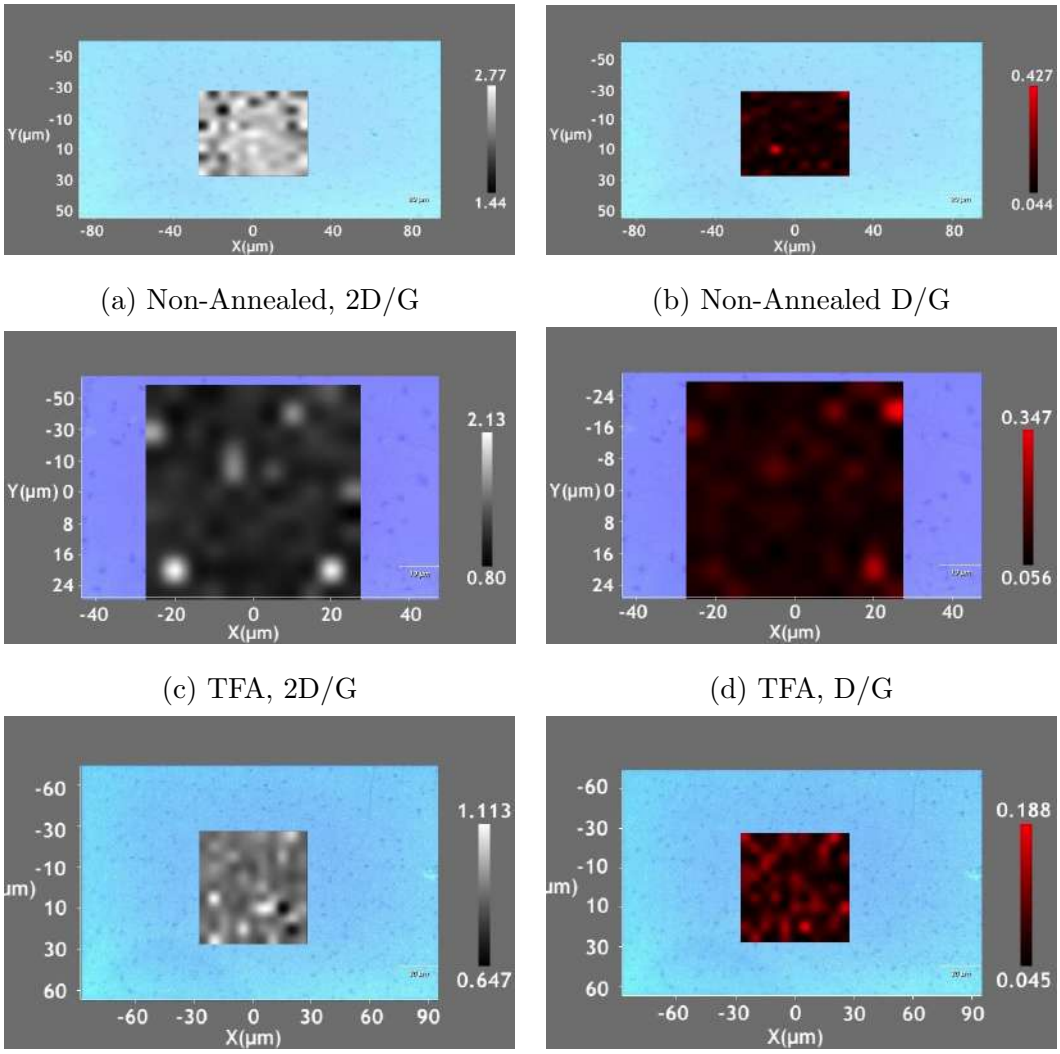
4.4.2 Results & Discussion

Pre-Transfer Process: Conditional Annealing Step

The pre-process annealing of graphene was optimised previously using tube furnace annealing (TFA) at 400 °C for 8 hours [1]. The temperature range assessed previously was determined to be with in 400 - 700 °C (depending on annealing systems) [1]. Increased adhesion after annealing has been linked to covalent bonding to graphene structure (SiO to Graphene bonds). This effect was enhanced during TFA compared to rapid thermal annealing (RTA). To check on potential damage from long vacuum anneals, non-processed blank graphene was compared under different annealing conditions RTA 10 minute anneal and 8 hour tube furnace anneal at 400 °C with vacuum at (10^{-3} mbar).

Figure 4.23 shows the 50 x 50 μm map scans for the blank graphene, TFA graphene and RTA. The blank graphene map 2D/G shows a few patches where the ratio drops below a ratio of 1.5. This could indicate some multilayer regions or contamination/doping from transfer process. The blank graphene map D/G shows mostly low damage graphene with 1 region of high damage (0.4 ratio). The TFA 2D/G map shows a large shift down to a ratio around 1 for the majority of the graphene with a few patches staying at the 2 ratio (indicating small regions of pristine graphene post anneal). The TFA D/G map shows a similar trend to the blank graphene majority low damage 0.05-0.1 with a few patches near 0.3-0.4. This suggests that overall damage remains low across the graphene sample. The RTA

2D/G map scans also show a decrease down to a ratio of 1 for a majority of the map. The RTA D/G shows very few regions of damage with figures ranging from 0.04-0.2 across the map.



(a) Non-Annealed, 2D/G

(b) Non-Annealed D/G

(c) TFA, 2D/G

(d) TFA, D/G

(e) RTA, 2D/G

(f) RTA, D/G

Figure 4.23: Raman map scan 50 x 50 μm: (a) blank graphene 2D/G ratio, (b) blank graphene D/G, (c) TFA graphene 2D/G ratio, (d) TFA graphene D/G ratio, (e) RTA graphene 2D/G ratio, (f) RTA graphene D/G

Both the annealed samples appear to see a decrease in the 2D/G ratio, this could be caused by doping changes to the graphene during the annealing process. Doping can be introduced through annealing due to interactions with the SiO_2 substrate

at high temperatures as well as interactions with high temperature gases [21]. The maps scans show no distinctive patterns of damage or doping and the patches of damage appear to be random across the graphene surface even on the blank samples.

Figure 4.24 shows the normalised spectra of Raman map scans for non-annealed, RTA (10-minute) anneal and Tube Furnace (8-hour) anneal. As previously stated a decrease in the 2D peak for both annealing processes can be seen. Additionally, a peak shift can be seen for both the 2D and G peaks, these shifts suggest that the graphene has undergone either strain/doping during the annealing process [19].

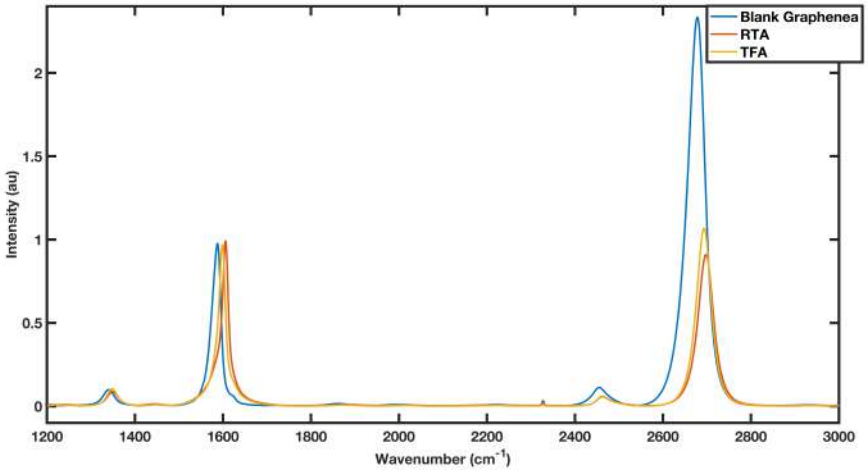


Figure 4.24: Raman spectra normalised and averaged from the map scan data of blank graphene, RTA treated graphene 10 minutes and TFA treated graphene 8 hours.

Figure 4.25 shows a scatter plot of ω2D and ωG for blank graphene and RTA annealed graphene. The data points for blank graphene lie centrally between the strain and doping axis this suggests that even the pre-processed graphene has experienced some nanometre-scale strain and P-type doping (hole-doping) from growth and transfer. The RTA annealed sample shows data points shifting both upwards along the strain axis and the P-type doping axis. This would suggest both an increase in strain due to the high temperature surface deformation expansion and cooling. An increase in doping, which could be due to electron removal due to the

high temperature creating SiO dangling bonds at the graphene/substrate interface.

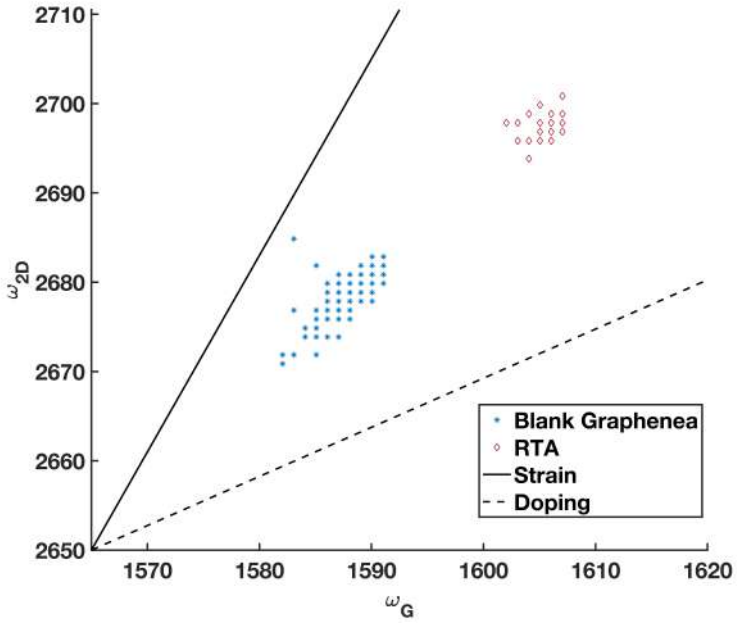


Figure 4.25: ω2D and ωG scatter plot of blank graphene compared to RTA annealed graphene.

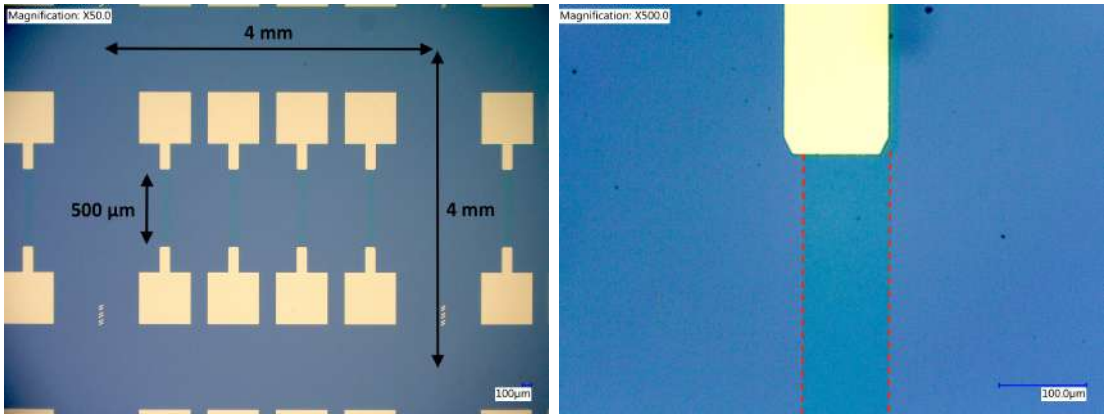
Table 4.6 shows the averaged ratios 2D/G, D/G and derived grain size L_a for the blank graphene, TFA and RTA annealing methods. The quantified results show no significant increase in damage or reduction in the extracted grain size (L_a) due to pre-process annealing, suggesting any CO and C=O bond formation during the anneal is rare and will not effect the SP^2 graphene structure greatly.

Table 4.6: Table of averaged peak ratios from Raman map scans of blank, TFA and RTA annealed graphene.

	I_{2D}/I_G Ratio	I_D/I_G Ratio	Approximate Grain Size (L_a)
Blank Graphene	2.3590 ±0.2004	0.0999 ±0.0470	192.4 ±90.5
TFA	0.9117 ±0.0673	0.0877 ±0.0272	219.2 ±68.0
RTA	1.0802 ±0.1608	1.0470 ±0.0349	183.6 ±61.2

To assess the effect of annealing on final device resistance a quarter wafer of GRC two terminal resistor chips were fabricated using each annealing method; a total of 112 graphene channels. As well as higher temperature RTA (700 °C); Tube Furnace (700 °C) and vacuum oven anneal 24 hours (200 °C), a set of control devices were fabricated without annealing. The 200 °C vacuum oven anneal was tested to improve fabrication efficiency as multiple wafers can be loaded and annealed by oven vacuum annealing.

GRC devices were fabricated using the standard 400 °C TFA and RTA anneal from the same Graphene wafer (F55513), for all 112 channels per process type. Figure 4.26 shows the fully fabricated GRC design devices for annealing experiments.



(a) (b)

Figure 4.26: (a) Keyence image 50x zoom of standard process fabricated GRC design. 4 graphene channels per 4 mm x 4 mm. (b) 500 x zoom graphene channel and metal contact pad region of individual channel.

Figure 4.27 shows the IV measurement data input bias vs measured current. This quantity of data cannot be visualised through this approach very accurately.

Figure 4.28 shows the resistances of each annealing process seen plotted in a box and whisker plot. This data shows subtle differences in the resistances for each annealing method. The majority of data points appear to be overlapping within the 25^{th} to 75^{th} percentile for each annealing method, this suggests no significant difference in resistance based on the fabrication annealing method.

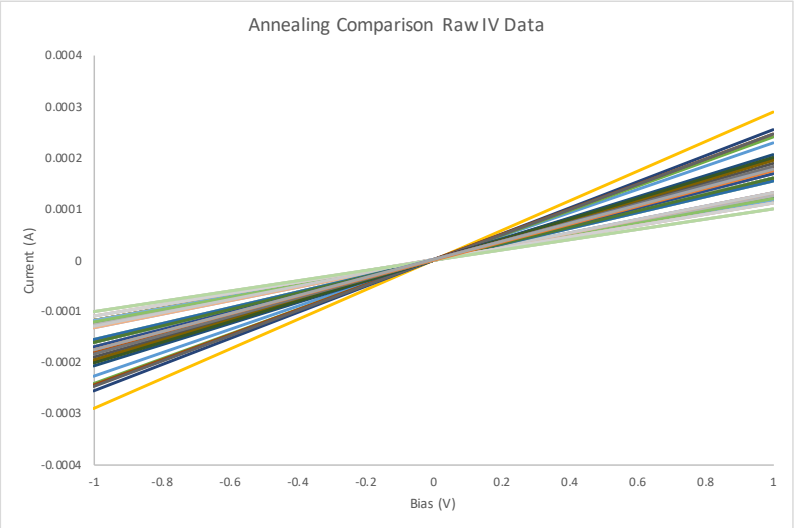


Figure 4.27: IV data -1 V to 1 V for 112 TFA and RTA annealed GRC devices

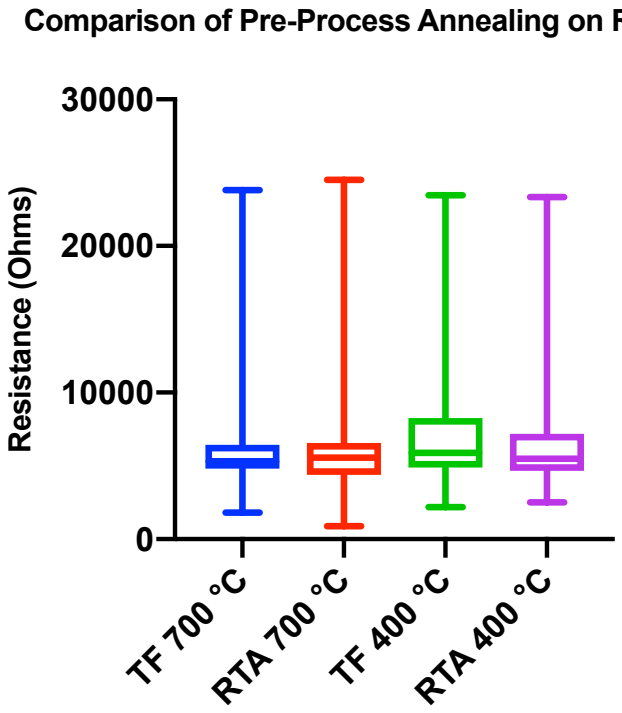


Figure 4.28: Comparison of each pre-process annealing method based on final device resistance calculated from two-terminal IV measurement. Box and whisker plot with highest and lowest resistance plotted at the end of each whisker, mean, upper and lower quartiles represented by the box.

The resistance data from the box and whisker plot shows the data being unevenly spread due to high resistance devices. Figure 4.29 shows the individual resistances measured for each of the 112 devices in the RTA 400 °C. The majority of the resistance data is below 10,000 Ω with only 6 devices above 15,000 Ω and one device above 20,000 Ω.

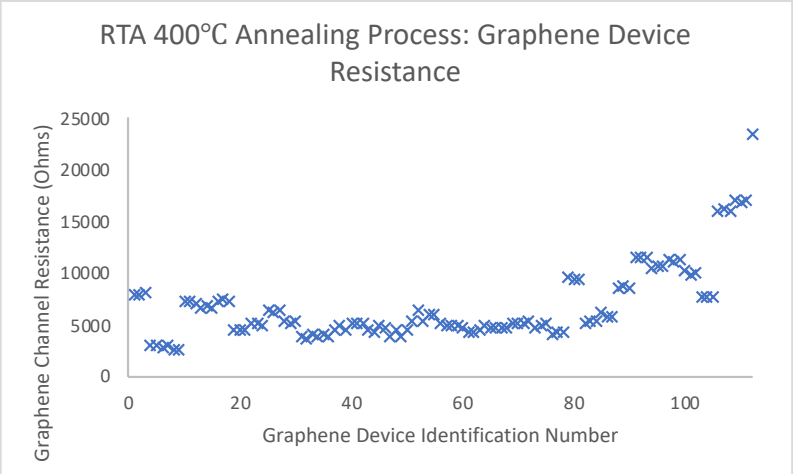


Figure 4.29: Spread of data for the 112 devices in the RTA 400 °C pre-transfer annealing comparison.

Table 4.7 shows the graphene channel yield per process and average resistance. The data shows that there is no statistical difference between the 700 °C Tube Furnace and RTA, or Tube furnace 700 °C and RTA 400 °C. There is a significant difference between each RTA temperature 700 °C and 400 °C, each Tube Furnace temperature 700 °C and 400 °C, and also the 400 °C Tube Furnace and RTA Mann Whitney test $P = 0.0227$ or smaller.

Overall the best approach based solely on resistance is not clear. All approaches produce a similar number of working devices with similar variability. Based on the literature, lower temperature high vacuum annealing reduces structural defects and doping. This would suggest the TFA 400 °C process was the better annealing process, even if it the data here does not show any main difference between them.

Table 4.7: Device median resistances per pre-process anneal type. Device yield: Number of working devices (devices that produce a linear resistance response). Device yield based on variability per quarter wafer number of devices with a resistance within 10 % of the median of the batch.

Process Type	Median Resistance (Ohms)	Device Yield Working Devices	Device Yield Within 10%
700 °C TF	5315±3154	95.5	12.8 %
700 °C RTA	5558±3312	97.3	10.1 %
400 °C TF	5887±3331	95.5	9.0 %
400 °C RTA	5476±3196	95.4	9.3 %

Annealing Process Time Dependency

Following the pre-process anneal TFA 400 °C, conducted overnight, process steps 2 - 4 take place within 24 hours routinely. According to Das et. al. annealing produces C-O and C=O bonds with the dielectric surface improving adhesion [22]. This would suggest a permanent increase in adhesion if SiO to C bonding was the sole contributor to the increase in adhesion post annealing.

Table 4.8 shows the total number of graphene channels that produced a linear IV response/device yield. The data set will need repeating before conclusions can be made, but the preliminary data suggests that fabrication within 3 days of annealing is required for a good device yield. This also suggests that the annealing process does not permanently increase graphene substrate adhesion.

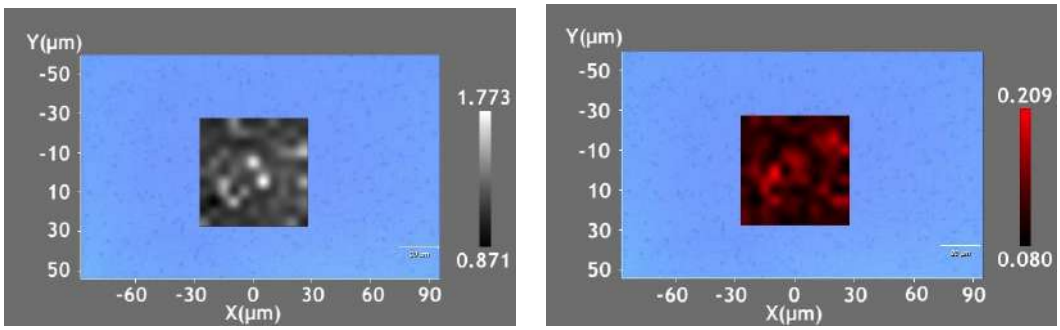
Table 4.8: Device yield (graphene channels that show a linear IV characteristic), with remaining fabrication steps of the Pre-Transfer process started within a set time period after the pre-process anneal step.

Time Period of Fabrication Post Pre-Process Anneal	**Device Yield (%)**
<24 hours	96
24 - 48	100
48 - 72	92
72 - 96	8
168 - 192	0

The other effect of graphene/substrate annealing is the removal of H_2O molecules from the surface and between the graphene and SiO_2 substrate. This has been shown to improve carrier concentration, reducing the effect of the H_2O molecules on the doping and charge scattering of the graphene [23]. The removal of this interfacial H_2O layer could temporarily improve graphene adhesion to the SiO_2. Post annealing the H_2O molecules slowly return decreasing the adhesion.

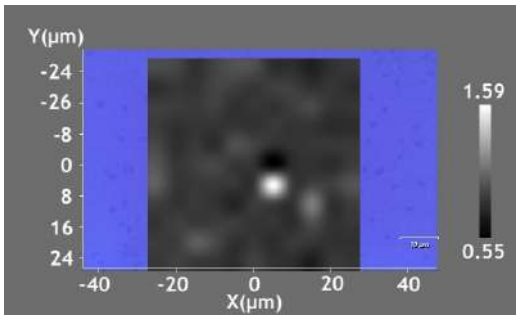
Pre-Transfer Fabrication Process: Comparison Of Photoresist

The Pre-Transfer fabrication process requires the use of 2 photolithography steps; one for metal lift-off step using a Bi-Layer photoresist (PR) protocol and, two an etch mask step using a single layer positive PR MicroPosit single layer protocol. Figure 4.30 shows the Raman map scans with the 2D/G ratio and D/G ratio displayed for each of the photoresist comparison samples after removing the photoresists. The blank sample (annealed and Solvent Cleaned) shows a similar ratio scales to the cleaned PR test samples, where each map scan shows evenly distributed areas of damage and doping with minimum hot spots. This suggests the graphene samples are fairly representative without any significant flaws or double layer patches. After resist processing with both Bi-Layer and single layer positive PR.

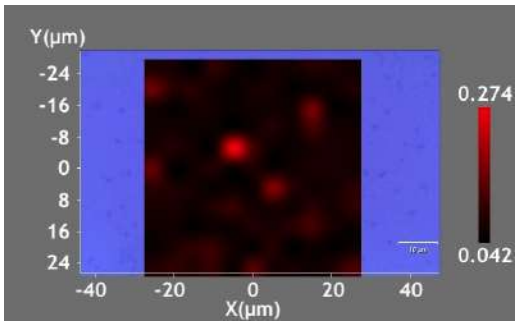


(a) Blank, 2D/G

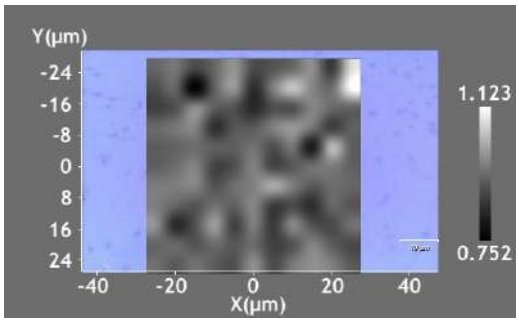
(b) Bank, D/G



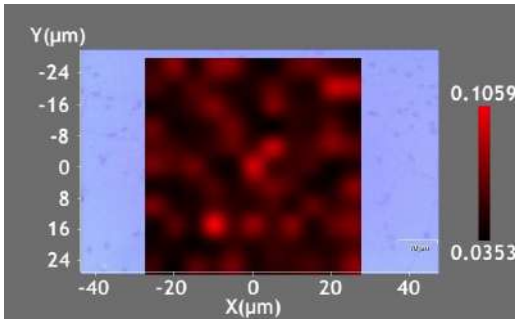
(c) Single layer PR, 2D/G



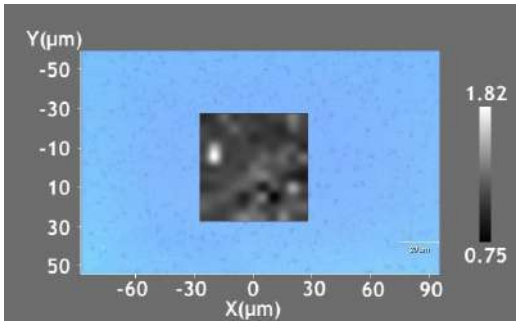
(d) Single layer PR, D/G



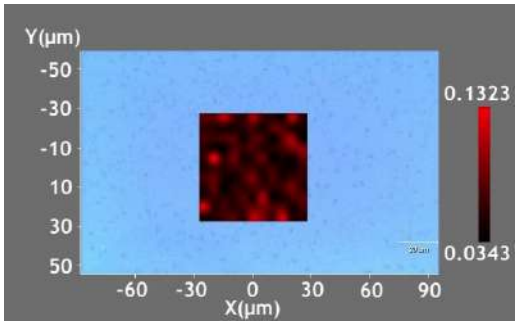
(e) Single layer PR + Extra Clean, 2D/G



(f) Single layer PR + Extra Clean, D/G



(g) Bi-layer PR + Extra Clean, 2D/G



(h) Bi-layer PR + Extra Clean, D/G

Figure 4.30: Raman map scan 50 x 50 μm: (a) Blank graphene 2D/G ratio, (b) Blank graphene D/G ratio, (c) MicroPosit Solvent Cleaned graphene 2D/G, (d) MicroPosit Solvent Cleaned graphene D/G, (e) MicroPosit Solvent Clean and LOR Remover Clean graphene 2D/G, (f) MicroPosit Solvent Clean and LOR Remover Clean graphene D/G, (g) Bi-Layer Solvent Clean and LOR Remover Clean graphene 2D/G, (h) Bi-Layer Solvent Clean and LOR Remover Clean graphene D/G.

Figure 4.31 shows the normalised spectra of Raman map scans for photoresist comparison samples. Similar to the map scans there are no distinct differences in height between 2D or G peaks between the samples. There are also no notable peak shifts that would indicate signs of doping or strain applied to the sample for any of the photoresists.

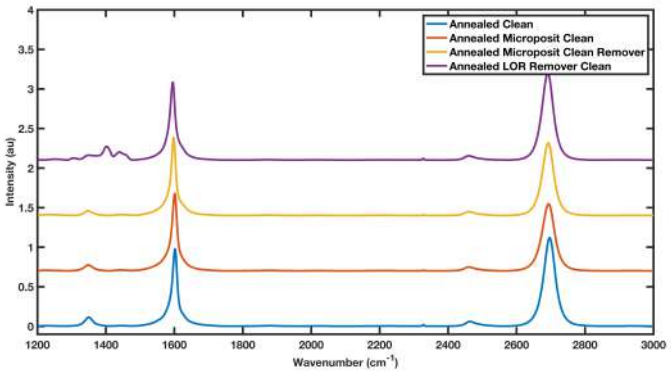


Figure 4.31: Raman spectra normalised and averaged from the map scan data of blank graphene, Microposit Solvent Cleaned (SC), Microposit SC and LOR Remover Cleaned, Bi-Layer SC and LOR Remover Cleaned.

From the averaged map spectra of the Bi-Layer photoresist sample it is clear that there are additional peaks in the 1280 - 1480 cm^{-1} region surrounding the G peak region (Figure 4.32. These additional peaks indicate the presence of additional carbon bonds, as they aren't present in the other spectra. This is likely due to photoresist residue from the LOR5A component of the Bi-Layer photoresist [24]. This suggests the Bi-Layer photoresist process for metal lift-off leaves residue on the graphene surface. These residues could interfere with graphene functionalisation and effect the graphene's conductivity due to their charge scattering effects on the graphene's pi orbitals reducing the free movement of electrons. Peaks associated with PMMA such as O=C-O-CH_3 appear at 1397.

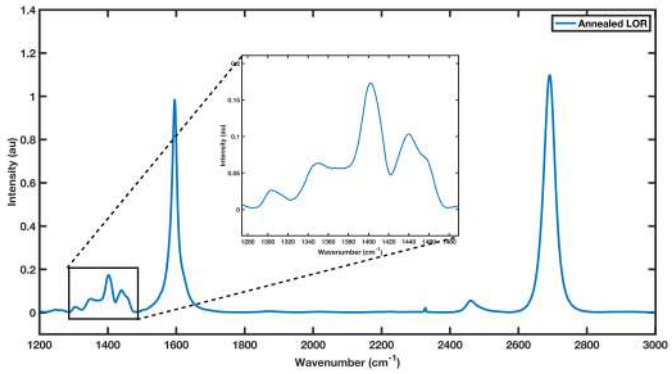


Figure 4.32: Averaged Raman spectra from map scan data of Bi-Layer photoresist protocol (LOR) followed by Solvent Clean and LOR Remover process

Table 4.9 shows the averaged ratios 2D/G, D/G and derived grain size L_a for the blank graphene, Microposit Solvent Cleaned (SC), Microposit SC and LOR Remover Cleaned, Bi-Layer SC and LOR Remover Cleaned methods. The quantified results show no significant increase in damage or doping from any of the photoresist processes compared to blank graphene.

Table 4.9: Average peak ratios and calculated grain size for different photoresist processes.

	I_{2D}/I_G Ratio	**I_D/I_G Ratio**	**Approximate L_a Grain Size (nm)**
Blank	1.1292 ±0.1288	0.1146 ±0.0188	167.8 ±27.5
MicroPosit PR, SC	0.8588 ±0.0476	0.0584 ±0.0117	329.2 ±66.0
MicroPosit PR, SC + Remover	0.9258 ±0.0769	0.0743 ±0.0241	258.7 ±83.9
LOR & MicroPosit PR, SC + Remover	1.1058 ±0.1037	0.0655 ±0.0150	293.5 ±67.2

Pre-Transfer Fabrication Process: Comparison Of Adhesion Metal Used In Metal Contact Stack & Effect On Yield & Resistance

For the Pre-Transfer process, fabrication of the first metal deposited (adhesion layer) does not solely make contact with the graphene but also makes contact with the wafer substrate (SiO_2/Si). In the case of the 3 Graphene Channel Dip Chip Design the area of adhesion metal making contact with the graphene per chip was 0.15 mm^2 (Figure 4.33, whilst the total area of the electrodes in contact with the SiO_2 was 18.55 mm^2.

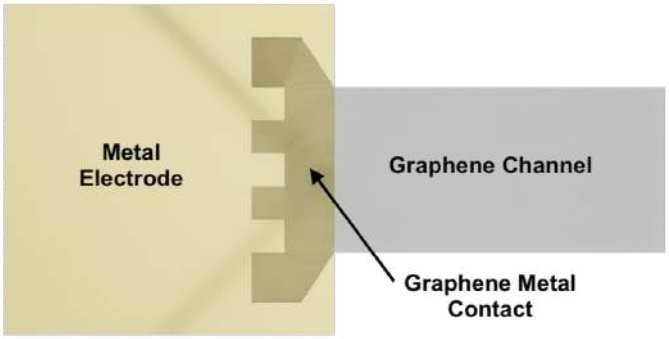


Figure 4.33: Diagram of metal contact pad and graphene channel, showing metal graphene contact area.

The three metals used in both the semiconductor industry as a whole and specifically in graphene FET fabrication are Cr, Ni, and Ti [25] [26]. In Pre-Transfer fabrication the adhesion metal is PVD deposited onto the SiO_2/Si substrate and the castellated contact region of the graphene channel simultaneously. The contact resistance of these metals on graphene has been previously been investigated [27] [28]. This previous work had established both Titanium and Nickel as having some of the lowest contact resistances on average, Other metals such as Cobolt and Palladium also showed low contact resistance. However, these were not investigated at this stage due to them not being good adhesion metals for the SiO_2 substrate.

Figure 4.34 shows box and whisker plot for adhesion metal comparison. The median calculated resistance for Cr was found to be the lowest at 5255 $\pm$2334 Ω

followed by Nickel at 6163 ±3572 Ω and then Titanium at 6414 ±552 Ω. Chromium resistance was shown to be significantly lower than both Nickel and Titanium, (Mann Whitney test $P < 0.0001$). There was no significant difference between the Nickel and Titanium resistance values.

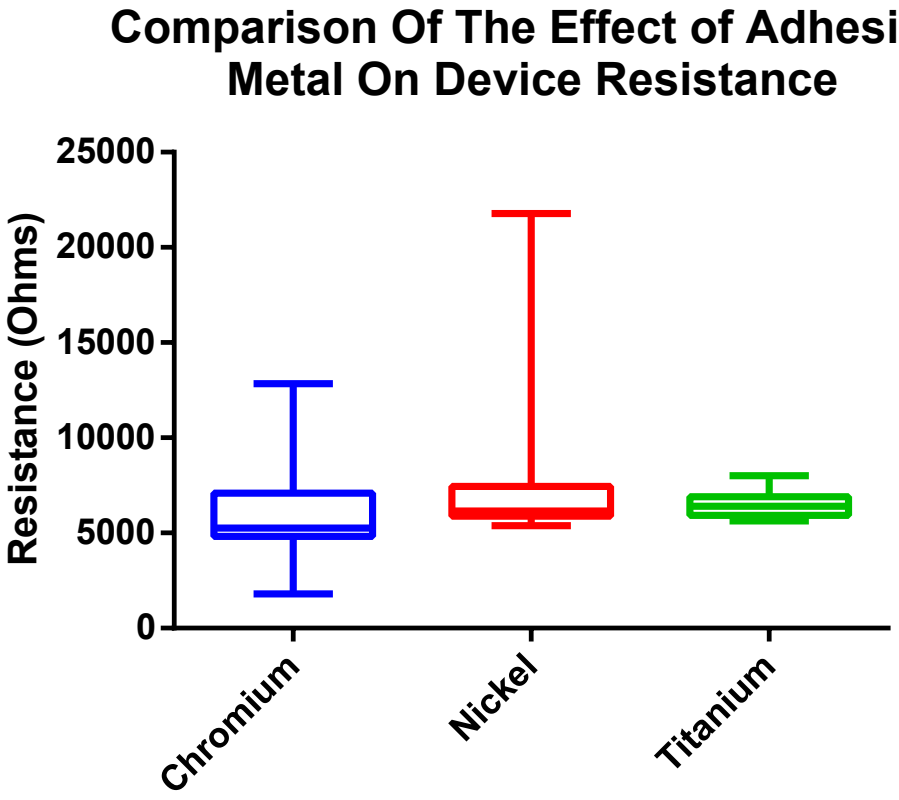


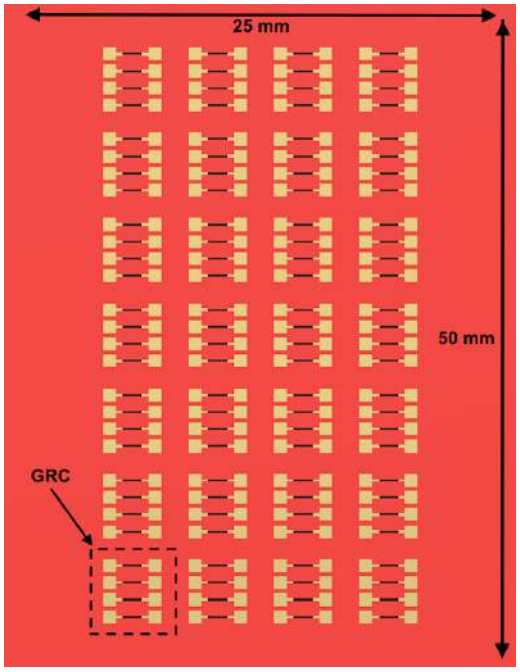
Figure 4.34: Box and whisker plot of device resistances comparing adhesion metals Chromium, Nickel and Titanium in contact with the graphene. Box and whisker plot with highest and lowest resistance plotted at the end of each whisker, median, upper and lower quartiles represented by the box.

Effect Of Device Position On Resistance To understand the accuracy of these resistance results the device resistances and physical location on the wafer were investigated.

Figure 4.35 was created using the data from the adhesion metal comparison

showing graphene resistance (Ω) and physical position within the wafer. Each SiO_2 substrate as previously mentioned is 50 mm x 25 mm giving an area 1250 mm^2 with graphene channels clustered in groups of 4 per chip.

A comparison of average graphene channels resistances for Titanium data set. The average resistance of the left hand column (6761 Ω) and right hand column (6105 Ω) of devices were shown to be significantly different (unpaired Mann Whitney test P = 0.0010). The average resistance of the top row (6075 Ω) and bottom row (7417 Ω) devises were shown to be significantly different (unpaired Mann Whitney test P = 0.0286). This suggests the physical location of devices within a process wafer affects the resistance as significantly as the adhesion metal used.



(a) GRC Array

4955 Ω	4836 Ω	6317 Ω	8354 Ω
4940 Ω	5213 Ω	9179 Ω	3466 Ω
5814 Ω	6393 Ω	11820 Ω	3265 Ω
1810 Ω	5081 Ω	10921 Ω	7560 Ω
1817 Ω	5481 Ω	11669 Ω	7093 Ω
3162 Ω	10078 Ω	10346 Ω	7621 Ω
3175 Ω	8076 Ω	8089 Ω	4878 Ω
7232 Ω	8439 Ω	16558 Ω	5424 Ω
10945 Ω	12986 Ω	17352 Ω	6781 Ω
5911 Ω	6576 Ω	23767 Ω	5779 Ω
4099 Ω	4550 Ω	9472 Ω	4317 Ω
5057 Ω	4573 Ω	5135 Ω	4303 Ω
10937 Ω	11394 Ω	4684 Ω	5112 Ω
13615 Ω	12840 Ω	5049 Ω	5313 Ω
7919 Ω	8653 Ω	4784 Ω	4944 Ω
10601 Ω	8726 Ω	4621 Ω	5448 Ω
5450 Ω	6184 Ω	4899 Ω	9014 Ω
2861 Ω	2133 Ω	4718 Ω	9880 Ω
1611 Ω	2127 Ω	4861 Ω	5688 Ω
4334 Ω	2362 Ω	4943 Ω	5280 Ω
5641 Ω	6368 Ω	5255 Ω	4804 Ω
3671 Ω	4294 Ω	5195 Ω	5179 Ω
5338 Ω	6068 Ω	5176 Ω	5309 Ω
4469 Ω	4921 Ω	4831 Ω	5679 Ω
3977 Ω	4697 Ω	8222 Ω	5316 Ω
5839 Ω	6316 Ω	4956 Ω	4522 Ω
4321 Ω	4869 Ω	5997 Ω	9815 Ω
4289 Ω	5022 Ω	5227 Ω	5656 Ω

(b) Chromium

5676 Ω	6142 Ω	6447 Ω	5800 Ω
5935 Ω	15353 Ω	5958 Ω	5839 Ω
5837 Ω	7506 Ω	6161 Ω	5931 Ω
5978 Ω	5870 Ω	6167 Ω	5821 Ω
5994 Ω	21610 Ω	22714 Ω	5934 Ω
6001 Ω	24028 Ω	23634 Ω	5633 Ω
12329 Ω	23161 Ω	12494 Ω	6046 Ω
34871 Ω	28657 Ω	12772 Ω	28989 Ω
17331 Ω	10232 Ω	X Ω	43212 Ω
12336 Ω	8729 Ω	6806 Ω	30573 Ω
16225 Ω	17981 Ω	6645 Ω	24135 Ω
21786 Ω	6367 Ω	7425 Ω	32991 Ω
34430 Ω	6459 Ω	6710 Ω	41678 Ω
12786 Ω	6425 Ω	6096 Ω	37110 Ω
11078 Ω	6293 Ω	6145 Ω	16236 Ω
11084 Ω	6232 Ω	6212 Ω	23281 Ω
9427 Ω	6106 Ω	6309 Ω	27033 Ω
6087 Ω	6164 Ω	6651 Ω	13994 Ω
7805 Ω	5946 Ω	6350 Ω	9176 Ω
6970 Ω	5738 Ω	6100 Ω	10114 Ω
5636 Ω	5883 Ω	6092 Ω	8164 Ω
5765 Ω	5846 Ω	6070 Ω	6139 Ω
5649 Ω	5842 Ω	6160 Ω	7403 Ω
5523 Ω	5708 Ω	27354 Ω	7028 Ω
5457 Ω	5906 Ω	6716 Ω	6415 Ω
5588 Ω	5764 Ω	6220 Ω	5924 Ω
5504 Ω	5892 Ω	5833 Ω	5860 Ω
5386 Ω	5930 Ω	6220 Ω	6364 Ω

(c) Nickel

X Ω	X Ω	X Ω	X Ω
X Ω	X Ω	X Ω	X Ω
X Ω	X Ω	X Ω	X Ω
X Ω	X Ω	X Ω	X Ω
5628 Ω	5898 Ω	6395 Ω	6251 Ω
5672 Ω	5895 Ω	5865 Ω	6392 Ω
6270 Ω	5926 Ω	6243 Ω	6124 Ω
5914 Ω	6176 Ω	6064 Ω	6053 Ω
6197 Ω	5959 Ω	5919 Ω	6616 Ω
5937 Ω	5859 Ω	6216 Ω	6037 Ω
5787 Ω	6015 Ω	5660 Ω	6485 Ω
6049 Ω	5777 Ω	6173 Ω	6401 Ω
5860 Ω	5869 Ω	6159 Ω	6825 Ω
5816 Ω	5861 Ω	6709 Ω	6800 Ω
5914 Ω	5731 Ω	5918 Ω	6699 Ω
5844 Ω	5705 Ω	6428 Ω	6752 Ω
5850 Ω	12237 Ω	7262 Ω	6927 Ω
5796 Ω	6547 Ω	7278 Ω	7439 Ω
6161 Ω	6189 Ω	6903 Ω	8009 Ω
6568 Ω	6463 Ω	6844 Ω	13199 Ω
6509 Ω	6958 Ω	6950 Ω	7795 Ω
6715 Ω	7024 Ω	6719 Ω	9570 Ω
6727 Ω	6818 Ω	7151 Ω	6770 Ω
6911 Ω	6765 Ω	6992 Ω	9588 Ω
6763 Ω	7062 Ω	6593 Ω	6591 Ω
7124 Ω	7086 Ω	7025 Ω	6355 Ω
7262 Ω	7292 Ω	X Ω	7207 Ω
9386 Ω	7520 Ω	7313 Ω	6942 Ω

(d) Titanium

Figure 4.35: Heat Map created using graphene channel resistance data and physical location of the graphene channels on the substrate. Colour coded from lowest resistance, represented as green, to the highest resistance or broken channel represented in red. (a) CAD graphic of Graphene Resistor Chip (GRC) array on 50 x 25 mm SiO_2/Si substrate. (b) visually shows no strong trend hot spots of low resistance. (c) visually shows some clusters of higher and lower resistance. (d) visually shows a gradient across the substrate from high to low resistance left to right.

Due to the large variation within each sample, further investigation was required to determine the adhesion metal that yielded the lowest resistance and highest device yield. Previous devices were fabricated based on the Graphene Resistor Chip design to increase total number of graphene channels per sample. This test was done using the Dip Chip design to mimic exact device production procedures. One 100 mm wafer from Graphenea wafer number F57339 was divided into 4 quarter pieces to reduce inter wafer variability for each of the adhesion metals tested. The extra quarter that Palladium (Pd) as the graphene contact metal. Previous experiments have shown Palladium produce a low resistance contact with graphene [29].

The resulting resistances were calculated from devices that produced a linear IV response. Each quarter wafer produced 8 Dip Chip Origin chips this gives a total of 24 graphene channels per metal tested. The device yield for linear IV working devices for Cr, Ni and Ti were all within the 96% - 100% range. However, the purely Pd based metal stack resulted in a device yield of 13%. This was caused by the metal contacts lifting off around the graphene due to pour adhesion with the SiO_2. The three resulting graphene channel resistances from the Pd quarter piece were not included in the analyses due to lower repeat number.

Table 4.10 shows the distribution of the adhesion metal resistance data in terms of skewness and kurtosis, as one or both of the calculated numbers are above 2 this suggests the data is not normally distributed for each metal [30]. Descriptions of skewness and kurtosis can be found in the Appendix 8.2.1

Table 4.10: Distribution data calculated from the adhesion metal comparison graphene resistances.

	Skewness	Kurtosis
Chromium	2.26	7.54
Nickel	1.87	2.63
Titanium	3.39	14.74

Figure 4.36 shows the resistance data for each of the metals tested. The Median

resistance for Cr was found to be the second lowest at 8190 ±1474 Ω with Nickel being the lowest at 6787 ±1493 Ω and Titanium the highest at 10865 ±2716 Ω. The Relative Standard Deviation was lowest for Chromium at 18% followed by Nickel at 22% with Titanium having the highest at 25%. Nickel was shown to be significantly lower than Chromium and Titanium, ($P = 0.005$ anf $P < 0.0001$ Mann Whitney test). Chromium was also shown to have a significantly lower resistance than Titanium, ($P < 0.0001$ Mann Whitney test). Both Chromium and Nickel have been reported in the literature as producing the lowest contact resistance to graphene. The most reported figure shows Nickel as producing the lowest contact resistance this could be due to its low carbon solubility, compared to Titanium which is likely to form Ti Carbides at low temperatures removing carbon from the graphene sheet [31] [32].

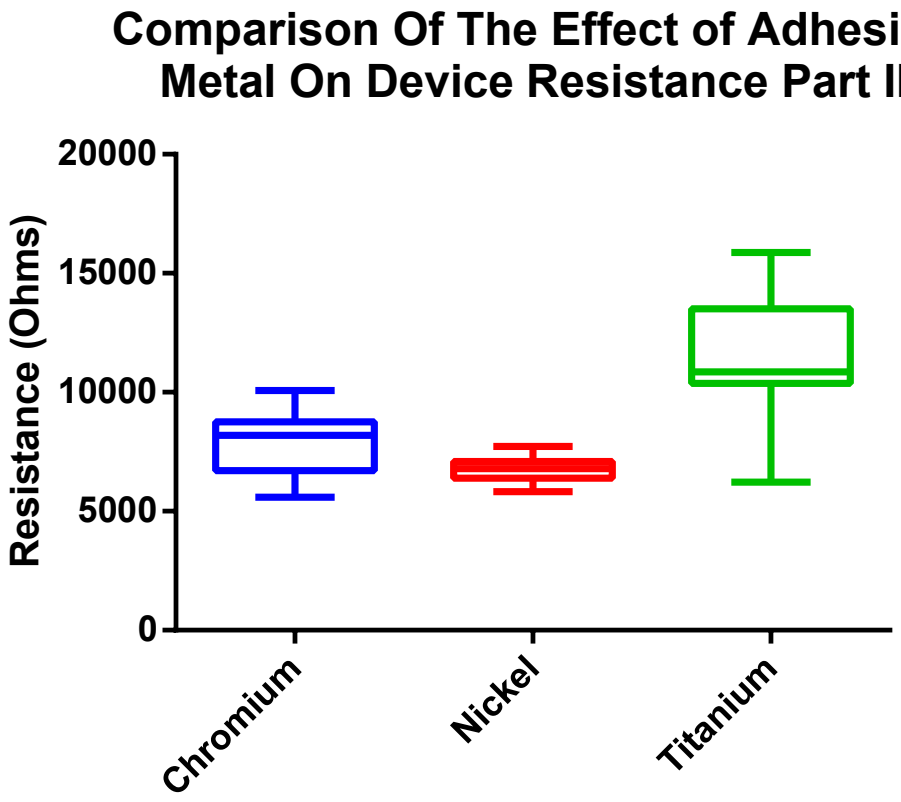


Figure 4.36: Box and whisker plot of device resistances comparing adhesion metals in contact with the graphene.

In conclusion both Nickel and Chromium produce graphene chips with very similar IV characteristics. Based on the literature Nickel is a better candidate for producing the lowest contact resistance. However, at this stage with the current length and high resistance of graphene channels either metal can be used for fabrication.

Pre-Transfer Yttrium Sacrificial Layer Process

The yttrium sacrificial layer integrated into the Pre-Transfer fabrication process flow was included to reduce contaminants (e.g. photoresist) from contacting the graphene surface, therefore not leaving residues after device fabrication.

The thickness of Yttrium deposited onto the graphene (and whole substrate

surface) was between 5 - 12 nm, based on internal crystal monitor reading of Quorum Sputter Coater, the thickness was then confirmed by Ellipsometry. Due to the lack of substrate shutter on the Quorum Sputter Coater whilst in thermal evaporation mode, precise termination at an exact thickness is not possible.

With the thickness variation the wet etch is also variable for each batch process. To identify an etch endpoint the colour change of the graphene channel is used as an indicator of yttrium removal. Figure 4.37 shows the graphene channel with yttrium present (light blue) and the graphene channel once Yttrium is etched away (dark blue/purple). The final wet etch step of the fabrication process removes the Yttrium from the entire graphene channel. All yttrium must be removed in order to functionalise the graphene channel (especially when π-π stacking functionalisation molecules).

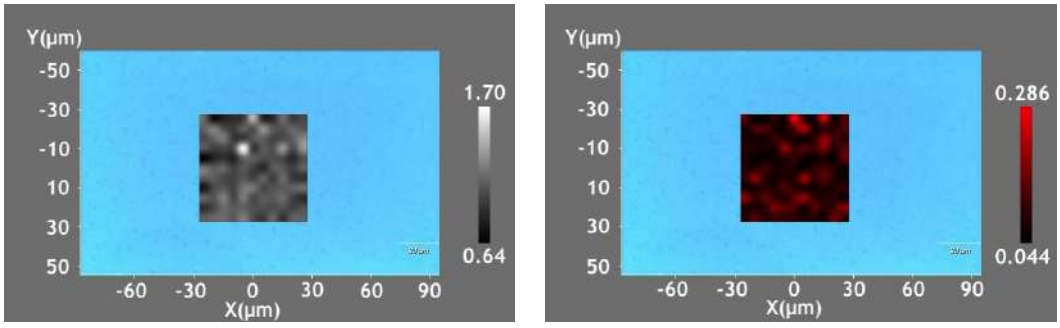
(a) (b)

Figure 4.37: Keyence 4000x zoom image of right hand edge of graphene channel and metal contact pad region. (a) Post metal lift off step 7a, yttrium layer remains on majority of graphene area (light blue colour). (b) Post HCl yttrium etch step 7b, Yttrium layer removed from graphene channel post 30 second etch.

The effect of graphene damage from Yttrium deposition was studied using both thermal evaporation (Quorum Technologies Q150) and magnetron sputtering (Lesker PVD 75). The PVD deposition parameters were trialled for Yttrium deposition on graphene to attempt a reduction in damage. Both the pressure and sputtering power

were reduced to their individual extremes and overall minimum settings, that were able to strike a plasma see and deposit material parameters in see Appendix. Each of these methods were tested on blank monolayer graphene 10 mm x 10 mm chips. However, these sputtering methods damage the graphene to such an extent that Raman spectra could not be obtained from the graphene [33].

The potential damage, doping and residue was analysed using Raman spectroscopy performed on a graphene on SiO_2/Si test piece, fabricated by TFA annealing, Yttrium evaporation and Bi-Layer photoresist, Photoresist LOR removal protocol and HCl yttrium etch process. Figure 4.38 shows the 50 x 50 μm Raman map scans of the 2D/G ratio and D/G of the graphene sample. The map scans reveal an evenly distribution of ratios in a small scale range. This suggests representative graphene maps show no signs of major damage or doping.



(a) (b)

Figure 4.38: Raman map scan 50 x 50 μm: (a) Yttrium Sacrificial Layer Pre-Transfer Process graphene 2D/G ratio, (b) Yttrium Sacrificial Layer Pre-Transfer Process graphene D/G.

Figure 4.39 shows the Raman spectra for Yttrium Sacrificial Layer processed graphene compared to the Bi-Layer processed graphene sample. There is visibly no difference in the height of the 2D peak and no sign of the 2D or G peaks shifting. This suggests no noticeable change in the doping or strain applied to the graphene. Additionally, the extra peaks seen in Bi-Layer (LOR) spectrum are not present in the Yttrium processed sample. This suggests that the Yttrium layer prevents

photoresist residues from the Bi-Layer process adhering to the graphene surface. This means a cleaner graphene surface in the finished G-FET device.

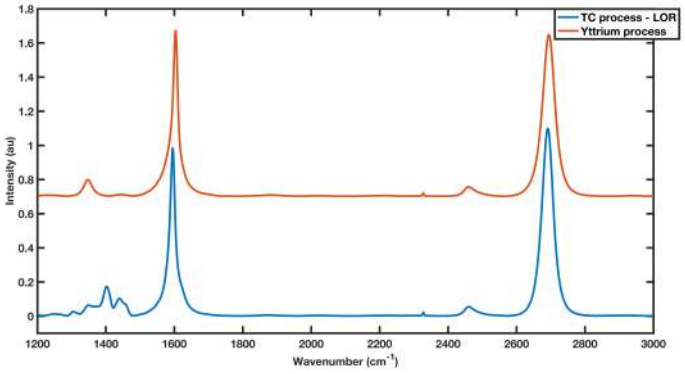


Figure 4.39: Raman spectra normalised averaged from the map scan data of Bi-Layer processed graphene and Yttrium Sacrificial Layer process plus Bi-Layer processed graphene.

Table 4.11 shows calculated averages for the 2D/G and D/G ratio and the derived grain size for each process. There is no difference in the 2D/G ratio suggesting no additional doping/strain is being applied through the use of the Yttrium process. The D/G ratio appears to be higher in the Yttrium process but also has a higher standard deviation. When comparing the Yttrium data to blank annealed graphene data the D/G (0.0999 $\pm$0.047), it is not significantly higher. This suggests the Yttrium process does not result in higher levels of damage, doping or strain in comparison to the blank annealed graphene sample. This makes it viable for integration into the Pre-Transfer process to improve the graphene surface quality.

Table 4.11: Average peak ratios and calculated grain size for Bi-Layer Process and Yttrium Process.

	I_{2D}/I_G Ratio	I_D/I_G Ratio	Approximate Grain Size (L_a)
Blank TFA Graphene	1.0802 ±0.1608	0.1047 ±0.0349	183.6 ±61.2
Pre-Transfer Process Bi-Layer Protocol	1.1058 ±0.1037	0.0655 ±0.0150	293.5 ±67.2
Yttrium Sac Process Bi-Layer Protocol	0.9568 ±0.1254	0.0991 ±0.0446	194.0 ±87.3

Conditional Annealing Process + Yttrium Sacrificial Layer

Additionally, the devices fabricated using the standard 400 °C tube furnace anneal, the low temperature anneals were also used to fabricate chips with and without the additional Yttrium sacrificial layer process steps. GRC design chips were fabricated on 20 x 50 mm graphene on SiO_2/Si test pieces to give 112 graphene channels per experimental set.

Figure 4.40 shows the resistance data of the standard Pre-Transfer process and Yttrium Sacrificial Layer process. The average (median) resistance of the Standard process was 5315 ±2371 Ω and the average resistance of the Yttrium sacrificial layer process was 4998 ±906 Ω. The average resistances calculated were significantly different, (Mann Whitney test P = 0.0001). The Standard Deviation difference was also significant, (F Test for Variance P = 0.0001). The total number of devices within 10% of the Median increased from 12.8 % to 21.1 %, which suggests the yeild of devices produced with the Yttrium process had lower variability.

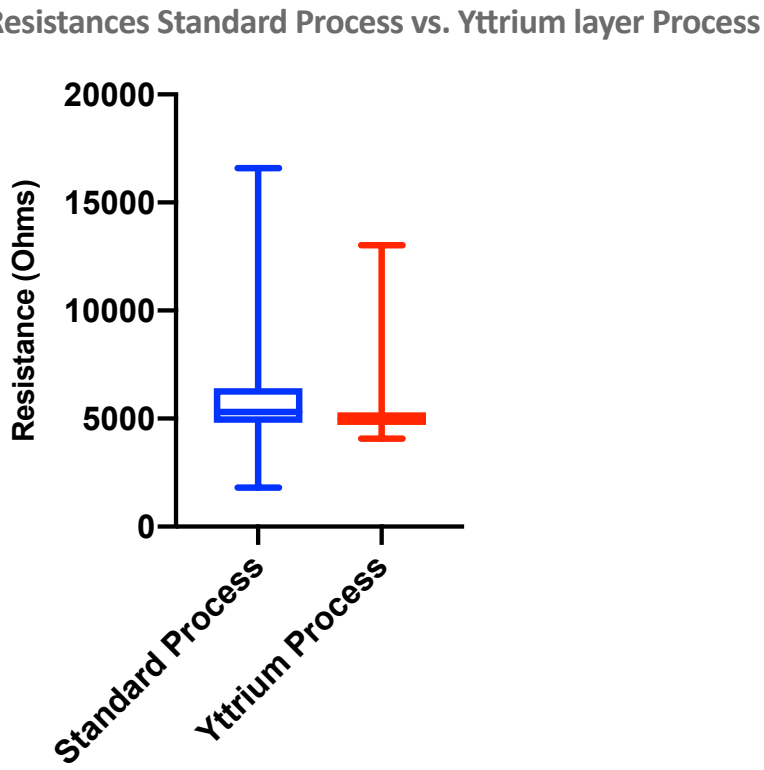
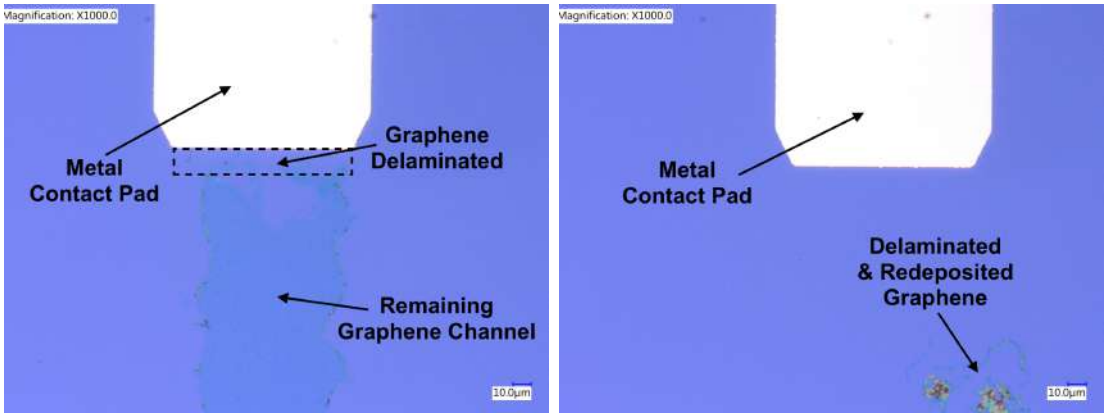


Figure 4.40: Comparison of device resistances of the standard Pre-Transfer process, and the Yttrium Sacrificial Layer process (3x batches were processed 112 graphene channels per process).

Devices fabricated using a vacuum oven anneal for 24 hours 200 °C resulted in graphene channels present on the surface for both process methods (not delaminated during processing). However, when IV measurements were performed on the low temperature Pre-Transfer processed devices. There were no linear IV responses measured (no conducting graphene channels). Out of the low temperature Yttrium process, only 3 channels were able to generate a linear IV measurement. Resistance was calculated and all were within the expected 4 - 6 kΩ range. With only 3 out of 112 channels working the resulting device yield is 2.68 % This is very low and would not be recommended for a fabrication process flow.

The devices fabricated without the pre-process anneal resulted in 0 working devices. To understand the reason for the low yields a further optical examination was performed using Keyence digital microscope. Figure 4.41 shows graphene de-

lamination of the channel for both process flows, where the graphene layer did not remain intact. This suggests that the standard pre-process annealing (400 °C) step is required for both processes.



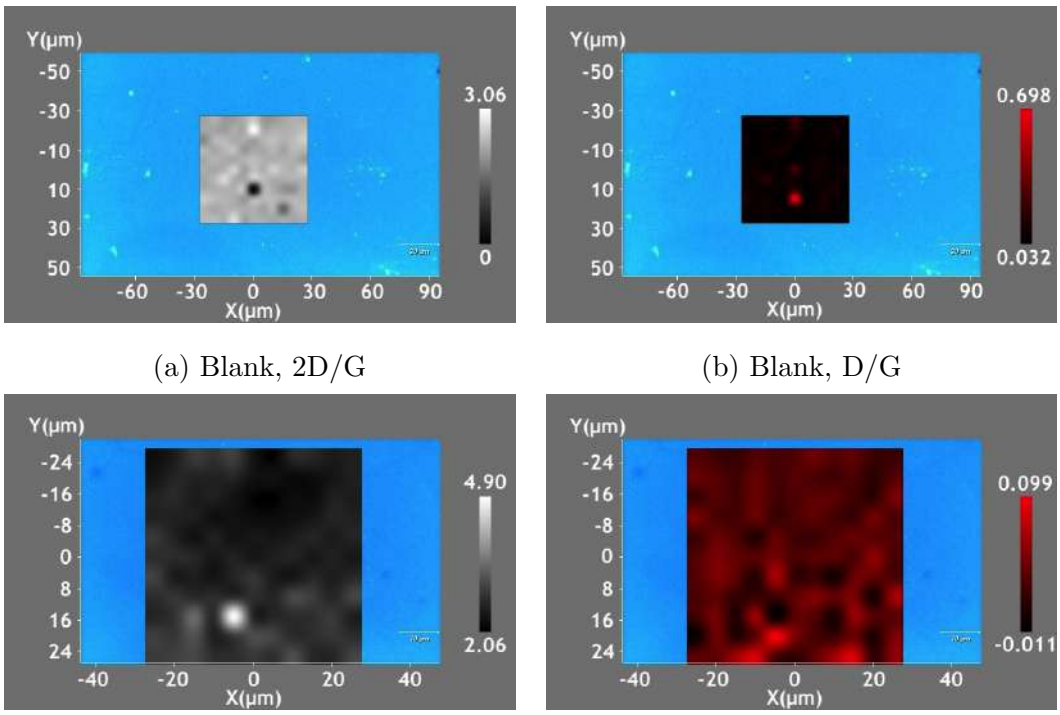
(a) (b)

Figure 4.41: Keyence 1000x zoom image of graphene channel and metal contact pad region. (a) Post Yttrium Etch, graphene channel partially remains but is disconnected from metal contact pads. (b) Post Metal Lift-Off step 7, No graphene channel remains.

Post-Transfer Process: Comparison Of Photoresists Removal On Graphene Cleanliness

The Post-Transfer process requires the use of 1 photolithography step to create an etch mask using a single layer positive PR AZ 5214 E protocol. Figure 4.42 shows the Raman map scans (50 x 50 μm) with the 2D/G ratio and D/G ratio displayed for each samples. The Post-Transfer blank graphene shows similar ratio scales to the AZ 5214 E sample. Each map scan shows evenly distributed areas of damage and doping with minimum hot spots. This suggests the graphene samples are fairly representative without any significant flaws or double layer patches. As these samples have not been annealed the 2D peak ratio is above 2, consistent with pristine graphene [34].

Figure 4.43 shows the normalised spectra of Raman map scans for the blank Post-



(a) Blank, 2D/G

(b) Blank, D/G

(c) Single layer PR, 2D/G

(d) Single layer PR, D/G

Figure 4.42: Raman map scan 50 x 50 μm: (a) Blank Post-Transfer graphene 2D/G ratio, (b) Blank Post-Transfer graphene D/G, (c) AZ 5214 E processed graphene 2D/G ratio, (d) AZ 5214 E processed graphene graphene D/G ratio.

Transfer graphene and 5214 E processed graphene. Similar to the map scans there are no distinct differences in height between 2D or G peaks between the samples. There are also no notable peak shifts that would indicate signs of doping or strain applied to the sample by the photoresist or cleaning. This suggests the photoresist has no effect on the graphene for strain/doping.

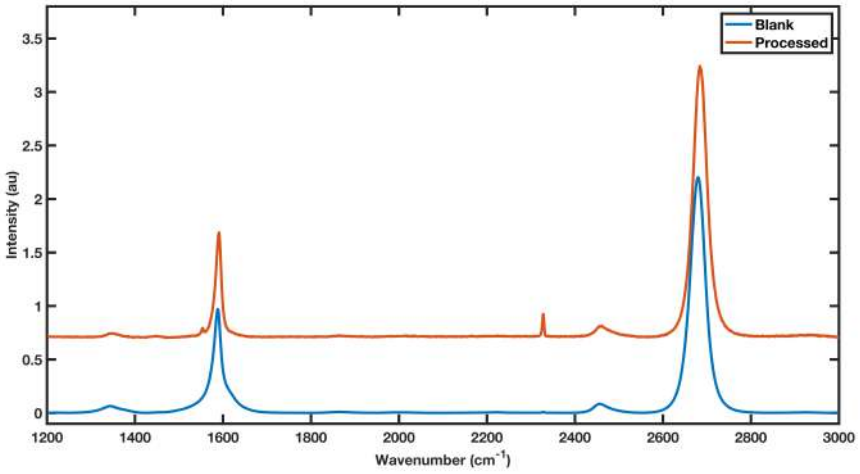


Figure 4.43: Raman spectras normalised and averaged from the map scan data of blank Post-Transfer graphene and AZ 5214 E processed Post-Transfer graphene.

Table 4.12 shows the averaged ratios 2D/G, D/G and derived grain size L_a for the blank Post-Transfer graphene and AZ 5214 E processed graphene. The quantified results show no significant increase in damage or doping from the photoresist processes compared to blank graphene. The Post-Transfer AZ 51214 E processed graphene has much less doping, strain and residue compared to the previously tested Pre-Transfer process, whilst the structural damage appears in a similar range for both process flows.

Table 4.12: Average peak ratios and calculated grain size for Post-Transfer Blank graphene and AZ 5214 E photoresist process.

	I_{2D}/I_G Ratio	I_D/I_G Ratio	Approximate Grain Size (L_a)
Post-Transfer Blank Graphene	2.2416 ±0.1939	0.0655 ±0.0407	293.5 ±182.4
Post-Transfer AZ 5214 E Processed	2.5455 ±0.2658	0.0464 ±0.0139	414.3 ±124.1
Pre-Transfer TFA Graphene	1.0802 ±0.1608	0.1047 ±0.0349	183.6 ±61.2
Pre-Transfer Bi-Layer Processed	1.1058 ±0.1037	0.0655 ±0.0150	293.5 ±67.2

Post-Transfer Process: Comparison Of Capping/Contact Metal

The Post-Transfer method used a single metal process step as oppose to graphene metal sandwich or stacked structure, using the capping metal as the graphene contact metal. Based on a search of the literature noble metals such as gold, palladium and platinum have been analysed with respect to their contact resistance for graphene electrical devices. Gold produced lowest contact resistance. Using the noble metals to compare contact resistance was not possible with the Pre-Transfer process method due to delamination of the contact metals. However, the effect on yield and wafer resistance / wafer wide standard deviation could be compared with the Post-Transfer process.

Eight standard Dip Chips were fabricated, each using 20 nm of chromium adhesion metal and 80 nm of capping metal, this results in 24 graphene channels to perform IV measurements on. Figure 4.44 shows the calculated resistances from the three capping metal chosen gold, palladium and platinum in a Box and Whisker plot. Two sets of the palladium capping metal were tested to compare sample variation.

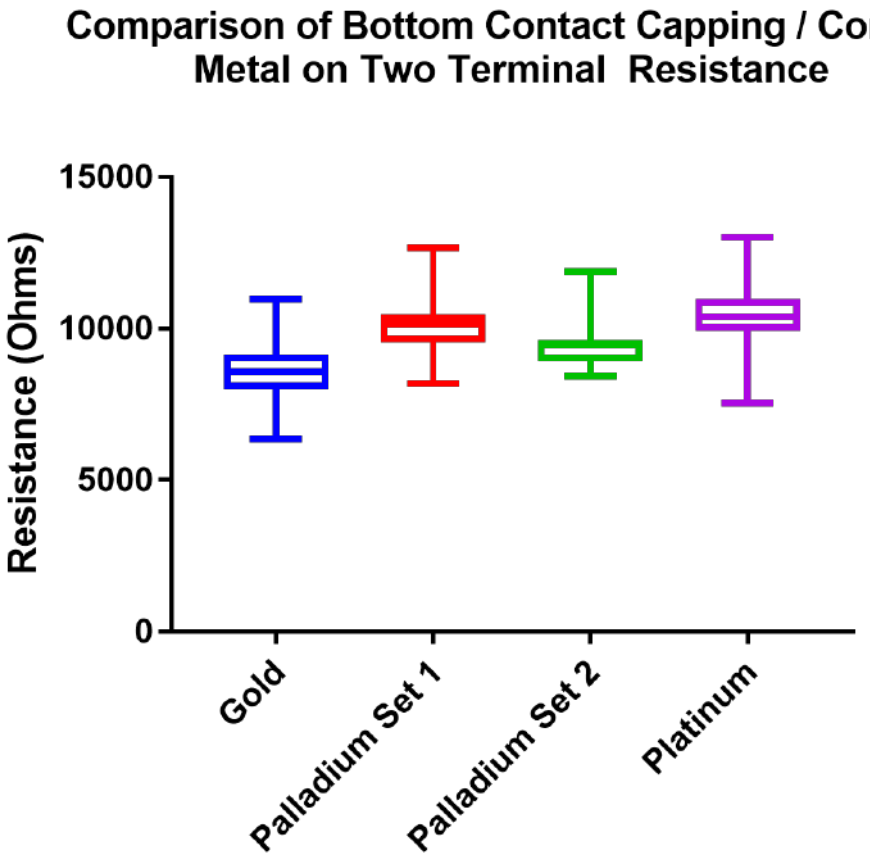


Figure 4.44: Comparison of Capping / Contact metal on two terminal resistance measurement of graphene channels using Dip Chip Design.

Table 4.13 shows the average resistances, standard deviation and relative standard deviation (RSD) for each capping metal. There is a significant difference between the resistance measurements of the Gold capping metal and Palladium set 1, set 2 and Platinum (P value of 0.004, unpaired t-test with Welch's correction). This suggests gold makes the lowest resistance devices for the Post-Transfer process flow. There was no significant difference between the palladium sets and the platinum. There was also a significant difference between the Palladium set 1 and set 2, which suggests that batch to batch processing can have a larger effect than the metal used for the capping / graphene contact. These results suggest that any of the noble metals can be used for Post-Transfer process flow to produce the graphene

Dip Chip devices, as the metal contact resistance is similar (Au and Pd would be recommended).

Table 4.13: Calculated resistance averages and relative standard deviation for capping metals deposited as part of the Post-Transfer Process

	Gold	Palladium Set 1	Palladium Set 2	Platinum
Mean Resistance (Ω)	8614	10101	9442	10427
Standard Deviation	997	836	736	909
RSD (%)	11.58	8.27	7.80	8.72

Post-Transfer Process: Comparison Of Dielectric Substrate

Alternative substrates were investigated in order to investigate their effect on graphene channel resistance. Silicon Nitride (Si_3N_4), as a graphene FET substrate, has been shown to produce similar electrical properties as SiO_2 and produce distinctive Dirac peaks whilst performing Dirac point measurements [35].

A set of 8 standard Dip Chips were fabricated totalling 24 graphene channels on a Si_3N_4 substrate wafer. IV measurements were used to calculate he average resistance measured on Si_3N_4 substrate, which was 19664 ±3060 Ω. This is approximately 104 % more than the average resistance measurement on SiO_2 of 9626 ±786 Ω. Figure 4.45 shows a large range of data as seen in the relative standard deviation of the Si_3N_4 set (15.6 % compared to 8.8 % for the SiO_2 set). This suggests that Dip Chip devices can be fabricated on Si_3N_4 substrates. However, the electrical performance does not equate to SiO_2, as the average resistance per channel has doubled. This could potentially reduce sensitivity to resistance change, which would be detrimental for a "chemiresistive' sensor.

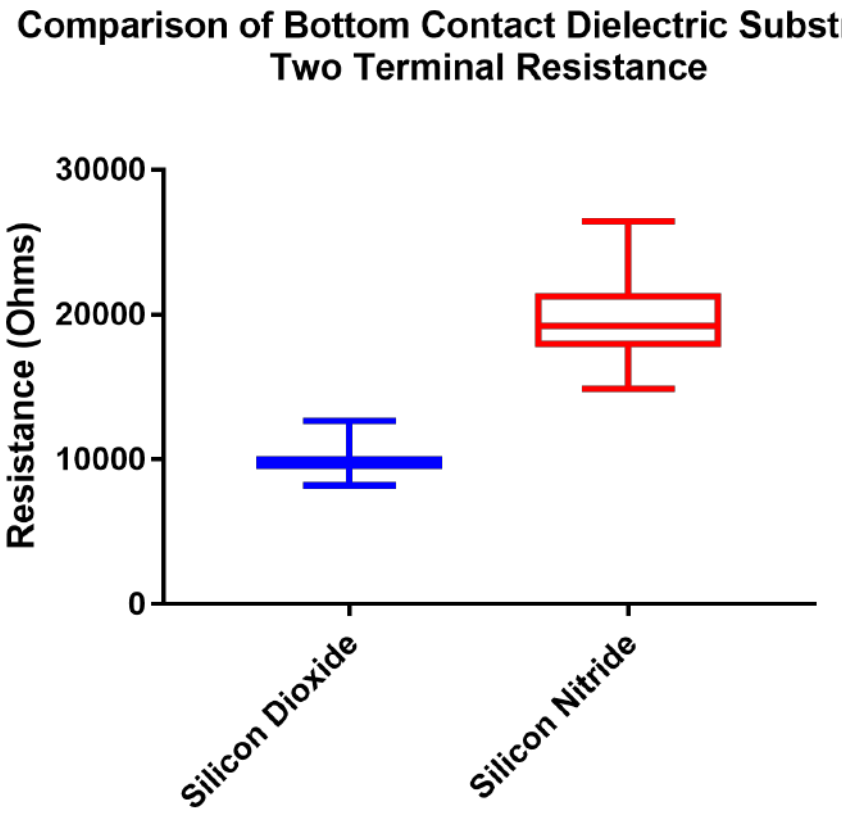


Figure 4.45: Two terminal resistance measurements using Dip Chip Origin design using different dielectric substrates for Post-Transfer fabrication process.

The reason for the higher two terminal electrical resistance on Si_3N_4 is due to the higher sheet resistance reported for monolayer graphene on Si_3N_4. This caused by graphene's lower carrier mobility on Si_3N_4 substrates, the reduced carrier mobility is due has been linked to impurity densities in the deposited film and subsequent charge scattering [36].

Improving Graphene Transfer Yield, Buried Electrode Process

As previously stated, graphene transfer is provided primarily by a contracted company HexagonFab. The company has a guarantee on number of working graphene devices (conducting graphene channels) of 50 %. The yield of working devices for 2 wafers each containing 96 potential graphene channels was 73 %. In order to in-

crease device yield increasing surface flatness has been recommended as a method to improve graphene performance [37], [38].

With the standard SiO_2 thickness being 300 nm, there is vertical space in this layer for the metal contacts to be etched away and the metal to be deposited within the etched trench regions producing a flatter overall substrate for graphene transfer. Figure 4.46 shows an infographic with approximate material dimensions. The thickness of the metal contact pads have been reduced for proof of concept to match the achieved SiO_2 etch depth. Contact pads in graphene research for IV probing can be much thinner that of standard devices that would require interconnects in larger circuits [39].

(a) (b)

Figure 4.46: (a) Represents the standard Post-Transfer fabrication process. The graphene approx 0.36 nm in thickness does not lie flat on the substrate at the metal contact interface, creating regions of stress at the corners of the metal contacts and reduced surface adhesion. (b) Buried electrode Post-Transfer concept, with the metal sunk into the SiO_2 dielectric layer resulting in a flatter surface with less impact on the graphene surface.

An etch series was performed to optimise the SiO_2 etch process using the Oxford Instruments RIE tool. The etch series was time based and was done on 20 mm x 20 mm chips which had been photo-patterned with a photoresist etch-mask. The total exposed area of SiO_2 was less than the total exposed for a full wafer etch, this will create some discrepancy in etch depth when compared to full wafer etch, due to the total exposed surface area of SiO_2 to the etch gases.

However, this etch characterisation is useful to check if the etch rate is linear for the depth targeted. After the etch process the photoresist etch mask was then removed using a Solvent Clean revealing the surrounding non etched SiO_2 surface. The step height of the etch was measured using AFM and averaged over 5 regions per map and 3 maps per quarter. Figure 4.47 shows the etch depth with respect to time plotted, the average etch rate was calculated as 0.86 nm/s.

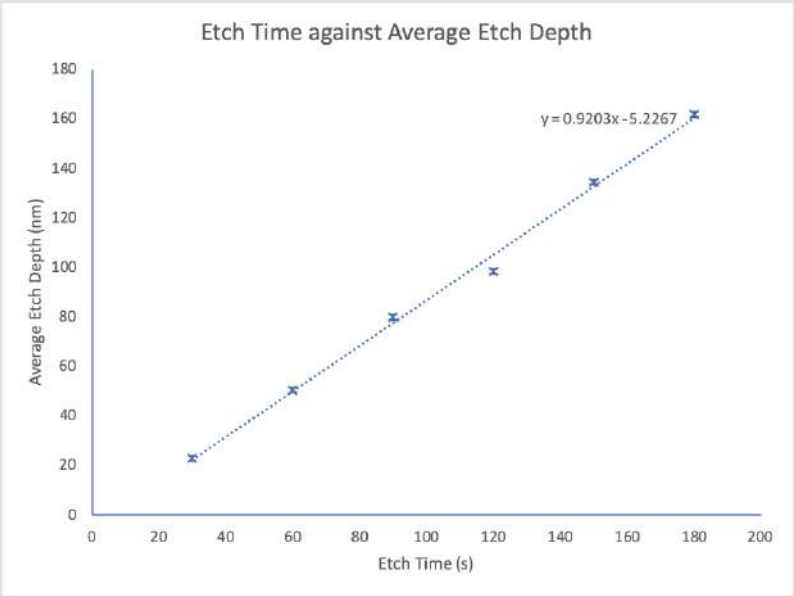


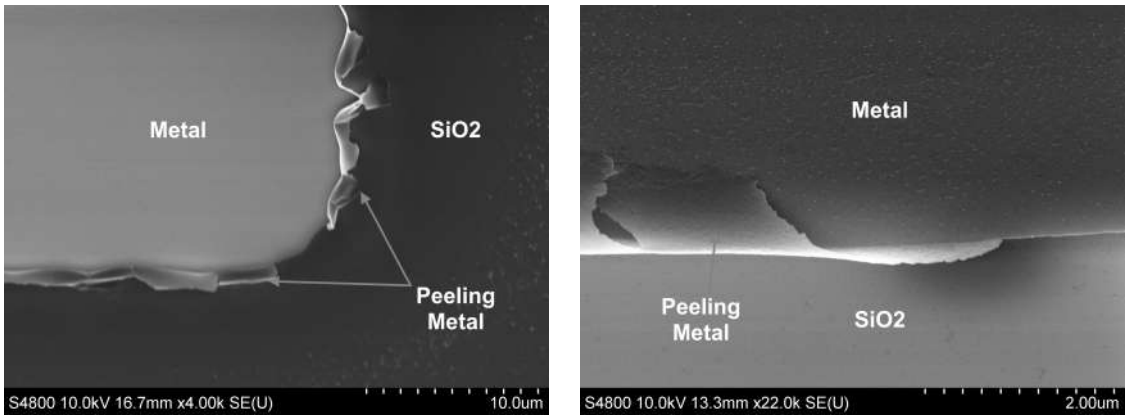
Figure 4.47: SiO_2 etch series based on increase etch time against the depth of etch, using 20 mm x 20 mm SiO_2/Si chips partially photo-patterned with etch mask

Using the line equation from Figure 4.47 a new etch series on two full wafers, photo-patterned using the metal electrode mask for Dip Chip for targetted etch depths of 50 nm and 100 nm (corresponding predicted etch times 60 s and 114 s was performed). The resulting etch depths for full wafer exposed SiO_2 were 26 nm and 50 nm. These etch depths fell short of the expected results only achieving 50 - 52 % of the expected depth. Based on these results the etch rate for full wafer Dip Chip Origin pattern was 0.44 nm/s. Based on this etch rate a wafer was etched for 137 s for a target etch depth of 60 nm. An average of 57.6 nm was measured across the wafer.

This process was repeated on a second wafer but the photoresist etch mask was

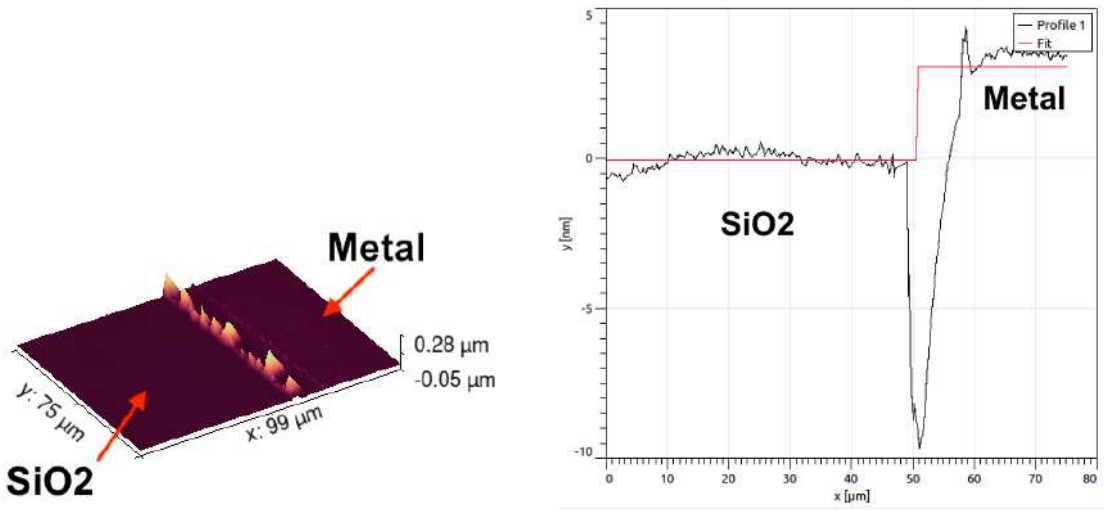
retained. The photoresist used was nLOF 2070 (Microchemicals GmbH, Germany), a negative photoresist for metal lift-off. PVD deposition details can be found in Materials and Methods Chapter section 3.7.1, metal deposition step was then tailored to fill the etched SiO_2 trench. 20 nm of Cr adhesion metal and 40 nm Pd capping metal was deposited on the wafer. Metal lift-off was performed using 10 minutes in Technistrip D350 at 80 °C, followed by a solvent clean.

The resulting metal electrode appearance looked irregular / rough. SEM was used to investigate the metal edges of the buried contacts as well as AFM to determine the resulting step height of the metal contact pad relative to the SiO_2 substrate. The SEM identified metal that did not lift-off effectively during the lift-off process (Figure 4.48). Figure 4.49 shows the AFM cross section profile with an average step height of 3 nm calculated for the metal electrodes.



(a) (b)

Figure 4.48: (a) SEM 4000x magnification corner region of rectangular metal electrode using buried back contact process, curled edges of metal roughly visible. (b) SEM 22000x magnification of horizontal region of metal electrode (a) clearly showing deposited metal folded over at edges.

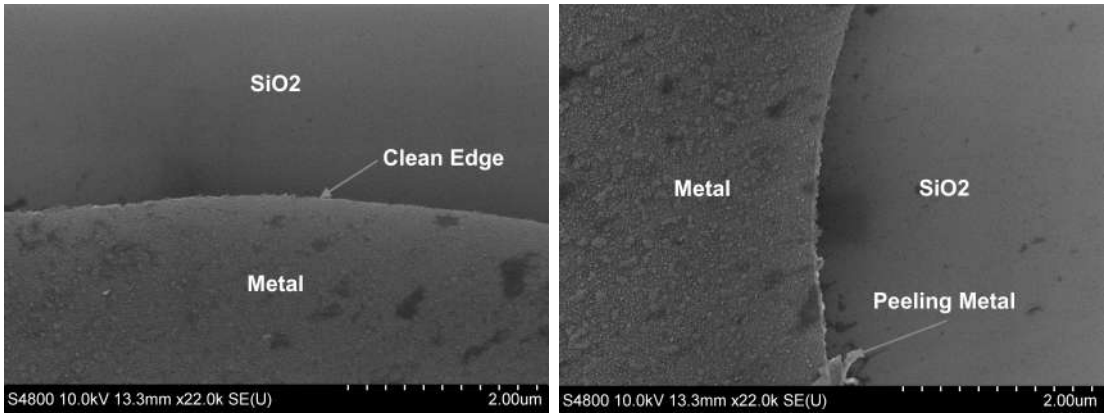


(a) (b)

Figure 4.49: (a) AFM 3D representation of 100 μm x 75 μm scanned area showing step height from Silicon Dioxide surface to buried metal electrode structure (b) Height linear profile averaged from 10 μm wide area path, height of Silicon Dioxide set as 0 nm.

The resulting chips were manually planarized using a lint free cloth and IPA to remove some of the curled metal edges that had resulted in the rough edges. SEM was used to check the planarized surface. Figure 4.50 shows SEM images of planarized buried electrode metal edges. Most of the curled metal was removed resulting in smooth clean edges. However, some sections of curled metal still remained. To remove all metal a wafer polishing/planarization tool would be required.

Graphene transfers and the remaining steps of Post-Transfer fabrication process was completed on two wafers with metal electrodes fabricated using the buried back contact process. The resulting device yields were calculated as 79 % 83 %. Further wafer transfers will be required for statistical analyses. However, based on early results, device yield from graphene transfer can be improved using the buried back contact method.



(a) (b)

Figure 4.50: (a) SEM 22000x magnification of metal electrode after planarization process, excess metal still visible but predominantly clear. (b) SEM 22000x magnification of metal electrode all excess metal removed

4.5 Graphene Sensor Electrical Testing

The sensor designs are based around the use of a custom made SD card connector PCB, which in the future would form part of the point of care diagnostic setup. The PCB connector allows for easy electrical connection and device testing, and also allows for testing to be performed in solution eliminating the use of electrical probes. The PCB connector was tested and compared to electrical probing using the IV probe station to compare measurement variance over time and total circuit resistance. Additionally, optimisation of the measurement process including grounding vs gating of device bulk silicon was performed to reduce noise in the current measurement. Base-line measurements of the device were also performed, comparing measured voltage vs measured current and the speed of data acquisition on the accuracy of the measurement.

The Multiplex design was tested using liquids drop-cast (pipetted) onto individual graphene channels to test the procedure for multiplex functionalisation. Measurements were performed on each on the graphene channels before and after drop-casting with one graphene channel left blank as the control. The channels were then test functionalised using a drop-cast aptamer solutions, so that each graphene channel would be functionalised with a different aptamer bio-receptor as a proof of concept test for the Multiplex Design.

The Inverted MOSFET design was tested by performing gated FET measurements on the graphene channels. The fabrication process was optimised comparing SiO_2 and Al_2O_3 gate oxides for the MOSFET design. The resistance shift of the graphene channel due to electric field generated at the gate electrode was measured and compared for the Inverted MOSFET design and standard bulk silicon gate design.

The Matrix design fabrication process flow was optimised comparing polymer and dielectric interlayers, between the two layers of metal tracks/electrodes. The channels were then measured individually for a proof of concept test to show that all 9 channels can be operated individually.

4.5.1 Materials & Methods

IV Data Acquisition

Linear IV measurements -1 V to 1 V were performed and the resulting measured current and input bias was saved as a csv file output. Details of IV measurements can be seen in the Material & Methods Chapter section 3.11.2.

Source-Drain Curves from 0 V - 1 V were performed with constant gate bias, the gate bias is stepped after each sweep from 0 - 5 V. Measured drain current, input drain bias, measured gate current and input gate bias were saved as a csv file output.

Gated FET (Dirac Point) measurements were performed using parameters found in Material & Methods section 3.11.2.

IV Data Processing

CSV files for real-time measurements were processed in Excel (Microsoft, USA). The voltage was plotted against current. The resistance was calculated from inverse of the slope calculated from the linear region of the I-V graph.

Timing Data Processing

The speed of device handling and measurement taking by human operators were compared. All comparisons of timings for probe station to PCB connector operation were analysed using an unpaired t-test with Welch's correction for non equal variance.

Inter IV Probe Station Comparison

A comparison set of measurements were performed on the EverBeing IV probe station and Inseto IV probe station. The resulting resistances and measurement variance were shown to be significantly different. For all experimental measurements

a single probe station was used throughout (EverBeing). The experimental set up and results can be seen in Appendix section 8.2.3.

Measurement Speed Experimental Setup

To investigate the effect of changing step time on data reproducibility, a set of thirty IV measurements were performed with step time 0.2 s and 0.05 ms, measurements were taken alternately on a single graphene channel.

This set was then modified to a single IV measurement taken at each step time for 20 different graphene channels. The step time used first was alternated for each graphene channel measured.

PCB Connector vs IV Probe Station Experimental Setup

To evaluate the measurement accuracy of the SD Card PCB connector, measurements were performed on 12 graphene channels across 4 Dip Chip Design chips. The 12 graphene channels were then measured again using the EverBeing IV probe station. All channels were measured 10 times in each set up to calculate the variance between repeat measurements.

The time taken for a two terminal resistance measurement of a graphene channel on the graphene dip chip was compared when using the SD card connector to the EverBeing IV probe station. Five users with previous training and experience using the IV probe station were selected from the then current cleanroom user list (01/10/2017 - 01/10/2018). The trained individuals were given the same scripted safe operating procedure of the semi probe IV test station and the SD card connector. The graphene dip chip used for the experiment, the Semi-Probe IV probe station's micro manipulators and the SD card connectors starting positions and orientations were maintained for each user. Each user was asked to repeat the process three times per set up.

Connecting Bulk Silicon Into IV Measurement Circuit Experimental Setup

To evaluate the integration of the bulk silicon into the IV measurement circuit, 12 graphene channels were measured in each circuit setup (silicon grounded, silicon gated 0 V and silicon not grounded) in both the SD Card connector and the EverBeing IV probe station. Each channel was also measured 10 times in order to measure variance between each technique.

Multiplex Design Testing Experimental Setup

Matrix Design Dip Chips were fabricated using the Post-Transfer process within 1 week prior to testing. Graphene channel isolated resistance change testing was performed by pipetting a 5 μl volume of di H_2O onto channel one, channel two was left blank as a control and 5 μl of ethanol was applied to channel 3. IV measurements were performed on each of the channels three times prior to application of the solutions and measured a further three times 10 minutes after the application of the solutions. This was repeated on five chips for proof of concept.

Functionalisation testing was performed using aptamer (Thrombin and Brain Neurotic Peptide) application solution (Further details can be found in section 6.2.9). The application solution for Thrombin aptamer 10 μl was applied to channel 1, channel 2 was left blank and Brain Neurotic Peptide aptamer was applied to channel 3. The solution was incubated on the graphene surface for 12 hours followed by PBS wash steps and drying. IV measurements were performed on each of the channels three times prior to application of the solutions and measured a further three times 10 minutes after the application of the solutions. This was repeated on five chips for proof of concept.

Inverted MOSFET Design Fabrication Optimisation

Fabrication optimisation for the gate dielectric deposition and dielectric etching were tested during the development of the Inverted MOSFET Design Dip Chip. The first metal pattern layer follows the same process steps as the standard Post-Transfer

Fabrication process.

The first dielectric layer tested was SiO_2, deposition of SiO_2 was performed using PECVD (SPTS Technologies) to deposit a 300 nm thick layer onto the metal patterned wafer. Recipe for SiO_2 deposition can be found in Materials & Methods Chapter section 3.8.2. The seconds dielectric layer tested was Al_2O_3, deposition of Al_2O_3 was performed using MVD (SPTS Technologies) to deposit a 50 nm thick layer onto the metal patterned wafer. The recipe for Al_2O_3 deposition can be found in Materials & Methods Chapter section Al_2O_3.

Dielectric via etch of SiO_2 was performed by wet BOE etching recipe (Section 8.1.5). SiO_2 etch was also performed using RIE (Oxford Instruments) SiO_2 etch recipe (Section 6.3.3). Al_2O_3 was etched using AZ 726 Al_2O_3 etch protocol (Section 3.6.5).

The roughness value for MVD deposited Aluminium Oxide = 0.2 nm RMS

Via filling was performed using PVD metal sputtering (PVD protocol found Section 3.7.1). For SiO_2 via filling, a total metal deposition of 310 nm was chosen comprising of 200 nm Cr and 105 nm Pd. For the Al_2O_3 via filling, metal deposition of 55 nm comprised of 10 nm Cr and 45 nm Pd.

Matrix Design Fabrication Optimisation

Fabrication optimisation for specific process steps were tested during the development of the Matrix Design Dip Chip. The first metal pattern layer follows the same process steps as the standard Post-Transfer Fabrication process.

A permanent polymer photoresist (EpoClad) and a MVD deposited Al_2O_3 layer were investigated as the Matrix design interlayer. The layer between the 1^{st} and 2^{nd} metal tracks/electrode. Spin coating of the EpoClad layer was performed using spin coating and photolithography (protocol found in section 3.5.4). The second photolithography and metal patterning steps were performed using the standard Post-Transfer Metal process steps.

The Al_2O_3 50 nm dielectric layer was deposited by MVD. The Al_2O_3 layer was etched using AZ 726 Al_2O_3 etch protocol. The second photolithography and metal

patterning steps were performed using a modified version of the Bi-Layer photoresist protocol, using AZ 400 K (MicroChemcals GmbH, Germany) developer as a replacement for the AZ 726 developer step.

Matrix Design Electrical Testing

To perform IV measurements on all 9 graphene each channel represents a specific combination of source drain electrodes. The six contact electrodes are divided into source and drain electrodes, the first three electrodes (source electrodes) labelled A, B and C and the second three electrodes (drain electrodes) labelled 1, 2 and 3. Graphene channel 1 can be measured by probing A and 1, graphene channel 2 can be measured by probing A and 2 all the way through to graphene channel 9 measured by probing C and 3 (Figure 4.51).

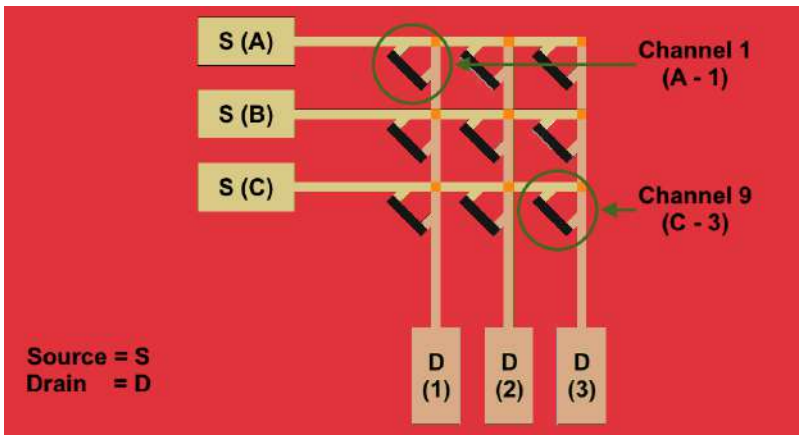


Figure 4.51: IV measurement process for Matrix design Dip Chip testing.

4.5.2 Results & Discussion

Effect of measurement speed on data reproducibility

When performing IV measurements on graphene devices using the preset (Kiethley TSP Express) measurement step time of 0.2 s, the total machine time can be calculated by multiplying this by the 101 steps that make up a linear sweep measurement. This results in a total measurement time of 20 s. When measuring a full

wafer of 32 Dip Chip graphene sensors, each chip contains 3 graphene channels and measuring each channel in triplicate equals 288 measurements. The total machine measurement time (excluding measurement setup]) will be approximately 5812 s (97 minutes). By reducing the step time to 0.05 s the time spent per measurement reduces to 5 seconds reducing total machine time to 1454 s (24 minutes).

Table 4.14 shows the average calculated resistance data for the single graphene channel measurement at each step time. Comparing the average (mean) resistance, the percentage difference between the numbers was calculated to be $< 1\ \Omega$ which is 0.002 %. The difference between the two data sets was not significant. From this result the change in resistance due to other unknown factors is far greater than the difference due to step time.

Table 4.14: Comparison of resistance measurements made on 400 x 100 μm graphene channel using the 0.2 s and 0.05 s step time setting on Keithley 2636 B measurement unit.

	Step Time 0.2 s	Step Time 0.05 s
Mean (Ohms)	4834.63	4834.13
Median (Ohms)	4833.33	4833.45
Range (Ohms)	13.61	13.56
Standard Deviation	3.80	3.10
Relative SD	0.08 %	0.06 %

To investigate step time further, 20 graphene channels were individually measured using both the 0.2 s and 0.05 s step time. Table 4.15 shows the analyses of these resistance measurements. Comparing the average (mean) resistance a difference of 4.67 Ohm (0.09 %), the difference between the two data sets was not significant.

Table 4.15: Comparison of resistance measurements made on 20 graphene channels, dimensions 400 x 100 /*mu*m using the 0.2 s and 0.05 s step time setting on Keithley 2636 B measurement unit.

	Step Time 0.2 s	Step Time 0.05 s
Mean (Ohms)	5466.26	5461.59
Median (Ohms)	5344.48	5353.92
Range (Ohms)	2006.15	1967.16
Standard Deviation	591.78	581.79
Relative SD	10.83 %	10.65 %

This data suggests that the step time does not effect the measurement accuracy within the range tested. IV measurements will be perfromed using the 0.05 ms step time for this body of work. This reduces machine process time by $\frac{1}{4}$, the timing bottle neck becomes the operator interacting with the software and GUI.

Comparison Of IV Probe Station & PCB Connector

To evaluate the SD Card PCB Connector in comparison to the IV probe station resistance measurements were performed on 12 graphene channels, the resistances of the channels were then compared. Figure 4.52 shows a box and whisker plot of the calculated resistances, the average resistance was calculated for the IV probe station (9462 $\pm$1034 Ω) and the PCB Connector (9585 $\pm$1020 Ω), an increase in resistance of 1.3 %. The means were compared and the increase was shown to be significant (P = 0.0019, paired t-test). This increase could be due to the increase in the number of contact points or the length/type of cables used. The increase in resistance seen when using the PCB is uniform for the measurements so should not effect measurement accuracy.

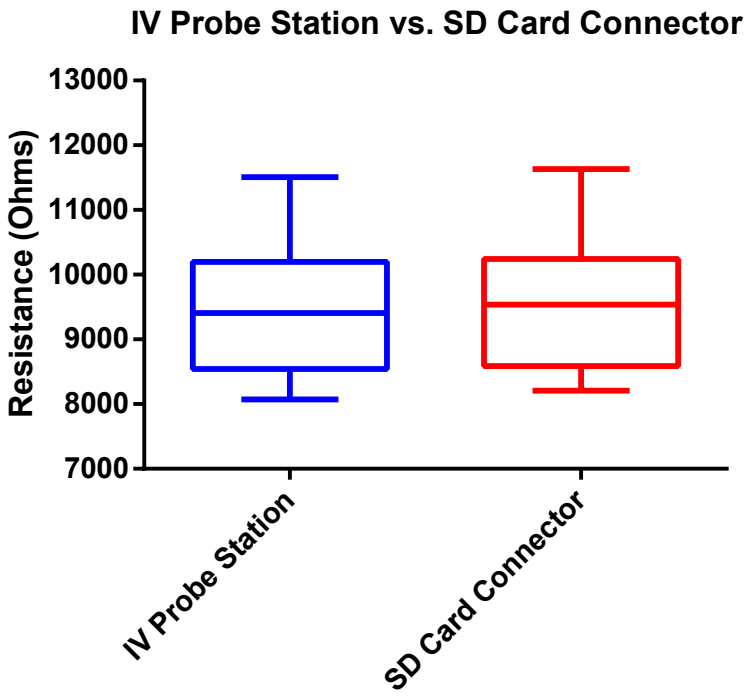


Figure 4.52: Box and Whisker plot showing calculated resistance measured on 12 graphene channels comparing the IV Probe Station and PCB Connector.

Secondly, the variance in the measurement itself was compared. The standard deviation for each set of 10 repeats was calculated for each set up. The average standard deviation of measurements on the IV probe station PCB connector were 29.1 Ω and 11.0 Ω respectively. When analysing the resistance data the variance was shown to be significantly different $P = 0.0112$, F - test for variance. The decrease in variation when using the PCB connector could be explained by the uniform nature of the pin position and pressure when using the PCB connector, which can connect to all 6 electrodes simultaneously, as opposed to individually bringing down 2 probes onto pairs of electrodes for each measurement.

The increase in resistance seen when using the PCB is uniform and the overall variance of the measurement is decreased, this makes it a suitable system for sensor based measurements especially when paired with its design advantages over the IV

probe station. Which has more variation, due to probing variance.

PCB Connector to IV Probe Station: Speed of Analyses

The SD connector PCB was designed for the Dip Chip graphene sensor to aid in functionalisation and sensing experiments. Part of the design functionality was to increase the speed of measurement setup. And to reduce time taken for multiple IV measurements made through fabrication and functionalisation. The speed of measurement setup can be crucial for accurate timings during time based experiments.

Table 4.16 and Table 4.17 shows the average timings for the IV probe station and SD card PCB connector operation. The average time taken for the two terminal measurement using the IV probe station and PCB connector was 25.2 ±3 s and 23.8 ±1.9 s respectively. This suggests that the PCB connector does not increase speed of data acquisition for a two terminal measurement.

Table 4.16: Time taken for a trained user to perform a two terminal resistance measurement using the Semi-Probe IV probe station.

	IV Probe Station Two Terminal Measurement			
Trained User	Repeat 1 (s)	Repeat 2 (s)	Repeat 3 (s)	Average (s)
1	25.11	24.75	24.5	24.79
2	29.81	23.11	22.4	25.11
3	30.18	30.62	27.43	29.41
4	22.61	20.89	18.71	20.74
5	28.97	27.14	21.73	25.95

Table 4.17: Time taken for a trained user to perform a two terminal resistance measurement using the SD card connector set up.

	SD Card Connector Two Terminal Measurement			
Trained User	Repeat 1 (s)	Repeat 2 (s)	Repeat 3 (s)	Average (s)
1	20.67	21.77	22.08	21.51
2	20.69	31.82	21.33	24.61
3	26.84	24.45	26.47	25.92
4	25.42	26.22	23.82	25.13
5	24.3	22.47	22.07	22.95

However, the PCB connector has eight internal metal pins for electrode connections at the same time compared to the IV probe station with just 2. Therefore the PCB card connector is more efficient for multiple measurements. Using a modified Keithley script and additional Keithley Source Measuring Unit, the two terminal resistance measurement can be taken simultaneously across all three graphene channels. If the Dip Chip design made use of all eight connector pins then 4 graphene channels could be measured simultaneously.

Using the timings above for the PCB connector but accounting for simultaneous three channels measurement. To compare the IV probe station for simultaneous measurements, two additional probe station arms were added to the system and the same individuals were asked to perform a two terminal resistance measurement on two graphene channels simultaneously (using a modified Keithley script for 2 simultaneous measurements). The average time taken for two simultaneous measurements were 43 $\pm$6.7 s as oppose to the 23.8 $\pm$3 s for PCB connector, the difference between average time taken doing two channels simultaneously was significantly different, ($P = < 0.0001$, Unpaired t test with Welch's correction). The time taken would be decreased further if the Dip Chip was redesigned to include 4 graphene channels and eight electrodes.

Effect Of Connecting To The Bulk silicon In The IV Measurement Circuit

The bulk silicon layer for the wafers used was P-type 1-10 Ωcm. The graphene is separated from the conductive bulk silicon by a 300 nm layer of SiO_2. This effectively forms a MOS capacitor. Any charge change in the bulk silicon could effect the graphene IV measurement. To compare the effect of integrating the bulk silicon into the graphene measurement circuit, three setups were compared. (1) Leaving the silicon not grounded in the measurement circuit, (2) grounding the silicon to the measurement circuit and (3) applying a gate voltage of 0 V to the silicon.

Figure 4.53 shows box plot for the calculated resistances for the 12 channels across 4 Dip Chips in each set up. The averaged resistance values for the graphene channels varied over each setup, but was not significant.

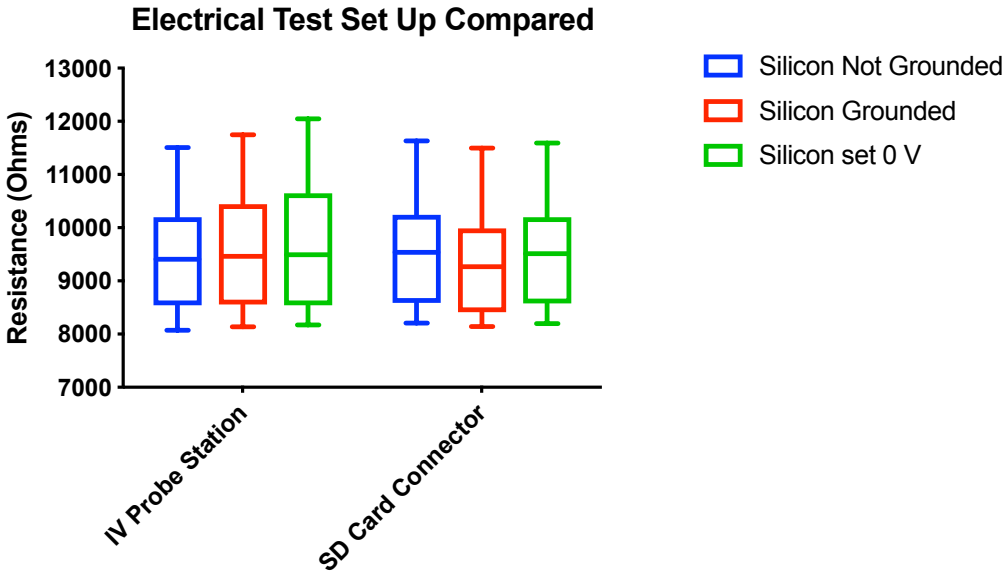


Figure 4.53: Box and whisker plot showing resistance measured on 12 graphene channels comparing the different silicon grounding options in both IV Probe Station and SD Card Connector.

When comparing how much variance is produced through repeated measurements of the same graphene channel for each bulk silicon set up on both the IV

probe station and the PCB connector, Table 4.18 shows the average standard deviation for each set up. The only statistical difference in terms of variance can be seen between the Grounded and not grounded set up whilst using the IV probe station, (P = 0.0175 F test for variance).

Table 4.18: Comparison of average standard deviation for the 10 repeats of resistance measurement for each silicon connection set up.

Bulk Silicon Connection	IV Probe Station Standard Deviation (Ω)	SD Card Connector Standard Deviation (Ω)
Not Grounded	29.12	11.01
Grounded	10.05	6.79
Set to 0 V	21.51	10.17

The data confirms the previous work that the PCB connector produces measurements with lower standard deviation compared to the IV probe station. The effect of grounding the silicon does not seem to produce any significant changes. For best practice all measurements will be performed with the silicon grounded in the IV measurement circuit.

Multiplex Design: Multi Region Measurements

The Multiplex Design was created to allow for multiplex/multiple bio-receptors to be functionalised onto a single chip. This would allow for multiple diagnostic markers to be detected using the same sensor platform.

The Multiplex Design did not require any fabrication optimisation as the Post-Transfer process flow was used without any modifications. To test the functionality of the Multiplex Design Dip Chip, H_2O and ethanol were drop cast onto individual graphene channels and IV measurements performed. These solutions were chosen as they have been shown to produce a resistance change on graphene resistors [40]. Figure 4.54 shows the fabricated Dip Chip with 10 μl solutions isolated on each graphene channel.

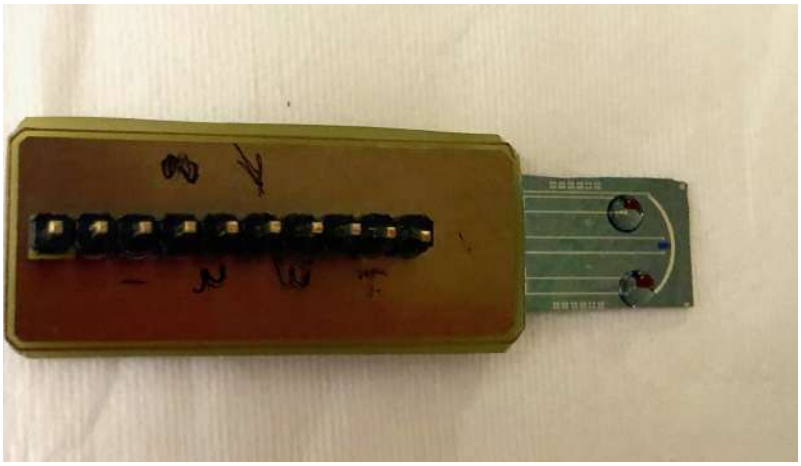


Figure 4.54: Multiplex design chip inserted into SD card based PCB connector. Channel 1 immersed in 10 μl droplet of di H_2O, channel 2 left blank and channel 3 immersed in 10 μl droplet of ethanol.

Table 4.19 shows the average resistances before and after application of drop-cast liquid and the calculated resistance change. The change in resistance in the di H_2O and ethanol can be clearly seen, whilst the change in resistance for the control channel was negligible. This suggests that this chip design can be used for Multiplex drop cast functionalisation.

Table 4.19: Average resistances calculated from IV measurements pre and post application of drop cast liquid.

	Pre Liquid Resistance (Ω)	Post-Liquid Resistance (Ω)	PercentageΔ (%)
Channel A (Di H_2O)	6651	7596	+ 12.4
Channel B (Ethanol)	7038	10114	+ 30.4
Channel C (Control)	7533	7473	- 0.8

Multiplex drop cast based functionalisation was tested using this design. Using

10 μl solutions of diluted Aptamers (BasePair Bio, USA) in buffer solution, could be directly drop cast onto individual channels. Thrombin aptamer application buffer was applied to channel 1, brain neuropeptide (BNP) aptamer was applied to the channel 3. During the solution 12 hour incubation period the solutions spread across the SiO_2 surface and combined.

This suggests the Multiplex Dip Chip can be used for individual measurements when applying drop casting test solutions on the surface for short time periods (10 minutes). However, the long incubation periods required for drop cast functionalisation caused the functionalisation buffers to mix resulting in a non specific sensor surface. Additional packaging (microfluidic structures) is thus required for successful multiplex functionalisation.

Inverted MOSFET Design Optimisation & Testing

The Inverted MOSFET design was created to enable gated FET style measurements of the graphene channels. The design uses a buried metal back gate design to allow the graphene surface to be open. This will enable sensing experiments to be performed in both liquid and dry environments. This design could also allow for individual graphene channels to be gated under different gate bias' which could allow greater measurement flexibility in the future.

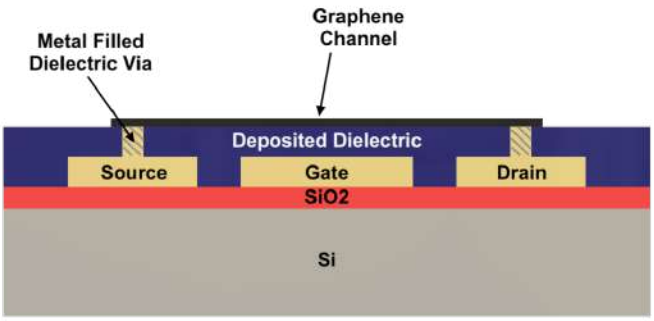
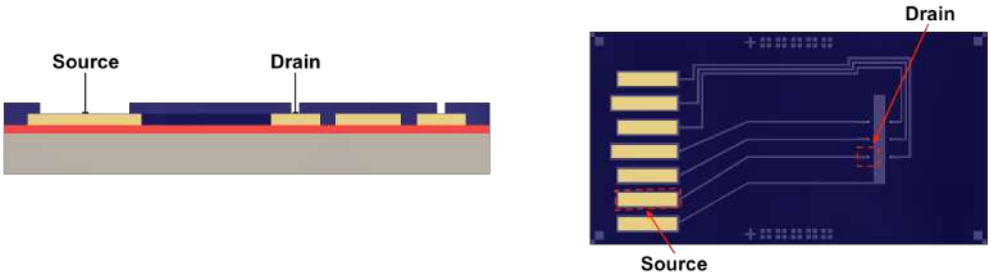


Figure 4.55: Infographic of the Inverted MOSFET design Dip Chip.

The main process flow outlined for the Inverted MOSFET Design uses several processes optimised in the Pre-Transfer and Post-Transfer process flows. The first new process is the dielectric deposition step, two materials SiO_2 and Al_2O_3 were trialled as the gate dielectric. Both materials have been used as standard gate oxide dielectrics [41].

For the dielectric etch step with deposited SiO_2, BOE etching was trailled, The etch was successful for the window to the contact electrodes at the base of the chip. However. the dielectric vias for graphene contact did not etch through, this was due to the photoresist etch mask acting as hydrophobic boundary preventing BOE entering the 50 μm diameter dielectric via. Using an RIE SiO_2 etch process, the SiO_2 layer was successfully etched through in both the contact electrodes and graphene contact vias. To confirm the dielectric via was etched through to the metal layer below, IV measurements were performed between the from graphene contact via and the contact electrodes and was confirmed as conductive (Figure 4.56).



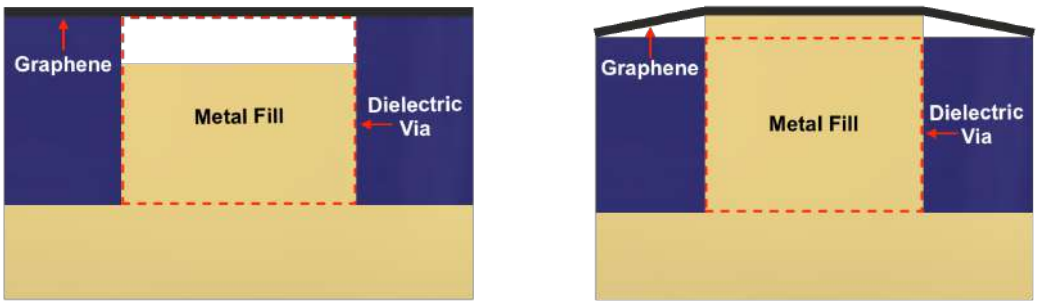
(a) Cross Section (b) ISO

Figure 4.56: (a) Cross section representation of Inverted MOSFET Chip post-dielectric etch. Checking the metal contact electrodes are exposed by IV measurement check (b) Full Inverted MOSFET CAD design showing contact electrodes and graphene contact vias.

The Al_2O_3 deposited dielectric was etched using Microchemicals AZ 726 developer during the photolithography step. The etch was shown to be successful using the IV measurement test and confirmed as conductive pathway.

The next process step was the metal filling of the etched vias using PVD metal

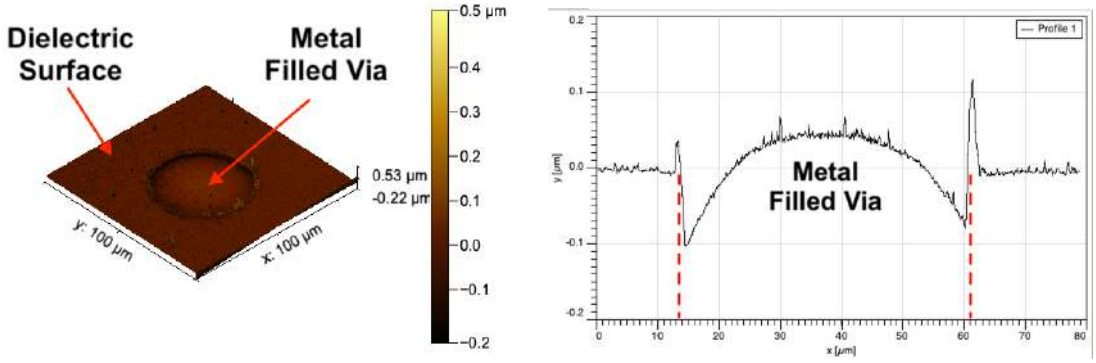
deposition. To determine whether the estimated PVD metal deposition had a step height above the dielectric surface. If the metal deposition does not reach the dielectric surface level the graphene would not be able to make contact with the metal post transfer (Figure 4.57). AFM was performed around the filled dielectric via area.



(a) Cross Section (b) ISO

Figure 4.57: (a) Cross section representation dielectric metal fill below dielectric surface, graphene cannot make contact with the metal. (b) Cross section representation dielectric metal fill above dielectric surface, graphene makes electrical connection with the metal.

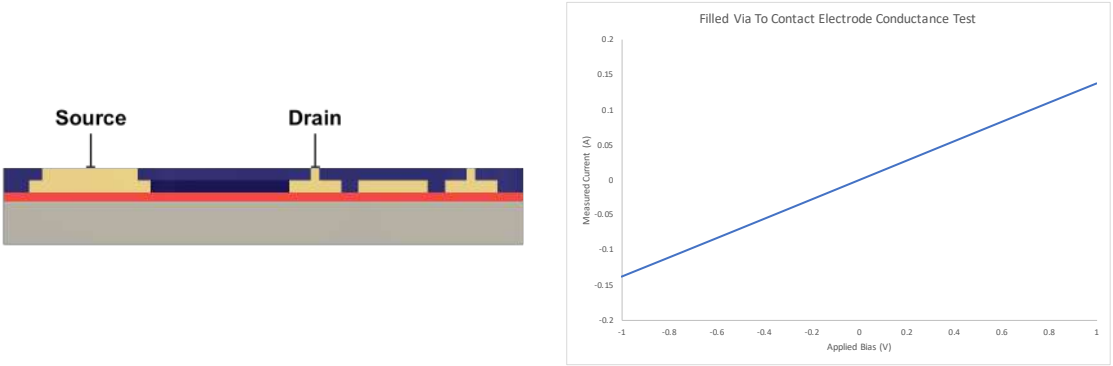
Figure 4.58 shows the AFM surface profile of metal filled via, the cross section shows the metal fill successfully reaches the dielectric surface. However, due to the metal sputtering technique the shadow effects of the via create a greater fill region in the centre of the via, creating a dome for graphene metal contact. Electrical testing Post-Transfer of the graphene layer will be needed to confirm electrical contact.



(a) Cross Section (b) ISO

Figure 4.58: (a) 3D view of metal filled dielectric via 50 μ diameter, some rough edge effects can be seen where excess metal deposited on the top ridge of the via. (b) Cross section profile of metal filled dielectric via showing a metal dome structure total dome height 44 nm above the dielectric surface.

After the metal fill step standard IV measurements were performed before the graphene transfer process to confirm conductance of the deposited metal. Both the SiO_2 and Al_2O_3 devices were shown to be conductive. Figure 4.59 shows an example IV measurement of the metal filled via to contact electrode resistance below 100 Ω.



(a) (b)

Figure 4.59: (a) Cross section diagram of metal filled dielectric vias for IV measurement conductivity test. (b) IV measurement of Inverted MOSFET design chip, metal filled via to contact electrode

Post-Graphene transfer IV measurements were performed on the graphene chan-

nels. Figure 4.60 shows the transferred graphene produces an ohmic contact. This suggests the metal filled vias are able to contact the graphene sheet. The calculated resistance was within the normal range for both the SiO_2 and Al_2O_3 gate dielectric.

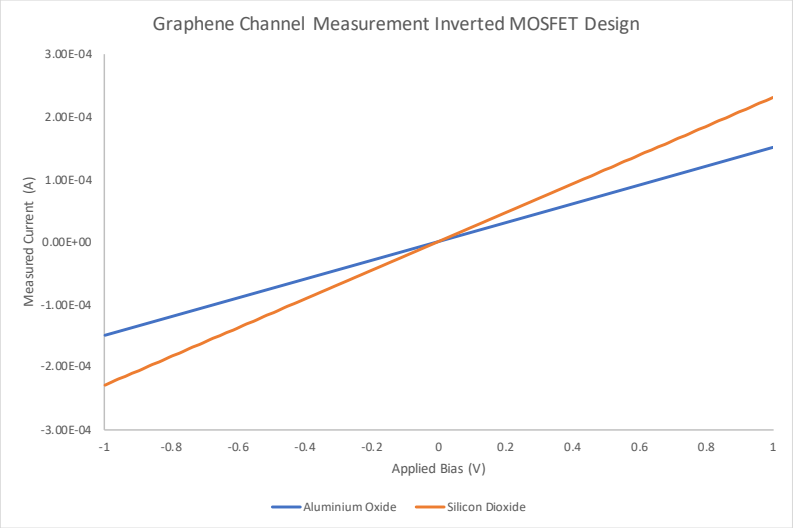


Figure 4.60: IV Measurement of Post-Transfer graphene channel on SiO_2 and Al_2O_3 deposited dielectrics.

Field Effect Transistor Measurements The inverted MOSFET design chips were tested using Gated FET devices in which the channel resistance is measured as a function of the gate voltage. Firstly the SiO_2 gate dielectric devices were tested. Figure 4.61 shows the Family of Drain curves Drain Voltage against Drain Current. The results show a change in channel conductance based on gate voltage. However, the resistance of the channel also changes throughout the measurement this indicates current leakage from the gate electrode.

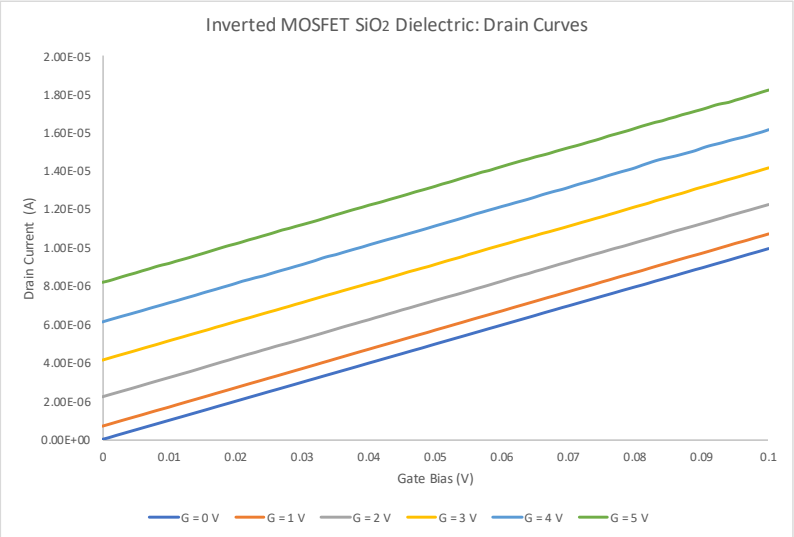


Figure 4.61: Drain Curve IV measurements gate bias applied to buried gate 0 V to 5 V

To investigate the potential leakage through the SiO_2 layer an IV measurement was performed between the buried gate and the graphene channel. Figure 4.62 shows the IV data of the leak check. The resistance measured through the SiO_2 was calculated as 57 kΩ with a current of 1.77 x 10^{-5} at 1 V, this is much higher than thermal SiO_2 where current should be in the sub nA range [42].

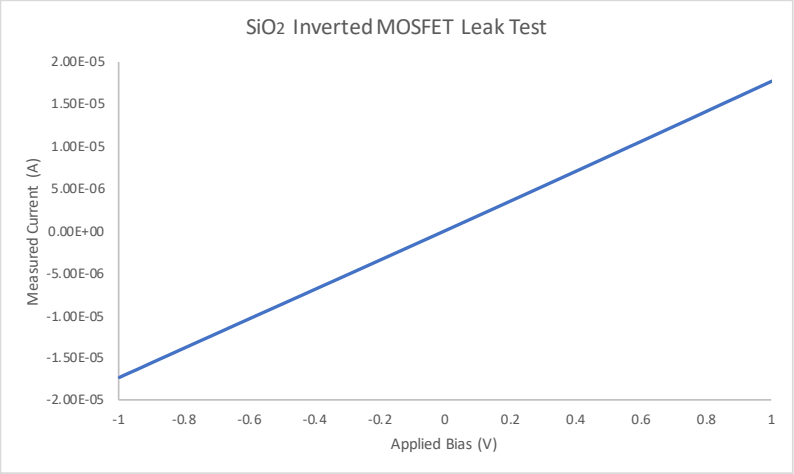


Figure 4.62: IV measurement of buried gate to graphene channel through SiO_2 dielectric layer.

This suggests the PECVD deposition SiO_2 is unsuitable as the gate dielectric layer. This could be due to the plasma processing which can include particle contamination as well as surface damage from the energetic plasma species leading to "pin holes" [43] . This suggests SiO_2 cannot be used as the dielectric layer for the Inverted MOSFET Design Dip Chip at this thickness.

Investigating MVD deposited Al_2O_3, gated FET measurements were performed to identify the effectiveness of the buried gate electrode (Figure 4.63).

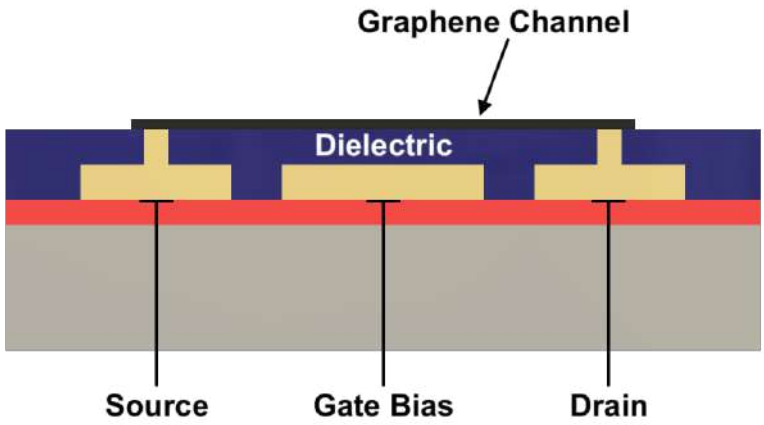


Figure 4.63: Diagram of gated FET measurement performed on Inverted MOSFET design Dip Chip, using the buried metal electrode as the gate electrode.

Figure 4.64 shows the drain family of gated IV measurements, the current can be seen to decrease as the gate bias is increased. The rate of change in resistance was calculated as 281 $\pm$71 Ω/V_G. Each current measurement crosses the Y axis at 0 V showing no signs of current leakage seen in the SiO_2 deposited chips.

To compare the effectiveness of the buried metal gate, a standard Post-Transfer Dip Chip was fabricated using an Si Gate etch process. The bulk P-type silicon was used to perform gated FET measurements on the standard Dip Chip design (Figure 4.65).

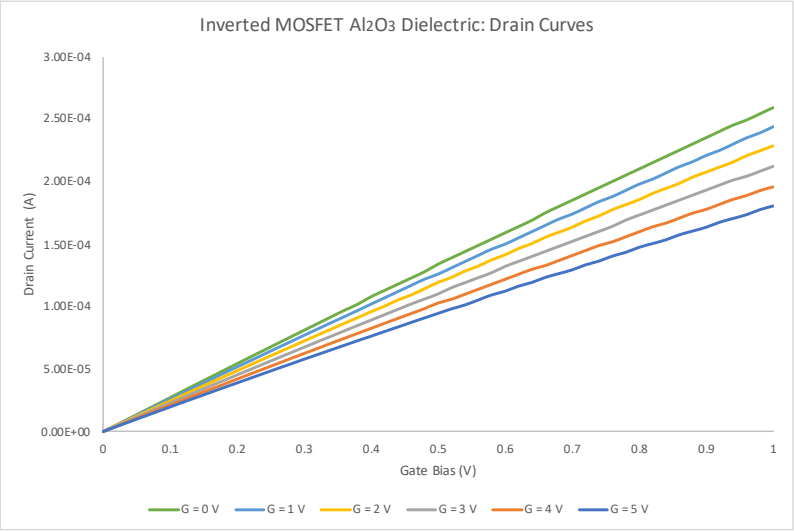


Figure 4.64: Drain Curve IV measurements with gate bias applied to buried gate (0 V to 5 V) using buried metal gate.

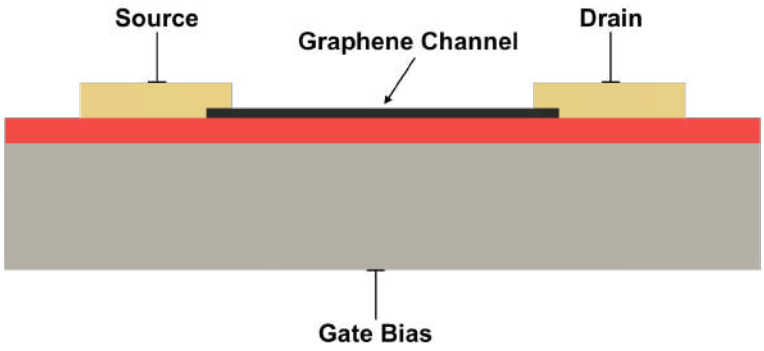


Figure 4.65: Diagram of gated FET measurement performed on standard Dip Chip, using the bulk silicon as the gate electrode.

Figure 4.66 shows the resulting FET measurements performed using bulk silicon gating of a standard Post-Transfer Dip Chip device. The rate of change in resistance was calculated as 423 $\pm$96 Ω/V_G this is higher than the measurement on the Inverted MOSFET design. However, this could be accounted for by the smaller area of the buried gate electrode not encompassing the whole of the graphene channel.

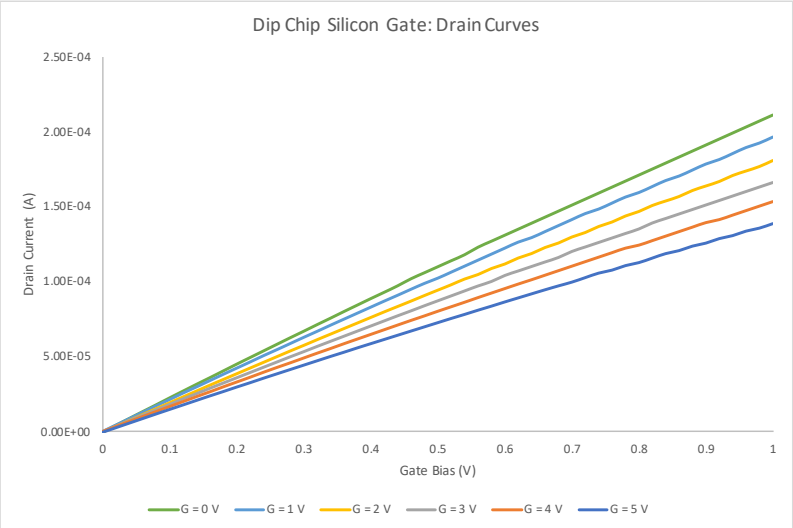


Figure 4.66: Drain Curve IV measurements gate bias applied to buried gate 0 V to 5 V using bulk silicon gate.

The Inverted MOSFET Design using MVD Al_2O_3 gate dielectric can be effectively used to perform gates graphene measurements. For further validation a Dirac point IV measurement was made using the inverted MOSFET design. Figure 4.67 shows the Dirac point measurement with peak neutrality point (Dirac Point) approximately 30 V. This confirms that the Inverted MOSFET Design Dip Chip can be effectively used as graphene FET device.

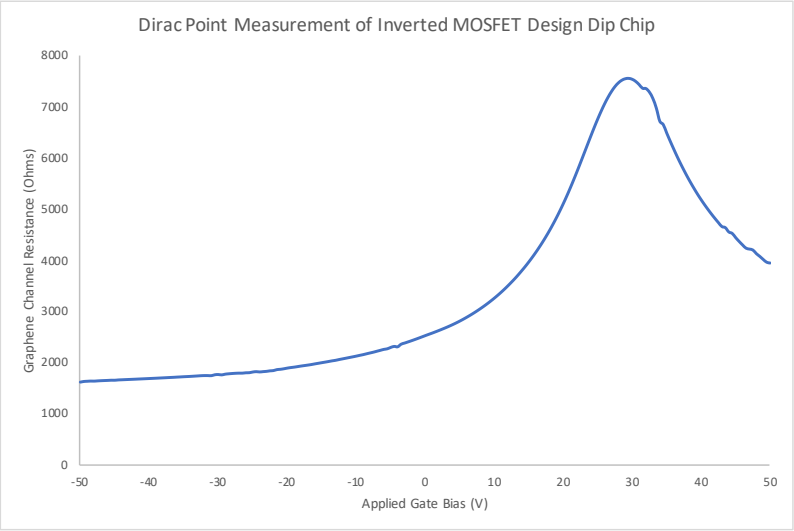
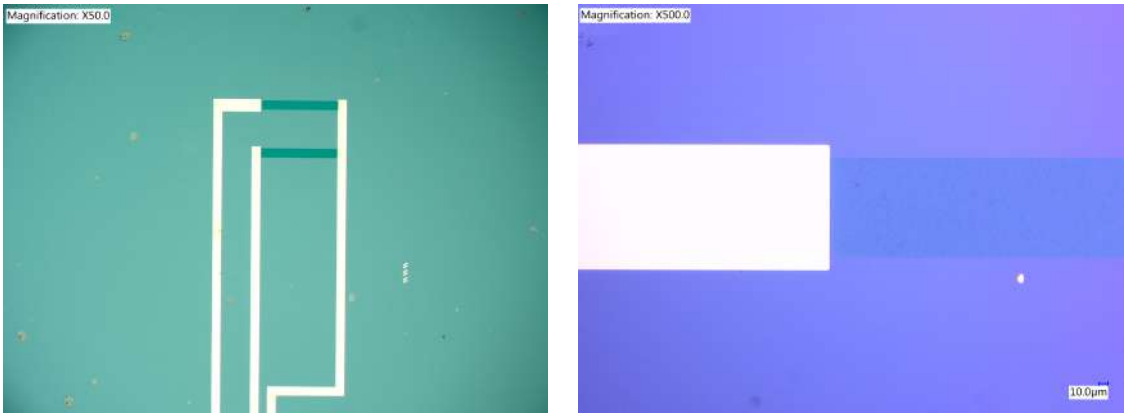


Figure 4.67: Gated FET measurement -50 to 50 V gate bias sweep, Dirac point style measurement

Shared Source Design: Electrical Testing

The Shared Source Electrode design was created to increase yield of graphene channels per chip (5 graphene channels), whilst keeping the fabrication process flow (and fabrication cost) the same. This increase in graphene channels will reduce total fabrication cost per channel and would enable more repeats in a sensing based experiment.

The fabrication process flow for the Shared Source design can follow either the Pre-Transfer flow or Post-Transfer flow. Figure 4.68 shows the Shared Source design Dip Chip fabricated using the Pre-Transfer fabrication method.



(a) (b)

Figure 4.68: (a) Light Microscope image 50x zoom of right cluster metal tracks, (b) Light Microscope image 500x zoom of graphene channel right cluster.

Checking individual resistance measurements for the Shared Source Design could not be performed simultaneously using the PCB connector set up due to shared source. Figure 4.69 shows IV measurements performed sequentially on each of the graphene channel. The data shows ohmic contacts for all 5 channels on a single chip. The average resistance for a single chip was 7112 $\pm$667 Ω. This design is a simple method to increase the number of graphene channels per chip with no extra costs, of additional fabrication steps.

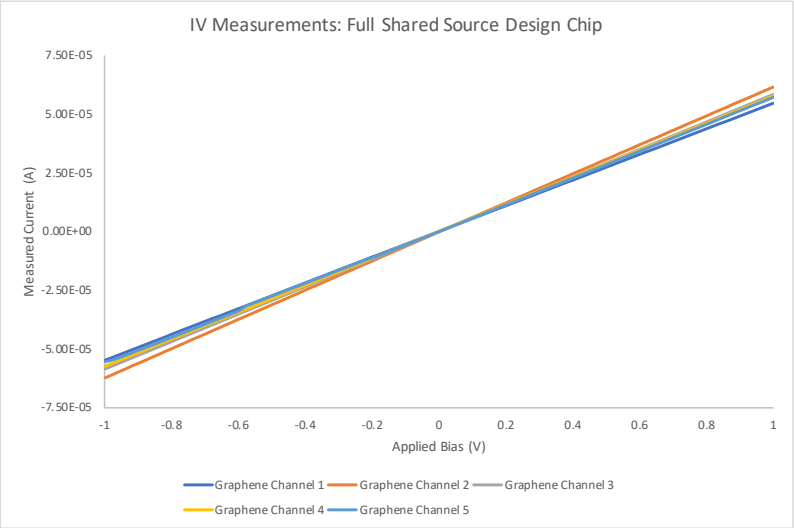
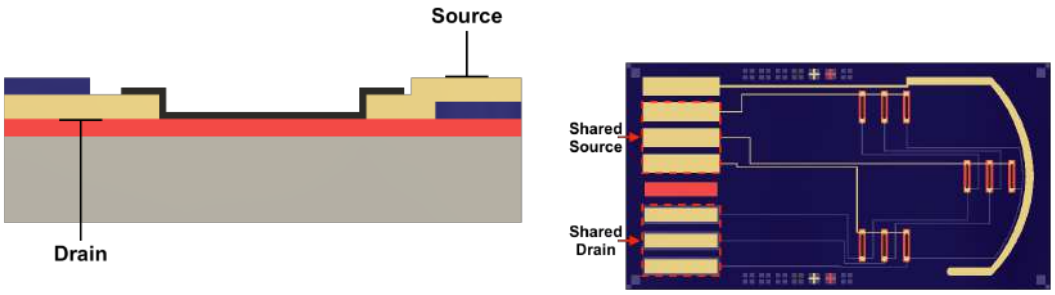


Figure 4.69: IV measurements shows all graphene channels have a linear response and ohmic contact.

Matrix Design: Fabrication Optimisation & Testing

The Matrix design was created to maximise the total number of graphene channels per chip (9 graphene channels). The design requires additional processing steps but the price per channel is estimated to be less than even the Shared Source design. The increase to 9 graphene channels will also allow for the total number of measurement repeats to increase further (more reliable diagnostics).



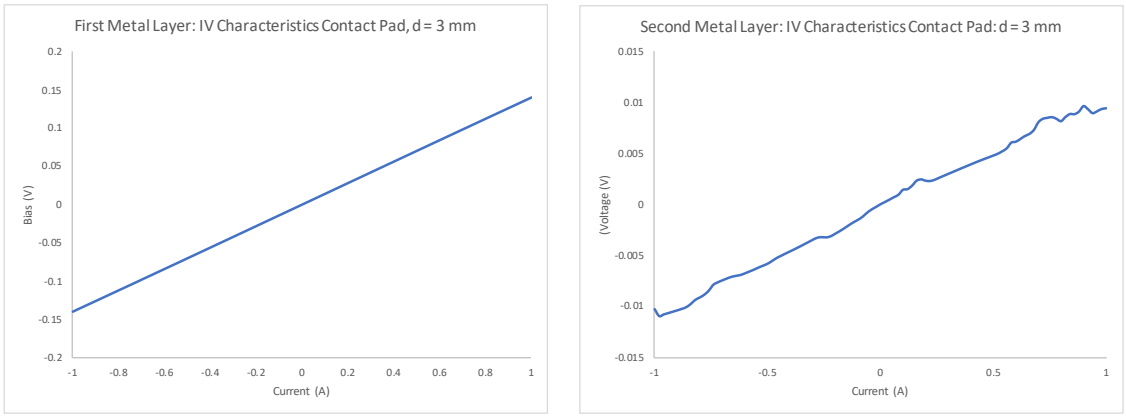
(a) (b)

Figure 4.70: (a) Cross section of Matrix design electrical measurement per graphene channel. (b) Full CAD diagram of Matrix design chip showing shared source and shared drain contact pads.

To fabricate the Matrix Design chip, extra process steps are required in order to produce an insulating layer between the crossing metal tracks. The first approach used permanent photo resist EpoClad5. This was spun directly onto the first patterned metal layer onto the SiO_2 wafer surface, the thickness of the EpoClad was measured by Elipsometry as 4.87 μm (Mean Square Error = 7.65).

The first and second metal layers were photo-patterned using Bi-Layer photoresist and Metal-Lift off using standard processes described previously in the fabrication process flow. Electrical leak tests were performed using the IV Probe Station between the two metal layers across the deposited EpoClad layer. However, during testing the surface of the metal was too fragile/uneven to make good electrical contact between the probe tip and contact pad.

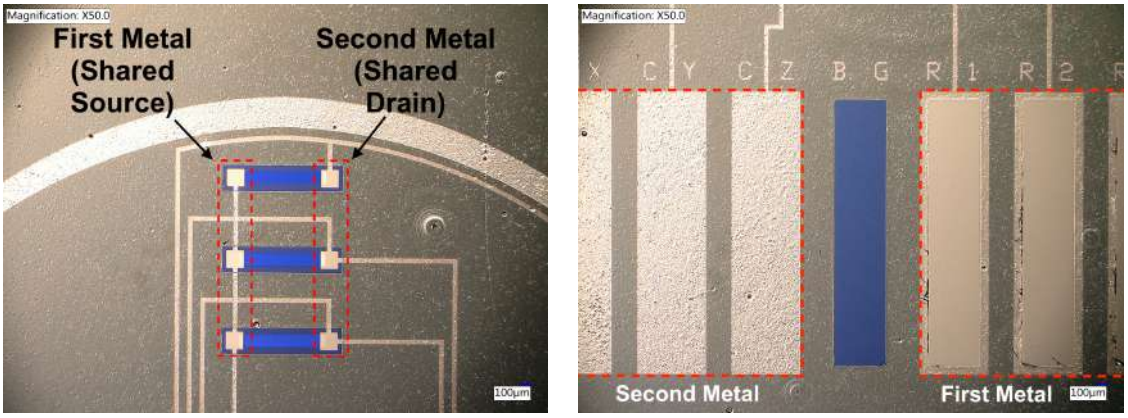
Figure 4.71 (a) shows the IV measurement across the a contact pad from the 1^{st} metal layer (metal deposited onto SiO_2/Si base substrate), the resulting IV measurement shows ohmic contact. The resistance calculated for the first metal layer was 6.21 Ohms (approximate). Figure 4.71 (b) shows the IV across a contact from the 2^{nd} metal layer (metal deposited onto EpoClad layer), the resulting IV measurement showed noise. The resistance of the second metal was calculated as 92.48 a difference of 171 %. With the metal thickness and geometry of the contact pad the same the only variation was the underlying substrate. This data suggests that EpoClad should not be used as the insulation (interlayer) for the Matrix design.



(a) (b)

Figure 4.71: (a) Voltage sweep -1 V to 1 V measuring current on Cr Pd contact pad first metal layer deposited onto polished SiO_2 substrate, probe position approximately 3 mm apart. (b) Voltage sweep -1 V to 1 V measuring current on Cr Pd contact pad second metal layer deposited onto EpoClad5 layer, probe position approximately 3 mm apart.

Aluminium Oxide was also investigated as high κ dielectric material that was successfully used as the gate insulating layer in the Inverted MOSFET design. This method will conformally coat the metal electrode layers even with a deposition of 50 nm Aluminium Oxide onto the first metal electrode mask with a metal thickness of 100 nm. Figure 4.72 shows a finished Matrix Design chip.



(a) (b)

Figure 4.72: (a) Shows the centre cluster of graphene channels, the left contact square pads represent a shared Source electrode and the right hand side represent individual Drain electrodes (b) The first metal layer can be seen on the right hand side, the second metal layer can be seen on the left hand side as the metal is deposited onto Al_2O_3. The centre "B G" (back gate) region represents a region of bare Silicon Dioxide that can be removed to make gate contact to the bulk silicon.

To check the results were not affected by any leakage current from electrode to electrode through the 50 nm Al_2O_3 layer, source-drain measurements were applied to the first and second metal layers as an attempt to measure leakage current across the Al_2O_3 layer. An IV sweep was performed (-10V - 10 V), no signal was measured therefore it was assumed that the leakage current was below the measurable range so would not effect the measurements. A capacitance measurement was performed using an electrical multimeter and gave a 1.05 nF response suggesting no leakage through the dielectric layer.

To confirm all graphene channels can be measured individually and produce their own unique current measurement, the IV probe station was used to perform IV measurements on all 9 graphene channels, using all electrode combinations. Figure 4.73 and Figure 4.74 shows the resulting IV measurements for all 9 graphene channels of a single Dip Chip. This data indicates all 9 graphene channels can be measured independently and therefore the Matrix design is the most efficient design in terms

of the number of graphene channels per chip for electrical based measurements.

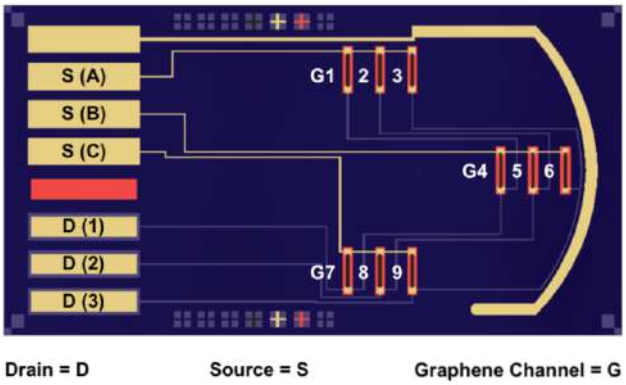


Figure 4.73: Diagram of IV measurements for all graphene channels.

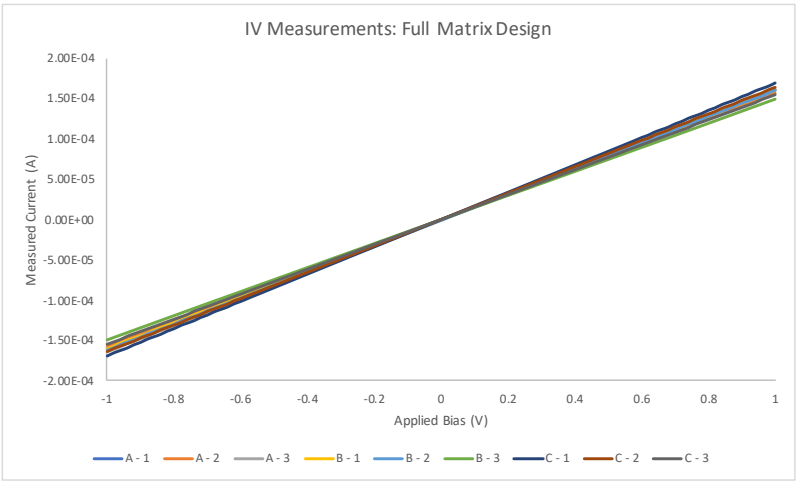


Figure 4.74: IV measurements of all graphene channels produce a linear/ohmic response.

4.6 Summary

Two main fabrication approaches have been developed for graphene sensors. The Pre-Transfer process, where graphene where the graphene is supplied on a SiO_2/Si and is present throughout the device fabrication process, and the Post-Transfer process, where the device metal contacts are processed first and followed by graphene

transfer onto the metal and SiO_2/Si substrate, the graphene is then present for the remaining process steps.

The Pre-Transfer and Post-Transfer fabrication process both produce low two terminal resistance measurements. The Pre-Transfer overall yield of graphene devices was on average higher that Post-Transfer process with working devices above 85 % yields from batch to batch. The Pre-Transfer inter-device resistance variability can be reduced with the use of an yttrium sacrificial layer process, preventing any photoresist from coming into contact with graphene surface throughout the processing procedure. The yttrium modified process also reduces total photoresist residue seen in the Pre-Transfer process (Raman spectra comparing Pre-Transfer Bi-Layer process to Pre-Transfer yttrium Bi-Layer process).

The main limiting factor of the Pre-Transfer process is the graphene anneal steps that are required to prevent graphene delamination and consequent device yield decreases. The graphene anneal step, performed in both Argon flow TFA and RTA systems, induces strain and doping into the graphene lattice structure (Raman stress strain scatter plots). Different photoresists were also compared, and a reduction in photoresist used throughout the process reduces the total residues present throughout. In terms of contamination, damage and strain the Post-Transfer process produces better quality devices, without the need for annealing, due to the transfer supplier and only using a single photolithography process with limited solvent cleaning required. The quality of these devices made during this process are superior in terms of minimum residues and low defect density. The limiting factors are the total yield being on average slightly lower than the Pre-Transfer process (73 %). The Pre-Transfer process has some advantages over the Post-Transfer process, Pre-Transfer processing produces a graphene edge contact due to the magnetron sputtering of the metal, damaging the graphene contact region. This can produce a lower contact resistance for Pre-Transfer devices. Both process flows should be improved with post process annealing of the metal contacts and further thermal cleaning of the graphene surface. This was limited in this research due to the added contamination from the furnace sources. Further research into the substrate

supporting the graphene should be conducted, as there is a lot of interest into the use of multiple 2D materials such as hexagonal boron nitride (increasing the carrier mobility of the graphene), and research into the doping effect of the substrate on the graphene channel (Bringing the Dirac point closer to 0 V).

In conclusion the designs put forward in this chapter have each solved an engineering challenge. The original Dip Chip design has enabled much faster data acquisition and facilitated easy set up of multi SMU measurements compared with the IV probe station measurements. The main advantage of this design is the ability to make full liquid submersion measurements without risk to the back end interconnects to each chip. It also allows rapid transfer between chips and solutions. The original design was multi-functional allowing for additional electrodes for electrochemistry-based measurements as well as purely electrical resistor-based measurements. These electrochemistry-based functionalisation processes can be achieved "on chip".

However, this design of Dip Chip is limited in terms of multiplex capability, all graphene channels arranged so close that functionalisation solutions will cross-contaminate from channel to channel. The Multiplex Design allows for application of up to two drop cast functionalisation chemistries as well as a control channel left non-functionalised. Alternatively, this could also be used to functionalise each of the three channels separately via a drop cast method. However, for individual electrochemical functionalisation this design suffers in the same way as the standard Dip Chip, in that all channels are immersed in the same solution. Even though a majority of the electrochemical material is functionalised on the specific channel, there is some cross contamination due to the channels all still being in close proximity and within the same solution. Further packaging is needed to enable integration with the chip for use with electrochemical functionalisation chemistries on each channel.

The Inverted MOSFET design addresses an additional working mode for the graphene chips; the ability to perform gated measurements isolated from the silicon substrate. This has been used to create an electric field that changes the conductivity of the graphene channel in a similar way to back gating the device using the bulk silicon as the gate electrode. This opens up future avenues of making dry gated and

liquid G-FET sensing measurements. The gate electrode is not submerged in ionic preventing the risk of the bulk silicon gating the ionic liquid. Also future designs using additional electrodes could allow the graphene channels to be individually gated using different potentials on each channel of interest opening up different research fields (e.g. CMOS). Or using different substrate and metals fully transparent G-FET systems could be investigated for photoelectronic research.

The last chip designs aimed to increase the total number of graphene channels per chip which could eventually increase the number of functionalisation chemistries per chip, but also reduce the total cost per channel of the sensor. The obvious way to reduce cost per chip is to reduce die size and add additional packaging. However, at this testing phase, the aim was to maintain the die size and electrode layout to be compatible with SD card connector. A simple modification used to shared source electrode between each graphene channel and individual drain electrodes. This produces an increase in the number of graphene channels without introducing additional fabrication steps. This design does limit the chips usability for electrochemistry, as each graphene channel is now connected. Thus so for CV and IES the channels will all respond as one electrode. The largest increase in graphene channels per chip comes in the Matrix design, this increases the graphene channels by 3 times more than the original Dip Chip design. This does increase the total number of process steps, hence increasing fabrication costs. However, for future designs and decreasing die size or increasing electrode number this design clearly excels in increasing graphene channel numbers and should be incorporated in purely electrical based systems.

Bibliography

[1] Ryan Michael Bigham. Development of process technology for silicon and graphene biosensor devices. Technical report, Swansea University, 2019.

[2] Siva Kumar Krishnan, Eric Singh, Pragya Singh, Meyya Meyyappan, and Hari Singh Nalwa. A review on graphene-based nanocomposites for electrochemical and fluorescent biosensors. *RSC advances*, 9(16):8778–8881, 2019.

[3] Sowmya Viswanathan, Tharangattu N Narayanan, Kiana Aran, Kathryn D Fink, Jacobo Paredes, Pulickel M Ajayan, Slawomir Filipek, Przemyslaw Miszta, H Cumhur Tekin, Fatih Inci, et al. Graphene–protein field effect biosensors: glucose sensing. *Materials Today*, 18(9):513–522, 2015.

[4] M Mitchell Waldrop. The chips are down for moore's law. *Nature News*, 530(7589):144, 2016.

[5] Peter O Hahn. The 300 mm silicon wafer—a cost and technology challenge. *Microelectronic Engineering*, 56(1-2):3–13, 2001.

[6] Inc Apacer Technology. microsd card. Datasheet, Apacer Technology, Inc, 2013.

[7] Charles Mackin, Vera Schroeder, Amaia Zurutuza, Cong Su, Jing Kong, Timothy M Swager, and Tomás Palacios. Chemiresistive graphene sensors for ammonia detection. *ACS applied materials & interfaces*, 10(18):16169–16176, 2018.

[8] Ning Gao, Teng Gao, Xiao Yang, Xiaochuan Dai, Wei Zhou, Anqi Zhang, and Charles M Lieber. Specific detection of biomolecules in physiological solutions using graphene transistor biosensors. *Proceedings of the National Academy of Sciences*, 113(51):14633–14638, 2016.

[9] Ning C. Wang, Enrique A. Carrion, Maryann C. Tung, and Eric Pop. Reducing graphene device variability with yttrium sacrificial layers. *Applied Physics Letters*, 110(22):223106, May 2017.

[10] Mitchell B Lerner, Deng Pan, Yingning Gao, Lauren E Locascio, Kian-Yong Lee, Jolie Nokes, Savannah Afsahi, Jeremy D Lerner, Amy Walker, Philip G Collins, et al. Large scale commercial fabrication of high quality graphene-based assays for biomolecule detection. *Sensors and Actuators B: Chemical*, 239:1261–1267, 2017.

[11] Kun Xu, Caifu Zeng, Qin Zhang, Rusen Yan, Peide Ye, Kang Wang, Alan C. Seabaugh, Huili Grace Xing, John S. Suehle, Curt A. Richter, and et al. Direct measurement of dirac point energy at the graphene/oxide interface. *Nano Letters*, 13(1):131–136, Dec 2012.

[12] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis. Single-layer mos2 transistors. *Nature Nanotechnology*, 6(3):147–150, Jan 2011.

[13] Zhaoli Gao, Hojin Kang, Carl H Naylor, Frank Streller, Pedro Ducos, Madeline D Serrano, Jinglei Ping, Jonathan Zauberman, Robert W Carpick, Ying-Jun Wang, et al. Scalable production of sensor arrays based on high-mobility hybrid graphene field effect transistors. *ACS applied materials & interfaces*, 8(41):27546–27552, 2016.

[14] Wei Sun Leong, Haozhe Wang, Jingjie Yeo, Francisco J Martin-Martinez, Ahmad Zubair, Pin-Chun Shen, Yunwei Mao, Tomas Palacios, Markus J Buehler, Jin-Yong Hong, et al. Paraffin-enabled graphene transfer. *Nature communications*, 10(1):867, 2019.

[15] Wei-Hsiang Lin, Ting-Hui Chen, Jan-Kai Chang, Jieh-I Taur, Yuan-Yen Lo, Wei-Li Lee, Chia-Seng Chang, Wei-Bin Su, and Chih-I Wu. A direct and polymer-free method for transferring graphene grown by chemical vapor deposition to any substrate. *ACS nano*, 8(2):1784–1791, 2014.

[16] Quang Hung Trinh, Md Mokter Hossain, Seong H Kim, and Young Sun Mok. Tailoring the wettability of glass using a double-dielectric barrier discharge reactor. *Heliyon*, 4(1):e00522, 2018.

[17] J Schwan, Sven Ulrich, V Batori, H Ehrhardt, and SRP Silva. Raman spectroscopy on amorphous carbon films. *Journal of Applied Physics*, 80(1):440–447, 1996.

[18] Andrea C Ferrari and Denis M Basko. Raman spectroscopy as a versatile tool for studying the properties of graphene. *Nature nanotechnology*, 8(4):235, 2013.

[19] Luca Banszerus, Hendrik Janssen, Martin Otto, Alexander Epping, Takashi Taniguchi, Kenji Watanabe, Bernd Beschoten, Daniel Neumaier, and Christoph Stampfer. Identifying suitable substrates for high-quality graphene-based heterostructures. *2D Materials*, 4(2):025030, 2017.

[20] Ji Eun Lee, Gwanghyun Ahn, Jihye Shim, Young Sik Lee, and Sunmin Ryu. Optical separation of mechanical strain from charge doping in graphene. *Nature communications*, 3:1024, 2012.

[21] Sunmin Ryu, Li Liu, Stephane Berciaud, Young-Jun Yu, Haitao Liu, Philip Kim, George W Flynn, and Louis E Brus. Atmospheric oxygen binding and hole doping in deformed graphene on a sio2 substrate. *Nano letters*, 10(12):4944–4951, 2010.

[22] Santanu Das, Debrupa Lahiri, Arvind Agarwal, and Wonbong Choi. Interfacial bonding characteristics between graphene and dielectric substrates. *Nanotechnology*, 25(4):045707, 2014.

[23] Jothiramalingam Kulothungan, Manoharan Muruganathan, and Hiroshi Mizuta. An in-situ annealing effect of graphene-graphene interlayer conduction. *arXiv preprint arXiv:1903.09899*, 2019.

[24] Hyeon Jun Hwang, Yongsu Lee, Chunhum Cho, and Byoung Hun Lee. Facile process to clean pmma residue on graphene using krf laser annealing. *AIP Advances*, 8(10):105326, 2018.

[25] Peter Ramm, James Jian-Qiang Lu, and Maaike MV Taklo. *Handbook of wafer bonding*. John Wiley & Sons, 2011.

[26] Ephraim Suhir, Yung-Cheng Lee, and CP Wong. *Micro-and opto-electronic materials and structures: physics, mechanics, design, reliability, packaging: Volume I Materials physics-materials mechanics. Volume II Physical design-reliability and packaging*, volume 1. Springer Science & Business Media, 2007.

[27] Eiichiro Watanabe, Arolyn Conwill, Daiju Tsuya, and Yasuo Koide. Low contact resistance metals for graphene based devices. *Diamond and Related Materials*, 24:171–174, 2012.

[28] Amit Gahoi, Stefan Wagner, Andreas Bablich, Satender Kataria, Vikram Passi, and Max C Lemme. Contact resistance study of various metal electrodes with cvd graphene. *Solid-State Electronics*, 125:234–239, 2016.

[29] Teresa Cusati, Gianluca Fiori, Amit Gahoi, Vikram Passi, Max C Lemme, Alessandro Fortunelli, and Giuseppe Iannaccone. Electrical properties of graphene-metal contacts. *Scientific reports*, 7(1):5109, 2017.

[30] Darren George. *SPSS for windows step by step: A simple study guide and reference, 17.0 update, 10/e*. Pearson Education India, 2011.

[31] Filippo Giubileo and Antonio Di Bartolomeo. The role of contact resistance in graphene field-effect devices. *Progress in Surface Science*, 92(3):143–175, 2017.

[32] GAKPA Giovannetti, PA Khomyakov, G Brocks, VM vd Karpan, J Van den Brink, and Paul J Kelly. Doping graphene with metal contacts. *Physical review letters*, 101(2):026803, 2008.

[33] C-T Chen, Emanuele A Casu, Martin Gajek, and Simone Raoux. Low-damage high-throughput grazing-angle sputter deposition on graphene. *Applied Physics Letters*, 103(3):033109, 2013.

[34] Isaac Childres, Luis A Jauregui, Wonjun Park, Helin Cao, and Yong P Chen. Raman spectroscopy of graphene and related materials. *New developments in photon and materials research*, 1, 2013.

[35] Sung Kyu Jang, Jaeho Jeon, Su Min Jeon, Young Jae Song, and Sungjoo Lee. Effects of dielectric material properties on graphene transistor performance. *Solid-State Electronics*, 109:8–11, 2015.

[36] Zhaoying Hu, Dhiraj Prasad Sinha, Ji Ung Lee, and Michael Liehr. Substrate dielectric effects on graphene field effect transistors. *Journal of Applied Physics*, 115(19):194507, 2014.

[37] Nikhil Jain, Tanesh Bansal, Christopher A Durcan, Yang Xu, and Bin Yu. Monolayer graphene/hexagonal boron nitride heterostructure. *Carbon*, 54:396–402, 2013.

[38] Ramy M Qaisi, CE Smith, Mohamed T Ghoneim, Qingkai Yu, and Muhammad Mustafa Hussain. Direct measurement of graphene contact resistivity to pre-deposited metal in buried contact test structure. In *2013 13th IEEE International Conference on Nanotechnology (IEEE-NANO 2013)*, pages 890–893. IEEE, 2013.

[39] Sam Vaziri. Fabrication and characterization of graphene field effect transistors, 2011.

[40] Shun Mao, Jingbo Chang, Haihui Pu, Ganhua Lu, Qiyuan He, Hua Zhang, and Junhong Chen. Two-dimensional nanomaterial-based field-effect transistors for chemical and biological sensing. *Chemical Society Reviews*, 46(22):6872–6904, 2017.

[41] G Ribes, J Mitard, M Denais, S Bruyere, F Monsieur, C Parthasarathy, E Vincent, and Ge Ghibaudo. Review on high-k dielectrics reliability issues. *IEEE Transactions on Device and materials Reliability*, 5(1):5–19, 2005.

[42] Robert K Willardson and Albert C Beer. *Semiconductors and semimetals*, volume 12. Academic press, 1977.

[43] Hui Fang, Jianing Zhao, Ki Jun Yu, Enming Song, Amir Barati Farimani, Chia-Han Chiang, Xin Jin, Yeguang Xue, Dong Xu, Wenbo Du, et al. Ultrathin,

transferred layers of thermally grown silicon dioxide as biofluid barriers for biointegrated flexible electronic systems. *Proceedings of the National Academy of Sciences*, 113(42):11682–11687, 2016.

Chapter 5

Graphene Sensor Passivation & Packaging

5.1 Introduction

The aim of passivation and packaging of the graphene FET sensor is to improve the efficiency of fabrication and functionalisation of the sensor, as well as its overall stability and sensitivity. The aim of packaging was also for improved usability and handling in terms of sample pre-processing and measurement taking, for the future goal of developing a diagnostic-based point of care sensor.

Passivation is used to protect the metal electrodes, isolating them from the reactions with chemicals used to modify the graphene surface, and from the reagents used for electrochemical reactions. This is particularly relevant in terms of electrochemical based sensing that applies a potential to the graphene surface, whereby any region of the exposed electrode (Graphene or exposed metal) will create the circuit and therefore impact the measurement. Being unsure of whether the functionalisation is primarily effecting the metal contacts or the graphene surface affects the reproducibility of the sensor measurement.

In terms of purely resistance-based measurements, it is also important to isolate the metal electrodes from the solution in which the measurement is being taken. In the case of sensing in PBS salt-based solutions or when sensing analytes present in a human blood plasma, the liquid environment can be highly ionic and result in short-circuiting; bypassing the graphene surface and making the measurement invalid.

Additionally, design and fabrication of a microfluidic packaging for the sensor

requires a uniform surface with controlled surface chemistry, which simplifies the adhesion process for the packaging material in contact with the chip surface. Passivation layers also prevent potential damage to graphene channels when small dimension microfluidic channels are applied close to the graphene-metal contact boundary when packaging is applied.

Both polymeric based passivation materials, as well as silicon-based dielectrics and metal oxide-based dielectric films, have been investigated. The challenges for passivating the graphene device relate to the deposition of a dielectric material without damaging the graphene surface. This also includes the removal/etch of the deposited material without inflicting damage. In order to remove passivation layers in selected areas, standard dry etch processes required additional modifications e.g. sacrificial layers, as did wet etch processes. Other approaches such as lift-off were investigated but these suffer from high-temperature deposition processes and cannot be used for highly conformal deposition processes. Polymeric methods were effective but limited in terms of functionality and additionally resulted in more carbon-based residues on the graphene surface.

After passivation the main focus of this chapter is on sensor packaging, the use of external components to integrate microfluidic channels and sample delivery systems with the sensor chip. Micofluidc systems such as PDMS plasma bonding and direct 3D printed microfluidics are trialled to form liquid tight packaging on the graphene sensor surface.

For use in blood clotting diagnostics the sensor packaging must be designed on the understanding of the current operational parameters of clotting diagnostics testing. The elements of a clotting panel that quantitatively perform detection of molecules include the direct fibrinogen test [1] which detects the levels of the molecule fibrinogen in circulation. The other test is for the D-Dimer peptide another bi-product of clotting itself which can be used to monitor clotting events [2]. Both of these molecule detection based tests can help diagnose multiple clotting disorders.

The hospital protocol requires blood samples to be taken from patients using a Trisodium Citrate tube. These (often vacutainer) tubes are then delivered to the lab

within 2 hours for processing. The lab will often hold the samples for up to 24 hours and even freeze processed samples (-40 °C) for further testing if required. For the direct fibrinogen detection method an Immunological assay of the monoclonal assay of fibrinogen is commonly used [3]. More recently aptamer-based assays [4]. Other clotting based disorders (heart/stroke) can also be diagnosed using the immunoassay based approach [5]. Immunoassay based tests require a platelet-poor plasma sample to run the assay to reduce non-specific detectable mass (blood cells). In hospital based labs the blood sample will be separated using centrifuge step at 1500 RCF (Relative Centrifugal Force) for 15 minutes to achieve platelet-poor plasma (platelet count $< 10,000$), this removes a majority of the circulating blood cells enabling an increase in sensitivity of the assay.

To improve diagnostic capability and reduce time processing costs for blood sample preparation, a static microfluidic system for blood separation was investigated, working towards a point of care system requiring only small volumes (prick test 10 - 50 μl) of blood. High flow rates and mass/flow rate difference of different sized particles were investigated towards a rapid sample pre-processing system. Initially, PDMS based microfluidic devices were tested as part of the blood clotting research study. Subsequently, when applying a microfluidic package directly to the graphene chip PDMS proved unreliable for bonding and alignment to the chip surface features. Thus, for development of multiplex functionalisation, the use of microfluidic 3D printing was assessed. Ultimately, both of these methodologies would be replaced with a simple plastic snap-on packaging.

5.2 Passivation

Passivation was shown to be required for both the functionalisation and sensing stages as it is important to isolate the metal tracks out of any solutions. In the case of electrochemical based functionalisation of the graphene channel, both gold nanoparticle deposition and polymerised Diaminonaphthalene (pDAN) require an acid-based solution for graphene functionalisation. This acid solution was expected to have little effect on the metal tracks as they are capped with a noble metal (Pd, Au or Pt) which should not corrode in the 0.25 M H_2SO_4. However, it has been shown that the polymerisation reaction of the pDAN on the graphene surface, as well as gold nanoparticle deposition process, do affect to the metal tracks of the device (capping metal Au) [6].

The electrochemical functionalisation protocol is based on a submersion method or drop cast method. On non-passivated chips, the total area of the metal tracks exposed to the solution is not precisely reproducible. Using the submersion method, the total metal track area depends on submersion depth and angle of the chip holder. The drop-casting method depends on the total area of the dispersion of the droplet. Additionally, the sensitivity of the device will also decrease as the antibody/specific bio-receptor will also attach to all pDAN amine groups available likewise any thiol terminated antibodies would attach to all available gold nanoparticles (reducing the concentration of bio-receptor on the graphene surface). Therefore the target sensing molecule/protein could bind to bio-receptors not on the active sensing area of the graphene channel and could lead to the attachment on the metal tracks of the device. For targets solutions that are extremely dilute ($<$ pg/ml), this would limit the sensitivity of the diagnostic test.

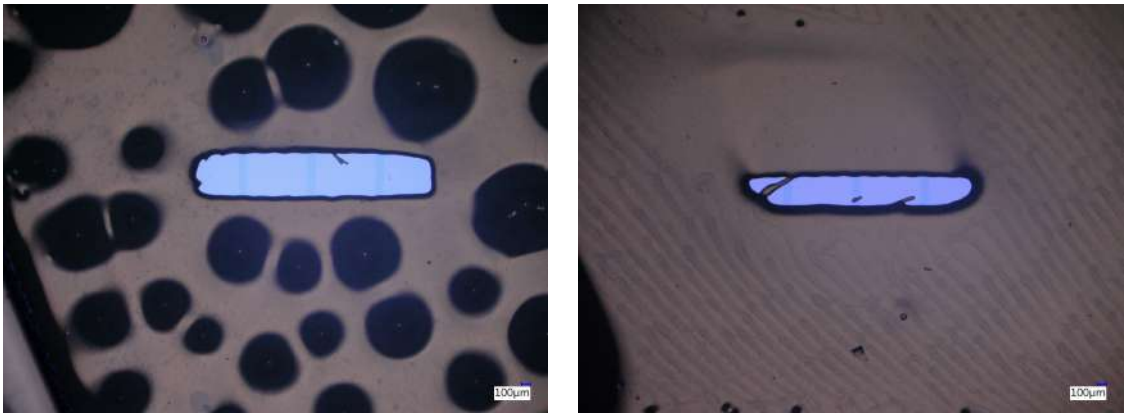
With the addition of a screen printed passivation layer to the graphene chip sensor [6], similar to the screen-printed passivation used in three-electrode Screen Printed Electrode (SPE) sensors, the total active area for polymerisation/electro-deposition is constrained to a smaller and well quantified area. (In the case of screen printed passivation the inaccuracy in passivation was 20 - 30 μm). This allows for

higher levels of reproducibility and should increase the overall sensitivity of the device.

For gated field-effect measurements using the graphene FET style sensing methodology, if the ionic solution used comes into contact with the metal track whilst a bias is applied, the signal could short across the solution. If the graphene channel has a high resistance due to length or functionalisation chemistry, the path of least resistance will be taken. Therefore the measurements taken in ionic liquids specifically during sensing or gated measurements could be affected. The measurement could then become invalid and the sensitivity and reproducibility of the sensor would also decrease.

The screen-printed insulation ink used previously for graphene device passivation [6] is used commercially for large scale flexible sensor fabrication. However, it is not routinely integrated into a semiconductor fabrication process flows. All fabrication processes for the graphene Dip Chip based sensor were cleanroom CMOS foundry level techniques.

The resolution of the printing process used to apply the passivation layer is much lower than the lithography based techniques. A window area of less than 300 μm resolution on the graphene surface would not be achievable using a screen-printed process. Therefore the ability to miniaturise and increase sensor yield is restricted using screen printing. Screen printing alignment for wafer level fabrication is also problematic. A specialist screen printing system would need to be developed for wafer level fabrication as well as being cleanroom compatible. Figure 5.1 shows the issues regarding the resolution and ink spreading outside of the required area result in issues with the graphene active area see.



(a) (b)

Figure 5.1: (a) Shows a standard Dip Chip with screen printed passivation using optimised parameters. The rectangle is not well defined at the edges but the graphene channels are clearly exposed and can undergo the functionalisation with an approximate surface area calculable. (b) A Dip Chip using the same process parameters from a different location on the wafer. The graphene channel area is reduced compared to that in (a), residues from the printing process can also be seen overlapping the graphene active area.

This passivation research has also investigated cleanroom CMOS compatible methodologies to passivate directly onto graphene-based FET sensors (100 mm diameter wafer compatible). Compatible with lithography, deposition and etching methods used to produce a higher level of fabrication accuracy whilst maintaining the graphene in undamaged SP^2 state. This passivation layer would then be able to be incorporated into any future designs and fabrication process flows.

Both photoresists and deposited dielectrics have been employed in semiconductor fabrication since its invention. The primary appeal of photoactive polymers is the low processing costs, a lower number of process steps, (so time and machine costs are reduced). The issues related to photoactive polymers is normally around their permanence and compatibility with functionalisation chemistries. And the polymer residues left on the graphene surface which can decrease the debye length affecting sensitivity of the graphene sensor [7].

Dielectric materials have been examined; they can be robust against multiple chemistries and do not leave behind organic / polymer residues on the graphene surface. The issues related to the dielectric deposition with graphene fabrication are the increased processing costs with multiple fabrication steps required using additional machines for fabrication. Additionally, the environment used in dielectric deposition can be hostile to graphene, as often high temperatures with reactive plasmas are used during fabrication.

5.2.1 Materials & Methods

Base Substrate

For process optimisation of polymeric and dielectric passivation techniques plain wafers without graphene were used to reduce fabrication costs.

Substrates include 100 mm plain Si wafers, 100 mm Si wafers with 300 nm thermal SiO_2 growth and 100 mm Si wafers with 100 nm LPCVD Si_3N_4 deposition (Si-Mat, Germany). Smaller test chips used for process development, the dimensions were 20 x 20 mm pieces diced using diamond tip scribe pen (Fisher Scientific, UK).

Photoresist & Photo-Active Polymers

Polymer-based passivation techniques were photo-patterned using standard spin coating and photolithography processes. Dielectric passivation methods required photo-patterning to produce photoresist Lift-Off masks (nLOF 2070 protocol) and positive masks to produce photoresist etch-masks for dielectric etching (AZ 5214 E photoresist protocol).

All photolithography steps were performed using Laurell Spin Coater and SUSS MA8 Gen3 Mask-aligner (section 3.5).

SU-8 Photolithography parameters can be found in the (Materials & Methods Chapter in section 3.5.3).

AZ nLOF 2070 photolithography parameters can be found in (Materials & Methods Chapter in section 3.5.3). The development time was shortened by 1 minute to

produce a straight edge wall profile. Hard-baking was performed using RTA with a set temperature of 250 °C for 10 minutes under vacuum and Ar flow.

Silicon Nitride: PECVD

Silicon Nitride (Si_3N_4) is a widely used passivation film used for gate and interlayer passivation. Si_3N_4 can deposited directly onto the graphene Dip Chip followed by a selective Si_3N_4 etching process to reveal the graphene channels.

Silicon Nitride Si_3N_4 was deposited using PECVD tool (SPTS, UK) using the deposition recipe (Materials & Methods Chapter section 3.8.2).

Silicon Nitride etch process was performed using the following RIE chamber parameters; CF_4 at 30 sccm diluted in 100 sccm O_2, 150 W and a chamber pressure of 100 mTorr.

The film thickness was measured using J.A. Woolam Ellipsometer and the measurement was analysed using Cauchy fit function and B-Spline fit function. Further details of (Ellipsometry measurement can be found in Materials & Methods Chapter section 3.12.5).

Figure 5.2 outlines the Si_3N_4 deposition and etch process flow; Figure 5.2 (a) Si_3N_4 is PECVD deposited onto the Dip Chip surface (thickness 100 nm). Figure 5.2 (b) 200 nm of Cu (Quorum evaporator) was evaporated onto the Si_3N_4 surface. Figure 5.2 (c) Photolithography (nLOF 2070 protocol) is used to photopattern the "passivation window" onto the Cu layer. Figure 5.2 (d) The Cu was specifically etched using wet etch 1:20 Nitric acid HNO_3 : H_2O_2 diluted 1:5 in di H_2O (BYU Cleanroom 2019) to form Cu etch-mask. Figure 5.2 (e) The photoresist was then removed using a Solvent Clean protocol to reveal the Cu etch-mask. Figure 5.2 (f) RIE Si_3N_4 etch process performed to reveal the graphene channel of the Dip Chip.

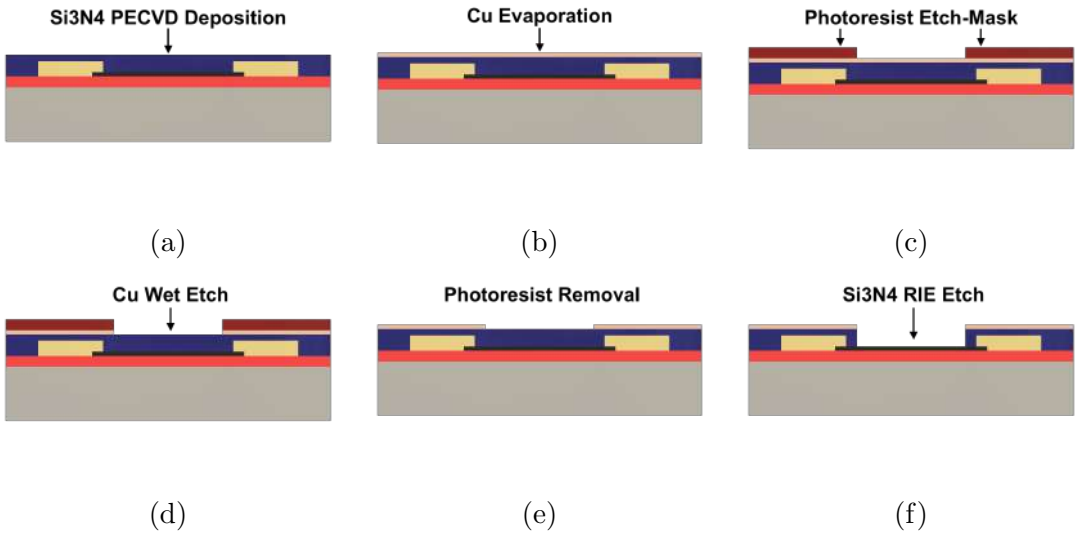


Figure 5.2: PECVD Si_3N_4 passivation process flow.

Silicon Nitride: Low Temperature PECVD

As an alternative approach to the Si_3N_4 deposited at 300 °C, Si_3N_4 can be deposited using the PECVD at lower temperatures (including ambient temperature). This allows for the use of a photoresist Lift-Off process. Figure 5.3 outlines the low temperature Si_3N_4 PECVD deposition and lift-off process flow; Figure 5.3 (a) Lift-off photoresist is patterned onto the Dip Chip surface (specifically the graphene channels). Figure 5.3 (b) Low Temperature PECVD process is used to deposit Si_3N_4 onto the photoresist and Dip Chip surface. Figure 5.3 (c) The sample is submerged in solvent solution to perform photoresist Lift-Off removing the Si_3N_4 selectively from the graphene channel, creating the "passivation window".

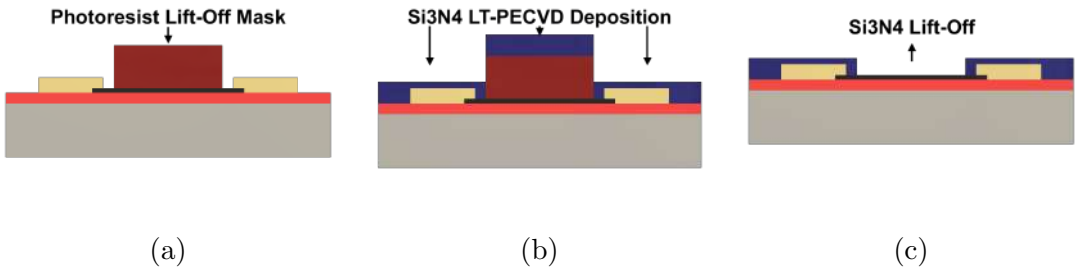


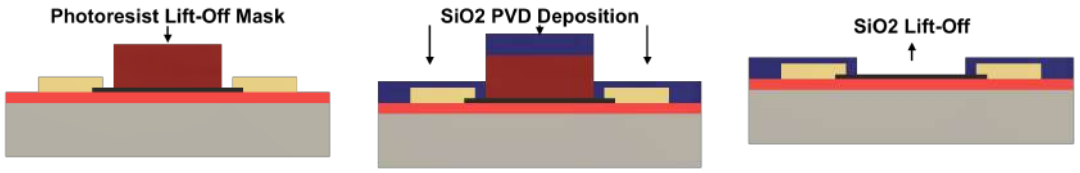
Figure 5.3: Low-Temperature (LT) PECVD Si_3N_4 passivation process flow.

Low-temperature PECVD silicon nitride was deposited using the same parameters for chamber pressure, gas flows and RF generators detailed above. The showerhead, chamber and platen temperature were reduced to set temperatures 35 °C, 80 °C and 100 °C respectively.

To assess the lift-off process used to pattern the nitride layer, photolithography was performed using the "Bi-Layer Protocol", on three plain Si 100 mm diameter wafers. For each of the the test temperatures (5 °C, 80 °C and 100 °C), approximately 100 nm ±2 of Si_3N_4 was deposited. Post deposition a solvent lift-off process using D350 Stripper (MicroChemicals, Germany) for 30 minutes in a bath at 80 °C followed by a second D350 Stripper bath for 30 minutes at 80 °C. The wafers were rinsed using two di H_2O baths.

Silicon Dioxide: PVD

SiO_2 can be deposited using physical vapour deposition (PVD) tool to fabricate the passivation layer. PVD is a low temperature process compatible with photoresist lift-off (parameters: Materials & Methods Chapter section 3.8.1). Figure 5.4 shows the PVD SiO_2 passivation process; Figure 5.4 (a) Lift-off photoresist is patterned onto the Dip Chip surface (specifically the graphene channels). Figure 5.4 (b) Deposition of SiO_2 using the PVD tool onto the photoresist and Dip Chip surface. Figure 5.4 (c) The sample is submerged in solvent solution to perform photoresist Lift-Off removing the SiO_2 selectively from the graphene channel, creating the "passivation window".



(a) (b) (c)

Figure 5.4: PVD SiO_2 passivation process flow.

Deposition parameters for PVD deposition of SiO_2 were: Chamber pumped down

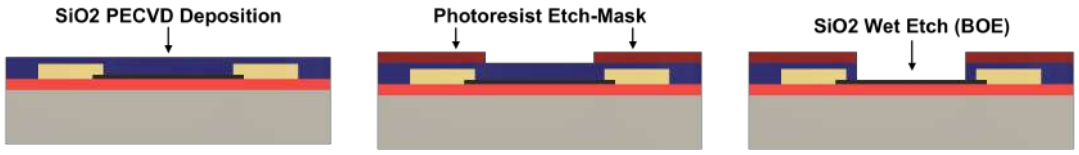
to 10^{-5} mTorr for 1 hour, the RF power is slowly ramped up to 50 W with Ar flow rate 80 sccm.

Passivated chips were tested was performed by Sulphuric Acid 40 % (Sigma Aldrich, UK) submersion to examine the films porosity. Permeation testing was performed on passivated chips diced into 20 x 20 mm squares from plain Si 100 mm diameter wafer, coated with 50 nm of Cu by metal evaporation (Quorum Evaporator, Quorum Technology UK).

Annealing was performed using RTA standard recipe found in Materials & Methods Chapter section 3.4.1. Recipe modified for 150 °C and 300 °C annealing temperatures.

Silicon Dioxide: PECVD

SiO_2 can be deposited at a much faster rate using PECVD deposition tool, The chamber temperature is set at 300 °C so is not compatible with the photoresist lift-off process. To create a passivation layer and passivation window the SiO_2 is deposited and selectively etched. Figure 5.5 shows the PECVD deposition etch process; Figure 5.5 (a) SiO_2 is deposited using PECVD tool onto the Dip Chip surface (thickness 300 nm). Figure 5.5 (b) Photolithography (nLOF 2070 protocol) is used to photo-pattern the "passivation window" onto the SiO_2 surface. Figure 5.5 (c) The SiO_2 passivation film is selectively etched using Buffer oxide wet etch. After etching the photoresist etch mask is removed using a Solvent Clean process.



(a) (b) (c)

Figure 5.5: PECVD SiO_2 passivation process flow.

PECVD deposition parameters for SiO_2 deposition can be found in the Materials

& Methods Chapter section 3.8.2.

The SiO_2 wet etch process used a buffered oxide etch (BOE) a buffered Hydrofluoric acid-based etchant (Microchemcals GmbH Germany) and was performed on photoresist etch masked samples. Photolithography"AZ nLOF 2070" protocol used with passivation window photomask.

An RIE dry etch process was investigated using an optimised SiO_2 etch recipe: 100 sccm flow rate of SF_6 with a flow rate of 4 sccm O_2 at a pressure of 60 mTorr and power of 100 W.

To create a protective layer on the graphene surface the Pre-Transfer yttrium modified process is used during Dip Chip fabrication. The yttrium layer protects the graphene during the SiO_2 deposition and etching processes. Figure 5.6 outlines the SiO_2 passivation process with yttrium protective layer. Process steps are as above with the addition of a final yttrium wet etch step (HCl 0.2 M), removing the yttrium sacrificial layer revealing the graphene surface.

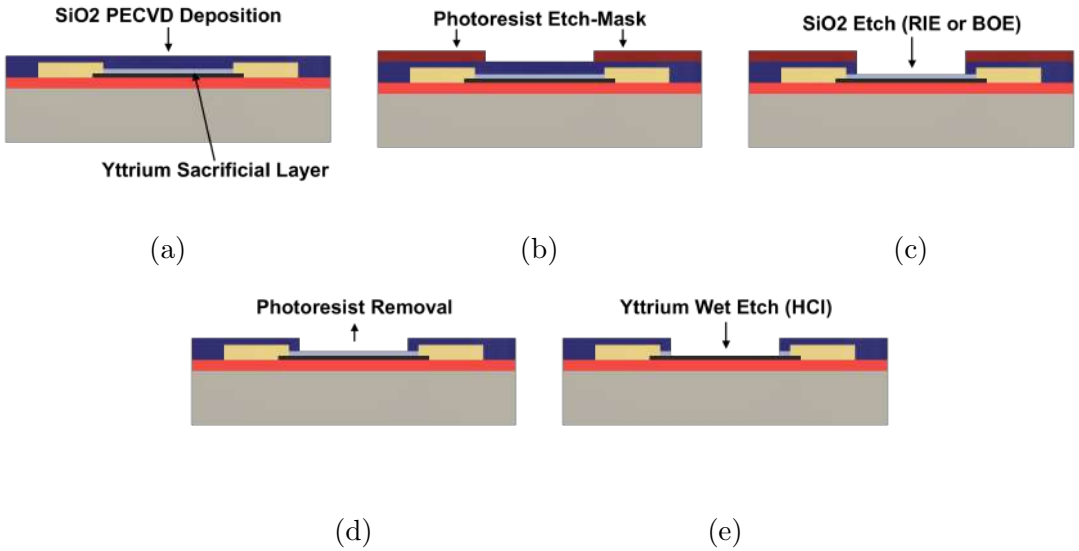


Figure 5.6: PECVD SiO_2 passivation process flow on yttrium sacrificial layer.

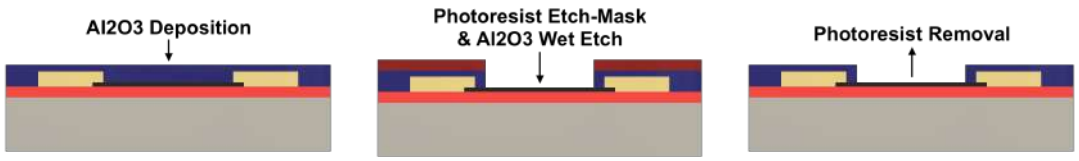
Yttrium evaporation was performed using Quorum evaporator using the process developed in Graphene Sensor Fabrication & Optimisation Chapter section 3.7.2.

Aluminium Oxide: MVD

A Molecular Vapour Deposition (MVD) tool from SPTS Technologies (UK) was used to deposit aluminium oxide (Al_2O_3) passivation layer; using a commercial optimised recipe for Al_2O_3 deposition, with a deposition rate of 0.07 - 0.08 nm/cycle. Each cycle requires 2 precursors (Trimethylaluminium and di H_2O Pegasus Chemicals UK) to be released and evacuated from the chamber sequentially. Each cycle takes approximately 20 s, for a thickness target of 30 nm Al_2O_3 approximately 715 cycles were required with an expected machine run time of approximately 4 hours. This deposition time is much slower than the approximate 38 s for controlled SiO_2 deposition of 100 nm.

During the photolithography process the chemical developer used AZ 726 are Tetramethylammonium hydroxide (TMAH) 2.38 % based developer. AZ TMAH based developers etch aluminium at a rate of 50 - 100 nm/min therefore to etch through the Al_2O_3 the wafer was left in puddle developer for 3 minutes, allowing 1-2 minutes to fully develop the photoresist and an additional 1 minute to etch through the graphene to the graphene channels and metal contact electrodes.

Figure 5.7 shows the MVD Al_2O_3 passivation process flow; Figure 5.7-(a) Al_2O_3 is deposited using the MVD tool onto the Dip Chip surface (50 nm thickness). Figure 5.7-(b) photoresist etch-mask is patterned onto the Al_2O_3 surface, during the photolithography development step the photoresist is developed and Al_2O_3 is etched in the same TMAH developer (AZ 726, MicroChemicals GmbH). Figure 5.7-(c) The photoresist etch-mask is then removed using a Solvent Cleaning process.



(a) (b) (c)

Figure 5.7: MVD Al_2O_3 passivation process flow.

AZ 726 photo-developer (MicroChemicals, Germany) was used as part of standard photolithography "AZ nLOF 2070" protocol found in Materials & Methods Chapter section 3.6.5.

IV Measurements & Resistance Calculation

IV measurements were performed using an IV Probe-station (Everbeing, China) combined with a Keithley 2636B Source Measurement Unit. Details on the measurement script, output file and resistance calculation can be found in the Materials & methods Chapter in section 3.11.1.

Resistance was calculated using the equation R = V / I.

Raman Spectroscopy

The settings for Raman map scans used in this work can be found in Materials & Methods Chapter section 3.12.3.

5.2.2 Results & Discussion

Photoresist & Photo-Active Polymer Passivation Layers

Photoresists and Photo-active polymers were optimised and compared as passivation films to protect the metal contacts/electrodes of the graphene Dip Chip sensor.

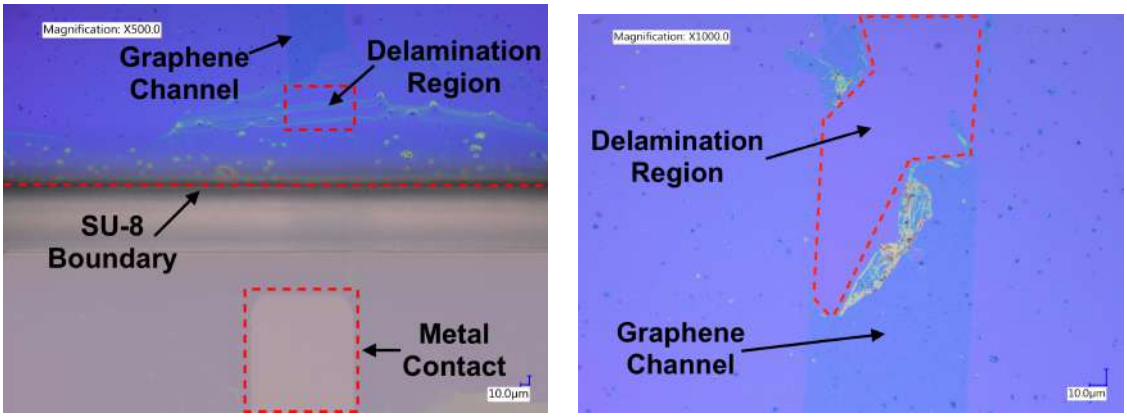
Photoresists can be photo-patterned to an alignment accuracy of 1-2 μm using mask alignment system. Negative photoresist is a single processing step and does not require additional materials or chemical modification to produce the protective layer, this simplifies production for research purposes but is limited in terms of medical device production as a majority of photoresists are not biocompatible. Additionally the use of certain photoresists has been known to leave residue on the graphene surface modifying the graphene's behaviour [7].

When exposed to the UV light, the negative photoresist becomes cross-linked/polymerized, and more difficult to dissolve in developer. The negative photoresist remains on the

surface of the substrate where it has been exposed and the developer solution removes only the unexposed areas.

SU-8 Photoresist SU-8 2025 (Micro Chem Corp.) originally developed as a masking photoresist but now predominantly used for microfluidics soft lithography. SU-8 cross-linking process can be set off by a single photon reaction therefore, SU-8 is know as a chemically amplified resist which is polymerized by photoacid generation. The UV light interacts with the salt in the solution creating hexafluoroantimonic acid which then protonates the epoxide groups in the resin monomer. The crosslinking of the monomers begin at this stage but will not significantly start to polymerize post exposure bake which raises the temperature and energy of monomers allowing them to fully crosslink.

A test process was run on 8 Dip Chips on a single quarter wafer piece to assess the effect of the photoresist on the graphene resistance measurements. Under optical microscopy, the graphene channels were seen to be damaged / sections of graphene had delaminated off the surface see Figure 5.8. No devices had an IV response so no post passivation resistance measurements could be taken.



(a) (b)

Figure 5.8: (a) Shows a Dip Chip graphene contact electrode with SU-8 passivation film with photo masked passivation window revealing graphene channel on SiO_2 substrate. The graphene channel appears to be damaged / delaminated although close to the at metal contact region appears to still be in contact. (b) Graphene channel region short distance from the edge of the passivation window shows complete delamination of the graphene and a full break in the channel.

The SU-8 photolithography method was repeated with a further 8 Dip Chips. The Dip Chips were RTA annealed for 10 minutes at 400 °C to improve adhesion of the graphene to the SiO_2 substrate. Figure 5.9 shows the resulting channels appeared to be unbroken with only minor delamination of the graphene.

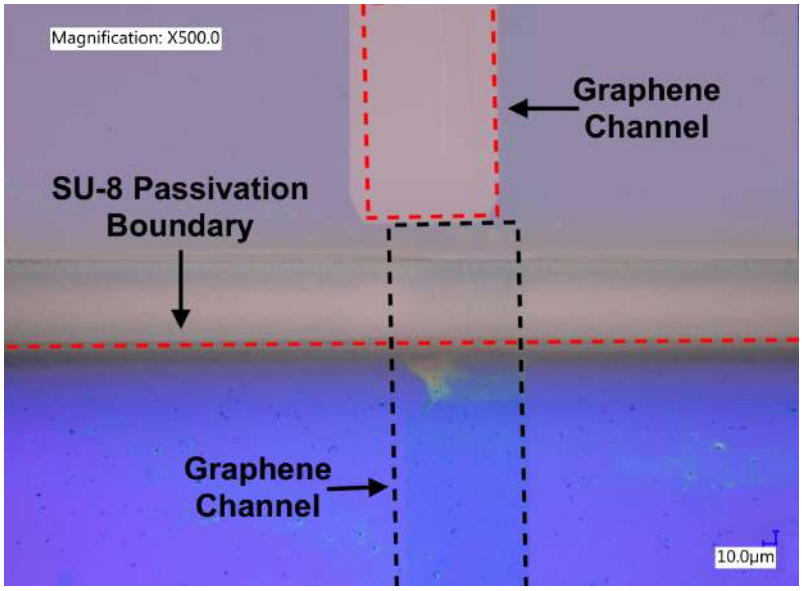


Figure 5.9: Optical Image of SU-8 passivated Dip Chip, graphene channel present after additional annealing step added into fabrication flow.

However, after IV measurements were performed, only 3 of the 16 channels produced a linear response, Table 5.1 shows the pre and post passivation resistance for the 3 working channels the high resistances suggests highly damaged/doped channels.

Table 5.1: Resistance data for Dip Chip graphene channels prior (Pre-Pass) and post SU-8 Passivation (Post-Pass). With the calculated change in resistance.

Dip Chip Graphene	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass	PercentageΔ (%)
Channel 1	8152	26809	+ 229
Channel 2	8335	52347	+ 528
Channel 3	7921	38407	+ 385

This could be due to stress on the graphene during the photolithography development stages. Or the solvent lifting off the graphene and causing damage at the SU-8 graphene boundary. Also during the heating steps of the SU-8 soft and

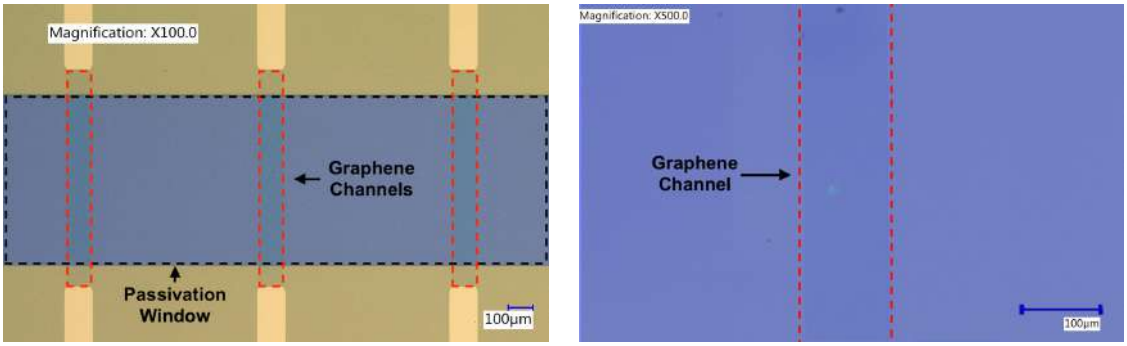
post-exposure bakes the SU-8 contracts and relaxes, this could also be the source of stress on the graphene sheet leading to damage and breaking of the sheet.

AZ nLOF 2070 Photoresist (Hard-baked) AZ photoresists (MicroChemicals GmbH) fall under the categories of positive, negative and multitone photoresists. Negative photoresists are generally more chemically resistant. Once crosslinked they are more durable over longer periods of time and are not broken down with further UV light exposure. nLOF 2070 (abbreviated to nLOF) a negative photoresist normally used for metal lift-off processes by producing an overhang at the photoresist edges. nLOF can be broken down by acetone and other solvents after photolithography (lift-off resist). This makes it less suitable as a film to passivate the graphene devices.

However, a further hardbaking step at temperatures above 150 °C can be done to make the photoresist more permanent. This can not be done on hot plate in atmosphere similar to he soft bake and post exposure bake step as 150 °C or above can cause some oxidation of the graphene layer. Vacuum annealing using the Tube furnace enabled the photoresist to be hard baked in an inert atmosphere.

The nLOF series photoresists have high thermal stability and can withstand hard baking of temperatures up to 250 °C without deformation. The disadvantage to nLOF is its lack of chemical stability although non-reactive to some organic solvents and bases under normal conditions nLOF will fully dissolve in Acetone and partially dissolve in ethanol and is reactive to acids.

A set of 8 Dip Chips were fabricated on a single quarter wafer piece to test the passivation process flow using nLOF. Figure 5.10 shows the geometry of the passivation window patterned onto the graphene Dip Chip.



(a) (b)

Figure 5.10: (a) Full Dip Chip passivation window patterned using nLOF 2070 photoresist. (b) Examination of individual graphene channel shows no photoresist present.

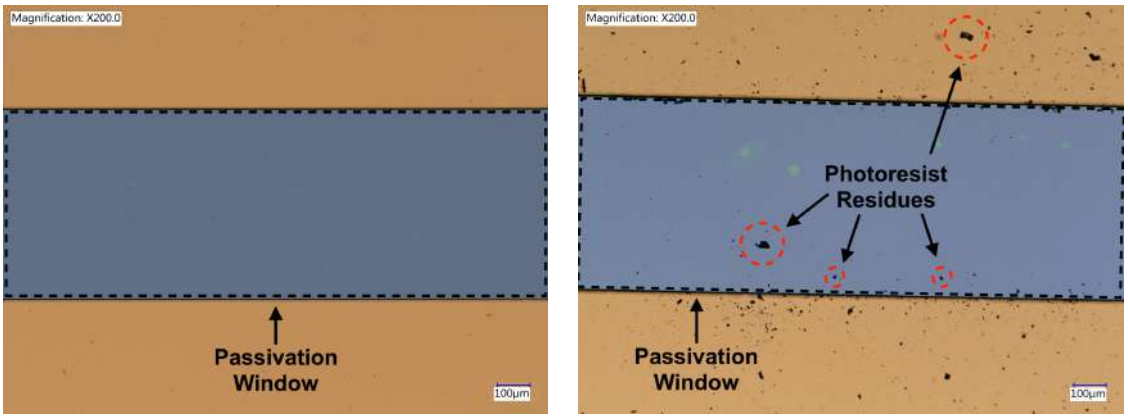
IV measurements were performed on the graphene channels before the passivation step. Following the RTA Hard bake step, the chips were left to cool and stabilise in ambient conditions before a follow-up set of IV measurements were performed to identify the effect of the overlapping passivation film. The effect of photoresist partially covering the graphene surface yields an increase in two-terminal resistance measurements (Table 5.2). The photoresist that overlaps the graphene channel, as well as any residues from the development process, have the effect of depleting the graphene electrostatically reducing the carrier mobility of the graphene. The total area of the graphene channel that is covered with the nLOF passivation film is 30000 μm^2 this is 30 % of the total graphene channel area which caused an average increase in resistance of 13 %.

Table 5.2: Resistance data for Dip Chip graphene channels prior (Pre-Pass) and post nLOF 2070 Passivation (Post-Pass). With the calculated change in resistance.

Dip Chip Graphene	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass	PercentageΔ (%)
16 Channel Average	8279	9371	+ 13.14
Standard Deviation	149	513	+ 4.43

The resulting resistance measurements identified that nLOF increased the device yield from effectively 0 % using the SU-8 passivation method to 100 % yield. This suggests that thermal stability of nLOF is much better than SU-8 and causes less thermal stress on the graphene channel, resulting in functioning channels.

To test the chemical stability of the hard-baked nLOF 2070, blank SiO_2 chips were used to repeat the same photolithography process, including the passivation photomask used for the Dip Chip samples. The resulting film was imaged using Keyence microscope. Figure 5.11 (a) shows clean defined edges and a clean substrate through the passivation window. To replicate a functionalisation environment the chips were submerged in ethanol for a 12 hour incubation period followed by a di H_2O rinse step. The chips were then imaged a second time. Figure 5.11 (b) clearly shows discolouration of the substrate as well as breaking down of the nLOF around the feature edges.



(a) (b)

Figure 5.11: (a) SiO_2 with nLOF 2070 exposed using passivation window mask and hard baked at 250 °C. (b) After 12 hours submersion in ethanol, some residues and fragmentation can be observed on the chip surface.

This method of passivation would suffice for certain research purposes not using solvent-based functionalisation and sensing approaches, but would break down over time. This would never be up-scalable for industrial production due to low chemical stability. Additionally, the biocompatibility issues of the AZ photoresists (Toxic &

Hazardous chemical compounds) would severely limit its biological sensing based applications.

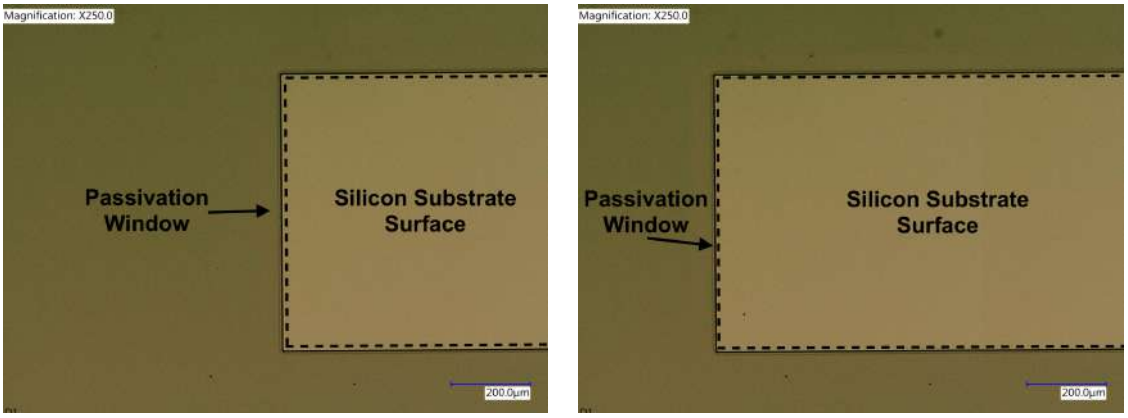
EpoClad 5 The permanent photoresist EpoClad5 part of the the EpoClad EpoCore range of polymeric waveguide resists (MicroResist GmbH). EpoClad is a chemically amplified negative tone photoresist that is developed in organic solvents including acetone. The exposed polymer requires a post exposure bake to enabling cross-linking of the monomer components.

EpoClad designed to be the permanent base layer for optical microfabrication applications has excellent thermal stability within the 100 - 200 °C range. This provides a passivation film that does not expand due to thermal or solvent interactions making it more suitable compared to the AZ nLOF 2070 and SU-8. Hard baking of the photoresist between 120-140 °C improves stability and prevents delamination.

EpoClad and EpoCore are epoxy-based photo-active materials designed for optical waveguides and optical multifunctional biosensor applications. The EpoClad "cladding" resist was designed to adhere well to silica substrates and remain chemically inert post UV curing.

EpoClad also has lower thermal stability compared to nLOF with a glass transition temperature of 180 °C, although this product does not need a hot bake for permanent curing. To compare to nLOF a SiO_2 chip was coated, exposed to UV using the passivation photomask and incubated in ethanol overnight to replicate a solvent functionalisation environment.

Figure 5.12 shows EpoClad pattern on Silicon wafer substrate, no discolouration of the surface and no changes to the EpoClad walls during the incubation step can be seen.



(a) (b)

Figure 5.12: (a) Blank SiO_2 with EpoClad 5 exposed using passivation window mask and developed in Acetone followed by IPA rinse step. (b) After 12 hours submerged in ethanol, no changes were observed for the substrate or passivation layer.

Subsequently, a series of Dip Chips were fabricated and passivated using the EpoClad recipe. A batch of 8 Dip Chips on a single quarter wafer piece were tested. EpoClad, designed for photonics, is transparent and the graphene metal boundary can be observed through the passivation layer. Figure 5.13 shows all channels optically appeared unbroken with minimal delamination.

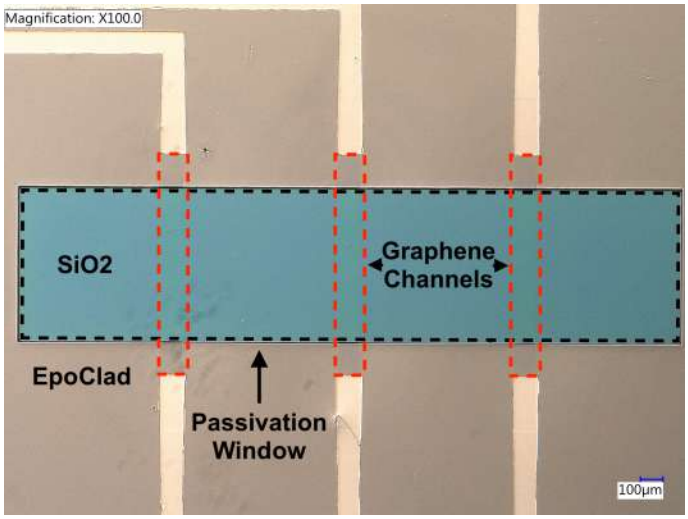


Figure 5.13: Optical microscope image of Dip Chip Origin 3 graphene channels with EpoClad passivation window.

Before passivation, IV measurements were performed on the channels before and after the EpoClad passivation process (followed by a drying/stabilisation period of 12 hours). Table 5.3 shows the calculated resistance data for pre and post passivated Dip Chips. The resistance increase seemed greater than that of the nLOF passivation method, although the standard deviation across multiple devices was also increased compared to nLOF. The device yield was also high from pre to post passivation staying at 100 %.

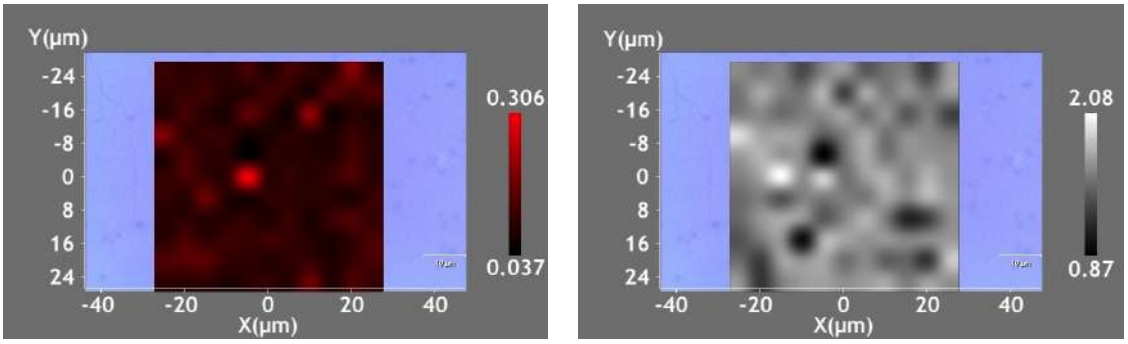
Table 5.3: Resistance data for Dip Chip graphene channels prior (Pre-Pass) and post EpoClad Passivation (Post-Pass). With the calculated change in resistance.

Dip Chip Graphene	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass	PercentageΔ (%)
16 Channel Average	7858	11972	+ 52.35
Standard Deviation	1205	1917	+ 59

The reason for the greater increase in resistance could be due to batch to batch graphene variability. The photoresist epoxy structure could have a stronger charge scattering effect on the graphene surface. However, with its high chemical stability, this permanent photoresist is the most effective passivation based polymer trialled.

To investigate the effect of the passivation processing and identify potential residues on the graphene Raman spectroscopy was performed on graphene the exposed graphene within the passivation window.

Figure 5.14 shows Raman map scans showing the D/G ratio and 2D/G ratio of EpoClad passivated graphene. The average D/G ratio was calculated as 0.1091 ±0.0321 which is not significantly different to blank unprocessed graphene 0.1146 ±0.0188, this suggests a lack of structural damage to the graphene surface. The average 2D/G ratio was calculated as 1.5832 ±0.2086 this is an increase when compared to the blank graphene 1.129 ±0.2004. When the ratio is calculated as 2 or greater this indicates monolayer graphene. Change of this peak can be due to contamination and can be caused by electro or hole-doping of the graphene surface.



(a) (b)

Figure 5.14: Raman map scan 50 x 50 μm of EpoClad passivated graphene, (a) D/G ratio map. (b) 2D/G ratio map.

This could have occurred due to the EpoClad contact with the graphene or the baking steps involved in the photolithography process [8]. The 2D peak in both samples does not have a ratio of 2 suggesting hole doping from the anneal step. The higher peak for the EpoClad sample suggests a different doping profile to the blank sample, this could be due to time spent in ambient conditions or the epoxy/resist in previously in contact with the surface.

Figure 5.15 shows a comparison of the spectra of annealed graphene with solvent cleaning compared to graphene inside the EpoClad passivation window.

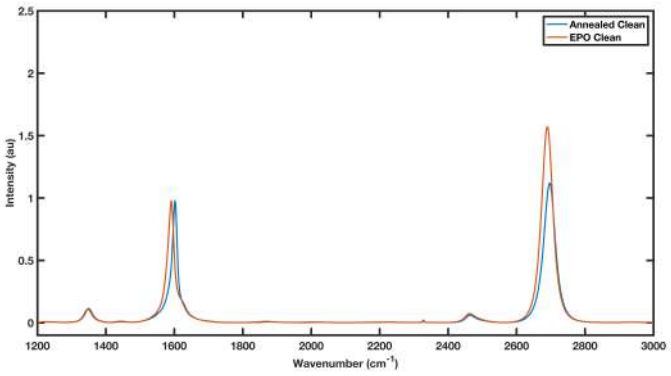


Figure 5.15: Normalised Raman Spectrum's of annealed clean graphene layer and graphene from EpoClad passivated sample.

The EpoClad passivated sample appears to be shifted to a lower wavelength,

with a slight broadening of the peaks. This would suggest a slightly higher level of contamination introducing some defects into the graphene. However, this widening could just be a result of the peak shifting [9].

A doping against strain scatter plot was used to investigate the changes seen in the 2D peak. Figure shows the strain/doping scatter plot derived from the Raman map scan showing an increase in applied strain to the graphene surface.

The Dirac Point measurement pre and post passivation of the graphene channel with EpoClad was also obtained using gated FET measurements. Figure 5.16 shows a slight shift and height change. This was expected with an epoxy photoresist being in permanent contact with a 30 % surface area of the channel. Additionally, photoresist residues on the main body of the channel could have charge scattering effect on the graphene channel reducing the carrier concentration.

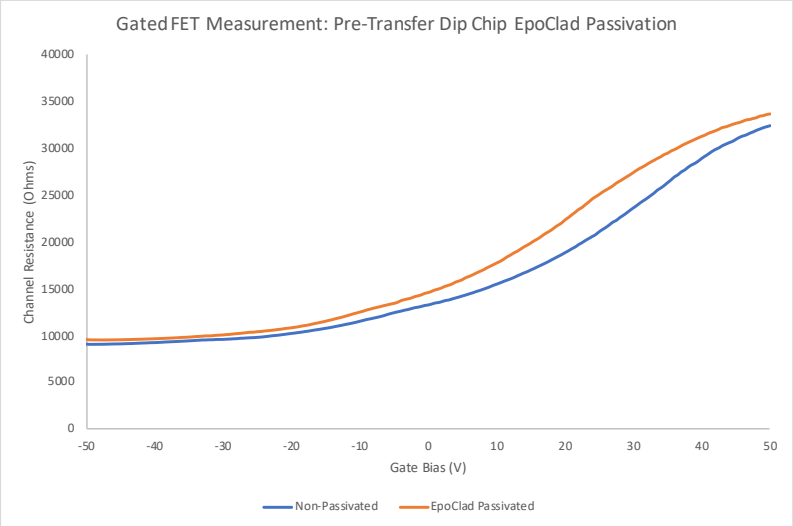


Figure 5.16: Gated FET Dirac point measurement of Pre-Transfer processed Dip Chip before and after EpoClad passivation process.

Graphene Sensor Passivating Films: Dielectric Materials

In the integrated circuits industry dielectric layers are deposited as various Gate, Interlayer and DRAM (dynamic random access memory) insulating layers. Dielectric layers for gate applications have primarily been SiO_2 based. Other methods of

producing gate dielectrics include addition of Nitrogen at the boundary layer and more recently the use of metal oxides with high κ that can be produced in thin film depositions. Interlayer dielectrics traditionally require low κ characteristics to avoid capacitive couple and cross talk between the conductive layers. This enables devices to be built up a of multiple with metal tacks passing over each other in 3D space. This allows for increasing more and more dense components per chip.

For the purpose of passivating the metal tracks on the Dip Chip devices either a low κ dielectric or a high κ dielectric can be used. The primary reason to prevent functionalisation chemistries from binding and a secondly to avoid measuring changes occurring at the metal surface can be achieved with either.

Silicon Nitride: PECVD

Unlike photo-active polymers, dielectric deposited films cannot be patterned directly. A photoresist process is required in order to pattern the dielectric layer. For high-temperature Si_3N_4 deposited films a patterned etch mask approach was taken. The film was directly deposited onto the Dip Chip and the passivation window was then etched into the Si_3N_4 material, following photoresist patterning. This window exposes only the graphene channel.

A plasma enhanced chemical vapour deposition (PECVD) system (SPTS UK) was used to deposit low-stress Si_3N_4 films at a deposition rate of 100 nm per minute. This deposition rate allows for rapid processing in industrial settings. Silicon Nitride is a low κ dielectric and often used for interlayer passivation [10]. With both PECVD deposition Nitride and Silicon Dioxide the deposition platen temperature of 300 °C prevents the use of a photoresist lift-off process. With this high deposition temperature, the only approach is to directly deposit the Nitride onto the graphene surface. This process is followed by photolithography patterning of a photoresist etch mask on top of the Si_3N_4 surface. The plasma mixtures required to etch the nitride selectively (CF_4/H_2, $CF_4/O_2/N_2$, $SF_6/O_2/N_2$, $SF_6/CH_4/N_2$ and $SF_6/CH_4/N_2/O_2$ [11]) were not available on our RIE system. The etch recipe chosen lacked N_2 carrier gas present in the literature recipe.

A nitride etch series was performed on PECVD deposited Si_3N_4 film (110 nm MSE 1.05) to determine an approximate etch rate. RIE etches were performed for 1 minute followed by Ellipsometer film thickness measurement. Table 5.4 shows the new thickness measurement of the deposited film and calculated etch rate. The etch rate was determined as 1 nm/min, this can be used to estimate total etch time (111 minutes) required to etch through the full thickness to open the passivation window.

Table 5.4: RIE etch series for PECVD deposited silicon nitride film

Etch Time (minutes)	Thickness Measured (nm)	Etch Rate (nm/minute)
1	109	1
2	108.2	0.9
3	107.3	0.89
4	105.45	1.14
5	104.7	1.06

The etch time of 111 minutes was performed on 8 Dip Chips using a Cu etch-mask. The etch resulted in etching the graphene channels and SiO_2 substrate beneath.

The etch gases involved etched the base SiO_2 substrate much faster than the Si_3N_4. Even using a graphene protection layer (e.g. Ni, Y or Al), under etching of the SiO_2 would etch the graphene and causing damage.

This process flow was assessed to be impracticable with current tool sets. The Si_3N_4 etch process needs a greater level of control/feedback system to be applied as a graphene passivation method.

Low Temperature Silicon Nitride Deposition

Using a low-temperature PECVD environment for Si_3N_4 deposition enables the use of a photoresist lift-off mask, which can be patterned directly on the Dip Chip surface. This allows a lift-off technique to be used instead of having to etch through the

passivation window. Reducing the chamber platen and shower head temperatures in the PECVD system, reduced the deposition rate to a rate of 5 - 6 minutes per 100 nm.

Figure 5.17 shows the resulting lift-off optical images, the only deposition temperature that resulted in photoresist lift-off was 35 °C as the higher temperatures appear to damage the photoresist below.

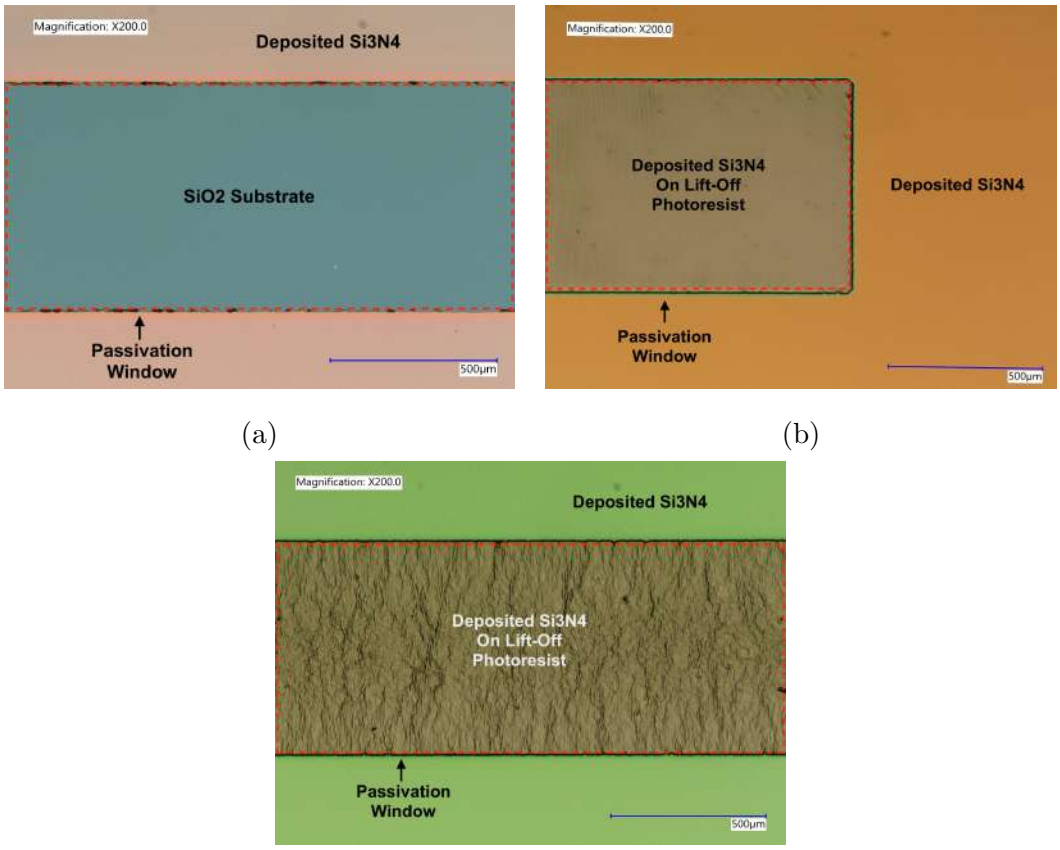
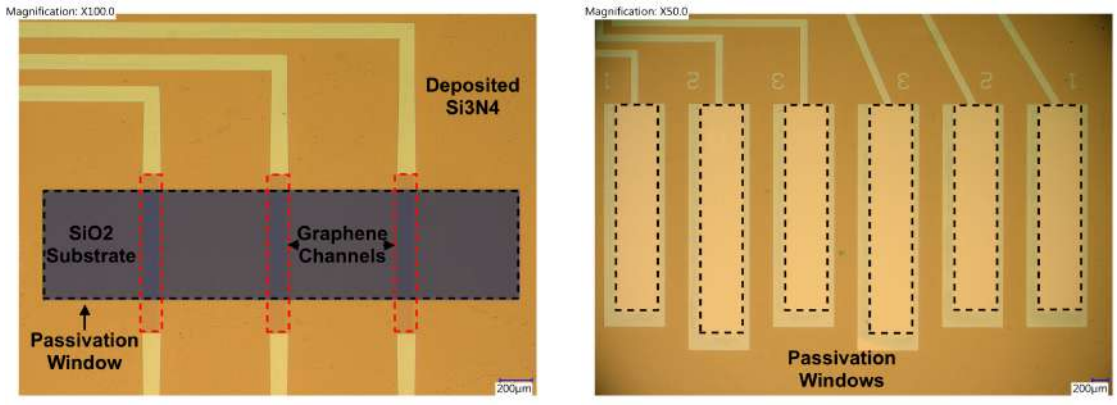


Figure 5.17: (a) Successful Si_3N_4 lift-off process, revealing SiO_2/Si substrate below, (35 °C Si_3N_4 PECVD deposition temperature). (b) Un-successful Si_3N_4 lift-off process, the photoresist remains under the deposited Si_3N_4, (80 °C Si_3N_4 PECVD deposition temperature). (c) Un-successful Si_3N_4 lift-off process, the photoresist remains under the deposited Si_3N_4, (100 °C Si_3N_4 PECVD deposition temperature).

Although the photoresist has good thermal stability above 100 °C, the photore-

sist could have been plasma hardened due to the process gases generated plasma in the chamber [12]. The 80 °C and 100 °C samples were left overnight in solvent bath D350 and both samples did yield complete photoresist lift-off, (slow permeation/penetration of the hardened photoresist).

Using the Si_3N_4 deposition temperature of 35 °C and lift-off process was then tested using graphene Dip Chips. A batch of 8 Dip Chips using a quarter wafer piece was fabricated using the Pre-Transfer process, IV measurements were performed before the passivation process. The photoresist lift-off pattern and deposition parameters for the 35 °C silicon nitride film measured previously at 98.46 nm thickness (5 minute 16 s deposition time), were used to deposited nitride onto the Dip Chip sample that had been placed onto a carrier wafer for transport into the PECVD chamber. The lift-off process was performed using two 30-minute submersions in solvent D350 at 80 °C. Figure 5.18 shows the resulting graphene channels examined optically to inspect for delamination and breaking points. No breakage or delamination was observed across the graphene Dip Chip devices. All channels were then measured using IV probe station the calculated resistances were then compared to the IV results from before the passivation process.



(a) (b)

Figure 5.18: Low temperature silicon nitride PECVD deposition onto Dip Chip devices using bi layer photoresist lift-off process. (a) opened passivation window to graphene channels. (b) window opened to metal contact electrodes.

Table 5.5 shows an increase in resistance. This could be due to the doping effect of silicon nitride but more likely due to structural damage sustained to the graphene from the highly reactive plasma during the PECVD deposition process. The total yield with a linear response was 96 % with repeats and further lift-off optimisation the total yield could be increased further.

Table 5.5: Resistance data for Dip Chip graphene channels prior (Pre-Pass) and post low temperature silicon nitride Passivation (Post-Pass). With the calculated change in resistance.

Dip Chip Graphene	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass	PercentageΔ (%)
16 Channel Average	10112	12092	+ 19.81
Standard Deviation	1438	1585	+ 4.42

Figure 5.19 shows partial delamination of the silicon nitride, visible after the samples were immersed in and withdrawn from cleaning solutions. This could be due to low substrate adhesion or reduced temperature during Si_{34} deposition. The mechanism of lifting off the film could also apply stress to the film at the edges of the passivation. To improve this method further, substrate adhesion would need to be investigated further, this is an added complication as surface treatments would bind to the graphene channel in addition to the SiO_2 substrate. The nature of the silicon nitride deposition does not lend itself to a lift-off process for an industry-based process. A silicon nitride etch would be more practical and produce and more accurate passivation geometry when scaling down the window size when miniaturising the graphene channels.

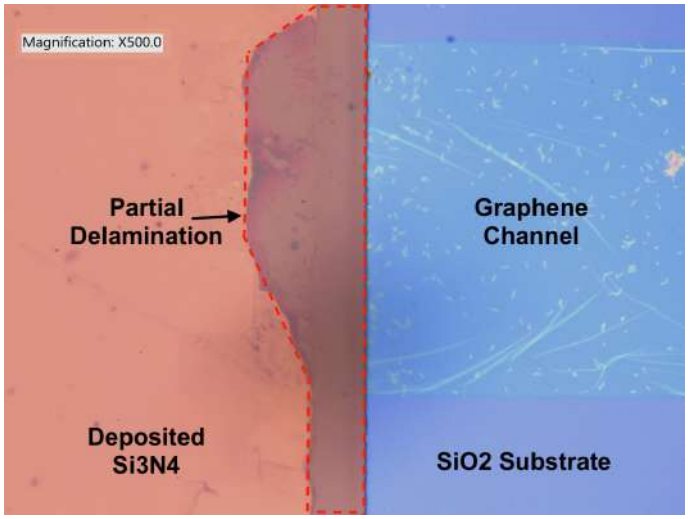


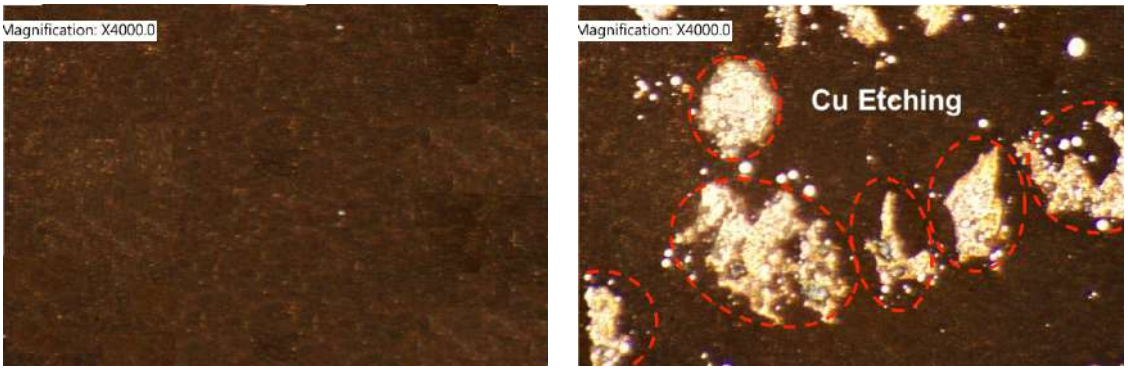
Figure 5.19: Low temperature silicon nitride lift-off after submersion in water. discolouration of liquid under passivation layer at contact edges.

Silicon Dioxide: PVD

An initial investigation into the use of PVD deposited dielectric films for a lift-off passivation approach was investigated. Due to the amorphous nature of films deposited using PVD, films are routinely annealed at high temperature to form a crystal structure. For dielectrics such as SiO_2 the required annealing temperature is in the range of 400 - 1000 °C [13]. However, higher annealing temperatures in the 400 °C or above range have been shown to change the doping and strain on the graphene surface. Temperatures above 600 °C result in damage to the graphene metal contact region [14].

Dielectric deposition by PVD systems has slower deposition rates than standard conductive targets. A deposition rate of 0.01 - 0.02 nm per second was. To test the porosity of the deposited SiO_2 films annealing at in a range of 100 - 300 °C, copper was deposited on 20 x 20 mm Silicon wafer pieces before the deposition of SiO_2 50 nm by RF sputtering. These pieces were annealed at different temperatures for 10 minutes using the RTA system. Sample 1 was not annealed, Sample 2 was annealed at 150 °C and Sample 3 was annealed at 300 °C. The samples were then submerged in H_2SO_4 to test the liquid porosity of the deposited films.

Samples 1 and 2 reacted strongly with the H_2SO_4 effervescing within 30 s of submersion in the solution. Sample 3 did not appear to react with the H_2SO_4 solution. Figure 5.20 shows sample 3 under magnification, the sample shows discolouration in patches across the surface, these patches represent regions of copper partially etched through SiO_2 film. This suggests the films are porous and would not make an effective passivation layer to protect the electrodes from acid-based functionalisation chemistries.



(a) (b)

Figure 5.20: (a) PVD deposited SiO_2 50 nm film onto PVD deposited Cu 10 nm. Annealed in RTA 300 °C for 10 minutes. (b) Sample submersed in 0.25 M for 2 hours and rinsed in di H_2O. Bright regions represent copper etched regions and porous regions of the SiO_2 film

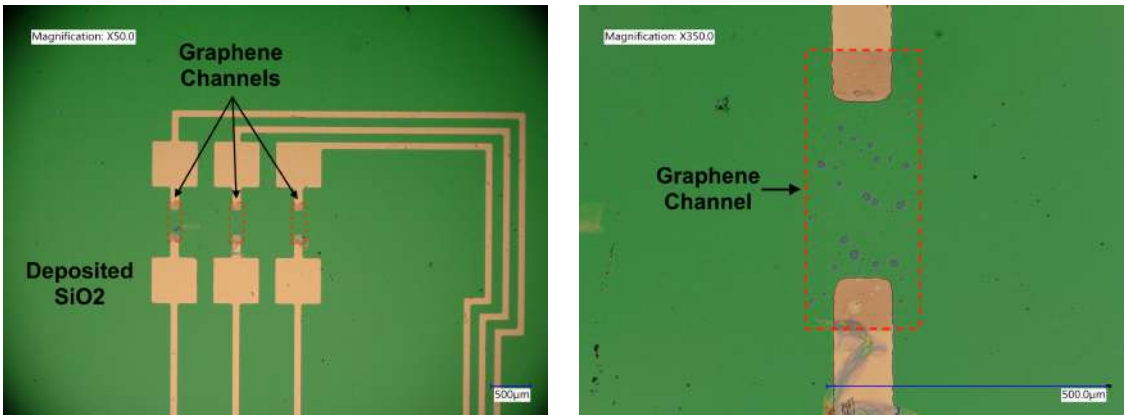
Silicon Dioxide: PECVD

The PECVD (SPTS, UK) can deposit SiO_2 at rate of up to 1 μm per minute. This allows for rapid deposition of micron thick SiO_2. Rather than focusing on a low-temperature deposition solution a direct deposition followed by a SiO_2 etch process was investigated.

The etch rate for BOE on SiO_2 and quartz is 2 nm/s (Brigham Young University Cleanroom resources). The approximate etch time for a 100 nm thick SiO_2 film would be 50 s based on aforementioned etch rate. A 100 nm PECVD SiO_2 film was deposited on plain silicon wafer cleaved into pieces. An etch series of 30 s,

35 s, 40 s, 45 s, 50 s and 55 s in BOE followed by di water rinse steps. The remaining thickness of SiO_2 was measured using ellipsometry. Post 40 s there was no measurable thickness of SiO_2 remaining, with 9 nm remaining after 35 s. A target etch time of 38 - 40 s was repeated and successfully etched the complete 100 nm film.

PECVD deposited SiO_2 using the 300 °C chamber temperature and etching the passivation window requires the SiO_2 to be deposited directly onto the surface of Dip Chip. A batch of 8 Dip Chips were fabricated on a quarter wafer piece, IV measurements were taken for each of the graphene channels. A 100 nm SiO_2 film was then deposited onto the Dip Chips directly coating the graphene channels. Post deposition the graphene was barely visible through the SiO_2 passivation layer, some discolouration of the surface appeared around the graphene region see Figure 5.21. This could be organic contaminants/photoresist residues reacting with the chamber vapour reactants. Or this could be chemical reactions of the chamber gases reacting with the graphene surface.



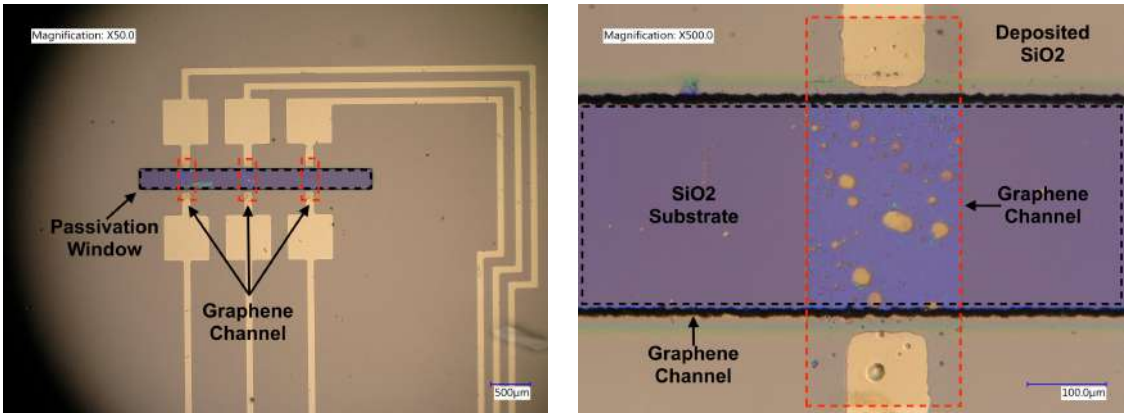
(a) (b)

Figure 5.21: (a) Graphene channels of Dip Chip coated with 100 nm PECVD SiO_2 film deposited at 300 °C. (b) Examination of channel 1 shows discolouration of regions, trapped bubbles of contamination.

To assess whether the graphene has high conductivity post PECVD deposition, separately to post BOE etch, the Dip Chips were photo patterned with the pas-

sivation window etch mask, followed by etching the metal electrode window using a BOE oxide 38 s etch process without etching the graphene passivation window. This allowed for IV measurements to be made on the graphene channels whilst still encapsulated with the SiO_2.

The passivation window was then etched using the BOE 38 s second etch to open the graphene channels to atmosphere (Figure 5.22). The channels were then measured again using the IV probe station after the BOE etch.



(a) (b)

Figure 5.22: (a) Photoresist etch mask on direct PECVD deposited SiO_2, after 38 s BOE etch process. (b) Discolouration circular spots on graphene surface remain after BOE etch of SiO_2, the discoloured regions increase in size post etch.

Some graphene channels were unable to produce a response during IV measurements this suggests the graphene channels were too damaged structurally or chemically to create an electrical circuit. The major change occurred post-deposition whereby channels still produced a linear response. However, the resistance increase was so high (initial range 5-8 kΩ, after deposition 60 - 250 kΩ) that effectively the graphene SP^2 structure was no longer present. This suggests the direct PECVD deposition of silicon dioxide onto graphene should be avoided during the fabrication process flow, as it causes high resistances and variation.

Based on the previous work using yttrium as a sacrificial layer to improve device yields and reduce contamination residues, the yttrium sacrificial layer could also act

as a protective layer during PECVD deposition of SiO_2. The use of a sacrificial layer to protect the graphene during the etch phase would also open up the possibility of a dry etch process to remove the oxide layer This would result in more control of the etch and reduce potential undercut.

A 100 nm film ± 3 nm of SiO_2 was deposited using PECVD on a plain Si wafer. Then cleaved into quarter wafer pieces. An etch series of 210 - 240 s was performed, the 100 nm film was fully etched in 220 s (based on ellipsometry measurements).

To assess he efficiency of using the yttrium sacrificial layer in the fabrication process, a batch of 8 Dip Chips were fabricated using the Yttrium modified top contact process, up to the process step before the final HCl etch (used to remove the Yttrium from the exposed region of the graphene channel). The wafer was then moved into the PECVD using a carrier 100 mm wafer and a 100 nm film ± 3 nm of SiO_2 was deposited.

The 8 Dip Chips were prepared with a photoresist etch mask in order to selectively etch the passivation window. The PECVD SiO_2 was then etched using the 220 s RIE etch. The Yttrium was then removed using dilute HCl etch to reveal the graphene channel both of these steps can be seen in Figure 5.23. The optical images show no signs of damage to the graphene channel.

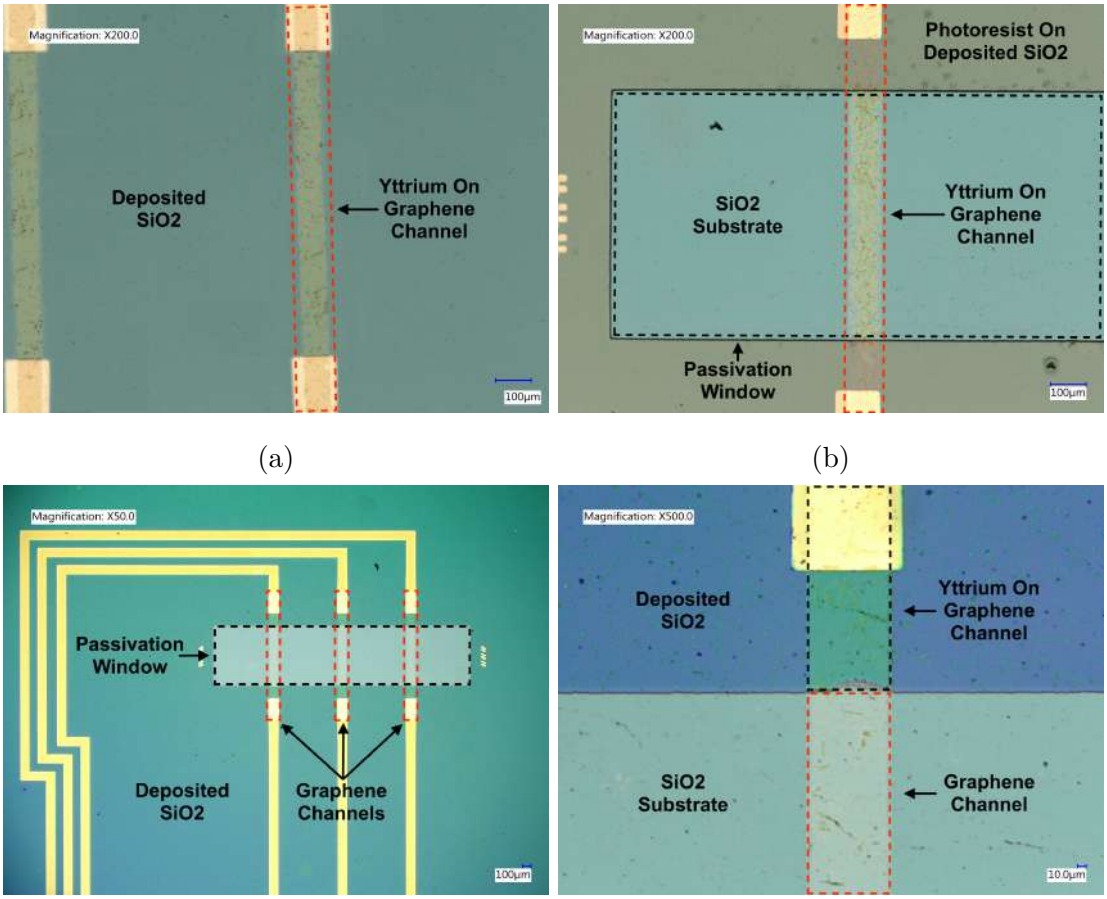


Figure 5.23: (a) Graphene channel with Yttrium sacrificial layer fabricated using the modified top contact process. (b) Graphene channel with yttrium sacrificial layer present post PECVD deposition and RIE etch of SiO_2 (photoresist etch mask still present). (c) Dip Chip, post HCl etching to remove yttrium sacrificial layer. (d) Examination of graphene channel reveals no delamination or regions of intense damage, slight under etch of graphene edges shown by discolouration.

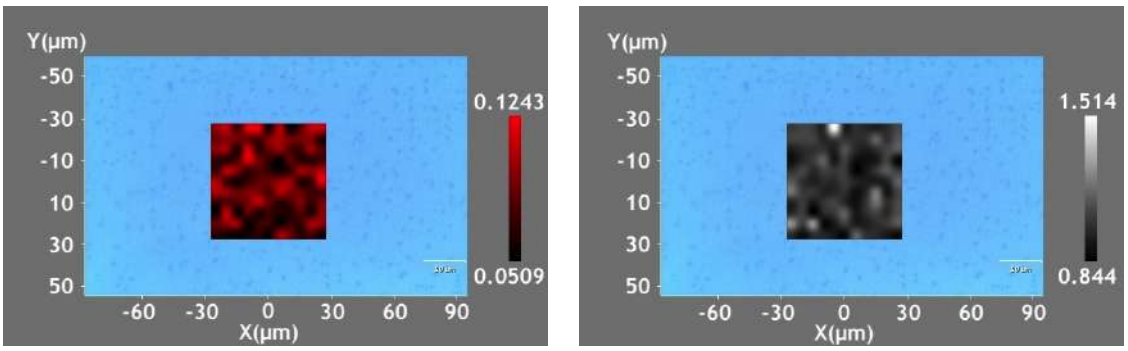
IV measurements of the graphene channels were performed before the PECVD SiO_2 passivation process. This data was not representative of the finished device as the yttrium sacrificial layer was still present, reducing the channel resistance. So in comparison, the average resistances from the previous 4 sets of Dip Chips fabrications were compared to the averages post passivation and Yttrium removal. Table 5.6 shows that the resulting resistance measurements of the Dip Chips are

within 20 % of the previously averaged data. This increase could be down to some Yttrium forming carbides with the graphene at the 300 °C temperature within the PECVD chamber.

Table 5.6: Resistance data for an average Pre-Transfer Dip Chip graphene channels, Dip Chip with Sacrificial Yttrium Layer prior (Pre-Pass) to SiO_2 passivation and post passivation followed by Yttrium Etch (Post-Pass).

	Averaged Pre-Passivation Resistance From Previous Processes (Ω)	Post-Passivation and Yttrium Removed Resistance (Ω)
16 Channel Average	8599	10436
Standard Deviation	1420	1466

To investigate whether there is any damage occurring to the graphene during the plasma etch process the graphene channels were analysed using Raman spectroscopy (Figure 5.24).



(a) (b)

Figure 5.24: Raman map scan 50 x 50 μm of Yttrium SiO_2 RIE etched followed by HCl Yttrium etched graphene, (a) D/G ratio map. (b) 2D/G ratio map.

Raman map scans looking at the D/G ratio and 2D/G ratio. The average D/G ratio of the RIE etched sample was calculated as 0.0818 ±0.0159 with an average 2D/G ratio of 0.9684 ±0.0727 these figures were compared to Pre-Transfer Yttrium

processed non-passivated samples where the average D/G ratio was calculated as 0.991 ±0.0446 and average 2D/G ratio calculated as 0.9569 ±0.1254. The passivation process does not appear to introduce any additional damage to the SP^2 bonding structure of the graphene seen in the D/G ratio. There is also no difference in the 2D/G ratio suggesting no changes to doping or strain applied to the graphene.

Figures 5.25 shows the similarities between the normalised spectra of the SiO_2 passivated graphene compared to the non-passivated graphene (both using Yttrium sacrificial layer). There is no real shift in the spectra or major changes in peak intensities. This suggests that the use of Yttrium as a sacrificial etch mask is effective at protecting the graphene sheet from both the PECVD deposition and RIE etch process. This means the graphene Dip Chip can be effectively passivated using PECVD deposited SiO_2, an inert and chemically resistive film. Without causing damage or introducing residues to the graphene surface.

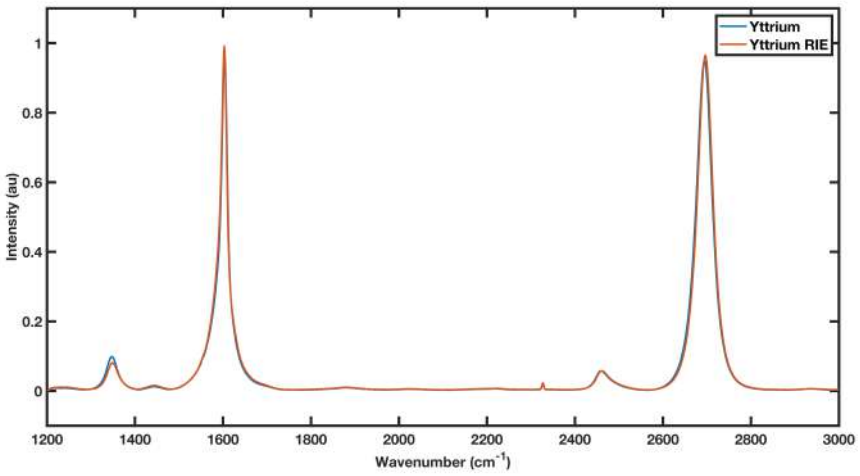


Figure 5.25: Normalised Raman Spectrum's of Yttrium SiO_2 RIE etched followed by HCl Yttrium etched graphene layer and Yttrium by HCl Yttrium etched graphene.

SiO_2 PECVD Deposited With Si_3N_4 Substrate During the SiO_2 etch process once the deposited SiO_2 film has been etched, any further etch time using the dry etch RIE process and the wet BOE etch process results in under etching of the graphene (Figure 5.26 a&b). This Introduces of structural damage to the graphene

channel. These effects would become more noticeable during the miniaturisation of this process, when decreasing the graphene channel size.

To improve the device process flow towards miniaturisation, an etch stop was introduced to prevent the under etching. Using a Si_3N_4 coated substrate wafer (University Wafer Inc, USA), to provide an etch-stop and prevent under etching of the graphene channel for both etch methodologies (Figure 5.26 c). The etch rate of Si_3N_4 in BOE less than 1 nm/minute [15].

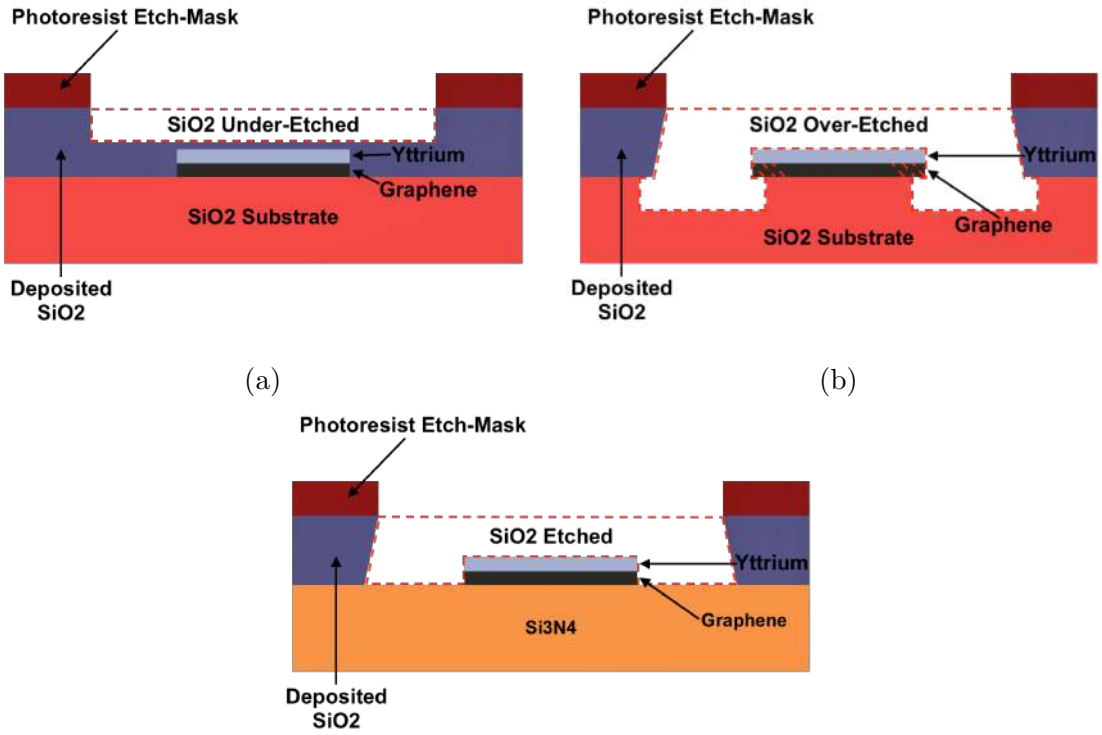
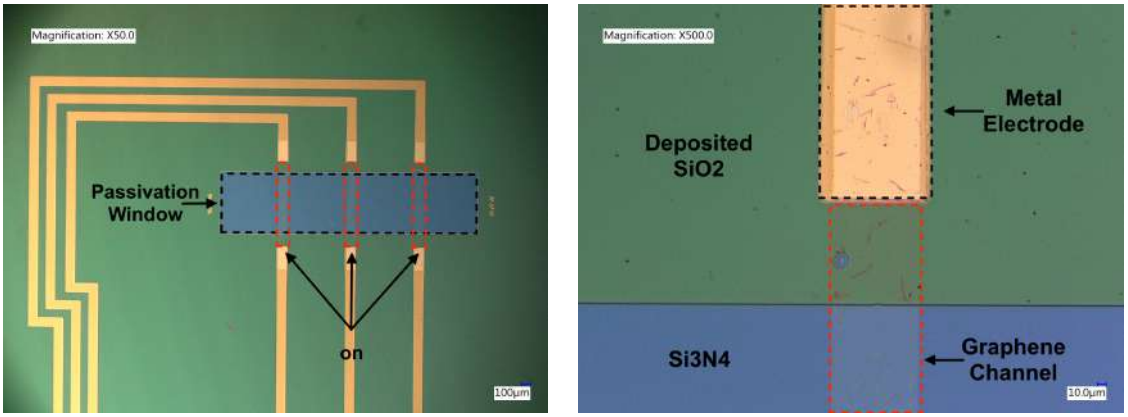


Figure 5.26: (a) PECVD deposited SiO_2 during etching process (under-etched), the yttrium/graphene channel is not fully exposed so cannot be functionalised. (b) PECVD deposited SiO_2 during etching process (over-etched), the substrate SiO_2 is also etched and the graphene channel is damaged. (c) PECVD deposited SiO_2 during etching process, successful etch of deposited SiO_2 to the base substrate (Si_3N_4 etch-stop, exposing the yttrium/graphene channel.

The next stage was to repeat the process of PECVD deposited SiO_2, the RIE

etch using the yttrium sacrificial layer. However, Graphenea does not supply wafer-scale monolayer graphene on silicon nitride wafers. The Post-Transfer fabrication process was used with silicon nitride wafers to fabricate 8 Dip Chips. The yttrium sacrificial layer was introduced after the graphene transfer step. The PECVD SiO_2 passivation process using graphene protected with yttrium was then performed. Figure 5.27 shows the resulting fabricated devices. This method produced a much cleaner device without undercut of the graphene channel due to the Nitride acting as an etch stop.



(a) (b)

Figure 5.27: (a) PECVD deposited SiO_2 on top of graphene devices (using yttrium protective layer) fabricated on silicon nitride wafer. Yttrium sacrificial layer etched using HCl solution. (b) Graphene channels show no signs of delamination or damage with little to no under cut of the graphene channel.

IV measurements were performed on a separate set of un passivated 8 Dip Chip devices fabricated from the bottom contact process on the same silicon nitride wafer to compare to the passivated devices. Table 5.7 shows the calculated resistance data, the average resistance of the Dip Chips appears to increase post-passivation. The standard deviation for the passivated devices also increases. In general the device variability is higher on Nitride based devices. The higher variability and higher resistance values (lower carrier mobility) for the Dip Chips would need to be investigated further, to ascertain whether the benefits fabricating with nitride

substrates is worth developing sensors with higher resistances compared to SiO_2 substrates.

Table 5.7: Resistance data for Dip Chip with Sacrificial Yttrium Layer prior (Pre-Pass) to Si_3N_4 passivation and post passivation followed by Yttrium Etch (Post-Pass).

	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass
16 Channel Average	19664	22048
Standard Deviation	3061	9126

For results presented, using a SiO_2 substrate is suggested to produce the lowest resistance-based devices with low variability. PECVD deposited SiO_2 passivation films would allow for a commercial level process flows and potential further miniaturisation of the graphene channels and die. Thermal metal evaporation is less common in CMOS level fabs but PVD deposited yttrium has causes damage to graphene to a point where the graphene channels conductivity is destroyed. Thus, thermal evaporation or e-beam evaporation of yttrium is required for the yttrium process step.

Aluminium Oxide: MVD

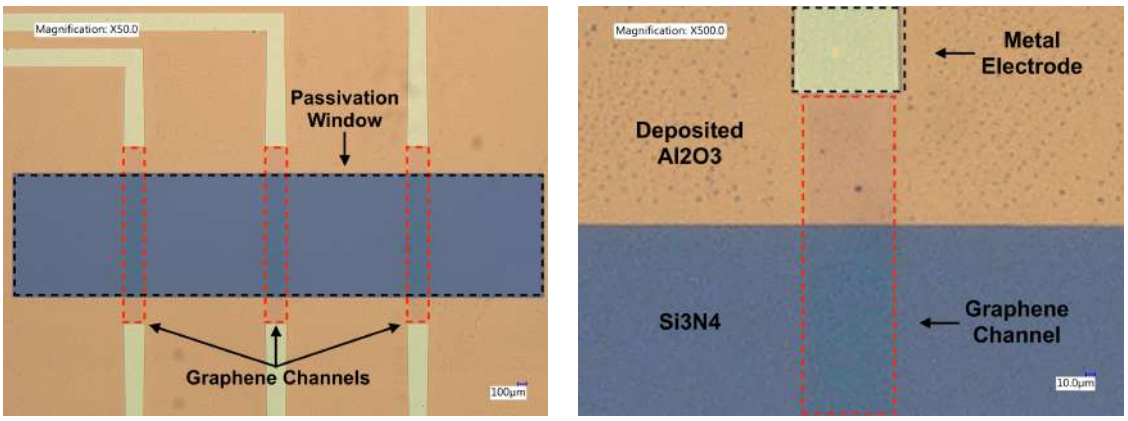
The most common methodology for passivation of graphene devices is the use of aluminium oxide (Al_2O_3), usually deposited via Atomic Layer Deposition (ALD) [16], or via E-beam evaporation sources to minimise graphene damage [17]. Al_3O_2 is chemically resistant to solvents and low concentration acids. Al_2O_3 is etched in strong acids and strong bases. Thus, etching of Al_2O_3 is possible using standard photolithography developers e.g. AZ 726 (TMAH based). MVD deposited Al_2O_3 has a reported stoichiometry of Al/O = 41.0/59.0, at 10 nm a dielectric contant of 9, a breakdown field of 8 MV/cm and a leakage current of 4 x 10^{-9} A/cm^2

To assess the passivation process a set of 8 Dip Chips were fabricated on a quarter

wafer SiO_2 substrate. An MVD film of Al_2O_3 715 cycles was deposited directly onto the exposed graphene channels. As the MVD chamber can process multiple wafers simultaneously a Si control wafer was used to measure the deposited thickness using ellipsometry (50.8 nm recorded).

To etch the deposited Al_2O_3, sequential photolithography and was etched was used. Using an AZ nLOF 2070 photoresist etch mask, the passivation window was etched using AZ 726 developer. Once the soluble photoresist is removed from the window the sample was left in developer for an additional 2 minutes to etch the exposed Al_2O_3, revealing to the graphene layer. The SiO_2 substrate acts as the etch stop preventing under etching of the graphene channel.

This process could be optimised further by using one photoresist developer AZ 400K to remove the soluble photoresist followed by a dilute Trimethylaluminium (TMAH) solution to etch the Al_2O_3. The passivation layer post photolithography etch can be seen in Figure 5.28.



(a) (b)

Figure 5.28: (a) MVD deposited Al_2O_3 passivation window on graphene devices fabricated on SiO_2 wafer. Al_2O_3 was etched during a photolithography development step using AZ 726 developer. (b) Graphene channels show no signs of delamination or damage with little to no under cut of the graphene channel.

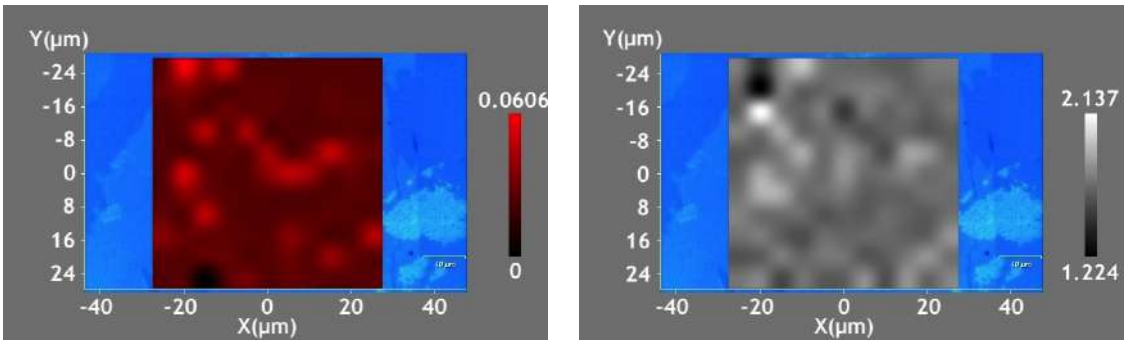
IV measurements were performed before the MVD deposition and can be compared to IV measurements performed post photolithography etch of Al_2O_3.

Table 5.8 shows calculated resistances from the IV measurements. The resistance change seen in devices post passivation saw no significant increase, an increase (doubling) in standard deviation was seen. This suggests the MVD process has no significant effect on the graphene channels in terms of electrical conductivity.

Table 5.8: Resistance data for Dip Chip graphene channels prior (Pre-Pass) and post MVD aluminium oxide passivation (Post-Pass). With the calculated change in resistance.

Dip Chip Graphene	Resistance (Ω) Pre-Pass	Resistance (Ω) Post-Pass	PercentageΔ (%)
16 Channel Average	9978	10053	0.75
Standard Deviation	1564	2331	30.43

Raman spectroscopy was used to identify levels of damage in the graphene structure, comparing pre and post passivation samples. Figure 5.29 shows the graphene map scans looking at the D/G ratio and 2D/ G ratio. The D/G map shows very low levels of damage overall graphene structural uniformity high.



(a) (b)

Figure 5.29: Raman map scan 50 x 50 μm of MVD Al_2O_3 deposited and etched passivated graphene, (a) D/G ratio map. (b) 2D/G ratio map.

Figure 5.30 shows the Raman spectra comparison of pre and post passivation using MVD deposited Al_2O_3. There is no visible shift in the peak positions suggesting low levels of nanoscale-strain/doping.

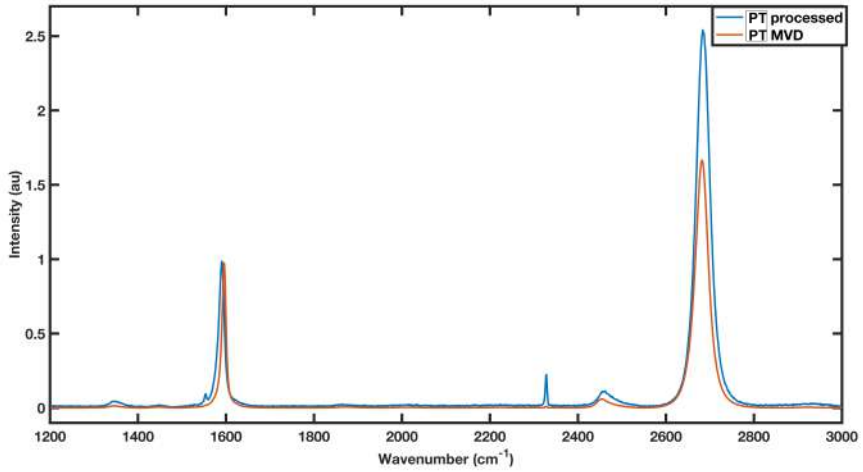


Figure 5.30: Normalised Raman Spectrum's of Post-Transfer process Dip Chip pre and post-passivation using MVD Al_2O_3 passivation process.

Table 5.9 shows the average peak ratios and derived grain size for Post-Transfer fabricated Dip Chips before and after MVD Al_2O_3 passivation. From the D/G ratio and grain size it is clear no damage occurred during the Al_2O_3 deposition or etching process.

Table 5.9: Average peak ratios and calculated grain size for Post-Transfer Dip Chip pre and post MVD aluminium oxide passivation Process.

	I_{2D}/I_G Ratio	I_D/I_G Ratio	Approximate Grain Size (L_a)
Graphene Pre-Passivation	2.5455 ±0.2658	0.0464 ±0.0139	414.3 ±124.11
Graphene Post-Passivation	1.6779 ±0.1222	0.0138 ±0.0077	1393.1 ±777.3

The MVD Al_2O_3 passivated graphene shows a reduction in the damage peak (the lowest seen in all Raman map samples). Similar effects are seen in the literature, ALD Al_2O_3 deposition onto graphene surface can have a "Healing" effect, removing chemical defects to the graphene surface [18]. The decrease in 2D/G ratio would

suggest a doping/strain effect due to either the deposition or the HCl etch step.

Dielectric Passivation Comparison

The two effective dielectric etch methods tested were the PECVD deposited SiO_2 with Yttrium sacrificial layer process and the MVD deposited Al_2O_3. Figure 5.31 shows the comparison of normalised Raman spectra of the Post-Transfer MVD Al_2O_3 passivated graphene compared to Pre-Transfer PECVD SiO_2 Yttrium passivated graphene.

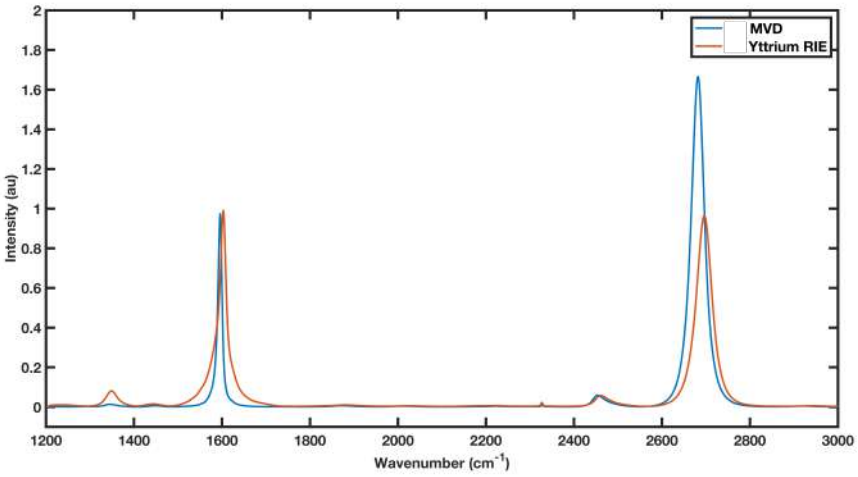


Figure 5.31: Normalised Raman spectra of graphene samples, post-Transfer Dip Chip with MVD Al_2O_3 deposited and etched compared to Pre-Transfer Dip Chip with sacrificial yttrium layer and PECVD SiO_2 deposited and etched.

Table 5.10 shows the average peak ratios and derived grain size for Post-Transfer fabricated Dip Chip MVD Al_2O_3 passivated, and Pre-Transfer fabricated Dip Chip Yttrium PECVD SiO_2 passivated. The total damage (D/G ratio) is substatially lower in the MVD passivated sample a difference of 0.068 (142 %). Additionally the 2D/G ratio is higher for MVD suggesting lower levels of strain/doping. This method of passivation shows the least damage to the graphene structure with the least change in doping as well. The total process steps and machine time costs are also lower when comparing the dielectric passivation methods.

Table 5.10: Average peak ratios and calculated grain size for Post-Transfer Dip Chip with MVD aluminium oxide passivation Process. Compared to Pre-Transfer Yttrium sacrificial layer Dip Chip with PECVD SiO_2 passivation process

	I_{2D}/I_G Ratio	I_D/I_G Ratio	Approximate Grain Size (L_a)
MVD Al_2O_3 Passivation	1.6779 ±0.1222	0.0138 ±0.0077	1393.1 ±777.3
PECVD SiO_2 Passivation	0.9684 ±0.0727	0.0818 ±0.0159	235.0 ±45.7

Dielectric passivation produces the most effective and chemically inert passivation materials. They could also be used as a gate oxide material in a top gate FET based design (Figure 5.32). the two most effective in terms of stable resistance measurements and low structural damage, were (1) the RIE etch of PECVD deposited SiO_2 using an evaporated yttrium sacrificial layer to protect the Pre-Transfer graphene; and (2) the photolithography based etch of MVD deposited Al_2O_3 passivated Post-Transfer graphene.

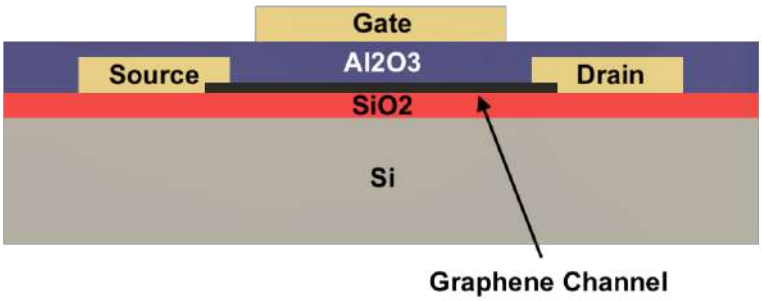
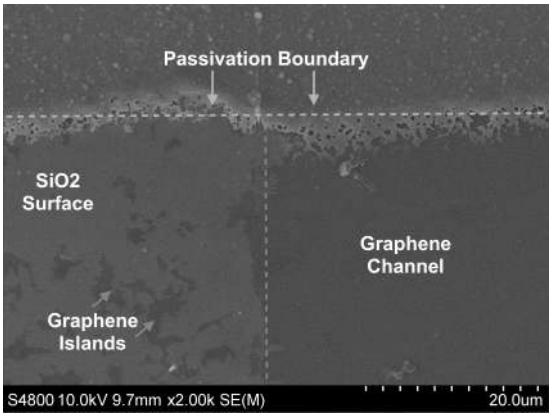


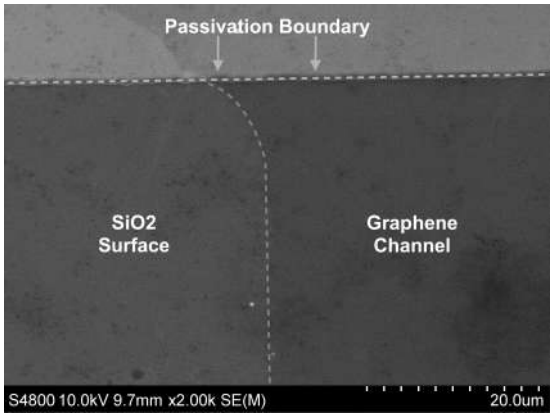
Figure 5.32: Diagram of top gated graphene FET design.

To investigate the graphene surface after these passivation processes further,

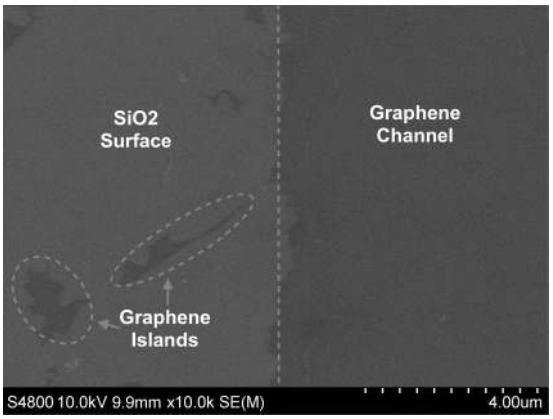
scanning electron microscopy was used to look for potential sheet defects. Figure 5.33 (a) shows the PECVD SiO_2 samples based on RIE etch show signs of being partially under etched at the edge of the passivation window. Figure 5.33 (b) Additionally, the graphene channel edge appears quite rough due to the under etching of the yttrium layer during the O_2 plasma etch step. Figure 5.33 (c) the MVD Al_2O_3 has a clean edge profile, Figure 5.33 (d) shows the graphene channel also appears to have a well-defined edge etch profile. This indicates that the MVD Al_2O_3 process produces a much more well defined process and would be better suited toward industry and further miniaturisation.



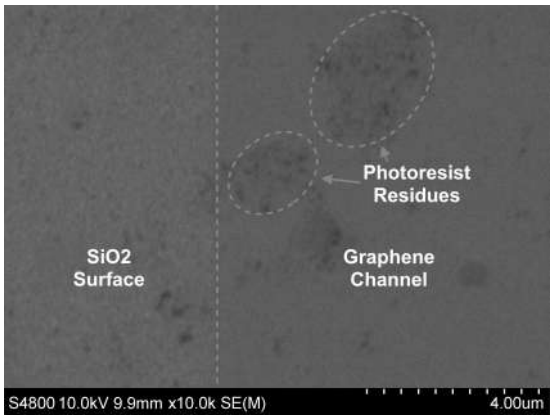
(a) SiO_2



(b) Al_2O_3



(c) SiO_2



(d) Al_2O_3

Figure 5.33: (a) Boundary region: PECVD deposited SiO_2 passivation film can be seen at the top of the image with an over etched edge region bordering the graphene channel and thermal SiO_2 substrate. The substrate SiO_2 on the left of the image shows signs of residues and graphene, due to yttrium residues preventing O_2 plasma etching of the graphene layer. (b) Boundary region: MVD deposited Al_2O_3 passivation film can be seen at the top of the image. The boundary layer appears to be crisp and well defined along both the graphene channel (right) and thermal SiO_2 substrate. (c) Graphene channel edge region of SiO_2 passivation chip. The edge appears undefined with unetched graphene islands close to the main channel. (d) Graphene channel edge region of Al_2O_3 passivation chip, Clearly defined channel edge. Some residues are present on the graphene surface, results from after the graphene channel etch or the graphene transfer process.

Further surface analyses were performed using AFM to compare the surface roughness and height differences of the graphene channel that has undergone the Al_2O_3 passivation method compared to SiO_2 passivation. The boundary region between the passivation layer and graphene channel was investigated (Figure 5.34). Figure 5.35 & Figure 5.36 show 3D map scans of this boundary region for the two passivation approaches.

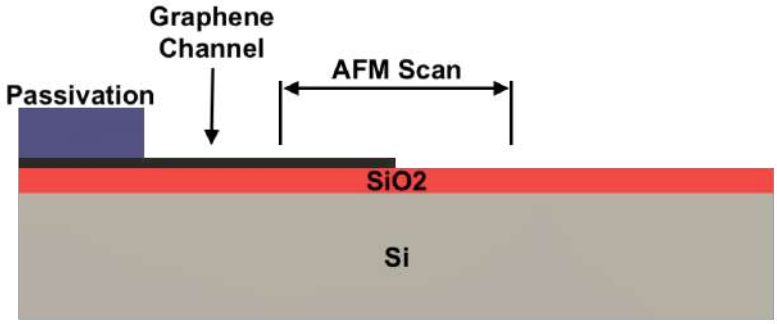


Figure 5.34: Diagram of AFM scan region.

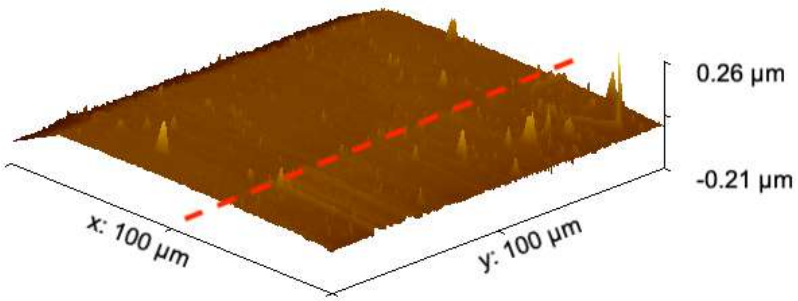


Figure 5.35: AFM 3D Map of graphene etch boundary with SiO_2 substrate boundary. The graphene has undergone metal evaporation, plasma deposition of dielectric, RIE dielectric etch followed by HCl wet etch.

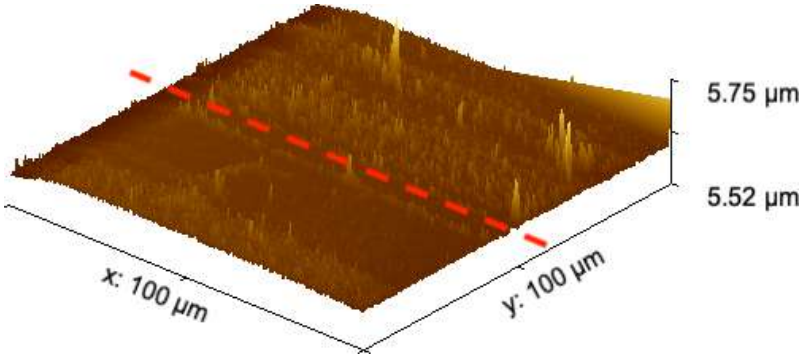


Figure 5.36: AFM 3D Map scan of graphene etch boundary with SiO_2 substrate boundary. The graphene has undergone direct MVD deposition of Al_2O_3 followed by TMAH wet etch.

The resulting roughness measurements were taken from 250 μm^2 area of total AFM map scan. Table 5.11 show a significant increase in roughness for the graphene in both passivated samples. This is due to a combination of structural damage, as a result of deposition and etch processes, as well as photoresist residues from the multiple photolithography steps. The increase in root mean square height (Sq) for SiO_2 passivated sample is 274 % with an increase of 187 % for the Al_2O_3 passivated sample. Both processes bring imperfections with the increases in roughness, on average the MVD deposited Al_2O_3 produces the lowest Sq and arithmetical mean height (Sa), suggesting this process produces lower levels of graphene contamination post-fabrication.

Table 5.11: AFM roughness root mean square height (Sq) and arithmetical mean height (Sa) comparison of MVD aluminium oxide and PECVD silicon dioxide passivation process.

	Graphene Roughness Sq (nm)	Graphene Roughness Sa (nm)
Blank Grapahene	2.94	2.18
PECVD Processed	10.92	7.57
MVD Processed	8.44	5.95

5.3 Packaging

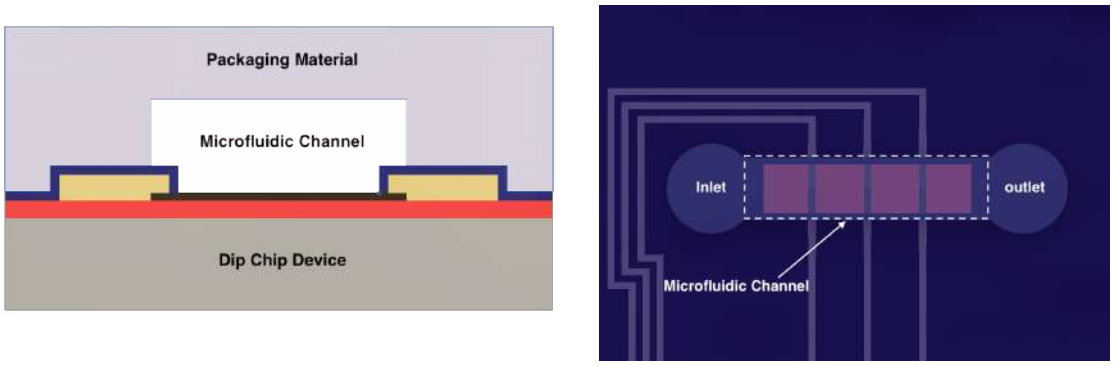
Packaging for biosensors enables connection between the sensor chip and the measurement system to be made. The packaging is used to improve performance and increase the functionality of the platform.

Microfluidic packaging can reduce total sample volumes and improve reliability by keeping stable volumes over the active sensor area. Microfluidic packaging can also be used for sample pre-processing, miniaturising procedures such as filtration or amplification, otherwise performed separately in the lab [19].

The design of a sensor package, that can be applied post graphene chip fabrication, enables the functionalisation steps to be performed in a more controlled system. Moving towards a commercial fabrication flow, chemical functionalisation process will also need to be automated. Drop-cast functionalisation was not possible using the current Multiplex design due to the hydrophilic nature of the passivation film, this could take the form of an open microfluidic system made of hydrophobic material.

However, for electrochemical functionalisation the graphene channel and two external electrodes (Ag/AgCl and Pt electrode) are required for the electrochemical three electrode setup. This would require an enclosed microfluidic system to isolate each graphene channels in the functionalisation solution.

Figure 5.37 shows the initial package design for the Dip Chip, a single microfluidic channel that crosses all three graphene channels. A separate inlet and outlet are used, so that liquid can flow through the channel and a constant volume can be held over the graphene active area.



(a) (b)

Figure 5.37: (a) Cross section CAD image of microfluidic channel applied to a passivated graphene Dip Chip. (b) Top down view of Dip Chip graphene channel cluster. Outline of microfluidic channel can be seen covering all three graphene channels. Circular regions at either end of the microfluidic channel represent the inlet and outlet junctions.

In order to develop a scalable microfluidic process, a series of methods have been examined. The ability to photo pattern PDMS has been investigated extensively for microfluidic systems [20]. The resolution of "photo-definable" PDMS does not result in a residue-free process as some PDMS layers remain on the substrate surface, similar to nano-imprint and substrate conformal imprint lithography an etching/ashing process is required to remove residues from features. The resolution of the channels achieved with this process is 250 μm. The main issue with upscaling is the lack of commercial photo-curable PDMS and elastomer products. Products such as Ostemer (Ostemer, Sweden) and UV-PDMS Shin-Etsu (Japan) require cladding layers to provide adhesion to the substrate, or would require etching to remove the base layers. To etch the remaining cladding/base PDMS layers would require etch-masks patterned across 3D features (trench walls).

To reduce process steps compared to a UV curing PDMS type process a direct thermal curing PDMS process combined with a dry etch process was developed. This way microfluidic channels could be patterned and etched away. An additional

layer to seal the microfluidic would then be bonded to the etched layer. Traditional thermal cured PDMS bonding to graphene Dip Chips was also optimised and tested with H_2O flowing across the graphene. A new fabrication method was developed for direct 3D printing of microfluidic channels onto a silicon chip, this was then used to print single channel and multiplex microfluidic packages onto graphene Dip Chip sensors for functionalisation.

In a separate research component the sample pre-processing (whole blood), for a blood clotting diagnostic sensor was investigated. Blood separation techniques in microfluidic systems were fabricated and optimised, to produce a blood pre-processing system suitable for a point of care diagnostic platform.

5.3.1 Materials & Methods

PDMS Microfluidic Bonding

The microfluidic design was created as a 2D AutoCAD file. This was converted to a polymer film photomask supplied by JD Photo-Data (UK). To create the master mould a plain Si wafer was used as the base substrate using the "AZ 125 nXT Microfluidic" photolithography protocol (section 3.5.3), using the single-channel microfluidic packaging photomask. Post-development the photoresist was hard-baked at 150 °C to create the master mould.

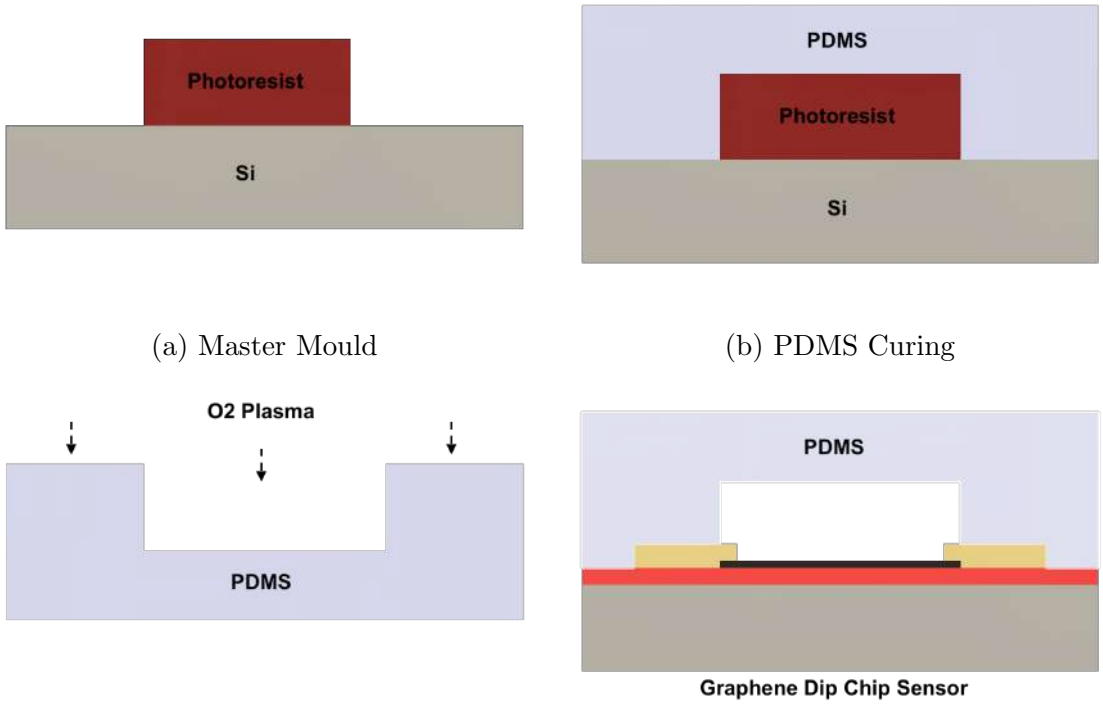
The silicon and photoresist master mould was inserted into a container so that PDMS could be poured onto the wafer and set to a thickness of 3 - 4 mm. The PDMS was then cured at 50 °C for 4 hours. The cured PDMS was then peeled off the master mould and cut using a scalpel into individual die.

PDMS to Dip Chip bonding is achieved using RIE O_2 plasma, 50 W, for 30 s and a chamber pressure of 75 mTorr for treatment of the PDMS layer. The treated PDMS layer is brought into contact with the Dip Chip surface. After 30 seconds of compressing the two surfaces together using a 100 g weight, the PDMS and silicon chips are heated at 80 °C to complete the bonding process.

Methanol (Sigma Aldrich, UK) was applied by pipette to the Dip Chip surface

before contact is made with the PDMS as a lubricant. The volume of methanol applied was not fixed and was added in excess until full surface coverage.

Figure 5.38 shows the full process flow for PDMS layer fabrication and bonding to graphene Dip Chip.



(a) Master Mould

(b) PDMS Curing

(c) Plasma Treatment

(d) PDMS SiO_2 Bonding

Figure 5.38: (a) Photolithpgraphy process to create inverted master mould of microfluidic channel. (b) PDMS pouring and thermal curing at 50 °C for 4 hours. (c) PDMS layer peeled off master mould, RIE O_2 plasma treatment used to modify PDMS surface. (d) Activated PDMS surface is brought into contact with SiO_2 surface for bonding.

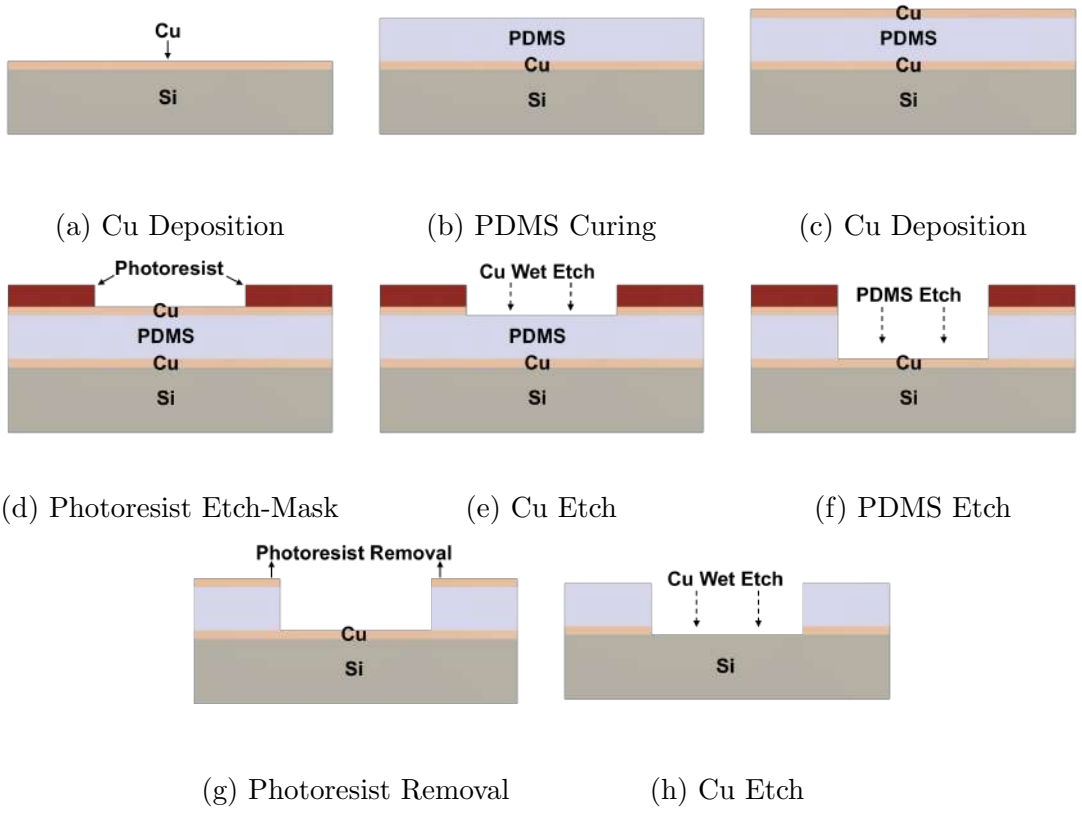
PDMS Spin Coating & Etching

To produce thin-film PDMS microfluidic chips for testing, Slygard 184 Elastomer (Dow) 10:1 ratio was mixed and degassed in a vacuum desiccator for 1 hour before spin coating. A volume of 2 ml was spin-coated using a Laurel spin coater on a

plain Si 100 mm wafer substrate. A spin curve was created by repeating the spin coating process on multiple wafers (diffrerent spin speeds tested and PDMS thickness measured). The spin coating recipe comprised of a single spin step for 45 s with an acceleration of 500 rpm/s the final spin speed was adjusted per wafer from 1000 - 5000 rpm in 1000 rpm intervals.

A hard copper etch mask was used due to the etch depth required (10 μm) [21]. A recipe based on an existing RIE [22]. The etch gases 75 sccm CF_4, 25 sccm O_2 and the chamber pressure of 60 mTorr were kept constant. Due to the spin coating thickness of PDMS, the total etch-time for PDMS is longer than standard thin film etch recipes, this extended time increases the plasma heating effect on the sample. To avoid the samples overheating the etch power was set at 150 W and the etch time was broken up to allow for cooling into 15-minute steps.

For the PDMS etch series plain si wafers were coated in PDMS using a spin coater speed of 3000 rpm. The cured PDMS was coated with 200 nm of evaporated Cu (Quorum evaporator). Followed by photolithography "nLOF 2070 protocol", of the passivation window photomask onto the Cu surface. The exposed copper was etched using wet etch 1:20 Nitric acid HNO_3 : H_2O_2 diluted 1:5 in di H_2O (BYU Cleanroom 2019). The photoresist was then removed using a Solvent Clean to reveal the Cu Hard etch mask. Figure 5.39 shows the process flow of PDMS etching process.



(a) Cu Deposition (b) PDMS Curing (c) Cu Deposition

(d) Photoresist Etch-Mask (e) Cu Etch (f) PDMS Etch

(g) Photoresist Removal (h) Cu Etch

Figure 5.39: (a) Cu deposited (thermal evaporation) using quorum sputter coater. (b) PDMS pouring and thermal curing at 50 °C for 4 hours. (c) Cu deposited (thermal evaporation) using quorum sputter coater. (d) Photo-patterning using nLOF 2070 to fabricate photoresist etch-mask. (e) Cu wet etched using Nitric acid solution to create Cu etch-mask for selective PDMS etching. (f) RIE plasma etch process of PDMS layer to Cu etch stop layer. (g) Photoresist removed using Solvent Clean process. (h) Cu wet etch process to reveal base substrate and remove Cu etch-mask from PDMS surface.

PDMS etching was performed using RIE plasma etching. A photoresist etch mask AZ nXT 125 spun at 3000 rpm to produce a 20 μm thick etch mask. Protocol for RIE PDMS etch uses CF_4 75 sccm and O_2 25 sccm with a pressure 50 mTorr. Power was varied but set at 150 W with cycles of power on and power off to prevent the substrate overheating. The photoresist etch mask was then removed using a Solvent Clean.

3D Printed Microfluidic Packaging

The details of file conversion and the polymer filament used in the microfluidic 3D printer can be found in Materials & Methods Chapter section 3.9.3 (Figure 5.40).

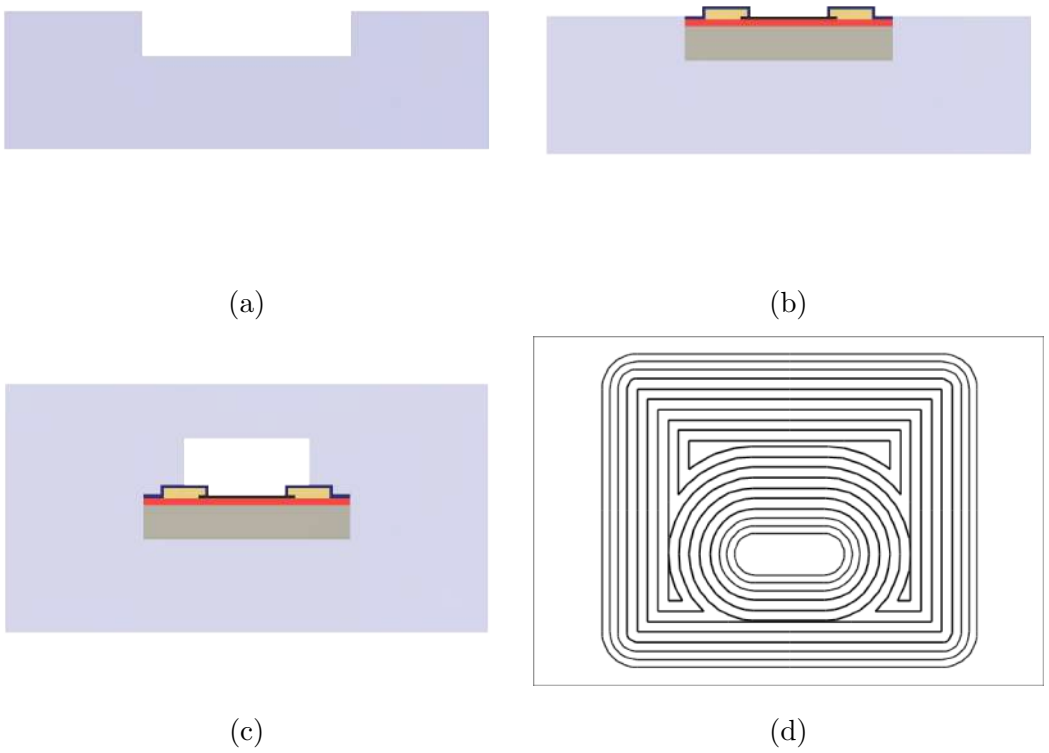


Figure 5.40: (a) Base layer COC printed directly onto Fluidic Factory print bed, notch for embedding Dip Chip set to 530 μm to allow for shrinkage of material. (b) Dip Chip epoxy bonded to base layer aligned with notch region allowed to set for 15 minutes. (c) The top layer containing the microfluidic channel is then printed directly onto the surrounding COC as well as the Dip Chip surface materials. (d) Fluidic Factory conversion file showing individual filament path of open chamber region.

To improve polymer filament to sensor surface adhesion and create a liquid-tight seal of the microfluidic channel, screen printed passivation layer was integrated onto the Dip Chip surface [6]. The mechanism for fabricating the packaged chip involved

splitting the print into two halves. Printing a base with a recessed region to place and fix the Dip Chip substrate, inserting the Dip Chip and bonding it in place followed by printing the second half of the design containing the microfluidic channels printed directly onto the Chip.

Microfluidic Liquid Testing

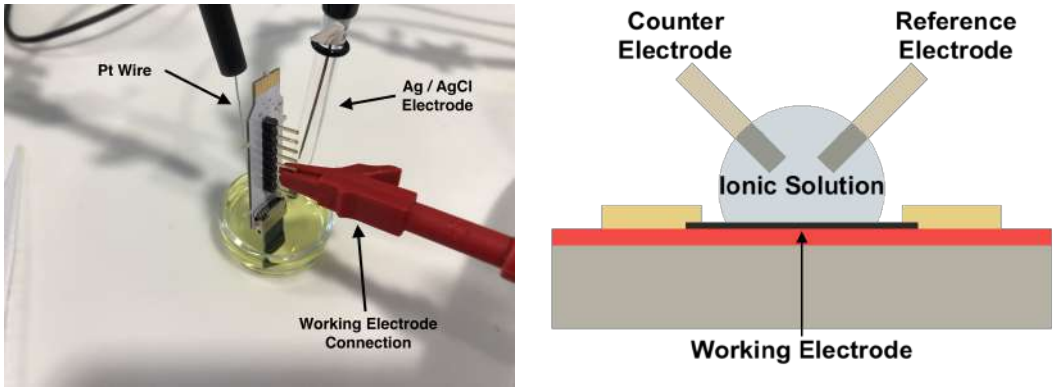
Liquid testing of both open microfluidic chambers and sealed microfluidic chambers were performed using di H_2O and a red food colouring (amazon.co.uk, UK).

Electrochemical Functionalisation

Details of Electrochemical functionalisation using a 3 electrode setup can be found in Materials & Methods Chapter section 3.10.2.

Details for electrodeposition of gold and electrochemical polymerisation of pDAN can be found in Materials & Methods Chapter section 3.10.3.

For in packaging functionalisation of both methods the SD card connector is used to enable submersion of the Dip Chip inside the ionic functionalisation solution. The graphene channel represents the working electrode, the Ag / AgCl reference electrode and Pt wire as the counter electrode see Figure 5.41. Firstly the process of multiplex functionalisation was repeated using a passivated non-packaged Dip Chip. The first functionalisation mechanism to be tested was the electrodeposition of Au



(a) (b)

Figure 5.41: (a) Foreground shows the Dip Chip inserted in SD card connector. A single header pin connected by crocodile clip creates a connection to a single graphene to act as the working electrode. Back left Pt wire counter electrode. Back right the Ag / AgCl reference electrode protected with Double-Junction System (Metrohm, Switzerland). (b) Graphene channel in three-electrode electrochemical system.

Optical and Physical Analyses

For SEM imaging the parameters used (Section 3.12.1).

For AFM imaging the parameters used (Section 3.12.4).

Electrochemical Analyses

Square-Wave Voltammetry and Pulsed-Differential Voltammetry cycle settings (Section 3.11.3).

Blood Separation Microfluidics

Details of blood collection and ethics (Section 3.9.3).

Blood was collected within 4 hours of testing the microfluidic devices. The blood was removed from the collection tube using a 5 ml Luer-lock syringe (BD, USA) and then connected to the syringe pump (Single Microfluidic Syringe Pump,

World Precision Instruments, USA). Microfluidic tubing was used for connection with $1/16^{th}$ outer diameter (Darwin Microfluidics, UK). connected via PEEK Micro-Fitting connectors (Sigma Aldrich, UK) to the syringe.

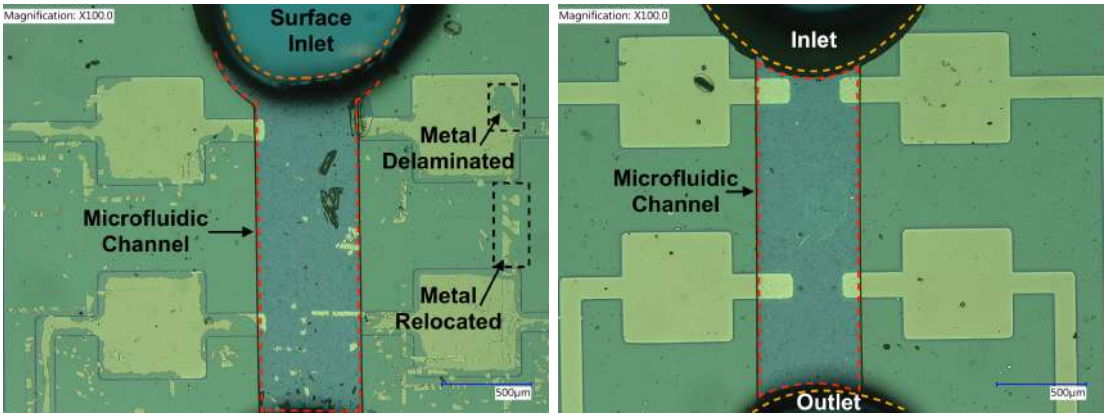
5.3.2 Results & Discussion

PDMS Microfluidic Bonding

Polydimethylsiloxane (PDMS) is widely used for microfluidic-based research as well used for early-stage rapid prototyping. And often used for substrate level packaging through the use of imprinting and bonding to the substrate. Based on a two-component mixture (monomer and curing agent), the end product is a flexible polymer with a low Young modulus (1.32–2.97 MPa), which is optically transparent [23]. The initial design for Dip Chip packaging consisted of a single microfluidic channel with regions to connect the inlet and outlet. This can then form a microfluidic cell to flow liquid across the graphene channel. The SiO_2 substrate makes up a majority of the Dip Chip surface area so should provide a similar bonding surface to PDMS glass bonding.

For PDMS to glass bonding, both surfaces are plasma treated and are brought into contact. The two reactive surfaces react and covalently bond to each other [24]. However, this methodology cannot be used as O_2 plasma treatment of the graphene surface would result in damage/removal of the graphene. In this modified process, the Dip Chip was not plasma treated before being brought into contact with the PDMS chip.

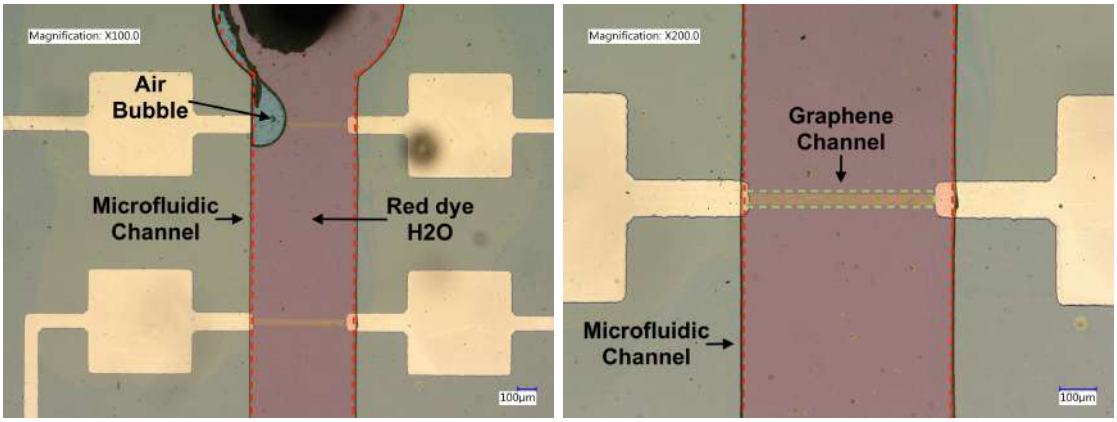
This modified plasma bonding process was tested by directly bonding PDMS to non-passivated chips with metal electrodes (no graphene present). Bonding in a single step process by manually manipulating the PDMS block proved difficult and inaccurate. Figure 5.42 shows the PDMS that came into contact with the chip but due to misalignment was required to be repositioned on the Dip Chip surface, as a result of this movement the metal contacts were seen to partially delaminate.



(a) (b)

Figure 5.42: (a) Non passivated Dip Chip, PDMS was brought into contact with the SiO_2 and metal electrodes incorrectly. The PDMS was repositioned to improve alignment (b) PDMS accurately aligned using a single attempt. Metal contacts appear intact.

Methanol was introduced lubrication agent to aid the alignment of the chips without affecting the PDMS to SiO_2 bond. Figure 5.43 shows chips that were successfully aligned, connected to syringes and tested with di H_2O mixed with red food colouring. Red food colouring was added for visualisation of the liquid transport through the channel.



(a) (b)

Figure 5.43: (a) PDMS Microfluidic chip bonded to graphene Dip Chip. Punctured inlet region visible leading to microfluidic channel filled with di H_2O (red food colouring added). (b) Graphene channel fully exposed to di H_2O inside microfluidic channel.

Resistance measurements were performed on the graphene channel before bonding, after bonding and after the introduction of di water into the microfluidic system. Alignment by hand in this manner is incredibly time-consuming without high accuracy yields. Some chips were misaligned (approximately 40 %). Table 5.12 shows there was no significant change in resistance on the three Dip Chips tested after bonding PDMS microfluidic to the surface. A resistance increase was then observed during the flow of di H_2O across the surface. This suggests that liquid is flowing across the graphene surface as a resistance change was observed.

Table 5.12: Calculated graphene channel resistance before PDMS bonding and calculated change in resistance (%) after bonding and after liquid testing

	Resistance (Ω) Pre-Bonding	Post-Bonding PercentageΔ (%)	di H2O Test PercentageΔ (%)
9 Channel Average	8481	-1.37	26.42
Standard Deviation	793	0.57	4.80

This method was successful in fabrication of a useable microfluidic package on top of the graphene Dip Chip. Difficulties regarding the plasma bonding and the alignment process result in a lower than optimum yield. Additionally, this process is hard to upscale and would not be compatible with the miniaturisation of the graphene channel. Alignment under these conditions would require specialised equipment made more difficult with not being able to plasma treat the SiO_2 substrate.

PDMS Spin Coating & Etching

The aim is to cure PDMS directly onto the finished graphene Dip Chip wafer. The flat PDMS could then have photoresist spin-coated onto the surface to pattern a photoresist etch-mask. Using a modified PDMS anisotropic dry etch to etch through the PDMS down to the Dip Chip graphene [22]. The microfluidic would then be sealed using a flat piece of PDMS plasma bonded, or pressured sealed using a rigid material.

For the PDMS etching microfluidic process, first the PDMS layer was spin coating in its liquid form, followed by thermal curing. A PDMS thickness spin curve was created to calibrate PDMS thickness with respect to spin speeds. Figure 5.44 shows PDMS thickness of 10 μm from using a speed of 5000 rpm, this speed was chosen for for etch process development.

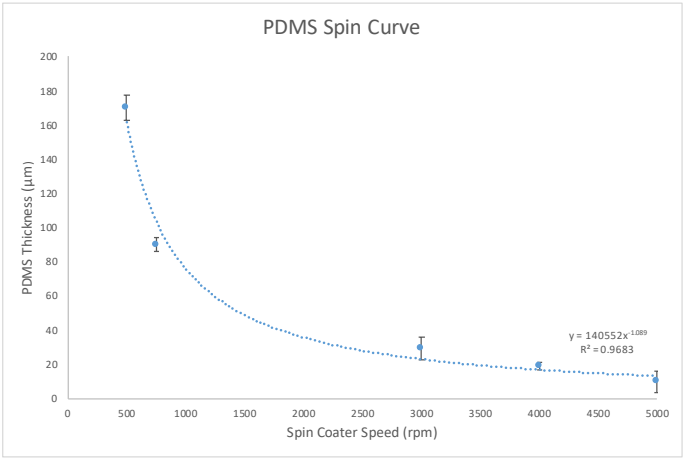


Figure 5.44: PDMS thickness/spin speed calibration for a PDMS composed of 10:1 ratio PDMS elastomer to curing agent followed by 1 hour of degassing. After spinning PDMS thickness was measured at multiple points using Keyence microscope. Fitted with

To determine the etch rate of PDMS using an RIE process, an etch series was created by etching quarter wafer test pieces of a silicon wafer coated with PDMS film with a Cu etch mask. The quarter wafer samples were RIE etched for increasing lengths of time (15-minute intervals to avoid overheating).

Figure 5.45 shows the resulting etch depths measured by profilometer. The average etch rate of 12 μm per hour was estimated. For a PDMS spin of 5000 rpm, 8 - 10 μm thickness a 1 hour etch should be sufficient to etch through the PDMS layer.

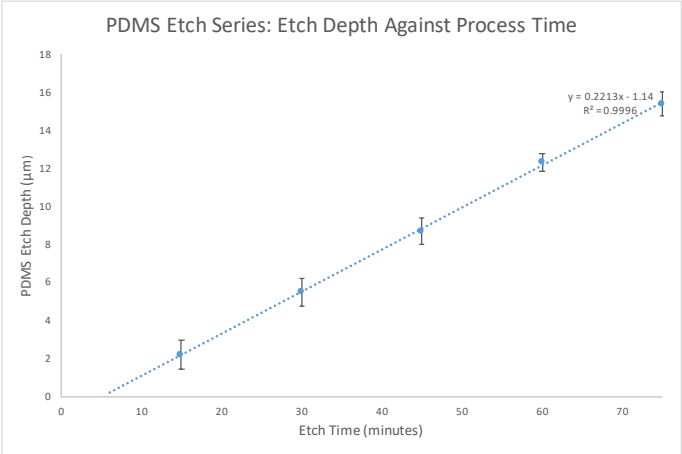
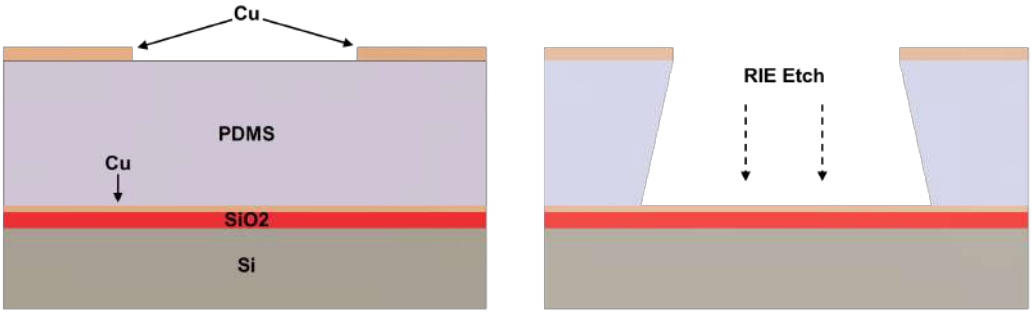


Figure 5.45: PDMS RIE etch series, monitoring the effect of increasing etch duration against measured etch depth.

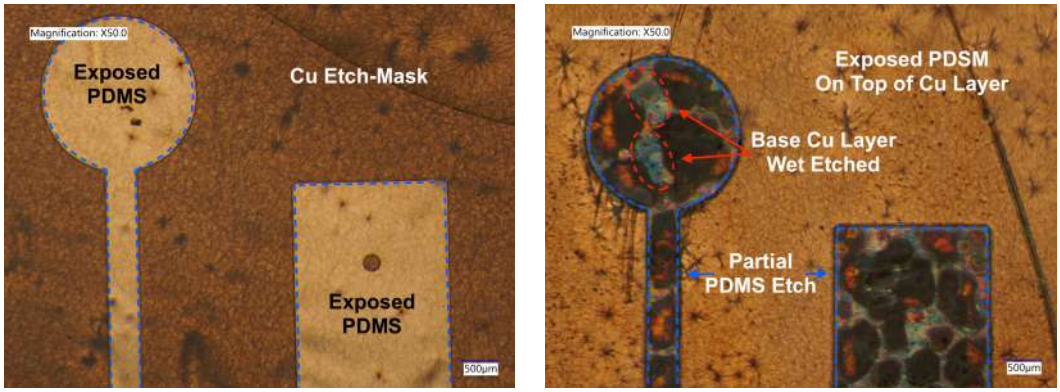
For the PDMS microfluidic etch experiment a copper base layer on the Si substrate was required, to clearly define when the PDMS layer is etched through to the base substrate (Etch recipe would continue to etch Si after penetrating the PDMS layer). In the final device packaging, the graphene surface would need to be protected by a sacrificial metal layer. Cu layer used to represent the sacrificial layer required to protect the graphene during the RIE etch process. Figure 5.46 shows the the PDMS etch experiment. Additionally, the Cu layer deposited on the substrate can be wet etched as an indicator of the PDMS layer being etched through successfully.



(a) (b)

Figure 5.46: (a) Cu etch mask created using Dip Chip Test Structure photomask on top of spin coated PDMS layer. (b) RIE deep PDMS isotropic etch, Cu etch stop layer used to prevent etching of the Si substrate.

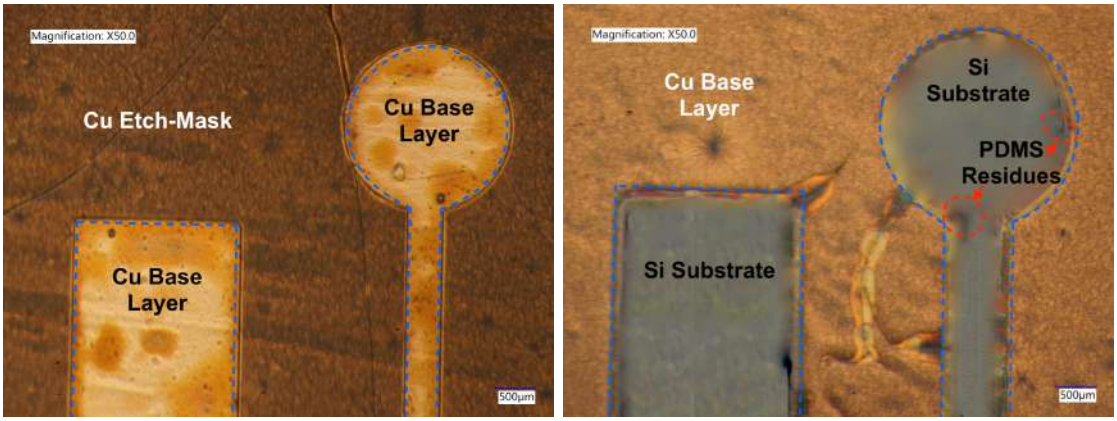
Following the RIE etch process and complete etch through the PDMS layer, a further Cu wet etch step was completed to remove the Cu etch mask. The Cu wet etch step removed the substrate etch stop layer partially see Figure 5.47. This suggests the etch has not fully removed the PDMS layer as the copper is only etched in the break regions "cracks" in the PDMS film.



(a) (b)

Figure 5.47: (a) Patterned Cu etch mask on top of cured PDMS layer. Substrate Cu etch stop layer visible through PDMS layer. (b) 60 minute RIE etch process followed by Cu wet etch, Cu top etch mask layer removed, substrate etch stop layer partially etched clustered in regions where PDMS film is thinnest.

Further etching was required to fully remove the PDMS film from the base of the etched regions. A second sample was etched for a total of 75 minutes using the staggered 15-minute etch protocol, followed by a Cu wet etch for 5 minutes. The resulting etch removed the patterned Cu etch mask as well as the Cu etch stop, which indicates that the PDMS has been etched through completely (Figure 5.48). The residues left behind could not be removed with di H_2O rinse steps, which suggests that more than pure Cu etching takes place. PDMS is known to absorb acids and break down over time, the reactions on the surface are likely to be the break down products of PDMS such as small weight oligomers ($(CH_3)_3Si[OSi(CH_3)_2]_xOSi(CH_3)_3$) [25].



(a) (b)

Figure 5.48: (a) PDMS sample etched for 75 minutes in RIE system. Substrate Cu etch stop layer visible through PDMS layer. (b) 75 minute RIE etch process followed by Cu wet etch, Cu top etch mask layer removed, Cu etch stop layer removed with some minor residues visible.

The 75 minute etch process was repeated on 2 further samples. The next stage of testing involved forming a seal on the top surface of the PDMS film to create an enclosed microfluidic channel. The second layer of PDMS was drop cast and cured on a smooth silicon wafer. The RIE O_2 plasma bonding process used to bond PDMS to SiO_2 / glass was also used to bond PDMS to PDMS.

However, the resulting bonding process when applied to the previous RIE etched sample did not result in bonding. Therefore it was impossible to produce a liquid-

tight between the two PDMS layers. This could be due to either the copper deposition process, or could be due to the absorption/reaction of the PDMS surface to the nitric acid during the Cu etch process, PDMS ageing and surface degradation have been shown to reduce bonding effects [24].

To investigate whether the bonding issue was due to Cu evaporation layer or was due to the nitric acid etch step. To investigate PDMS to PDMS bonding, PDMS was drop cast, cured and cut into 10 mm x 10 mm pieces for testing. Standard RIE O_2 plasma (40s), PDMS to PDMS bonding was performed as a control test. Three pieces of PDMS were submerged in the Cu wet etch solution (Nitric acid) rinsed twice in di H_2O baths and dried using compressed air. The bonding procedure (40 s) RIE O_2 plasma was performed on both non-treated and treated PDMS samples before bringing the section into contact for bonding. Permanent bonding was not achieved in the nitric acid treated samples. This suggests that the acid treatment of the PDMS damages the surface, reducing the number of active sites available for covalent bond formation, and prevents bonding.

The PDMS etching method is better for direct alignment of the microfluidic channel. However, the etching process damages the PDMS surface making further bonding and device sealing impossible.

3D Printed Microfluidic Packaging

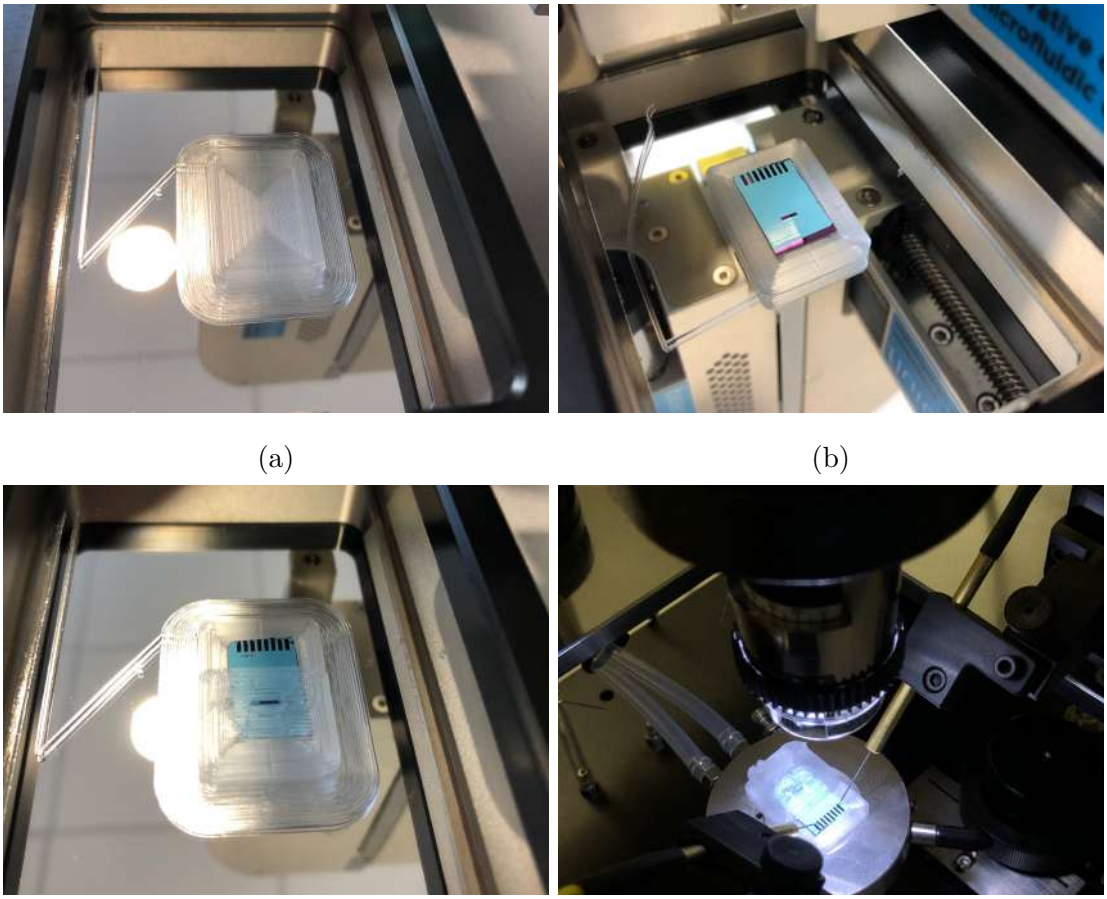
3D printed microfluidics is a growing research trend. The three main categories of 3D printers used for microfluidic applications are Inkjet 3D printing (i3DP), Stereolithography (SLA) and Fused deposition modelling (FDM). Each of these methods has pros and cons regarding microfluidic 3D printing, as seen in the 3D Printed Microfluidics section of the Literature Review Chapter.

The SLA based printers are currently limited in terms of printing materials that can be used (e.g. biocompatible materials). SLA's high resolution makes it best suited for microfluidic channels with dimensions down to 150 μm in height or width [26]. However, with a lack of pause capability (The ability to stop and start the 3D print in an open to air environment), it would be difficult to insert

the Dip Chip inside the microfluidic. A two-part system could be fabricated but liquid-tight adhesion to the chip surface without the use of a gasket could lead to leakage and contamination of the device. The i3DP based printers are currently focused on large scale commercial manufacture. Open channels with 200 μm cross are achievable [27]. The i3DP system has multi-material benefits but is not currently targetted to microfluidic systems.

The need to create a liquid-tight seal on the Dip Chip surface favours specialised FDM 3D printing (as the polymer can solidify on the chip surface). The Fluidic Factory 3D printer (Dolomite Microfluidics UK) is designed specifically for liquid-tight microfluidic prototyping, and has pause functionality enabled within its standard software. It has a channel resolution of 320 μm width and 150 μm height using cyclic olefin (COC), a biocompatible polymer filament. Based on specifications from Dolomite Microfluidics direct printing of a microfluidic chamber directly onto a screen-printed electrode chip. It was recommended by the manufacturer not to print directly onto a rigid substrate such as Si as the polymer contracts upon cooling and could partially delaminate from the surface. In contrast, the screen-printed electrode chip (Drop Sense Metrohm, Switzerland) is coated with a passivation ink layer, this layer has a lower stiffness than the polyethylene naphthalate or polyethylene terephthalate substrate. This low stiffness value allows for deformation upon cooling of COC filament reducing the chance of delamination and producing a liquid-tight seal shown to last for 2 hours upon testing.

The first microfluidic design was based on creating an open chamber over the channel to allow IV probing the graphene channel as well as leak checking the COC passivation ink film interface. The fabrication process of the first test package was completed with a printing run time of 37 minutes and filament usage of 0.71 m. The microfluidic cartridge was successfully printed, encapsulating the graphene region of the Dip Chip (Figure 5.49). IV measurements were performed using the Everbeing IV probe station, graphene channel resistances were calculated to identify changes to resistance pre and post packaging.



(a) (b)

(c) (d)

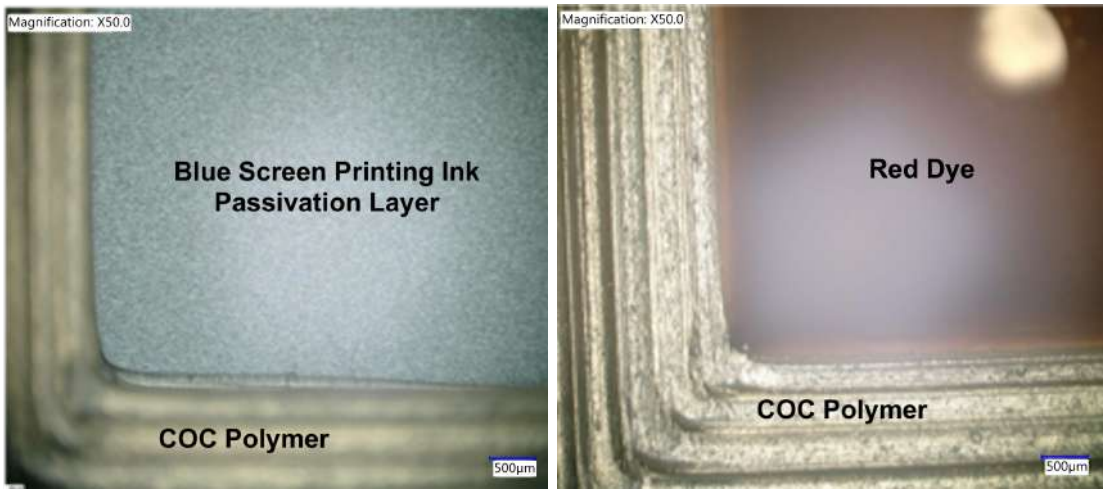
Figure 5.49: (a) First half of print completed with full Dip Chip recessed inset. (b) Dip Chip with blue passivation ink layer, epoxy bonded to COC print. (c) Second half of print with alignment of window opening to graphene channel. (d) IV probing of encapsulated Dip Chip.

The initial resistances were calculated before 3D printed packaging, post-packaging and after di H_2O pipetted into the open chamber. Table 5.13 shows the averages calculated for each test step. There was a minor decrease in resistance post-packaging and an increase in resistance after the application of H_2O. The data shows FDM printing with a nozzle temperature of 225 °C does not affect the graphene electrical conductivity at a distance of 500 μm from the channel.

Table 5.13: Calculated graphene channel resistance before 3D printed packaging and calculated change in resistance (%) after packaging and after liquid testing

	Resistance (Ω) Pre-Packaging	Post-Packaging PercentageΔ (%)	di H_2O Test PercentageΔ (%)
3 Channel Average	8829	-1.05	10.78
Standard Deviation	108	0.62	12.53

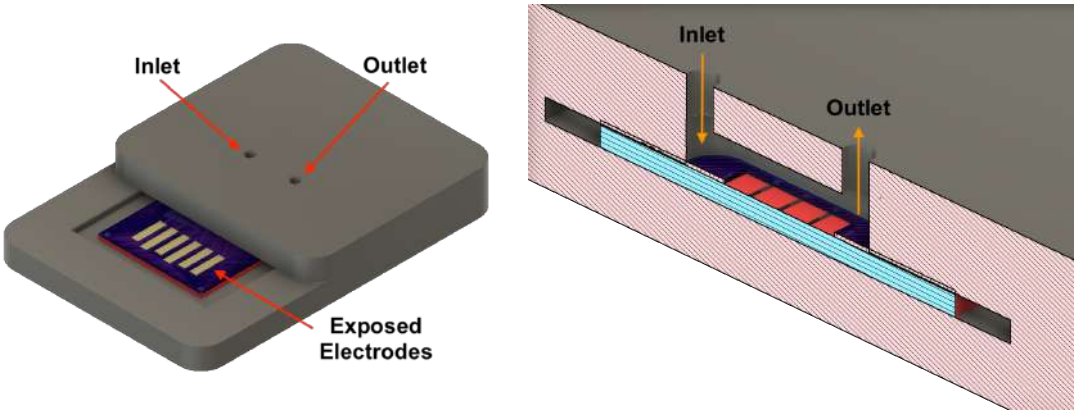
Liquid leak testing was performed using the open chamber design, using red food colouring to identify any leakage at the COC printed film interface. The red food colouring (100 μl) was pipetted into the chamber and left for 2 hours inside a sealed petri dish to prevent evaporation of the liquid. Figure 5.50 shows the microfluidic chamber edges examined optically. No sign of leakage could be discerned, the screen printing passivation ink appears to be an effective deformation layer when applied to Si chips similar to screen printed electrodes.



(a) (b)

Figure 5.50: (a) Bottom left corner of 3D printed packaging open chamber. Visible blue passivation screen printing ink and COC printed polymer. (b) Red food colouring pipetted into open chamber and examined after 2 hours. No sign of diffusion into the COC region.

The next stage of testing was to fabricate a complete microfluidic channel with inlet and outlet so liquid can be flown through the chamber over the graphene channel. Figure 5.51 shows he initial 3D design involves a simple vertical inlet and outlet with a 1.5 mm width 5 mm length, 300 μm height microfluidic channel see CAD design.

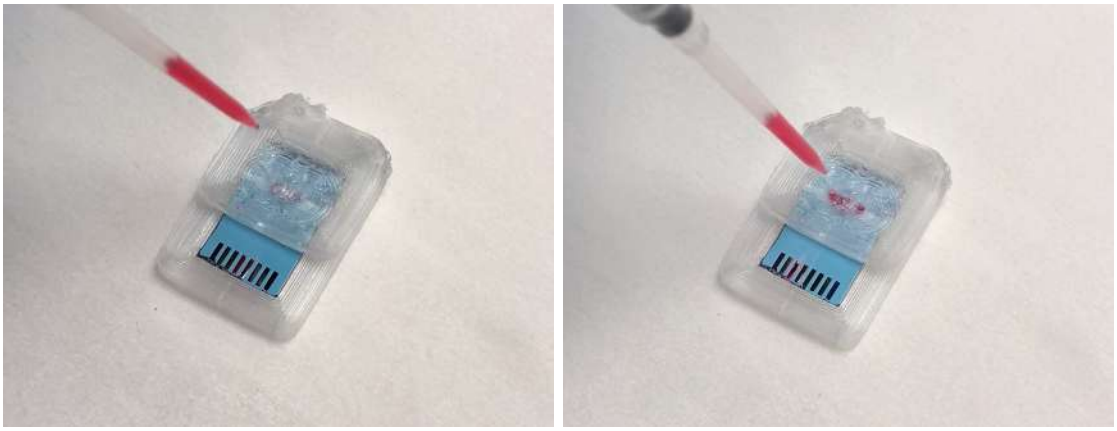


(a) (b)

Figure 5.51: (a) 3D printed microfluidic Dip Chip cartridge with exposed metal electrodes for IV probe measurements. (b) Sectional of the microfluidic channel above the graphene channel of Dip Chip.

Figure 5.52 shows the microfluidic flow of red dye that was pipetted into the microfluidic channel. The cartridge was left for 2 hours in a sealed container and examined optically to check for signs of leakage. No signs of fluid leakage were observed after the two hours. This suggests that 3D printed COC microfluidic channels can be effectively printed directly on the chip surface, creating a microfluidic package for the sensor.

This method of packaging can be used to create additional microfluidic features in vertical space with a minimal footprint area, compared to PDMS soft lithography which requires multiple layers of bonding to create vertical 3D features.



(a) (b)

Figure 5.52: (a) ISO view of 3D printed microfluidic Dip Chip cartridge with exposed metal electrodes for IV probe measurements. (b) Section analyses of the microfluidic channel above the graphene region of Dip Chip.

Functionalisation in Packaging

Multiplex functionalisation was previously demonstrated using electrochemical deposition techniques [6]. The 3 graphene channels present on the Dip Chip were used to functionalise the first graphene channel with Gold (Au) nanoparticles. An Au nanoparticle will preferentially bind a bio-receptor molecule that contains a thiol group at its base [28]. The second graphene channel is then left blank as a control channel, to monitor environmental change and later isolate the effects of physisorption vs chemical absorption of the target molecules. The third graphene channel was functionalised via electro-deposition of poly 1,5-Diaminonaphthalene (pDAN) [29]. The exposed amine groups of the pDAN can then be modified with EDC/NHS (1-ethyl-3-(3-dimethylaminopropyl)carbodiimide/N-hydroxysuccinimide) which allows for direct immobilisation of enzymes/antibodies via connection of their amine groups [30].

Figure 5.53 shows the resulting current measured during the 60 s electro-deposition of Au . The graph shows an increase in current during deposition of Au onto the graphene channel. The current saturates after 24 - 25 s, at this point it is thought

that the graphene channel is fully coated with a conducting film of Au. For optimised biosensor applications it would be important to tune this protocol for the exact quantity of Au deposition required. However, for this multiplex study proving the ability to deposit Au on a single graphene channel is the main outcome.

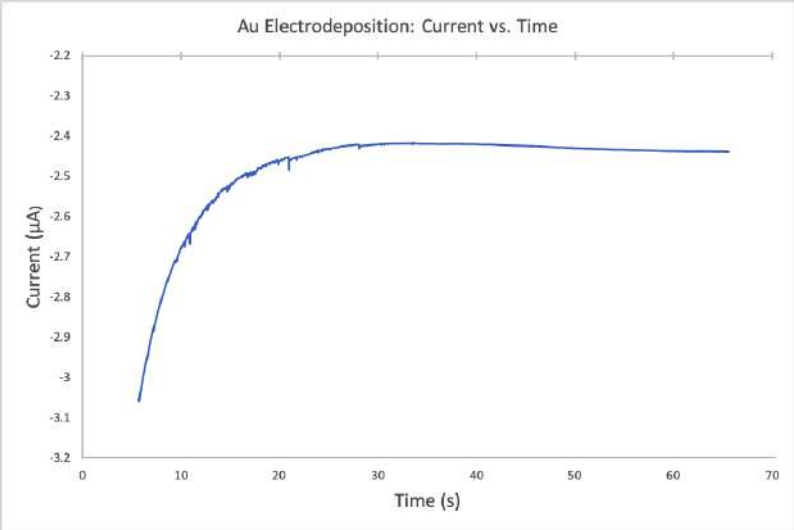


Figure 5.53: Electro-deposition of Au onto graphene channel 1. Graph showing current against time measured using 3 electrode set up (counter electrode current measurement).

The second functionalisation process, polymerisation of DAN molecules, was performed on the third graphene channel. Using a 3-electrode system the third graphene channel was connected to form the working electrode. Figure 5.54 shows the plot of current against applied potential. The increasing oxidation and reduction peaks represent the addition of more layers of pDAN onto the surface as the additional amine groups of the DAN layer undergo redox reactions.

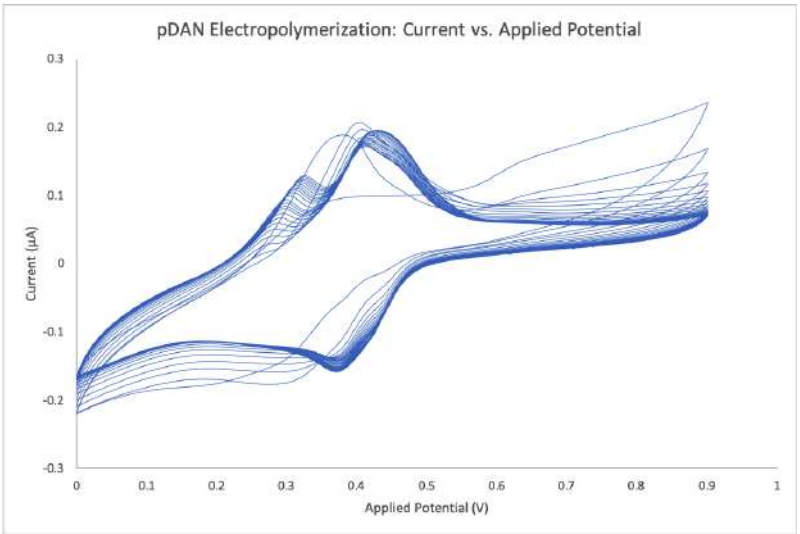


Figure 5.54: Electropolymerisation of pDAN onto graphene channel 3. Cyclic voltammetry plot showing current measured against the applied potential.

The graphene channels were imaged prior and post multiplex functionalisation using a Keyence microscope (Figure 5.55). The images clearly show changes to the graphene surface. A lot of residues from cross-contamination of solutions and the functionalisation processes remained on the SiO_2 surface.

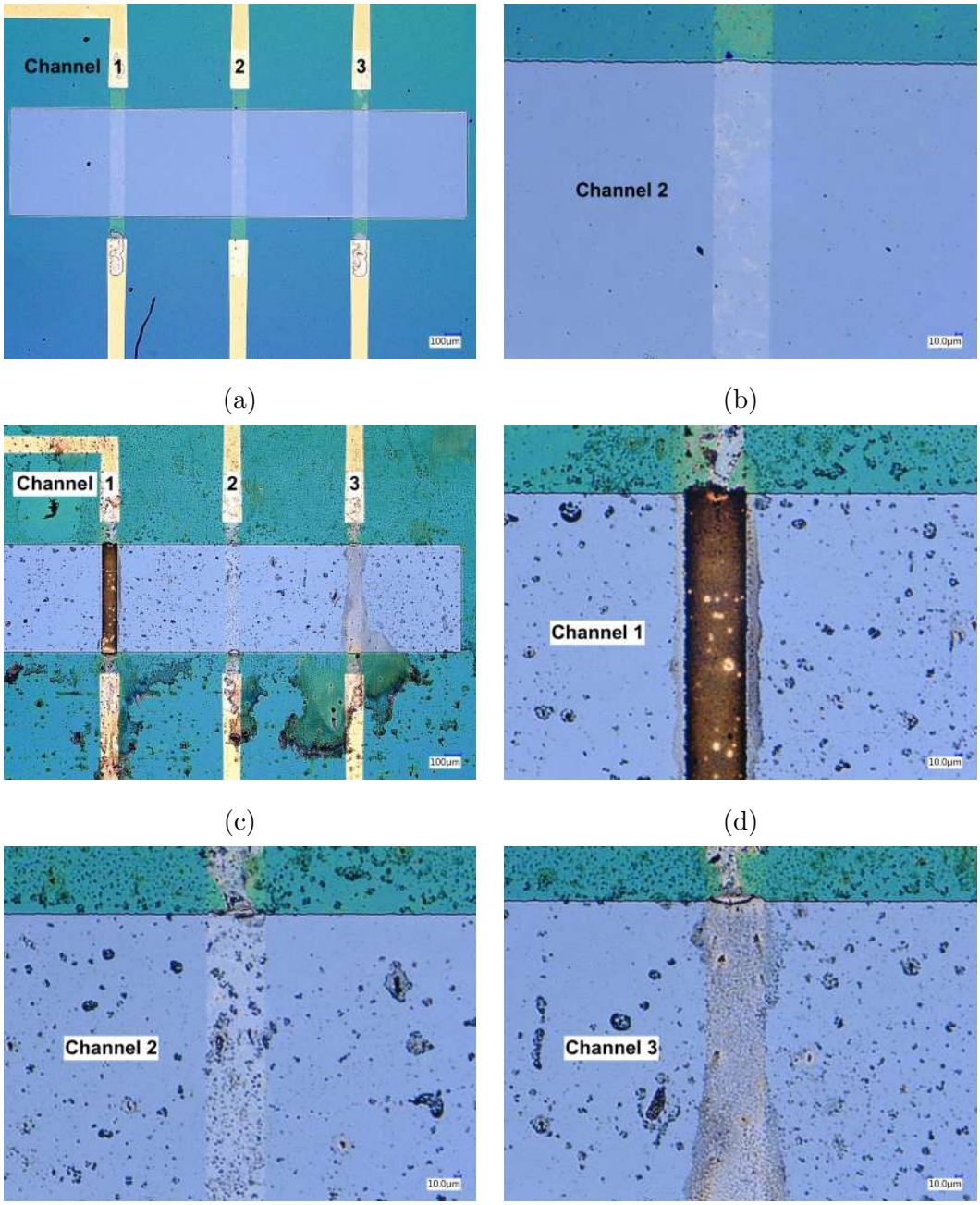


Figure 5.55: (a) Pre-functionalised, graphene channels are blank. (b) Pre-functionalisation, control channel 2. (c) Graphene Channels post multiplex functionalisation; channel 1 Au deposited, channel 2 control not functionalised, channel 3 pDAN deposited. (d) Channel 1 showing dark orange colour fully coated with Au an dark colouration due to other contaminants Cl, C. (e) Channel 2, not functionalised, other contaminants have adhered to the graphene and surrounding surface. (f) Channel 3 with pDAN deposited onto the graphene surface and expanding outward from the channel as the total mass of pDAN increased with each CV cycle.

Figure 5.56 shows SEM images from further examination of the functionalised graphene surface. SEM clearly shows that the centre control channel is contaminated due to the electrochemical functionalisation process. This could lead to bio-receptors attaching to the surface by physisorption and suggests the channel is not a true control.

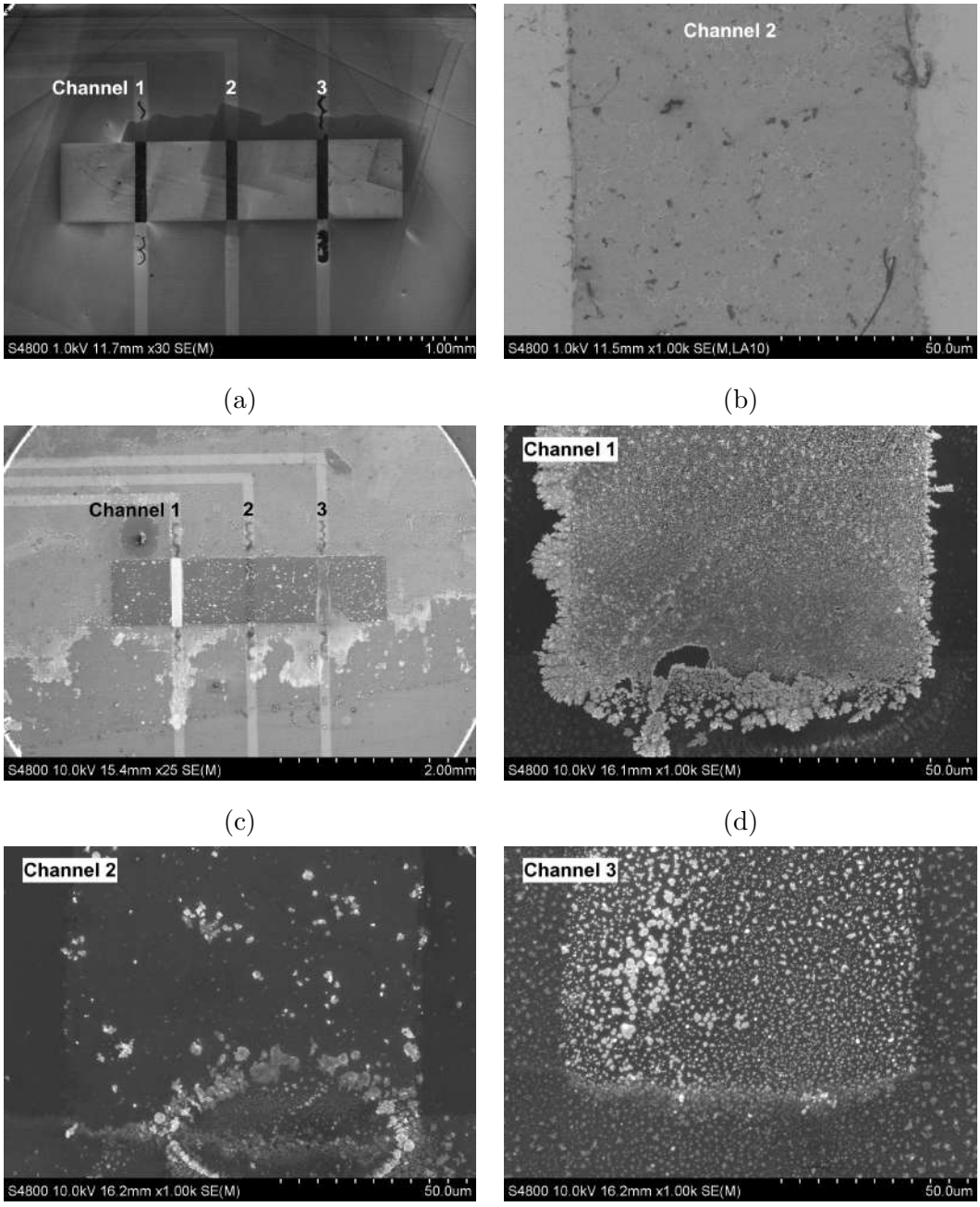
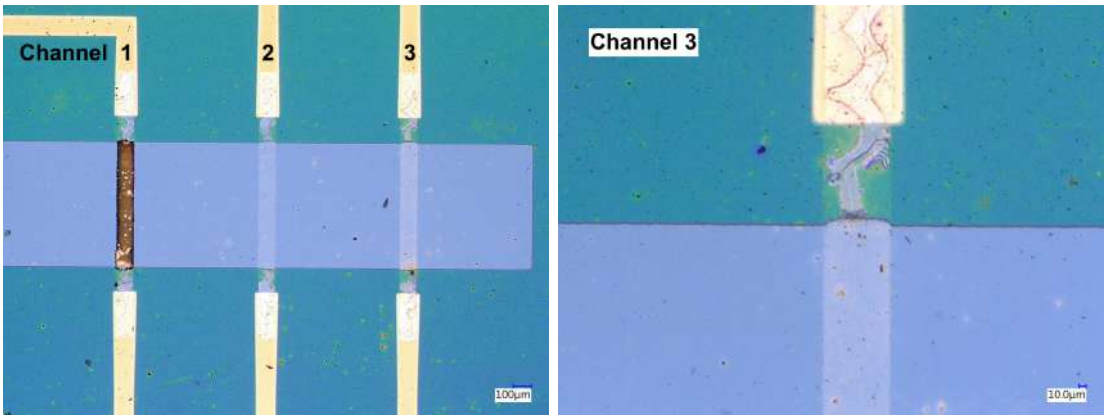


Figure 5.56: (a) SEM images Pre-functionalisation (graphene channels are blank). (b) Pre-functionalisation, control channel 2, some environmental contamination seen on surface. (c) Graphene Channels post multiplex functionalisation; channel 1 Au deposited, channel 2 control not functionalised, channel 3 pDAN deposited. (d) Channel 1 showing crystal like growth of Au on the surface, extreme growth can be seen on the edges. (e) Channel 2 remains not functionalised. However, other contaminants have adhered to the graphene surface, including Au and monomer DAN clusters. (f) Channel 3 with pDAN deposited onto the graphene surface with additional clusters of Monomer DAN adhering to the surface.

To remove surface contaminants a solvent clean was used. The majority of contaminants remained even after the solvent clean so a 2 s pulsed sonication step was used in di H_2O. Figure 5.57 shows the graphene channels after clean process, the clean has removed a majority of contaminants but also removed the deposited pDAN layer from the graphene surface.



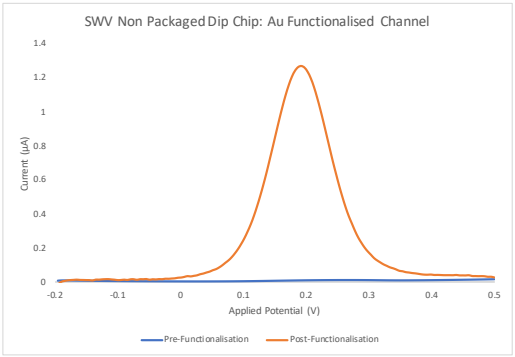
(a) (b)

Figure 5.57: (a) Graphene channels post sonication, Au remains on channel 1, contaminants removed and pDAN layers removed from channel 3. (b) Magnification of channel 3 pDAN layers removed during sonication process.

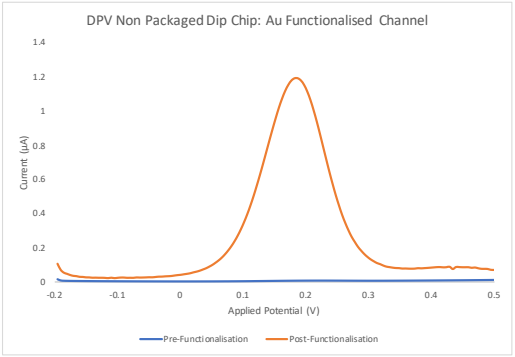
Electrochemical analyses methods were conducted to further validate the effect of functionalisation on the graphene channels. Firstly square wave voltammetry (SWV) was used to measure changes in current through the graphene three-electrode circuit. Secondly, differential pulse voltammetry was then performed as a secondary voltammetry technique to measure the changes in current. Each graphene channel was measured before functionalisation. After the final functionalisation process (pDAN), the Dip Chip was washed with buffer 10x wash steps and then measured using SWV and DPV for a second time.

Figure 5.58 shows the resulting electrochemical plots, (a) and (b) clearly shows a large increase in response from the initial blank graphene to the substantial Au coated peak (graphene peak hidden due to the scale of Au peak). Figure 5.59 (a) and (b) representing the control channel the SWV show a slight a shift/new peak

near 0.1 this could be due to the contamination seen on the surface of the control channel. (b) DPV results also show a sign of peak shifting and new peaks appearing at approximately 0.4 V. Figure 5.60 (e) and (f) display the functionalisation of pDAN on the graphene surface forming 2 peaks representing the redox behaviour of the amine groups.

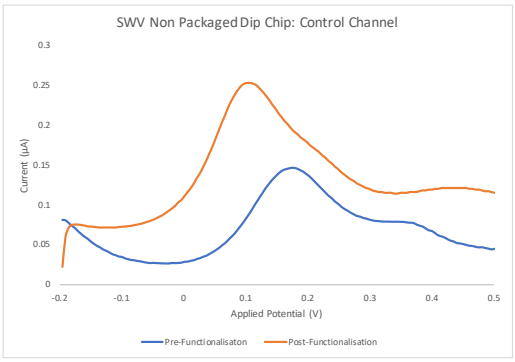


(a) SWV: Channel 1 (Au)

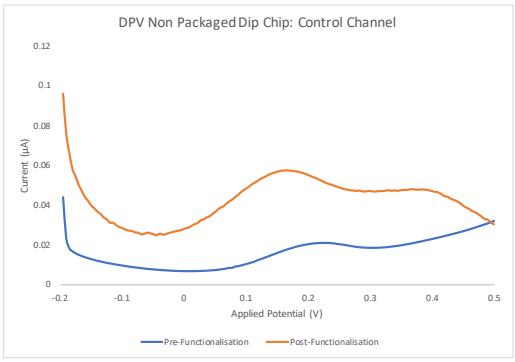


(b) DPV: Channel 1 (pDAN)

Figure 5.58: (a) SWV of graphene channel 1 pre-functionalisation (blank) and post Au electro-depostion showing large peak response at 0.19 - 0.2 V.(b) DPV result showing similar trend to SWV for Au functionalised surface.

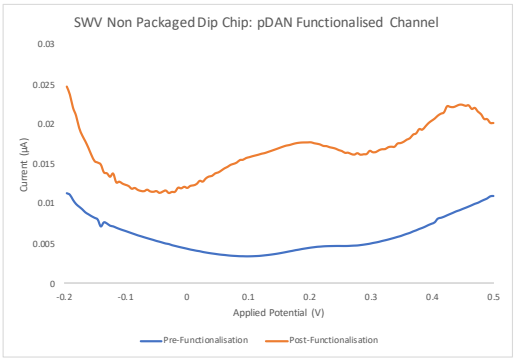


(a) SWV: Channel 2 (blank)

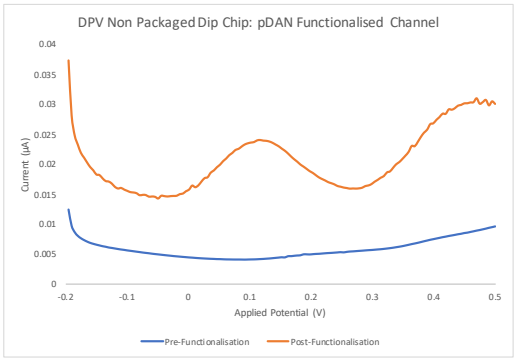


(b) DPV: Channel 2 (blank)

Figure 5.59: (a) SWV of the control channel shows a small increase in current for the graphene peak post functionalisation but also shows additional peaks at 0.1 and 0.45 V. This could be due to contamination of the channel with Au/DAN. (b) The DPV result confirms the additional peaks seen after the other channels had undergone functionalisation.



(a) SWV: Channel 3 (pDAN)



(b) DPV: Channel 3 (pDAN)

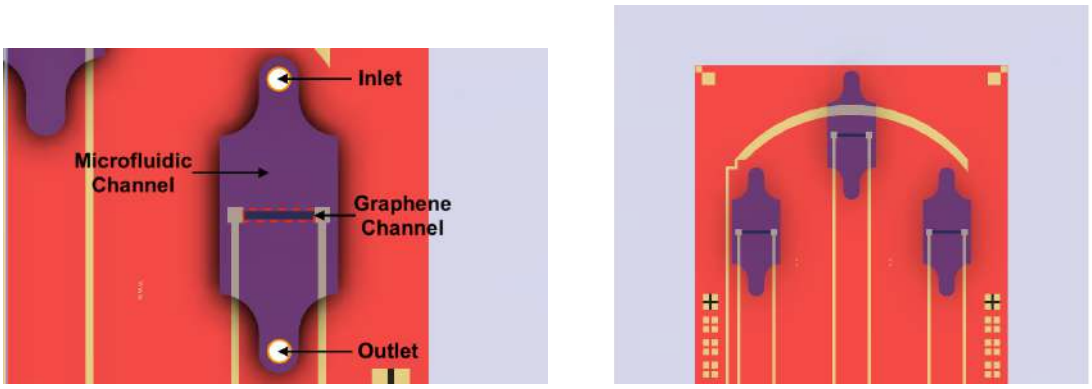
Figure 5.60: (a) SWV result of pDAN functionalised channel shows two additional peaks as a result of the amine groups of the pDAN surface at 0.11 V and 0.45. (b) DPV result confirms additional peaks seen in SWV result.

This method of multiplexing the graphene channels appears to be effective in terms of readable peak shifts due to the functionalisation process. Further research would need to be conducted to create an effective electrochemical based sensor for diagnostic purposes. Early work on pDAN based functionalisation has shown the

potential for binding sensing using enzyme-based bio-receptors to the NH_2 groups of the DAN layer [29]. The difficulty faced with this process is the potential for cross-reactions due to contamination of the graphene surface from the multiple functionalisation solutions. To create a better multiplex platform, the graphene channels must be isolated in the functionalisation solutions individually to prevent cross-contamination.

Multiplex Packaging

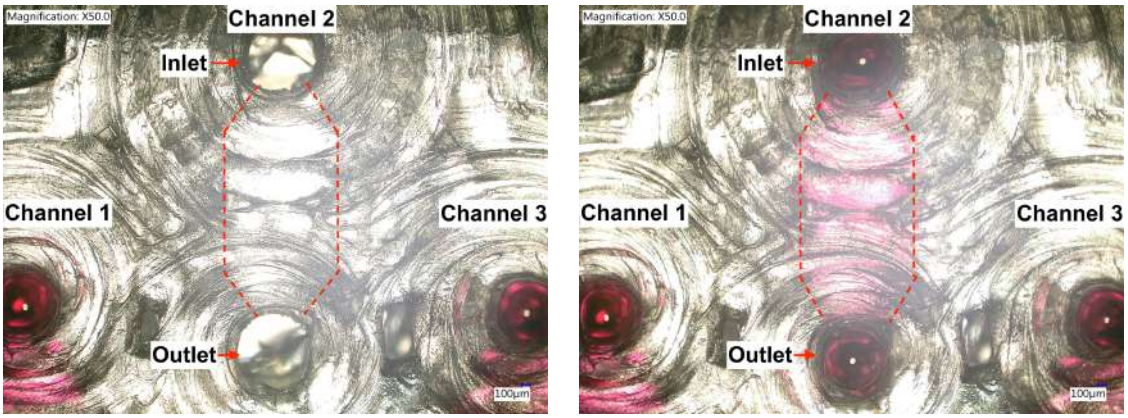
To deliver a more stable electrochemical functionalisation process with less cross-contamination of the channels, the Dip Chip: Multiplex (Dip Chip M) design could be combined with a newly designed 3D printed packaging. The design of microfluidic channels in the Dip Chip M package was redesigned to accommodate the additional space used per channel. The inlet and outlet regions were reduced in size to enable the increased distance between them. A better liquid-tight seal to the chip surface and and alignment of the microfluidic channels can be seen in Figure 5.61. Using 3 individual microfluidic channels enables exposure of graphene channels individually to electrochemical functionalisation by blocking the inlet and outlet of the other graphene channels.



(a) (b)

Figure 5.61: (a) Sketch design of microfluidic channel centre top. (b) Alignment of Dip Chip M with microfluidic channels of intended packaging.

The next stage involved file conversion and test printing the microfluidic package, the total print time calculated was 29 minutes and total filament usage 0.32m of. To check the internal microfluidic structures were isolated the central channel (2) was filled with di H_2O and the outer microfluidic channels (1 & 3) were filled sequentially with red food dye (mixed 1:5 di H_2O). Figure 5.62 (a) show the microfluidic cartridge after 2 hours in a sealed container. No signs of cross-contamination could be seen. Figure 5.62 (b) shows the microfluidic channel was then filled with red food colouring to confirm all 3 microfluidic channels are functional.



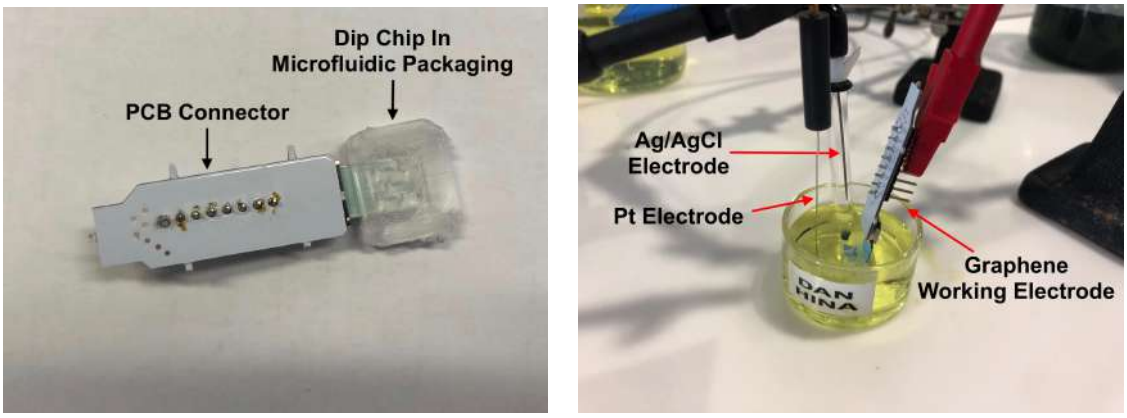
(a) (b)

Figure 5.62: (a) Microfluidic channel 2 containing di H_2O no colour bleeding from surrounding microfluidic channels. (b) Microfluidic channel 1, 2 and three individually containing coloured di H_2O.

Multiplex Functionalisation

The Dip Chip M packaging design was shown to be liquid-tight. The next stage of testing was to repeat the multiplex electrochemical functionalisation process. The design Dip Chip M 3D printed package enabled the attachment of the SD card connector so that it could be used in the electrochemical three-electrode circuit similar to a non-packaged Dip Chip (Figure 5.63). To guarantee that the ionic liquid component of the circuit has made contact with the graphene surface, the solution is first pipetted into the microfluidic channel before full submersion in the

solution.

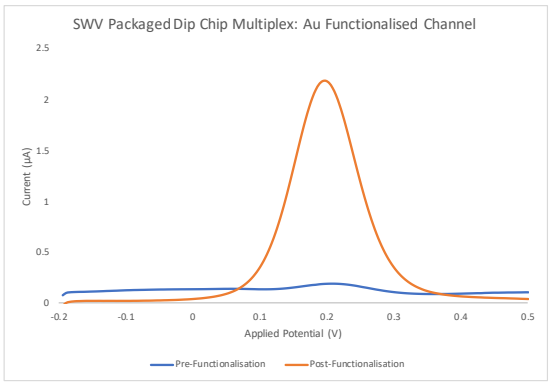


(a) (b)

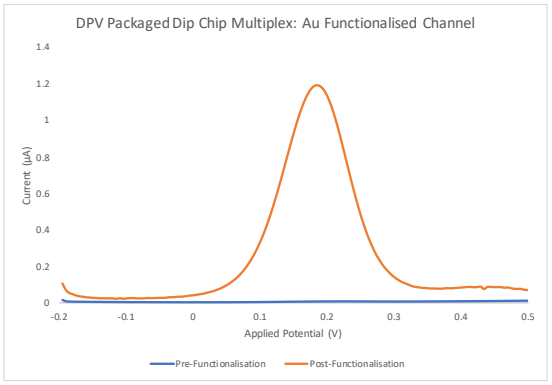
Figure 5.63: (a) Dip Chip M packaged in 3D printed microfluidic, connected to SD card connector PCB. (b) Submerged and packaged Dip Chip M completing the 3 electrode circuit for electrochemical measurements.

During each functionalisation step, the two graphene channels that are to be excluded from the circuit are protected from the solution using a small volume of silicone-based sealant. After functionalisation, the silicone was removed of the inlets and outlets. The resulting channels cannot visually be inspected for functionalisation. To identify functionalisation SWV and DPV were performed using the same sweep parameters as for the unpackaged Dip Chip. The solution was pipetted into each microfluidic channel before submersion of the fully packaged device in the solution. Figure 5.64 (a) and (b) shows the SWV and DPV results for the Au functionalisation of graphene channel 1 both show the same high peak at 0.2 V representing the deposited Au. Figure 5.65 (a) and (b) shows the control channel SWV has an additional peak pre and post-functionalisation between 0.5 - 0.6 V this could represent additional material on the graphene channel or could be caused by a reaction with the COC printed cartridge. The DPV result shows no sign of the additional peaks post-functionalisation this suggests the graphene channel was isolated from the functionalisation chemistries. Figure 5.66 (a) and (b) shows the SWV and DPV for the pDAN functionalised channels contain the same 2 additional

peaks found that represent the amine groups present in the molecule. This suggests both Au electro-deposition and electro-polymerisation of pDAN are possible within a microfluidic package submerged in the electrochemical solution.

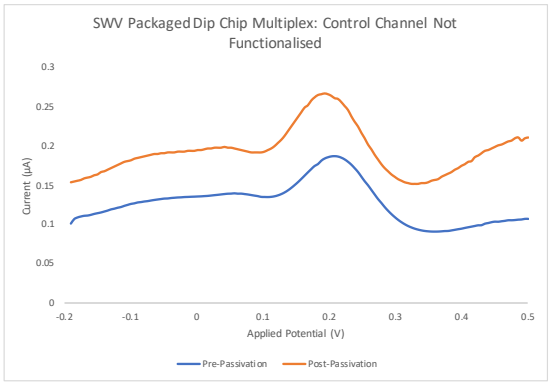


(a) SWV: Channel 1 (Au)

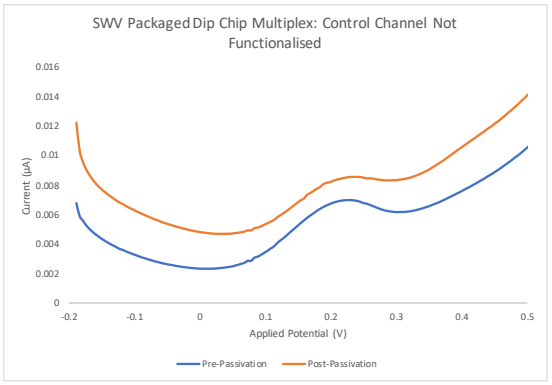


(b) DPV: Channel 1 (Au)

Figure 5.64: (a) SWV of graphene channel 1 pre-functionalisation (blank) and post Au electrodepostion showing large peak response at 0.19 V. (b) DPV result confirming Au peak post functionalisation.

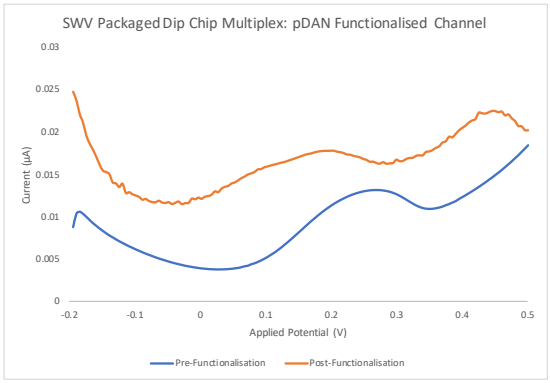


(a) SWV: (Channel 2 (blank))

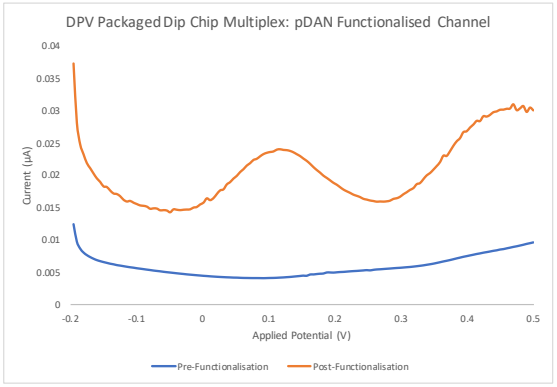


(b) DPV: Channel 2 (blank)

Figure 5.65: (a) SWV of blank graphene, pre-functionalisation shows secondary peak at 0.5 - 0.6 V this could be a result of the COC polymer in the solution. Post-functionalisation there is a small current increase but no additional peaks present on graph. (b) DPV result does not show the additional peak pre or post-functionalisation, overall current does increase but no additional peaks are present.



(a) SWV: Channel 3 (pDAN)



(b) DPV: Channel 3 (pDAN)

Figure 5.66: (a) SVW result for pDAN functionalisation shows 2 additional peaks representing the amine functional groups of pDAN. (b) DPV result confirms pDAN functionalisation of graphene channel 3.

This method of multiplex functionalisation shows promise regarding isolation of each graphene channel within individual liquid solutions. With better alignment systems for the microfluidic packaging, the graphene channels could be miniaturised along with the microfluidic channels. This would allow for a greater number of graphene channels per chip and increase the multiplex capacity of a single chip.

Blood Separation Microfluidic Device

Regarding development of a packaged blood clotting diagnostics sensor, the ideal system for measuring diagnostic analytes in blood would be to apply human serum (Platelet poor plasma with post-coagulation) to the graphene surface. This would limit the interaction of practically all cells present in the blood. This increases the likelihood of detection by eliminating a majority of not useful mass in the sample as well as reducing the effects of physisorption on the graphene surface by relatively high mass blood cells.

However, for clotting based diagnostics a number of the molecules involved in coagulation be removed if human serum was used for detection. Instead, plasma has been chosen as the target fluid sample for preparation that would be required for a

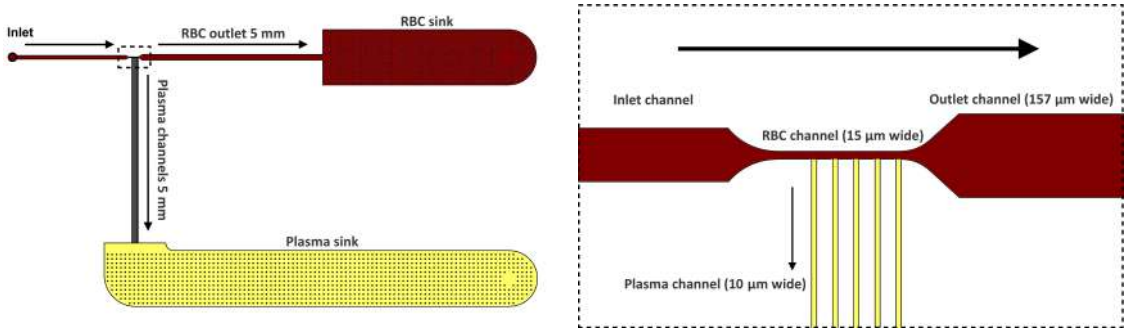
clotting diagnostic molecular assay sensor. This would retain the clotting molecules that would be the target of clotting diagnostic assays whilst also removing the majority of cellular mass from the sample, thus improving detection accuracy.

The standard methodology to produce platelet-poor plasma (PPP) containing < 10 X $10^3/\mu$L platelets, would be to centrifuge citrated whole blood samples. This methodology is also used to generate platelet-rich plasma (PRP) also used for diagnostic assays [31]. There are microfluidic devices based on small spinning disks like centrifuges [32]. However, these systems often require multiple machines with motors and moving parts. Equally these systems are not as compact as simple laminar lab on chip style microfluidic that enables smaller packaging and point of care style systems [33].

Multiple methodologies have been applied to blood separation microfluidics, in addition to centrifugal based systems. These include filtration, sedimentation, capillary hydrodynamics as well as active methodologies [34]. These methods have been reviewed in the Blood Separation Microfluidics section of the Literature Review Chapter. The methods involving filtering and hydrodynamic approaches have the best potential for point of care based approach, due to their high speed and limited device complexity.

Blood Separation Device 1

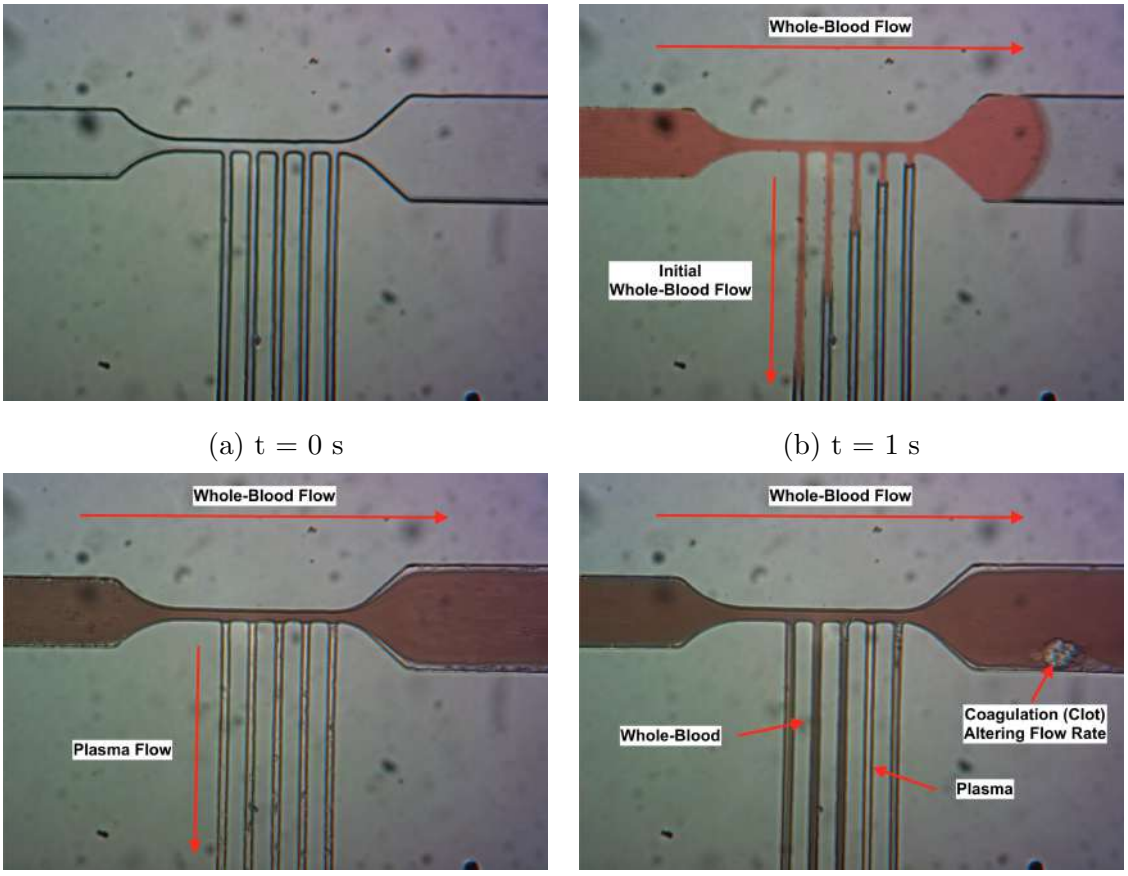
The first microfluidic design trialled was based on fluid resistance and flow rate ratio control. Figure 5.67 shows this system with 1 inlet for whole blood, 1 blood plasma outlet and 1 concentrated whole blood outlet schematic. A test design geometry and fluid resistances was sourced from the literature [35]. The design was created in AutoCAD and a photomask was purchased from (JD PhotoData, UK). The microfluidic device had channels with dimensions of 10 μm. Additional plasma extraction would change the flow rate ratio, increase the flow rate through the plasma extraction channels allowing more blood cells to flow down them and decreasing the separation efficiency.



(a) (b)

Figure 5.67: (a) The outer regions of the microfluidic device where inlet outlet holes will connect to exterior tubing. (b) Separation Region of microfluidic device with 5 plasma extraction channels perpendicular to "whole-blood flow" channel.

The recommended flow rates for these size channels trialled within the literature were between 10 μl/hour and 5 μl/min. A series of flow rates including 10 μl/hour, 100 μl/hour and 1000 μl/hour were tested using citrated whole blood. The first test of the device was performed at 100 μl/hour. Figure 5.68 shows time-lapse images of the separation process, the extraction channel region can be seen effectively separating plasma for the first 15 s. After this period coagulation appears in the main flow channel disrupting the geometry and flow rate.



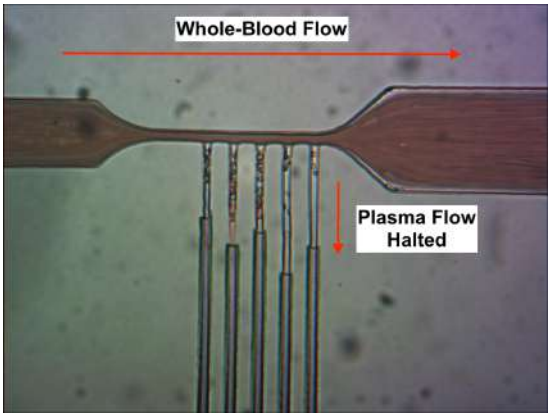
(a) t = 0 s (b) t = 1 s

(c) t = 15 s (d) t = 22 s

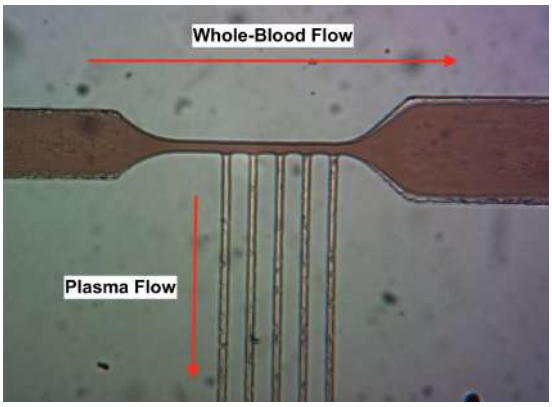
Figure 5.68: (a) Time point 0s: Blood has yet to reach the extraction channels. (b) Time point 1 s: Whole blood has reached the extraction channels, initially blood cells also travel down extraction channels. (c) Once flow rates stabilise at time point 15 s, plasma passes through extraction channels. (d) Coagulation occurs visibly close to the extraction channel, disrupting flow. Blood cells can be seen travelling down the extraction channel.

The flow rates chosen were then tested on new microfluidic devices. Figure 5.69 shows the resulting separation at the 5 extraction channels for each speed after 10 s of flow. The 10 μl/hour device did not produce a large flow rate through the extraction channels, and post 20 s, the device did not extract plasma effectively. The 100 μl/hour device showed signs of coagulation after 15 s resulting in a change of flow rate. Similarly the 1000 μl/hour device showed signs of coagulation and

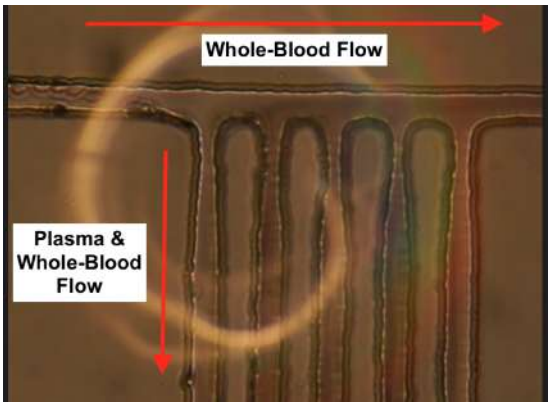
irregular flow after 16 s.



(a) t = 15 s



(b) t = 15 s



(c) t = 15 s

Figure 5.69: Time-lapse images of blood separation device tested with whole blood. (a) Flow rate of 10 μl/hour showed signs of physical blocking at 10 s. (b) Flow rate of 100 μl/hour shows plasma flow. (c) Flow rate of 1000 μl/hour plasma separation channels high flow rate containing plasma and red blood cells.

The resulting separated plasma was not able to be collected in any measurable quantity. The device design would not enable the collection of a sufficient volume for cell counting due to the small channel and sample volumes. Additionally, this design was inefficient in terms of fabrication, as the small microfluidic channel dimensions resulted in low yields and blockages. Microfluidic channels with larger internal dimensions would be less affected by coagulation, using an increased flow rate through the device, a large enough volume of plasma could be obtained for analyses.

Blood Separation Device 2

The second device design is based on pinched flow fractionation (PFF). PFF can be used to separate particles out based on size, within a laminar flow microfluidic channel. Figure 5.70 shows the blood separation microfluidic design, the whole blood inlet channel constricts in width "Pinched", before broadening out into a wider channel. Smaller particles will move out towards the walls of the channel. As the channel broadens, this separates the whole blood based on particle size. A plasma extraction channel is placed at the immediate edge of the broadened region see design.

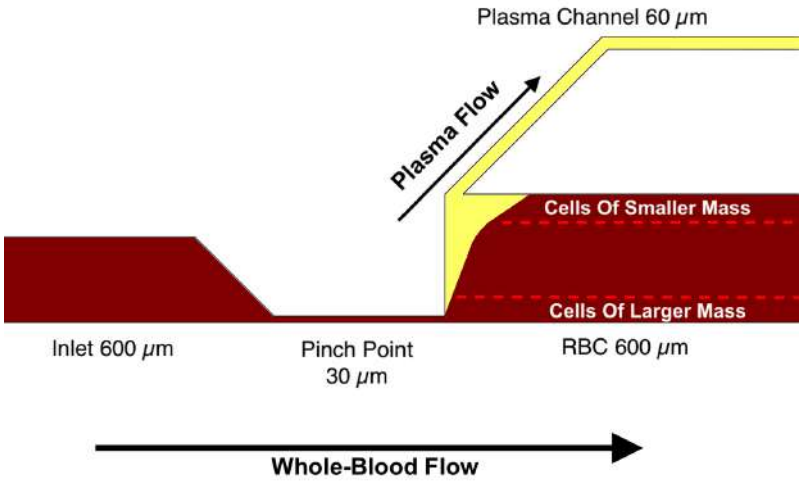
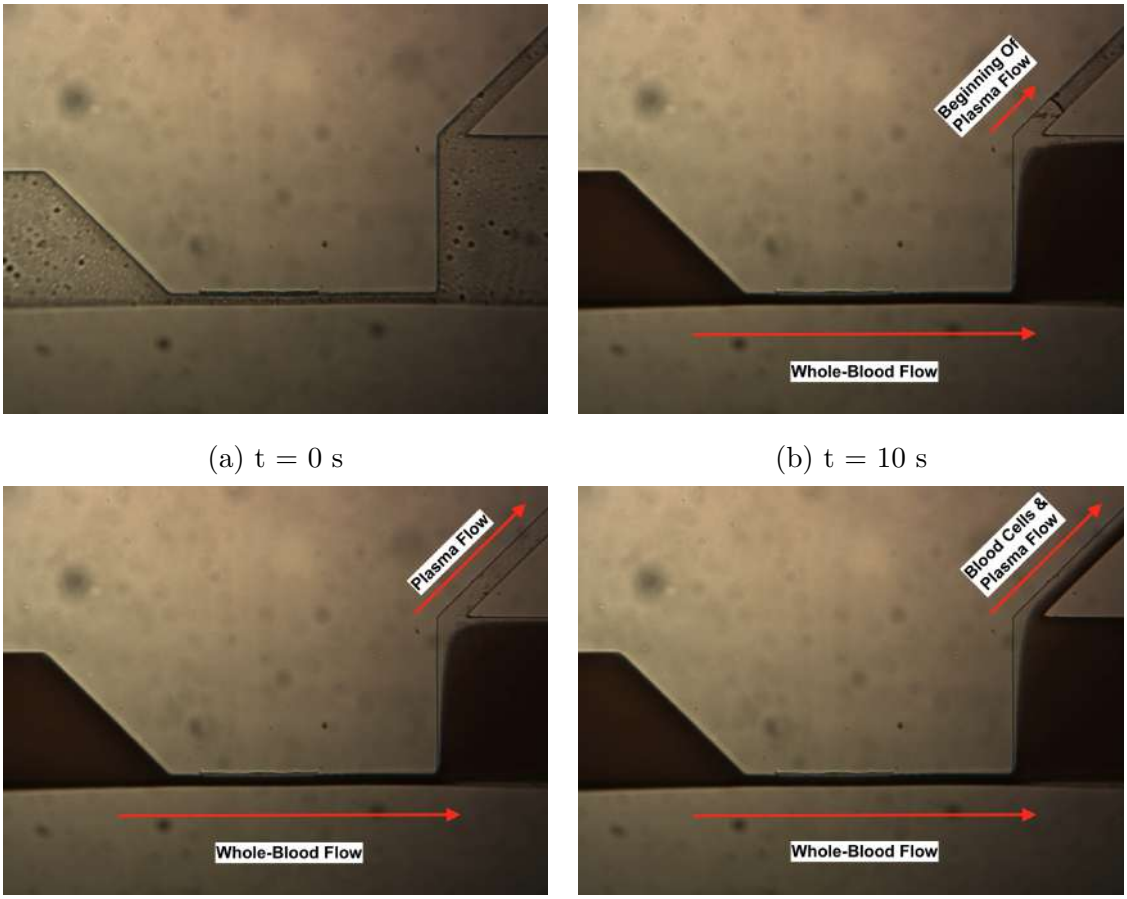


Figure 5.70: Blood separation PFF design showing whole blood flowing left to right. The channel height (40 μm), channel widths are annotated on the design.

The literature reviewed suggested this design could optimally separate blood at both room and body temperature, based on a flow resistance ratio between the plasma extraction channel and the red blood cell (RBC) channel of 1:5.7. There was no optimisation of this ratio but the higher of the two ratios tested was more efficient [36]. To investigate this design further the plasma extraction channel length was varied from 16 mm to 34 mm. This produced flow resistance ratios 1:6.9, 1:13, 1:18.9 and 1:24.1. The flow rate of 200 μl/min was used to gather a minimum sample

of 20 μl. Figure 5.71 shows the plasma separation by PFF devices at different time points.



(a) t = 0 s (b) t = 10 s

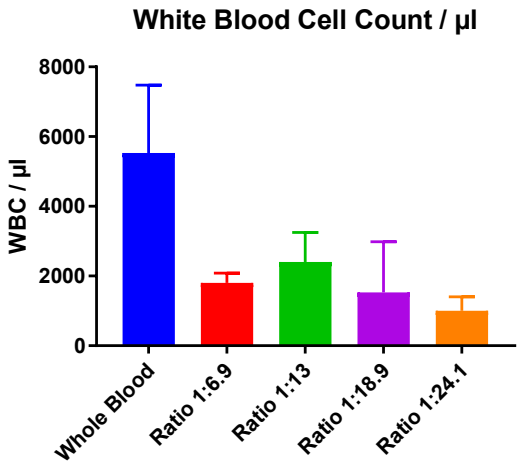
(c) t = 150 s (d) t = 160 s

Figure 5.71: (a) Time point 0 s: Blood has yet to reach the pinch point. (b) Time point 10 s: Whole blood has reached the broadened channel region, the plasma extraction partially stalled as flow continues down RBC channel. (c) Time point 150s: Plasma flows through extraction channel towards collection tube. (d) Post-150 s Coagulation has occurred within the RBC channel disrupting flow, blood cells can be seen travelling down extraction channel.

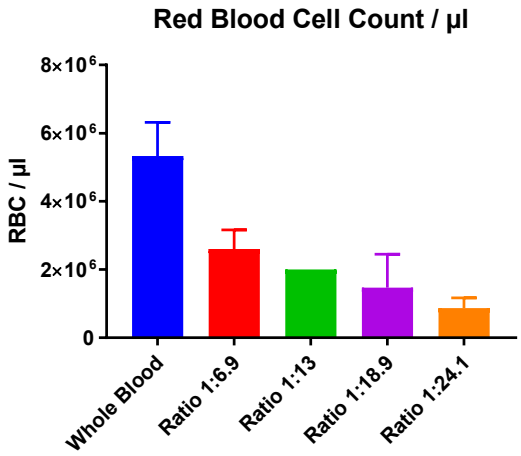
Each flow resistance design was fabricated and tested using three devices, plasma was extracted by connecting the plasma extraction outlet via microfluidic tubing. After a run time of 180 s per microfluidic device, the plasma extracted into the microfluidic tubing was collected into a sealable 1.5 ml Eppendorf tube. The samples

were diluted 20-fold in PBS to produce a volume of 400 μl. This allowed content analyses using a haematology analyser, whole-blood was used as the control. The total cell count per μl was then extrapolated out from the diluted sample data.

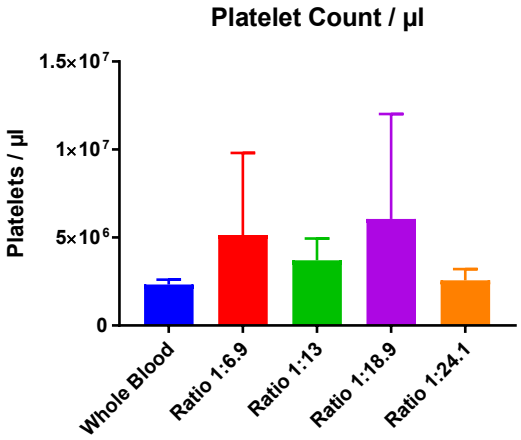
Figure 5.72 (a) shows White Blood Cell count (WBCs) for each flow rate ratio. Each flow rate ratio produces a sample with fewer WBCs than the whole blood sample. The highest flow rate ratio appears to produce the purest plasma although. Figure 5.72 (b) shows Red Blood Cell count (RBC's) for each flow rate ratio, the higher flow rate ratio also produces plasma with the fewest RBC's, suggesting the higher the flow rate ratio the purer the plasma sample. Figure 5.72 (c) shows the total platelet count per sample, no clear trend can be be determined, which would suggest the platelets were not filtered out by the microfluidic separation device. Platelet count was higher in the separated samples meaning the PFF separation process does reduce the total platelet count compared to whole blood.



(a)



(b)



(c)

Figure 5.72: (a) White blood cell count performed by dilution of microfluidic sample measured by haematology analyser. (b) Red blood cell count performed by dilution of microfluidic sample measured by haematology analyser. (c) Platelet count performed by dilution of microfluidic sample measured by haematology analyser.

The microfluidic separation device 2 shows more promise than device 1 as measurable samples were gathered over extended separation times. Although device 2 could not separate platelet cells it was able to reduce the total RBCs and WBCs which make up the majority of the mass in whole blood. Future work looking at filtration and capillary action microfluidic could also be beneficial for a point of care

system. As this would remove the requirement of syringes and flow rates for the sample to be separation, but does rely on a slower blood separation system.

5.4 Summary

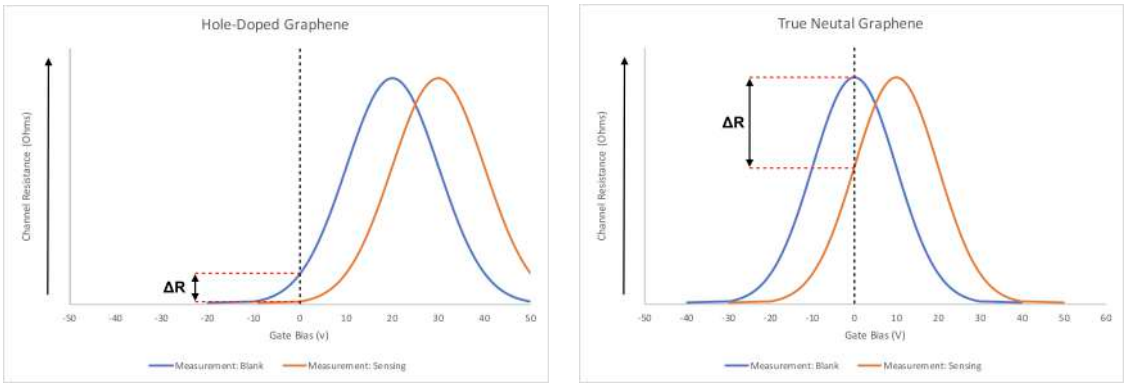
With regards to the passivation processes developed, the use of a photoresist passivation layer is an incredibly attractive approach for research-level development. The single processing step is efficient time and resources. Using permanent photoresists such as the EpoClad resist (Micro Resist Tech GmbH, Germany) which is chemically inert and requires minimal time for solvent-based processing. The difficulty with photoresist processing on graphene is that the epoxy and carbon residues from the photoresist adhere to the graphene surface Cleaning processes are difficult to develop long solvent exposures can damage or even delaminate the graphene surface, whilst using a plasma or sputtering process will cause damage.

The only available process for cleaning is the use of inorganic acids. However, this method of cleaning is not compatible with photoresist-based passivation layers or with certain metal electrode structures, depending on the acid concentration. Upscaling graphene sensor technology would not be practical using a photoresist based passivation layer. This is due to the different methods of functionalisation (some H_2SO_4 based) for the sensor. Overall photolithographic methods, although reasonable for certain lab-based research, are not a practical passivation material for the graphene sensor platform.

In comparison, deposited dielectric films require additional process steps and complexity but the resulting passivation films are generally inert to all functionalisation chemistries. Additionally, photoresist layers do not come directly in contact with the graphene surface, as they are patterned onto the dielectric layer, This reduces total organic/polymer residues on the graphene surface. PECVD deposited dielectric layers have the advantage of fast deposition rates and a choice of SiO_2 (most common dielectric choice for graphene fabrication). The difficulties of the PECVD are the high temperatures, plasma and high power plasma generation which

results in damage to any exposed graphene. To protect the graphene through this process, additional process steps are required to create a protective sacrificial layer on top of the graphene surface. When these additional process steps are taken into account the time advantages of the PECVD systems are removed.

The MVD deposited Al_2O_3 via an ALD style 2 step precursor deposition proved the most promising technique. Although the deposition rate for MVD Al_2O_3 were orders of magnitude different to the PECVD, the total thickness required for electrical isolation is much lower than the PECVD SiO_2. The ability to directly deposit the Al_2O_3 onto the graphene surface without damage, and its potential "healing" of the graphene's chemical damage suggests Al_2O_3 passivation produces graphene with a lower level of contamination or structural damage. The use of MVD Al_2O_3 creates a chemically resistant high κ dielectric layer, without introducing damage or residue to the graphene surface. Beyond these benefits, the change in Dirac point (charge neutrality point) post-passivation creates a clearly defined peak with high gradient closer to 0 V. This will increase the change seen in two-terminal resistance measurement by functionalisation and finally sensing stages. In theory, this will produce a graphene FET sensor with overall higher sensitivity to surface/doping modification (Figure 5.73).



(a) (b)

Figure 5.73: Dirac point measurements of a graphene sensor (hole-doping sensing response)(a) Measurement blank and post-sensing of a hole-doped graphene channel (ΔR small). (b) Measurement blank and post-sensing of a true neutral graphene channel (ΔR large).

Regarding packaging of the Dip Chip for functionalisation and later for sensing, a PDMS soft lithography approach is highly useful for microfluidics focused research, the only limiting factor is the requirement for photomask purchasing which can limit prototyping and new iterations of designs. PDMS can also be used for all dimensions of microfluidic channels required including sub μm scales meaning it could potentially be used for miniaturised graphene sensor designs. The primary issue with PDMS based microfluidic chips was the bonding and alignment to the graphene devices. The direct etching approach solves the alignment difficulties but also comes with bonding drawbacks. Further work would be required to reverse the effects of the acid treatment of the PDMS if possible, to make PDMS etched microfluidic structures an unscalable solution for miniaturised graphene microfluidic packaging. Until then further work examining other packaging methods have been investigated.

This severely limited the fabrication and testing of these devices. In comparison, the 3D printed microfluidic cartridges enable rapid prototyping of more designs faster than PDMS. Alignment of the device although not adjustable mid-print could be achieved with the use of 3D printed alignment slots. This process of packaging

proved the most reliable as functionalisation tests of graphene devices in packaging could be performed. The functionalisation processes of deposition and cleaning will need to be optimised in future work, to deposit the required quantity/thickness of Au s an optimised thickness of pDAN on the graphene surface. The microfluidic packaging did not impede the functionalisation process and was able to isolate the control channel improving the process overall.

Using microfluidic chips for sample pre-processing is becoming more common in commercial biomedical devices and is no longer just a tool for research. Blood separation is a standard process in hospital laboratories using large centrifuge machines. This level of blood separation was not achieved with either of the microfluidic device designs. However, blood cell separation was achievable, tuning the flow rate ratio could achieved higher levels of blood cell separation.

Bibliography

[1] W Miesbach, J Schenk, S Alesci, and E Lindhoff-Last. Comparison of the fibrinogen clauss assay and the fibrinogen pt derived method in patients with dysfibrinogenemia. *Thrombosis research*, 126(6):e428–e433, 2010.

[2] Sabine Eichinger, Erich Minar, Christine Bialonczyk, Mirko Hirschl, Peter Quehenberger, Barbara Schneider, Ansgar Weltermann, Oswald Wagner, and Paul A Kyrle. D-dimer levels and risk of recurrent venous thromboembolism. *Jama*, 290(8):1071–1074, 2003.

[3] J Jespersen, RM Bertina, and F Haverkate. Laboratory techniques in thrombosis - a manual, 1999.

[4] Christopher J Hamilton and Markus W Germann. Folding and base pairing of a fibrinogen specific dna aptamer. *Colonial Academic Alliance Undergraduate Research Journal*, 2(1):11, 2011.

[5] A Kappel and M Ehm. Immunoassays for diagnosis of coagulation disorders. *Hämostaseologie*, 30(04):194–201, 2010.

[6] Ryan Michael Bigham. Development of process technology for silicon and graphene biosensor devices. Technical report, Swansea University, 2019.

[7] Behiye Boyarbay Kantar, Muhittin Ozturk, and Hidayet Cetin. The effects of lithographic residues and humidity on graphene field effect devices. *Bulletin of Materials Science*, 40(1):239–245, 2017.

[8] Jinpyo Hong, Min Kyu Park, Eun Jung Lee, DaeEung Lee, Dong Seok Hwang, and Sunmin Ryu. Origin of new broad raman d and g peaks in annealed graphene. *Scientific reports*, 3:2700, 2013.

[9] Luca Banszerus, Hendrik Janssen, Martin Otto, Alexander Epping, Takashi Taniguchi, Kenji Watanabe, Bernd Beschoten, Daniel Neumaier, and Christoph

Stampfer. Identifying suitable substrates for high-quality graphene-based heterostructures. *2D Materials*, 4(2):025030, 2017.

[10] Guoqing Chen. Method and structure for low-k interlayer dielectric layer, March 24 2009. US Patent 7,507,656.

[11] C Reyes-Betanzo, SA Moshkalyov, MA Pavanello, ACS Ramos, and JW Swart. Plasma etching of si3n4 with high selectivity over si and sio2. In *Proceedings of SBMicro2001-XVI International Conference on Microelectronics and Packaging*, pages 70–75, 2001.

[12] Francis Ko, Sandy Chen, and Charlie Lee. Plasma enhanced method for increasing silicon-containing photoresist selectivity, April 1 2003. US Patent 6,541,361.

[13] Jianyu Fu, Haiping Shang, Zhigang Li, Weibing Wang, and Dapeng Chen. Thermal annealing effects on the stress stability in silicon dioxide films grown by plasma-enhanced chemical vapor deposition. *Microsystem Technologies*, 23(7):2753–2757, 2017.

[14] Tommi Kaplas, Vytautas Jakstas, Andrius Biciunas, Algimantas Luksa, Arunas Setkus, Gediminas Niaura, and Irmantas Kasalynas. Effect of high-temperature annealing on graphene with nickel contacts. *Condensed Matter*, 4(1):21, 2019.

[15] Kirt R Williams, Kishan Gupta, and Matthew Wasilik. Etch rates for micromachining processing-part ii. *Journal of microelectromechanical systems*, 12(6):761–778, 2003.

[16] Andrea Cabrero-Vilatela, Jack Allen Alexander-Webber, AA Sagade, Adrianus Indrat Aria, Philipp Braeuninger-Weimer, Marie-Blandine Martin, RS Weatherup, and Stephan Hofmann. Atomic layer deposited oxide films as protective interface layers for integrated graphene transfer. *Nanotechnology*, 28(48):485201, 2017.

[17] Anderson D Smith, Karim Elgammal, Xuge Fan, Max C Lemme, Anna Delin, Mikael Råsander, Lars Bergqvist, Stephan Schröder, Andreas C Fischer, Frank

Niklaus, et al. Graphene-based co2 sensing and its cross-sensitivity with humidity. *RSC Advances*, 7(36):22329–22339, 2017.

[18] Sang-Min Kim, Youngji Cho, Jae-Hyun Kim, Hak-Joo Lee, Jun-Mo Yang, Seung-Mo Lee, et al. Healing defective cvd-graphene through vapor phase treatment. *Nanoscale*, 6(11):5639–5644, 2014.

[19] Nathan Ward, Xiaoyi Mu, Gustavo Serrano, Elizabeth Covington, Cagliyan Kurdak, Edward T Zellers, Andrew J Mason, and Wen Li. Adaptable chip-level microfluidic packaging for a micro-scale gas chromatograph. In *2012 7th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, pages 57–60. IEEE, 2012.

[20] Preetha Jothimuthu, Andrew Carroll, Ali Asgar S Bhagat, Gui Lin, James E Mark, and Ian Papautsky. Photodefinable pdms thin films for microfabrication applications. *Journal of Micromechanics and Microengineering*, 19(4):045024, 2009.

[21] Mehmet Ozgur, Michael Pedersen, and Michael Huff. Comparison of the etch mask selectivity of nickel and copper for a deep, anisotropic plasma etching process of silicon carbide (sic). *ECS Journal of Solid State Science and Technology*, 7(2):P55–P59, 2018.

[22] J Garra, T Long, J Currie, T Schneider, R White, and M Paranjape. Dry etching of polydimethylsiloxane for microfluidic systems. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 20(3):975–982, 2002.

[23] Gerardo Perozziello. *Packaging of microfluidic systems: A microfluidic motherboard integrating fluidic and optical interconnections*. Technical University of Denmark, 2008.

[24] RWRL Gajasinghe, SU Senveli, S Rawal, A Williams, A Zheng, RH Datar, Richard J Cote, and Onur Tigli. Experimental study of pdms bonding to various

substrates for monolithic microfluidic applications. *Journal of Micromechanics and Microengineering*, 24(7):075010, 2014.

[25] Michael W Toepke and David J Beebe. Pdms absorption of small molecules and consequences in microfluidic applications. *Lab on a Chip*, 6(12):1484–1486, 2006.

[26] Niall P Macdonald, Joan M Cabot, Petr Smejkal, Rosanne M Guijt, Brett Paull, and Michael C Breadmore. Comparing microfluidic performance of three-dimensional (3d) printing platforms. *Analytical chemistry*, 89(7):3858–3866, 2017.

[27] Rafał Walczak and Krzysztof Adamski. Inkjet 3d printing of microfluidic structures on the selection of the printer towards printing your own microfluidic chips. *Journal of Micromechanics and Microengineering*, 25(8):085013, 2015.

[28] Shun Mao, Ganhua Lu, Kehan Yu, Zheng Bo, and Junhong Chen. Specific protein detection using thermally reduced graphene oxide sheet decorated with gold nanoparticle-antibody conjugates. *Advanced materials*, 22(32):3521–3526, 2010.

[29] Anitha Devadoss, Rhiannan Forsyth, Ryan Bigham, Hina Abbasi, Muhammad Ali, Zari Tehrani, Yufei Liu, Owen Guy, et al. Ultrathin functional polymer modified graphene for enhanced enzymatic electrochemical sensing. *Biosensors*, 9(1):16, 2019.

[30] China Y Lim, Nicholas A Owens, Ronald D Wampler, Yixin Ying, Jennifer H Granger, Marc D Porter, Makoto Takahashi, and Katsuaki Shimazu. Succinimidyl ester surface chemistry: implications of the competition between aminolysis and hydrolysis on covalent protein immobilization. *Langmuir*, 30(43):12868–12878, 2014.

[31] B Boneu, G Bes, H Pelzer, P Sie, and H Boccalon. D-dimers, thrombin antithrombin iii complexes and prothrombin fragments 1+ 2: diagnostic value

in clinically suspected deep vein thrombosis. *Thrombosis and haemostasis*, 65(01):028–032, 1991.

[32] Ju-Nan Kuo and Xuan-Fu Chen. Plasma separation and preparation on centrifugal microfluidic disk for blood assays. *Microsystem Technologies*, 21(11):2485–2494, 2015.

[33] Witold Szymon Mielczarek, EA Obaje, TT Bachmann, and Maïwenn Kersaudy-Kerhoas. Microfluidic blood plasma separation for medical diagnostics: is it worth it? *Lab on a Chip*, 16(18):3441–3448, 2016.

[34] Siddhartha Tripathi, YV Bala Varun Kumar, Amit Prabhakar, Suhas S Joshi, and Amit Agrawal. Performance study of microfluidic devices for blood plasma separation - a designer's perspective. *Journal of Micromechanics and Microengineering*, 25(8):084004, 2015.

[35] Sung Yang, Akif Ündar, and Jeffrey D Zahn. A microfluidic device for continuous, real time blood plasma separation. *Lab on a Chip*, 6(7):871–880, 2006.

[36] Angeles Ivón Rodríguez-Villarreal, Martin Arundell, Manuel Carmona, and Josep Samitier. High flow rate microfluidic device for blood plasma separation using a range of temperatures. *Lab on a Chip*, 10(2):211–219, 2010.

Chapter 6

Graphene Sensor Real-Time Measurements

6.1 Introduction

Thus far the work within this thesis has developed fabrication processes for graphene sensor chips to produce sensors with the lowest channel resistance. This has involved ensuring the graphene channels have a high degree of structural integrity (SP^2 bonds) and minimal residue on the channels.

Following optimisation of the graphene Dip Chip fabrication materials and processes, electrical characterisation and sensing was performed. The results were compared between of the optimised Dip Chip using Post-Transfer fabrication process flow and MVD Al_2O_3 passivation (PT-MVD Chip) and the previously established Pre-Transfer fabrication process flow with screen-printed ink passivation process (PT-SPI Chip) [1].

To fully compare the electrical and sensing performance of the graphene Dip Chip the electrical setup (grounded silicon, Faraday cage ect.) and timescales for measurement were optimised for each chip. Following the electrical setup and timescale optimization, the resistance response of the graphene channels for both the PT-MVD Chip and PT-SPI Chip were measured in air, di H_2O and other solvents that the graphene comes into contact with during cleaning, functionalisation and sensing steps. These include IPA and Acetone solvents used for cleaning and phosphate-buffered saline (PBS). This was then used to characterise the responses at each stage of the experiment for each chip. Resistance measurements were performed periodically at each stage of the experiment for both chips to measure the response to each

step in real-time.

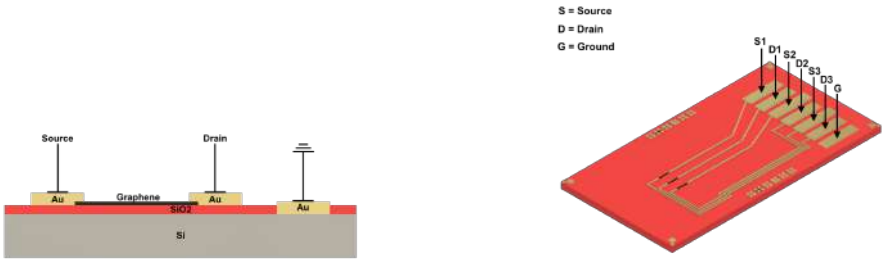
The main goal of the work within this thesis was to develop a sensor to binding/sensing of a target antigen in real-time. This allows real-time feedback for sensor optimisation for a range of targets/uses in future. The response data from the PT-MVD Chip was used to design an experiment for real time quantitative sensing of αthrombin protein, spiked in PBS solutions. Thrombin is the key molecule in two of the three main tests in the standard medical coagulation screen (PT and aPTT), making it the analyte target for the sensor tests. A thrombin-aptamer was used as the bio-receptor due to its high affinity and specificity to the αthrombin antigen and the short physical length of the aptamer maintaining proximity to the graphene surface [2]. As the aptamer is chemically synthesised, either end of the DNA sequence can be modified as part of the base-pair additive process. Thrombin-aptamers are well established for testing biological assays and have an open source published sequence [3]. BNP levels are elevated in cases of cardiovascular disease and stroke but for this work the BNP-aptamer is used as a negative control, the BNP-aptamer will not bind the thrombin molecule so any change in resistance seen will be due to physisorption of the αthrombin on the graphene surface [4]. The Aptamer's purchased (Base-Pair Bio, USA), were synthesised with a pre-conjugated pyrene molecule at the base 5' end to allow for π-π stacking directly on the graphene surface. Thus, no additional functionalisation steps were required. The final part of this chapter highlights the results of the real-time IV measurements and resistance change due to target protein binding to the functionalised graphene surface.

6.2 Materials & Methodology

6.2.1 Real-Time IV Measurement Setup

IV measurement were performed on graphene channel Dip Chip sensors with the bulk silicon grounded, the grounded silicon setup was used to reduce electrical noise during the two-terminal (source drain) measurements (Figure 6.1. Parameters for

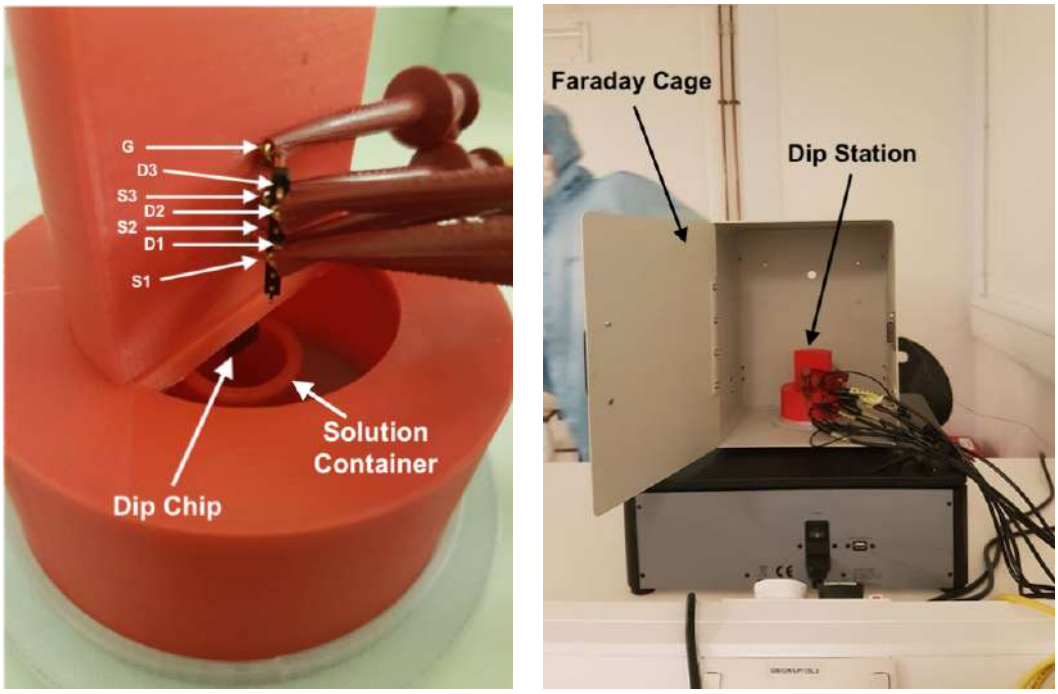
real-time IV measurements (voltage sourced, step time ect) can be found in section 3.11.2.



(a) (b)

Figure 6.1: (a) Infographic of two-terminal IV measurement performed on graphene Dip Chip. (b) PCB Connector pin connections Dip Chip in Dip Station rig

A custom holder (Dip Station) was designed to enclose and interconnect with the PCB Connector, Dip Chips can thus be suspended at a set height in solution (Figure 6.2). The custom holder and sample pot were placed inside a Faraday cage during the real time measurements. The PCB Connector was connected via BNC (Bayonet Neill–Concelman) hook clip cables (RS Components, UK) fed through the Faraday cage via slits in the side panel. Electrical IV measurements were made using three separate Source Measurement Unit (SMU) across two Keithley 2636B Source Measure Unit (Tektronix, USA).



(a) (b)

Figure 6.2: (a) Hook clips connected to the header pins of SD Card PCB. Through the housing window, suspended Dip Chip is connected to SD Card PCB Connector, supported inside housing unit. Housing unit contains sample pots for liquid solution testing. (b) Housing and connection cables connected inside Faraday cage for electrical shielding during experiments.

6.2.2 Gated FET Meaurement

To identify the Dirac point (charge neutrality point) of a Dip Chip graphene channel, gated FET-style measurements were performed on the Dip Chip. The IV probe station is used to probe the electrical contact pads connected to a single graphene channel (source and drain) using a single Keithley SMU (SMU-A). The bulk silicon of the chip was connected via an electrical probe to a second Keithley SMU (SMU-B). Parameters for real-time IV measurements (voltage sourced, step time ect) can be found in section 3.11.2.

6.2.3 Real-Time Data Analyses

Files for real-time measurements were processed in Excel (Microsoft, USA). Resistance was calculated using the equation R = V / I and plotted with time.

Rate Of Change In Resistance Calculations

The rate of change in resistance of the real-time resistance data was calculated by Excel function "SLOPE" which calculates the linear regression of the x y coordinates.

Real-Time Data Normalisation

Graphene resistance values of graphene have a large range (from 3 kΩ - 15 kΩ). Visualisation of the real-time resistance change of multiple graphene channels on a single graph is therefore impractical. Normalisation of the data converts all input data to a common scale with an average of 0 and a standard deviation of 1. Normalisation equation can be found in the Appendix.

Normalisation values were calculated in Excel (Microsoft, USA) using Real-Time resistance data.

For the sensing experiments the "sample" was selected as the first 10 data prior to the addition of the analyte. This would be the "base-line" of a diagnostic sensor any change due the analyte can then be seen moving away from the base-line.

6.2.4 Testing Of Dip Chip In Real-Time

Firstly, three 9.8 kΩ resistor (RS components, UK) were tested over a 2 hour period inside and outside of the Faraday cage test station, in order to access the background noise of measurement, measurements were repeated five times.

6.2.5 Vacuum - Ambient Experimental Setup

The effect of storing the graphene in vacuum prior to experiments on the resistance and rate of resistance change during real-time measurements was investigated. A set of graphene Dip Chips were stored in cleanroom ambient conditions and a set were stored in a vacuum desiccator. The parameters for the two storage conditions can be seen below.

Vacuum Chips = Graphene Dip Chips were stored in vacuum desiccator (10 mBarr) for 12 hours overnight.

Ambient Chips = Graphene Dip Chips stored in ambient cleanroom conditions (21 °C, 50 % humidity).

IV measurements were performed on vacuum chips within 2 minutes of removal from vacuum desiccator.

6.2.6 Di H_2O Submersion & Drying Experimental Setup

Dip Chips were submerged in a 5ml ABS plastic (acrylonitrile butadiene styrene) container filled with 4ml of di H_2O Dip Station. The water level was then 4-5 mm above the graphene channels whilst submerged. The minimum submersion time of 2 hours was used prior to drying.

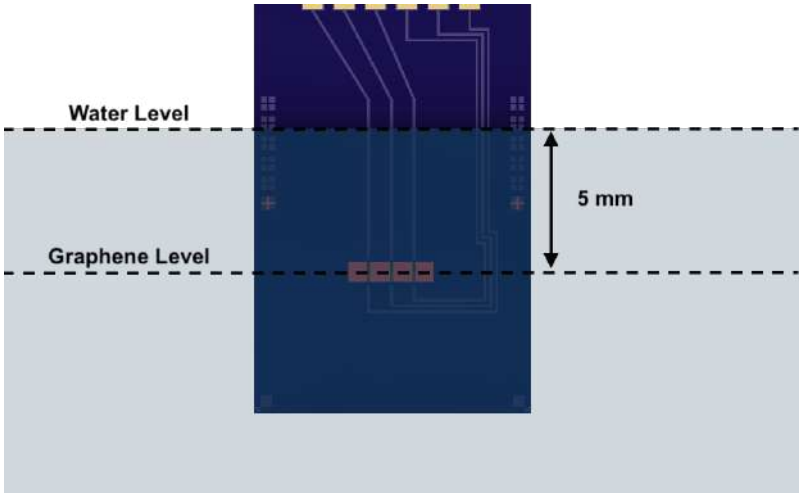


Figure 6.3: Graphene channels submerged 5 mm below liquid level in Dip Station setup.

Drying was performed using compressed air to displace water off the surface. Alternatively the liquid sample pot was removed from the Dip Station and the water was allowed to evaporate off the graphene surface. IV measurements were performed immediately following drying as a function of time.

6.2.7 Solvent Submersion & Drying Experimental Setup

Solvent-based experiments were performed by submerging the Dip Chip in 4 ml of IPA or Acetone in the Dip Station setup. Due to the higher vapour pressure of Acetone and IPA the solution pot would require a periodic top up, to keep the volume at the 4 ml mark. This was done at 2 hour intervals during the submersion phase.

During the drying phase of the experiment the solution pot was removed from the Dip Station and the solvent was allowed to evaporate from the chip surface.

6.2.8 PBS Submersion & Drying Experimental Setup

PBS-based experiments were performed by submerging the Dip Chip in n 3.6 ml of di H_2O, 0.4 ml of concentrated PBS solution was then added to the di H_2O solution

to make up 4 ml of standard 10 mM PBS. Submersion experiments were performed using the Dip Station setup, IV measurements were performed during the addition of the 0.4 ml concentrated PBS solution. For the drying-phase of the experiment the Dip Chip was removed from the solution and dried with compressed air.

Concentrated PBS solution was made up from PBS sachet (Sigma Aldrich, UK) added to 100 ml of di H_2O.

6.2.9 Graphene Surface Functionalisation

The graphene surface was functionalised using thrombin-aptamer with pre-conjugated pyrene stacking molecule (Base-Pair Bio, USA). The negative control graphene channels were functionalised with BNP-aptamer (brain natriuretic peptide) with pre-conjugated pyrene molecule (Base-Pair Bio, USA). For aptamer functionalisation, 10 μl of "Functionalisation Solution" (5 μM) was pipetted onto each graphene channel followed by a 12 hour incubation in a sealed container at 5 $^\circ$ containing a di H_2O-based humectant.

After the 12-hour incubation the excess Functionalisation Solution was washed off the graphene surface using 10 mM PBS solution by pipette, the wash process was repeated ten times.

After aptamer functionalisation of the graphene surface regions of unoccupied space remain on the graphene surface, this could allow direct physio absorption of other molecules onto the graphene surface, resulting in a resistance change and lower sensitivity. To reduce the potential physisorption, the blocker molecule 10 kDa Polyethylene glycol (PEG) with a pre-conjugated pyrene stacking molecule was used to fill open sites. PEG-pyrene (Sigma-Aldrich, UK), was made up in a 1 g per 100 ml solution in 10 mM PBS solution. 10 μl of PEG-pyrene solution was pipetted onto each graphene channel followed by a 12-hour incubation in a sealed container with a humectant. After the 12-hour incubation stage, the excess PEG-pyrene solution was washed off the graphene surface with ten repeats of PBS wash steps. This excess concentration of PEG-pyrene solution will saturate the remaining

unoccupied graphene surface.

Aptamer Functionalisation Solution

The aptamer Functionalisation Solution (5 μM) was made using the following protocol; 2 μl of Aptamer Re-Suspension Buffer (100 μM) (Base-Pair Bio, USA) was added to 2 μl of Folding Buffer (Base-Pair Bio, USA), the solution was mixed using pipette force action. This combined solution (50 μM) was then added to 36 μl of Application Buffer (composed of 10 mM TrisHCl (pH 7.4), 150 mM NaCl, 1 mM MgCl, Polyethylene glycol sorbitan monolaurate 0.05%, Sigma Aldrich, UK), followed by "vortex" mixing for 5 s.

6.2.10 Thrombin Sensing Experiment

Thrombin sensing experiments using the Dip Station setup with vertical orientation of the Dip Chip were not applicable for sensing. Due to the small sample volumes of the αthrombin 8.9 μl / ml (Thermo Fisher, UK). A set volume of 30 μl of "sensing solution", was pipetted onto the Dip Chip (orientated horizontally graphene surface up).

A dilution series was created to test the sensors response to increasing concentrations of the target analyte (Table 6.1), this was done sequentially in real-time measuring the Dip Chip IV response.

Table 6.1: Thrombin concentrations used in sensing experiments

Sensing Solution	αThrombin Concentration
1	1 pg/ml
2	5 pg/ml
3	10 pg/ml
4	100 pg/ml
5	1 ng/ml
6	10 ng/ml
7	100 ng/ml
8	1 μg/ml

Real-Time Sensing Experiment Protocol

First the graphene channels were stabilised in liquid, this was performed by pipetting 30 μl of PBS onto the graphene channel and incubating for 3.5 hours. The solution was then washed off the graphene surface with ten repeats of PBS pipette washing. This was followed by the application of the sensing solution 1 the protein was then incubated on the graphene surface for 45 minutes. The process of PBS washing and application of the next sensing solution was then repeated iteratively. After the final sensing solution was incubated and washed off the surface, the Dip Chip was then left to dry for the remaining period of the real-time measurement (12 hours).

6.3 Results & Discussion

6.3.1 Testing Of Dip Chip In Real-Time

The electrical setup for the real-time measurements was characterised and optimised to reduce noise, seen previously for the graphene baseline measurements. A standard 9.8 kΩ resistor was used as the control device as it would produce a known resistance without much deviation.

Figure 6.4 shows the three resistors simultaneous current measurements using for both setups. From the measurements performed outside of the Faraday cage (non-shielded) the standard deviation was calculated as 1.810 ±0.377 Ω with a relative standard deviation of 0.0185 ±0.004 %. In comparison the measurements performed inside the Faraday cafe "shielded" the standard deviation was calculated as 1.461 ±0.552 Ω with a relative standard deviation of 0.0149 ±0.005 %. The standard deviation is marginally lower for the shielded setup but this was not calculated as statistically significant (unpaired t-test). For graphene Dip Chip testing this noise could prove important in performing reliable sensing measurements.

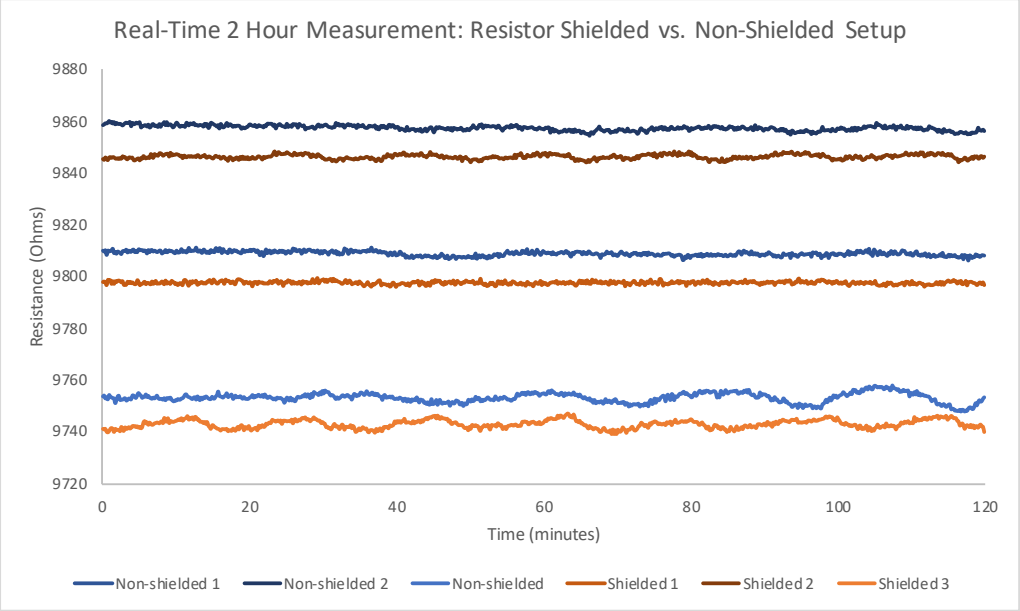


Figure 6.4: Calculated resistance data from real-time IV measurements performed over 2 hours on three 9.8 kΩ resistor in and outside of Faraday cage test setup.

The same measurement was repeated using a PT-SPI Chip in and outside of the Faraday cage experiment setup. Figure 6.5 shows the simultaneous real-time IV measurements on the graphene Dip Chip for both setups.

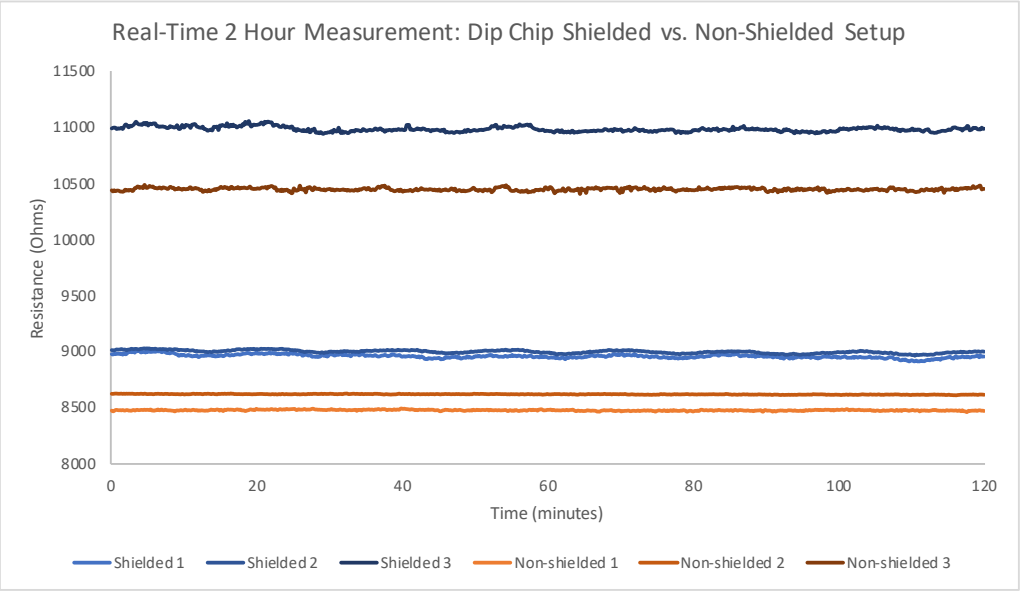


Figure 6.5: Calculated resistance data from real-time IV measurements performed over 2 hours on graphene Dip Chip in and outside of Faraday cage test setup.

The non-shielded graphene measurements yielded an average standard deviation of 13.707 $\pm$1.711 Ω and a relative standard deviation of 0.140 $\pm$0.018 %. The shielded measurements had an average standard deviation of 8.588 $\pm$2.920 Ω and a relative standard deviation of 0.0914 $\pm$0.033 %. The standard deviation when measuring the resistance of a graphene Dip Chip is higher than for a standard resistor, this is expected as the graphene surface is far more sensitive to environmental changes compared to the resistor (temperature, humidity, pressure etc.).

The shielded graphene measurements have a lower standard deviation than the non shielded measurements. This means to reduce electrical noise the Faraday cage should be integrated as part of the measurement setup. Future real-time IV measurements will be performed using the Faraday cage experimental setup.

It is hard to visually compare resistance results and noise due to the difference in starting resistances. Figure 6.6 shows a direct comparison of graphene channel 1 shielded against non-shielded. From this data it is hard to visual identify the levels of noise and even the trend of the resistance values.

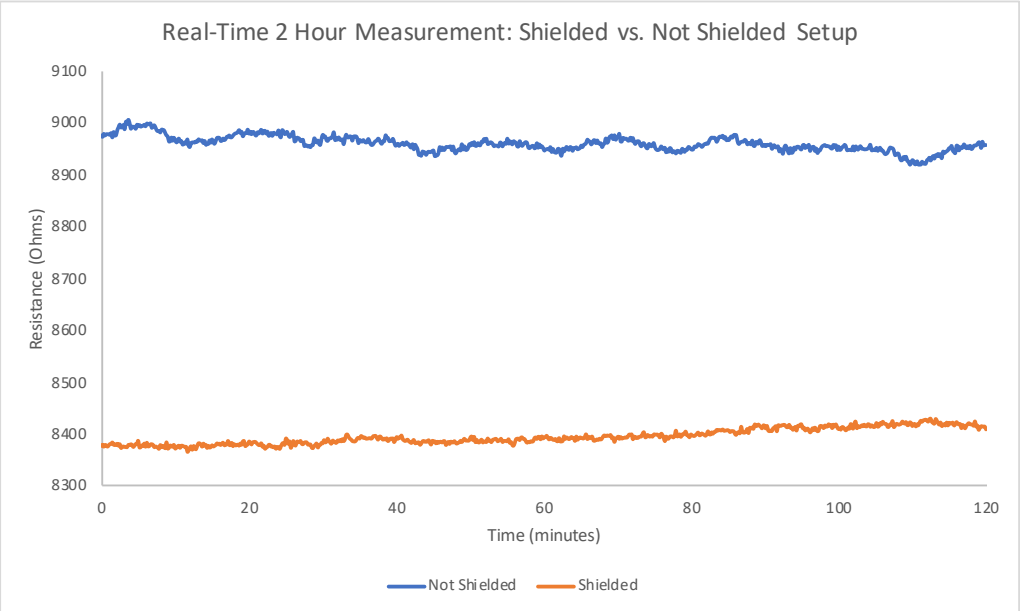


Figure 6.6: Comparison of calculated resistance data from real-time IV measurement of graphene channel 1 in shielded and non shielded electrical setup.

Figure 6.7 is a better illustration of this data set, Figure 6.7 shows normalised data, plotting the Z-score against time of graphene channel 1 shielded against non-shielded. It is clearly visible that the shielded measurement has less noise that the non shielded measurement.

To compare multiple graphene channels simultaneously, data will be normalised before plotting in future results.

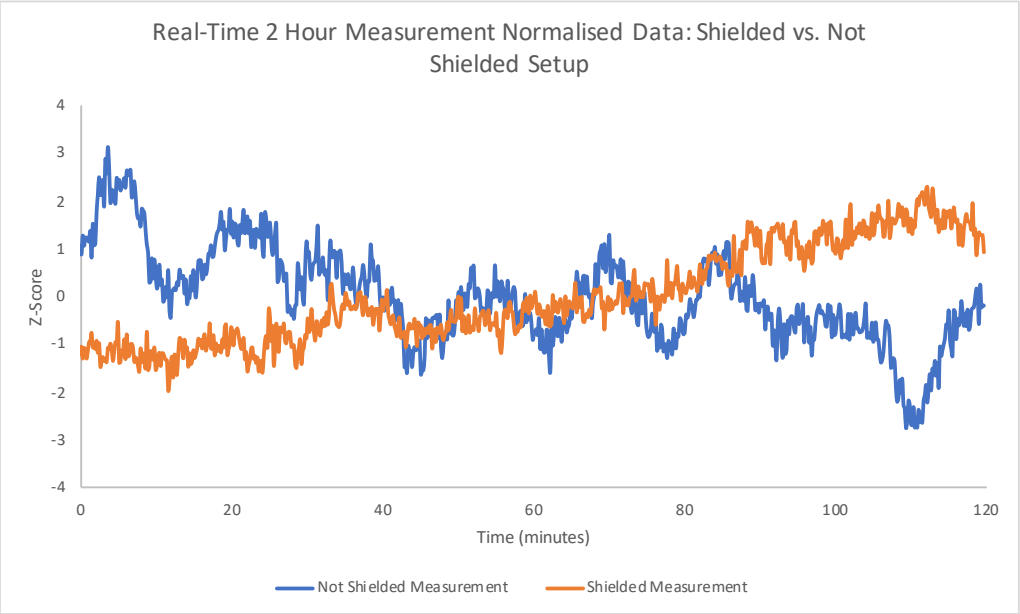


Figure 6.7: Comparison of normalised z-score data from real-time IV measurement of graphene channel 1 in shielded and non shielded electrical setup

6.3.2 Auto 0 Function Test

The Auto 0 function improves measurement accuracy by removing internal voltage offset due to temperature. It does so by measuring the voltage across the input terminals and calculating the off-set voltage before each input measurement. It then subtracts the off set voltage from the input voltage of the measurement.

For long duration experiments it is recommended to use the Auto 0 function. This slows down the measurement, overall removing drift in the measurements as it self calibrates before each individual measurement. Figure 6.8 shows the effect of the Auto 0 (On vs. off) function for 3 graphene channels during a 10 hour real-time IV measurement. From the graph it is not clear if either measurement produces a higher degree of measurement drift.

To quantify potential drift in the measurement the original resistance data was analysed to calculate the slope (rate of change in resistance). The slopes during Auto 0 (On vs. Off) IV measurements were calculated as -4.1237 $\pm$0.3861 Ωmin^{-1} and -5.8033 $\pm$0.4824 Ωmin^{-1} respectively. This shows the Auto 0 function produces

a lower rate of change in resistance and therefore less drift in the measurement. All future real-time based measurements use the Auto 0 On function to reduce the degree of measurement drift.

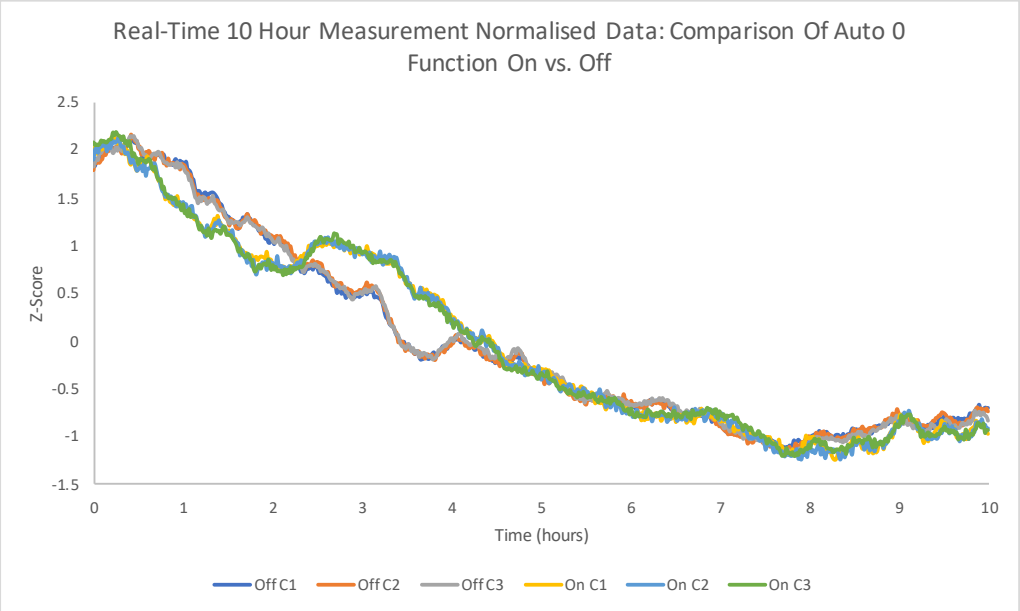


Figure 6.8: Normalised data of real-time IV measurements performed over 10 hours comparing a graphene Dip Chip Auto 0 set "Off" set "On".

6.3.3 Vacuum - Ambient Measurements & Drift Determination

All the graphene channels measured previously appear to have a degree of drift in their resistance, which decreases over a period of time (Figure 6.8 & 6.5). To determine the extent of this drift over a longer duration, a Dip Chip was measured over a 100 hour period in ambient conditions (four sequential 25-hour measurements stitched together). Figure 6.9 shows the normalised resistance data as a function of time. The average slope calculated over the full 100 hour period was -5.0627 $\pm$0.8144 Ωmin^{-1}. The average slope for the first 10 hour period and last 10 period were calculated as -45.0460 $\pm$4.6998 Ωmin^{-1} and 1.6254 $\pm$1.6254 Ωmin^{-1} respectively. The initial rate of resistance decrease appears to be much higher compared to the

rate of resistance change over the 100 hour measurement period.

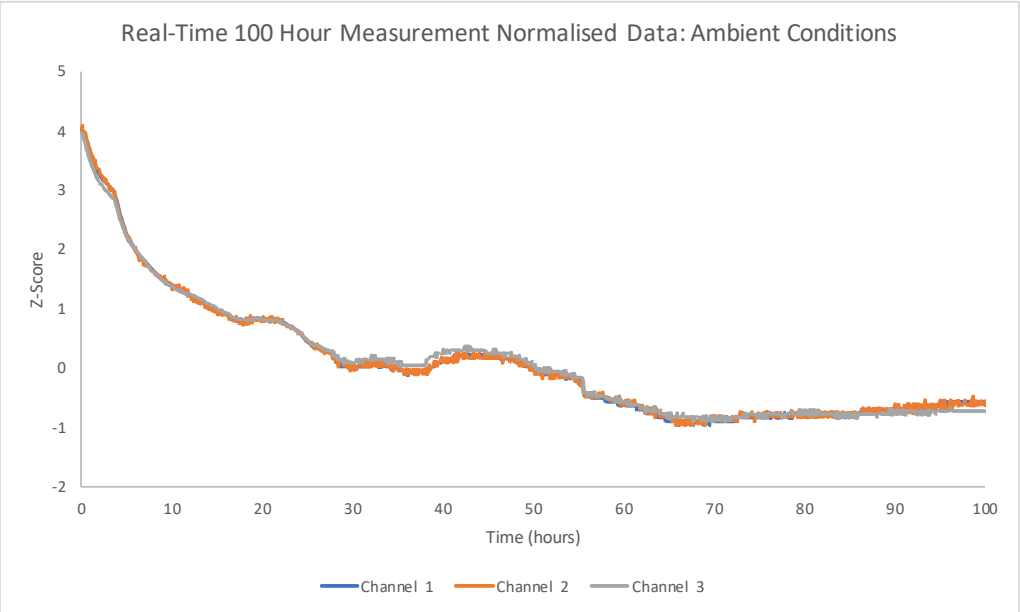


Figure 6.9: Normalised data of real-time IV measurements performed on graphene Dip Chip over a 100 hour period in ambient conditions.

This could be due to a variety of factors, environmental conditions, storage conditions or could be due to current induced cleaning of surface residues / contaminants [5], [6]. The samples are stored under vacuum post fabrication, the return to atmospheric pressure and humidity could also be the cause of the initial resistance decrease.

To determine the cause of this effect an experimental series was devised whereby six Dip Chips (PT-SPI) were stored in vacuum for a 12 hour period. The chips were randomly paired for the experiment into groups A and B. Group A chips were measured for 50 hour real-time measurement straight out of vacuum. B chips were measured after the same 50 h period spent in ambient conditions.

Figure 6.10 and Figure 6.11 shows a representation of the normalised resistance data for group A and B. The average Slope from group A channels was calculated as -10.8642 $\pm$2.3460 Ωmin^{-1} and the average for group B was calculated at -3.1188 $\pm$3.4125 Ωmin^{-1}. The average change in resistance was calculated from the first and final hour of measurement. Group A average equalled -8.3734 $\pm$3.6056 % and

group B calculated as -1.1372 ±1.6900 %. The initial increase in resistance seen in Figure 6.10 could be due to initial adsorption of ambient air molecules.

The difference in slope and resistance change between group A and B suggests that maintaining the graphene channels in vacuum is the primary cause of the initial drop in resistance at the start of real time measurements. Exposure to ambient humidity appears to reduce the resistance of the channel, and provide a more stable baseline. This aligns with other research that suggests water vapour/humidity causes hole-doping and reduces resistance, due to the lowest unoccupied orbitals of H_2O accepting charge from the graphene [7]. Future measurements will be left in ambient conditions 3 days prior to IV measurements.

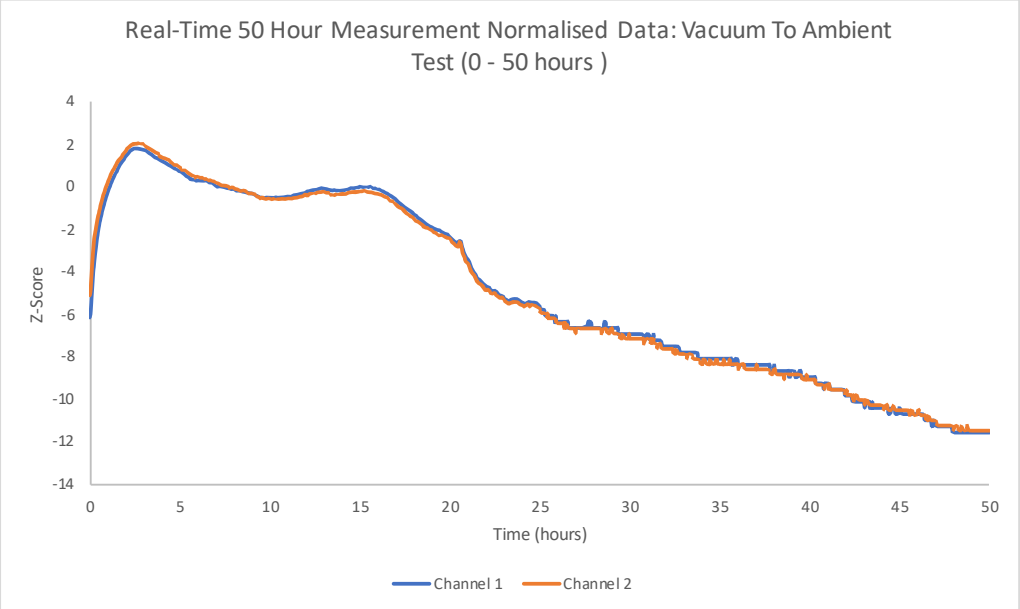


Figure 6.10: Normalised data of real-time IV measurements performed over time period 0 - 50 hours on Dip Chip stored in vacuum.

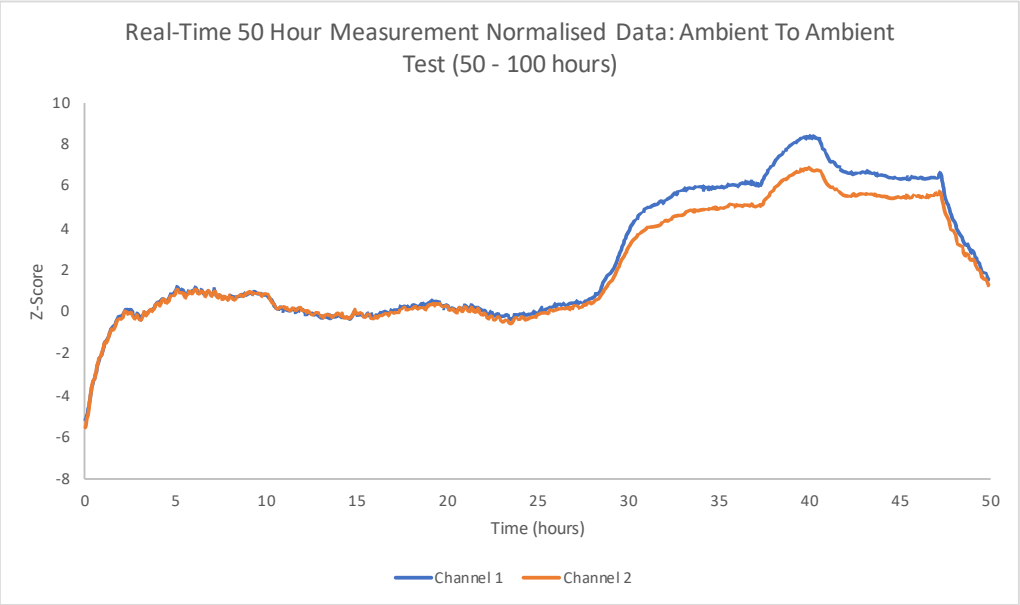


Figure 6.11: Normalised data of real-time IV measurements performed over time period 50 - 100 hours on Dip Chip stored in ambient from 0 - 50 hours.

6.3.4 Di H_2O Submersion Measurements

Functionalisation and sensing require the addition of a solution onto the graphene surface. It is important to understand the effect of these solutions on the graphene's electrical properties, so that the sensing based experiments can separate the effect of the solution compared to the effect of the analyte itself.

The ability to measure changes whilst submerged in liquid is vitally important for a sensor based chip. A majority of bio-marker based diagnostics medical samples are liquid based; blood, urine ect [8]. Figure 6.12 shows the normalised real-time resistance data against time of a PT-SPI Chip submersion in di H_2O after 10 minutes measurement in air. The measured resistance increases rapidly within the first 2 hour period. The average change in resistance was calculated as 56.5828 $\pm$5.3205 %. This resistance increase, induced by the application of H_2O, does not follow the behaviour normally exhibited by graphene in relation to exposure to humidity. The most reported behaviour is a decrease in resistance due to the hole-doping effect of the water vapour removing electrons from the graphene sheet was expected [9]

[10] [11] [12]. Therefore, further investigation into the doping effect of the H_2O submersion was required to determine the cause of the resistance increase.

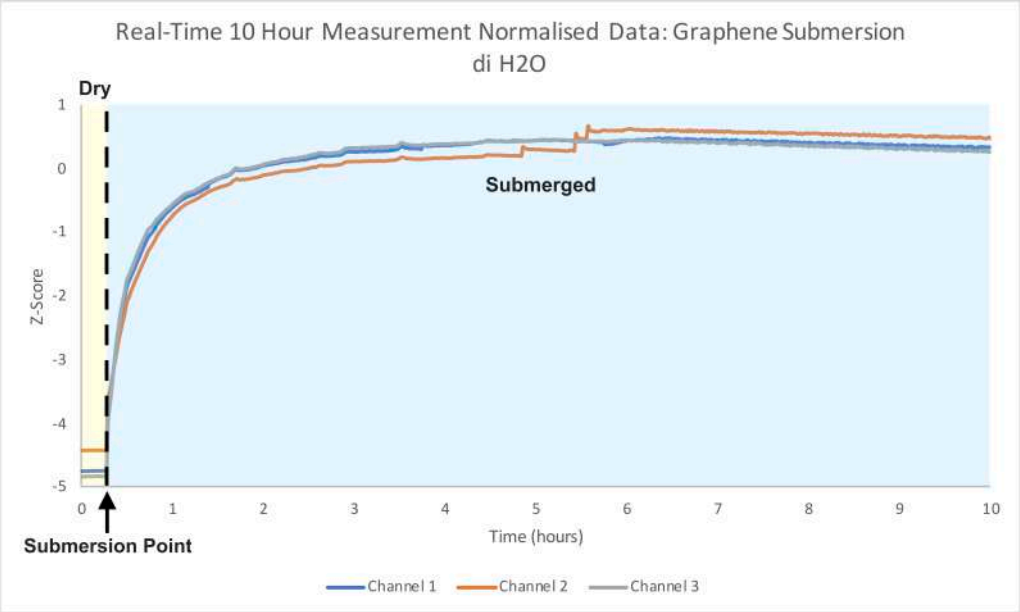


Figure 6.12: Normalised data of 10 hour real-time IV measurements of graphene after submersion in di H_2O.

To investigate the change in doping of the graphene a IV probe station gated FET (Dirac point) measurement was performed on a PT-SPI Chip, first in ambient conditions followed a 20 μl volume of H_2O pipetted onto the graphene surface and incubated for 10 minutes. Figure 6.13 shows the resulting channel (source-drain) resistance was measured as a function of the gate potential. The Dirac point (charge neutrality point) is not captured within the -50 V - 50 V sweep for the "dry" measurement. The Dirac point appears to be within the 50 V to 100 V region. This range is expected for graphene devices fabricated using graphene sourced from Graphenea (Spain). Graphenea recommends Acetone treatment (12-hours) to shift the Dirac point close to 0 V for their devices

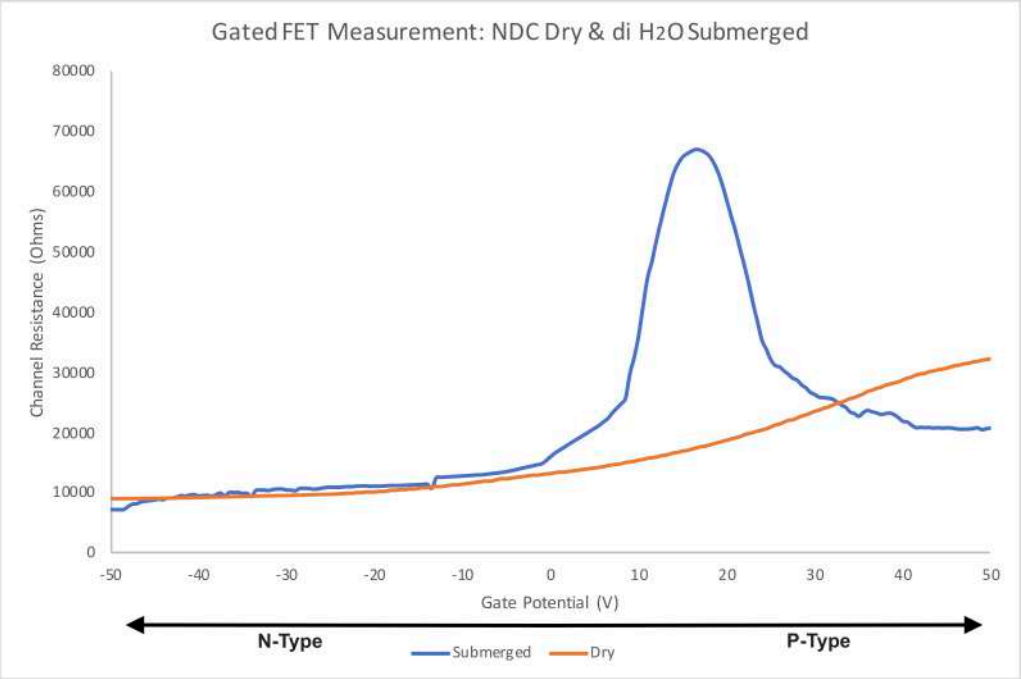


Figure 6.13: Gated FET resistance data (Dirac point) of PT-SPI Chip in ambient conditions prior and post application of di H_2O.

The resistance calculated (source-drain) in ambient conditions prior to the addition of di H_2O was calculated as 13269 Ω.

The effect of H_2O submersion shifts the Dirac point to within the -50 V - 50 V range, measured at a gate bias of 17.5 V. This shift from +50 V down to 17.5 V suggesting the graphene has been electron-doped by the H_2O submersion.

This result can be explained by the electric double layer of water formed at the surface of the graphene channel [13]. Similar to a liquid-gated graphene field-effect (LG-FET) where an electric double layer of ions present at the graphene surface form an electric field which dopes the graphene channel [14]. This electric double layer could be formed by the weakly acidic H_2O, this means that there will be H_3O^+ and OH^- ions present which could form the double layer above the graphene surface [15]. The induced electric field produced, has a electron-doping effect on the graphene causing the Dirac point to shift toward the N-type region [16].

The resistance measured at 0 V whilst submerged in di H_2O is 15847 Ω this is a resistance increase of 19.43 % which fits the trend seen in the real-time submersion

experiments. Further experimentation using different solvents and a comparison of the PT-MVD Chip which had a starting Dirac point in N-type region, should be investigated further to understand the water absorption an desorption effect on the graphene prior to functionalisation based experiments.

6.3.5 Di H_2O Drying Measurements

Standard IV measurements made on graphene resistors are done on a dry graphene surface. Dry IV measurements were performed throughout the fabrication and early graphene sensor experiments [17]. Following the submersion experiments and the observation of the extended time required for the resistance of the device to stabilise, an investigation into the effect drying / evaporation of di H_2O on the graphene devices was performed.

Figure 6.14 shows the normalised real-time resistance data against time of a PT-SPI Chip drying after being submerged in di H2O. The average change in resistance was calculated between 0 - 3 hours as -11.6277 $\pm$2.2288 %. The resistance change between hours 3-4, calculated as -0.5689 $\pm$0.3110 %, less than the baseline of drift seen in ambient real-time measurements of (-1.1372 $\pm$1.6900 %). All graphene channels exhibit a large initial drop in resistance "drying period" followed by a plateau where the graphene channel resistance decrease is in line with the drift seen in real-time graphene measurements.

This suggests that IV measurements performed on dry graphene Dip Chips should be performed 3 hours post submersion in di H_2O. Otherwise the change in resistance seen could be due to the effect of drying and not related to specific surface modification.

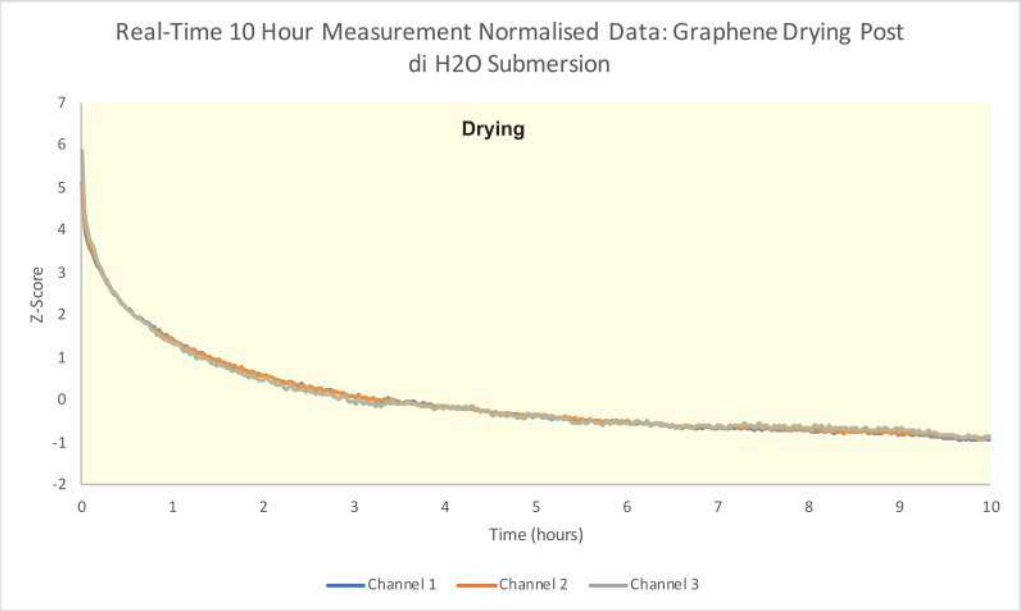


Figure 6.14: Normalised data Dip Chip 10 hour real-time experiment. Dip Chip submersed in di H_2O for 2 hours then dried with compressed air prior to measurement time point 0.

6.3.6 Di H_2O Submersion & Drying Measurements

To investigate the effect of liquid submersion and surface drying further the time period for measurement was extended. Firstly, experiments on submersion in di H_2O and drying were performed. This method allows monitoring of the initial device resistance, resistance change due to submersion and the end resistance post drying. The changes seen due to the di H_2O can be subtracted from the sensing response in both wet and dry resistance measurements. This will allow a future comparison of sensing wet vs dry measurements.

The first set of submersion drying experiments were performed on three PT-SPI Chips, Figure 6.15 shows the normalised resistance data against time for one of these chips. The data has been normalised to the starting resistance data points from the first 15 minutes of the experiment.

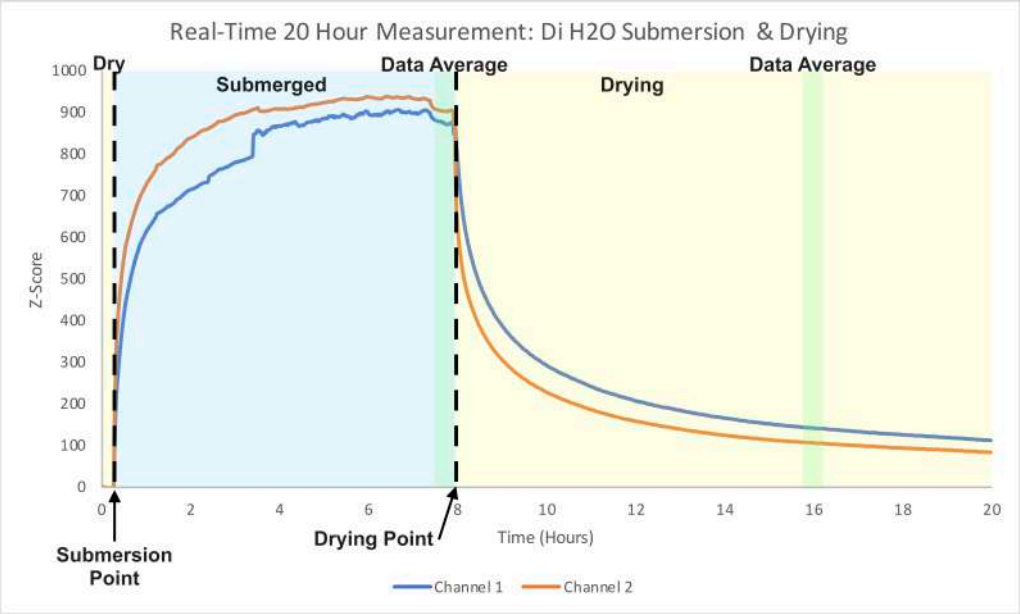


Figure 6.15: 20 hour real-time experiment, data normalised to dry starting resistance, After 15 minutes graphene submerged in di H_2O. At 8 hours graphene removed from liquid and dried using compressed air (PT-SPI Chip).

From the repeat experiments, the IV data was used to calculate an average resistance of the dry (pre-submersion region), the average resistance of the wet region (10 data points at 8-hours submersion) and the average resistance of the drying (10 data points after 8-hours drying). These averages were used to calculate the change in resistance due to submersion and resistance change due to drying (Table 6.2).

Table 6.2: Table showing average resistance "dry" and percentage change in resistance for submersion and drying (PT-SPI Chips).

	Initial Dry Resistance (Ω)	8 Hours Submersion ΔResistance (%)	8 Hours Drying ΔResistance (%)
9 Channel Average	6622	65.07	9.24
Standard Deviation	528	10.45	3.35

This data suggests that to gain an stable resistance reading of the graphene,

whilst submersed in di H_2O, the measurement should be taken a minimum of 4 hours post submersion. Stable dry measurements might not be possible within the 14 hours post submersion. The resistance change due to di H_2O alone, is on average a 65.07 $\pm$9.24 % increase. To use this system for sensing the response due to molecular binding close to the surface would need to create a resistance change in excess of 75 % to even see the signal.

These submersion/drying experiments have been performed using the PT-SPI Chips. To compare the response to the PT-MVD Chips, the same experimental set up was used. Three repeats were performed on the PT-MVD Chips to calculate the average resistance change due to submersion.

Figure 6.16 shows the normalised resistance data from the 20-hour real-time IV measurement for a PT-MVD Chip. The change seen was a decrease in resistance over time, the complete opposite to the PT-SPI Chips. The reason for this decrease in resistance must also be related to the doping effect of the electric double layer, which is produced by the H_3O^+ and OH^- molecules whilst submerged.

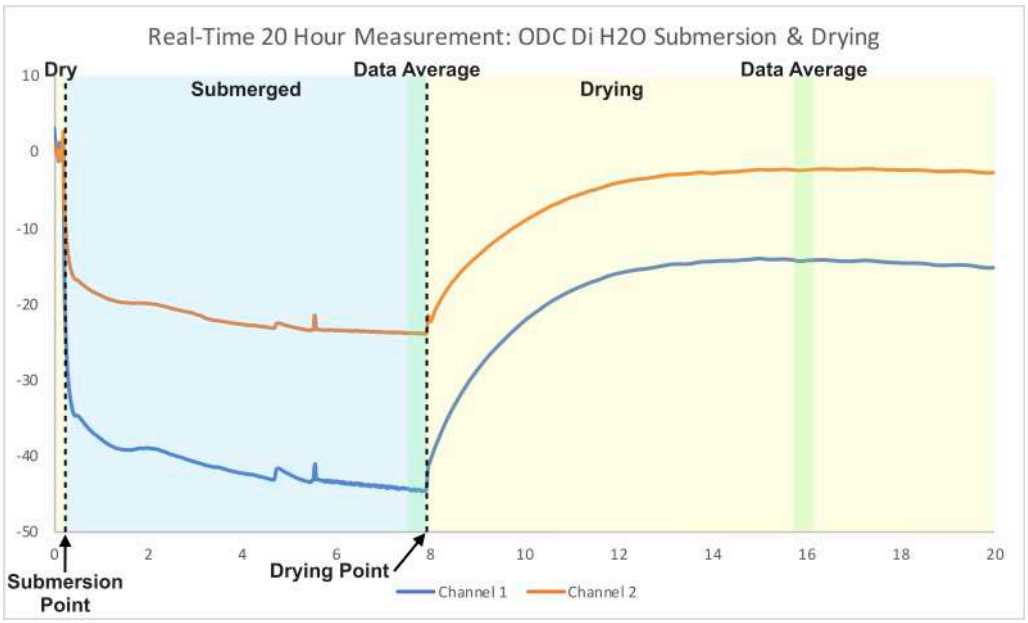


Figure 6.16: 20 hour real-time experiment, data normalised to dry starting resistance, After 15 minutes graphene submerged in di H_2O. At 8 hours graphene removed from liquid and dried with compressed air (PT-MVD Chip).

Table 6.3 shows the average resistance dry (pre-submersion) taken from the first 10 data points. The resistance change was calculated based on the average resistance calculated for 10 data points at the 8-hours of submersion time point, and 8 hours of drying. Interestingly, all PT-MVD Chips tested showed the same decreasing trend in resistance for each graphene channel. Similarly the change in resistance is large, an average of -57 %, as with the PT-SPI Chips, any signal from sensing will need to exceed this threshold to be detectable over the drying period.

The decreasing resistance trend returns over the a 6 hours drying period in ambient conditions. This means that dry sensing measurements should be taken at least 6 hours post drying for reliable measurements.

Table 6.3: Table showing average resistance "dry" and percentage change in resistance for submerged and drying (PT-MVD Chips).

	Initial Dry Resistance (Ω)	8 Hours Submersion ΔResistance (%)	8 Hours Drying ΔResistance (%)
9 Channel Average	7293	-57.41	-14.92
Standard Deviation	1013	7.34	10.78

Further testing was needed in order to understand why PT-MVD Chips produces a negative change in resistance compared to the PT-SPI Chips positive change. Gated FET measurements were performed on a dry PT-MVD Chips, followed by the addition of di H_2O. Figure 6.17 shows the resulting Dirac points plotted on the same graph and the doping shift. The response to di H_2O is similar for the PT-SPI Chips and PT-MVD Chips. The graphene for both devices are electron-doped (shifted left on x-axis) by the submersion in H_2O due to the electric double layer. The difference is the starting position of the Dirac point for the PT-MVD and PT-SPI chips which determines where the shift in resistance for the real-time IV measurements.

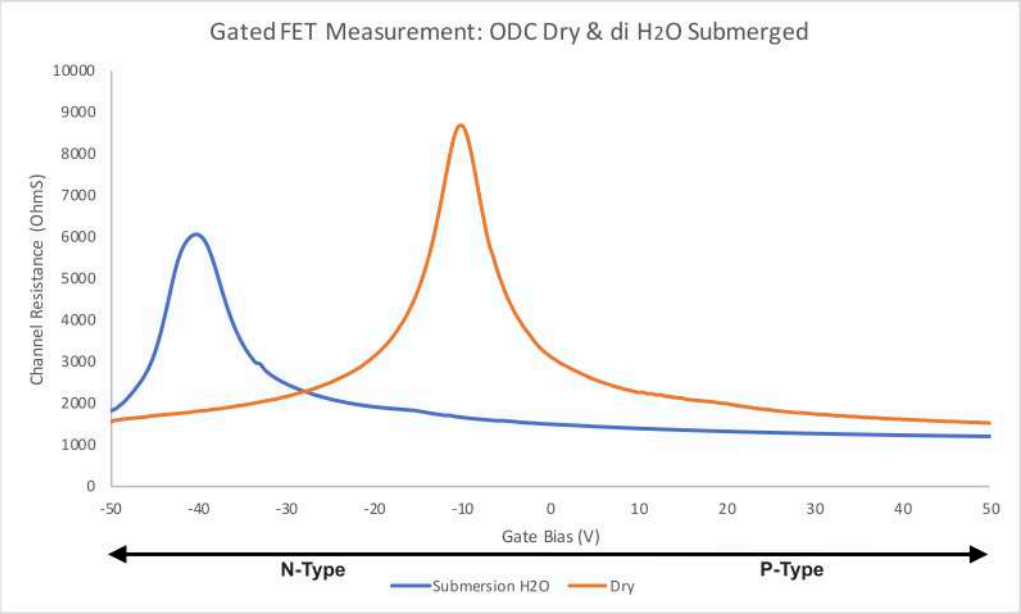


Figure 6.17: Gated FET (Dirac point) measurement before and after application of di H_2O onto the graphene surface (PT-MVD Chip).

6.3.7 Solvent Submersion & Drying

Prior to functionalisation, the graphene chips are cleaned using a solvent based cleaning protocol: 10-minute acetone bath followed a 5-minute IPA bath. To understand the effect on the resistance of the graphene channel after these cleaning procedures, the submersion and drying 20-hour real-time IV measurement was repeated using three PT-SPI Chips for both solvents.

During the first set of Acetone experiments, all 3 measurements showed signs of measurement error. Figure 6.18 shows an example of where the experiment failed after 170 minutes of measurement (exceeding normal measurement range 100000 Ω). The initial submersion can be seen to cause an increase in resistance to a stable plateau for the first 40 minutes of measurement. This initial plateau was observed for multiple PT-SPI Chips with an average resistance change of 311 ±111 % calculated. However, with such a large standard deviation and the break down in signal mid measurement these figures are not reliable indicators of the effect of Acetone on doping. After this period the resistance begins to increase further in a

chaotic pattern, full IV measurement can be found in the Appendix. After the real-time experiment, IV measurements were performed on the chips in dry conditions. No linear response was observed, therefore the graphene channel had been damaged or delaminated.

As the breakdown occurred on all channels on the three PT-SPI Chips the experiment was not worth repeating on the PT-MVD Chips. PT-SPI Chips have been submerged in Acetone and other solvents for longer time periods during fabrication. So it is unclear why the channels failed between 40 - 170 minutes during the real-time measurements.

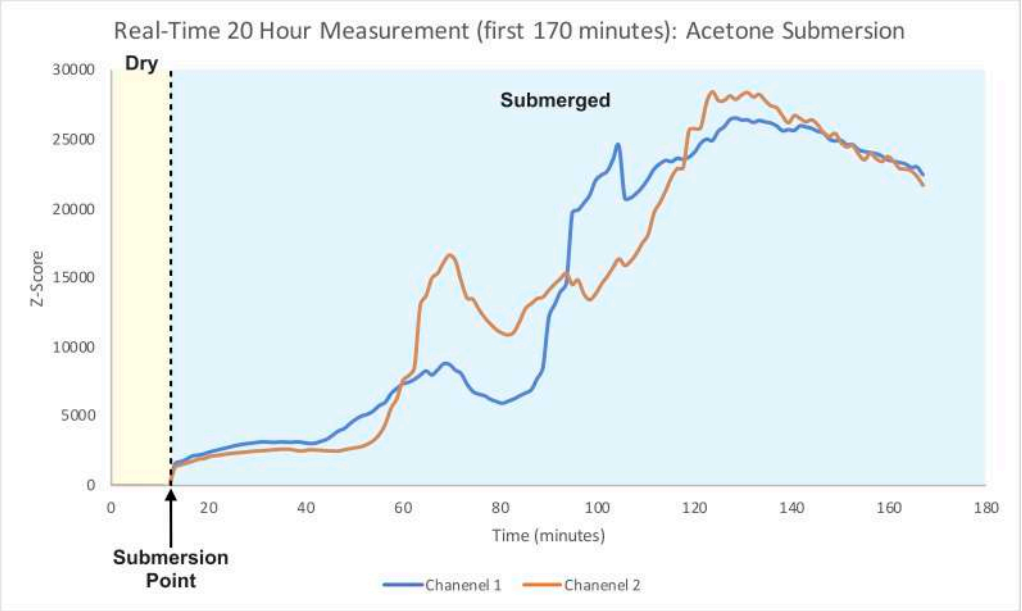


Figure 6.18: 170 minute real-time IV measurement (normalised data), after first 10 minutes of dry measurement the chip was submerged in Acetone. At 170 minutes the data no longer fits with in the IV measurement range (PT-SPI Chip).

The 20-hour real-time dry and submersion IV measurements were performed using IPA solvent with three PT-SPI Chips (normalised data, Figure 6.19). After the initial increase in resistance upon submersion in IPA, the resistance increases linearly before starting to plateau after 6 hours. The resistance had not fully plateaued after 8 hours submerged when the chip was removed from the solution and dried. The return to base line resistance was then measured during the drying period.

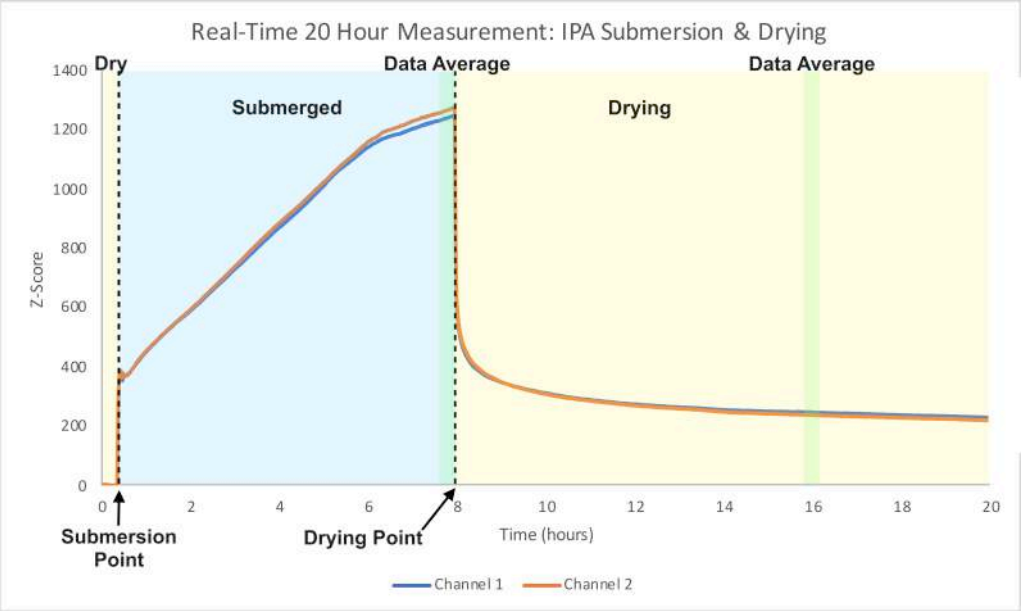


Figure 6.19: 20-hour real-time experiment (data normalised to starting resistance), After 10 minutes the chip is submerged in IPA. At 8 hours the chip was removed from the IPA solution and dried with compressed air (PT-SPI Chip).

Table 6.4 shows the average increase in resistance over the first 8 hours was calculated at 52.84% this is 12% less than the change relating to di H_2O. After the 8 hour drying period the Δresistance from baseline was 10.9%, similar to the drying rate of the di H_2O. The initial upward resistance spike at submersion full encapsulation is likely due to the electric double formation effecting the resistance measurement. With IPA having a much higher vapour pressure than H_2O it could be inferred that the resistance decrease back to baseline (dry) happens much faster with IPA drying.

This data suggests a gradual doping of graphene and a large initial doping change, due to the electric double layer. The gradual doping could be related to solvents spreading to the interlayer region between the graphene and SiO_2 surface [18]. Both H_2O and IPA solutions produce a slow return to baseline (dry resistance). The slope post 4 hours dry was calculated as -33.47 $\pm$1.13 Ωmin^{-1} compared to -34.52 $\pm$1.57 Ωmin^{-1} after 11 hours. These trapped interlayer molecules slowly escape and the graphene returning to the doping state caused by the SiO_2 substrate.

Table 6.4: Table showing average resistance "dry" and after 8 hours submersion in IPA and the percentage change in resistance (Pre-Transfer screen-printed ink passivated chip).

	Initial Dry Resistance (Ω)	8 Hours Submersion ΔResistance (%)	8 Hours Drying ΔResistance (%)
9 Channel Average	7319	52.84	11.36
Standard Deviation	649	10.90	12.43

Although the baseline (dry resistance) is not reached after 8 hours post compressed air drying, the resistance decrease stabilises after 4 hours. For future sensing experiments data taken dry would need to be measured at the same time point post 4 hours to account for the effect of drying / doping of the graphene surface.

The real-time IPA submersion drying experiments were then repeated using the ODCs to compare the response between chip fabrication processes. Similar to the di H_2O experiment, the resistance of the graphene channel experienced an initial rapid decrease upon submersion in the IPA (Figure 6.20).

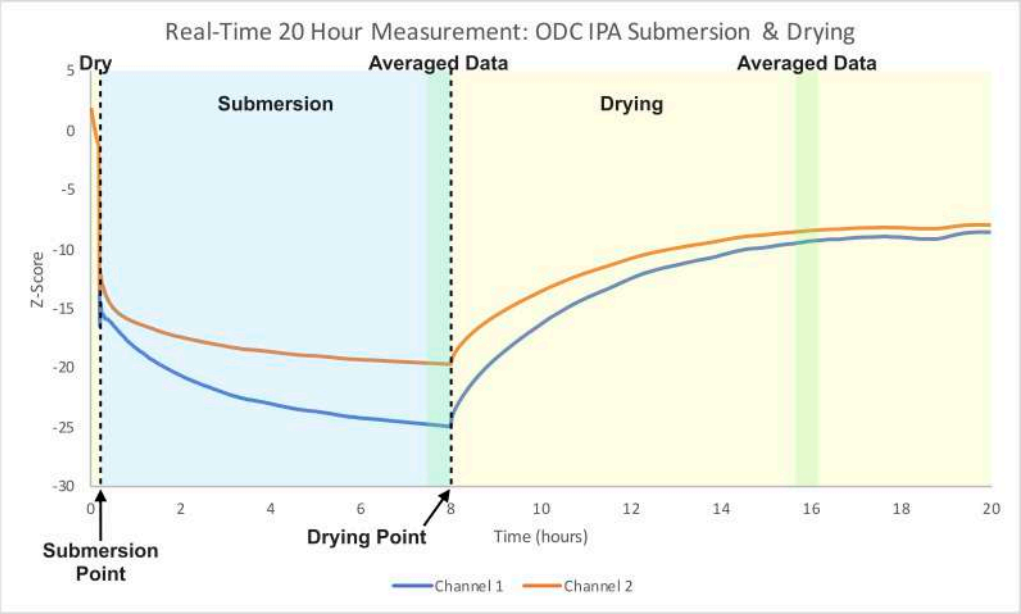


Figure 6.20: 20-hour real-time experiment (data normalised to starting resistance), After 10 minutes the chip was submerged in IPA. At 8 hours the chip is removed from the IPA solution and dried in compressed air (PT-MVD Chip).

Table 6.5 shows the average resistance dry, change in resistance (dry to average data) after 8 hours submersion and change in resistance (dry to drying average data) after 8 hours drying were calculated. The resistance change is not as high in response to IPA as for the di H_2O result. This mirrors the results seen in the PT-SPI Chip experiments. The recovery period back to baseline appears to be longer than for the PT-SPI Chips. The recovery time to reach baseline once dry is much more gradual. The change in resistance (slope) returns to a resistance decrease after 10 hours of drying in ambient conditions.

This suggests that when processing and making real-time IV measurements of PT-MVD Chips in future experiments, chips should be left for at least 10 hours in ambient conditions prior to measurement. PT-MVD Chips in general behave in a similar way to IPA and H_2O. The change in resistance seen as a result of liquid submersion is due to the starting resistance and predominant charge carrier (type of doping) of the graphene channel after fabrication.

Table 6.5: Table showing average resistance "dry" and after 8 hours submersion in IPA and the percentage change in resistance (PT-MVD Chip).

	Initial Dry Resistance (Ω)	8 Hours Submersion ΔResistance (%)	8 Hours Drying ΔResistance (%)
9 Channel Average	4882	-49.20	-17.75
Standard Deviation	513	14.98	5.65

6.3.8 Phosphate Buffered Saline Submersion

PT-MVD chips are used primarily for the functionalisation and sensing research because overall graphene quality was shown to be much higher post-passivation, seen in Passivation & Packaging Chapter. Similar PT-SPI chips have been shown to cluster functionalisation reagents around photoresist and screen printing ink residue reducing sensor uniformity [19]. With limited bio-receptors and protein reagents it was deemed inefficient to use both PT-SPI and PT-MVD chips for the sensing experiments.

The di H_2O submersion/drying experiments show a resistance change on the PT-MVD Chips. However, both aptamer functionalisation and protein sensing will be performed in phosphate buffered saline (PBS). To understand the resistance change due to PBS exposure, a di H_2O/PBS submersion experiment was performed.

Figure 6.21 shows the initial resistance change due to submersion in di H_2O and after 8 hours the resistance change due to the addition of PBS to the solution.

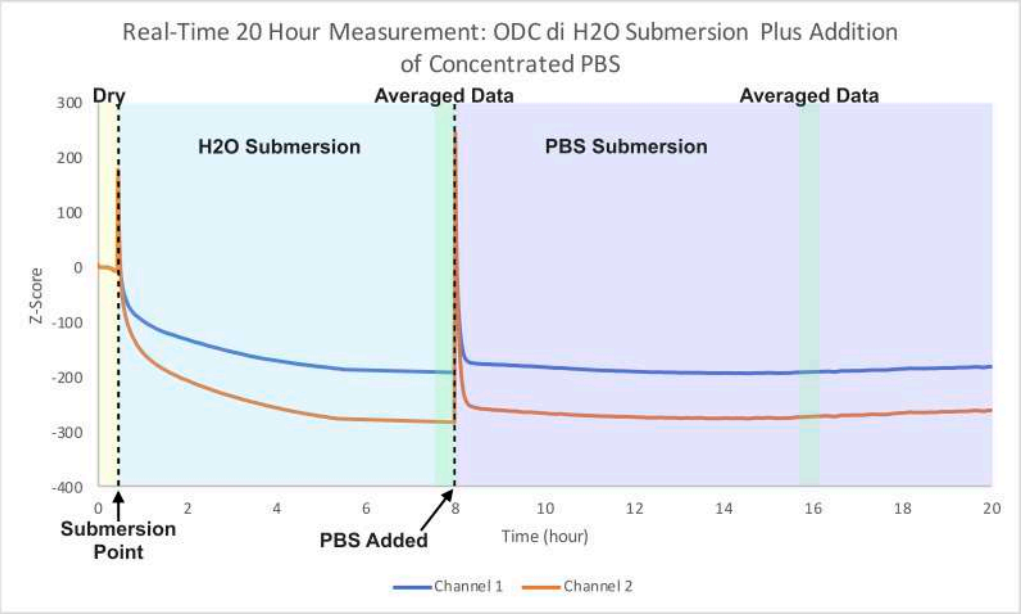


Figure 6.21: Real-time 20 hour measurement: Data normalised to initial 10 minutes dry resistance, followed by submersion in di H_2O for 8 hours. An additional 400 μl of 100 mM PBS was added to the di H_2O after 8 hours to create a 10 mM PBS concentration (PT-MVD Chip).

The average decrease in resistance after PBS exposure was calculated as -59.53 $\pm$14.21 %. This change is very similar within 2 % of the change due to di H_2O. The large standard deviation means it is difficult to see any significant difference between submersion in di H_2O vs. submersion in PBS. This suggests that PBS submersion should be treated the same as di H_2O submission when, a stabilisation time of approximately 3-4 hours prior to sensing will suffice to create a stable resistance baseline.

6.3.9 Surface Functionalisation

Prior to sensing experiments, IV probe station measurements were performed on the PT-MVD chips prior to functionalisation and post aptamer and PEG functionalisation experiments.

Figure 6.22 shows the resistance data for blank graphene and functionalised

graphene. Not all functionalised graphene channels exhibit an increase in resistance. This could be due to variations in the graphene chips or the uniformity of the functionalisation chemistry. As mentioned in the Multiplex design chip testing in Chapter 1, the hydrophilic chip surface causes the functionalisation solution to spread unevenly around the the chip surface.

The increase in resistance seen after functionalisation of the graphene channel with π-π stacking aptamer (bio-receptor) and PEG-pyrene (blocker molecule). Could be due to doping shift brought about by the π-π stacking molecule pyrene Pyrene and pyrene derivatives have been shown to have hole-doping (electron withdrawing) effects [20]. Or due to the reduction in the graphene's carrier mobility, caused by the functionalisation molecules increasing the charge scattering sites (density of electron-hole puddles) on the graphene, or by disrupting the SP^2 bonding structure of the graphene [21].

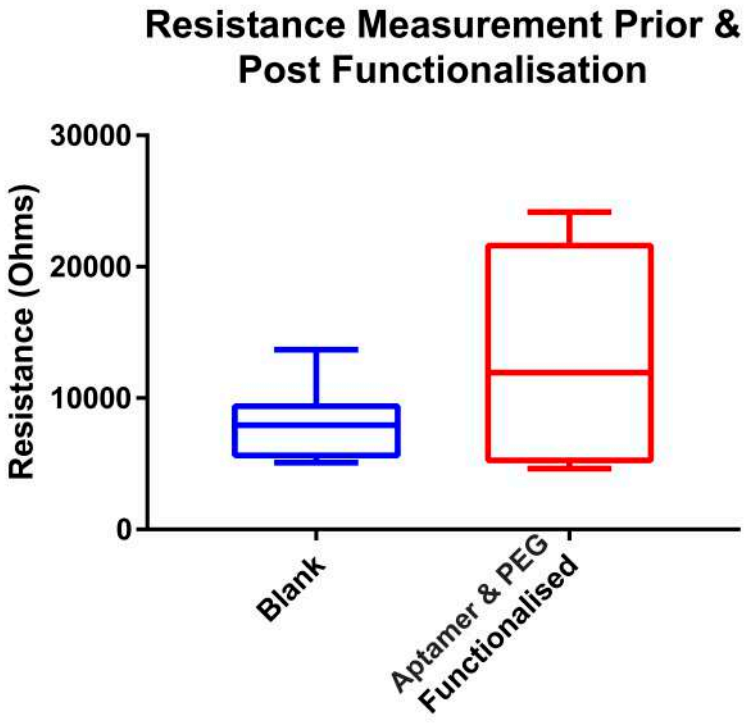


Figure 6.22: Box and whisker plot: IV probe station resistance measurements of blank PT-MVD Chip prior and post aptamer and PEG-pyrene functionalisation.

The increase in resistance shown in the IV probe station measurements was investigated further using FET style (Dirac point) measurements. Figure 6.23 shows a Dirac point measurement of a functionalised device. This shows the Dirac point of the graphene close to the 0 V. This means that a standard two terminal IV resistance measurement would result in graphene resistance being close to its highest resistance (charge neutrality point). A functionalisation process that results in a Dirac point close to 0 V can be useful for real-time chemiresistive measurement, further changes in doping (Dirac point shifting) during protein binding would result in a large resistance change due to the high degree slope of the Dirac point.

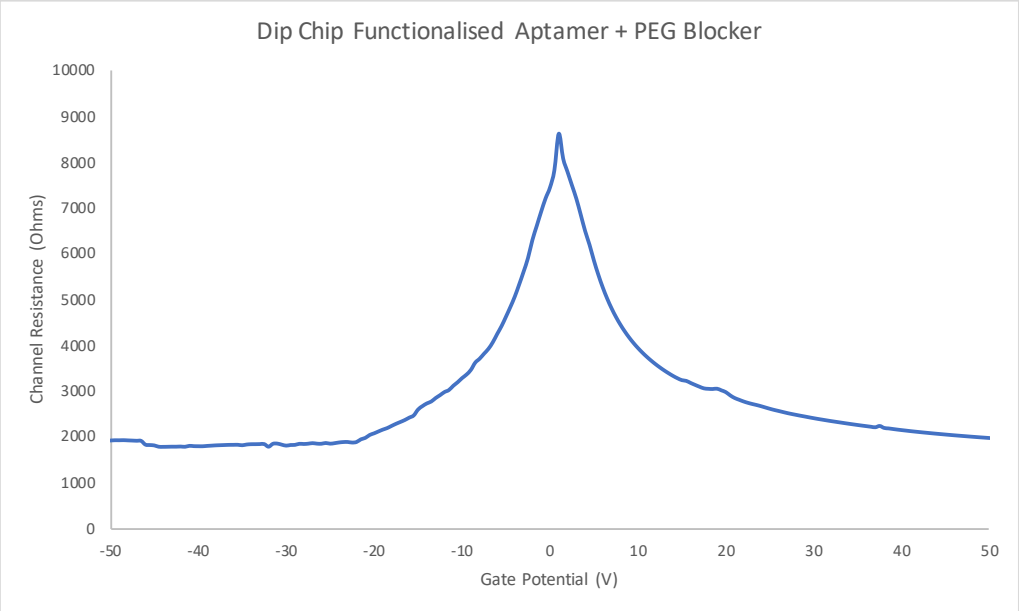


Figure 6.23: Gated FET (Dirac point) measurement of a graphene device functionalised with Thrombin-aptamer and PEG-pyrene blocking molecule.

6.3.10 Thrombin Sensing Experiment

Sensing based experiments were performed on three PT-MVD Chips functionalised with the thrombin-aptamer and Peg-pyrene, as well as three PT-MVD Chips functionalised with BNP-aptamer as the negative control. The chips were submerged in PBS for the first 3 hours to allow for stabilisation in liquid. The αThrombin protein concentrations were added and allowed to stabilise/incubate for 45 minute periods,

the thrombin concentration was increased at each 45 minute intervals from 1 pg/ml to 1 μg/ml.

Figure 6.24 shows the resulting sensing experiment comparing the thrombin-aptamer and bnp-aptamer. The resistance data was normalised and the average Z-scores were then plotted against time.

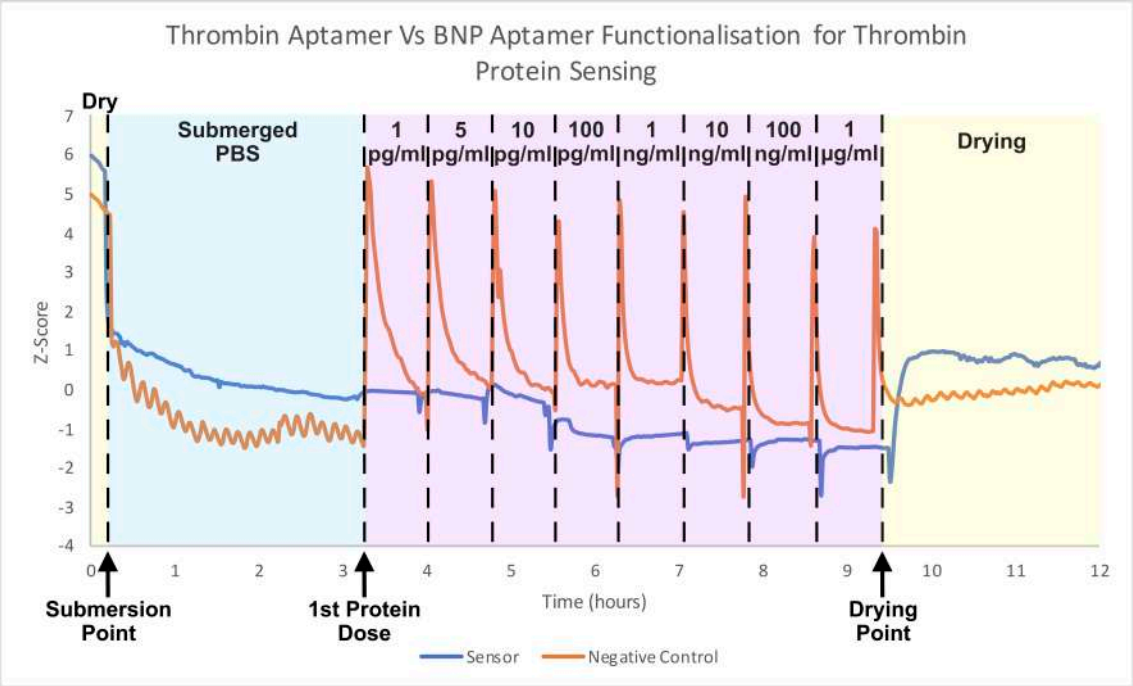


Figure 6.24: Real-time 12 hours measurement: Averaged Z-score values plotted from averaged resistance data. Thrombin-aptamer positive control vs BNP-aptamer negative control, after 3 hour stabilisation period. PBS spiked with concentrations of αThrombin protein introduced at 45 minute intervals (PT-MVD Chips).

The decrease in resistance at each concentration of the thrombin added to the thrombin-aptamer chips can be seen. However, a similar trend is also visible in the BNP-aptamer chips. It is difficult looking at the normalised data alone to determine changes due to αthrombin binding.

Using the original IV measurement data, average resistances data was calculated from 10 data points from the dry, submerged for 3 hour and 3 hours dry sections of the experiment. Table 6.6 shows the resistances taken dry, submerged and dry

post sensing. The change in resistance from submerged to dry post measurement is 42.08 ±11.62 % in the negative control whilst the sensor produces a much smaller change 5.91 ±0.17 %.

Table 6.6: Table showing the average resistances calculated at key stages of sensing experiment for thrombin-aptamer and BNP aptamer (Negative control) graphene sensors.

	Initial Dry Resistance (Ω)	3 Hours Submersion Resistance (Ω)	Final Dry Resistance (Ω)
Sensor Average	22652 ±2140	10976 ±3308	11619 ±3485
Negative Control Average	5961 ±1852	4425 ±838	6385 ±1705

Using the calculated resistance from the IV measurements, the resistance change for each concentration of αthrombin was calculated. To avoid the sharp initial change in resistance seen at the application of the protein solution, the data from the second half of the 45 minute protein incubation period was used to calculate the average resistance.

Figure 6.25 shows the average change in resistance from submerged baseline at each concentration across repeat experiments have been calculated. The resistance change follows a pattern in the sensor based chips decreasing with increase in αThrombin concentration. In contrast the negative control shows little to no change in resistance with applied concentration of αthrombin.

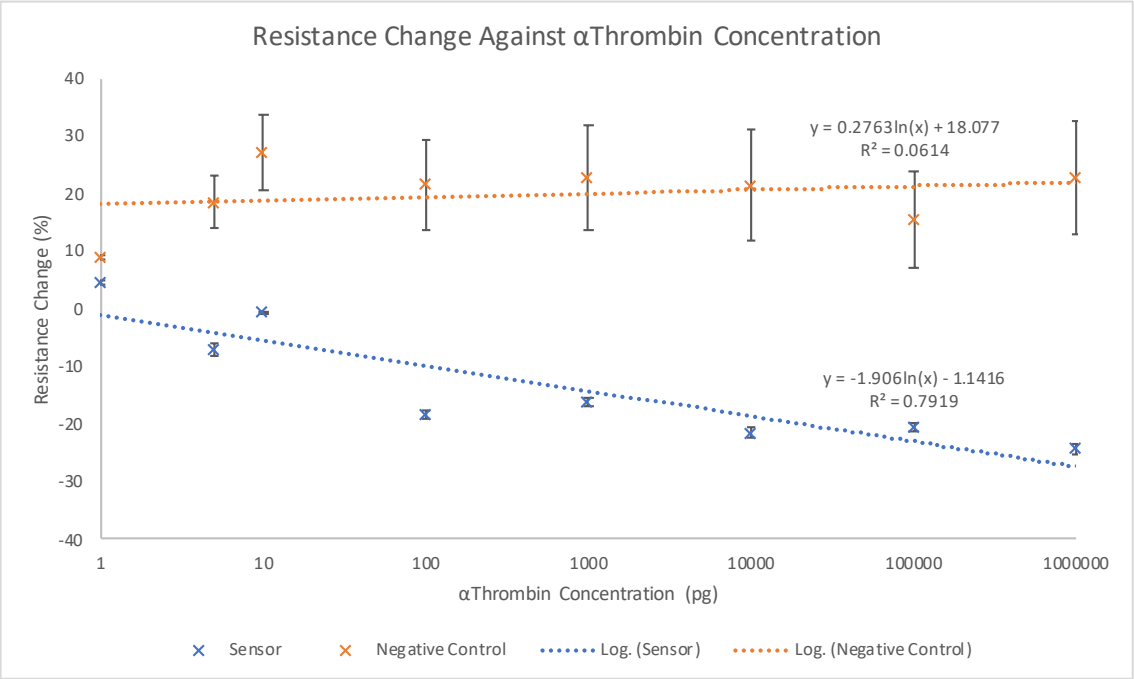


Figure 6.25: Resistance change calculated from the measured resistance of the thrombin-aptamer and BNP-aptamer functionalised chips after 3 hours of submersion in PBS. In response to increasing concentrations of αthrombin.

The first concentrations of 1-100 pg/ml appeared to see the largest resistance change in the thrombin-aptamer functionalised sensor. The slope of these first 4 data points was calculated as -0.185 % per pg/ml, the slope of the last 5 data points was calculated as -5.44 x10^{-6} % per pg/ml. This suggests the graphene sensor is highly sensitive in the 1-100 pg/ml region and above 100 pg/ml the sensor is saturated.

These early results show signs that the thrombin-aptamer functionalised graphene sensor effectively responds to specific binding as the negative control shows negligible signs of resistance change with the increasing concentration of αThrombin.

This could lead to a diagnostic sensor with qualitative and quantitative capability. A quantitative sensor is required for certain diagnostic assays that require information of protein concentration within specific ranges [22].

To explain the change in resistance it is important to understand how the aptamer binding to thrombin causes a reorientation of the aptamer. Aptamers can

reorient closer to graphene surface hole-doping the sensor (e.g. dopamine, glucose). Whilst other aptamers can reorient away from graphene channels and electron-dope the graphene surface (e.g. serotonin, S1P) [23].

Previously studies have shown an increase in graphene resistance due to the thrombin binding, (these sensors were not fabricated with the same blocking molecule systems and could suffer interference from the solution) [2]. However, the change in resistance during the real-time experiments will be determined by the starting and end position of the Dirac point (doping shift). Figure 6.26 shows FET-style Dirac point measurements, performed using IV probe station on dried PT-MVD chips after functionalised (aptamer and PEG-pyrene) and after thrombin sensing real-time experiment. The functionalised chips Dirac point has height of approximately 10 kΩ whilst the thrombin sensing chip has a height of 3 kΩ, the slope of the Dirac points can be used to calculate the carrier mobility of the graphene channel equation details found in the Appendix [24]. A decrease in slope means a reduction in carrier mobility of the graphene after the thrombin sensing experiment binding. This could explain the resistance decrease behaviour seen in the real-time based sensing experiments.

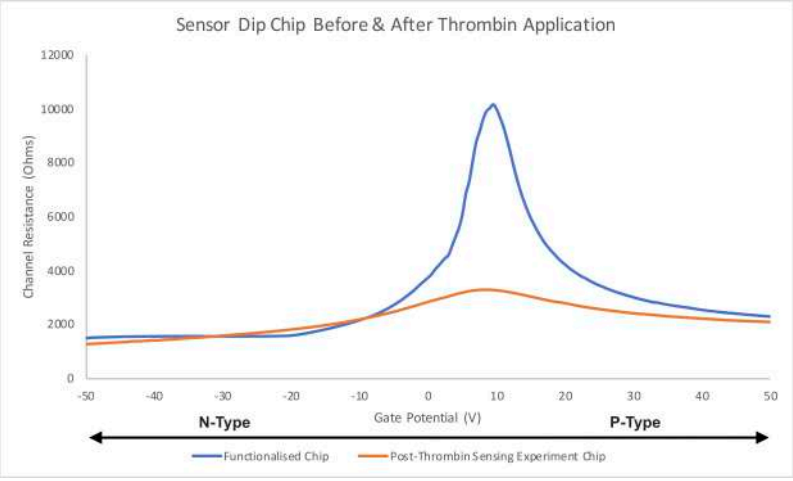


Figure 6.26: Gated FET (Dirac point) measurement of thrombin-aptamer functionalised Dip Chip before and after αthrombin exposure in real-time sensing experiment (Figure 6.24).

The pre-sensing submersion times (equalisation time) were determined in the di H_2O submersion and were shown to be similar in PBS submersion experiments (3-4 hours). This equalisation time was used during the thrombin sensing experiments to create a better test system and reduce error. This allowed the resistance change due to the addition of the thrombin could be isolated from the change due to submersion in the aqueous environment.

This study did not look into the consistency of this equalisation time. However, to translate this technology into a point of care testing system this equalisation time would need to be removed from the test set up. One approach would be to study the repeatability of the equalisation time and whether this resistance change could be subtracted from the measurements change in resistance. Therefore the sensor could be packaged in its dry state and the adsorption of water would be corrected for during sensing.

Alternatively a much better approach would be to use a hydrogel component which is applied to the sensing surface during the packaging of the device. This remains on the graphene surface whilst packaged and during operation. This way the graphene would be kept under a constantly hydrated environment with a set pH (matching sample solution) and ion concentration. The "blood" sample would make contact with the hydrogel and the proteins of interest would be able to diffuse through the hydrogel and bind to the bio-receptor on the graphene surface. This approach has been tested and shown to provide a detection limit of 0.2 mM and does not require the extended equalisation time window [25].

6.4 Summary

Electromagnetic noise was eliminated for electrical measurements of "Dip Chip" graphene devices via electrical shielding using a Faraday cage. The Auto-0 function appears to reduce the current drift in the measurement system when turned on and for real-time based experiments should be used for graphene devices.

With regards to the storage of graphene samples, although the use of vacuum

dessication has benefits for long term graphene storage, reducing risk of contamination, prior to performing IV based measurements, the graphene should be removed from vacuum storage for 3-4 days prior to the experiment. Additionally a set of real-time measurements should be performed prior to measurement to create a baseline resistance of the device (e.g. 3-4 hours). These extra measurements are suggested to have some joule heating/cleaning effect on the graphene if residues are present. This will allow changes due to sensing can isolated from changes due to heating/cleaning improving accuracy of the IV measurement.

The comparison of PT-SPI and PT-MVD Chips with respect to resistance change, in solutions of di H_2O and solvents, both chips respond to submersion with opposing changes in resistances (PT-SPI = increase in resistance, PT-MVD = decrease in resistance). This does not give an indication of which chip would best perform regarding sensing. However, the PT-MVD Chip has a measurable (definable Dirac point) and previous Raman data (Passivation & Packaging Chapter), showed a cleaner low defect graphene sheet. Therefore PT-MVD Chips were taken forward to the functionalisation and sensing based experiments.

Further information gathered from submersion and drying experiment focused around the resistance change seen due to H_2O, PBS and IPA exposure. Using the real-time data for submersion in the different solutions, the stabilisation times of the submerged graphene and also the stabilisation once the device is returned to dry ambient conditions, could be calculated. A minimum stabilisation time in PBS of 3 hours was used in the αthrombin sensing experiments.

The sensing experiment was not fully optimised in terms of automation and timings between cleaning steps and droplet spreading for both functionalisation and application of αthrombin spiked solutions. However, when the resistance change data was analysed a change in resistance could be seen related to αthrombin concentration in the Sensor based chips and but no trend could be seen in the Negative control. This indicates that the effect of non specific binding / physio absorption effects is negligible to the sensor performance. The graphene sensor platform is most sensitive 1-100 pg/ml concentrations, the sensitivity was estimated at a resistance

change of 0.2 % per pg/ml. Using the graphene sensor that has been optimised throughout this work, real-time visualisation of the thrombin protein binding to a graphene bound bio-receptor has been achieved. This is the first stage in producing an effective protein detection system for point of care diagnostics.

Bibliography

[1] Ryan Michael Bigham. Development of process technology for silicon and graphene biosensor devices. Technical report, Swansea University, 2019.

[2] Yanping Wang, Yinghong Xiao, Xiaoling Ma, Na Li, and Xiaodi Yang. Label-free and sensitive thrombin sensing on a molecularly grafted aptamer on graphene. *Chemical Communications*, 48(5):738–740, 2012.

[3] Bin Deng, Yanwen Lin, Chuan Wang, Feng Li, Zhixin Wang, Hongquan Zhang, Xing-Fang Li, and X Chris Le. Aptamer binding assays for proteins: the thrombin example—a review. *Analytica chimica acta*, 837:1–15, 2014.

[4] Bin Hong, Junhai Kai, Yongjie Ren, Jungyoup Han, Zhiwei Zou, Chong H Ahn, and Kyung A Kang. Highly sensitive rapid, reliable, and automatic cardiovascular disease diagnosis with nanoparticle fluorescence enhancer and mems. In *Oxygen Transport to Tissue XXIX*, pages 265–273. Springer, 2008.

[5] Arne Quellmalz, Anderson D Smith, Karim Elgammal, Xuge Fan, Anna Delin, Mikael Östling, Max Lemme, Kristinn B Gylfason, and Frank Niklaus. Influence of humidity on contact resistance in graphene devices. *ACS applied materials & interfaces*, 10(48):41738–41746, 2018.

[6] Joel Moser, Amelia Barreiro, and Adrian Bachtold. Current-induced cleaning of graphene. *Applied Physics Letters*, 91(16):163513, 2007.

[7] Yaping Dan, Ye Lu, Nicholas J Kybert, Zhengtang Luo, and AT Charlie Johnson. Intrinsic response of graphene vapor sensors. *Nano letters*, 9(4):1472–1475, 2009.

[8] Dae Kim, Hong Oh, Woo Park, Dong Jeon, Ki Lim, Hyung Kim, Byoung Jang, and Kwang Song. Detection of alpha-fetoprotein in hepatocellular carcinoma patient plasma with graphene field-effect transistor. *Sensors*, 18(11):4032, 2018.

[9] Christos Melios, Cristina E Giusca, Vishal Panchal, and Olga Kazakova. Water on graphene: review of recent progress. *2D Mater.*, 5(2):022001, 2018.

[10] Anderson D Smith, Karim Elgammal, Frank Niklaus, Anna Delin, Andreas C Fischer, Sam Vaziri, Fredrik Forsberg, Mikael Råsander, Håkan Hugosson, Lars Bergqvist, et al. Resistive graphene humidity sensors with rapid and direct electrical readout. *Nanoscale*, 7(45):19099–19109, 2015.

[11] Fazel Yavari, Christo Kritzinger, Churamani Gaire, Li Song, Hemtej Gulapalli, Theodorian Borca-Tasciuc, Pulickel M Ajayan, and Nikhil Koratkar. Tunable bandgap in graphene by the controlled adsorption of water molecules. *small*, 6(22):2535–2538, 2010.

[12] Yinxiao Yang, Kevin Brenner, and Raghu Murali. The influence of atmosphere on electrical transport in graphene. *Carbon*, 50(5):1727–1733, 2012.

[13] Yue Hong, Sanmei Wang, Qiang Li, Xin Song, Zegao Wang, Xi Zhang, Flemming Besenbacher, and Mingdong Dong. Interfacial icelike water local doping of graphene. *Nanoscale*, 2019.

[14] Ciril Reiner-Rozman, Melanie Larisika, Christoph Nowak, and Wolfgang Knoll. Graphene-based liquid-gated field effect transistor for biosensing: Theory and experiments. *Biosensors and Bioelectronics*, 70:21–27, 2015.

[15] Nan Lei, Pengfei Li, Wei Xue, and Jie Xu. Simple graphene chemiresistors as ph sensors: fabrication and characterization. *Measurement science and technology*, 22(10):107002, 2011.

[16] Lijin George, K Shakeela, G Ranga Rao, and Manu Jaiswal. Probing the electric double-layer capacitance in a keggin-type polyoxometalate ionic liquid gated graphene transistor. *Physical Chemistry Chemical Physics*, 20(27):18474–18483, 2018.

[17] Zhen Wang, Kongyang Yi, Qiuyuan Lin, Lei Yang, Xiaosong Chen, Hui Chen, Yunqi Liu, and Dacheng Wei. Free radical sensors based on inner-cutting graphene field-effect transistors. *Nature communications*, 10(1):1544, 2019.

[18] Wei Zhan, Zhijun Xu, and Xiaoning Yang. Molecular interlayer intercalation of ethanol-water mixture towards go laminated membranes. *Separation and Purification Technology*, page 116029, 2019.

[19] Abhishek Tyagi, Xiaotian Liu, Irfan Haider Abidi, Zhaoli Gao, Byung Min Park, Xiangze Zeng, Xuewu Ou, Aldrine Abenoja Cagang, Minghao Zhuang, Md Delowar Hossain, et al. Modular functionalization of crystalline graphene by recombinant proteins: a nanoplatform for probing biomolecules. *Nanoscale*, 10(47):22572–22582, 2018.

[20] Thanawit Kuamit, Manussada Ratanasak, Chompoonut Rungnim, and Vudhichai Parasuk. Effects of shape, size, and pyrene doping on electronic properties of graphene nanoflakes. *Journal of molecular modeling*, 23(12):355, 2017.

[21] A Bhaumik, A Haque, MFN Taufique, P Karnati, R Patel, M Nath, and K Ghosh. Reduced graphene oxide thin films with very large charge carrier mobility using pulsed laser deposition. *J. Mater. Sci. Eng*, 6(4):1–11, 2017.

[22] Francesco Padovani, James Duffy, and Martin Hegner. Nanomechanical clinical coagulation diagnostics and monitoring of therapies. *Nanoscale*, 9(45):17939–17947, 2017.

[23] Nako Nakatsuka, Kyung-Ae Yang, John M Abendroth, Kevin M Cheung, Xiaobin Xu, Hongyan Yang, Chuanzhen Zhao, Bowen Zhu, You Seung Rim, Yang Yang, et al. Aptamer–field-effect transistors overcome debye length limitations for small-molecule sensing. *Science*, 362(6412):319–324, 2018.

[24] Hua Zhong, Zhiyong Zhang, Haitao Xu, Chenguang Qiu, and Lian-Mao Peng. Comparison of mobility extraction methods based on field-effect measurements for graphene. *AIP Advances*, 5(5):057136, 2015.

[25] Hamed Hosseini Bay, Richard Vo, Xiaochuan Dai, Huan-Hsuan Hsu, Zhiming Mo, Siran Cao, Wenyi Li, Fiorenzo G Omenetto, and Xiaocheng Jiang. Hydrogel gate graphene field-effect transistors as multiplexed biosensors. *Nano letters*, 19(4):2620–2626, 2019.

Chapter 7

Conclusion

The aim of this work was to develop a graphene-based biosensor platform for direct detection of a blood clotting biomarker (Thrombin protein). This involved analysing and optimising the current fabrication process flow as well as developing alternative sensor design for added sensor functionality.

The use of chemical vapour deposition (CVD) grown graphene is widely used due to its high quality, large area growth and low cost production. Lattice structure damage and photoresist residue on the graphene surface can cause a reduction in carrier mobility and often results in hole-doping, which causes the Dirac point of the graphene channel to move further from 0 V. Therefore, graphene sensor fabrication been optimised in this thesis to reduce total damage and residues present on the graphene. The CVD growth and the graphene transfer process for sensor fabrication were outsourced to professional suppliers who use a wet graphene transfer process. However, the wet transfer process involves directly applying photoresist/polymers to the graphene surface, therefore a residue is often present on the graphene regardless of sensor fabrication.

The novel residue-free vacuum transfer system developed within in Chapter 1 of this thesis could allow a completely residue-free solution to graphene transfer. The process was partially successful, the pre-processing of the wafer was successfully optimised to contain vacuum dicing tracks (VDTs) and through silicon vacuum vias (TSVVs), these features were successfully etched out of the silicon substrate. When these structures were tested as part of the vacuum transfer rig the foil sheet was successfully held down onto the wafer surface producing a wrinkle free foil layer. The vacuum successfully held the foil in place during the addition of the liquid etchant and remained in place during the hours of etching. The graphene

was transferred in small patches onto the SiO_2 substrate identifiable using Raman single point measurements. However, this process was not successful at full graphene sheet transfer, a majority of the graphene self-adhered forming rolled up patches and delaminated from the SiO_2 surface. Further optimisation of the suction effect and graphene surface adhesion is required in future to produce full graphene channels using this process.

When comparing cost per chip and cost per graphene channel between the original Dip Chip design (3 graphene channels) and the optimised Dip Chip designs it was clear that the Shared Source design (5 graphene channels) decreased the cost per graphene channel from £7.22 to £4.33, a reduction of 40 %, whilst keeping the overall wafer/chip fabrication cost the fixed at £693.50. Drop cast functionalisation by aptamers was shown as an effective method of functionalisation for the Shared Source design to increase repeats per chip allowing it to be more cost-effective compared to the standard Dip Chip. The only disadvantage of the Shared Source design is that it is not suitable for electrochemical functionalisation and sensing; regardless of chip layout all graphene channels are connected and act as a single electrode so cannot be used for electrochemical functionalisation.

The Matrix design took the maximum graphene channels per chip even further to 9 graphene channels using the same number of contact electrodes (6). This process flow required additional steps and machine time so the total cost per wafer and chip increased by 45 % from £693.50 to £1007.50. However, the increase in graphene channels allowed a reduction in the total cost per channel was to £4.11, a decrease in cost of 5 % compared to Shared Source design. The marginal cost per channel decrease would depend on the G-FET foundry so would need to be analysed individually per foundry. Despite the cost reduction of the Matrix design being marginal, the main advantage of the design is the total number of channels per chip. This increase to 9 channels enables more repeats per sensor in the same solution leading to more accurate diagnostics. Furthermore, with appropriate multiplex packaging, each of the 9 channels could be functionalised with a different bio-receptor resulting in a more efficient diagnostic system.

Table 7.1: Summary Table of Dip Chip Designs Part I

Dip Chip Design	Functionality	Graphene Channels Per Chip	Fabrication Cost Per Channel (£)	Fabrication Cost Per Wafer (£)
Dip Chip Standard	(a) 3 Resistor Measurements (b) 3 Gated Measurements Using Substrate Si (c) 3 Electrochemical Measurements	3	7.22	693.50
Shared Source Electrode	(a) 5 Resistor Measurements (b) 5 Gated Measurements Using Substrate Si (c) 1 Electrochemical Measurement	5	4.33	693.50
Matrix	(a) 9 Resistor Measurements (b) 9 Gated Measurements Using Substrate Si (c) 1 Electrochemical Measurement	9	4.11	1007.50

Table 7.2: Summary Table of Dip Chip Designs Part II

Dip Chip Design	**Functionality**	**Graphene Channels Per Chip**	**Fabrication Cost Per Channel (£)**	**Fabrication Cost Per Wafer (£)**
Inverted MOSFET	(a) 3 Resistor Measurements (b) 3 Gated Measurements Buried Metal Electrode (c) 3 Electrochemical Measurements	3	11.43	1097.50
Multiplex	(a) Multiplex 3 times Functionalisation (b) 3 Resistor Measurements (c) 3 Gated Measurements Using Substrate Si (d) 3 Electrochemical Measurements	3	7.22	693.50

The Inverted MOSFET (metal–oxide–semiconductor field-effect transistor) design was shown to effectively perform gated FET style measurements on graphene channels in Chapter 1. The graphene channels conductivity was measured at a range of gate voltages showing the change in charge carriers under the effect of the electric field. The Inverted MOSFET device was compared to a standard Dip Chip device using the P-type bulk silicon as the gate electrode, the bulk silicon gate appeared to show a greater degree of resistance change 423 $\pm 96\ \Omega/V_G$ compared to the Inverted

MOSFET design (281 $\pm$71 Ω/V_G). However, this could be due to the metal gate only covering roughly half of the graphene channels area. Additionally, depending on the position of the Dirac point for the graphene channel the shift in conductivity would depend on the proximity to the Dirac peak and slope of the Dirac peak.

The Multiplex design was tested using a drop-cast functionalisation method which allowed for each graphene channel to be encapsulated with a separate solution. In principle, this was shown to be effective with small volumes (10 μl) applied to the surface for a small time window 5-15 minutes. However, for drop-cast π-π stacking aptamer functionalisation the timescales were over 8 hours in length and during this extended period, the hydrophilic surface caused the solution to spread across the chip. To test the method two graphene channels were functionalised simultaneously with two separate aptamers. Due to the functionalisation time being over 12 hours the two solutions merged and cross-contaminated both graphene surfaces. Even if the multiplex functionalisation was performed sequentially the spreading of the solution would have contaminated the other graphene channels making drop-cast multiplex functionalisation using this design not possible.

The Multiplex design was later tested during the investigation into electrochemical multiplex functionalisation. During these experiments, electrochemical functionalisation was first shown to be possible using a standard Dip Chip. Using optical microscopy, SEM and voltammetry measurements cross-contamination was identified due to graphene contact with each functionalisation solution. Using the Multiplex Design chip and microfluidic packaging the functionalisation of Au and pDAN was successfully performed on isolated graphene channels. This prevented cross-contamination as the other graphene channels did not come into contact with the solution. This showed that multiplex functionalisation was possible with the Multiplex design chip. This also suggests that a drop-cast π-π stacking functionalisation would be possible using the Multiplex design chip in combination with the microfluidic packaging.

The standard Dip Chip design was tested using the PCB connector system, first the speed of handling and taking measurements using PCB connector vs. IV Probe

Station was compared. The results showed very similar time lengths required for both measurement systems (25.2 ±3 s and 23.8 ±1.9 s respectively. However, using modified measurement software it was shown that the Dip Chip with PCB connector was much faster and easier to perform multiple measurements. All graphene channels were measured simultaneously with the same time spent handling the chip (7.9 s per channel). The PCB connector also enabled the use of full submersion IV measurements to be performed in various solutions. Overall this approach has enabled the development of the real-time liquid submersion research despite it being costly in terms of silicon chip size (Dip Chip size 182 mm^2 Resistor Chip size 16 mm^2.

The fabrication processes for both the Pre-Transfer and Post-Transfer routes were investigated and optimised at each process step. The Pre-Transfer process requires annealing to prevent graphene delamination during the photolithography steps, this achievable with both rapid thermal annealing (RTA) and tube furnace annealing (TFA) systems. Raman data from both methods show strong indicators of graphene doping, 2D/G ratio reduction below the ideal (Ratio = 2) of pristine graphene to 0.911 for TFA and 1.08 for RTA. There were little signs of graphene lattice (SP^2) damage both methods produced D/G ratios within the range of blank graphene (0.05-0.15). The Post-Transfer fabrication process appears to be the preferred route as it does not require a pre-process anneal step. The photoresist used for the Pre-Transfer process was also investigated, the multi-layer photoresist system was shown to produce the most residue with additional Raman peaks around 1400 cm^{-1}. The Raman spectroscopic mapping showed the single layer positive photoresist (with and without additional solvent cleaning), appeared to produce no residue peaks in this region. The damage levels did not exceed the D/G ratio of blank graphene. The 2D/G ratio remained in the range of annealed graphene (0.84-1.24) suggesting no significant doping changes. The positive single layer photoresist was also tested with the Post-Transfer process and showed no signs of residue peaks, damage or doping from the Raman data. The metal used for graphene contacts were tested in both process flows, data suggested that the average device resistance

was lowest using Cr (5255 Ω for a 500 μm x 100 μm channel), as the adhesion metal in the Pre-Transfer process. The noble metal used for the Post-Transfer process was not significant. The data does suggest that on average the resistance of Pre-Transfer devices is lower than Post-Transfer devices (0..5 k Ω on average), this can be explained by the PVD step creating side contacts through the metal deposition in the Pre-Transfer process.

The introduction of an yttrium sacrificial layer into the Pre-Transfer process was shown to be beneficial in removing residues previously seen with the multilayer photoresist process. The Raman spectra of the Yttrium and multilayer processed chips showed no sign of the additional peaks seen around 1400 cm^{-1} for the multilayer process alone. The sacrificial layer process also reduced the average resistance of the graphene channels and also decreased the inter-device resistance variation compared to the standard Pre-Transfer process (4998 ±906 Ω and 5315 ±2371 Ω. There were fewer broken devices on average using the sacrificial layer increasing process yield (7-8 %). In general, the yttrium sacrificial layer process seems very beneficial even though it increases the total number of process steps by four (one evaporation step, and three wet etch steps).

When comparing the optimised Pre-Transfer and the Post-Transfer process flows the overall graphene quality in terms of residue, damage and doping are all better with the Post-Transfer process. The device yields are both very similar with both processes, the variation in device resistances appears total devices within 10 % of the median between 10-15 % for Pre-Transfer Process and 14-21 % for Post-Transfer Process. Overall the Post-Transfer process appears to be the better route.

Table 7.3: Summary Table of Fabrication Process Flows

Fabrication Process	**Contamination To Graphene Surface**	**Graphene Damage D/G Ratio**	**Graphene Stress/Strain 2D/G**	**Doping Shift Of Graphene**	**Fabrication Cost Per Wafer (£)**
Pre-Transfer	Photoresist Residue Present	0.066 ±0.015	1.106 ±0.104	Hole-Doping 50+ V	933.50
Pre-Transfer + Yttrium	None Reported	0.099 ±0.045	0.957 ±0.125	Hole-Doping 50+ V	1003.50
Post-Transfer	None Reported	0.046 ±0.014	2.545 ±0.266	Hole-Doping 50+ V	693.50

The next stage of fabrication optimisation focused on the passivation material used and method to produce the passivation window. Various processes (Spin Coating, PVD, PECVD, MVD) were trialled to improve from the previously developed screen-printing method. Permanent polymer EpoClad was shown to be the most effective method for direct patterning of a polymer-based passivation, it did not appear to increase photoresist residues there were no signs of additional Raman peaks near the 1400 cm^{-1} wavelength. The method of developing EpoClad post-exposure in pure Acetone had some negative side effects, causing partial delamination of the graphene breaking the channels. The PECVD deposited dielectrics caused damage to the graphene when deposited directly onto the graphene's surface. When using an yttrium sacrificial layer, PECVD SiO_2 was deposited and the passivation window directly etched through to the yttrium layer with the graphene channel remaining intact and undamaged. The IV data suggested a small increase in resistance when compared non-passivated devices, increasing from 8599 ±1420 Ω to 10436 ±1466 Ω. Damage was seen to be within the normal D/G ratio range (0.0991). The MVD deposited Al_2O_3 process was successfully deposited and passivation window etched (TMAH etchant) without causing damage to the graphene surface, the MVD Al_2O_3 on average had a lower D/G ratio post-passivation (Pre-passivation calculated as 0.0655 and post-passivation 0.0138). This suggests the MVD process can effectively heal the graphene of structural damage. The MVD process also electron-doped the graphene channel moving the Dirac point closer to 0 V (-11 V compared to 50+ V). When comparing the two dielectric processes the MVD Al_2O_3 produced better quality graphene post-fabrication.

Table 7.4: Summary Table of Passivation Techniques

Passivation Technique	**Contamination Of Graphene Surface**	**Graphene Damage D/G Ratio**	**Doping Shift Of Graphene**
EpoClad	None Reported	0.109 ±0.032	Hole-Doping 50+ V
SiO_2 With Yttrium	None Reported	0.082 ±0.016	Hole-Doping 50+ V
Al_2O_3	None Reported	0.014 ±0.008	Electron-Doping -11 V

PDMS moulded microfluidic packaging was trialled on the Dip Chip graphene devices, the plasma bonding proved successful and liquid could directly flow over the graphene channel. However, the bonding process is not reliable due to the manual alignment and short activation window. The direct 3D printing of a microfluidic cartridge successfully produced a liquid-tight seal (2-hour liquid test) and proved to be more reliable for alignment to the Dip Chip. This method was able to produce a microfluidic channel across a standard Dip Chip, and a more complex Multiplex cartridge aligning 3 microfluidic channels to each of the graphene channels.

Microfluidic devices were developed and tested for biological sample pre-processing. Using whole blood these designs were tested with a syringe driver to separate the blood and collect a volume of plasma. The pinch point fractionation system was showed to be the most effective at collecting plasma. The device geometries were optimised, the most effective device had the highest flow rate ratio (24:1) between the plasma extraction channel and the whole blood waste channel. This device could effectively reduce the total number of red blood cells (from $5.4x10^6$ to $0.7x10^6$ per μl) and white blood cells (from 5700 to 1100 per μl), delivering a plasma sample to a microfluidic chamber. This device was tested using controlled flow rates (syringe pump) its role in a point of care system would need to be developed further.

The real-time measurement chapter looked at the optimisation of IV measure-

ments of graphene submerged in liquids and solvents. The information regarding stabilization times (3-4 hours) in water and PBS were used to develop the thrombin protein sensing experiment. MVD passivated Post-Transfer process fabricated chips were chosen for use in the protein binding experiment due to their low resistances and measurable Dirac points within the gated sweep range. The thrombin aptamer functionalised chips were shown to produce a resistance decrease with the increasing concentration of αthrombin protein. The graphene is most sensitive in the low concentration range of 1 – 100 pg/ml, producing a resistance change of 0.2 % per pg/ml of αthrombin. The BNP aptamer (used as the negative experimental control) did not show any trend with increasing concentrations of /$alpha$thrombin. This helps validate the thrombin aptamer result suggesting that the decrease in resistance scene was due to protein binding and changing the doping/carrier concentration of the graphene channel. This result achieves the aim of a real-time protein binding system which can be used to study future surface functionalisation approaches and help develop a G-FET biosensor platform for POCD,

7.1 Future Work

Through this work multiple facets of the biosensor design and fabrication process have been optimised. The sensor was shown to effectively detect low concentrations of thrombin protein in real-time. The next stages of development will aim to reduce fabrication costs further, develop a multiplex functionalised sensor for multiple diagnostic biomarkers.

For the residue-free graphene transfer system, the surface treatment of the wafer can be investigated further to look at increasing hydrophobicity and improve graphene adhesion preventing etchant from being trapped under the graphene sheet. The size of the die and uniformity of the vacuum applied can also be investigated, smaller die and an increase in vacuum features would increase the uniformity of the vacuum across the graphene Cu foil.

Whilst assessing the designs tested in this thesis it is clear that the most effective

way to reduce cost per graphene channel is to implement a Matrix design with additional contact electrodes (plus the 1-2 contacts for gating). The number of graphene channels cubes with the number of drain contact electrodes, increasing the number of contacts used from 6 to 10 would increase the number of graphene channels in the Matrix design from 9 to 5. This would require a complete redesign of the Dip Chip as well as the connection system. The way to reduce total sensor costs is to reduce the total area of each chip, this would allow more chips to be fabricated per wafer. This again would require a complete redesign of the Dip Chip and connector system; the electronic packaging of the chip needs to be investigated further. Reducing die size and wire bonding to a small PCB which in turn can be connected to the measuring system for testing would help reduce cost per sensor. However, to decrease die size further without reducing total electrical contacts would require newer approaches such as metal filled TSVs and flip-chip bonding for 3D integration.

The Inverted MOSFET design is only a proof of concept stage and has multiple applications for future research. Firstly, for sensor-based research, a real-time sensing experiment can be investigated using gated field-effect measurements to track the doping shift of the graphene channel during the drop-cast functionalisation process and the liquid drying process to further understand the changes that occur at each step. Following up with an investigation into the sensing process itself comparing the level of analyte quantification using a gated measurement compared to resistance- based measurement. The other route for research could involve a redesign with additional contact electrodes so that multiple buried gates can be implemented on a single chip tuning each channel individually to hold the gate voltage at each channels Dirac peak so that the sift due to binding can be measured as larger change making the device more sensitive.

For the Multiplex sensor design spreading the graphene channels across the surface was not effective for drop-cast functionalisation. However, a simple permanent photoresist or epoxy screen-printed coating could provide an open reservoir around each graphene channel. The hydrophobicity of these polymers would keep the liquid

within the reservoir preventing the functionalisation solution from spreading across the chip's surface. If these polymers did not have the required height to trap the functionalisation solution, a 3D printed microfluidic package could be used instead. This process will become more complicated and take up more space with additional multiplex bio-receptors. Alternatively, If the chips were being redesigned to miniaturise the silicon footprint and then bond the small die to a PCB, this could be taken a step further and multiple chips could be bonded to a single PCB each of these sensor chips could be functionalised separately using an open drop cast method then combined onto a single PCB producing a multiplex sensor platform.

Device fabrication optimisation still has some areas that can be investigated further. The length, width and geometry of the graphene channel has not been investigated in this body of work. How changing these parameters could affect device resistance and sensitivity to analyte detection should be investigated. The use of annealing to clean graphene and improve graphene metal contact resistance could be explored further. This will become more relevant as graphene length decreases reducing channel resistance to a point where contact resistance may dominate the measured resistance of the device. Lastly to improve reliability and yield it would be worth investigating parallel graphene channels per resistance measurement. This could increase sensor yields as each graphene region would be made up of multiple channels if one graphene channel is disconnected the sensor could still operate effectively. A compromise would need to be made in terms of lowered resistance and possibly a reduction in sensitivity against the increased yield of working devices.

Future research to increase graphene wafer yield should also include advancements in graphene transfer systems and graphene adhesion to the base substrate. Adhesion was the primary problem throughout the optimisation of the Pre-Transfer process. Alternatively using the Post-Transfer process and improving the contact resistance of the graphene/metal contacts or the use of a shadow mask to produce the metal contacts on the graphene would help increase yield. The introduction of "Side Contacts" where multiple metal carbide bonds can form and decrease contact resistance should be investigated further. The graphene channel geometry can

also be changed to increase yield and potentially increase total channel number by decreasing the size of the graphene channels.

Looking into passivation further PECVD silicon nitride as a passivation material should be investigated potentially as an interlayer-based passivation material. Using the new APS (SPTS UK) dielectric etch tool etching the passivation window would be achievable using the built-in feedback system. This would enable the etch to stop once the Nitride layer has been etched through to the SiO_2. This approach combined with the use of a sacrificial protective layer such as Yttrium could result in an undamaged graphene sheet post Si3N4 etch and result in a good passivation technique. This could be used for a multilayer device such as the Matrix Design or future combination designs. From a design standpoint reducing the size of the passivation and changing its geometry to fully "picture frame" the graphene should be investigated using different materials to alter the carrier mobility and doping of the graphene channel.

The future of packaging research needs to be investigated regarding the use of microfluidics for functionalisation, sensing or functionalisation and sensing. The level of microfluidic sample pre-processing will depend heavily on the location of the target analyte whether it is found in the bloodstream, inside cells or is the cell itself. 3D printed cartridges are not up-scalable beyond the research phase at this current time point in technology but have been essential in prototyping a working design. Laser cutting or injection moulding systems can be investigated for upscaling and commercialisation once designs have been tested and finalised using the 3D printing system.

There are many approaches to achieve blood cell separation by laminar microfluidics the difficulty with the designs used in this research is the control of flow rates. This can be achieved with the use of pumps, even in a handheld point of care device. For future research, a purely capillary driven system should be investigated to combine with the Dip Chip packaged. With fewer moving parts operation of the sensor will be much easier to implement as well as reducing material/fabrication costs. A capillary system involving a filter-based system small volume microfluidic channels

would be best suited for this area of research and could lead to the end goal of a point of care diagnostic test where a patient would only need to supply a droplet of blood for an accurate diagnosis.

There are different approaches to real-time sensing that can be explored further, long term experiments would be beneficial with modifications to the software used to control the Keithley SMUs, longer duration measurements with more data points could be fully automated. This would allow for a long-term stability experiment of weeks/months for the graphene channels in ambient conditions as well as submerged in di H_2O and other solvents. Looking at the dielectric constant of the solvent and its effect on graphene resistance would also be worth investigating. An accurate temperature humidity detector connected to the measurement system would also be beneficial to see trends/changes in resistance due to atmospheric conditions would allow for more dry measurements to be performed more accurately.

During functionalisation, the 30 μl of solution would spread around the chip surface and the main mass of solution would not be focused on the graphene channel. The issue with a plain Al_2O_3 / SiO_2 passivated surface is the hydrophilic nature of the dielectric film. Due to the high surface tension of H_2O, a precipitate deposition effect (ring effect) will mean particulates are highly concentrated around the edge of the volume. With this volume spread across a larger area of the chip, the aptamer molecules could be unevenly distributed away from the graphene channel. As mentioned previously a hydrophobic ring structure/packaging would benefit both multiplex functionalisation but also standard all-channel functionalisation as well. Repeats of this experiment will be required to prove the real-time specific binding experiment. Knowledge gained from these real-time experiments suggests a longer stabilisation period in PBS prior to the first experiment. As well as a longer incubation period for the protein concentration on the graphene surface. Ideally, if the resources allowed a vertical submersion in 4 ml of PBS with the same pot being spiked by the αThrombin would allow for clearer visualisation without drying a re-stabilisation in each concentration of protein. The only difficulty with this style of experiment besides large volumes of protein would be the build-up of additional

protein concentrations without washing off non-specifically bound αThrombin, it would be difficult to accurately determine the true concentration of αThrombin in the solution pot.

The functionalisation process could also be investigated further. Aptamer concentration was not optimised or blocking molecule length. There are many factors for potentially improving functionalisation of the surface which can now be investigated as the system has been set up and a baseline of sensitivity has been achieved. The range of the αThrombin dilution could also be extended to test the sensitivity limits beyond mg/ml. Lastly, the use of the buried electrode gated chips would enable FET style Dirac point measurements to be made sequentially in the Dip Station setup. Being able to do real-time Dirac point measurements would give more information throughout the sensing experiment. Plotting the peak height, doping shift and even the slope can give additional information about the interactions on the graphene surface. With more information, the protein binding interaction and environmental surface interactions can be examined further leading the development of a POCD sensor with higher sensitivity and selectivity.

Planned Publications:

Effect of MVD aluminium oxide passivation of Graphene FET pH Sensor Performance

Appendix

8.1 Materials & Methods

8.1.1 Introduction: Centre for NanoHealth Cleanrooms

The graphene sensors developed within this work were fabricated and characterised using nano-fabrication based tools housed in the Centre for NanoHealth (CNH) Swansea University. The facilities comprise of a fully equipped class 1000 and 100 cleanroom used for the fabrication of the semiconductor integrated graphene chips. As well as a class 1000 biocleanroom that employed for the biochemical functionalisation / modification of the sensor surface, as well as for the electrical and electrochemical characterization of the sensor.

The centre also houses other analytical tools such as a Scanning Electron Microscope (SEM) and Energy dispersion X-ray spectroscopy (EDX) tool that can be used for examination of device features down to 1-10 nm. An atomic force microscope (AFM) that can determine device feature step height and surface roughness within 1nm. A Raman Spectrometer that can be used to measure graphene damage as well as identify chemical bonds of the chemistries applied to the sensor.

Additional to the facilities of CNH tools from other research centres across Swansea University were employed such as X-ray photoelectron spectroscopy (XPS) for graphene surface analysis. As well as Screen printing facilities from the Welsh Centre for Printing and Coating (WCPC).

8.1.2 Photolithography

Photolithography is an optical method used in the microfabrication industry to transfer a pattern onto a substrate. The basic principle is similar to traditional photography. A light source specifically UV 365 nm or 436 nm wavelength is shone

through a photo-mask onto a light sensitive polymer film "photoresist" on the surface of the substrate. The photo-mask consists of opaque and transparent sections that form geometric patterns that are transferred onto the photoresist, see Figure 8.1 for flow diagram of the whole process.

There are two main categories of photoresist; positive and negative and the category can be determined by the effect of UV exposure on the chemical solubility of the resist.

- Positive resist exposed to UV light becomes soluble when placed in resist developer. The unexposed regions will remain insoluble in the resist developer and remain on the substrate.

- Negative resist that is exposed to UV light becomes insoluble in resist developer and remain on the substrate. Whilst the unexposed regions will dissolve in the resist developer.

The insoluble resist forms a pattern that has been transferred from the photo-mask. This resist pattern can be used to protect the underlying silicon or glass from further treatments such as etching or chemical deposition. The resist can then be removed using a solvent clean revealing the unprocessed silicon beneath.

Positive Photoresist Process: A. Clean silicon wafer, 100 mm diameter, 0.5 mm thickness, N type doped. B. Positive photoresist AZ 9260 spin coated 3000 rpm for 30 seconds, softbaked 110 °C for 3.5 minutes. C. Resist exposed to UV 2000 mJ/cm^2 through photomask. D. Exposed photoresist wafer submerged in developer AZ 726 for 2 minutes. Exposed photoresist is soluble in AZ 726, removed using developer and rinsed in DI water then dried with compressed air. Negative Photoresist Process: 1. Clean silicon wafer, 100 mm diameter, 0.5 mm thickness, N type doped. 2. Negative photoresist AZ nLof 2070 spin coated 3000 rpm for 30 seconds, softbaked 100 °C for 5 minutes. 3. Exposed to UV 240 mJ/cm^2 through photomask. 4. Exposed photoresist wafer submerged in developer AZ 726 for 2 minutes. Exposed photoresist cross linked and no longer soluble in AZ 726, removed using developer and rinsed in DI water then dried with compressed air (Figure 8.1).

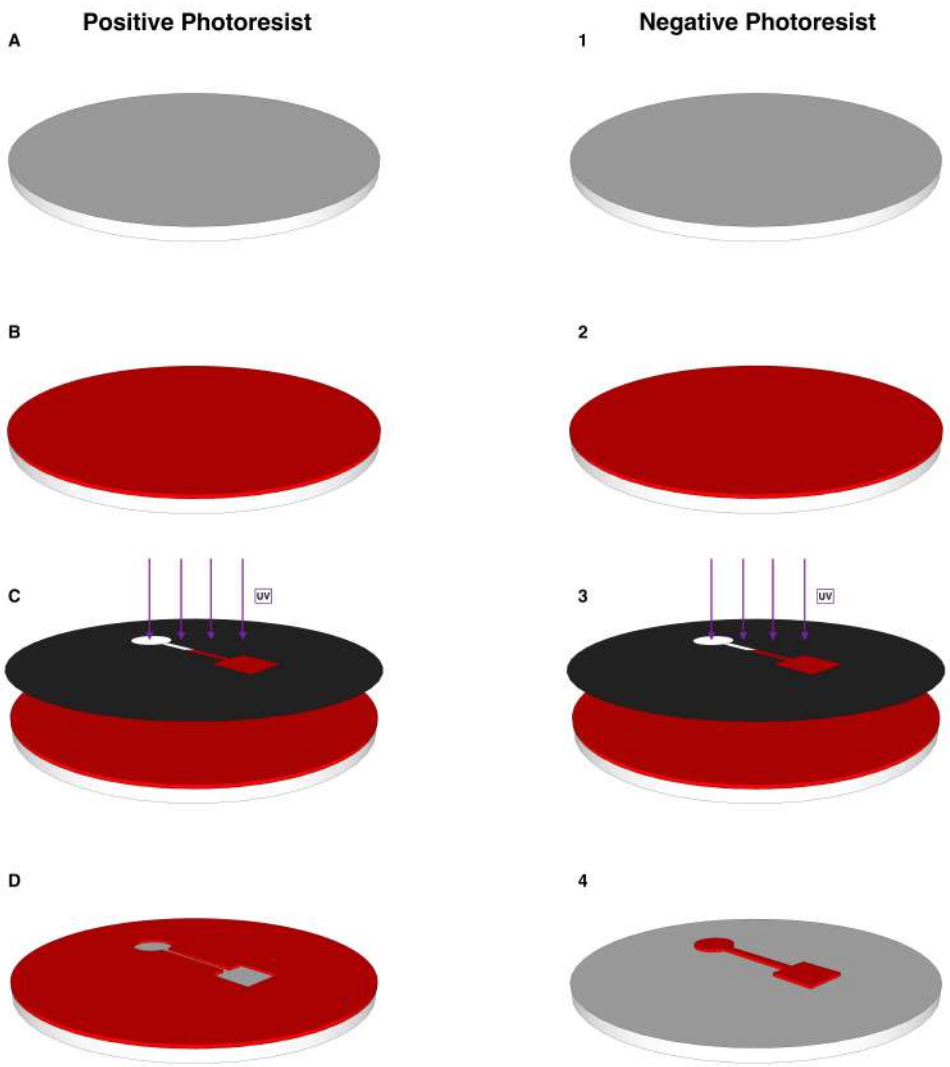


Figure 8.1: Photolithography full protocol.

Photolithography is an integral part of the electronics and semiconductor industry, as well playing a crucial role in the microelectromechanical systems (MEMS) industry over the last 20+ years. Microfabrication is a collection of techniques that include deposition, growth, etching, doping and etching. Lithographic techniques enable the design and layout of the device patterned and to be developed in combination with these other techniques.

8.1.3 PDMS

This is due to its optical transparency, physical flexibility and its changeable surface chemistry. PDMS has been used in micro-electro-mechanical-systems (MEMS) industry to create microfluidic device components. So as a working layer for this microfluidic device PDMS was a safe option to create the PDMS device and attain functionality.

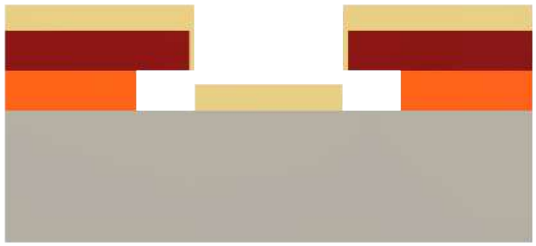
The fabrication of a polydimethylsiloxane (PDMS) device involves first creating a master template fabricated on a silicon wafer. The templates were produced using negative photoresist and the standard photolithography process as seen in figure or using the etching process post lithography. Both lithography and etching were trialled. The lithography method was favoured as optimisation of film thickness requires a single wafer that can be cleaned after each set of photolithography.

8.1.4 Metal Lift-Off Photoresist

The metal contact layer is produced by a metal lift-off process. Whereby a photoresist layer is patterned on the surface followed deposition of a metal layer. When the photoresist layer is later removed any metal deposited on the photoresist will be removed and metal deposited directly on the substrate will remain. Photoresists achieve clean lift-off with with the use of "over hang" geometry. Metal deposited using a sputtering based method is deposited in a directional manner and therefore does not form a single conformal sheet over the over hang of the photoresist enabling a clean line of metal pattern on the surface see Figure 8.2 (a) Bi layer photoresist LOR bottom layer microposit S1813 top layer over hang produced. (b) Metal deposition step from sputtering source majority of metal deposited perpendicular from sputtering source above. (c) Photoresist removal resulting in metal lift-off.

The bi layer photoresist system uses a non photoactive resist as the base layer LOR 5A (DOW) with a positive photoresist microposit S1813 as the photoactive top layer. The microposit layer is exposed to UV and becomes soluable in chemical developer AZ 726. After the exposed material is removed the LOR resist is also

(a)



(b)

(c)

Figure 8.2: Bi-Layer lift-off process.

removed by the AZ 726 developer, longer time spent in developer the larger the over hang is produced.

8.1.5 Potassium Hydroxide Etch

Silicon dioxide is often used as an etch mask when using wet etching techniques. Potassium hydroxide (KOH) etching can be used to etch silicon as seen in equation 8.1.1. To etch specific regions of a silicon substrate an etch mask must be produced.

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^2 - + 2H_2 \tag{8.1.1}$$

Two standard materials can be used as an etch mask for wet etching. The first is SiO_2, where a film is deposited using PE-CVD on both sides of the silicon substrate. A Photoresist mask is then patterned onto the SiO_2 surface. The resist protects the oxide during HF exposure. The patterned substrate is then immersed in a HF oxide etch. The SiO_2 is etched in the exposed regions but protected under the photoresist. The photoresist is then removed. The silicon substrate is immersed in a KOH solution and placed in a hot bath 70 °. The etch rate is dependent on KOH concentration and hot bath temperature. The SiO_2 etches at a much slower rate compared to the exposed silicon areas. Once the silicon is etched sufficiently, the remaining SiO_2 on the surface can be removed by HF etch.

Alternatively if an etch stop layer is required, a Si_3N_4 film can be deposited using PE-CVD. The same surface patterning process can be applied, however the KOH etch rate for Si_3N_4 is significantly slower than SiO_2.

If the crystal orientation of the silicon is 100, the KOH etched anisotropically, with an angle of 54.74° from the plane, producing a cavity with a trapezoid cross section (Figure 8.3).

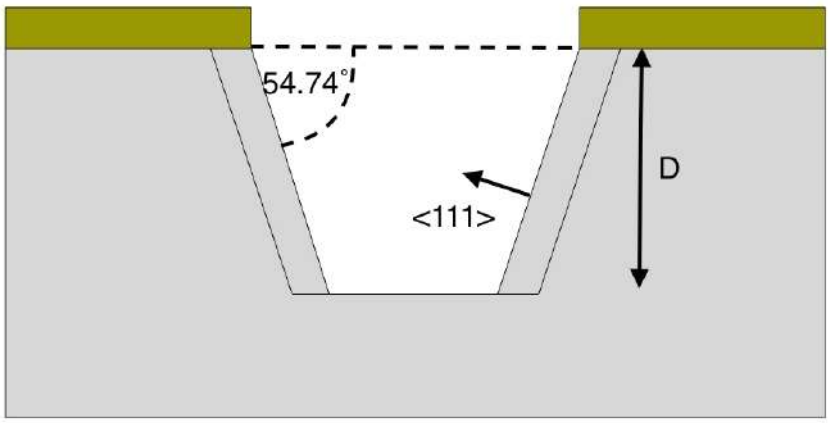


Figure 8.3: KOH produces an anisotropic etch on silicon, with a <100> miller indices plane at the base and <111> on the cavity walls.

8.1.6 Buffered Oxide Etch

Hydrofluoric etching has already been covered in the sample preparation section as a method of removing oxides. However, when etching thin layers of SiO_2 the reaction of concentrated HF (60 %) is fast at 2μm/min. This makes it difficult to control the thickness of oxide being removed during a single etch. In this case a buffered HF solution or buffered oxide etch (BOE) is used. The buffering agent, often ammonium fluoride (NH_4F), reduces the etch rate of the HF to more manageable levels 100 nm/min.

BOE is also used as a glass etchant, often combined with 20% HCl to produce smoother etched features.

8.1.7 Scanning Electron Microscopy

Scanning electron microscopy (SEM), is one type of electron microscopy that produces an image using a focused beam of high-energy electrons as it scans across the surface of the sample. The electrons interact with the surface of the sample producing a variety of signals that are received by a detector or multiple detectors.

The signals are processed by the SEM's computer to produce an image, from the topography can be determined as well as crystal structure and orientation and even the composition of the sample. Samples are imaged under vacuum to prevent the electron beam from interacting with molecules in the surrounding environment. The image is created by the detection of primary backscatter (electrons are backscattered due to elastic collisions with atoms in the sample they lose little energy during a collision), and secondary electrons (electrons from the primary beam ionise the atoms in the sample, secondary electrons are emitted from the ionised atoms). The energy signatures of these electrons depend on the surface topography of the sample.

8.1.8 Energy-dispersive X-ray Spectroscopy

Energy-dispersive X-ray Spectroscopy (EDX) is a technique for elementary analysis to determine the chemical composition of the sample. The EDX penetrates the sample, higher accelerating voltages can penetrate the sample further. EDX capability is achieved using Oxford instruments EDX detector in combination with the SEM. The working principle involves using the SEM to identify the region that you wish to analyse. The EDX uses the SEM's focused electron beam to excite the sample in this region. Ground state or unexcited electrons can be hit out of its shell by an electron of the same energy from the electron beam. This leaves an electron-hole in the energy shell. An electron from a higher energy shell can drop down to fill this electron-hole, emitting excess energy in the form of photons. It is the emitted photons that are detected by the EDX.

The electron will not return directly to its original energy shell it will release photons of different wavelengths as it moves down the energy shells to its stable state. This is called the X-ray emission spectrum. The EDX identifies the different elementary components of a sample; this is due to each element having a unique X-ray emission spectrum.

8.1.9 Atomic Force Microscopy

In basic principles, it is a mechanical device able to measure very small changes down to atomic and molecule level. The pointed tip is brought into contact with the material that needs to be characterised. The force between the tip and the sample is converted into a bending, or deflection, of the cantilever. This deflection is measured using a laser that is reflected off the back of the cantilever onto a detector. This is then converted digitally to a force map and height and roughness data.

8.1.10 Raman Spectroscopy

Cosmic Ray Removal

The process of cosmic ray removal if performed within the Wire software package (Figure 8.4).

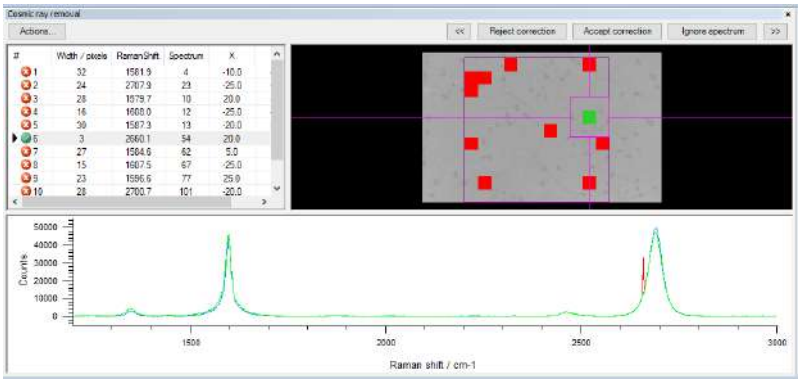


Figure 8.4: Cosmic ray removal process

8.2 Graphene Sensor Fabrication & Optimisation

8.2.1 Skewness & Kurtosis

Definitions of skewness and kurtosis come from IBM SPSS statistics (SPSS Inc).

Skewness

"Skewness measures the degree and direction of asymmetry. A symmetric distribution such as a normal distribution has a skewness of 0, and a distribution that is skewed to the left, e.g. when the mean is less than the median, has a negative skewness."

Kurtosis

"Kurtosis is a measure of tail extremity reflecting either the presence of outliers in a distribution or a distribution's propensity for producing outliers"

8.2.2 Graphene Sensor: Design & Fabrication

The drawing action of solvents to determine Dip Chip length were performed on SiO_2 coated Si hand diced to the correct width. When one of the chip is submerged (dipped) into a container of water. The chip was marked 5 mm from one end to represent the position of the graphene channels. The chip was submerged into the water the graphene channel mark approximately 1 mm below the meniscus. A period of 10 minutes was given and the travel distance of the solvent up the chip was marked and measured. The water travel was measured as 2 mm in water, the experiment was repeated for ethanol the total travel was measured as 5 mm.

8.2.3 Inter Probe Station Comparison

In order to check the inter machine variability as well as the probe to SD connector variability. A single device was measured thirty times on both probe stations; EverBeing and Inseto probe stations, using grapheme channels with dimensions 400 x 100 /*mu*m and using the 0.2 s and 0.05 s step time setting on Keithley 2636 B measurement unit (Table 8.1).

The difference in average (mean) resistance between the two probe stations is 24.78 Ohms a difference of 0.53 %. This is a statistical significant difference P = <

0.0001, Unpaired t test with Welch's correction. This difference could be accounted for by the metallurgy of the contact probes or simply the length, brand or type of cables used to connect the probe tips to the Keithley units. At this stage the resistance of the individual connection wires do not need to be ascertained. Using a single IV probe station for each experimental set will remove the inter probe station variability.

The variance of the two probe stations was also compared. The relative standard deviation of the Inseto probe station was more than double that of the EverBeing station. The difference in variance between the two probe stations was statistically significant P = < 0.0001, F - test of equality of variance. So further experiments would be based primarily on the EverBeing station to reduce machine variance within the results.

	Inseto Station	Everbeing Station
Mean (Ohms)	4718.28	4693.41
Median (Ohms)	4718.84	4693.45
Range (Ohms)	15.65	7.34
Standard Deviation	5.05	2.00
Relative SD	0.11 %	0.04 %

Table 8.1: Comparison of resistance measurements made on 1 graphene channel, on both Inseto and EverBeing IV probe station.

8.2.4 IV Data Analyses

The standard method for analysing an IV linear sweep measurement to obtain resistance from a csv file is by opening taking 1 over the slope of the line graph. Providing the line graph has a linear fit, (the contacts were ohmic). This uses the Resistance equation $R = \frac{V}{I}$, where R = Resistance (Ohms), V = Voltage (Volts) and I = Current (Amps). The IV sweep used has 101 data points and the time to calculate this for a single csv file is negligible (approximately 1 minute). But when

measuring multiple repeats per graphene channel (e.g. 3) and 96 graphene channels per wafer (Dip Chip Origin design). This totals 288 csv to process, this could effectively take almost 4-5 hours of monotonous tasks. Writing a Python Script to improve data analyses speed for single or triple graphene channel reading enabled all 288 csv files to be processed in seconds. The Python code can be seen in Appendix.

8.3 Graphene Sensor Real-Time Measurements

8.3.1 Normalisation of Resistance Data

Normalising to the data mean and normalising to the baseline device resistance (Z-score) was performed using the formula,

$$z = \frac{x - \overline{x}}{S} \tag{8.3.2}$$

Where $\overline{x}$ is the mean of the sample and S is the standard deviation of the sample.

8.3.2 Extracting Carrier Mobility From Dirac Point Measurements

The direct transconductance method (DTM) uses the gate voltage dependent transconductance (g_m) of the graphene measured during Dirac point measurement using the formula,

$$\mu_{DTM} = \frac{g_m}{LWV_{ds}C_g} \tag{8.3.3}$$

Where $g_m = \mathcal{D}I_{ds}/\mathcal{D}V_g$ and the C_g is the capacitance of the substrate dielectric.

8.3.3 Acetone Submersion & Drying IV Measurement

Full IV measurement of submersion and drying experiment performed on PT-SPI Chip, data normalised to dry starting resistance, After 15 minutes graphene submerged in acetone. At 8 hours graphene removed from acetone and dried with compressed air (Figure 8.5).

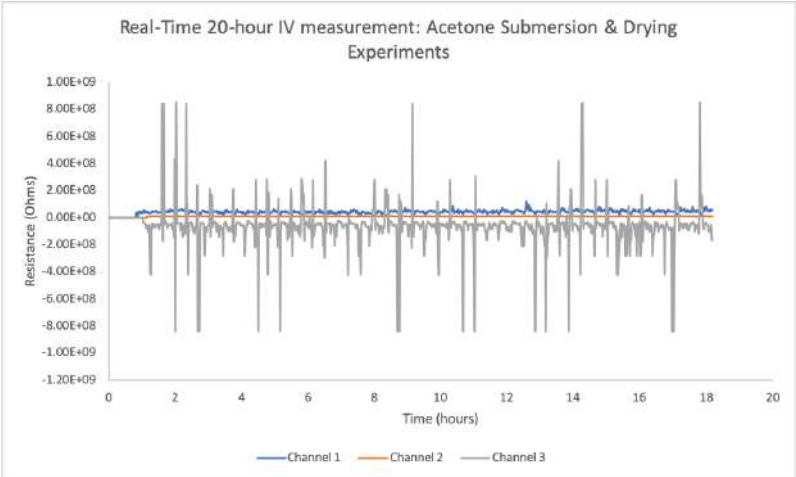


Figure 8.5: 20 hour real-time experiment, acetone submersion (PT-SPI Chip).