Smooth DC-Link Y-source Inverters: Suppression of Shoot-through Current and Avoiding DC Magnetism

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***Abstract*— The Y-source impedance network is truly referred to as the origin of the magnetically coupled impedance source (MCIS) inverters. The key characteristics, including high boost capability and design flexibility, are associated with the coupled inductor turn ratio. However, the magnetic element brings some practical challenges, such as voltage spikes, high shoot-through (ST) current, and bulky coupled inductors. This paper proposes two new Y-source inverters with clamped DC-link voltage. Due to the high boost ability, they are suitable for single-stage high gain inversions. Additionally, the significant reduction in the amplitude of the ST current leads to a reduction of the total power loss and capacity of the reactive component. Another attractive characteristic is that the Y-shaped coupled inductor's stored energy is no longer affected by the power rating of the converter, as a result of the zero dc magnetizing current. All these contribute to the high efficiency and power density of the proposed converters. The design guidelines of the components are presented and a thorough comparison with the state of the art is carried out. The achievements are then confirmed through extensive tests on a 500W laboratory setup.**

***Index Terms*— Magnetically coupled impedance source network, magnetizing current, ST current, voltage spike, Y-source inverter.**

I. Introduction

Z-SOURCE inverter [1] has been introduced to solve the problems of the traditional voltage source inverter. In this converter, the semiconductors are no longer vulnerable to the unwanted simultaneous conduction of the switches in the same leg (ST state). The x-shaped network consisting of the two pairs of the inductors and capacitors is placed between the input voltage source and the H-bridge and hence not only the ST mode is allowed but also the dc-link voltage can be boosted to the desired value by advantageous employment of this mode. Therefore, the buck-boost inversion is done in a highly reliable single-stage operation with no need for dead-time insertion. Due to these advantages, many structures and modulation strategies have been proposed to improve the characteristics of the Z-source inverter [2], [3]. Among them, some works such as [4]–[8] are devoted to enhancing the boost ratio. Because, where a high voltage gain is required, the Z-source inverter operates with a long ST time which translates to a low modulation index of the inverter circuit. Therefore, the output waveforms deteriorate and the H-bridge semiconductors experience high voltage stresses in the wake of the high dc-link voltage requirement. The MCIS inverters [4] have been introduced to somehow solve this issue while the Y-source inverter (YSI) [9] is generally known as their origin. They offer one additional control parameter, derived from the turn ratio of the coupled inductor and can increase the dc voltage by the boost factor, expressed as (1), where V_{PN} and V_{in} are the dc-link and input voltages, respectively. Also, D denotes the ST duty cycle and δ is a function of the turn ratio. This way, by adjusting the δ factor, the required dc-link voltage can be obtained with a lower ST time duration. Furthermore, along with D, the δ factor determines the voltage and current stresses of the components. Thus, it can be utilized as an extra degree of design freedom.

$$B = \frac{V_{PN}}{V_{in}} = \frac{1}{1-\delta D} \tag{1}$$

However, besides these advantages, the coupled inductor utilization imposes some drawbacks to the circuit. First, the unachievable unity coupling factor in practice causes voltage spikes across the dc-link of the inverter semiconductors when it switches from ST to non-shoot-through (NST) state. Therefore, many methods have been offered to actively or passively tackle this problem [10]-[26]. Some of them just aim to propose a solution for this problem while the others offer some other benefits too. To reduce the leakage inductance and the equivalent series resistance (ESR) of the coupled inductor of the Y-shaped coupled inductor, the Δ-source impedance network is recently proposed in [18]. However, a major drawback is that the turn number of the second winding of the coupled inductor, N_2, is determined by the Δ-shaped coupled inductor voltage loop. It means that N_2 cannot be considered as a flexible design parameter contributing to the gain formula. Furthermore, the need for an additional absorbing circuit to clamp the dc-link voltage spikes is still inevitable. However, when the snubber circuit such as resistor-capacitor-diode [27] is utilized the required snubber capacitor is less

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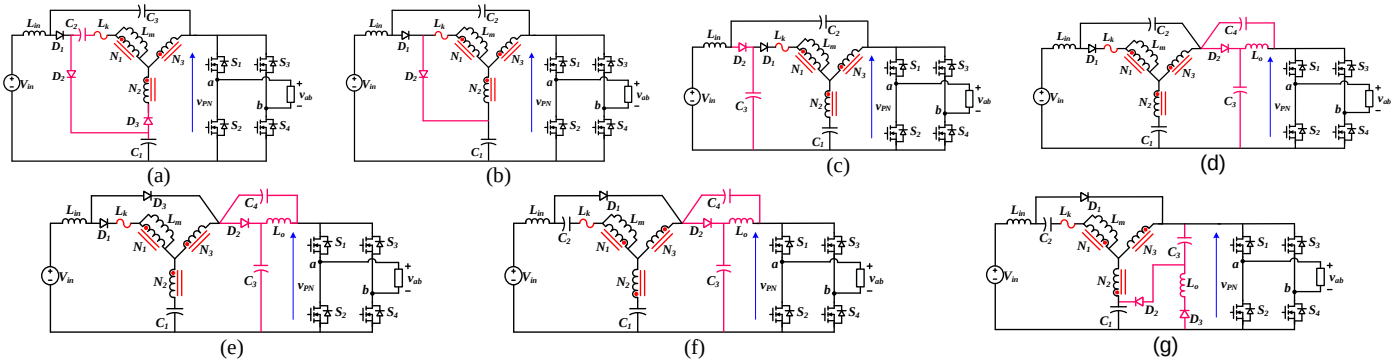


Fig. 1. The circuit diagram of the clamped dc-link voltage YSIs: (a) voltage-double YSI [19], (b) clamped qYSI [20], [21], (c) LH-YSI [22], (d) HS-YSI [23], (e) DA-YSI [24], (f) O-YSI [25], and (g) LCD-qYSI [26].

than the Y-source network. As another approach, to avoid the voltage spike across the dc-link of YSI, and at the same time, improve its voltage gain, and input current, the Y-shaped coupled inductor is combined with a voltage double cell and a low pass LC filter is added to the input too [19]. It is depicted in Fig. 1(a). When the converter switches from ST to NST state, due to the conduction of diodes D_1, and D_2 the dc-link voltage is clamped by the capacitors C_1, and C_3. However, because of the simultaneous conduction of all diodes at the beginning of NST mode, a huge voltage drop, $(\delta-2)V_{PN}$ appears across the leakage inductor. Therefore, a high current circulates in the circuit. A similar approach is proposed in [20], [21] with one less diode and capacitor and a lower voltage gain, as illustrated in Fig. 1(b). Nevertheless, in this approach, the dc-link voltage is still higher when the snubber diode conducts. In other words, the peak of the voltage spike is limited by the clamp circuit, but it is not fully mitigated and still deteriorates the voltage stresses of semiconductors.

The low-spike high-efficiency YSI (LH-YSI) [22] is one of the successful converters, which is derived by replacing one of the discrete inductors of the quasi Z-source inverter (qZSI) [28] with the Y-source impedance network as illustrated in Fig. 1(c). The leakage inductor energy is recovered through the capacitor C_3 and diode D_2. Besides, in addition to the continuity of the input current, the high blocking voltage of the diode D_1, which is a common problem among all MCIS inverters, reduces from $(\delta-1)BV_{in}$ to $(\delta-2)BV_{in}$ in comparison to YSI. As a step forward, the high step-up YSI (HS-YSI) [23] and the diode-assisted YSI (DA-YSI) [24] are proposed as the cascade connection of the YSI with an input current smoothing circuit and qZSI, respectively [28]. Their circuit configurations are shown in Figs. 1(d) and (e), respectively. Along with the aforesaid achievements, they improve the voltage gain characteristics of the YSI. However, the volume of the coupled inductor is the other main concern of these converters, as the minimum value of the dc magnetizing current equals the input current and it is a serious problem at high voltage gain applications (high input current). As a recent work, the optimized YSI (O-YSI) is proposed to tackle this problem [25]. It is derived by repositioning D_1 and C_2 of the HS-YSI and reconfiguring its coupled inductors windings as illustrated in Fig. 1(f). The series connection of C_1 and C_2 with N_1 and N_2 windings of the Y-shaped coupled inductor along with the common node of its windings results in a zero average magnetizing current. Therefore, it offers a higher power density than the other smooth dc-link voltage inverters. The same Y-shaped coupled inductor configuration with zero magnetizing currents is also employed by the authors in [26] while it is offered to using of the inductor- capacitor-diode (LCD) snubber instead of the cascade technique utilization. This circuit is illustrated in Fig. 1(g). As can be seen, ideally, the LCD snubber recovers the stored energy of the leakage inductor to the circuit without losses. However, the component design of the LCD snubber is a serious challenge in this method, due to the dependency of their stresses on the leakage inductance value. Moreover, both of the latest approaches still suffer from a large coupled inductor windings current resulting in high power losses and volume of the windings.

The second common problem of the MCIS inverters (the spiky circuits and even the clamped ones) originates from their ST current. When one investigates the ST current of all these converters, it will be revealed that the input current multiplied by δ flows through the circuit during the ST mode. In other words, reducing the required ST duty cycle will deteriorate the ST current waveform proportionately. It results in high power losses and high semiconductors ratings.

Also, some MCIS inverters have been developed based on quasi switched boost inverter (qSBI) [29] to simultaneously take advantage of both the coupled inductor and the switch. The early solutions [30], [31] integrate one more winding to the input inductor magnetic core of qSBI. While they inherit almost all advantages of the MCSI inverter, the switch

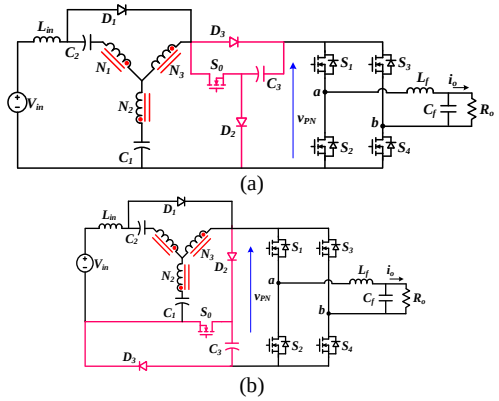


Fig.2. Proposed converters (a) type I and (b) type II.

experiences high voltage spikes, the input current deteriorates, and the ST current is still too high. As a step forward and to have a continuous input current, the authors in [32] have offered to replace the input inductor of a-source impedance network [33] with qSBI. Furthermore, in [34] the cascade connection of qSBI and qZSI has been proposed while the discrete inductor is replaced with a switched coupled inductor cell. Although in this way the switch of these impedance networks is clamped, the dc-link spikes can be regarded as the main disadvantage of these converters. Besides, all of these switched-based converters require a bulky coupled inductor as the magnetizing current is always larger than the input current.

To solve the aforementioned issues, this paper offers two novel MCIS inverters, shown in Figs. 2(a) and (b). They can effectively suppress the dc-link voltage spike. The high efficiency and power density of these converters originate from the low ST current in terms of the magnitude and its duration. The coupled inductor volume is significantly reduced due to the low windings' current as well as the zero average magnetizing current. In addition, the lowST current permits the lower ratings of semiconductors . In the following, their operation principles are explained first to show how they can effectively recover the leakage inductor energy and smooth the dc-link voltage. The currents and voltages of all components are derived in all modes of operation to facilitate the proper design of circuit components. In the next step, the successful competitors are compared with the proposed inverters from various aspects. Then, all of their features are verified experimentally via tests on a 500W laboratory setup.

I. CIRCUIT ANALYSIS

As shown in Figs. 2(a) and (b), one discrete inductor L_{in}, three capacitors (C_1~C_3), three diodes (D_1~D_3), five switches (S_0~S_4), one Y-shaped coupled inductor with (N_1:N_2:N_3) as its turn ratio, and the output low pass filter, comprising of L_f, and C_f are the same elements of both types of the proposed inverters that are connected in different configurations. In type I, the negative terminal of the input voltage source is directly connected to the source of the H-bridge MOSFETs S_2 and S_4 while it is connected to the source of S_0 in type II. However, both of these converters are identical in all modes of operations. Therefore, in the following, just type I is analyzed.

A. Operation principle

The same as all impedance source networks, the proposed inverter operation consists of two distinct modes; ST and NST. Its equivalent circuits are presented in Fig. 3. For the sake of simplicity, the H-bridge and the load can be replaced with a switch that conducts in ST and blocks in NST in parallel with a current source. It draws the constant current I_o from the impedance network terminals that equals the average value of the output current within one switching period, T_s. The three windings coupled inductor is modeled with a magnetizing L_m, and leakage L_K inductors on the first winding side. All inductances and capacitances are considered sufficiently large that the current through the inductors and voltage across the capacitors can be assumed constant during a switching period. However, due to the low value of the leakage inductance, its current suddenly changes. With these

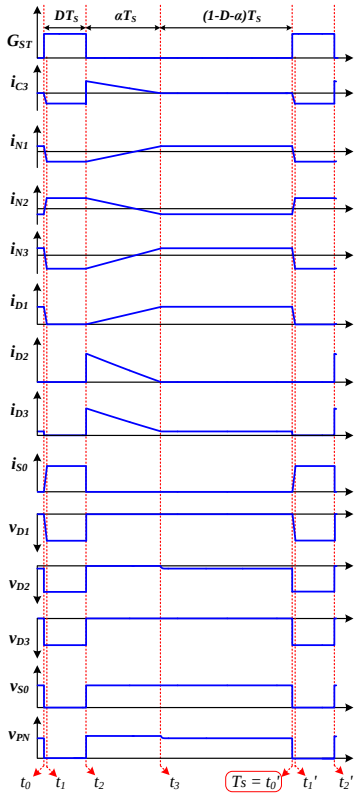


Fig. 4. Key waveforms of the proposed inverter.

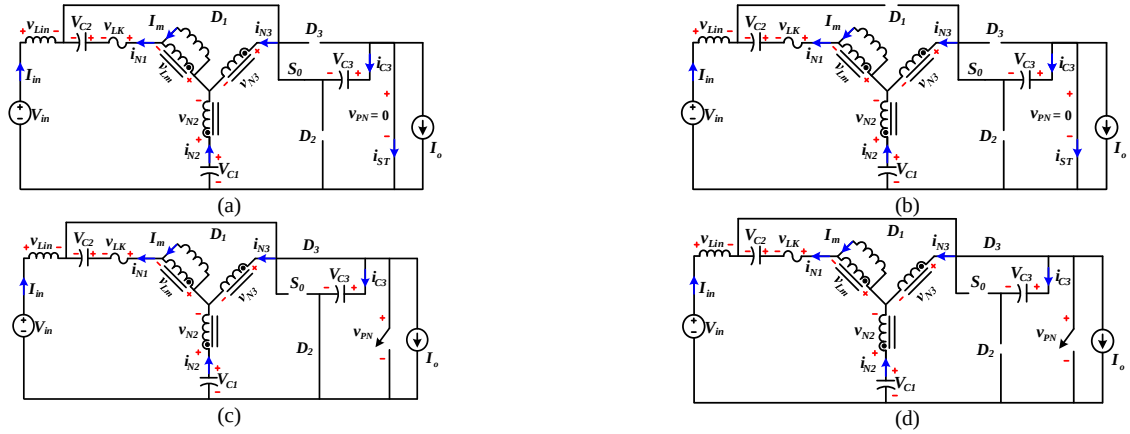


Fig. 3. Equivalent circuits of the proposed inverter type I (a) ST state [t_0, t_1], (b) ST state [t_1, t_2], (c) NST state [t_2, t_3], and (d) NST state [t_3, T_s].

considerations, the key waveforms of the proposed inverter are depicted in Fig. 4. Both ST and NST states are divided into two intervals as described in the following.

1) ST state

a) Interval I [t_0, t_1]

When all switches are ON, the converter enters the ST state and the dc-link voltage v_{PN} drops to zero. Both D_2 and D_3 are reverse biased by C_3 and block. Also, D_1 conducts during this state until the energy stored in the leakage inductor decays to zero. The equivalent circuit of this state is demonstrated in Fig. 3(a). Because of the low value of the leakage inductance, its current reduction occurs at a rapid rate. Therefore, the time interval of this state is very short and, except for the leakage inductor, the energy of all reactive elements can be supposed constant during this state.

b) Interval II [t_1, t_2]

The equivalent circuit of this state is shown in Fig. 3(b). As can be seen, all diodes block while the switches conduct. All capacitors and the input voltage source charge L_m, and L_{in} as depicted in Fig. 4. It is safe to suppose that the time duration of this interval is the ST time duration, i.e. DT_s.

2) NST state

a) Interval III [t_2, t_3]

In this state, S_0 is turned OFF and the H-bridge operates at zero or active state while all diodes are forward-biased. As shown in Fig. 3 (c), the dc-link voltage is clamped at the voltage value of C_3 via the path provided by D_2. The voltages across windings of the coupled inductor are also clamped by the capacitors. Therefore, as depicted in Fig. 4, it avoids any abrupt change in the coupled inductor windings current and a resultant voltage spike across the dc-link voltage when the inverter enters NST state.

b) Interval IV [t_3, T_s]

The current of D_2 reaches zero at t_3 while the state of the other semiconductors remains the same as the previous interval. Thus, the voltages across the coupled inductor windings are still clamped by C_1 and C_2. Besides, as illustrated in Fig. 4, a small voltage drop emerges at dc-link voltage during this interval that is associated with the blocking voltage of D_2. However, as will be revealed, it does not considerably affect the overall performance and mathematical analysis of the proposed inverter circuit.

B. Current analysis

As previously mentioned, the dwell time of the first interval is negligible and the energy of L_{in}, L_m, and the capacitors remains unchanged during this short time. Thus, starting with Fig. 3(b), when all active switches conduct and the diodes are reverse-biased, the capacitors currents can be expressed as

$$i_{C1}^{II} = i_{N2}^{II} \tag{2}$$

$$i_{C2}^{II} = -I_{in} \tag{3}$$

$$i_{C3}^{II} = -I_{in} - i_{N2}^{II}. \tag{4}$$

Also, based on Ampere's law, the current of the coupled inductor windings should meet (5).

$$N_1 i_{N1} + N_2 i_{N2} + N_3 i_{N3} = 0 \tag{5}$$

Considering (2) to (5), the current through C_1 and C_3 can be obtained from the input current I_{in}, and the turn ratio of the coupled inductor, as

$$i_{C1}^{II} = -KI_{in} \tag{6}$$

$$i_{C3}^{II} = -(K+1)I_{in} \tag{7}$$

where

$$K = \frac{N_1 + N_3}{N_2 - N_3}. \tag{8}$$

When the converter switches from ST to NST state, all diodes start conducting and S_0 is turned OFF. As shown in Fig. 4, the currents of the capacitors change linearly in this interval and their equations can be easily approximated from just the two points. Due to the clamped coupled inductor windings, their currents change continuously. Therefore, one can conclude that the windings currents at the begging of the NST mode $i_{Nx}(t_2^+)$ equal the one at the end of the ST state $i_{Nx}(t_2^-)$ where x = 1, 2, 3. With this consideration, the first point of the linear equation of the capacitor current during the third time interval can be expressed as (9) to (11).

$$i_{C1}(t_2^+) = -KI_{in} \tag{9}$$

$$i_{C2}(t_2^+) = -I_{in} \tag{10}$$

$$i_{C3}(t_2^+) = (K+1)I_{in} - I_o \tag{11}$$

At the moment that the current of D_2 reaches zero, i.e. t_3, the converter enters the second mode of the NST state. As depicted in Fig. 4, the capacitors' currents are constant during this time interval. By applying KCL in the equivalent circuit (Fig. 3 (d)) and considering (5), the capacitors currents can be obtained as (12) to (14). These are the final values of the previous interval, too.

$$i_{C1}^{IV} = I_{in} - I_o \tag{12}$$

$$i_{C2}^{IV} = \frac{I_{in} - I_o}{K} \tag{13}$$

$$i_{C3}^{IV} = 0 \tag{14}$$

According to the current balance law of the capacitor, its average value in the steady-state is equal to zero, then

$$\int_{t_1}^{t_2} i_{cx}\,dt + \int_{t_2}^{t_3} i_{cx}\,dt + \int_{t_3}^{T_s} i_{cx}\,dt = \int_{0}^{DT_s} i_{cx}\,dt + \int_{DT_s}^{(\alpha+D)T_s} i_{cx}\,dt + \int_{(\alpha+D)T_s}^{T_s} i_{cx}\,dt = 0 \tag{15}$$

where x = 1, 2, 3 represents the number of the capacitor. Furthermore, $\alpha = (t_3 - t_2)/T_s$ is the proportionality factor. As previously discussed, the time interval of the first mode of ST state is almost negligible. Thus, one can assume that $DT_s \approx (t_2 - t_1)$.

Assuming (9) to (14) as the two points of the linear equation of the capacitors currents during the first mode of NST state, their linear waveforms can be easily calculated. Thus, by substituting capacitors currents within the three-time intervals

in the time integral equation of (15), one can conclude

$$\alpha = \frac{2D(1-D)}{D + K/(K+1)} \tag{16}$$

$$I_o = \frac{1-2(K+1)D}{1-D} I_{in}. \tag{17}$$

Therefore, the current through all elements can be determined.

C. Voltage Analysis

In this subsection, the voltages of the inductors are calculated during each time interval. Then, by applying the volt-second balance to them, the voltage across the capacitors and the boost factor of the proposed converter are calculated. First, by writing KVL in the equivalent circuit of ST mode (Fig. 3 (b)), the voltage equations can be expressed as

$$v_{Lm}^{ST} = \frac{N_1}{N_2 - N_3}(V_{C1} + V_{C3}) \tag{18}$$

$$v_{Lin}^{ST} = V_{in} + KV_{C1} + V_{C2} + (K+1)V_{C3} \tag{19}$$

After that, the converter enters NST mode, when all diodes conduct, S_0 is OFF, and the H-bridge works in zero or active state. By writing KVL in Fig. 3 (c), the voltage across the inductors during this mode can be written as (20) to (22), where v_{LK}^{III} denotes the voltage across the leakage inductor.

$$v_{Lm}^{III} = -\frac{N_1}{N_2 - N_3}(V_{C3} - V_{C1}) \tag{20}$$

$$v_{Lin}^{III} = V_{in} - V_{C3} \tag{21}$$

$$v_{LK}^{III} = K(V_{C3} - V_{C1}) - V_{C2} \tag{22}$$

At t_3, the current of D_2 reaches zero and the converter enters the second mode of the NST state. The voltage expressions during this mode are written as (23) to (25). As can be seen, in comparison to the equations of the previous interval, just the blocking voltage of D_2 appears in this mode. Besides, due to the clamped circuit consisting of C_2, and the series connection of L_k and L_m, the leakage inductor's voltage can be obtained as (25).

$$v_{Lm}^{IV} = -\frac{N_1}{N_2 - N_3}(V_{C3} - V_{C1} + v_{D2}^{IV}) \tag{23}$$

$$v_{Lin}^{IV} = V_{in} - V_{C3} - v_{D2}^{IV} \tag{24}$$

$$\begin{aligned} v_{LK}^{IV} &= \frac{-L_K}{L_K + (1 + N_3/N_1)L_m} V_{C2} \\ &= K(V_{C3} - V_{C1} + v_{D2}^{IV}) - V_{C2} \end{aligned} \tag{25}$$

Since $L_K << L_m$, it can be assumed that $v_{LK}^{IV} \approx 0$. Thus, from (25),

$$v_{D2}^{IV} = -(V_{C3} - V_{C1}) + V_{C2}/K. \tag{26}$$

Comparing (26) and (22) reveals that $v_{LK}^{III} = -Kv_{D2}^{IV}$. Hence, to obtain the blocking voltage of D_2 during the second mode of the NST state, the voltage across the leakage inductor during the first mode of NST should be calculated. To do so, it can be easily estimated according to the current-voltage relation of the leakage inductor, as

$$i_{N1}(t_3) = i_{N1}(t_2) + \frac{1}{L_K}\int_{t_2}^{t_3} v_{LK}\, dt. \tag{27}$$

Due to the series connection of C_2 and L_K, $i_{N1} = i_{C2}$. Thus, from (3), (13), and (27), the voltage across D_2 during the last mode of the NST state can be obtained as

$$v_{D2}^{IV} = \frac{K+1}{2}\left[\frac{K/(K+1)D + 1}{1-D}\right]^2 \frac{L_K D}{T_s} I_{in} \tag{28}$$

Again, due to a very small L_K, the value of V_{D2}^{IV} can be safely assumed negligible (a few volts). Thus, for the sake of simplicity, it is ignored during [t_3, T_s] in the following analysis. Hence, the voltages across the capacitors and the boost factor of the proposed converter can be obtained by applying the volt-second balance law to the input and magnetizing inductors that results in

$$\begin{cases} V_{C1} = \dfrac{(1-2D)}{1-2(K+1)D} V_{in} \\ V_{C2} = \dfrac{2KD}{1-2(K+1)D} V_{in} \\ V_{C3} = \dfrac{1}{1-2(K+1)D} V_{in} \end{cases} \tag{29}$$

$$B = \frac{1}{1-2(K+1)D}. \tag{30}$$

Assuming the simple boost modulation [29], the maximum achievable modulation index, M, is $1-D$. Consequently, the voltage gain, G, of the proposed inverter is

$$G = MB = \frac{V_o^{\max}}{V_{in}} = \frac{1-D}{1-2(K+1)D} = \frac{1-D}{1-\delta D} \tag{31}$$

where V_o^{max} represents the maximum ac voltage across the load.

II. Elements Design and Comparison

Generally, the second harmonic power (2ω) is introduced by all single-phase inverters. In the impedance source inverters, it causes to 2ω ripple on the inductor current, and capacitor voltage of the network, and hence the dc-link voltage of the inverter. Many approaches have been offered to reduce or avoid penetrating the 2ω ripple into the impedance networks [35]–[37]. In this section, it is assumed that this undesired power is effectively suppressed by one of these methods. Therefore, the design of the components is performed by assuming just the switching frequency ripple.

A. Elements design

The inductance value is determined from the voltage across the inductor during the charge or discharge mode and its dwell time. Based on the circuit analysis, both L_m, and L_{in} are charged during the ST mode. Thus, from (18), and (19), one can obtain

TABLE I
COMPARISON AMONG PROPOSED INVERTERS AND THE OTHER SUCCESSFUL COMPETITORS

Conveter	LH-YSI [22]	HS-YSI [23]	DA-YSI [24]	O-YSI [25]	LCD-qYSI [26]	Proposed (type I & II)
B	$1/(1-(1+K)D)$	$1/(1-(2+K)D)$	$1/(1-(2+K)D+KD^2)$	$1/(1-(2+K)D)$	$1/(1-(1+K)D)$	$1/(1-2(1+K)D)$
V_{C1} / V_{in}	$(1-D)B$	$(1-2D)B$	$(1-2D)B$	$(1-2D)B$	$(1-D)B$	$(1-2D)B$
V_{C2} / V_{in}	$(\delta-1)DB$	$(\delta-2)DB$	NA	$(\delta-2)DB$	$(\delta-1)DB$	$(\delta-2)DB$
V_{C3} / V_{in}	$(1-(\delta-1)D)B$	$(1-D)B$	$(1-D)B$	$(1-D)B$	V_{C3}^{LCD}	B
V_{C4} / V_{in}	NA	DB	DB	DB	NA	NA
I_m / I_{in}	$1+N_3/N_1$	$1+N_3/N_1$	$(1+N_3/N_1)(1-D)$	0	0	0
I_{Lo} / I_{in}	NA	1	1	1	$V_{C3}^{LCD}\,DT_s/L_o$	NA
V_{D1} / V_{in}	$(\delta-2)B$	$(\delta-2)B$	$(\delta-2)B$	$(\delta-2)B$	$(\delta-1)B$	$(\delta-2)B$
V_{D2} / V_{in}	B	B	B	B	$(1-D)B+V_{C3}^{LCD}$	B
V_{D3} / V_{in}	NA	NA	$(\delta-2)DB$	NA	$V_{PN}-V_{C3}^{LCD}$	B
I_{D1} / I_{in}	$(\delta-1)/(1-D)(\delta-2)$	$(\delta-1)/(1-D)(\delta-2)$	1	$(\delta-1)/(1-D)(\delta-2)$	$1/(1-D)$	$((1+D)(0.5\delta-1)+D)/(1-D)(0.5\delta-1)$
I_{D2} / I_{in}	$(\delta-1)/(1-D)$	$(\delta-1)/(1-D)$	$1/(1-D)$	$(\delta-1)/(1-D)$	$(\delta-1)/(1-D)+I_{Lo}/I_{in}$	$((1+D)\,0.5\delta-1)/(1-D)$
I_{D3} / I_{in}	NA	NA	1	NA	I_{Lo}/I_{in}	$0.5\,\delta$
V_{S0} / V_{in}	NA	NA	NA	NA	NA	B
I_{S0} / I_{in}	NA	NA	NA	NA	NA	$0.5\,\delta$
I_{ST} / I_{in}	δ	δ	δ	δ	δ	$0.5\,\delta$

$V_{C3}^{LCD} = 0.5DB + 0.5\sqrt{[(DB)^2 + 4L_kL_oI_{N1}^2/(DT_sV_{in})^2]}$

$$\begin{cases} L_m = \dfrac{N_1}{N_2-N_3}\dfrac{2(1-D)D}{1-2(K+1)D}\times\dfrac{V_{in}T_s}{2\Delta i_m} \\ L_{in} = \dfrac{2(K+1)(1-D)D}{1-2(K+1)D}\times\dfrac{V_{in}T_s}{2\Delta i_{in}} \end{cases} \tag{32}$$

where Δi_m and Δi_{in} are the difference between the maximum and minimum values of the magnetizing and input inductors current during one switching period, respectively.

To have an acceptable voltage ripple across the capacitors, their value should be calculated based on their charge or discharge current and its time duration. Referring to Fig. 4, C_3 is just discharged during the ST mode while the other capacitors charging operation is performed in both ST and NST modes. However, based on the current analysis subsection, the linear current via C_1 and C_2 can be easily estimated during the first mode of the NST state and their charge time can be readily estimated from their zero-crossing point. Accordingly, the capacitance values are calculated and expressed as (33) in which P_o is the nominal power of the converter, and ΔV_{C1}, ΔV_{C2}, and ΔV_{C3} are the capacitors voltage ripple.

$$\begin{cases} C_1 = \dfrac{(2K+1)[K-(K+1)D]D}{[(K+1)D+K]}\times\dfrac{P_oT_s}{2V_{in}\Delta V_{C1}} \\ C_2 = \dfrac{(2K+1)[K-(K+1)D]}{[(K+1)D+K]K}\times\dfrac{P_oT_s}{2V_{in}\Delta V_{C2}} \\ C_3 = (K+1)D\times\dfrac{P_oT_s}{2V_{in}\Delta V_{C3}} \end{cases} \tag{33}$$

To select the proper semiconductors, the maximum value of the current through and the voltage across them are calculated and the results are summarized in Table I.

B. Comparison

In this section, the proposed converters are compared with their counterparts from various points of view. Their voltage and current are presented in Table I. Referring to Figs. 1 and 2, the minimum number of components, including the magnetic core, windings, and capacitors belongs to the proposed converters. However, they have the maximum number of active switches and are mediocre in terms of diode count. It is not enough to only compare the number of elements and a more detailed comparison will be presented in the following. Before that, it is worthy to figure out from where the main attributes of the proposed converter originate, especially when compared to the other smooth dc-link competitors. To do this, let generally take a look at the evolution of the MCIS inverters while their main advantages are listed in Fig. 5(a). In each step forward, the MCIS inverters have added some features to the precedented ones while keeping those main advantages. However, all of them deteriorate the ST current. But the added advantages of the proposed converters consist of the low ST current magnitude too. Comparing the ST currents, it is evident that $0.5\delta I_{in}$ passes through the proposed converters in ST mode while it is δI_{in} for the competitors. It means that δ can be chosen twice larger for the same voltage gain, resulting in a considerably lower ST time duration, lower voltage stress of the H-bridge, and lower amplitude of the switching harmonics, assuming that the ST current is the same. The other major disadvantage of some competitors is the non-zero magnetizing current. It imposes a serious constraint on selecting δ. To investigate this issue, I_m and ST current are plotted versus δ for the understudy

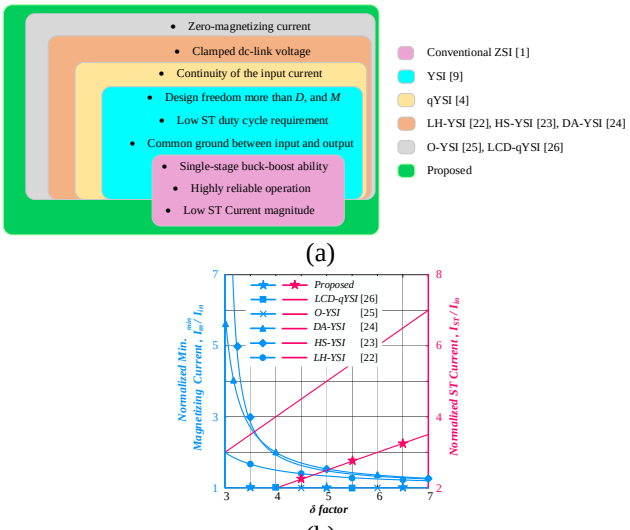
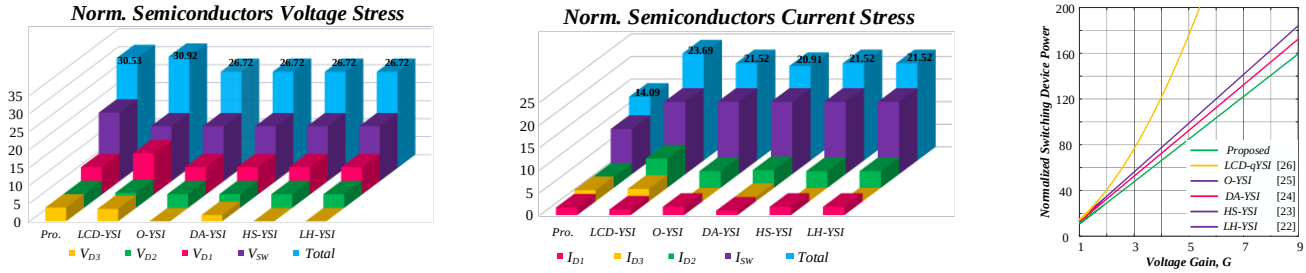


Fig.5. (a) Evolution of the ZSI based on MCIS inverters and (b) investigation of the ST current and minimum dc magnetizing current of the coupled inductor versus δ factor.



(a) (b) (c)

Fig. 6. Comparison of semiconductors' (a) voltage stress, (b) current stress, and (c) SDP of understudy cases.

topologies in Fig. 5(b). As can be seen, the increase of δ decreases the dc-magnetizing current while at the same time the ST current increases. It means that in a try to reduce I_m by increasing δ, the ST current magnitude increase is a severe limit. As an advantage, the zero average value of the magnetizing current of the proposed converters avoids such an undesirable extra constraint. Even though the increase in δ lowers the ST time required, it directly affects other MCIS converters' parameters, especially the voltage and current stresses of the components. As can be seen, the bigger the δ factor, the higher the ST current and the voltage stress of semiconductors (here D_1) of all MCIS inverters. For this reason, it should be chosen carefully to ensure that the aforementioned parameters will be acceptable.

Based on the application that determines the power rating and the required voltage gain, the volume of the inductors or the ST current is more important. Thus, as an example, $\delta = 4$ is considered for all understudy cases to have a numerical design and comparison from different aspects.

1) Active elements

The main parameters that determine the power losses and price of the active devices are the voltage and current stresses. As presented in Table I, D_1 experiences the maximum voltage stress among the semiconductors for all MCIS inverters. Although, the proposed inverters decrease this parameter in comparison to the original impedance network YSI, and LCD-qYSI from $(\delta-1)BV_{in}$ to $(\delta-2)BV_{in}$. The voltage stresses of all active devices are shown in Fig. 6 (a). It is evident that the maximum voltage stresses among all clamped dc-link voltage inverters belong to LCD-qYSI. The proposed converters have fair values. The other key factor is the maximum current stress that is the ST current. As can be seen, the competitors suffer from the high value of δI_{in} while the proposed ones offer half of this value. The current stresses of the active devices are depicted in Fig. 6(b), which shows the proposed converters experience the minimum ones. However, to have a fair comparison, it is necessary to compare the understudy topologies from the switching power devices (*SDP*) point of view. Because it is a measure of the total semiconductor device requirement [38]. This parameter is defined as (34) where $V_{i,\,max,}$ and $I_{i,\,max}$ are the maximum voltage and current stress of i^{th} semiconductor of the converter, respectively. It is calculated for the proposed converters as (35) as well as the competitors based on the voltage and current stresses summarized in Table I and the results are plotted in Fig. 6(c). As can be seen, the proposed converters offer the minimum *SDP* among the understudy cases, hence, it directly means the minimum semiconductor device requirement.

$$SDP = \frac{1}{P_{out}} \sum_{i=1}^{n} V_{i,\max} I_{i,\max} \tag{34}$$

$$SDP_{\text{Pro}} = \frac{B}{P_{out}} \left\{ \frac{3}{1-D} \left[(0.5\delta - 1)(1+D) + D \right] + 2\delta \right\} \tag{35}$$

2) Reactive elements

a) Capacitors

The volume of the capacitor is directly related to its maximum stored energy [39]. Therefore, this parameter is calculated for the proposed converters based on (29) and (33) while for the competitors is obtained according to the parameters presented in Table I. The results are plotted in Fig. 7 while the same voltage ripple is considered for all capacitors. As can be seen, the proposed converters are smaller in comparison to the LH-YSI, HS-YSI, O-YSI, and LCD-qYSI while are bulkier than the DA-YSI in terms of the

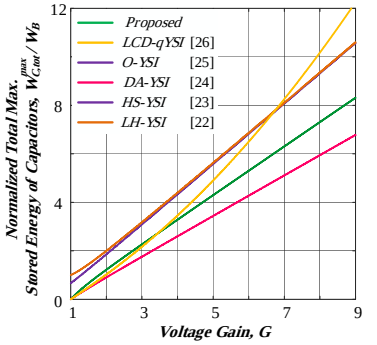


Fig. 7. Comparison of the total maximum stored energy of the capacitors

TABLE II
NUMERICAL DESIGN OF THE COUPLED INDUCTORS FOR DIFFERENT CONVERTERS

Conv.	$L_m(I_{Lm}{}^{max})^2$ *(mH.A²)*	*RMS of windings current (A)*	*Part num. of core*	*Volume and weight*			*Turn*	K_u *(%)*	*MLT (mm)*
				Par.	*mm³*	*gr*			
LH-YSI [22]	73.1930	5.93: 11.17: 9.36	77072	*Core*	49700	288.26	77: 17: 64	30.61	91.005
				Win.	28162	202.47			
HS-SYI [23]	63.2524	6.05: 7.41: 6.50	77072	*Core*	49700	288.26	51:17:85	24.26	88.304
				Win.	21950	157.81			
DA-YSI [24]	65.4133	4.35: 4.60: 4.79	77072	*Core*	49700	288.26	51:51:121	25.46	88.793
				Win.	22989	164.56			
O-YSI [25]	2.1523	3.43: 8.12: 11.48	77090	*Core*	15600	90.84	84:84:28	49.91	70.36
				Win.	22098	158.87			
LCD-qYSI [26]	2.1523	2.71: 8.61: 11.25	77089	*Core*	15600	90.84	57: 95: 57	66.13	77.64
				Win.	31321	225.19			
Prop.	2.1523	3.34: 3.87: 7.15	77083	*Core*	10600	61.48	84:140:28	55.9	65.83
				Win.	16983	122.1			

volume of the capacitors.

b) Inductors

Referring to Table I, all the discrete inductors have the same average current as I_{in}, and all understudy circuits have two inductors in their structure, except for the proposed converters and LH-YSI, which have one fewer. Thus, their advantage over the others is obvious in terms of discrete inductors. However, the coupled inductors are different when their magnetizing current and windings currents are taken into account. Therefore, a numerical design is performed in the following to do an accurate comparison.

Maximum stored energy is the basic factor for the proper selection of the magnetic core to avoid core saturation. This parameter is calculated for the coupled inductor of the understudy cases and the results are presented in Table II. The first core with the higher $L_m(I_m^{max})^2$ is the proper core. The other design factor is the fill factor, K_u. It is defined as the fraction of the magnetic core window area that is filled by the wire and should not be more than 65% [40]. The required area of the windings should be calculated according to the rms value of the winding current and the current density, i.e. $A_w = I_{rms}/J$. The current density is often considered between 3 and 8 A/mm^2. Here, it is selected 4 as a tradeoff between the length of the wire and the efficiency. Also, to reduce the skin effect, the Litz wires are used for the required A_w. Consequently, the area of the winding can be obtained and the cores are selected while the core saturation and fill factor are assumed at the same time and the results are given in Table II. Based on the obtained fill factors, the mean length per turn (MLT) of the windings are derived from the cores datasheet. Although, the coupled inductor with almost ac flux are designed in the different manner in comparion to the ones with a high dc fulx [41], the volume of magnetic core and windings mainly determines these coupled inductors' volume such as the others. Eventually, the weight and volume of the cores and winding are calculated. As can be seen, although the proposed converters, O-YSI, and LCD-qYSI have the same values in terms of maximum stored energy, the higher current of the O-YSI, and LCD-qYSI windings causes a higher A_w and hence a higher core window requirement. Therefore, they are 1.37, and 1.7 times bulkier and 1.36, and 1.72 times heavier than the proposed converters in terms of the Y-shaped coupled inductor properties. Besides, the other competitors are already far beyond the proposed converters in this respect due to their non-zero dc magnetizing current and hence high maximum stored energy, as LH-YSI, HS-YSI, and DA-YSI are 2.82, 2.6, and 2.64 times bulkier and 2.67, 2.47, and 2.43 times heavier in comparison to the coupled inductors of the proposed inverters.

3) Non-ideal voltage gain characteristics

By considering the theoretical voltage gain equations of the proposed converters and the other MCIS inverters, they can change the output voltage from zero to infinity. However, similar to other boost converters their voltage gain is restricted in practice by the parasitic elements, mainly the equivalent series resistance (ESR) of the inductors and the capacitors, forward voltages of diodes, and the ON-state resistance of the diodes and MOSFETs. To investigate this issue, the ideal lossless and non-ideal voltage gain characteristics of the proposed converters and the competitors are calculated based on the method described in [42] and the results are summarized in Fig. 8. They are obtained based on the experimental conditions and the designed parameters in the previous subsection. The modulation index is supposed as $M = 1-D$. As shown in this figure, the proposed converters offer a slightly higher practical voltage gain. It is noteworthy that although the same δ factor is considered for all of the inverters, the competitors require a longer ST to compensate for the voltage drop originating from the parasitic components, especially at higher voltage gains. Therefore, the maximum achievable modulation index of the competitors is also reduced resulting in a higher dc-link voltage requirement and higher amplitude of the harmonics around the multiplications of the switching frequency.

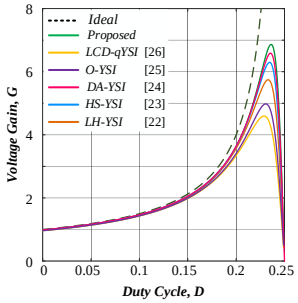


Fig. 8. Comparison of ideal and practical voltage gain versus duty cycle.

I. Small Signal Analysis

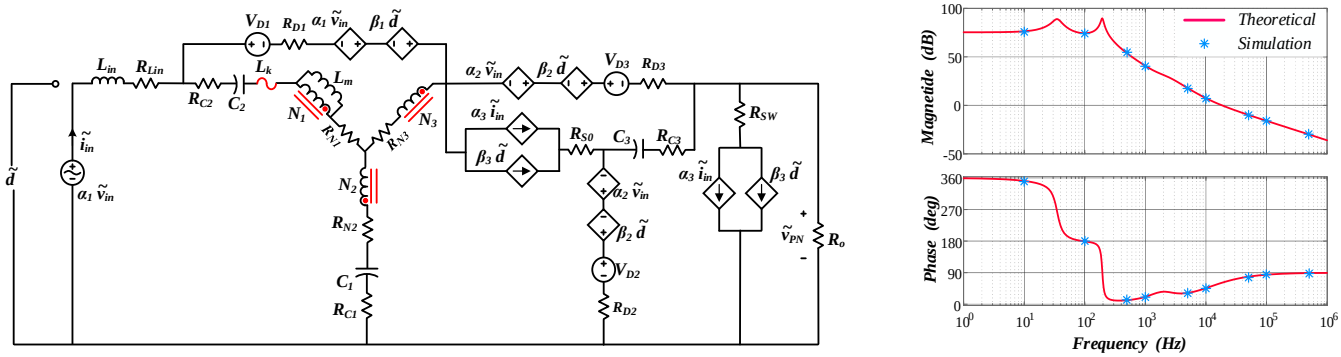
The small-signal model is used to approximate the behavior of power electronic converters with linear equations and provide a means for dynamic and control studies. The circuit averaging technique consists of averaging the current and the voltage of nonlinear elements within one switching period. To do so, diodes and switches are modeled as dependent voltage or current sources [43]. The average of the diodes voltages and the switch current can be obtained from Table I. By extracting the small-signal part of these average values, one can write

$$\tilde{v}_{D1} = \frac{(\delta-2)D}{1-\delta D}\tilde{v}_{in} + \frac{(\delta-2)V_{in}}{(1-\delta D)^2}\tilde{d} = \alpha_1\tilde{v}_{in} + \beta_1\tilde{d} \tag{36}$$

$$\tilde{v}_{D2,D3} = \frac{D}{1-\delta D}\tilde{d} + \frac{V_{in}}{(1-\delta D)^2}\tilde{v}_{in} = \alpha_2\tilde{v}_{in} + \beta_2\tilde{d} \tag{37}$$

$$\tilde{i}_{S0,SW} = 0.5\delta\left[I_{in}\tilde{d} + D\tilde{i}_{in}\right] = \alpha_3\tilde{i}_{in} + \beta_3\tilde{d} \tag{38}$$

where the values with a ~ are perturbations around the operation point. The diodes and the switches are then replaced by the controlled sources shown in (36)-(38), as depicted in Fig. 9 (a). Moreover, the parasitic elements are considered in this average model circuit. From this model, any required transfer function can be attained readily. Therefore, by applying some KVLs and KCLs to this circuit while the input voltage is assumed constant, the transfer function of the control to the voltage of C_1, $G_{vc1\text{-}d}(s)$ is obtained as (39). The



(a) (b)

Fig. 9. (a) AC small signal model, and (b) Bode plot of proposed impedance source network.

$$G_{v_{c1}-d}(s)=\frac{\tilde{v}_{C1}}{\tilde{d}}=\frac{-1e5s^5-8.116e09s^4-1.037e14s^3-8.001e17s^2-5.495e19s+8.451e22}{s^6+16490s^5+2.034e08s^4+6.247e10s^3+3.107e14s^2+2.299e16s+1.444e19} \quad (39)$$

Bode plot of (39) is illustrated in Fig. 9 (b). To confirm the validity of the derived transfer function, the linear small-signal model of the proposed network is implemented in MATLAB/Simulink software. In this figure, both the simulated and calculated Bode plots are shown together which show a close match.

II. Practical Evaluation

To confirm the superior performance of the proposed converter, a 500W laboratory setup is provided. The test rig is shown in Fig. 10 while the parameters and test conditions are presented in Table III. The unipolar PWM and the ST signals are generated by the STM32F407. Also, the coupled inductor is intentionally wound loosely to better reveal the voltage spike mitigation capability of the proposed converter, and the leakage inductances are measured as 0.62, 13.8, 1.25 µH for the first, second, and third windings, respectively. It should be noted that although it is possible to mitigate the 2ω ripple power from the dc side of the converter utilizing extra active and/or passive techniques like what is already presented in [37], here to just concentrate on the novel circuit topology, large capacitances (680µF/400V) are employed for C_1, C_2, C_3 to filter out the low-frequency voltage ripple. Furthermore, considering the effects of parasitic components, the required ST duty cycle is higher than the theoretical value to obtain the desired voltage gain. Therefore, D, and M are set to 0.191 and 0.809 here in order to obtain 220Vrms from 100 Vdc.

First, to show the voltage spike reduction feature of the proposed converter, the part of the circuit that clamps dc-link is disabled. Indeed, D_3 is short-circuited and the gate pulse of S_0 is set to zero. The experimental conditions, presented in Table III, are also considered while IGBTs (FGH40T120SMD) are employed here to avoid the failure of the semiconductors against the voltage spikes. Furthermore, by assuming the boost factor of this converter (B = 1/ [1−(K+1) D]), the spiky circuit requires K = 3 to have the same δ factor (δ = 4). To do so, the turn ratio of the coupled inductor is then modified as 140:84:28. The experimental results including the dc-link voltage and the current of the coupled inductor windings are shown in Fig. 11. When the transition from ST to NST state happens, all currents of the coupled inductor windings abruptly change. Consequently, the voltage spikes appear across the dc-link as its peak value reaches around 1000V while its stabilized value is 396V.

The experimental waveforms of the MCIS inverter with the clamped dc-link are presented in Fig. 12. First, to show the operating modes of the proposed converter, the voltages across the semiconductors are shown in Fig. 12 (a). As can be seen,

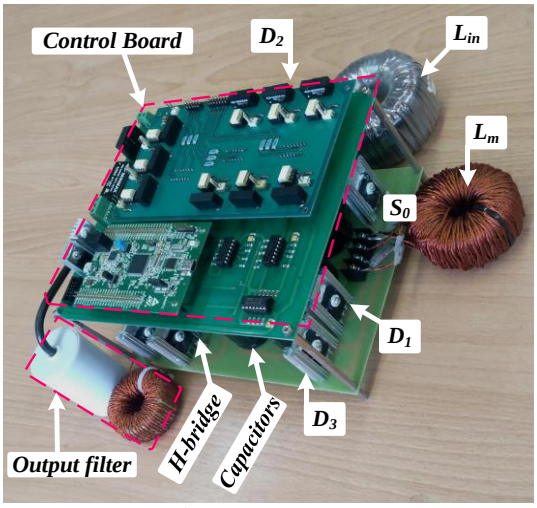


Fig. 10. Photograph of the experimental setup.

Table III
Circuit Parameters and Test Conditions

Parameter	Value
Output power, P_o	500 W
Output voltage, V_o	220 Vrms / 50 Hz
Input voltage, V_{in}	100 VDC
Carrier frequency, f_C	20 kHz
Turn ratio & δ	84: 140: 28 & 4
Inductors L_{in} & L_m	4000 µH & 538 µH
Magnetic Cores for L_{in} & L_m	0077735A7 & 0077615A7
R_{Lin}	260 mΩ
R_{N1}: R_{N2}: R_{N3}	147: 196: 22 mΩ
Capacitors, C_1 = C_2 = C_3	680 µF / 400 V & 32 mΩ
Switches for clamped (spiky) circuit, S_0~S_4	IRFP460 (FGH40T120SMD)
Diodes, D_1 & D_2, D_3	C4D10120D & APT30D60B

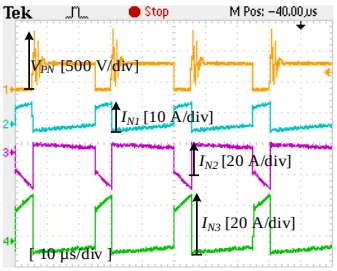


Fig. 11. Experimental Results of the MCIS inverter without clamping technique.

all diodes are reverse-biased in the ST state. On the contrary, in the NST state, S_0 is turned off, and the voltages across the diodes are almost zero. Note that, unlike the DA-YSI, the voltages across D_2 and D_3 are clamped by the capacitors and the ringing is not noticeable in their waveforms. However, the same as the YSI and the smooth dc-link competitors, there is the resonance circuit consisting of the coupled inductor leakage inductance and the capacitance of D_1. Therefore, the ringing appears on the blocked voltage by this semiconductor. Besides, during NST mode, the voltage of D_2 is almost zero which means its blocking voltage is negligible in the second mode of the NST state. To investigate its effect on the dc-link voltage, the ST pulse, the dc-link voltage, and the voltage and current of D_2 are measured and the results are presented in Fig. 12 (b). When the current of D_2 reaches zero, there is no considerable voltage drop at dc-link in comparison to the first mode of the NST state. In other words, the calculated drop of 12 V (from (28)) can be safely ignored in comparison to the dc-link voltage of 393 V. Also, the time interval of this mode αT_s is measured as 10.4 µs that is consistent with its calculated value of 11.18 µs from (16). Then, the high-frequency magnetizing current ripple of the coupled inductor L_m, and the input inductor L_{in}, are shown in Fig. 12 (c). Both of them are charged during ST state and then deliver their energies to the load and capacitors in the NST state. Also, as already expected, the average current of the coupled inductor is almost zero. Next, to show the clamping capability of the proposed inverter, the windings currents of the coupled inductor are shown in Fig. 12 (d). When the inverter enters the NST state, all of them change linearly. Therefore, no noticeable voltage spikes occur across the semiconductors of the H-bridge. Also, the voltages across the capacitors are depicted in Fig. 12 (e). To boost the voltage from 100V to 220Vrms, the capacitors C_1, C_2, and C_3 experience 240, 140, and 394 V, respectively. Then, the output waveforms of the proposed inverter are shown in Fig. 12 (f). The output voltage and current, the dc-link voltage, and the terminal voltage of the H-bridge are presented in this figure. As can be seen, the dc-link voltage is almost smooth and no voltage spike can be detected in these waveforms. Also, the high quality of the sinusoidal waveform is confirmed with a total harmonics distortion (THD) read as 2.4%.

Next, the block diagram of a simple closed-loop control of the proposed inverter is illustrated in Fig. 13. (a) to investigate its dynamic and steady-state behaviors for the grid-connected application. A proportional-integral (PI) controller is designed

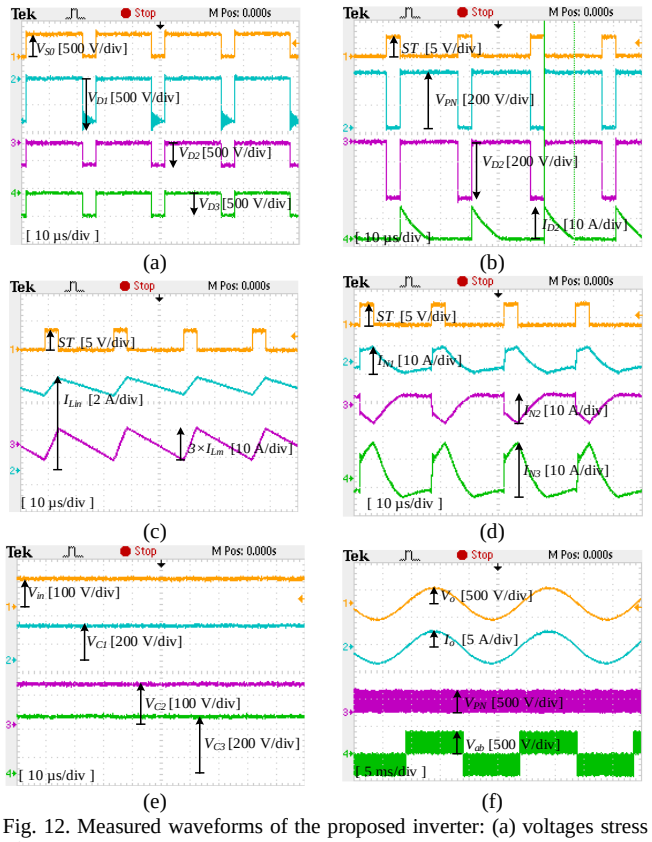


Fig. 12. Measured waveforms of the proposed inverter: (a) voltages stress of the impedance network active devices, (b) ST signal, dc-link voltage, voltage and current of D_2, (c) ST signal, and input and magnetizing currents, (d) current of coupled inductor windings, (e) input and capacitors' voltages and (f) output voltage and current, dc-link voltage (V_{PN}) and inverter voltage (V_{ab}).

based on the derived transfer function of (39) and frequency-

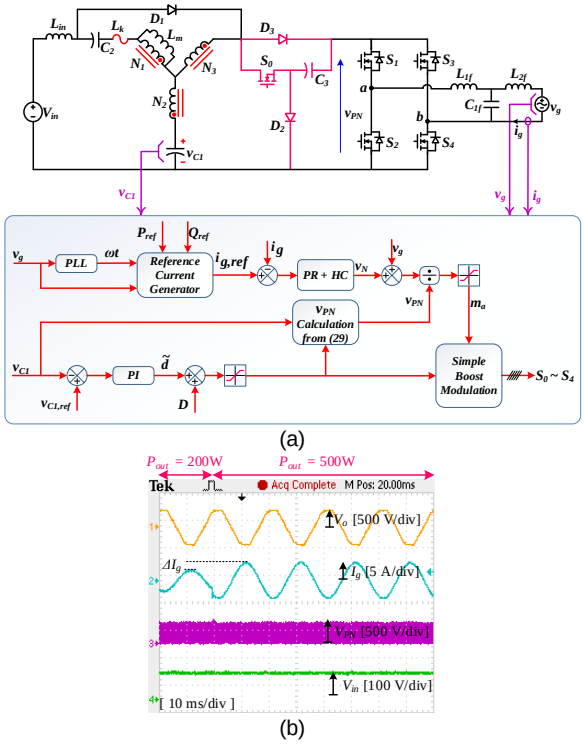
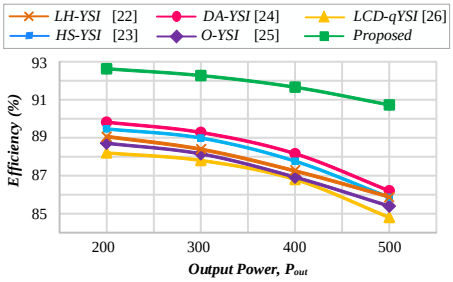
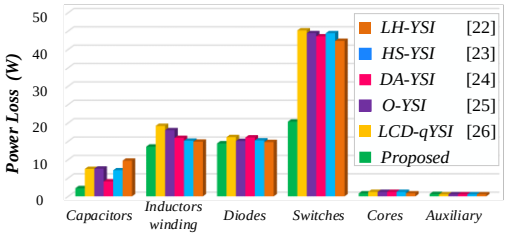


Fig. 13. (a) Control block diagram of the proposed MCIS inverter in grid connected application, and (b) experimental results for output power step change from 300 to 500W.



(a)



(b)

Fig.14 (a) Efficiency comparison and (b) loss distribution at 500W output power.

domain design approach explained in [44], which results in K_P = 1.48×10^{-5} and K_I = 648.6×10^{-5}. The closed-loop system is stable and the rise and settling times in response to a step-change in the reference of active power are almost 90.3 ms and 161 ms, respectively. The controller effectively regulates the dc-link voltage through the voltage feedback of the capacitor C_1. Also, D, the ST duty cycle at the equilibrium operating point, can be calculated from (31). Furthermore, $V_{C1,ref}$ can be obtained as $(1-2D)V_o^{max}/\eta(1-D)$ while considering simple boost modulation and (29). In addition, η is assumed here as the converter efficiency coeffeincet [45]. A phase-locked loop (PLL) is also used to detect the phase of the grid voltage and generate the reference current of the inverter based on the desired active and reactive powers i.e. P_{ref} and Q_{ref}. Then, a proportional-resonant (PR) controller with a harmonic compensation (HC) network is used for the current loop [46]. Finally, the PWM signals are generated based on the simple boost modulation. Fig. 13 (b) depicts the experimental results in response to a step change in the reference active power from 300 to 500 W while the test conditions are listed in Table III. Evidently, the simple control scheme of Fig. 13 (a) can provide a fast and smooth transient with a highly sinosoidal grid current as its THD is read 2.9% by a Fluke 435 power quality analyzer.

Furthermore, a comparative analysis of the efficiency of the understudy circuits is performed. The shoot-trough duty cycle is manually adjusted to keep the output voltage constant at 220Vrms while P_o changes from 200 to 500 W. To carry out a fair comparison, the passive components are designed according to the same current and voltage ripple for the inductors and the capacitors, respectively. Also, the same semiconductors, reported in Table III, are supposed here for all of them. Based on the above assumptions and the method presented in [15], the efficiencies are obtained and the curves are plotted in Fig. 14 (a). As already expected, due to the significant reduction of the ST current, the proposed converter offers higher efficiency in comparison to the competitors reaching 92% while the competitors cannot even reach 90%. The distribution of losses among different components is depicted in Fig. 14 (b). Based on the theoretical analysis, the competitors suffer from a high ST current, which is twice the proposed one. Therefore, the decrease of reactive components power losses was already expected. Although, the resistance values of the windings of the proposed inverter are supposed higher than the competitors due to the lower current stress and the same current density consideration. In addition, the total power loss of the active switches of the proposed inverter is obtained as 20.3W while it is 45.1W, 44.4W, 43.5W, 44.4W, and 42.3W for the LCD-qYSI [26], O-YSI [25], DA-YSI [24], HS-YSI [23], and LH-YSI [22], respectively. Also, the power loss of driver and isolated power supply power consumption is considered in the auxiliary power losses. Evidently, the total power losses of the switches of the proposed converter are decreased almost 100% in comparison to the competitors leading to efficiency improvement and lower cooling system requirements. In addition, the power loss in the magnetic cores is the lowest for the proposed one. However, in comparison with the nominal power of the converters, the calculated values of core losses for all magnetic cores are small and have a negligible effect on the converter efficiency.

Finally, the converters are compared in terms of power density in Fig. 15. The volume of the inductors, the maximum stored energy of the capacitors, and the power losses of the active devices as a measure of their cooling system volume are listed in this figure. All of these volume indicators are normalized by the minimum value in each case to facilitate the comparison. As can be seen, the volume of the coupled inductors of the proposed converter is the lowest among all. It is because of the zero-mean magnetizing current and lower windings area requirement in the wake of low ST current. It is almost 200% less than the LH-YSI. Also, the proposed inverter is ranked second when the volume of the capacitors of the inverters is investigated. It is just 28% higher than the DA-YSI that has the minimum capacitor volume. Furthermore, the proposed converter is superior in comparison to the competitors in terms of the cooling system. Totally, the competitors LH-YSI, HS-YSI, DA-YSI, O-YSI, and LCD-qYSI are roughly 80, 76, 60, 48, and 46% bulkier than the proposed topology.

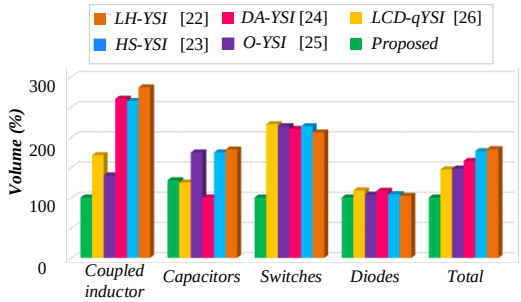


Fig. 15. Comparison of the understudy cases form volume point of view.

III. Conclusion

This paper proposes two MCIS inverters that offer a clamped dc-link voltage with no voltage spikes across the H-bridge semiconductors. Significant ST current reduction and zero dc magnetizing current of the coupled inductors are other main achievements. Therefore, the volume of the coupled inductors is almost independent of the power rating and voltage gain. Generally, in comparison to the other successful competitors with a smooth dc-link voltage, the proposed circuits offer a higher power density and efficiency. Also, the proposed clamping technique can be utilized to effectively suppress the voltage spikes of the other MCSI inverters with the lower shoot-through current. The validation of the aforesaid properties is done through extensive experimental tests on a 500 W laboratory setup.

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