Investigation into the manipulation of non-uniformity and undercut features of a positive profile through silicon via.

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Summary

The key enabling technology for 2.5D and 3D packaging applications is the through silicon via (TSV), this device allows integrated circuits and additional component layers to be vertically stacked, this minimises internal signalling lengths allowing for faster operation, reduced heat production and lower power consumption.

TSV's are commonly formed with a positive profile structure which minimises conductor deposition defects in downstream production stages. This research was carried out on an SPTS Technologies Ltd Pegasus™ deep silicon etcher employing a single step $O_2/SF_6/Ar$ process. The aim was to identify a predictable set of process parameters that can be used manipulate the dimensions of the 'undercut' feature that regularly forms at the top of the TSV profile during dry plasma etch processing.

An L16 (4^5) Taguchi Array was used to determine the interaction effects of changing five critical process parameters on the undercut feature dimensions. The results from the process sample runs were analysed using commercially available statistical analysis software to investigate any predictable interactions between process parameter values and TSV profile dimensions. The outcome showed that there were no relationships that would facilitate predictable manipulation of the undercut dimensions. However, a clear and predictable trend was observed from the results which showed that increasing the wafer platform temperature results in a decrease in across wafer non-uniformity of critical TSV profile dimensions.

Declarations

Declarations

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

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Date: 10/12/2021

This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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The University's ethical procedures have been followed and, where appropriate, that ethical approval has been granted.

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Definitions or Abbreviations

IC	Integrated Circuit
TSV	Through Silicon Via
ITRS	International Technology Roadmap for Semiconductors
ISSCC	International Solid-State Circuits Conference
DRAM	Dynamic random-access memory
FEOL	Front End of Line
BEOL	Back end of Line
CVD	Chemical Vapour Deposition
PVD	Physical Vapour Deposition
ECD	Electro Copper Deposition
CPU	Central Processing Unit
RAM	Random Access Memory
DoE	Design of Experiment
SEM	Scanning Electron Microscope
TE	Thermionic Emission
ICP	Inductively Coupled Plasma
RF	Radio Frequency
HeLuR	Helium Leak-up Rate
FCC	Federal Communications Commission
ISM	Industrial, Scientific and Medical
Pegasus	Plasma Etch Giving Advanced Speed Uniformity and Selectivity
RSq	R Square
RMSE	Root Mean Square Error
ESC	Electrostatic Chuck
W/mK	Watts per meter-kelvin
Torr	A unit of pressure equivalent to 1mm of mercury in a barometer

Chapter Content Descriptions

The contents of this programme of work are as follows: -

- Chapter 1 describes the history behind the integrated circuit from the time of its invention to current levels of technology and follows on to explain the evolution of the through silicon via and its manufacturing limitations.
- Chapter 2 introduces the design of experiments criteria and the analytical techniques that are used to investigate the manipulation of the positive profile TSV.
- Chapter 3 details the results obtained from the DoE etch process runs and explains the outcome from the data regression analysis.
- Chapter 4 discusses the steps taken with computer modelling simulation to eliminate the possibility that the across wafer non-uniformity changes were being affected by the wafer platform temperature.
- Chapter 5 explains the conclusions that were drawn from this programme of work and identifies areas that will allow the research to be expanded.
- Chapter 6 introduces the research paper that resulted from this program of work that was presented to the IMAPS 16th International Conference and Exhibition on Device Packaging.

Chapter 1 - Introduction

This chapter details the history of the integrated circuit from the time of its invention to current technology levels, following on to explain the evolution of integrated circuits and details why the through silicon via (TSV) was developed. The discussion then turns to some of the process and manufacturing limitations associated with the production of TSV's and how they are typically overcome, finishing with an investigation into current research on positive profile TSV manipulation and the expected scope of this programme of work.

1.1 Integrated Circuit History

The integrated circuit (IC) is sometimes referred to as a silicon chip or microchip and is a piece of silicon about the size of a small fingernail on which interconnected transistors, capacitors and resistors are fabricated as a single assembly. The IC is ubiquitous in everyday life and is used in virtually every piece of modern technology from washing machines to televisions, computer games consoles, military aircraft, or the International Space Station, all will have many integrated circuits embedded within them to control their operation.

The transistor is a semiconductor device which is a fundamental building block for all modern electronic devices, it consists of three layers of semiconductor material that are sandwiched together. When a current or voltage is applied to the centre layer of the stack it produces a large change in the current passing between the two outer layers, it is this effect that allows the transistor to be used as a switch or an amplifier in an electronic circuit. A working model of the junction transistor was first demonstrated by William Shockley and his team at Bell Laboratories in New Jersey USA in December 1947 [1]. In the years after its invention computer engineers used the transistor to increase the performance of their designs. Computers were initially constructed from a series of discrete components with each module performing a single task, however each unit needed to be physically wired and soldered to every other component in the system by hand, this meant that even a single incorrectly soldered joint could make the whole computer fail to operate. As computers became more powerful the performance enhancements were tied to the increasing complexity of the designs, this added ever growing numbers of interconnects between components inside the computer which resulted in the new models becoming increasingly unreliable as additional modules were added.

This problem was described by J. A. Morton, Vice President of Bell Laboratories in his June 1958 article “The Technological Impact of Transistors” at the “Proceedings of the IRE” (Institute of Radio Engineers) celebrating the 10 year anniversary of the invention of the transistor in which he described the “Tyranny of Numbers” [2]

“*Such systems, because of their complex digital nature, require hundreds, thousands, and sometimes tens of thousands of electron devices. The large amount of power used inefficiently and the high cost of reliability of the electron tube have prevented these expansions of electronics in all but a few cases where the high cost could be tolerated, even though not desired”*

Jack Morton – Bell Laboratories

Two months after Jack Morton made this speech, on the 12th September 1958, Jack Kilby of Texas Instruments managed to demonstrate the first working integrated circuit by manufacturing resistors and capacitors from a single piece of germanium and then wiring them into a transistor circuit [3]. Six months later, Robert Noyce of Fairchild Semiconductor invented a way to interconnect the capacitors, resistors, diodes and transistors of a circuit by laying a metal film over the semiconductor material and etching away the unnecessary parts to create the connections between each component [4], it was these two advances in technology that greatly reduced the size of computer components by removing all of the manual interconnects between each component, and allowed them to be mass produced.

There are 5 levels or generations of integrated circuit which are shown in Table 1.

Table 1: Levels of integrated circuit [5]

Level	Title	Active devices per chip
1	Small Scale Integration (SSI)	< 100
2	Medium Scale Integration (MSI)	100 – 10,000
3	Large Scale Integration (LSI)	10,000 – 100,000
4	Very Large-Scale Integration (VLSI)	100,000 to 1 million
5	Ultra-Large-Scale Integration (ULSI)	> 1 million

Small scale integration (SSI) circuits were essential for early aerospace projects and they were extensively used for the guidance systems in the Minuteman II & III nuclear weapons systems [6] and the Apollo Moon Programme [7]. The main advantages of the IC over discrete electronics in these applications were a decrease in the size, weight and power consumption against comparable components which are features that are crucial in a system where every extra gram of weight increases fuel consumption [8]. In the years between 1962 and 1964 the United States Government purchased nearly all the supplies of integrated circuits that were available as can be seen in table 2. It was this guaranteed market provided by the US Government that allowed the IC manufacturers to invest and expand the device production when costs were high and yields were low, this supported the fledgling market until the IC manufacturing costs dropped to a point at which they became attractive for commercial uses [9].

Table 2: Average price of IC's and proportion of production consumed by military [9]

Year	Average Price ($)	Consumed by Military %
1962	50 – 100	100
1963	31 – 60	94
1964	18 – 50	85
1965	8 – 33	72
1966	5 - 33	53
1967	3 – 33	43
1968	2 - 33	37

The ceaseless drive to put an ever-increasing number of circuit functions on a chip has provided the incentives to keep scaling down the devices in size. As the number of devices per IC are increased you achieve the additional benefits of higher yields, improved reliability, lower manufacturing costs and increased performance [10]. It was Gordon Moore in 1965 who first tabled the idea that device transistor density approximately doubles every year [11], but he revised this figure to doubling every two years in 1975. This rule which in now known as Moore's Law has held true since 1975 and is used to guide long term plans and research targets for the Semiconductor industry. While no specific limit has been established, it appeared that the validity of Moore's law for consumer electronics would cease at critical dimensions (CD's) smaller than 0.05µm (5 nanometres) due to fundamental limiting factors stemming from electron thermal energy and quantum mechanical tunnelling [12] through the gate oxide layer [13].

1.2 2.5 D and Beyond

Transistor miniaturisation was still the main focus of the semiconductor industry as recently as 2013, when the penultimate International Technology Roadmap for Semiconductors (ITRS) was released [14]. The report concluded that the physical gate length (an indication of how far current must travel within the device) of the transistors was predicted to shrink until at least 2028. The semiconductor manufacturers when being faced with ever increasing development and production costs to keep up with the pace of Moore's law decided that that the future led in a direction away from continual shrinking of transistor dimensions [15]. The path investigated was to build circuits using three dimensional concepts rather than the historical two-dimensional chips. The idea of building devices in three dimensions is not a new concept, with this being first identified by J. M. Early of Bell Labs who proposed the stacking of a number of components in a cubic configuration at the ISSCC (International Solid-State Circuits Conference) in February 1960 [16]. But it was not until ~2010 when the technology to manufacture these devices became cost effective, with the Intel "Ivy Bridge" CPU products becoming the first commercial 3D devices to be introduced to market in April 2012 [17]. The final ITRS 2.0 report released in April 2016 embraces the trends toward 3D architecture and predicts an end to the traditional shrinking of chip features by the early 2020's as it will become more cost effective to produce 3D IC's. Paolo Gargini the chair of ITRS said that the idea that we are facing an end to Moore's Law is completely wrong, stating that there is only one way of defining Moore's Law and that is that the "number of transistors doubles every two years." The law is simply a prediction on how many transistors can fit into a given area of IC irrespective of the whether it's done in a single layer or the stacking of multiple layers [15].

1.3 Integrated Circuit Packaging Types

Figure's 1 to 3 show the evolution of the integrated circuit layout since its invention in the early 1950's.

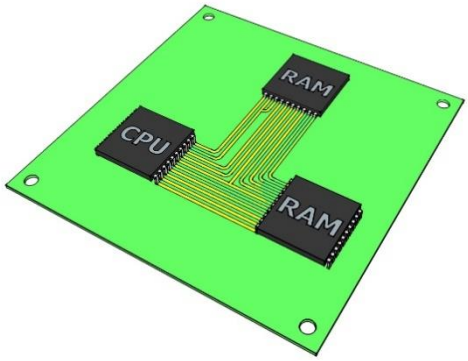


Figure 1: Traditional CPU/RAM

Figure 1 shows the typical circuit layout that is easily recognisable, where each device is separate on a circuit board and is connected via conductive 'tracks' running along the surface of the non-conductive substrate.

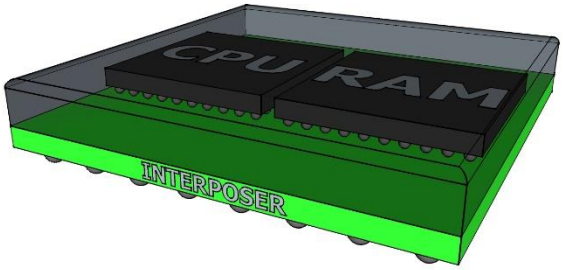


Figure 2: CPU/RAM in a single package (2.5D)

Figure 2 indicates the typical construction of a 2.5D assembly where individual devices are placed close together, and the connections are made via ‘through silicon vias’ (TSVs) and tracks inside the interposer layer which is used to spread the connections between the individual devices, this assembly is usually packaged together as a unit and has external connection points to allow for insertion into a larger assembly [18].

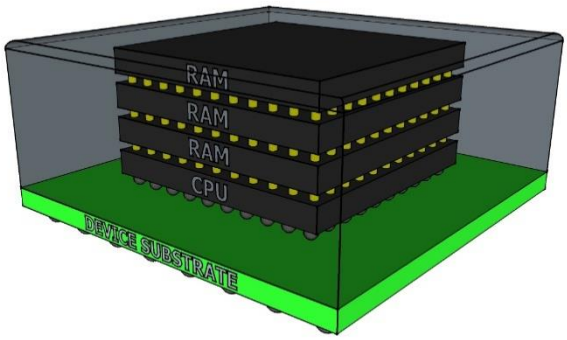


Figure 3: True 3D IC Package

Figure 3 shows a full 3D assembly, this is a device that has 2 or more layers of active components that are integrated both horizontally and vertically into a single package. All components in the layers communicate using on-chip signalling which minimises the internal signal connection lengths allowing for faster operation, less heat production and lower power consumption [19].

1.4 Through Silicon Vias (TSVs)

The key enabling technology for 2.5D and 3D IC packaging solutions is the through silicon via, the TSV is a conductive plug (usually formed from one of three materials, copper, tungsten, or polysilicon (poly-Si) which passes completely through the silicon die and forms connection points on the top and bottom surfaces of each layer. These connection locations allow additional component layers to be easily added allowing three dimensional integrated circuits to be constructed [18]. Figure 4 shows a cross section through a Samsung DDR4 Dynamic random-access memory (DRAM) memory device that displays a practical example of a TSV, the plug locations and the soldered connections between the individual DRAM dies are clearly visible in the 'underfill' sections indicated on the image.

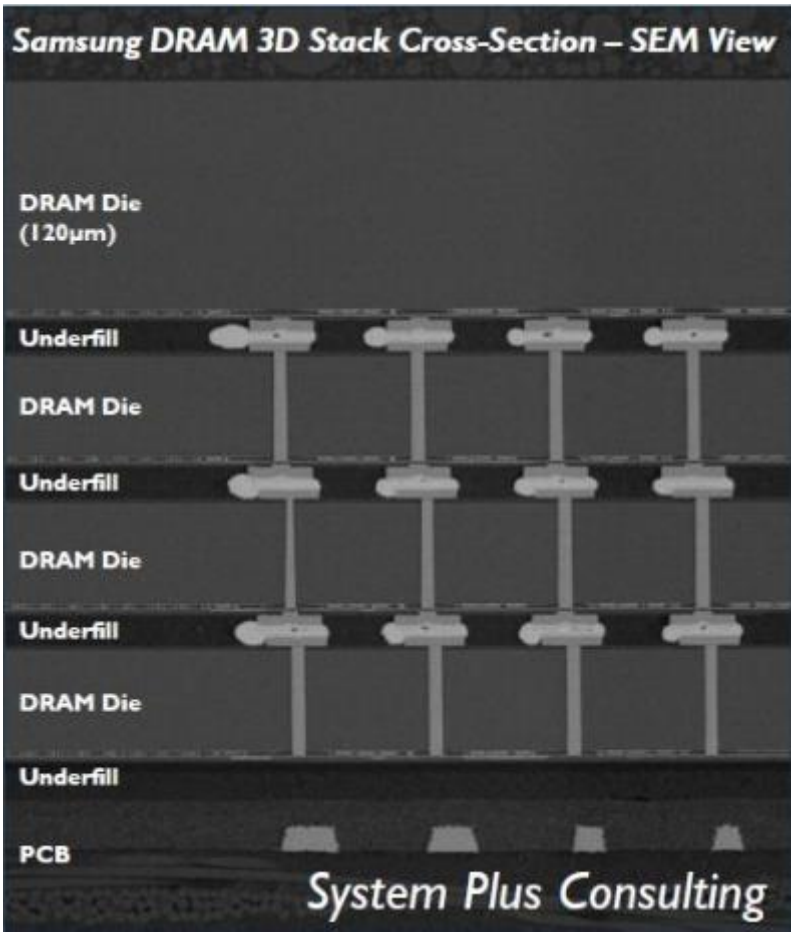


Figure 4: Samsung DDR4 DRAM Memory Stack (Source: Samsung 3D TSV, Stacked DDR4 DRAM report – System Plus Consulting, 2015.)

1.5 TSV Construction

TSVs can be fabricated at three positions in the device assembly process with each type of TSV having specific roles. TSV diameters are typically in the range of 0.2µm-100µm depending on the feature application, although it should be noted that as the diameter of the TSV reduces, the substrate thickness and TSV depth must also lower to preserve the aspect ratio of the feature below 20:1. This is to ensure that the etch and subsequent material fill can be assured to be of sufficient quality for successful manufacturing [20].

Via First – The TSV features are fabricated before any of the device components, the main drawback with this method is that the filling material is exposed to the full front end of line (FEOL) temperatures (>400^{o}C) [21], this limits the choice of filler material to either tungsten (W) or poly-Si, as copper (Cu) will migrate into the surrounding material at these temperatures. A key advantage with this method is that it is the simplest approach as there is no consideration needed for contamination or alignment of the TSV structures.

Via Middle – The TSV is created after the FEOL processes are complete but before the back end of line (BEOL) processes have begun, as a result the TSV is not subjected to the high temperatures that are required during the frontend process steps. A benefit of these lower heat loads is that copper can be used as the filler material as it will not migrate at lower processing temperatures. Copper is the preferred filler material due to its cost, low electrical resistance, compatibility with conventional interconnections, and is a good match to the coefficient of thermal expansion of silicon [22].

Via Last – The TSV's are created either during the formation of the Si BEOL structures, or at the end of the process when the wafer is effectively complete. The structures created at this stage in the process see very little heat load (<160^{o}C) and the process steps are considered to be low temperature [23], it has the disadvantage that the alignment of the TSV's to the die needs to be accurately positioned so that none of the completed components are damaged [24].

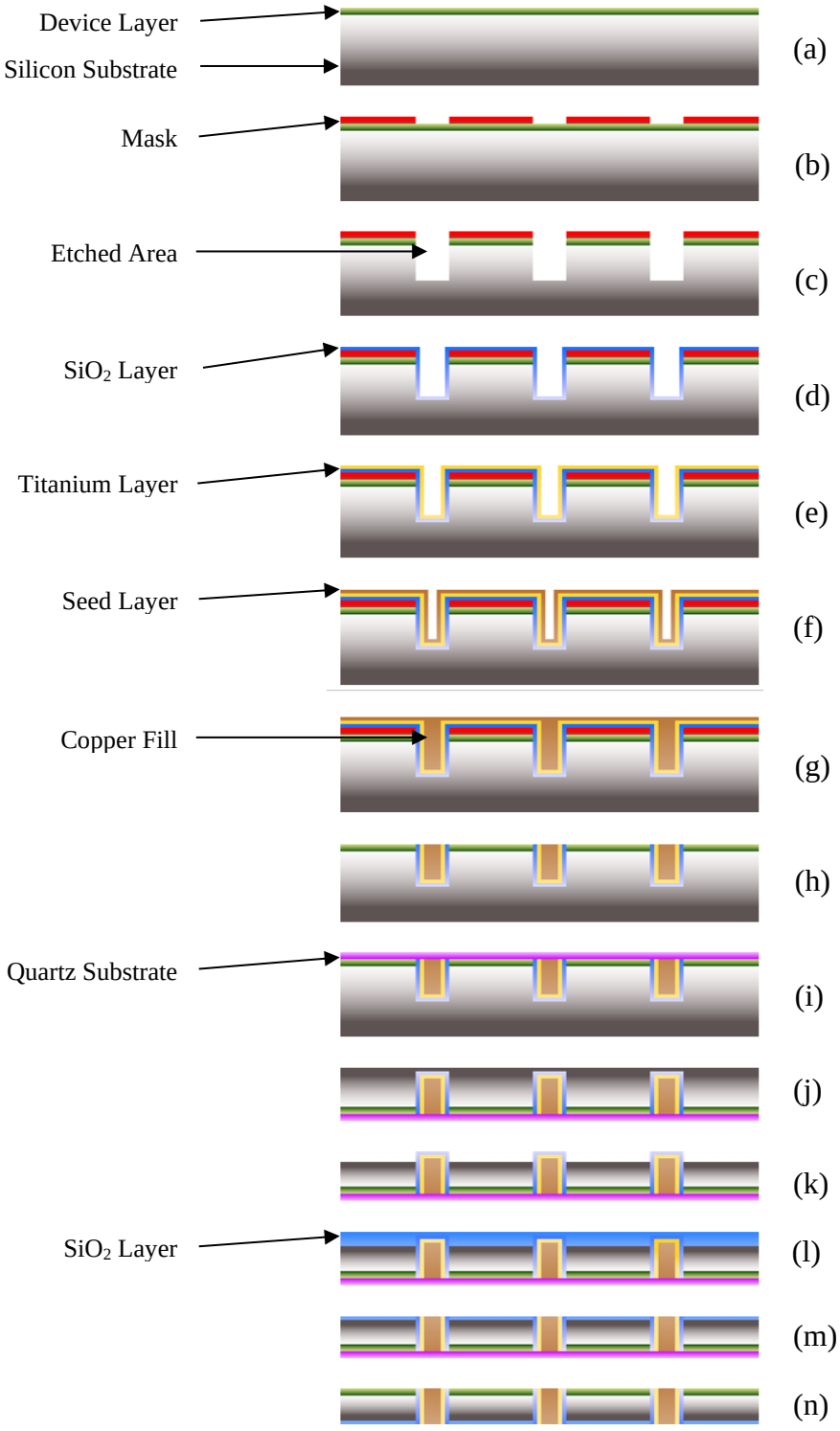


Figure 5: Typical TSV (via middle) Manufacturing Process

The list below explains the process steps that are illustrated in Figure 5, this a typical production method for a TSV irrespective of where in the process flow it is constructed.

(a) A substrate with the required device layer is prepared to the requirements of the application.

(b) A mask with the desired feature pattern is formed upon the surface of the substrate using a photolithographic process.

(c) The wafer is placed into an etch chamber and the features are etched to the required depth.

(d) A silicon oxide (SiO_2) layer is deposited via CVD (Chemical Vapour Deposition) onto the surface of the substrate, this is a dielectric material and acts as an insulating layer to prevent electrical contact between the copper plug and the silicon substrate.

(e) A titanium (Ti) layer is deposited via PVD (Physical Vapour Deposition) onto the surface of the substrate which acts as an adhesion layer allowing the copper plug to adhere firmly into the assembly.

(f) A copper seed layer is deposited onto the Ti layer via PVD and is used to prevent voids forming inside the copper plug during its formation.

(g) Copper is deposited onto the surface of the seed layer, covering the entire surface of the substrate whilst filling in the etched plug holes. The filling process can be performed using PVD, but more commonly it is laid down using an electro copper deposition (ECD) process.

(h) The entire stack of layers is ground or etched back to the device layer which leaves isolated vias within the device layer.

(i) A quartz substrate is bonded to the top of the device layer.

(j) The stack is flipped over so that the quartz becomes the base layer.

(k) The silicon substrate is etched away to expose the SiO_2 covered copper plugs.

(l) A further SiO_2 layer is deposited via CVD onto the entire surface of the substrate to a sufficient depth to cover the proud standing copper plugs.

(m) The SiO_2 is exposed to either etching or a grinding process that removes the excess material exposing the surface of the copper plug.

(n) The assembly is flipped over, and the quartz substrate is removed.

The completed assembly has a device layer with external connection points on both the top and bottom surfaces, these connection points will allow other components and modules to be intimately connected to the device in order to construct close coupled three dimensional structures [24].

1.6 TSV Profile Undercut Formation

This programme of work specifically deals with positive etch profiles and anomalies related to the manufacture of these features. This project will focus on the positive etch profile as opposed to straight or negative profiles [25] since the positive profile is the most widely used shape for TSV manufacturing as it has been proven to be more cost effective overall to produce than the other profile shapes.

Figure 6: TSV Feature Profiles [25]

This cost benefit is provided by the ease of producing follow on manufacturing steps that involve either metal or insulating material deposition; a positive profile with a smooth sidewall will produce the most consistent results for follow on manufacturing processes as no part of its shape overhangs any other part of the structure. A negative profile has a bottom width that is larger than its top width, and as a result a large part of the feature will be shadowed by the top opening of the profile. The straight profile has vertical ‘cliff edges’ which can cause difficulties obtaining a consistent film thickness and deposited material will naturally gravitate towards the bottom of the feature causing inconsistent film thicknesses [26].

One of the largest defects resulting from the positive etch process is the formation of a feature at the top of the profile that is often known as an ‘overhang’, ‘undercut’ or ‘lateral etching’; where the area directly below the mask is narrower than the widest dimension of the TSV structure as shown in Figure 7b. There are two main factors that influence its formation with the minor effect being the SF_6:O_2 ratio which can reduce the size of the undercut, but has the added effect of adjusting the taper angle of the holes as the ratio is changed [27]. For this series of experiments the SF_6:O_2 ratio has been fixed at 1.95:1 for the duration of this design of experiments (DoE) to minimise a known effect on the TSV profile shape skewing the interpretation of the results. The major effect that influences the size of the undercut is ‘ion scattering’ where the fluorine (F) ions are deflected by the edge of the mask into the top area of the feature and has the effect of significantly increasing the lateral etching in this area leading to the formation of the undercut, the level of lateral etching appears to be dependent on time/etched depth rather than depth/width (aspect ratio) [28]. Figure 7 (a) shows a positive profile TSV structure with no undercut at the top of the feature, Figure 7 (b) displays the same structure at a different location on the substrate which clearly shows the undercut formation.

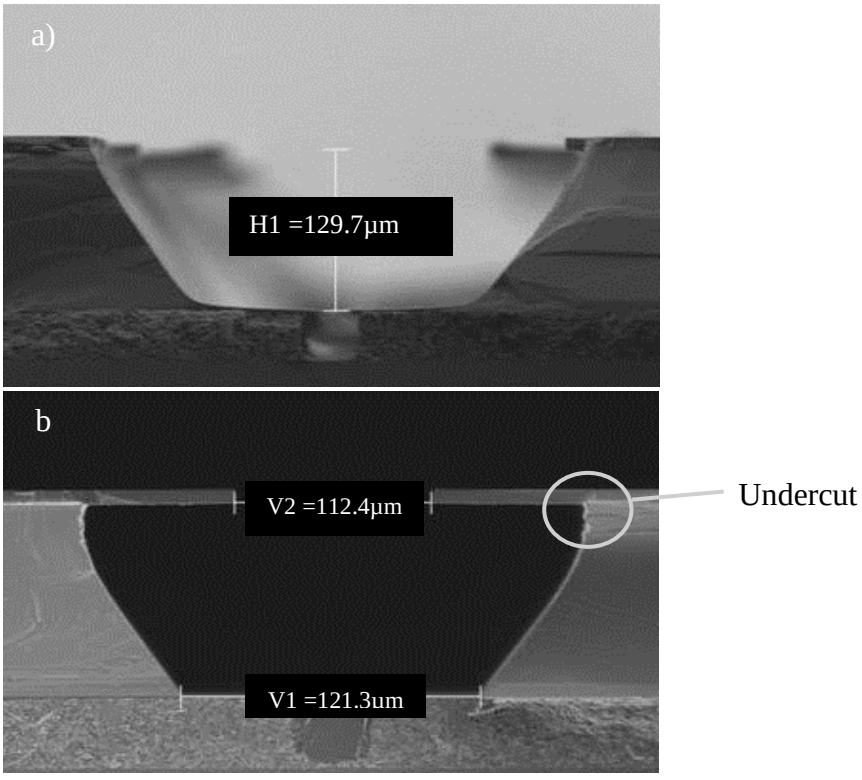


Figure 7: TSV Overhang, a) Centre position, b) Edge position

The next step in the manufacturing procedure after the TSV profile has been etched is to add a layer of metal via a physical vapour deposition (PVD) process, the film created by the PVD process is plasma vapourised from a metal target located at the top of the process chamber onto the wafer by gravity with no form of additional attraction. For this metallic film to be evenly distributed over the surface of the profile there must be a clear line of sight to all parts of the feature from the opening at the top of the TSV, no part of the internal surface of the structure must be overhanging any other part of the structure as documented in the introduction.

The presence of an overhang means that the top of the structure is covering at least some of the area below it, this creates a shadowed area that cannot be coated by the deposited metal layer as shown in [29], the overhang feature can be clearly seen in the SEM photograph of every process run that is detailed in the results section.

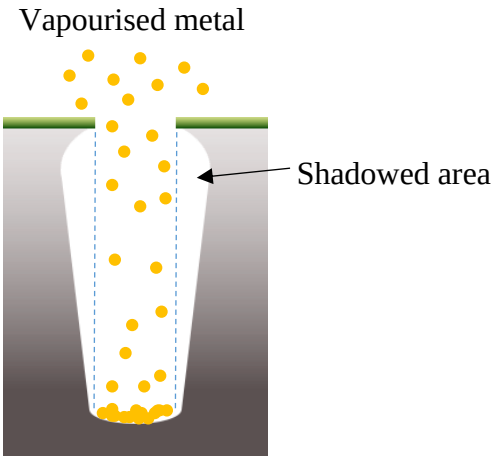


Figure 8: Overhang Shadowing Effect

1.7 Two Stage Undercut Removal Method

When a semiconductor device requires a TSV it is usually because this device is part of a larger assembly that will have other components connected to it. The size and position of the TSV's are crucial and are required to be consistent across the entire wafer surface to ensure that any mating parts line up accurately in further process steps as can be seen in Figure 4. The presence of an undercut is not ideal, as its size and uniformity at various locations across the wafer may not be consistent as shown in Figure 7 (a) & (b), with the resulting negative profile at the top of the TSV making it difficult to successfully deposit continuous insulating, diffusion and seed layers by standard deposition processes as the bowed surfaces are likely to create voids during the trench filling steps [29, 30]. Consequently, a follow on 'thinning' process is required to remove the undercut, leaving the feature with no overhanging areas. The removal of the undercut leaves a much more controllable feature as the sidewalls below the lateral etching region are more likely to conform to the feature dimension requirements due to a lack of lateral etching effects. A typical thinning process flow is shown in Figure 9, and typically follows these three steps irrespective of the method used to thin the material.

9 (a) Completed etch process

9 (b) Mask removal

9 (c) Thinning process

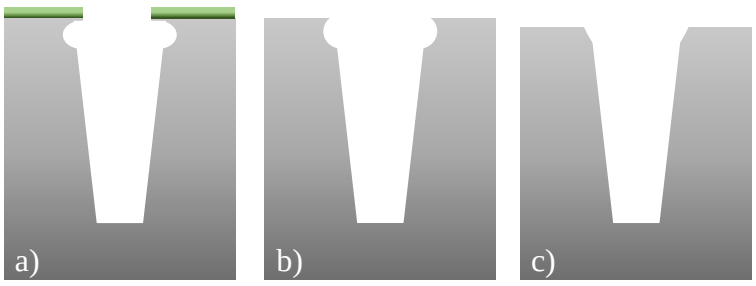


Figure 9: Typical overhang process flow removal process [31]

The ‘thinning’ procedure is another production process that involves physically stripping away the top layer of the substrate to a depth slightly below the bottom of the lateral etching region. This can be done by either a plasma etch blanket removal process where the top surface of the substrate is etched away in an ICP reactor [31], or by physically grinding the surface of the substrate away using a semiconductor grinding machine [32]. Whilst either thinning method can adequately remove the excess material, grinding can remove material at a faster rate than dry etching, but the final wafer thickness is more difficult to control. Testing has shown that grinding causes a damaged layer roughly 200nm thick that has large compressive stress leading to a concavely bowed substrate that requires an additional stress relief process when the griding is complete [33]. Dry etching is a slower method of material removal but it typically has an improved surface roughness value and chip strength is up to 50% greater after the process is completed, as stress is not introduced into the substrate during thinning, there is no requirement for a stress relief step at the end of the process [34].

The fact that the process is necessary adds additional costs and time to the production of the devices that could be avoided if the correct process recipe parameters are identified that create the TSV with the required profile during the etch step.

1.8 Current Research on Undercut Manipulation

Recent research shows that the size of the undercut or ‘local bowing’ as it’s sometimes described is dependent on the depth of the trench. As the etch progresses the TSV profile becomes deeper and larger with the undercut formation following this trend, the scope of the research so far is limited to parallel profile trenches and not the positive profiles that are being discussed in this project. Researchers [30] additionally found that the undercut form seemed to be dependent on the balance between the relative ion density and the fluorine/oxygen gas ratio, it was theorised that by adjusting the gas ratio you could alter the balance between passivation and sidewall etching. The ion density appeared to be key in the size of the undercut, as increasing the RF energy causes the undercut to increase in size. The researchers concluded that increasing the RF energy leads to more ion production but an unanswered question remained as to the mechanism behind the obvious pathway deviation of the ions away from the normal vertical direction of travel [30].

In a follow up study to this research, a separate team took the conclusion from the research paper written by M. Boufnichel and attempted to answer the question of why the ions appeared to be deviating from their vertical path and hitting the sidewalls of the feature, thus assisting in the formation of the undercut. The research was initiated by adjusting the ratio between the O_2 and SF_6 process gasses and it was observed that by changing this ratio the amount of lateral etching can be greatly reduced, but it was also found that adjusting this ratio produced strongly tapered sidewalls which is the effect that will be exploited in this programme of work. The researchers used a Monte Carlo simulation [35] to predict the transportation of etch species into the features and measured the numbers of fluorine radicals interacting with the sidewalls, the results of this test showed that the F radicals have a large effect on the etching of the sidewalls at the top of the feature, but this effect reduces with depth. It was concluded that this mechanism is responsible for the tapered sidewalls but cannot fully explain the type of lateral etching formation that appears during the etch process. It was noted during the experiments that the corner of the mask was becoming etched, and a chamfer was forming; if a line

was drawn down the chamfer angle and continued until the line intersected the feature sidewall it corresponded with the bottom of the lateral etching region. To prove this effect researchers have deliberately created a chamfered feature at the mask hole edge and ran the same etch process on the sample. It was recorded that the angle of the chamfer always predicted the bottom of the lateral etching region, increasing the etch time for these runs also increased the size and depth of the lateral etch feature. As a direct result of these trials the researchers concluded that the major mechanism in the formation of the undercut was ion scattering from the edge of the mask, the magnitude of the lateral etching effect was not influenced by mask thickness or material. The effect of the two mask edge profiles is illustrated in Figure 10, the black line shows that the lowest extent of the undercut region corresponds with the angle of the mask profile. The red line indicates that the lower regions of the lateral etching is less formed in a mask with a standard edge when all other process parameters are equal [28].

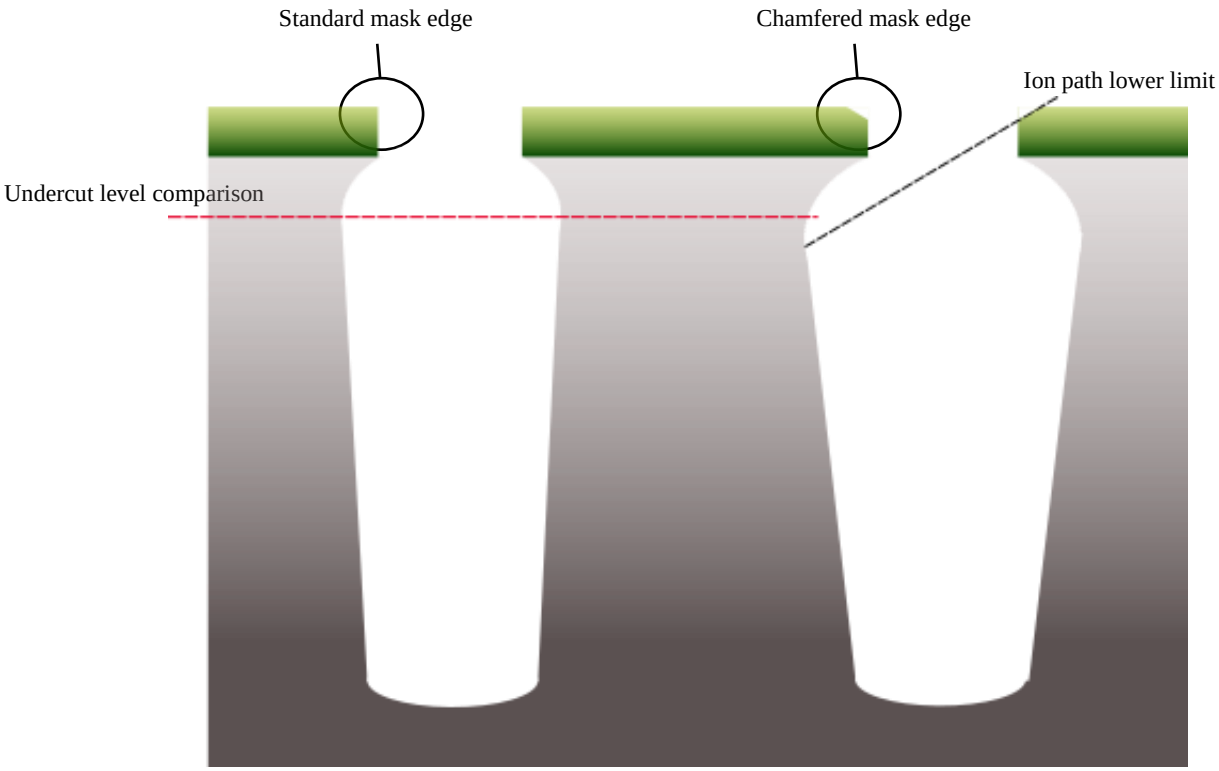


Figure 10: Effect of Mask Profile on Undercut [26]

1.9 Scope of the Research

This programme of research was designed to investigate the relationship between the specific process parameters that are deemed to be the most important factors when creating a positive profile through silicon via, the shape and the across wafer uniformity of the resulting etched features. The scope of the test is limited to the effect that the parameters have on each of the feature variables that are identified as part of the programme, the creation of an ‘ideal’ shape will not be investigated as part of this design of experiments.

Chapter 2 - Methodology

Chapter 2 describes the objectives that this thesis will achieve, the decisions and technology that were required for this research program to progress and covers the hardware and reactor process conditions needed to manufacture a positive profile TSV. In the latter areas of this section, the design of experiments (DoE) conditions and parameters are discussed along with the methods for categorising and analysing the results that would be obtained from the process trials.

2.1 Objectives of the Research

The objective of this research programme was to determine if the shape and across wafer non-uniformity of a positive profile TSV can be manipulated by adjusting the etch process parameters that are used to create these features. These TSV profiles are a relatively new technology with Intel 'Ivy Bridge' CPU being the first major product using these devices brought to market in 2012 [17]. Due to the short period of time since their introduction the manufacturing process used to construct the assemblies has not yet matured to the point where the excess costs have been removed [36].

This project attempted to identify the critical parameters than can be used to adjust the profile of the device that would allow subsequent processing steps to be fine-tuned for faster, more consistent results, which should in turn lower cost of production per die. Once costs lower to the point where high volume production suppliers can enter the marketplace with lower initial setup costs, the availability of the devices will be increased allowing for the devices to be installed into new applications [37].

The process used to research the TSV profile dimensions was to run an experimental series of 17 SPTS type-AT test wafers through an SPTS Pegasus™ deep silicon etching system. The first wafer (run 1) was baseline processed using the conditions detailed in Table 7, the remaining 16 wafers were individually run with the modified process conditions detailed in Table 10 (runs 2 – 17). Each wafer was cleaved using the process detailed in section 2.15 and the resulting samples were measured and photographed using a Carl Zeiss Sigma HV scanning electron microscope (SEM).

When all the results from the process samples were collated, the resulting information was analysed using JMP Statistical Discovery™ regression analysis software. This software will compare all results against each process parameter change and will attempt to identify any predicable patterns. The results of the regression analysis were investigated for any likely etch parameter changes that would allow the researcher to intentionally affect the TSV profile dimension sizes and across wafer non-uniformity.

2.2 Photolithography

Optical (photo) lithography is a photographic process which is commonly used in the fabrication of integrated circuits to facilitate the preferential etching of features in the surface of the substrate [38]. This process step is achieved by shining a light or another form of exposing radiation such as UV or X-rays through a plate known as a photomask onto a light sensitive polymer called a photoresist.

The photoresist material is a polymer that is placed onto the surface of the wafer and is exposed and developed to form a 3D relief image on the substrate. The main role of the polymer is to resist etching during the process step so that the pattern defined by the mask can be transferred into the substrate surface.

The photomask (which is frequently shortened to ‘mask’) is an opaque plate that has transparent sections that are the negative of the desired pattern to be transferred to the substrate. The light source is placed above this mask with the wafer below it. Once the source has been activated, the light passes through the transparent sections in the mask and exposes the photoresist, this causes a chemical reaction in the areas that have been exposed to the light source and a developer material usually tetramethylammonium hydroxide (TMAH) is used to remove the exposed sections of the photoresist [39].

There are two types of photoresists which are used according to the required application, positive resist is soluble in the areas exposed to the light source, negative resist is soluble in the areas that are masked from the light source. Each type has its own benefits and drawbacks [40].

Table 3: Photo Resist Characteristics [40]

Negative resists characteristics: -	Positive resists characteristics: -
+ High sensitivity to developers.	+ Excellent device resolution.
+ Good adhesion to the wafer.	+ Aqueous developers can be used.
+ High plasma etch resistance.	+ Minimal distortion from developers.
+ Lower cost than positive resist.	+ Excellent plasma etch resistance.
- Toxic organic developers are needed	- Poor wafer adhesion
- Image distortion from the organic developers	

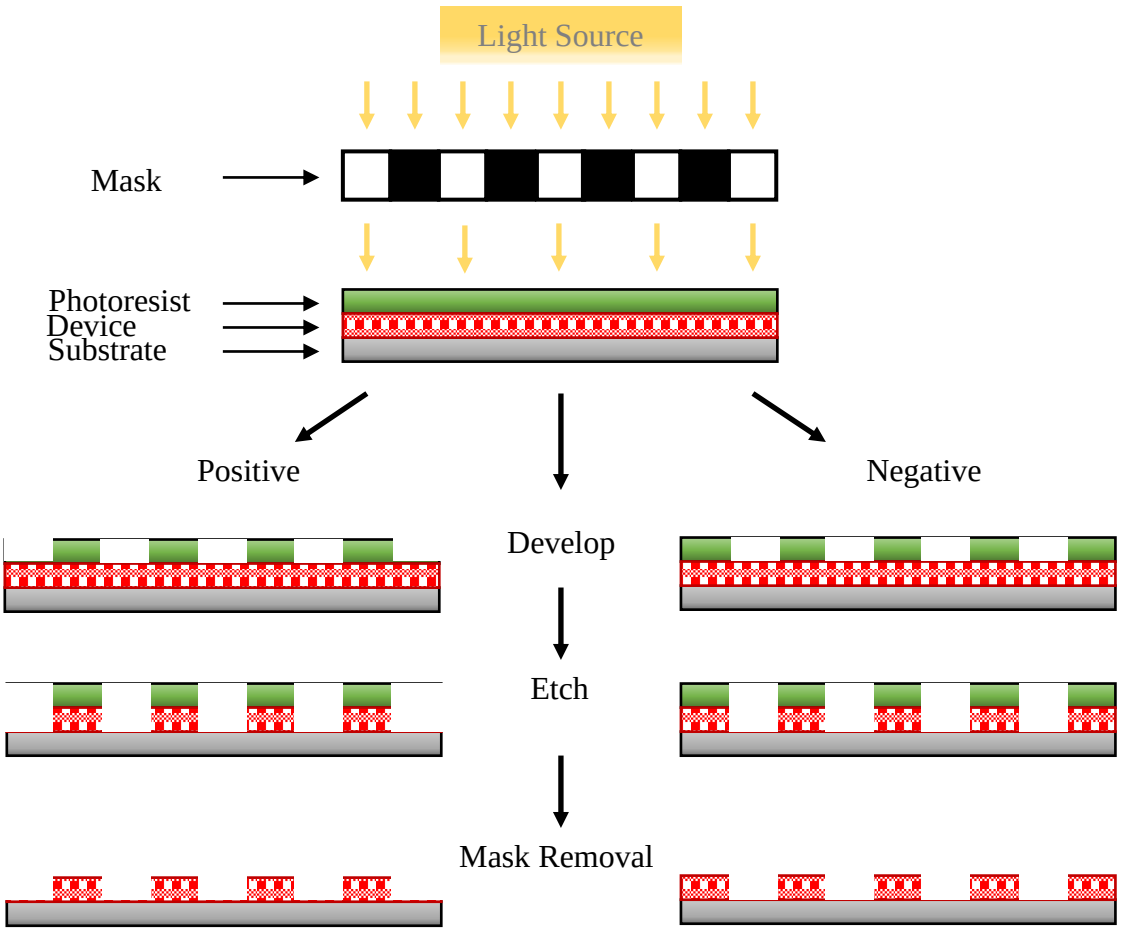


Figure 11: Photolithography Process [39]

2.3 Selection of substrate material and mask pattern

2.3.1 Substrate Material

While there are several materials that can be used as substrates in the semiconductor industry the two most common are silicon (Si) and germanium (Ge). These were selected because they are elemental semiconductors (from group 14 of the periodic table) with diamond like orderly atomic structures and relatively strong atomic bonds, this provides the crystal with strong mechanical properties that are advantageous for mechanical handling and processing [41]. Each material has its own advantages, with germanium having more free electrons over silicon at any temperature within its operating range, and silicon which is by far the most common semiconductor material as it is inexpensive to manufacture and readily available, as it is the second most common material in the earth's crust (by weight) [42]. The native oxide of silicon, is silicon dioxide (SiO_2) which is a hard etch resistant material that grows spontaneously on the surface of the wafer due to plasma oxidation [43], this property is frequently used to stabilise the surface of silicon semiconductors during process conditions. The ability to form SiO_2 on the surface of the wafer is the main reason for silicon to be chosen as the substrate material in this series of experiments as this effect is exploited during the process runs to limit isotropic etching of the TSV sidewalls [44].

2.3.2 Substrate Mask Design

The standard design of test substrates used within SPTS Technologies (SPTS) for trench and TSV etching trials are known as 'Type A' patterned wafers and are coated with a 3µm deep photoresist mask. For the purposes of this test, it was decided to use 'Type AT' wafers (see Figure 12) which have the same mask pattern as a Type A wafers, however they have an 8µm photoresist mask. This allows the etch to be run for a longer duration resulting in a greater profile depth over Type A wafers which permits a more complete formation of the undercut feature.

The mask is transferred onto the surface of the wafer resulting in 145 dies that are each a 10mm × 10mm square, the pattern has a series of holes and trenches that are detailed in Figure 12. Each die has a series of test via patterns that consist of circles 5µm × 9500, 10µm × 5400, 20µm × 1750, 30µm × 765 and 50µm × 549. The trenches in each die consist of 3.7µm × 5 with 1 × 3µm, 5µm, 10µm, 20µm, 30µm and 50µm but these are not used in this programme of work.

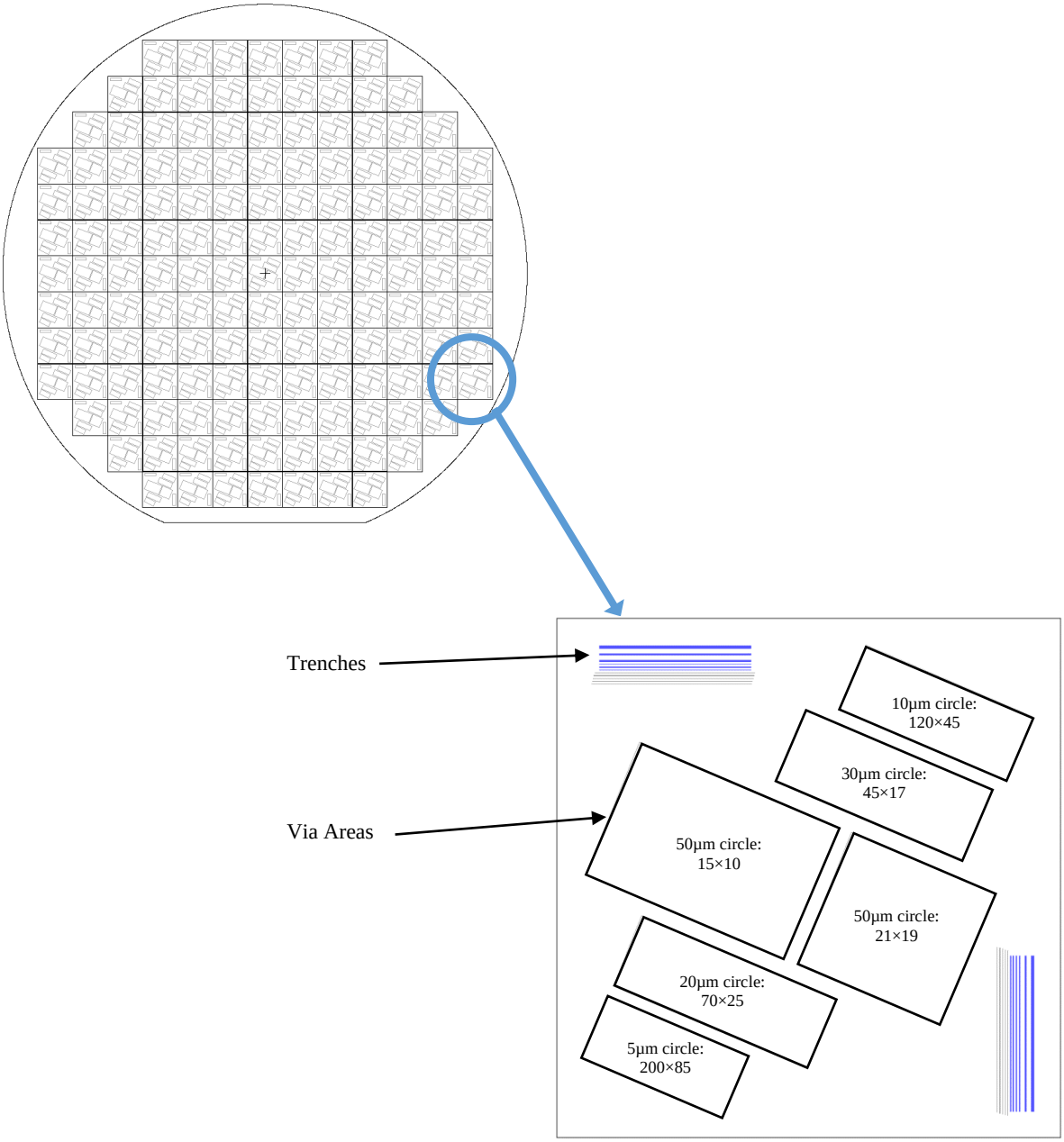


Figure 12: Test Wafer Layout (copied with permission of SPTS Technologies)

2.4 Substrate Etching

In order to generate the formation of a TSV, the substrate material needs to be subjected to a production process that preferentially etches the desired features into the surface of the substrate material. During the etch removal process there are two types of etch profile that can be produced, these are known as isotropic (a profile that is etched in all directions) and anisotropic (a profile that has selectively etched in one direction), the differences between the two are shown in Figure 13 & Figure 14 below [45].

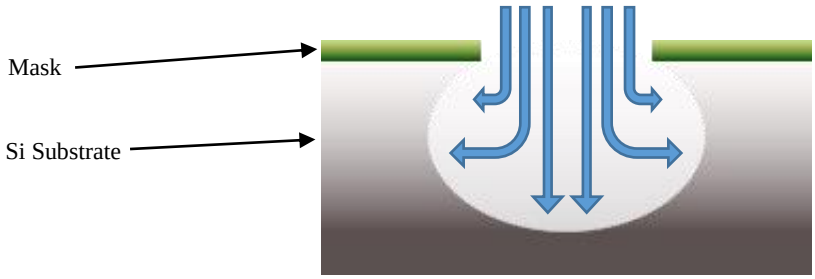


Figure 13: Isotropic Etch Profile [45]

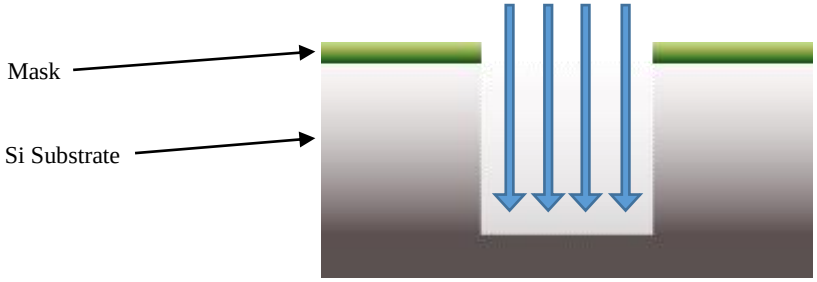


Figure 14: Anisotropic Etch Profile [45]

The majority of etch processes use one of the two process types detailed above, in this programme a combination of the process types will be used as the via will need to increase in width as well as depth in a controlled manner. This mix of the two forms is required to produce the characteristic tapered sidewalls of a positive etch profile [46] as shown in Figure 15.

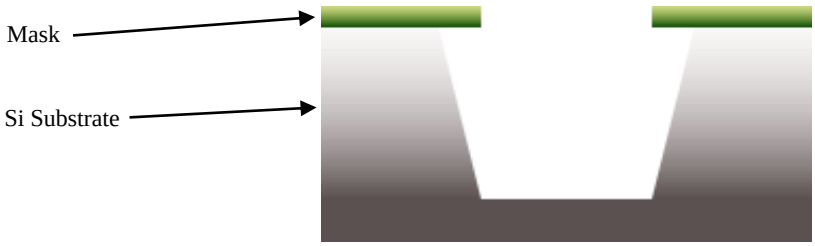


Figure 15: Positive Etch Profile [46]

There are two main methods to etch a desired profile in a silicon substrate and these are known as either chemical wet etching or (dry) plasma etching.

2.4.1 Chemical Wet Etching

Chemical wet etching is a material removal process that uses liquid chemicals to remove material from the surface of the substrate and typically results in an isotropic etch profile [47]. A mask is placed onto the surface of the wafer using photolithography, this mask defines the areas that are not to be removed during the etching process and form a reverse image of the final product.

A wet etch uses liquid chemicals to consume the exposed substrate material, there are normally three steps to an etch process, these are typically: -

1. Diffusion of the liquid etchant into the substrate material.
2. The subsequent reaction between the etching materials and the material that is being targeted, this is normally a reduction/oxidation (redox) reaction.
3. Removal of the reactant material and etch products from the surface of the substrate.

Typical chemicals that are used for these reactions are (1) Sulphuric acid (H_2SO_4), Ammonium Hydroxide (NH_4OH). (2) Hydrogen Peroxide (H_2O_2), Nitric Acid (HNO_3). (3) Water (H_2O), Acetic Acid (CH_3COOH) [48].

2.4.2 Plasma Generation

A plasma is a partially ionised gas that is energetically the fourth state of matter and contains roughly equal amounts of positively charged ions and negatively charged electrons, Figure 16 represents the ranges of temperature (particle energy) in which each of the 4 stages of matter typically occur [49].

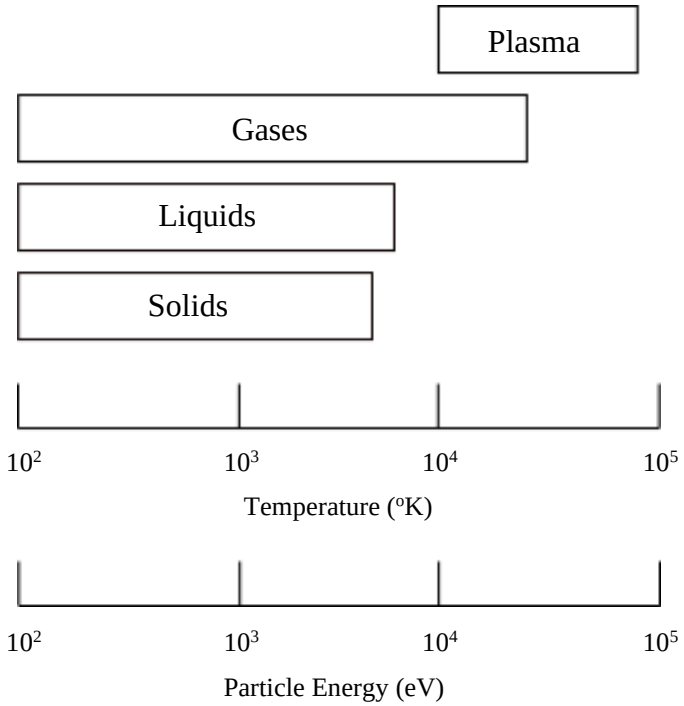


Figure 16: Matter State Vs Temperature [49]

In a typical neutral gas no forces are present between its molecules and they travel with a range of velocities, the movement of the molecules exhibit Brownian motion where the path taken by each molecule is controlled solely by collisions amongst the fast moving atoms and molecules within the gas, and impacts on the walls of the container [50].

2.4.3 Ionisation

A plasma can be defined as a quasi-neutral (similar number of positive and negative charges) gas of charged and neutral particles that exhibit a collective behaviour, in order to create a plasma three important processes will take place which are known as ionisation, excitation-relaxation and dissociation [51].

Free electrons are naturally present in any gas due to natural ionisation, these electrons are accelerated using a rotating magnetic field within a vacuum chamber until enough energy is gained to knock an orbital electron away from a gas molecule creating an ion as illustrated in Figure 17 [52].

[2.1]

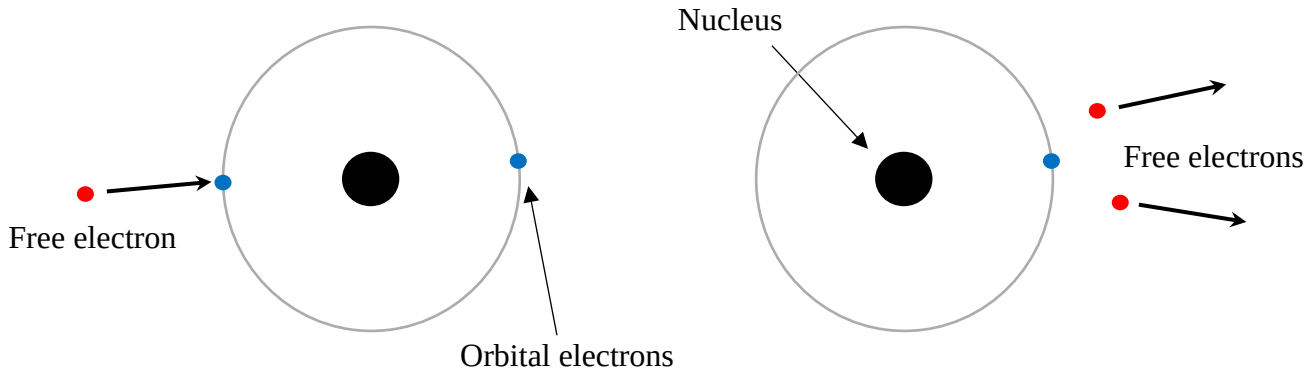


Figure 17: Ionisation of a gas molecule within a plasma reactor

The free electrons formed during the process of ionisation are continually generated and lost within the plasma by a process known as recombination, the plasma enters a stable state once the number of electrons that are lost is equal to the numbers that are being created.

2.4.4 Excitation – Relaxation

When fully formed the plasma will glow with a particular colour that is directly related to the gas molecules that are present in the reactor, for example argon (Ar) will glow light purple, xenon (Xe) will glow blue, nitrogen (N_2) will glow pink. The colour or 'glow discharge' is caused by an excitation-relaxation reaction and is emitted when a free electron strikes a gas molecule with insufficient energy to cause ionisation, but with enough energy to raise the molecule to an excited state quantum state, this is known as the Franck-Hertz effect and is illustrated in Figure 18 [53].

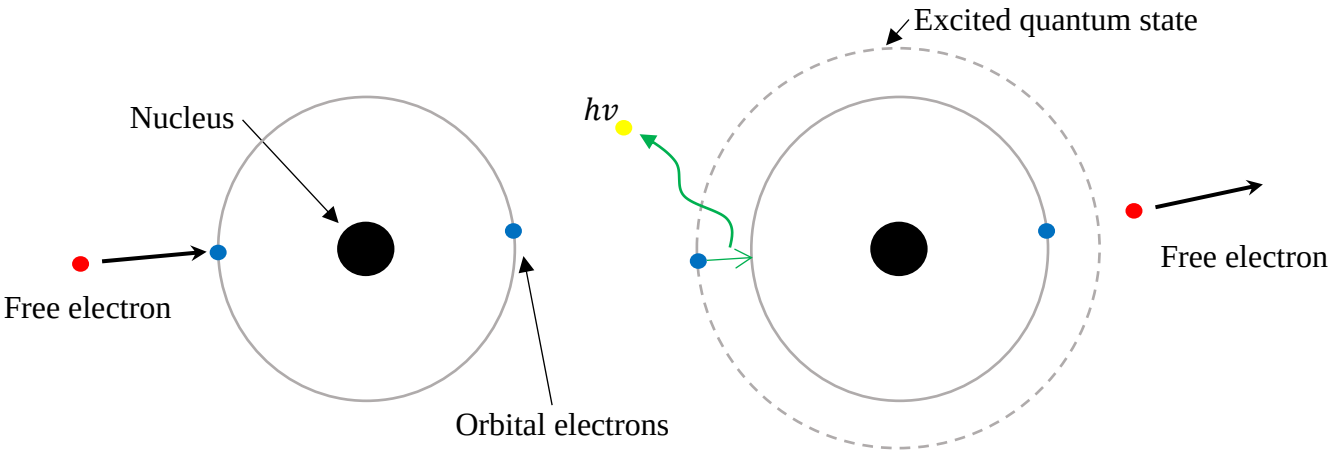


Figure 18: Excitation-relaxation photon emission

As the molecule spontaneously relaxes back to a ground state the excess energy is released as a photon whose frequency will give the plasma its colour, the amount of energy released can be expressed by equation 2.1

$$E = hv \qquad [2.1]$$

Where E (J) is the energy of the electron, h (J·s) is Planck's constant (6.62606957 $x10^{-34}$), v (Hz) is the frequency of the photon [54].

2.4.5 Dissociation

A further process that occurs within the plasma is the production of free radicals which are molecular fragments with unpaired electrons and are highly reactive in an etch environment. The free radicals are created in a plasma reactor by a method known as dissociation by electron impact, where a free electron hits a molecule and breaks the molecular bonds holding the atoms together resulting in the formation of free radicals that can be expressed in equation 2.2 and is shown in Figure 19 [46].

$$AB + e \longrightarrow A^* + B + e \qquad [2.2]$$

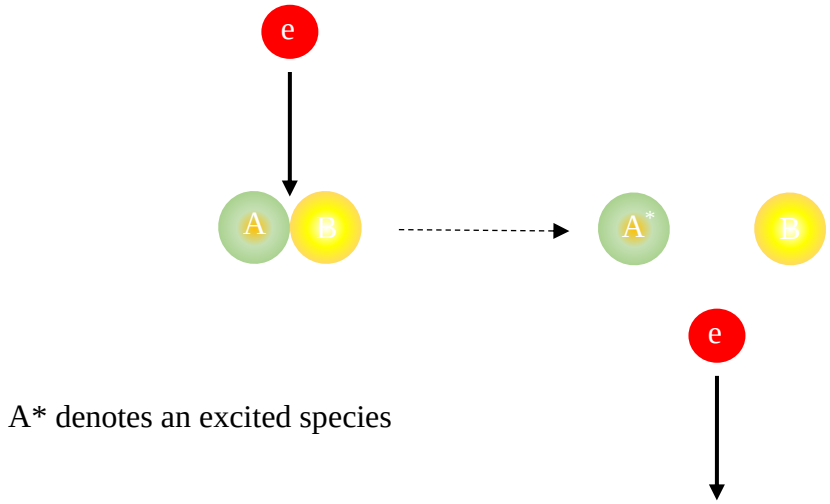


Figure 19: Dissociation by electron impact

Fluorine free radicals are chemically very reactive and will spontaneously etch silicon on contact through a process of adsorption of radicals, chemical reaction with the substrate and desorption of the waste reaction products [55]. The resulting etch profile produced using only radicals will be isotropic in nature and will have no directionality, this process will provide the bulk of the material removal with the ions producing the profile fine tuning (anisotropic part of the etch).

The gas used to produce the etch profiles in this DoE was sulphur hexafluoride (SF_6) which is widely employed as an etchant because it is a highly reactive at low temperatures, with fast etch rates

that do not damage the surface of the substrate undesirably [56]. SF_6 will readily dissociate in the plasma by the mechanisms illustrated in Table 4 [57].

Table 4: SF_6 Dissociation mechanism

SF_6+e	$\longrightarrow$	SF_5+F+e
SF_6+e	$\longrightarrow$	SF_4+2F+e
SF_6+e	$\longrightarrow$	SF_4+F_2+e
SF_6+e	$\longrightarrow$	SF_3+3F+e
SF_6+e	$\longrightarrow$	SF_3+F+F_2+e
SF_6+e	$\longrightarrow$	SF_2+4F+e
SF_6+e	$\longrightarrow$	SF_2+2F+F_2+e
SF_6+e	$\longrightarrow$	SF_2+2F_2+e
SF_6+e	$\longrightarrow$	$SF+5F+e$
SF_6+e	$\longrightarrow$	$SF+3F+F_2+e$
SF_6+e	$\longrightarrow$	$SF+F+2F_2+e$

2.5 Dry Plasma Etching

Plasma etching is achieved using surface chemistry that mainly consists of 3 steps:

1. Adsorption of radicals from the reactor environment.
2. The reaction between the silicon and fluorine.
3. Subsequent desorption of reaction products.

This reaction typically results in an anisotropic etch profile [55] and is achieved by creating a stable plasma inside a vacuum chamber between a pair of metal plates referred to as an anode (+) and cathode (-). Reactive gas and radio frequency (RF) energy are injected into the vacuum chamber producing a gas glow discharge to generate the reactive species that are needed to facilitate the removal of the surface of the substrate that is exposed by open areas in the mask.

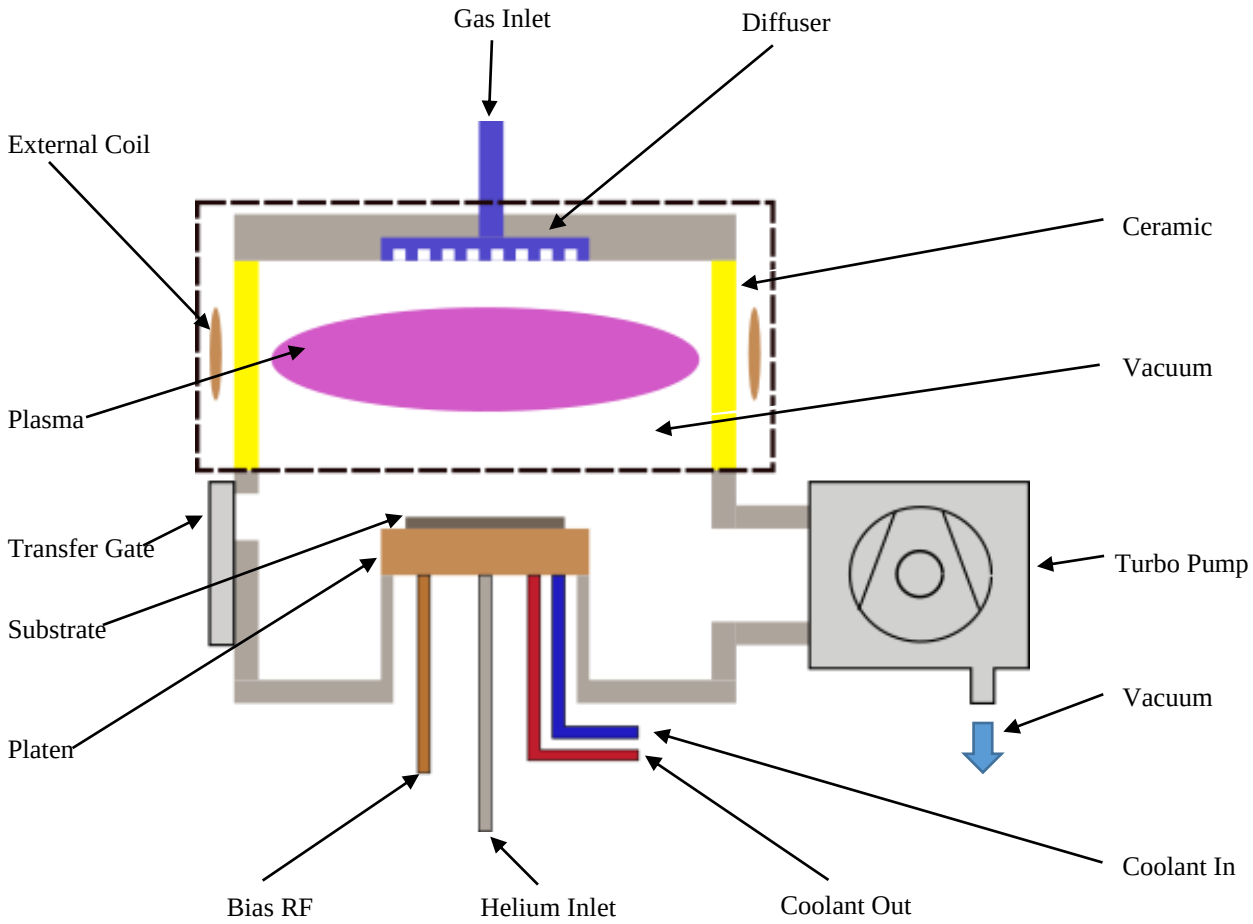


Figure 20: Typical SPTS Plasma Etch ICP System

The type of plasma etching chamber shown in Figure 20 is known as an inductively coupled plasma (ICP) reactor and it is of the type that will be utilised for this project.

Reactive gas is injected into the vacuum pressure vessel via the top cover of the source and passes through a diffuser which is designed to give a conformal spread of the gas into the chamber. An external coil is mounted around the outside of the ceramic pressure vessel to which RF power is applied at a frequency of 13.56 MHz which is the Federal Communications Commission (FCC) standard allocated frequency for Industrial, Scientific and Medical (ISM) equipment [58]. The RF power circulates around the coil which in turn causes a magnetic field to be generated that permeates the ceramic wall resulting in a plasma being formed inside the pressure vessel.

An ICP reactor causes a plasma to be formed inside the pressure vessel which consists of high levels of etch reactive species and charged particles. Variations in the coil RF power have a direct effect on the plasma density, with the ion energy being independently controlled via voltage bias control of the substrate. This bias control is made possible as the substrate is placed onto a platform (platen) that is driven by an independent RF power supply, the bias generator places either low frequency (380 KHz) [58] or high frequency (13.56 MHz) RF power onto the platen at a negative polarity. This attracts and accelerates the positively charged free ions present in the plasma towards the substrate, thus performing the physical part of the edge that leads to an anisotropic etch profile.

The wafer is held in place by a bi-polar electrostatic chuck (ESC), an assembly that uses two separate, biased metal plates that have opposing charges with a variable 6Kv to 12Kv potential difference, this establishes an electrostatic charge between the two plates that clamps the substrate tightly (chucking) onto the surface of the ESC as long as the voltage is maintained [59]. The substrate is kept at the processing temperature by combining two methods of cooling, the first being a chilled, non-conductive fluid flowing through the ESC to maintain a constant temperature, and the second component being helium gas (at a pressure between 6 and 20Torr) that is fed into the area between the

surface of the Esc and the chuck to act as a heat transfer mechanism that quickly conducts heat from the surface of the substrate into the cooling fluid flowing within the platen body. Without this cooling facility the substrate surface would rapidly overheat due to ion bombardment and plasma temperature, resulting in permanent device damage or destroying any mask that is present on the wafer.

The degree of anisotropy during the etch process depends on the specific plasma/material interactions that are occurring within the process chamber, as explained earlier in this section the etching process consists of three steps, adsorption, reaction, and desorption of the reaction products. If these three effects alone are present in the process, etching will occur spontaneously but the etch profile will be isotropic, in order to change the etch profile to anisotropic the etch step can be assisted by ion impact driven by the level of bias RF introduced into the vacuum chamber [55].

In an ICP reactor a typical etch gas used to etch Si is sulphur hexafluoride (SF_6), this is introduced into the chamber and is subjected to the magnetic fields that ignite the plasma. Ultimately a free electron strikes an SF_6 molecule which removes an electron and a fluorine (F) atom resulting in an SF_6 ion, a fluorine free radical (F*) and a free electron. The free electron that is released by this exchange is accelerated by the magnetic fields inducing the plasma and continues the chain reaction that is occurring within the process chamber. The SF_6 ion (see Table 4) [60] is now positively charged and the negative bias voltage is used to accelerate the ion into the surface of the substrate to produce the anisotropic trench profile. The fluorine free radical released is highly reactive and will freely react with the substrate surface but will only produce an isotropic trench profile [55]. Using the combined effects from both types of etching that occur on the surface of the substrate it is possible to achieve the positive etch profile taper that is required for this programme of work, the mechanisms involved in this process can be seen in Figure 21.

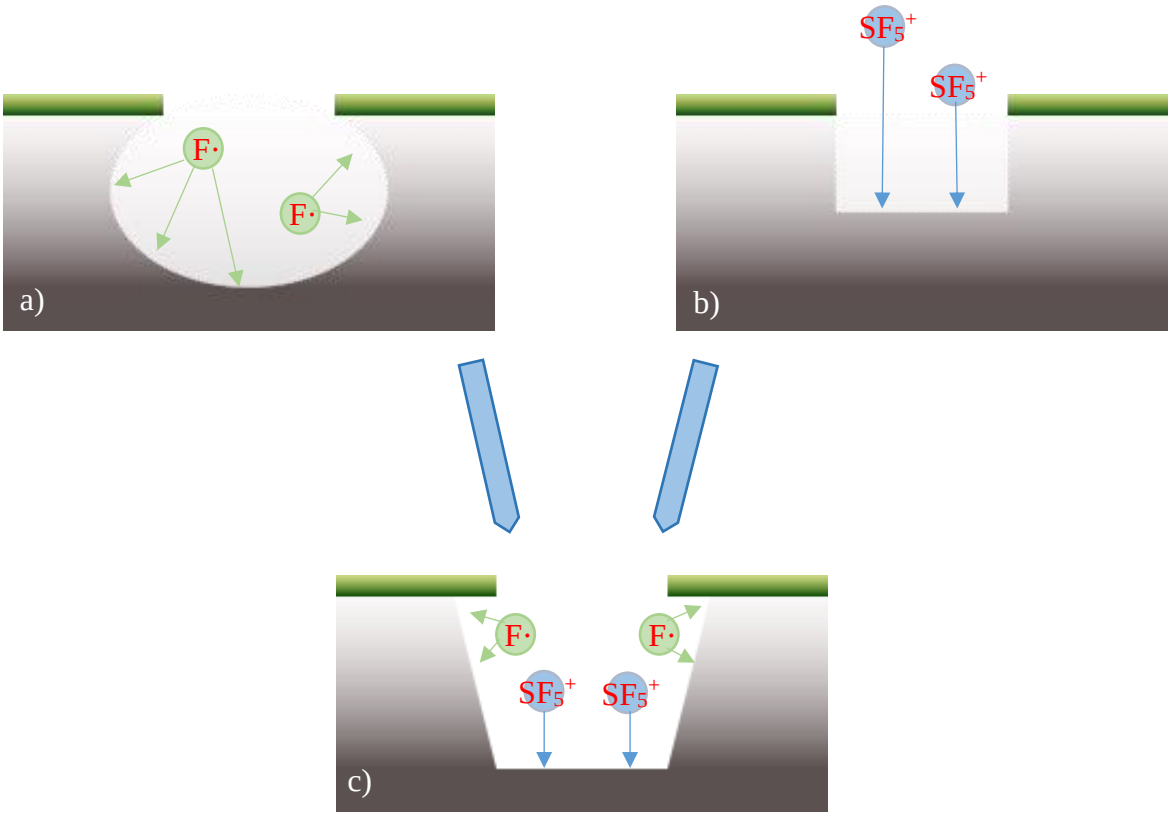


Figure 21: Etching Types and the Resulting Profiles (a) Chemical etching by fluorine radicals, (b) Physical etching by SF_6 ions, (c) Positive profile resulting from combined etching [46]

2.5.1 Edge Loading

Edge loading or ‘macro loading’ as it’s sometimes described, is a wafer level loading effect where the etching ability of the chamber environment is enhanced by a lack of substrate material over a local area. An area near the centre of a substrate will have material fully surrounding it and as a result the reactive species (ions and radicals) are evenly spread across the surface of the material. At the edge of the substrate, it will have material to the inside of the edge but no material to the outside, the result of this is that the ions being attracted downwards will hit the substrate but will pass without effect outside of the substrate area. The radicals that are not driven by the bias power, will etch the surface of the substrate as they contact it. Beyond its edge they are still present in the environment and will act

as a reservoir to top up the radicals being consumed during the process, locally increasing the etch rate of the TSV's around the edge [61].

2.5.2 Wet and Dry Etching Comparison

The decision for which method to use for the etching of silicon is entirely dependent on the desired result of the production process as each technique has its own strengths and weaknesses. Wet etching has much less expensive and simpler process equipment that is comparatively easy to scale to industrial levels. It produces a very high etch rate and has good material selectivity, but it does have the drawbacks that the etch process and device profile are difficult to control as the etch always produces the classic isotropic 'strawberry' shape. The chemicals used to produce the etch are toxic, expensive, and needed in large quantities, for many wet etching manufacturing tasks the treatment and disposal costs of process effluent often surpasses the manufacturing costs, increasing restrictions on waste disposal and landfill are leading to process improvements that reduce the environmental toll that can result from wet etch processes [62].

Dry etching, by comparison can control the etch depth and shape to a very high degree of accuracy and can produce small delicate structures. Any toxic or hazardous by-products of the etch process can be removed by a cleaning process within the same process chamber and surface conditioning can be used to prevent corrosion of the substrate when exposed to air [63]. Dry etching has significant financial drawbacks over wet etching as the equipment is expensive to purchase and requires trained, experienced technicians to ensure that the systems remain operational. Scaling up to industrial levels requires a large capital investment which can be out of reach for smaller manufacturers.

When choosing a manufacturing method consideration should be given to the above factors, in addition to: -

- The numbers of devices to be manufactured.
- Do the devices have small delicate features?
- What tolerances are adequate for the requirements of the product.
- The amount of capital available to purchase or modify existing equipment.
- Cost of ownership of the etch equipment.

For the purposes of this project the only real option was dry plasma etching as the required device profile control needed for both depth and sidewall angle to achieve the desired results is relatively simple to attain. Similar results would be difficult to achieve with wet etching as the etch rates are normally far too slow for production applications and precise alignment to the substrate crystal plane is needed to ensure that the correct profile shape and depth are achieved [64].

2.6 Scanning Electron Microscope (SEM)

The TSV features that were produced during this research project are too small to be seen with the naked eye, as a result of this some form of microscope was required to view and measure the etched profiles. The most common type of microscope available is an optical microscope which uses visible light to view a sample through a series of lenses, unfortunately this type of device is limited to profiles larger than 25µm as this is its lower resolution limit [65]. The TSV profiles produced for this project are often smaller than the lower limit of an optical microscope so another method to view and measure the device dimensions was found.

A less common microscope that is frequently used in semiconductor applications is the scanning electron microscope (SEM), this type of device has a lower resolution limit of around 0.2nm and can focus on more than one part of a feature at the same time, this allows the microscope to produce 3D images of the sample, although the resulting image is a digital reconstruction rather than the direct image that an optical microscope produces [66].

The TSV feature dimensions that produced using the process conditions detailed in Table 6 are frequently smaller than 5µm, as a result it was decided that a SEM was a more appropriate measuring device for use in this project.

A scanning electron microscope produces images by focussing an electron beam onto the surface of a sample and scanning it back and forth along the entire area that is being viewed. A set of detectors measure the signals that are being reflected from the sample and a digital image is reconstructed from the reflected signals, Figure 22 shows a block diagram of a typical SEM.

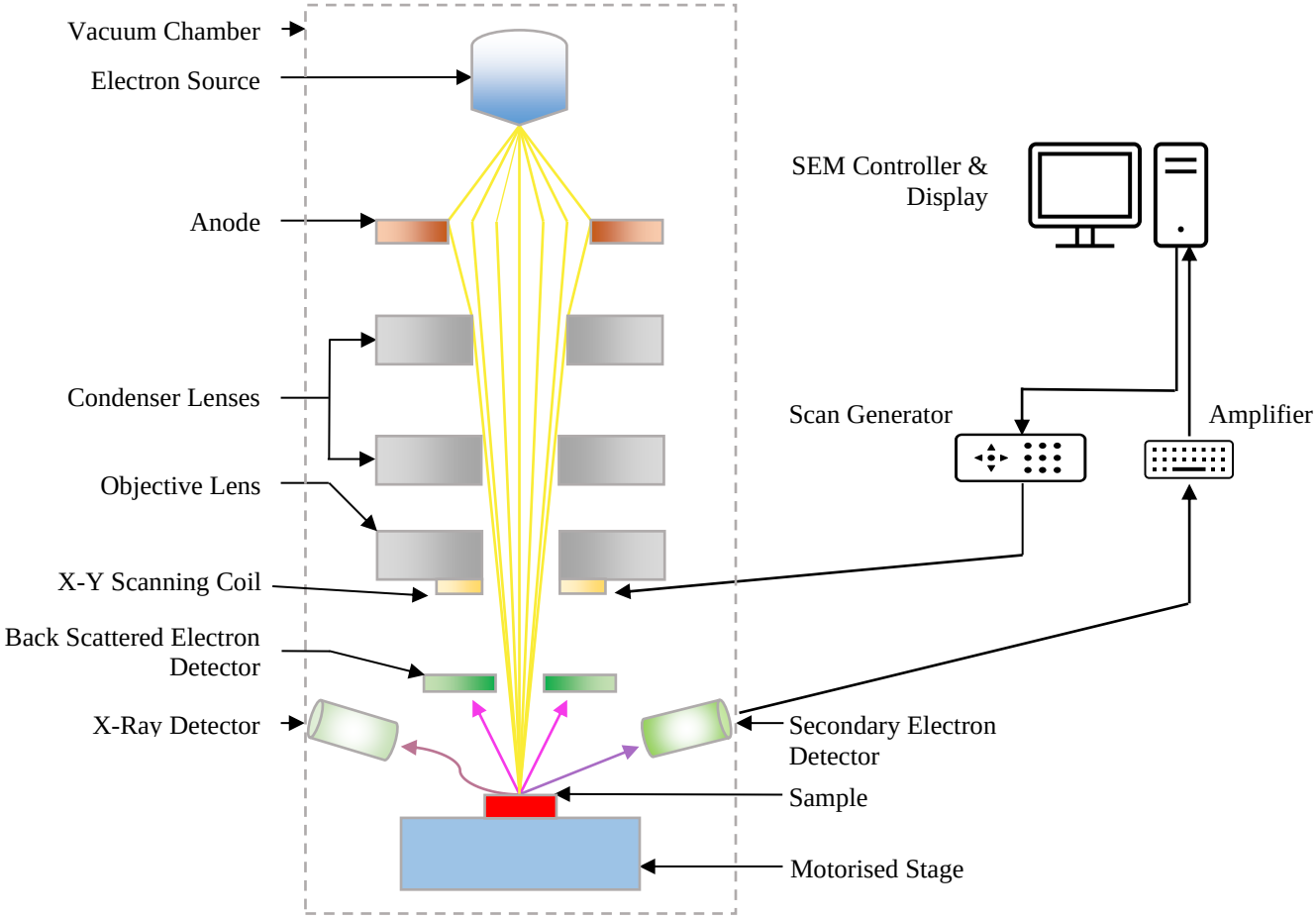


Figure 22 Scanning Electron Microscope Block Diagram

2.6.1 Vacuum Chamber

The internal components within the SEM (shown surrounded by a dashed box in Figure 22) are all contained within a high vacuum environment that prevents the electron beam from discharging 'arcing' to any of the internal components which would prevent the coherent beam from reaching the sample, the vacuum has the additional effects of removing any atmospheric contaminants from the environment which may deposit unwanted material onto the internal components or the sample thus lowering the quality of the resulting image [67] .

2.6.2 Electron Source

The electron gun is the source of the electron beam that illuminates the sample and is normally a thermionic emission gun (TE), electrons are produced by a heated tungsten (W) filament around 0.1mm diameter (cathode) that is held at a temperature of ~2800k [68].

2.6.3 Anode

The electrons produced by the source are roughly focussed by a negatively charged electrode (Wehnelt electrode) that is placed below the cathode, the electrons passing this electrode are gathered by an anode ring that has a positive voltage applied to it (between 1 and 30kV), this causes a beam to form that is ejected through a hole in the bottom of the assembly [68].

2.6.4 Condenser Lenses

As the beam exits the anode ring it passes through the condenser lens assembly, this adjusts the diameter of the electron beam which will allow the operator to adjust the final resolution and depth of field of the image [67].

2.6.5 Objective Lens

The objective lens is used to focus the beam into a fine point at the surface of the sample this allows a clear image to be produced by the microscope [67].

2.6.6 X-Y Scanning Coil

The X-Y coil takes a signal from the scanning generator which causes the beam to ‘raster’ across the surface of the specimen from left to right, top to bottom (like the action of a cathode ray tube) and synchronises with the picture displayed on the microscope screen. This action is used to adjust the magnification of the image, to increase magnification the beam is made to scan over a smaller section of the sample [68].

2.6.7 Motorised Stage

The motorised stage holds the sample that is to be viewed in a metal clamp that prevents any independent movement of the sample, the stage can be moved by the operator in the X, Y and Z axes which allows the operator to select the required area of view.

2.6.8 Backscattered Electron Detector

This component detects the high energy electrons that are deflected back in the direction of the beam, as a rule of thumb the number of backscattered electrons increases along with the atomic weight of the material being observed, the pattern of the electrons being observed by the backscattering detector is used to display compositional differences in the material [67].

2.6.9 Secondary Electron Detector

When the electron beam contacts the specimen, secondary electrons are produced from the emissions of valence electrons from the component material, these electrons have very low energy and only those emitted at the surface can be detected. The brightness of the electrons being produced is larger when the beam hits at an oblique angle and as a result these electrons are used to display the surface topography of the sample. The released electrons strike the secondary electron detector which emits a photon into a photomultiplier tube for each electron impact detected, this photon signal is converted to an electrical signal and passed through a pre-amplifier and an amplifier to increase signal strength, with this signal being subsequently projected onto the viewing screen, each point of light on the screen is a 1:1 ratio for each secondary photon detected [67].

2.6.10 X-Ray Detector

When the electron beam interacts with the specimen material, an inner shell electron can be ejected which causes the atom to be ionised, an electron subsequently moves from the outer shell to stabilise the electron, as this electron is at a higher energy level than the lower shell the atom needs

to shed an amount of energy equal to the total gained. This extra energy is released as an x-ray which is captured by the x-ray detector, as each atom fills the electron gap in a particular way the emitted x-ray will be at a frequency that relates to the individual material. As each element will produce a distinctive series of peaks, the signal can be used by the x-ray detector to identify the elements within the surface material of the sample [69].

2.7 Measurement Techniques Employed to Characterise the Etch Performance

2.7.1 Selectivity

The depth of a given etch can be controlled accurately using the running time of the process and the measured etch rate. However, the process must continue through to the required depth without the total removal of the photo resistive material of the masking layer, if this layer is eliminated there is likely to be an undesired change to the undercut dimensions. To determine the selectivity of an etch process, the mask thickness of the test wafer is measured before the etch process using a surface scan measurement system such as the KLA TENCOR® P10, and after the etch process using a scanning electron microscope (SEM). Selectivity can be calculated as shown in equation 2.3 assuming that all units are the same.

$$\text{Selectivity} = \frac{\text{Etch Depth}}{(\text{Pre Etch Mask Thickness- Post Etch Mask Thickness})} \quad [2.3]$$

Alternatively, the selectivity can also be expressed by equation 2.4

$$\text{Selectivity} = \frac{\text{Si Etch Rate}}{\text{Mask Etch Rate}} \quad [2.4]$$

Average selectivity can be calculated as shown in equation 2.5

$$\text{Average Selectivity} = \frac{\text{Average Etch Depth}}{(\text{Pre Etch Mask Thickness- Average Post Etch Mask Thickness})} \quad [2.5]$$

2.7.2 Etch Rate

The etch rate is a measure of the amount of material that can be removed in a measured period of time, it is a critical parameter as the running time for the etch process will determine the final profile of the structure. If the etch rate is not calculated correctly then the trench will be either ‘under etched’

and the undercut will not be fully formed, or the trench will be ‘over etched’, and the undercut profile will be larger than estimated which will affect the conclusions that can be drawn from the process run. The removed material was measured using a SEM and the resulting depth value is divided by the process time. The etch rate can be is calculated as given in equation 2.6.

$$\text{Etch Rate} = \frac{\text{Etch Depth}}{\text{Process Time in Minutes}} \qquad [2.6]$$

2.7.3 Etch Profile

An etch profile can be defined as change in the trench width as a function of etch depth and is noted as an angular value. This is an important parameter which ultimately defines the shape of the structure, the profile can be defined positive, negative, or vertical:

2.7.4 Positive Profile (+)

A positive profile is one that is defined as a feature that has its top width (TW) greater than its bottom width (BW). It is recorded as an angle, and its definition is presented in equation 2.7 and is illustrated in Figure 23.

$$\text{Positive Profile} = < 90° \ (\text{BW} < \text{TW}) \qquad [2.7]$$

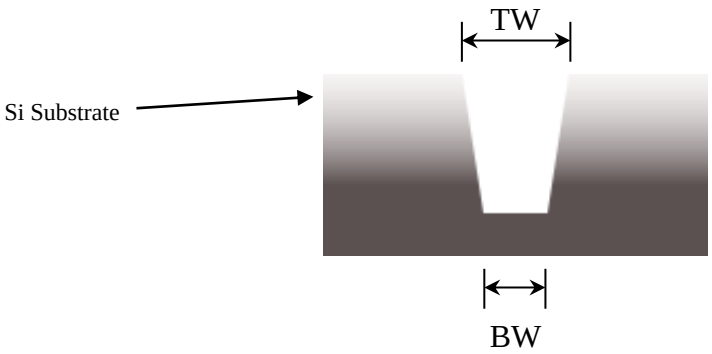


Figure 23: Positive Profile Measurement [25]

2.7.5 Negative Profile (-)

A negative profile, which is often referred to as re-entrant, is one that is defined as a feature that has its top width (TW) less than its bottom width (BW). It is recorded as an angle and its definition is presented in equation 2.8. and illustrated in Figure 24.

$$\text{Negative Profile} = > 90° \ (\text{BW} > \text{TW}) \qquad [2.8]$$

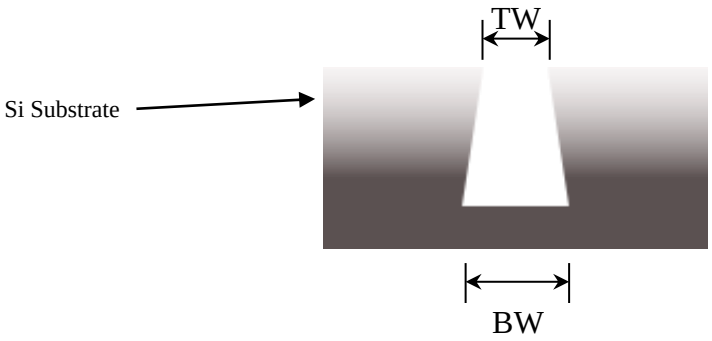


Figure 24: Negative Profile Measurement [25]

2.7.6 Vertical Profile

A vertical profile is one that is defined as a feature that has its top width (TW) equal to its bottom width (BW). It is recorded as an angle and its definition is presented in equation 2.9 and is illustrated in Figure 25.

$$\text{Vertical Profile} = 90° \ (\text{BW} = \text{TW}) \qquad [2.9]$$

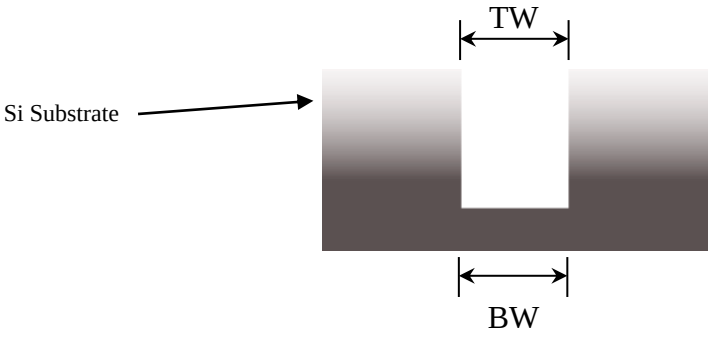


Figure 25: Vertical Profile Measurement [25]

The feature shape that is being investigated for this project is the positive etch profile, the ultimate angle of the sidewalls is not relevant for this series of experiments, but the top width must be greater than the bottom width and should be greater than or equal to the max width dimensions.

2.7.7 Etch Rate Non-Uniformity

Etch rate non-uniformity is defined as the uniformity of the etch depth across a substrate and is normally measured in the centre and edge locations, with the result being depicted as a percentage value as calculated in equation 2.10.

Non-uniformity is one of the most important parameters when manufacturing semiconductor devices as it has direct effect on production yield, the more uniform the devices are across the wafer the more successful any follow-on process are likely to be.

$$\text{Uniformity } (\pm\%) = \frac{(\text{Max Depth} - \text{Min Depth})}{(2 * \text{Average Depth})}\, x100 \qquad [2.10]$$

2.7.8 Tilt

Tilt is a measure of the direction of the etched profile from the vertical and is normally expressed as an angle as calculated in equation 2.11. The resulting angle is given as either a positive or negative symbol which indicates its direction with respect to the edge of the wafer, a device with a negative tilt is pointed inwards towards the centre of the substrate.

$$\theta = (\theta_1 - \theta_2)/2 \qquad [2.11]$$

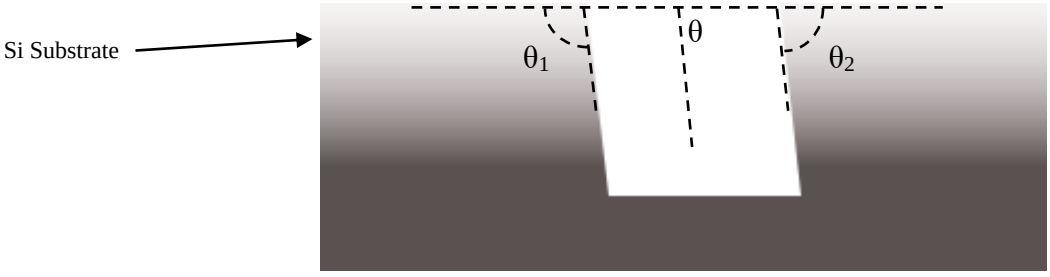


Figure 26: Profile Tilt Measurement

The tilt of an etch profile is usually measured using a SEM, when performing this measurement, the operator needs to align the sample that is being measured parallel to the viewing axis with the image working distance being held the same for all measurements. The resulting angle can only be used as a comparative measurement as SEM imaging can tilt a straight trench through image distortion, to minimise the distortion effect great care must be taken on sample alignment, especially when working with small features [70]. For a positive profile etch process tilt is not usually an aspect that needs to be considered, although it is possible that etched features can tilt outwards as you near the edges of the substrate if the process has not been fully tuned to the wafer size.

2.8 Etch Hardware

The ICP reactor used in this programme is the STS Pegasus (Plasma Etch Giving Advanced Speed Uniformity and Selectivity) deep silicon etcher (see Figure 27). This is an advanced ICP (Inductively Coupled Plasma) source, which has a novel 'annular' source design in which the plasma is generated and subsequently radiates into the larger main diffusion chamber where the substrate is located. The main benefits of this source design are: -

1. The dual coil plasma generation area allows the process module to couple more RF power into the plasma over a single coil ICP chamber for any given RF power level.
2. The plasma source can produce a neutral radical profile in the centre of the wafer that matches the loading effect and generates good uniformity up to a 200mm diameter wafer.
3. The source can generate a near uniform ion density profile as can be seen in Figure 28, and sheath thickness that greatly reduces feature tilting towards the edge of the wafer.

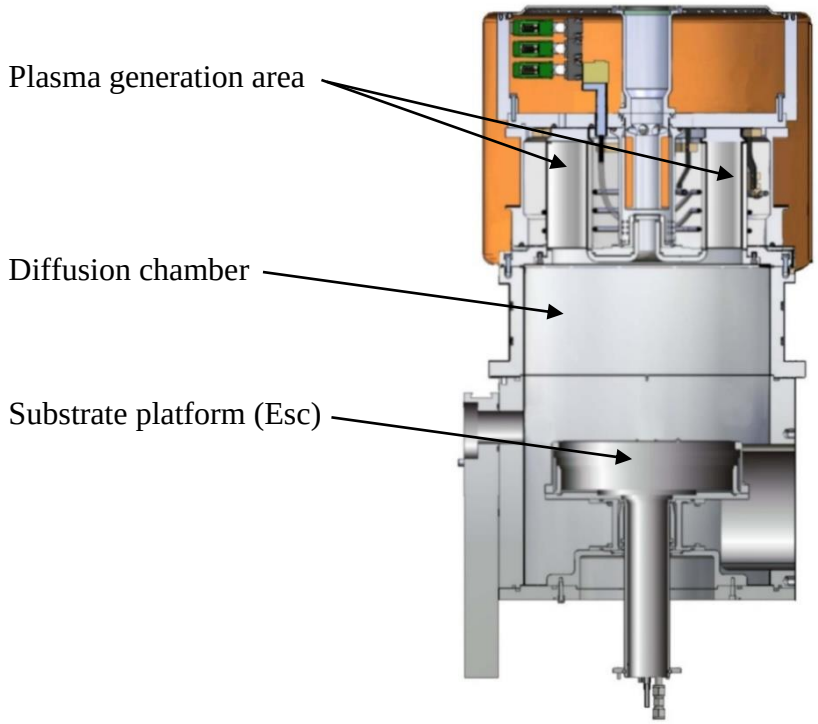


Figure 27: An SPTS Pegasus System® (copied with permission of SPTS Technologies)

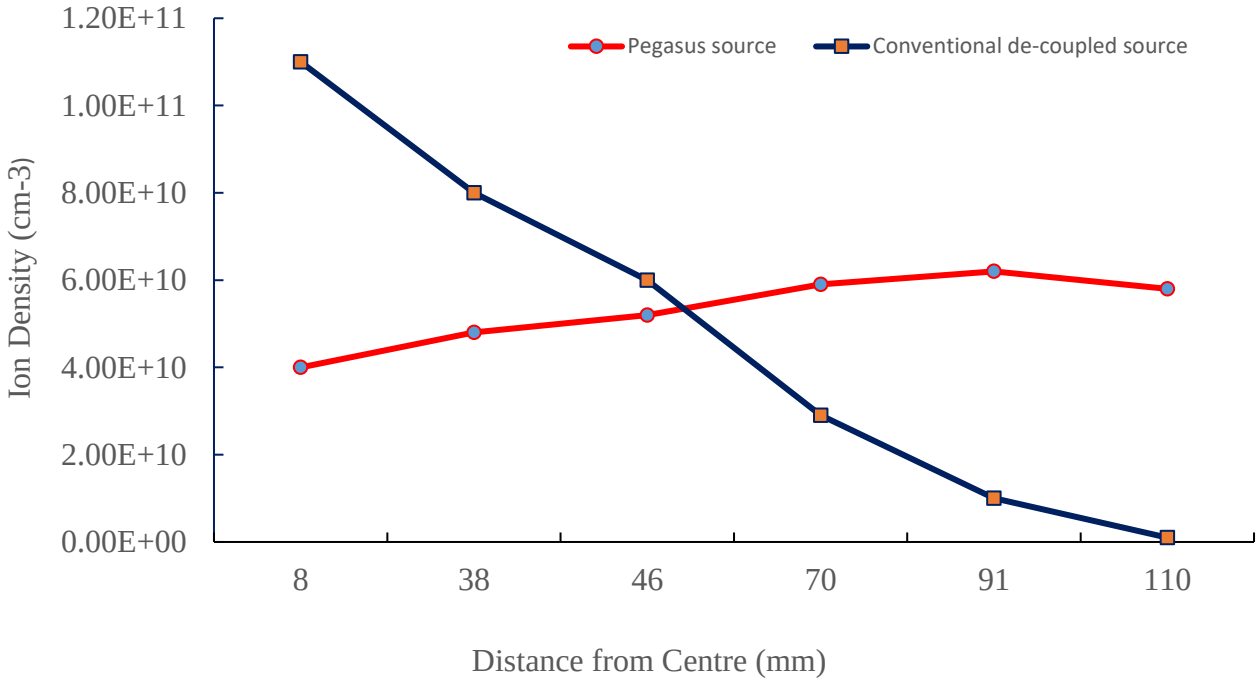


Figure 28: SPTS Pegasus Plasma Uniformity (reproduced with permission of SPTS Technologies)

The SPTS Pegasus has an interchangeable funnel/baffle system that assists the directionality of the ions towards the substrate and can be used to tune the tilt direction of the etched features across the wafer. The major performance milestones for the Pegasus system are: -

1. 50µm/min etch rate for silicon demonstrated in a development lab (1% exposed Area).
2. Etch uniformity of < 1-2% regularly achieved for 200mm diameter wafers.
3. Selectivity > 300:1 achievable for Photoresist masks.
4. Demonstrated side wall defects of less than 20nm.
5. Reduced feature tilting at all positions across the surface of the substrate.

Typical applications for DRIE etching are very wide and varied and are often used to manufacture devices that require smooth high aspect sidewalls with minimal notching at the base of the feature. Devices can include surface-micromachined gyroscope for car navigation and roll over protection, microphones and cavity etches, through silicon via and plasma dicing applications [71].

Advances in DRIE technology are allowing equipment manufacturers to continually improve manufacturing methods allowing for an ever-increasing portfolio of devices that can be manufactured using this type of equipment.

2.9 Etch Process Steps

2.9.1 Chamber Cleaning

Before the design of experiment runs can be initiated, the process reactor needs to be conditioned into a seasoned state where it is free from contaminants and has the correct chamber sidewall properties to successfully run the process repeatedly. The first of these steps is to run a 30-minute oxygen (O_2) clean to remove any biological contamination and clean the internal surfaces of the etch chamber that are wetted by the plasma, see Table 5 for the O_2 clean process conditions.

Table 5: O_2 Clean Parameters

Recipe Setting	Parameter Value
Process Time	30’00”
Process Pressure	20 mTorr
O_2	200 sccm
Coil Power	2.5 kW
Platen Power	100 W (13.56 MHz)
Platen Temperature	20^{o}C
Helium Backside Pressure	10 Torr

2.9.2 Chamber Conditioning

After completion of the O_2 clean step the etch reactor will need to be conditioned with an SPTS standard, switched step fluorine (F) based process (see Table 6 for the recipe conditions). The purpose of the conditioning process is to deposit a fluorine-based polymer onto the surface of the chamber walls to act as a barrier to prevent the aluminium faces of the chamber block absorbing free fluorine during the etch process. The absorption of the free fluorine is undesirable as it will reduce the fluorine available to the plasma to produce ions and the free radicals that are required for the etch effects to

occur, this would ultimately cause unpredictable changes to the process conditions which will affect the results of the etched profiles [72].

Table 6: Conditioning Run Parameters

Recipe Setting	Parameter Value
Process Time	9’54”
Process Pressure (etch)	100 mTorr
Process Pressure (dep)	25 mTorr
SF_6	450 sccm
O_2	45 sccm
C_4F_8 (dep)	200 sccm
Coil Power (etch)	2.8 kW
Coil Power (dep)	2 kW
Platen Power	40 W (13.56 MHz)
Platen Temperature	20 ^oC
Helium Backside Pressure	10 Torr

2.9.3 Inter Wafer Cleaning

Between each substrate an inter-wafer clean process is performed inside the etch chamber, this is a three-minute process that has the same parameters as the O_2 clean used in Table 5, but with the absence of a wafer on the electrostatic clamp and the helium backside pressure set to zero. The purpose of this clean is ensure that the chamber conditioning stays consistent throughout the duration of the DoE, without the addition of this step the chamber would become progressively dirtier after each process and the etch profile results would change between substrates. The inter-wafer process additionally acts to ensure that the surface of the Esc remains free from any particles or contaminants that could affect the rate at which the helium backside gas leaks past the wafer into the process chamber.

2.9.4 TSV Etch Process

The process parameters that are to be used as the basis for all the positive profile etch runs are shown in Table 7, these parameters were chosen because they are typical start points for this type of TSV process. Tests were carried out to determine the process run time that would allow the desired etch depth of >120µm to be obtained while retaining an intact photoresist mask post etch. These test runs resulted in a final process time of 15 minutes and a resulting etch depth of 176.8µm as can be seen in Figure 29 [73] and will be used as the starting point conditions for this research.

Table 7: TSV Process Parameters

Recipe Setting	Parameter Value
Process Time	15’00”
Process Pressure	90 mTorr
SF_6	156 sccm
O_2	80 sccm
Ar	42.5 sccm
Coil Power	3.35 kW
Platen Power	135 W (13.56 MHz)
Platen Temperature	20 ^oC
Helium Backside Pressure	10 Torr

An important consideration when etching a profile is that there is enough of the mask remaining after the process is complete (see Figure 30) to ensure that the silicon substrate is not damaged, the ratio of mask etch to silicon etch is called selectivity and the calculation for this is shown in equation 2.3.

$$\text{Selectivity} = \frac{176.8}{(8.21 - 2.404)} = 30.45$$

The resulting value from the equation is 30.45 which give a selectivity of ~30:1, this indicates that for every 1µm of photoresist mask depth that is etched 30µm of silicon will have removed.

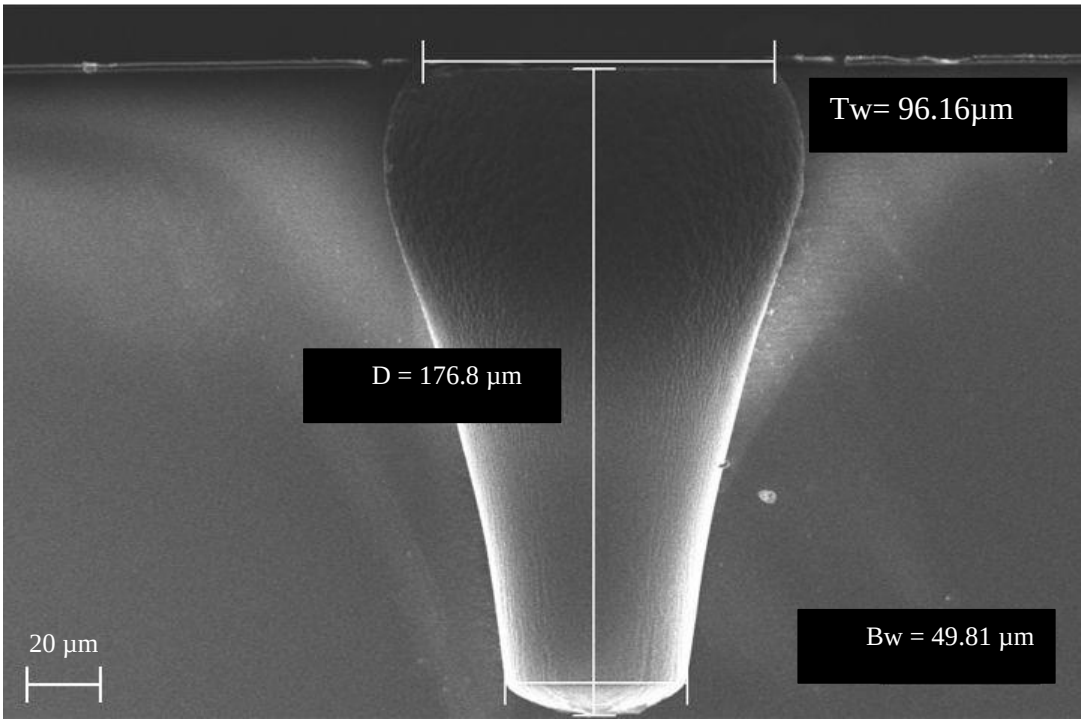


Figure 29: Initial Etch Process Test Result (centre)

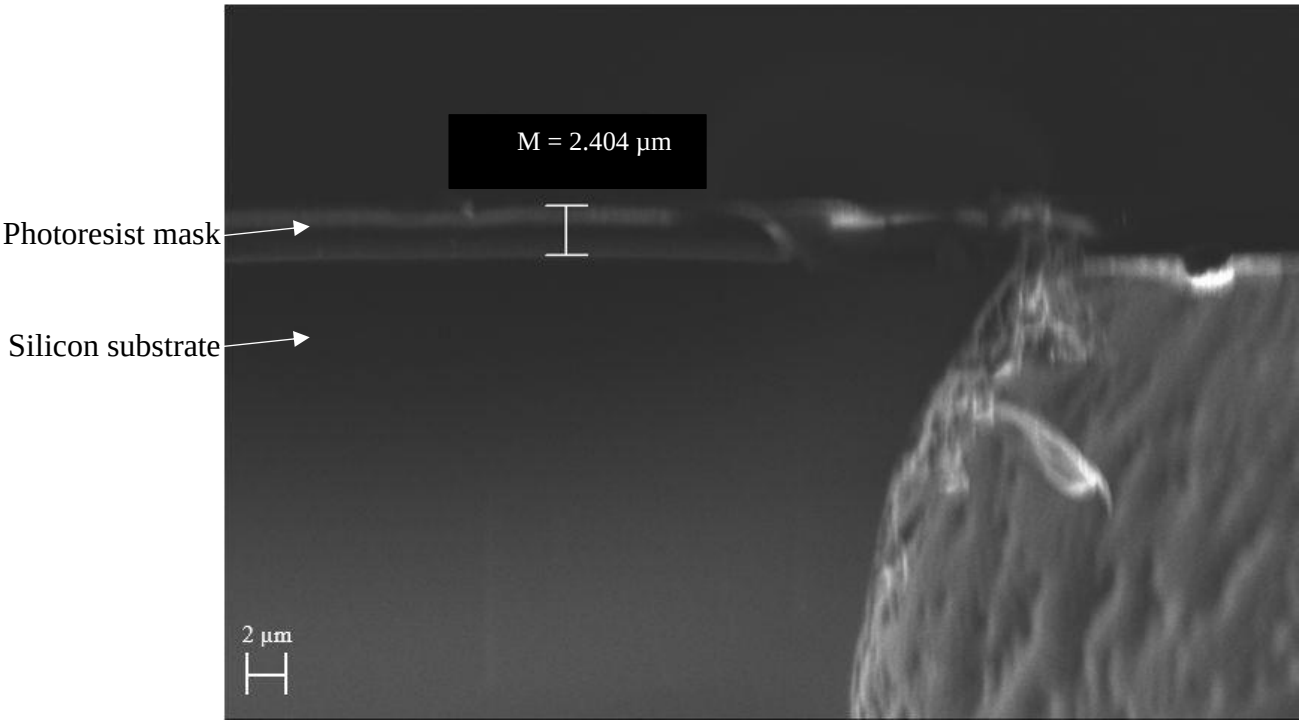


Figure 30: Initial Etch Test Result Mask Thickness

2.10 Etch Process Parameter Trends

2.10.1 Etch Gas

The etch gases (SF_6 and Ar) are the precursors to the etch step, when the plasma is struck it is these gases that are used to form the ions and free radicals that are utilised for both the chemical and physical stages of the etch process. Increasing the gas flow will increase the etch rate up to the point beyond which there is no benefit as the saturation point occurs where all the gas modules have been converted to etch species. When this position is reached both coil power and process pressure increases will be required to further improve the etch rate. The Ar gas present in the process environment will not add to the chemical portion of the etch but is used as a physical etch 'booster' due to its large, heavy molecules.

2.10.2 Passivation Gas

In this programme of work, O_2 is used as a passivation mechanism which causes the silicon to spontaneously form silicon dioxide (SiO_2) when exposed to oxygen during the process. The SiO_2 layer has a different chemical composition to silicon and consequently it is more prone to resist the isotropic segment of the etch process, this results in reduced localised etching which can be exploited to adjust the etch profile. There is a synergy between etch and passivation gas effects which need to be balanced to achieve the desired process results, as too little/much gas will change the shape of the etch profile.

2.9.3 Process Time

This is the length of time that the etch process runs, any increase in process time will have a direct result on the depth of the etch and its profile. Excess process time can increase the relative dimensions of undesirable etch characteristics such as sidewall roughness and has a direct effect on the remaining mask thickness post etch.

2.10.4 Process Pressure

Another method of increasing the chemical substrate etch rate is to raise the process pressure, a rise in the chamber pressure will induce more reactive species into the plasma by increasing the number of collisions between electrons and etch gas molecules, additionally this has the effect of raising the passivation layer deposition rate as the ion transit speeds are lower due to the increased collision rate. The etch rate will increase as the pressure is raised until the saturation point, where the electron/etch gas molecule collision rate becomes so high that the ion and gas species ability to reach the wafer begins to diminish and both the substrate and passivation layer etch rate reduces [73].

2.10.5 Coil Power

RF energy delivered to the source will rotate around the coil and produce a magnetic field that initiates and sustains the plasma. Coil power levels play an important role in the substrate etch rate, with a general rule of thumb being that the higher the coil power, the higher the etch rate. Alongside raises in coil power increases in gas flow and process pressure will typically be required to prevent ‘gas limiting’ which is the theoretical point at which you ionise all the available process gas.

2.10.6 Platen Power

RF energy delivered to the platen will attract the positively charged ions down towards the platen as it is negatively charged and thus provides the physical part of the etch process. Changes to platen RF power levels are used to affect the shape of the etch profile, the silicon etch rate and the mask selectivity [74]. If the platen power is set too low, it will not attract sufficient ions into the base of the features preventing complete removal of the material at the bottom of the voids which will give rise to rough surface finishes and micro masking (grass).

2.10.7 Platen Temperature

The deposition mechanism is a non-switched process is strongly dependent upon temperature, as the platen temperature is reduced the deposition rate of the passivation increases which further inhibits the isotropic and anisotropic etch rates. Higher coil powers will tend to elevate wafer temperatures during processing and as a result the required deposition rate is a balance between coil power level and platen temperature.

2.10.8 Helium Backside Cooling

Pressurised helium gas is injected into the space between the top surface of the electrode and the back side of the wafer during the production process. The gas is used as a cooling transfer medium that allows heat to be transmitted from the substrate to the thermostatic electrode allowing the product devices to remain at the required processing temperature to prevent overheating. Keeping the wafer at the correct temperature for the required process result is essential as any changes have a major effect on the etch profile, and high temperatures can damage any delicate devices that are present on the wafer. Varying the helium pressure will change the amount of heat transfer that is possible, with a higher helium pressure resulting in greater heat transfer over lower pressures.

For a Pegasus system the maximum permitted helium leak-up rate (HeLur) is 150 mTorr/min, this is the point at which the amount of helium gas leaking past the substrate and entering the process chamber can begin to have adverse effects on the process result. For this project the HeLur has been limited to 100 mTorr/min to avoid any possibility of the cooling gas causing issues with the DoE results as it will add a variable that is not being accounted for. Any wafer that is above the limit will be removed from the process chamber and the back side cleaned with isopropyl alcohol to bring the level within the permitted tolerance, if this is not possible the wafer will be replaced.

2.10.9 Etch Process Trend Table

Each parameter in the process recipe has a specific effect during the TSV etch, these effects can be used to predict the conditions that are going to have the best chance of manipulating the profile of the undercut across the surface of the substrate. A complete list of these trends can be seen below in Table 8, it is these known effects that formed the basis of the parameter selection that was undertaken for the DOE that is illustrated in section 2.11

Table Key:

↑ - Trend Increase ↓ - Trend Decrease ↔ - No or Minor Effect

Table 8: Etch Process Trends (reproduced with permission from SPTS)

Controlling Parameter	Etch Rate	Uniformity % +/-	Profile ↑ Negative ↓ Positive	Selectivity (Si: Mask)	Sidewall Roughness	Undercut	Micro Masking	Tilt
Etch Gas Increase (SF_6)	↑	↔↑	↑	↑	↑	↑↑	↓	↔
Passivation Gas Increase (O_2)	↔↓	↔↓	↔	↑	↓	↓↓	↑	↔
Process Time Increase	↑	↔↑	↑	↔↑	↑	↑↑	↑	↔
Process Pressure	↑↑	↑↑	↑↑	↑	↑	↑	↔↓	↔
Coil Power Increase	↑	↔↑	↑	↑	↑	↔↑	↓	↔
Platen Power Increase	↔↑	↔	↔↑	↓↓	↔↑	↔	↓↓	↓
Platen Temp Increase	↔↑	↔↑	↑	↑	↑	↑	↓	↔

2.11 Design of Experiments (DoE)

The method of laying out principles of experimentation involving multiple elements was first proposed by Sir R.A. Fisher in 1935 [75]. This method is known as factorial design and is used to identify all possible interactions for a given set of factors (parameters to be tested), this approach randomises the interactions between each factor to eliminate bias, but it has the drawback of creating a large number of experiments when a significant number of factors are chosen for testing.

In order to reduce the number of experiments to a manageable level, Genichi Taguchi designed a type of fractional factorial design that is based on a special set of patterns called orthogonal arrays, these introduce a way of conducting the minimum number of experiments that are required to estimate the main interaction effects for all of the available parameters [76]. In the Taguchi orthogonal array design only the main effects and two-factor interactions are investigated, higher-order interactions are assumed to be non-existent. In addition, designers are expected to identify which interactions might be significant before starting the design process, this may require that an initial screening experiment is conducted to identify the required parameters. Table 9 shows an example of a Taguchi two level array, in this case the example is known as an L4 (2^3), which means that this experiment would have 4 runs (L4), 3 factors (parameters to be examined), 2 levels (number of times the parameters change).

Table 9: Example L4 (2^3) Taguchi Orthogonal Array

Runs	**Columns**		
	1	**2**	**3**
1	1	1	1
2	1	2	2
3	2	1	2
4	2	2	1

2.12 DOE Run Parameters

The effect on the undercut for each of the single step etch process parameters is well understood and the trends for each of them are detailed in table 8, normally you would only manipulate the individual parameters that give the desired undercut value for the specific etch process result that you are trying to achieve. This project seeks to go beyond this and will try to identify which combination of these parameters has the greatest effect across the whole area of the wafer surface, as it can be seen from the results of the test detailed in section 3.1 that the profile of the etched TSV is significantly different at various test sites across the surface of the wafer.

The most likely candidate parameters for manipulating the undercut size have been taken from Table 8 and are listed below: -

1. Total gas flow.
2. Process pressure.
3. Coil RF power.
4. Platen power.
5. Platen temperature.

Table 7 gives the baseline process parameters for an etched profile of this type, using these values as the baseline it was decided for the purpose of this experiment that the values of each process parameter would be adjusted lower and higher than the base recipe in order to determine the effect of each process parameter on the overall etch profile. Each parameter range had four data points which were equally divided across the range, the values for each process run can be seen in Table 10.

Table 10: DOE Run Table

Run Number	Total Gas Flow	Coil RF Power	Platen RF Power	Process Pressure	Platen Temp
1	278.5	3350	135	90	20
2	139.25	2650	65	60	0
3	139.25	3000	100	90	10
4	139.25	3350	135	135	20
5	139.25	3700	170	170	30
6	278.5	2650	100	135	30
7	278.5	3000	65	170	20
8	278.5	3350	170	60	10
9	278.5	3700	135	90	0
10	417.75	2650	135	170	10
11	417.75	3000	170	135	0
12	417.75	3350	65	90	30
13	417.75	3700	100	60	20
14	557	2650	170	90	20
15	557	3000	135	60	30
16	557	3350	100	170	0
17	557	3700	65	135	10

The ratio between the three process gasses was intentionally fixed with only the total gas flow changing; the breakdown of the individual gas flows can be seen in Table 11.

Table 11: Process Gas Flows as a Percentage of Total Flow

Total Gas Flow	SF6 (56%)	O_2 (28.75%)	Ar (15.25%)
139.25	78	40	21.25
278.5	156	80	42.5
417.75	234	120	63.7
557	312	160	122.2

2.13 Profile Characterisation

Figure 31 is a diagram showing typical results from the TSV etch tests, the profile has several characteristics that help to define the shape of the profile with the main attribute being that the M_W dimension is always larger than B_W, the sizes of the individual dimensions can vary greatly between devices and are shown below for illustration purposes. The main characteristics of interest are depth (D), top width (T_W), maximum width (M_W), bottom width (B_W), the mask thickness (M_T) is used to calculate selectivity and does not form part of the feature characteristics.

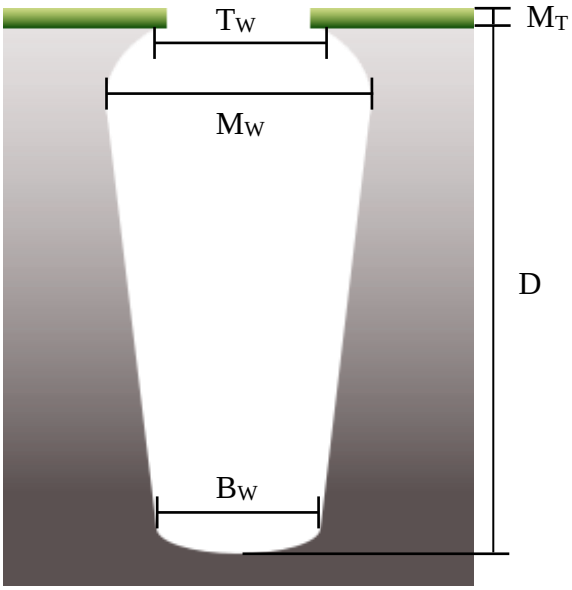


Figure 31: TSV Profile Explanation

Top Width (T_W)

Top width is the dimension of the very top of the feature where it touches the underside of the mask, this dimension is normally larger than the mask feature that defines it, due to the undercutting effects of both ion scattering from the edge of the mask and chemical etch as the process species beginning to etch the surface of the silicon.

Maximum Width (M_W)

Maximum width is the widest point of the etch profile, in a perfect profile this value would be the same as the top width, but this is rarely the case as the undercut is normally curved inwards towards the mask opening. It is the ratio between the maximum width and the bottom width that ultimately defines the type of etch profile, whether it is positive, negative, or vertical.

Bottom Width (B_W)

The bottom width is the dimension of the bottom of the profile 'wall' where it transitions to the profile base. The ideal etch profile will be a straight line between the bottom and maximum widths as illustrated in Figure 31.

Depth (D)

The depth of the profile is measured between the underside of the mask and the bottom of the profile. In a feature that would ultimately be used as part of a production device this depth would be a critical dimension and was specified to be >120µm which is the approximate point at which the undercut is fully formed. Figure 32 shows a failed process test that used the same process conditions as the run that resulted in Figure 29, the lack of undercut formation can be clearly seen in the underdeveloped profile.

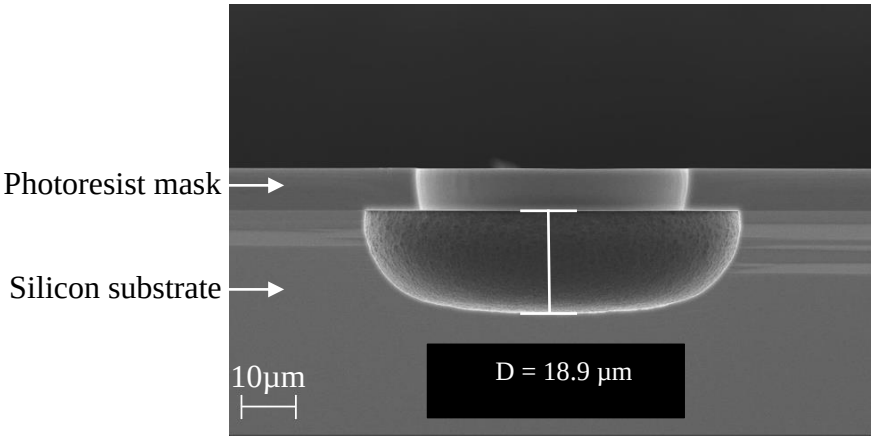


Figure 32: Failed Process Test

Mask Thickness (M_T)

Mask thickness is usually measured before and after the etch process has been run and is used to calculate selectivity as shown in equation 2.3. Mask thickness is primarily used as an indicator to the maximum etch depth limit, the test run shown in section 2.8.4 calculates the selectivity at 30:1. The mask thickness was measured at 8.2µm before the process runs were started meaning that the maximum possible etch depth without total mask removal is 8.2 x 30 = 246µm (assuming a linear etch rate).

2.14 Measurement Locations

The measurement locations on the surface of the wafer were taken at the positions shown in Figure 33, the locations are Centre (C), Left (L), Right (R), Main Flat (MF), Opposite Main Flat (OMF). Wafer 1 had measurements taken from all 5 locations, but due to the high degree of uniformity across the positions on the outside of the substrate it was decided on all subsequent process runs to only record measurements at locations C, MF, OMF. As these are the most likely positions to suffer non-uniformity issues due to localised effects caused by the location of the chamber pumping port and edge loading [61].

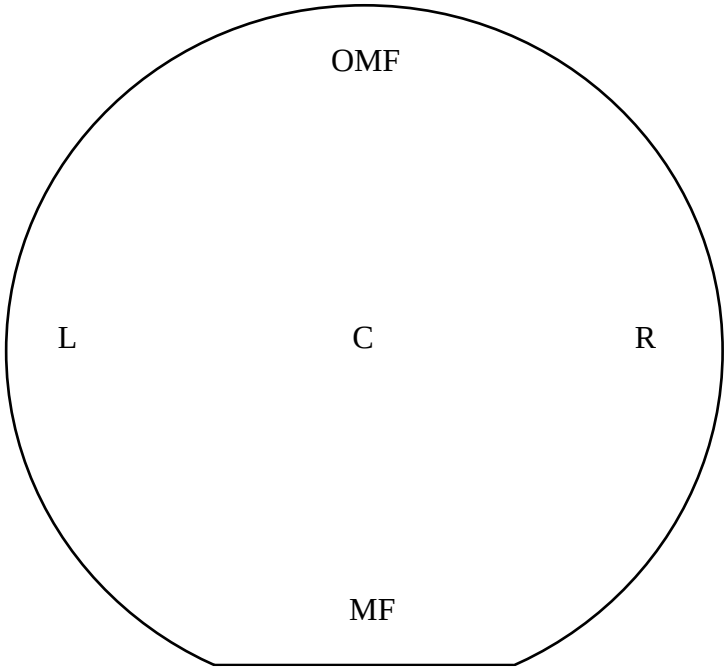


Figure 33 Measurement Locations

2.15 Sample Measurement

In order to measure the finished etch profiles of each process sample, the finished wafer was intentionally cut to allow access to the side profile of the target vias. The whole wafer was initially cleaved in the locations indicated by the red lines to remove a strip from the centre of the wafer and the resulting strip was further sectioned to free the target areas as indicated in Figure 34.

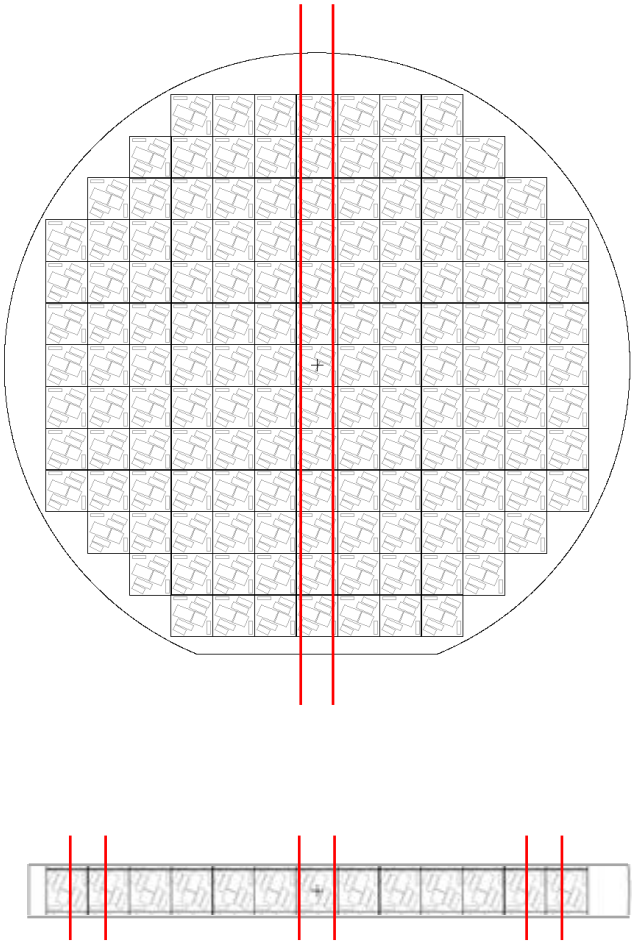


Figure 34 Processed Wafer Cleave Positions

Each sample piece was mounted into a SEM sample holder and inserted into a Carl Zeiss Sigma HV scanning electron microscope to allow profile measurement.

2.16 Analysis Method

Table 12: Full Results

Input Parameters								
Run No'	SF6 (56%)	O2 (28.75%)	Ar (15.25%)	Total Gas Flow	Coil RF Power	Platen RF Power	Process Pressure	Platen Temp
1	156	80	42.5	278.5	3350	135	90	20
2	78	40	21.25	139.25	2650	65	60	0
3	78	40	21.25	139.25	3000	100	90	10
4	78	40	21.25	139.25	3350	135	135	20
5	78	40	21.25	139.25	3700	170	170	30
6	156	80	42.5	278.5	2650	100	135	30
7	156	80	42.5	278.5	3000	65	170	20
8	156	80	42.5	278.5	3350	170	60	10
9	156	80	42.5	278.5	3700	135	90	0
10	234	120	63.7	417.75	2650	135	170	10
11	234	120	63.7	417.75	3000	170	135	0
12	234	120	63.7	417.75	3350	65	90	30
13	234	120	63.7	417.75	3700	100	60	20
14	312	160	122.2	557	2650	170	90	20
15	312	160	122.2	557	3000	135	60	30
16	312	160	122.2	557	3350	100	170	0
17	312	160	122.2	557	3700	65	135	10

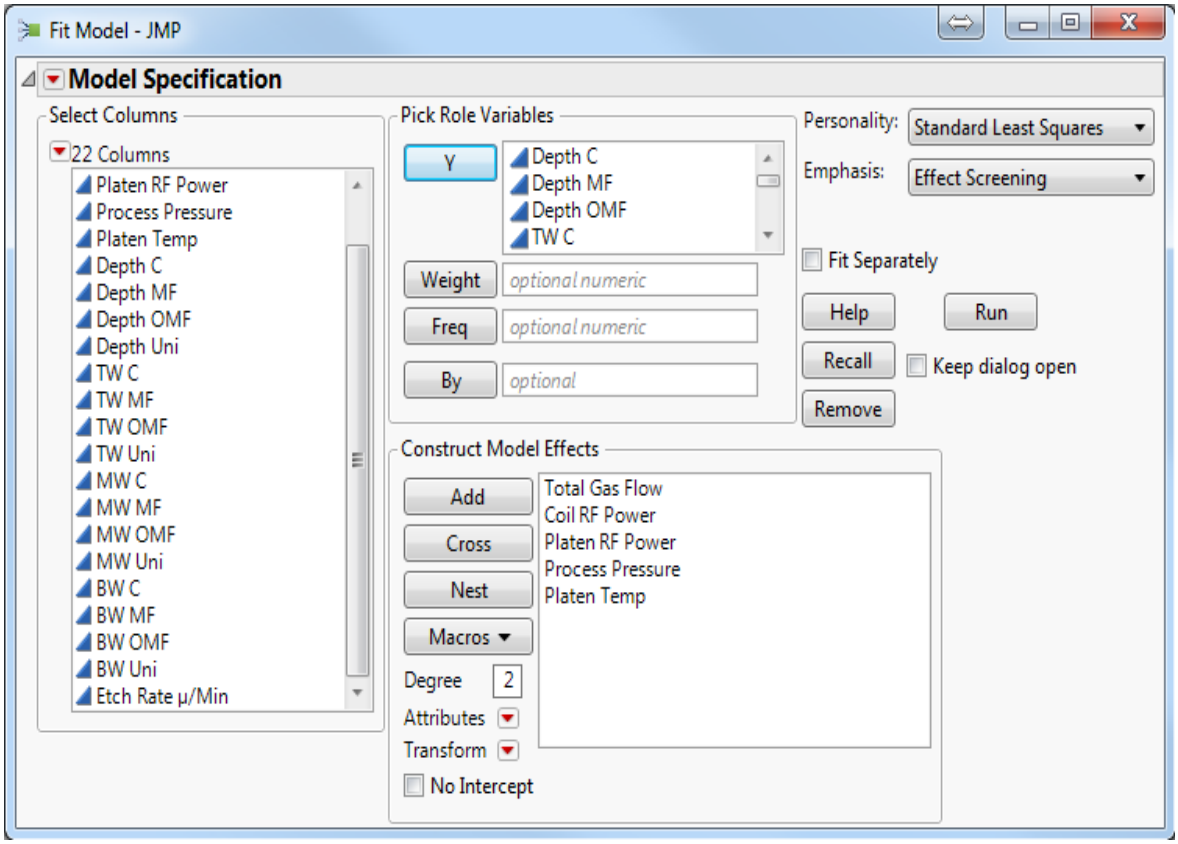
Measured Results (µm)																
Run No'	Depth C	Depth MF	Depth OMF	Depth Uni	TW C	TW MF	TW OMF	TW Uni	MW C	MW MF	MW OMF	MW Uni	BW C	BW MF	BW OMF	BW Uni
1	178.7	146.9	157.3	10.13	96.31	100.6	97.49	2.17	111.1	120.8	119.6	4.92	46.59	69.13	59.92	19.5
2	123.4	124.9	122	1.17	60.9	56.37	67.01	8.66	69.96	72.15	75.39	3.74	45.51	43.06	31.7	17.22
3	106.5	138.1	135.9	12.45	71.14	73.77	73.41	1.8	78.33	83.7	85.45	4.31	45.76	35.7	39.14	12.51
4	95.97	134	136.5	16.58	73.42	78.91	78.67	3.56	80.42	90.24	90.68	5.88	43.7	38.09	39.22	6.95
5	110.8	136.2	133.9	10	81.75	84.36	83.92	1.56	88.92	95.72	96.03	3.8	42.1	35.19	44.55	11.52
6	118.4	154.1	161	14.74	102.9	109.4	110.3	3.44	111	122.3	123.1	5.09	42.24	34.27	40.84	10.18
7	67.86	115.4	100.3	25.14	89.45	104.6	100.5	7.71	94.29	108.7	105.3	7.01	32.88	38.21	26.2	18.51
8	145.4	120.6	129.6	9.4	80.57	85.98	83.21	3.25	100.8	112.6	105.8	5.45	58.66	68.46	61.68	7.78
9	184.1	163.2	171.4	6.04	83.75	87.96	87.28	2.44	95.56	110	107.2	6.92	31.88	54.21	49.47	24.7
10	125.5	193.3	195.5	20.4	97.77	123.7	120.5	11.37	106.9	141.2	134.2	13.45	43.79	40.26	23.13	28.9
11	184.6	192.2	200.5	4.13	99.12	109.6	106.5	4.98	112.5	133.2	129.3	8.28	48.67	54.82	50.3	5.99
12	186.9	157.3	167.5	8.67	105.7	115.5	111.6	4.42	120.3	133.3	126.5	5.13	30.99	35.12	44.39	18.19
13	173.1	147.2	152.1	8.22	87.13	94.82	95.22	4.38	102.9	116.3	114.9	6.01	52.05	63.71	57.82	10.07
14	191.2	153.1	163.8	11.25	102.8	114.3	105.9	5.34	121.1	139	132.4	6.84	43.53	80.14	66.61	28.86
15	165.1	136.7	142	9.59	96.47	101.7	102.2	2.86	112.3	124.5	122.2	5.09	60.5	79.88	70.21	13.8
16	114	172.2	147.1	20.15	96.71	129	116.9	14.14	107.3	142	128.5	13.78	43.73	46.37	48.78	5.28
17	132	175.6	162.5	13.91	111.4	129.7	132.2	8.36	122.2	124.5	136.8	8.47	43.72	42.67	49.84	7.89

Table 12 shows the full parameter set and results, due to the high number of input variables, a large volume of resulting output data was produced making the manual identification of interactions between the variables problematic. A powerful way to interpret the correlations between variables is to use a regression analysis table, this is a parametric technique [77] that is used when two or more variables are thought to be systematically connected by a linear relationship, it is parametric in nature because it makes certain assumptions based on the provided data set. Regression analysis can be performed using a software package such as Microsoft Excel, but this method is not feasible for large data sets as the calculations need to be performed individually. To automate this process, it was deemed that a specific statistical analysis software package would be preferable, as they are designed to analyse the data using multiple methods that are more likely to identify subtle interplays between process criteria. While there are many such software packages on the market today, the product that was settled on was JMP Statistical Discovery™ from SAS [78].

The entire table of results shown in Table 12 were recorded in Microsoft Excel format, these were subsequently imported into the JMP software for analysis using the Fit Model analysis option within the JMP software. In order to create the statistical model specific information needs to be provided, the Construct Model Effects are the parameters that need to be investigated for possible interactions, these were: - Total Gas Flow, Coil RF Power, Platen RF Power, Process Pressure and Platen Temperature. The Pick Role Variables are the etch profile dimensions that are to be investigated, for this programme these were: - Depth (centre, main flat and opposite main flat), Top Width (centre, main flat and opposite main flat), Maximum Width (centre, main flat and opposite main flat), Bottom Width (centre, main flat and opposite main flat). Once the investigation parameters are provided, the data must be subjected to a series of software tests that are designed to investigate all the possible interactions within the data set. A series of models were run with varying statistical model effects (macros) and the best results were found with the combination of a Full Factorial Model which investigates the relationship between each parameter and every other parameter in the provided

information. The personality type ‘Standard Least Squares’ is used in addition to the model with this effect minimizing the sum of the squares of the residuals (the difference between the actual and fitted value in the model) with a view to finding the best possible value for the regression coefficients. The Emphasis option was set to the default (Effect Screening), this parameter simply defines the display options for the report and has no actual effect on the values of the results, the Fit Model options setup can be seen in Figure 35.

Figure 35: JMP Fit Model settings



Chapter 3 – Results

This chapter presents the results obtained from the design of experiments process runs and interprets the outcomes investigated by the regression analysis software. The results are presented with SEM photographs and profile dimension measurements, with explanations of the variations in profile change.

Table 13 contains the values of the measured pre-etch mask thickness, the helium leak-up rate and the selectivity for each of the numbered process runs, this information is not going to be analysed as part of this research project. The mask thickness is used as part the selectivity calculation which shows the silicon to mask etch rate ratio, the helium leak-up rate is a good measure of how well the wafer is clamped to the platen during the etch process, a lower number is preferable as less helium is leaking from underneath the substrate into the process chamber during the etch process.

Table 13: Sample mask thickness, HeLur, Selectivity

Run	Pre-etch mask thickness (µm)	HeLur mTorr/Min	Selectivity
1	8.24	33.2	28:1
2	8.21	33.32	46:1
3	8.31	82.7	41:1
4	8.32	36.9	40:1
5	8.5	21.2	38:1
6	8.49	26.5	51:1
7	8.52	58.1	76:1
8	8.31	49.4	17:1
9	8.23	30.9	32:1
10	8.59	27.8	46:1
11	8.18	38.2	31:1
12	8.22	33.9	56:1
13	8.46	25.6	24:1
14	8.52	34.1	23:1
15	8.17	39.5	20:1
16	8.6	78.5	38:1
17	8.4	31.5	50:1

The results from each process run are shown below in the order that they were performed, run 1 is the baseline process and the results of the parameter changes can be seen in the tables and SEM photographs that are documented for each of the following runs.

3.1 Run 1: (Starting process)

Table 14: Run 1 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	96.31	111.1	46.59	178.7	3.084
Right	98.74	119.5	58.83	153.7	2.656
Left	99.72	122.8	53.90	148.0	2.393
Main Flat	100.6	120.8	69.13	146.9	2.403
Opposite Main Flat	97.49	119.6	59.92	157.3	2.475
Uniformity (%)	2.17	4.92	19.5	10.13	12.44

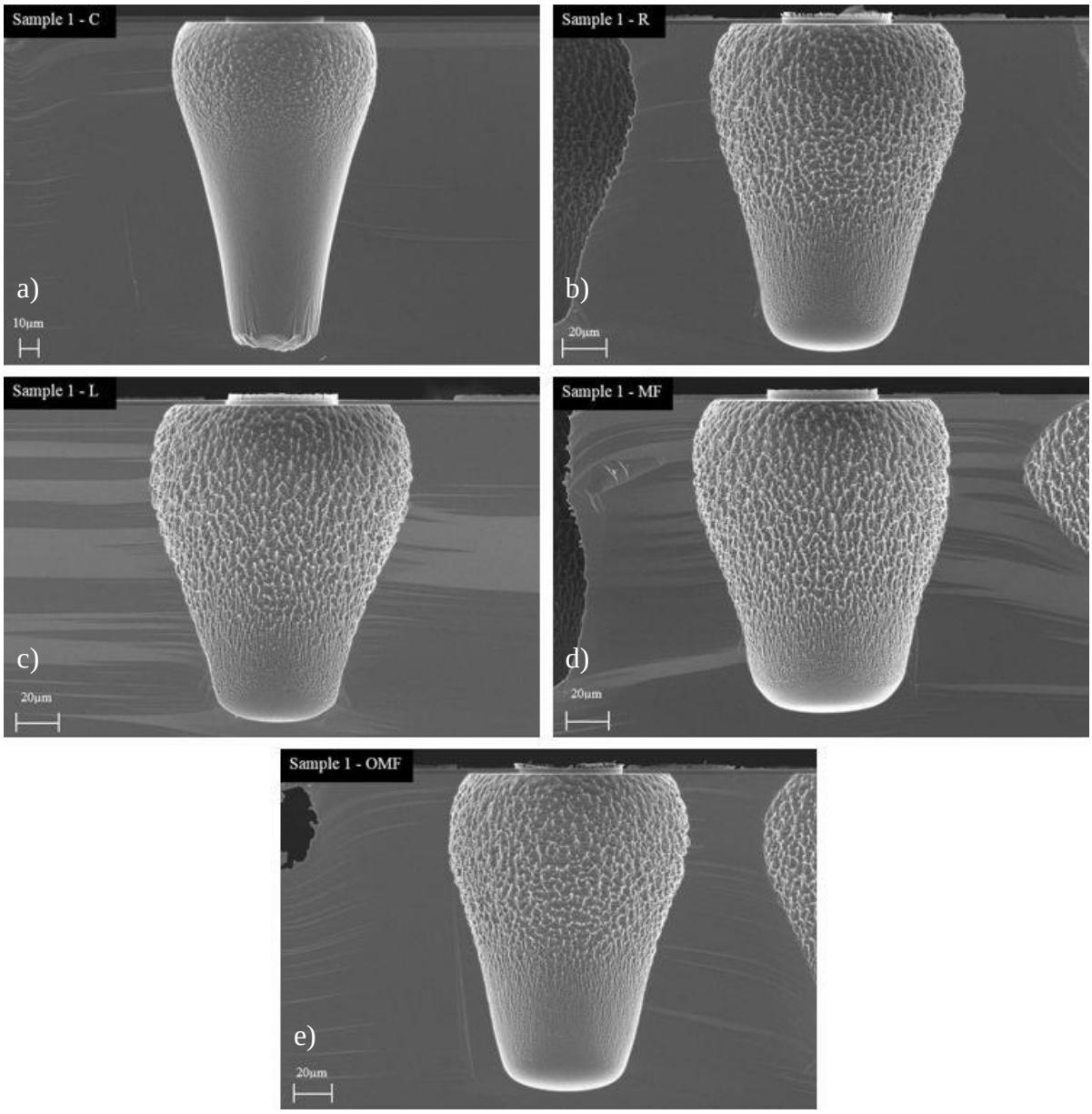


Figure 36: Run 1 Results - a) Centre b) Right c) Left d) Main Flat e) Opposite Main Flat

3.2 Run 2: (- gas flow - coil RF - platen RF - pressure - platen temperature)*

Table 15: Run 2 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	60.9	69.96	45.51	123.4	5.662
Main Flat	56.37	72.15	43.06	124.9	5.544
Opposite Main Flat	67.01	75.39	31.7	122.0	5.362
Uniformity (%)	8.66	3.74	17.22	1.17	2.71

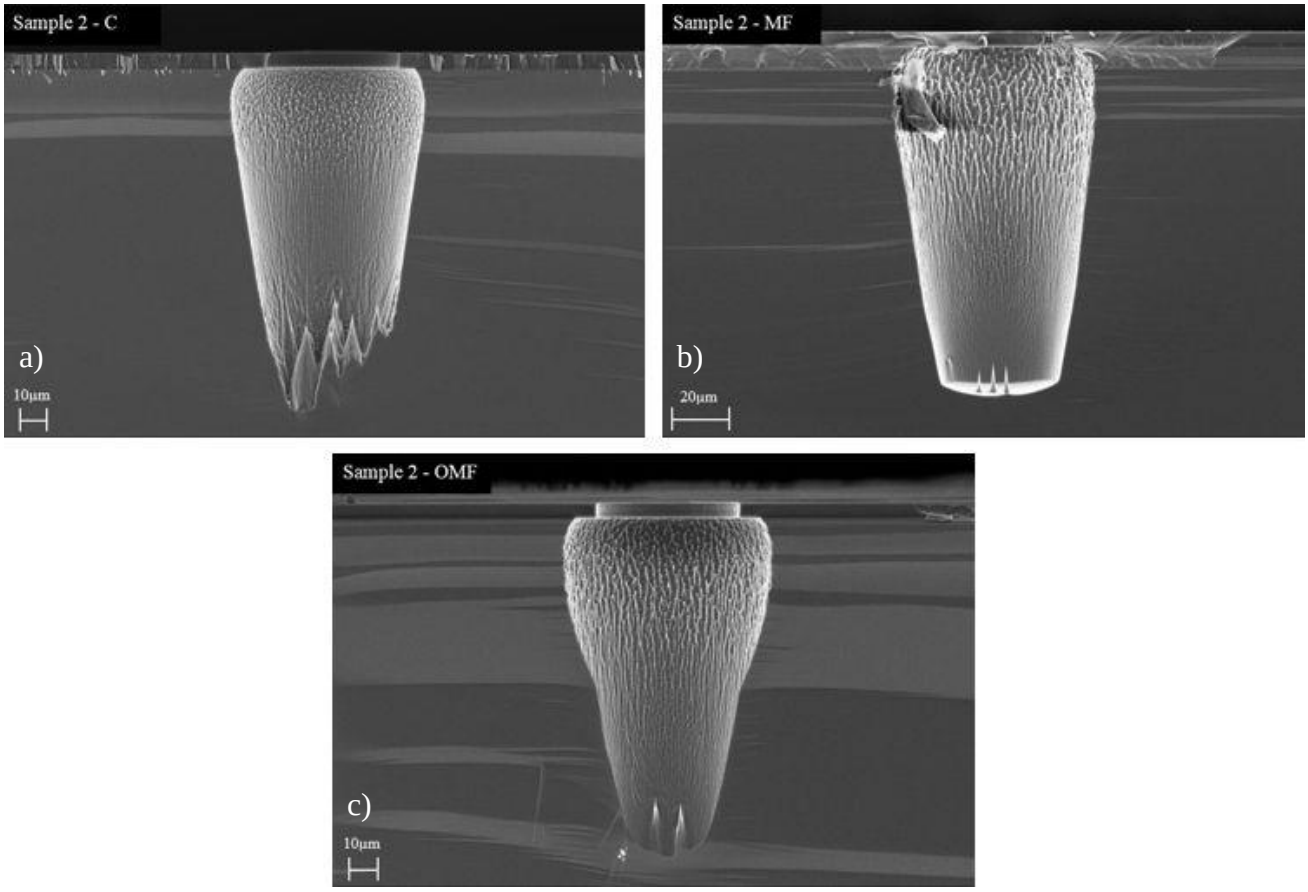


Figure 37: Run 2 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 1 shows the standard process conditions as detailed in Table 7, the effects of the changes made to the recipe in run 2 are showing clearly on the results in Figure 37. All three profiles are experiencing reduced depth which correlates to the lower coil power setting, the spikes in the bottom of each feature are micro-masking which is likely to be a combination of the result of the lowering the coil power and platen temperature decreasing the passivation layer etch rate.

*When compared to the previous process

3.3 Run 3: (= gas flow + coil RF + platen RF + pressure + platen temperature)*

Table 16: Run 3 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	71.14	78.33	45.76	106.5	5.613
Main Flat	73.77	83.7	35.7	138.1	5.081
Opposite Main Flat	73.41	85.45	39.14	135.9	4.983
Uniformity (%)	1.8	4.31	12.51	12.45	6.03

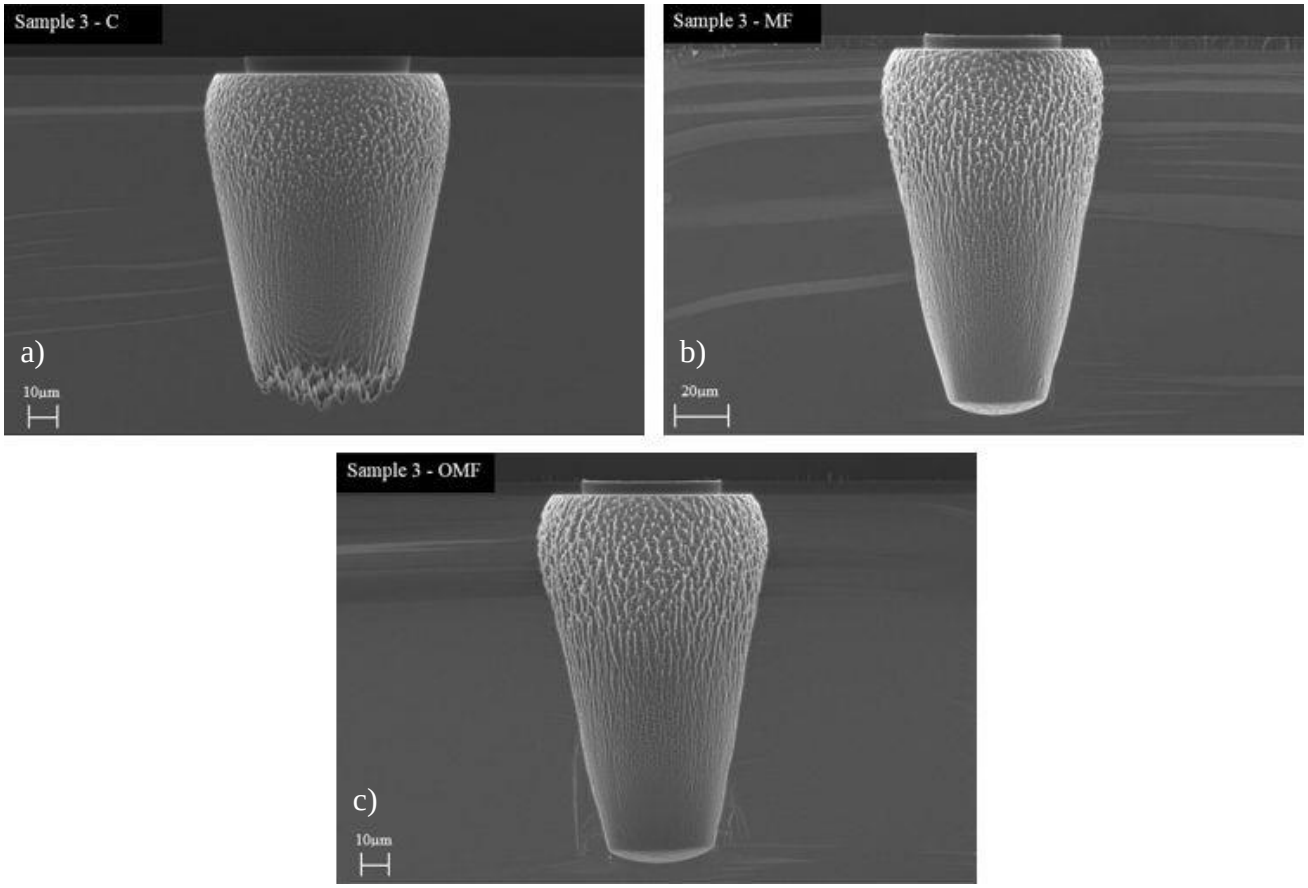


Figure 38: Run 3 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 3 has a reduced depth over the control recipe (run 1) which is due to the lower coil RF power and total gas flow. The results shown in Figure 38 (b) & (c) are very similar and are both located on the periphery of the substrate. The centre of the wafer (Figure 38a) is showing low etch depth and large amounts of micro masking which is likely to be caused by ‘edge loading’ where the edges of the substrate have more species available to them and have a higher etch rate as a result.

3.4 Run 4: (= gas flow + coil RF + platen RF + pressure + platen temperature)*

Table 17: Run 4 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	73.42	80.42	43.70	95.97	5.539
Main Flat	78.91	90.24	38.09	134.0	5.139
Opposite Main Flat	78.67	90.68	39.22	136.5	5.192
Uniformity (%)	3.56	5.88	6.95	16.58	3.78

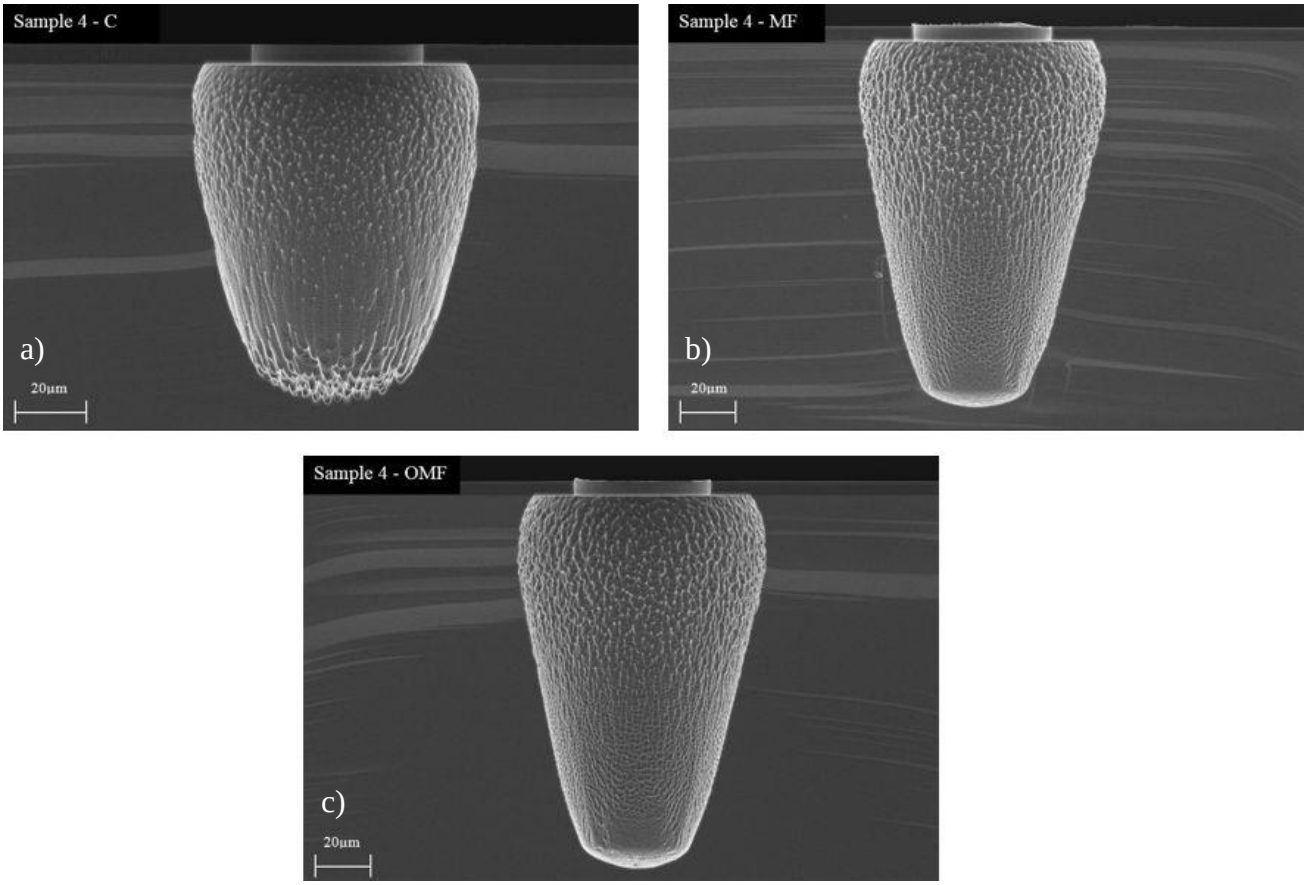


Figure 39: Run 4 Results – a) Centre b) Main Flat c) Opposite Main Flat

Figure 39 (a) again shows the effects of edge loading as the depth is lower than Figure 39 (b) & (c), the feature sizes are slightly smaller than the base line etch. This is likely to have been caused by the increase in process pressure that results in a longer mean free path between the plasma and substrate surface due to increased etch species collisions.

3.5 Run 5: (= gas flow + coil RF + platen RF + pressure + platen temperature)*

Table 18: Run 5 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	81.75	88.92	42.1	110.8	5.492
Main Flat	84.36	95.72	35.19	136.2	4.906
Opposite Main Flat	83.92	96.03	44.55	133.9	5.013
Uniformity (%)	1.56	3.8	11.52	10	5.7

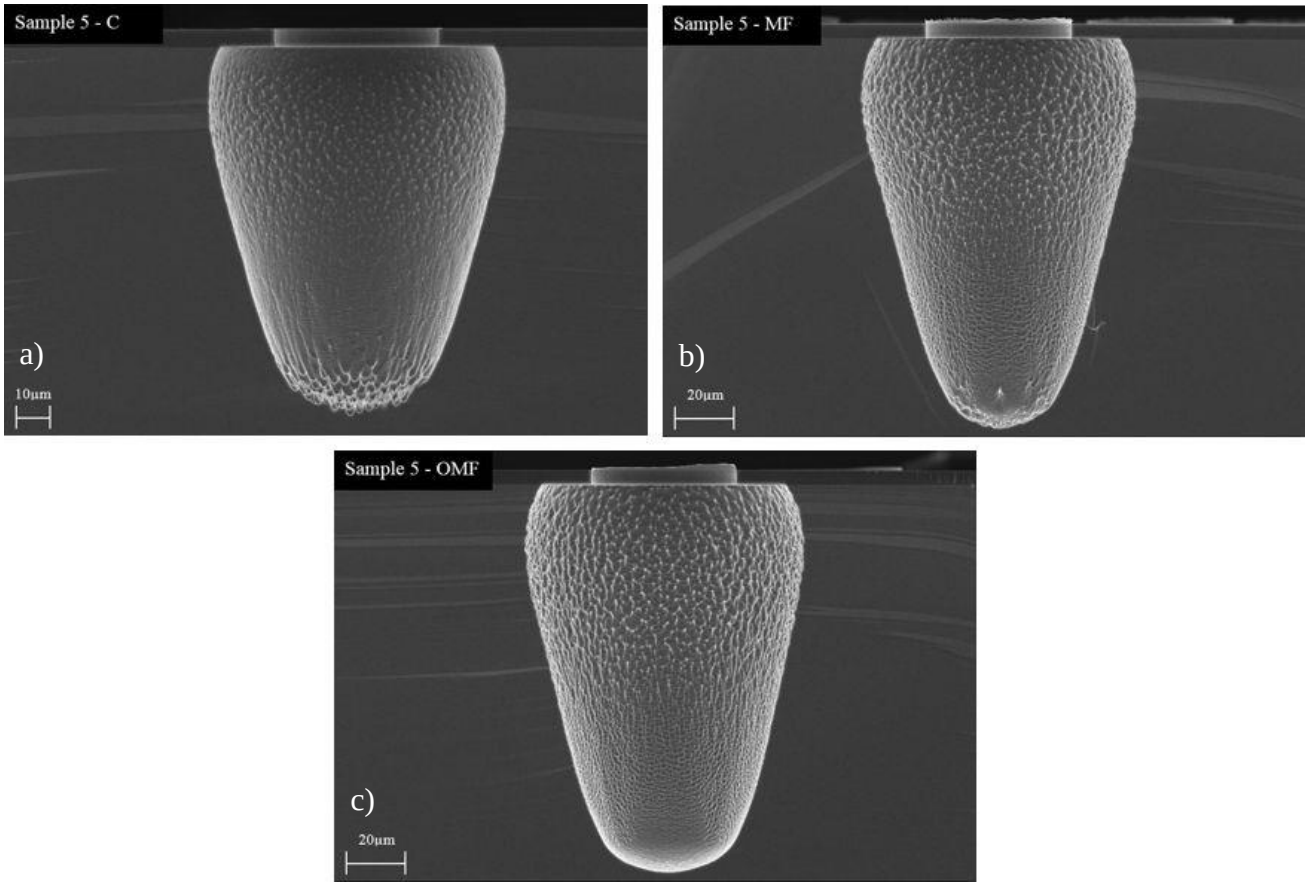


Figure 40: Run 5 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 5 (Figure 40) indicates that the profile non-uniformity between the three element positions is much reduced even with the lower etch rate typically seen in the centre position. The Coil and Bias RF powers are higher for Run 5 than the baseline process which will increase the etch rate, but this is counteracted by the large increase in process pressure.

3.6 Run 6: (+ gas flow - coil RF - platen RF - pressure = platen temperature)*

Table 19: Run 6 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	102.9	111	42.24	118.4	6.005
Main Flat	109.4	122.3	34.27	154.1	5.611
Opposite Main Flat	110.3	123.1	40.84	161	5.418
Uniformity (%)	3.44	5.09	10.18	14.74	5.17

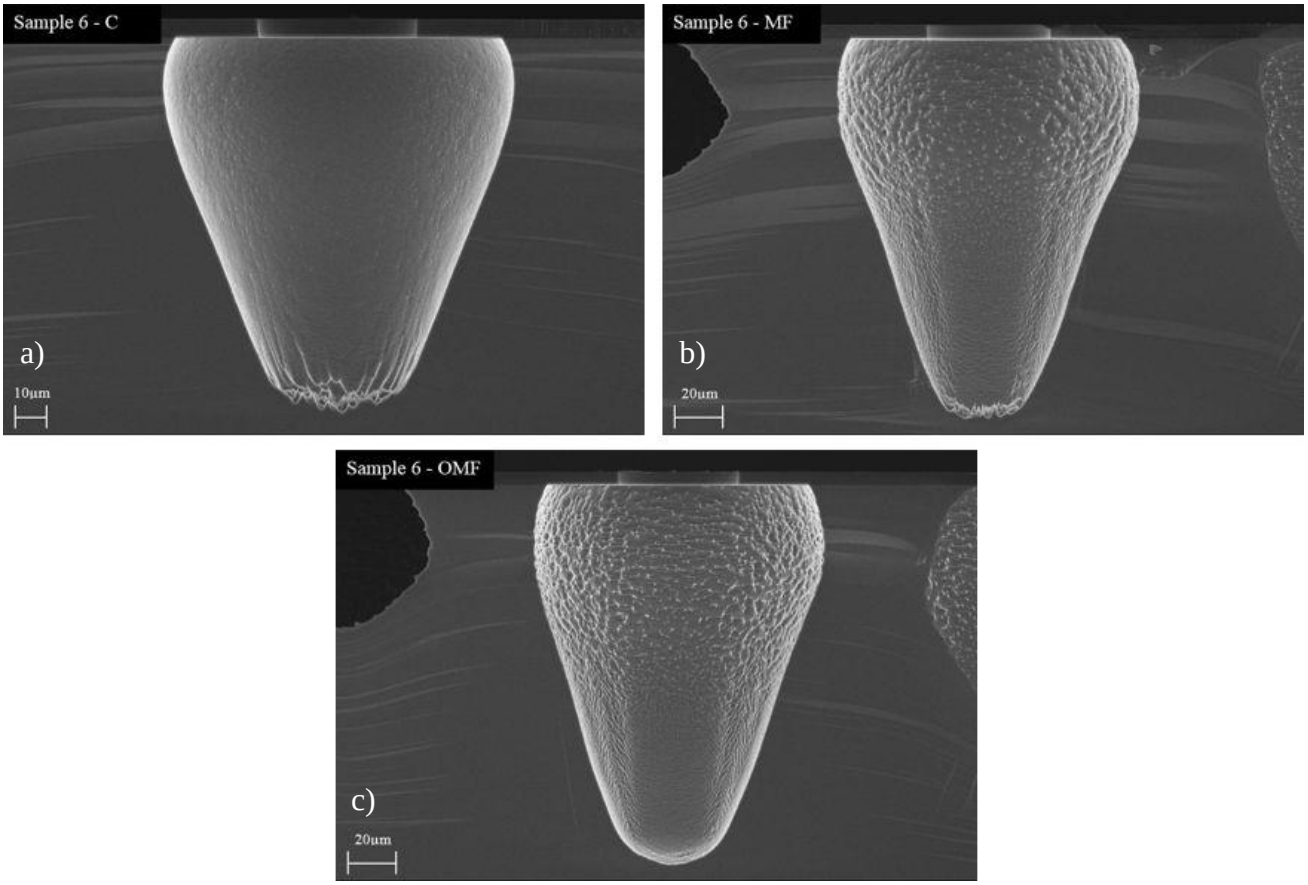


Figure 41: Run 6 Results – a) Centre b) Main Flat c) Opposite Main Flat

The results in Figure 41 are showing increased depth over the previous 4 runs, along with increased lateral etching that has enlarged the undercut compared to the prior runs. The reason for the increased top width dimension is likely to be increased ion scattering due to decreased process pressure.

3.7 Run 7: (= gas flow + coil RF - platen RF + pressure - platen temperature)*

Table 20: Run 7 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	89.45	94.29	32.88	67.86	7.366
Main Flat	104.6	108.7	38.21	115.4	7.606
Opposite Main Flat	100.5	105.3	26.2	100.3	6.828
Uniformity (%)	7.71	7.01	18.51	25.14	5.35

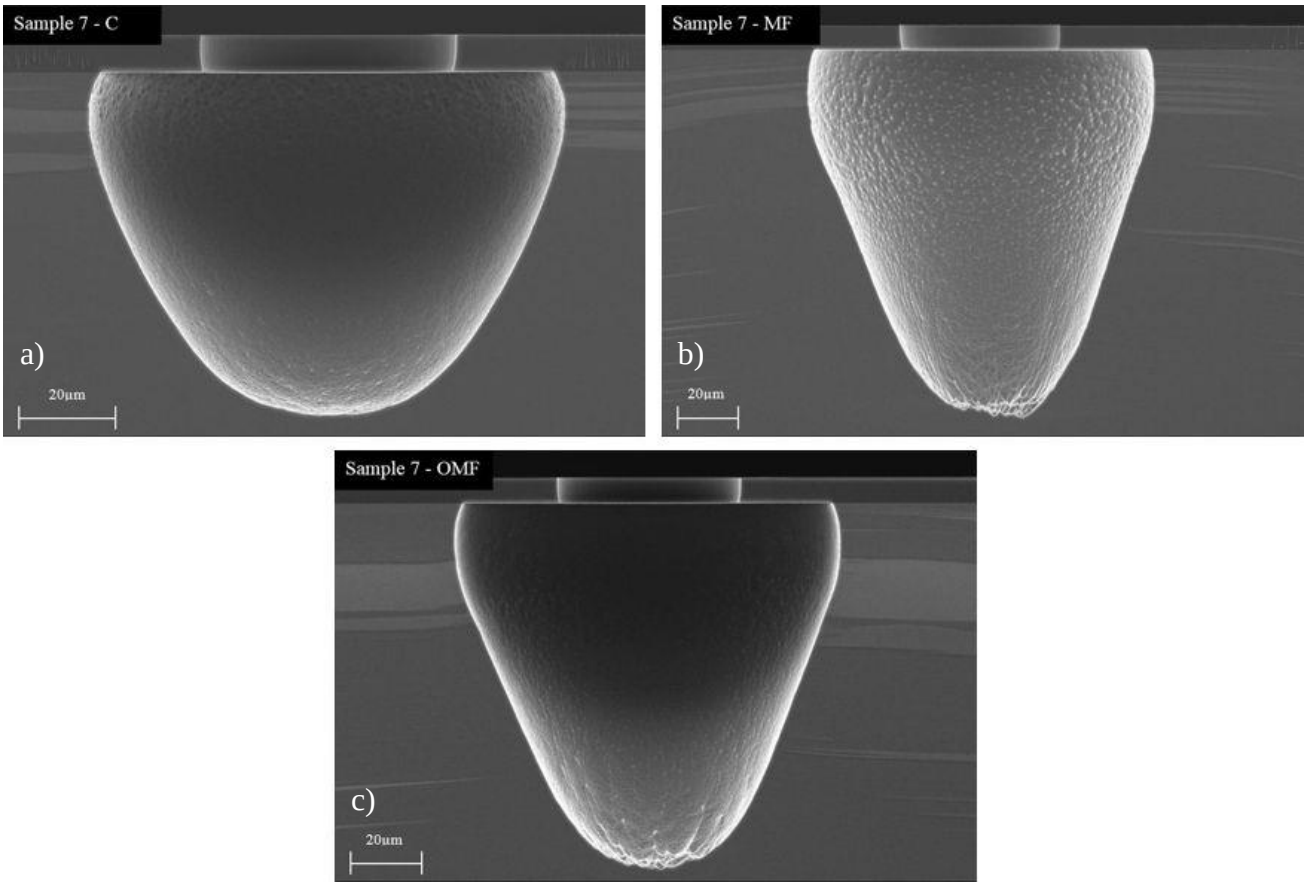


Figure 42: Run 7 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 7 is showing a large difference in profile when compared to the previous results, in Figure 42 the shape of the features has changed from an inverted cone to a more ‘strawberry’ like shape. This is caused by a combination of low RF bias power and high process pressure that is limiting the ability of the process chamber to remove the passivation layer in the bottom of the feature.

3.8 Run 8: (= gas flow + coil RF + platen RF - pressure - platen temperature)*

Table 21: Run 8 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	80.57	100.8	58.66	145.4	0
Main Flat	85.98	112.6	68.46	120.6	0.803
Opposite Main Flat	83.21	105.8	61.68	129.6	0.368
Uniformity (%)	3.25	5.45	7.78	9.40	0.103

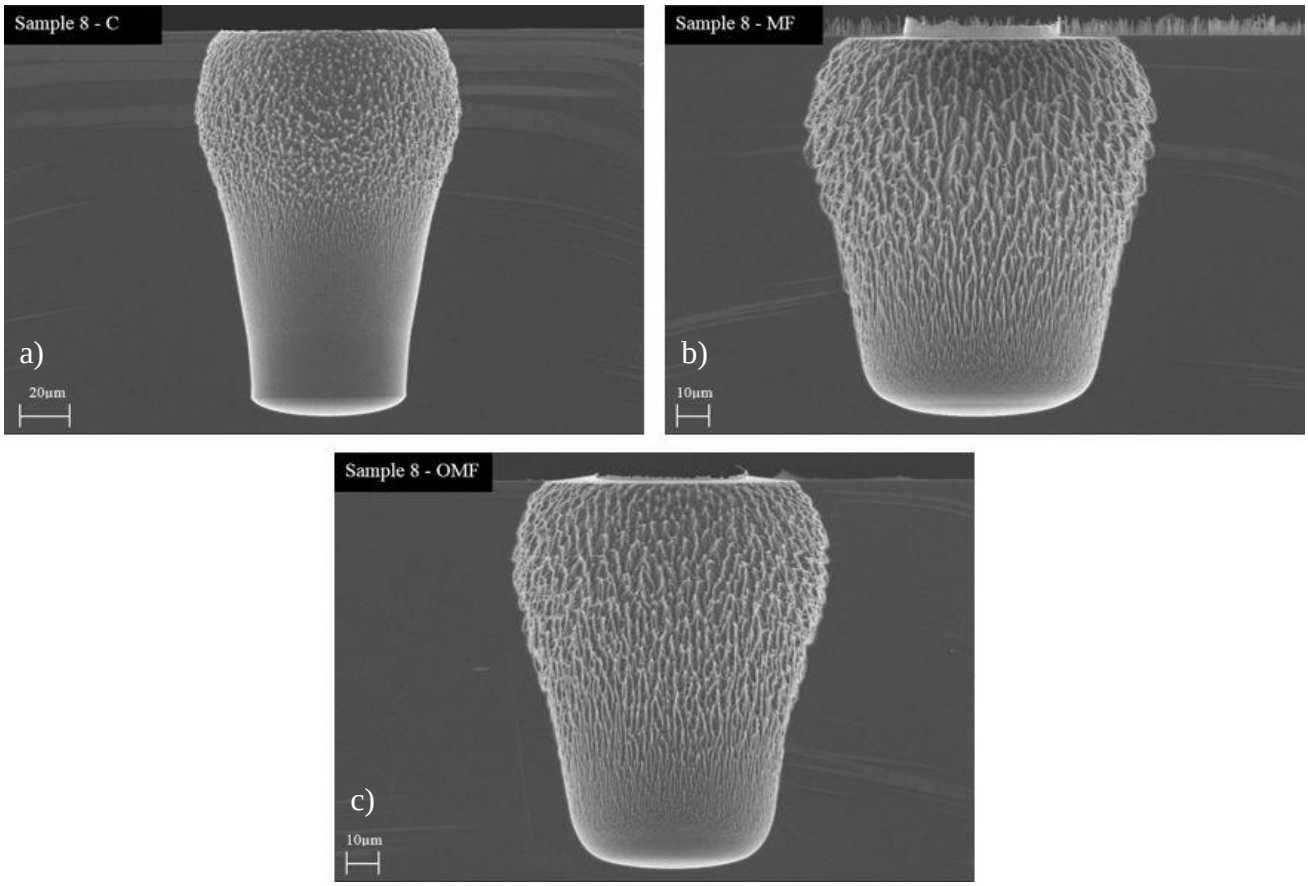


Figure 43: Run 8 Results – a) Centre b) Main Flat c) Opposite Main Flat

The mask shown in Figure 43 was etched away completely in the centre (a), two additional measurements around the centre where the mask is still present were recorded with etch depths of 146.2µm and 143µm. These additional measurements are very similar to the depth shown for the actual centre position, indicating that the mask was intact until the final few second of the etch process. The high etch rate is due to the combination of high powers and low process pressure in this process recipe.

3.9 Run 9: (= gas flow + coil RF - platen RF + pressure - platen temperature)*

Table 22: Run 9 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	83.75	95.56	31.88	184.1	2.788
Main Flat	87.96	110	54.21	163.2	2.862
Opposite Main Flat	87.28	107.2	49.47	171.4	2.788
Uniformity (%)	2.44	6.92	24.7	6.04	1.31

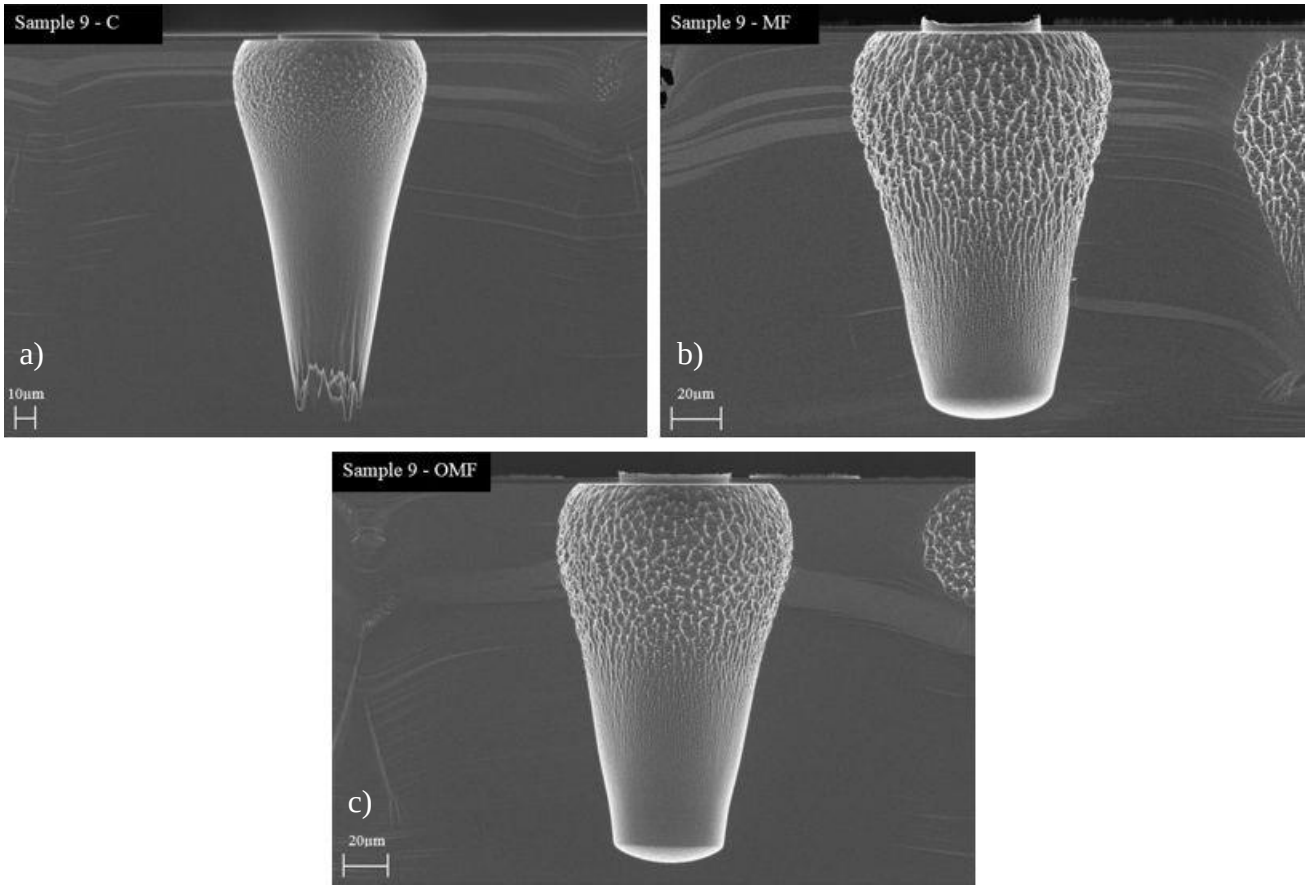


Figure 44: Run 9 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 9 has high coil and bias RF powers combined with a lower pressure; this has increased the etch rate and is highlighted in Figure 44 by the long/slim etch profiles. The spikes at the bottom of the feature that can be seen in Figure 44 (a) are the likely result of micro-masking due to the low platen temperature, and edge loading.

3.10 Run 10: (+ gas flow - coil RF = platen RF + pressure + platen temperature)

Table 23: Run 10 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	97.77	106.9	43.79	125.5	5.518
Main Flat	123.7	141.2	40.26	193.3	4.395
Opposite Main Flat	120.5	134.2	23.13	195.5	4.771
Uniformity (%)	11.37	13.45	28.9	20.4	11.47

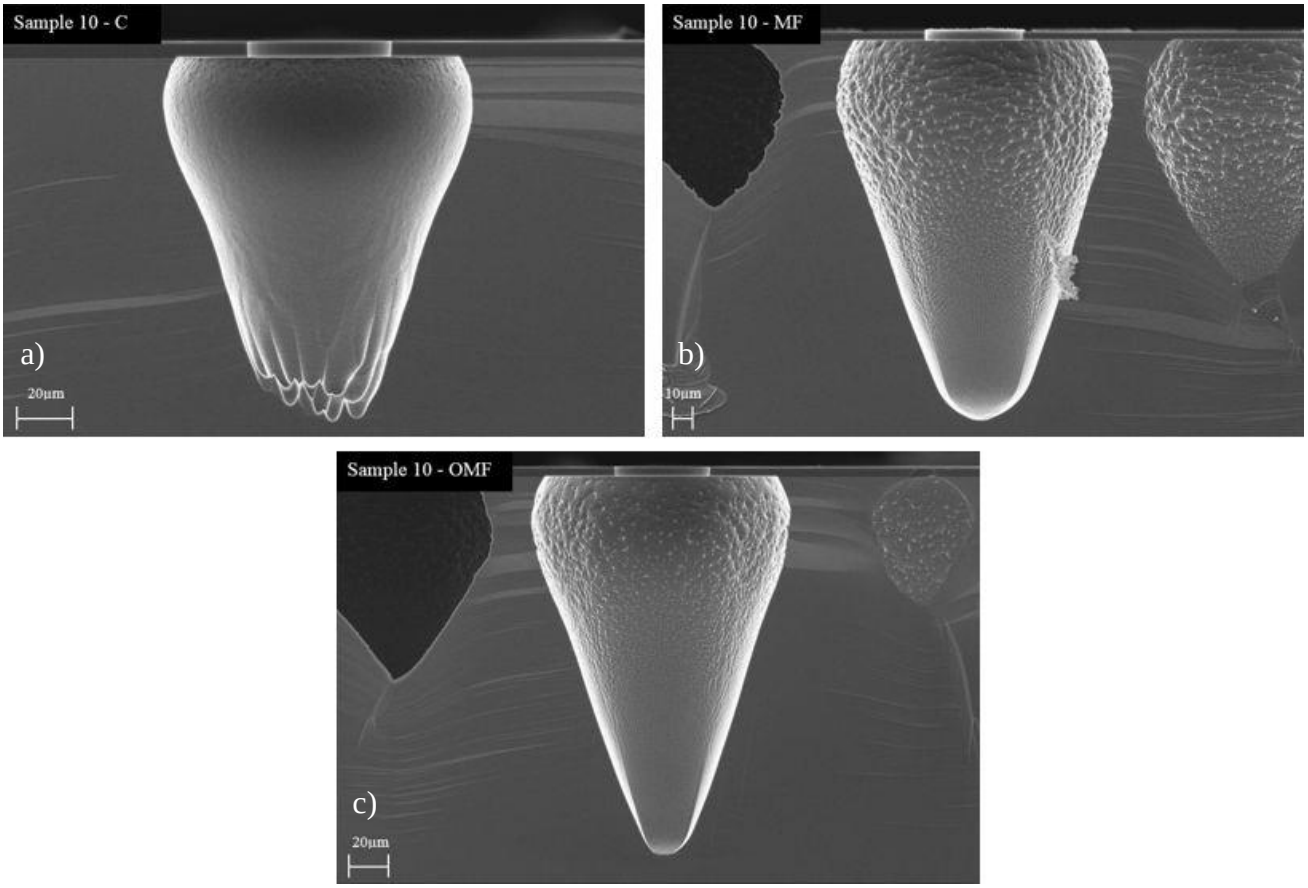


Figure 45: Run 10 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 10 results as shown in Figure 45 are showing increased dimensions overall, except for the bottom width. This is counterintuitive, as you would expect to see an increase across all dimensions with these process conditions. Although a possible explanation is that the feature is simply deeper than that seen in run 9 and as a result the feature is more formed.

3.11 Run 11: (= gas flow + coil RF + platen RF - pressure - platen temperature)*

Table 24: Run 11 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	99.12	112.5	48.67	184.6	2.230
Main Flat	109.6	133.2	54.82	192.2	1.842
Opposite Main Flat	106.5	129.3	50.30	200.5	1.637
Uniformity (%)	4.98	8.28	5.99	4.13	15.58

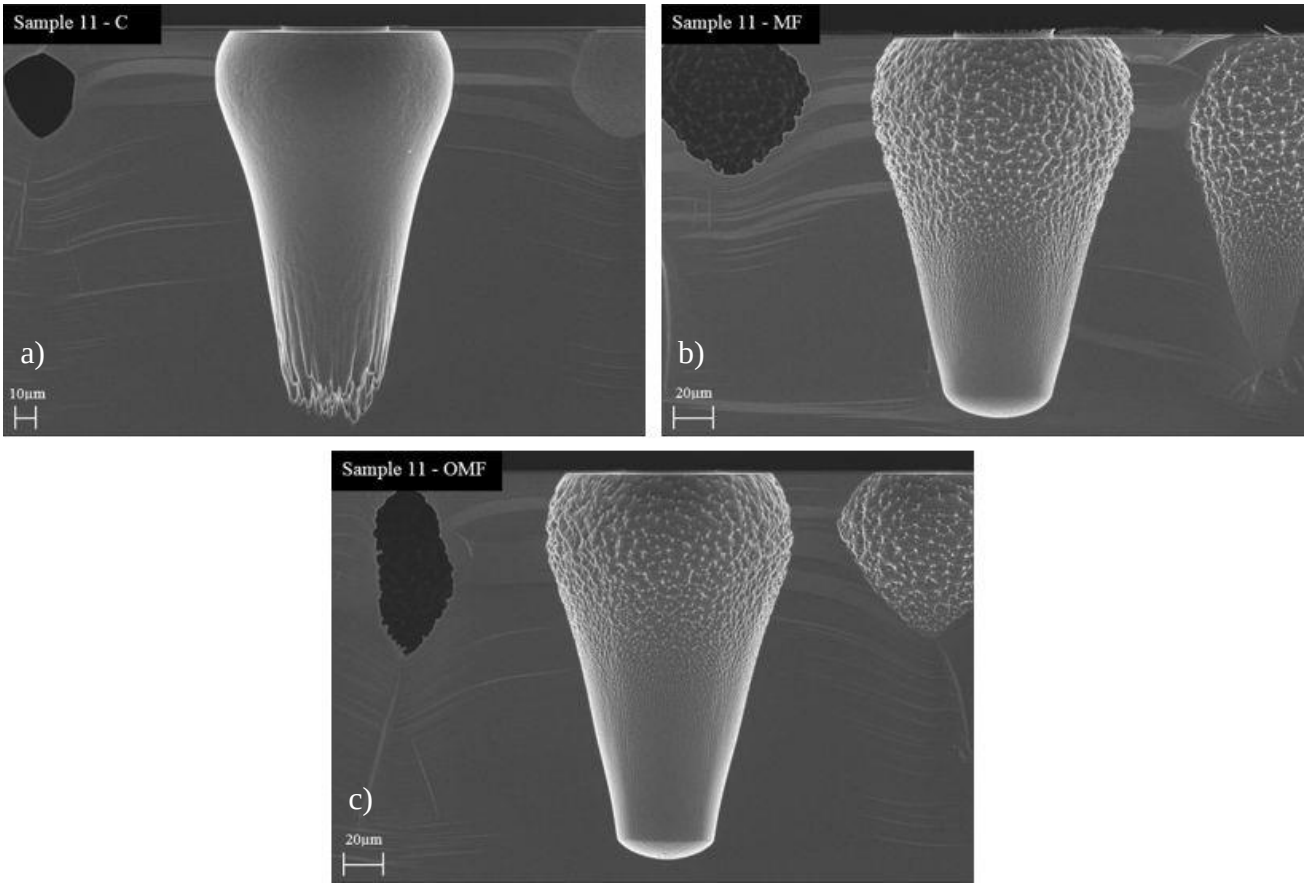


Figure 46: Run 11 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 11 results are shown in Figure 46 and clearly show the effects of high gas flow and bias power, the etch depth is deep and the mask thickness is reduced in comparison to other runs. Overall, the etch profile is good but the centre position shown in Figure 46 (a) has micro masking that has prevented the profile reaching its full depth, and its smaller dimensions when compared to Figure 46 (b) and (c) again showing the edge loading effect.

3.12 Run 12: (= gas flow + coil RF - platen RF - pressure + platen temperature)*

Table 25: Run 12 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	105.7	120.3	30.99	186.9	5.329
Main Flat	115.5	133.3	35.12	157.3	5.043
Opposite Main Flat	111.6	126.5	44.39	167.5	5.236
Uniformity (%)	4.42	5.13	18.19	8.67	2.75

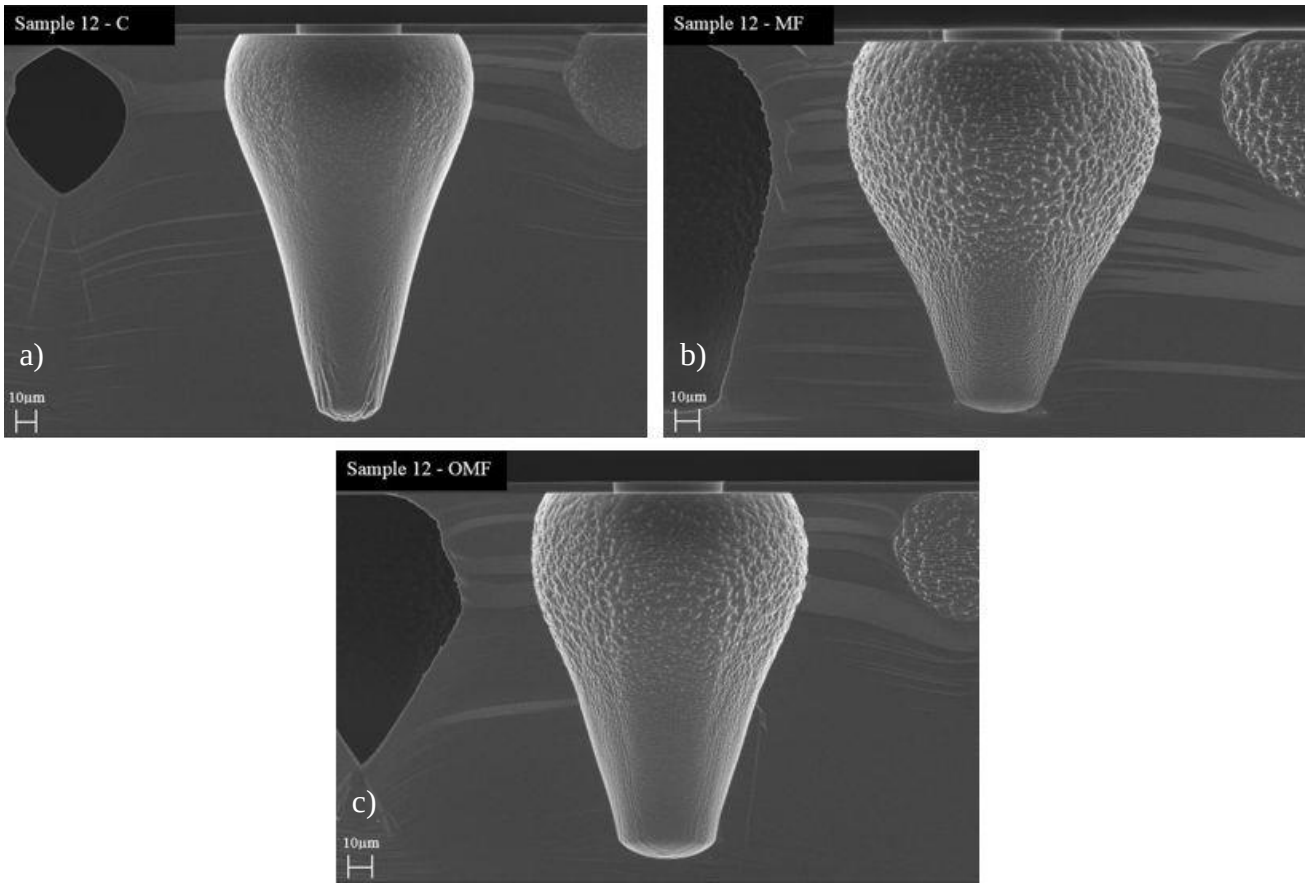


Figure 47: Run 12 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 12 can be compared directly to run 11, the effects reduced bias power and pressure can be seen in Figure 47. The etched profile shapes are wider and shallower when compared to the images in Figure 46, as the passivation layer is not being etched away as quickly which results in the lateral etching component becoming more prevalent, thus increasing the profile width/depth ratio.

3.13 Run 13: (= gas flow + coil RF + platen RF - pressure - platen temperature)*

Table 26: Run 13 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	87.13	102.9	52.05	173.1	1.299
Main Flat	94.82	116.3	63.71	147.2	1.846
Opposite Main Flat	95.22	114.9	57.82	152.1	2.305
Uniformity (%)	4.38	6.01	10.07	8.22	27.68

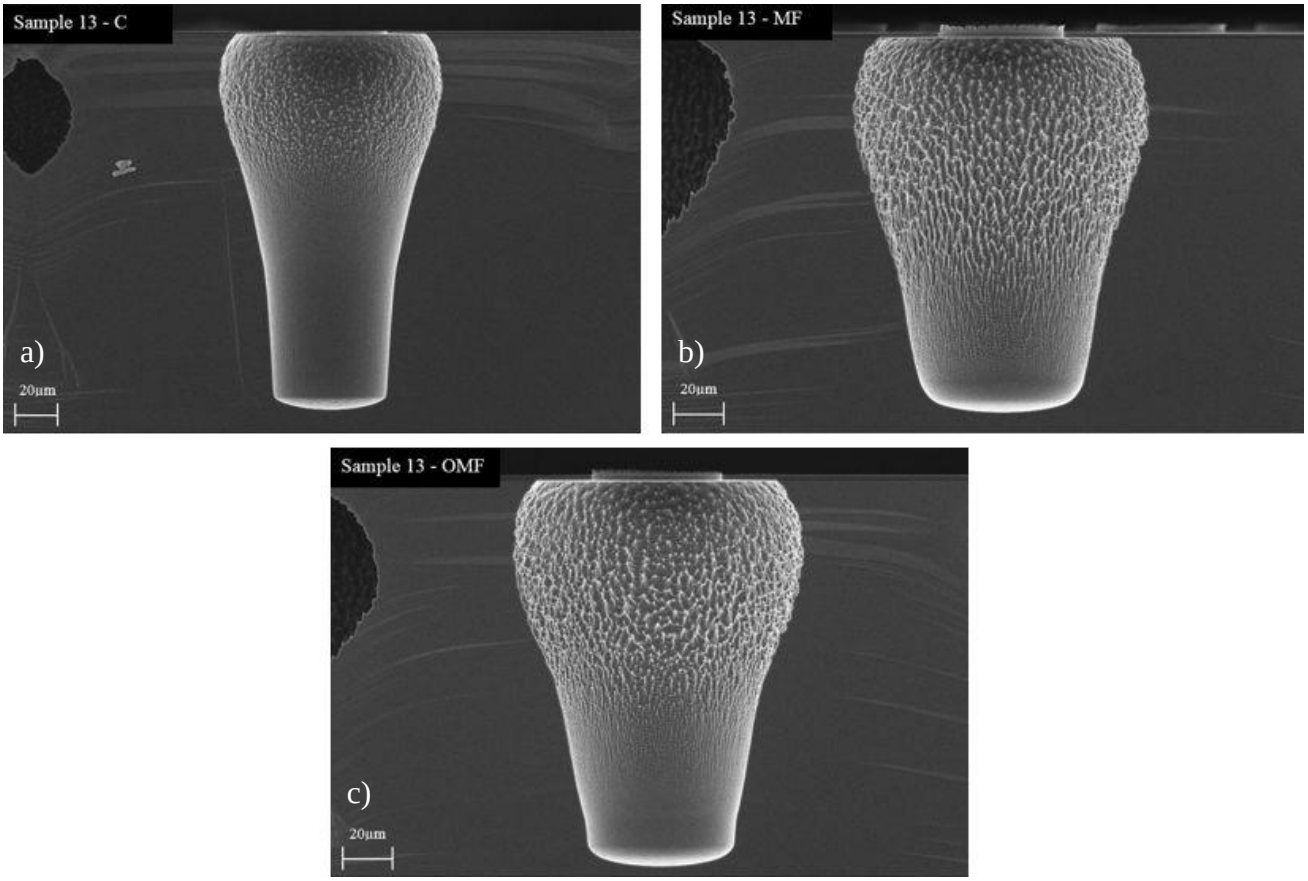


Figure 48: Run 13 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 13 (Figure 48) results are comparable to both runs 11 and 12, the coil and bias RF powers are increased, while the process pressure is decreased, these combined effects are causing large amounts of anisotropic etching which is manifesting as straighter sidewalls, a wider bottom dimension and a less rounded base. The increased power levels and lower pressure are allowing the ions to remove more of the passivation layer on the sidewalls in the area below the maximum width dimension.

3.14 Run 14: (+ gas flow - coil RF + platen RF + pressure = platen temperature)*

Table 27: Run 14 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	102.8	121.1	43.53	191.2	1.421
Main Flat	114.3	139.0	80.14	153.1	0.893
Opposite Main Flat	105.9	132.4	66.61	163.8	1.017
Uniformity (%)	5.34	6.84	28.86	11.25	23.78

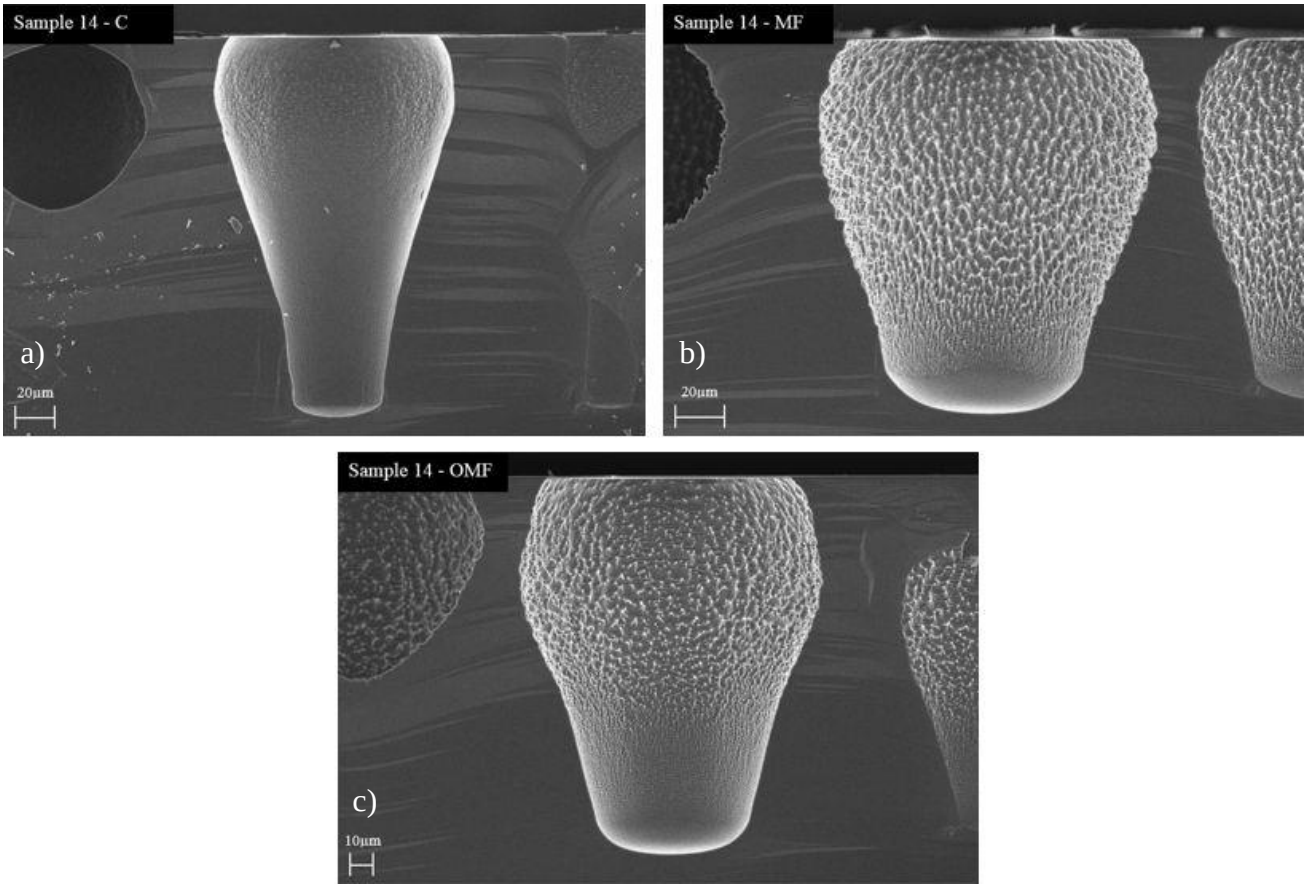


Figure 49: Run 14 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 14 is the start of the maximum gas flow runs which is run in conjunction with low coil and high bias RF power. The effects of this environment can be clearly seen in Figure 49, where the etch profile is deep but is showing large isotropic etch characteristics with the classic ‘strawberry shape’ clearly visible in Figure 49 (b) & (c). Figure 49 (a) is again showing the less dense plasma conditions of the Pegasus source with the etch features in this area having less lateral etching effects.

3.15 Run 15: (= gas flow + coil RF - platen RF - pressure + platen temperature)

Table 28: Run 15 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	96.47	112.3	60.50	165.1	0.502
Main Flat	101.7	124.5	79.88	136.7	1.217
Opposite Main Flat	102.2	122.2	70.21	142.0	1.026
Uniformity (%)	2.86	5.09	13.80	9.59	39.07

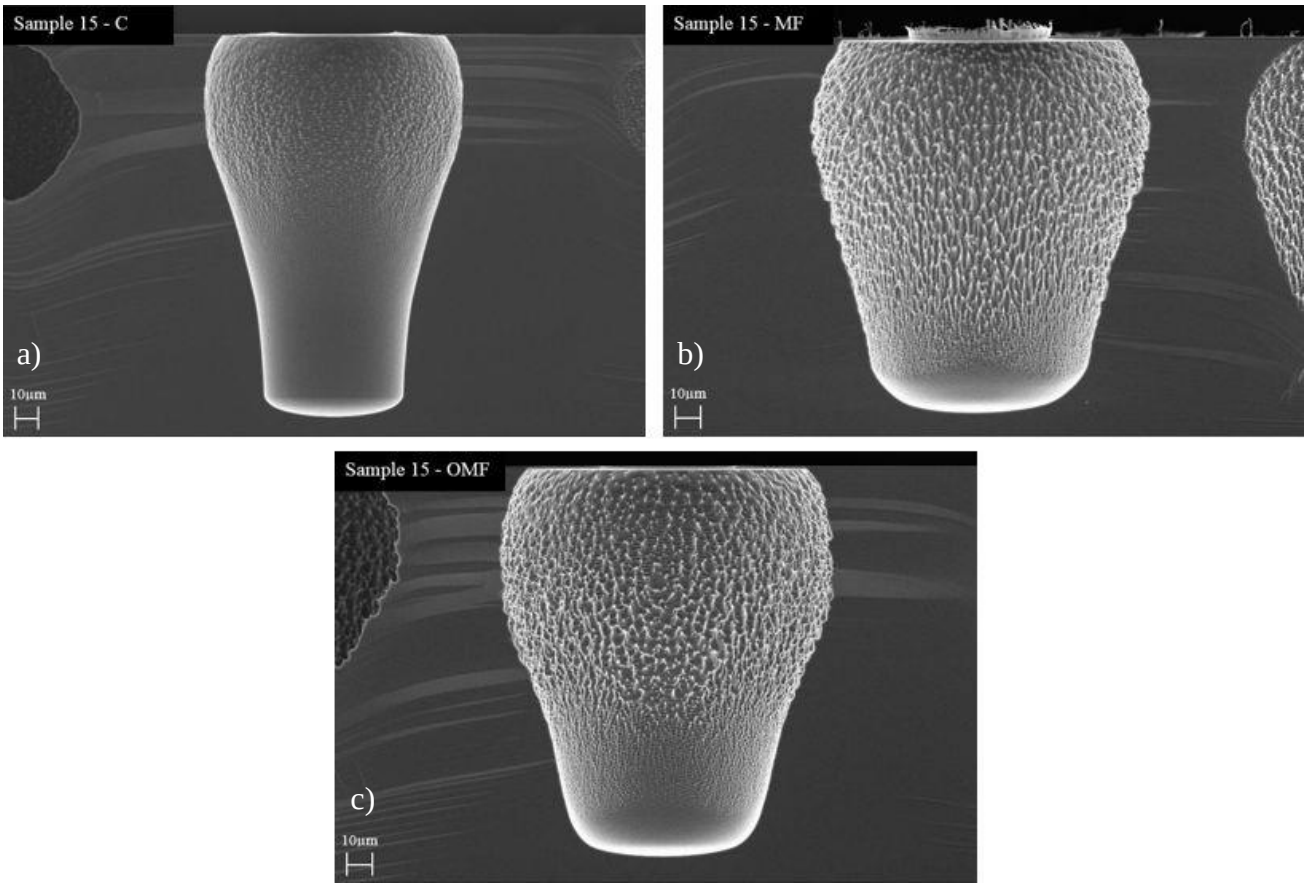


Figure 50: Run 15 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 15 shown in Figure 50 is highlighting the changes in the process conditions between runs 14 and 15, the increase in coil RF power and the reduction in process pressure is producing a similar shape but the profile width dimensions are reducing. The reduction in bias RF power is manifesting as a reduction in profile depth.

3.16 Run 16: (= gas flow + coil RF - platen RF + pressure - platen temperature)*

Table 29: Run 16 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	96.71	107.3	43.73	114.0	5.280
Main Flat	129.0	142.0	46.37	172.2	4.488
Opposite Main Flat	116.9	128.5	48.78	147.1	4.741
Uniformity (%)	14.14	13.78	5.28	20.15	8.18

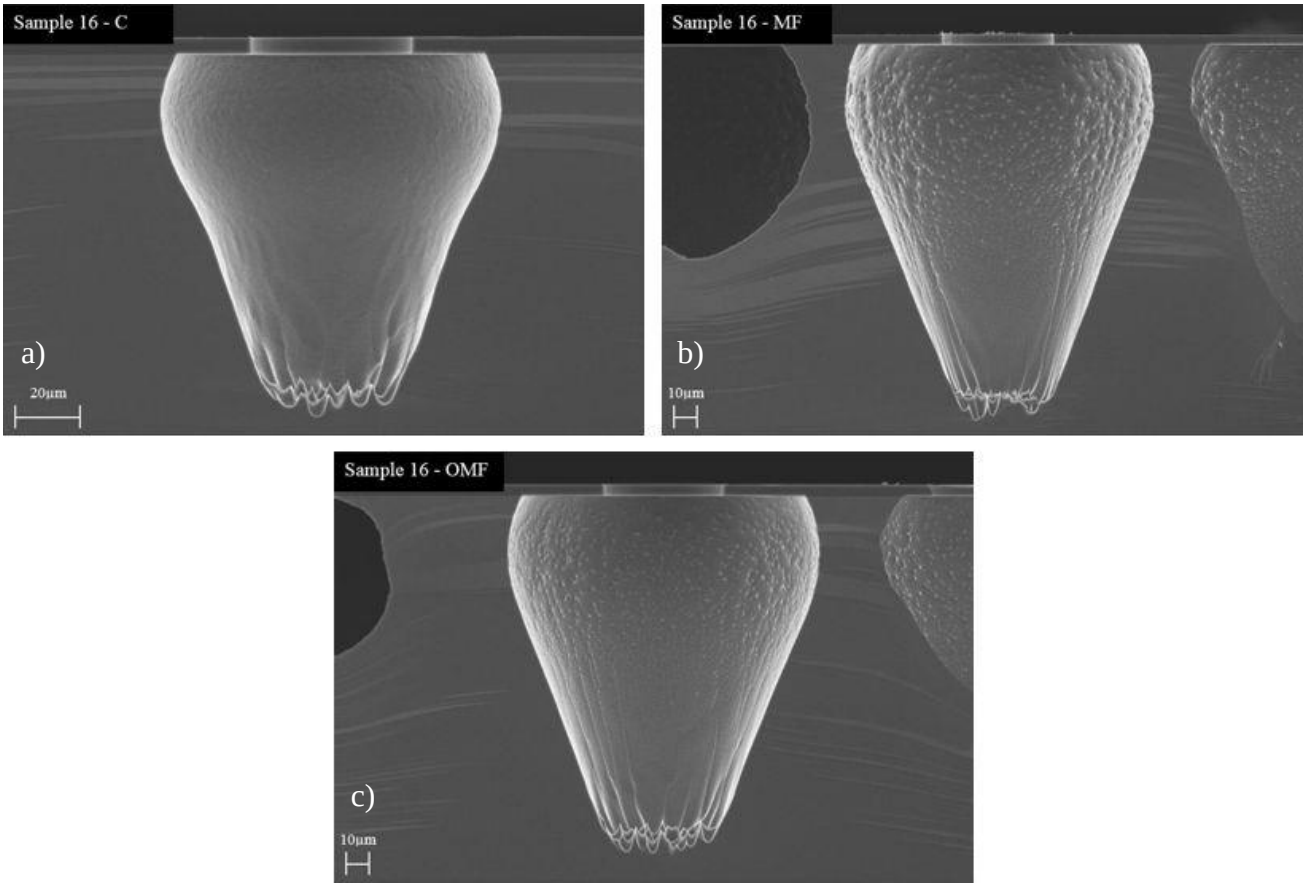


Figure 51: Run 16 Results – a) Centre b) Main Flat c) Opposite Main Flat

Figure 51 shows the results from run 16, the etch profile is significantly less isotropic than the previous two results with a good surface finish, with the area below the maximum width dimension having the desirable straight sidewalls that are needed for TSV applications. The etch is not complete as micro masking can be seen at the bottom of all three profiles, this is likely to be a result of reduction in bias RF power level and platen temperature.

3.17 Run 17: (= gas flow + coil RF - platen RF - pressure + platen temperature)*

Table 30: Run 17 Results

Position	T_W (µm)	M_W (µm)	B_W (µm)	D (µm)	M_T (µm)
Centre	111.4	122.2	43.72	132.0	5.481
Main Flat	129.7	145.0	42.67	175.6	5.154
Opposite Main Flat	132.2	136.8	49.84	162.5	5.141
Uniformity (%)	8.36	8.47	7.89	13.91	3.23

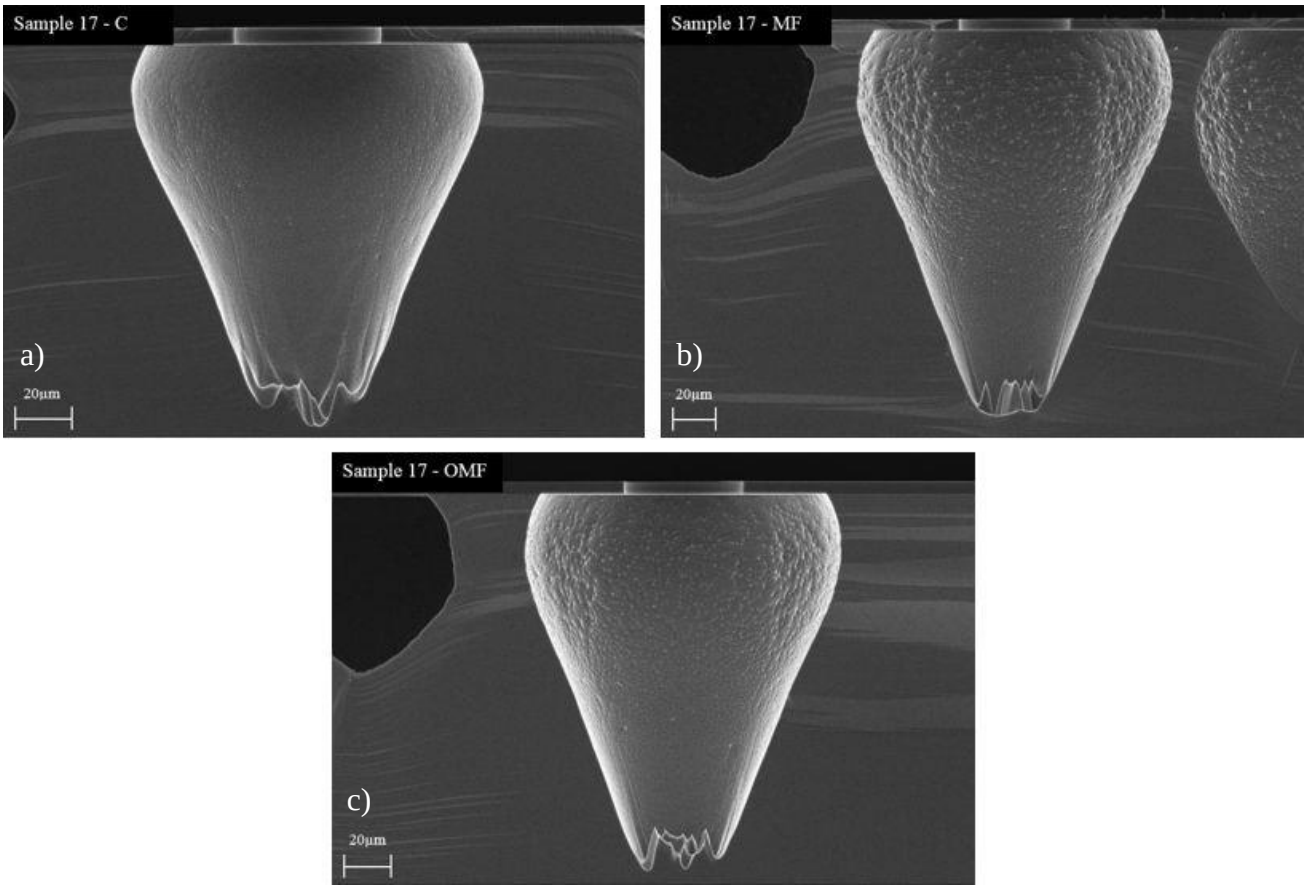


Figure 52: Run 17 Results – a) Centre b) Main Flat c) Opposite Main Flat

Run 17 (shown in Figure 52) is the final run in this DoE and continues the trend of the last two runs, the feature shape is desirable, but the bottom of the profile is showing increased levels of micro masking which is caused by the decrease in bias RF power reducing the downward energy of the ions.

3.18 Results Analysis Interpretation

When the computer model was run, the simulation compared each effect against all others to check for a predictable correlations between parameters, the result of this check is shown in the model response as an R-Square (RSq) value. RSq is a value ranging from 0 to 1, with 0 being no predictable relationship and a value of 1 having a completely predictable correlation.

The model will also indicate the maximum error level of any prediction and this is displayed as a Root Mean Square Error (RMSE) value, this is an estimation of the standard error deviation, with a value of 0 being ideal.

The sorted parameter estimate table shows the model effects presented from top to bottom in order of effect on the defined variables, with the Prob>|t| (p-value) value determining the significance of the results. The Prob>|t| is a number between 0 and 1 and is interpreted in the following way: A small Prob>|t| (typically ≤ 0.05) indicates strong evidence against the null hypothesis (The null hypothesis is an arithmetic theory suggesting that there is no statistical relationship between two sets of measured data [79]) and is considered to show that there is at least one significant effect in the model.

The direction of the bar in the sorted parameter estimate table indicates the expected results from the measured effect, as an example Table 31 shows that the process pressure produces the most significant effect on the centre depth, with the bar located to the left of the centre. This predicts that increasing the process pressure will cause the centre depth to become smaller (shallower), with the length of the bar indicating the magnitude of the effect that changing the pressure will have on the result (longer bar specifies a larger affect)

3.19 Results Analysis

3.19.1 Depth, Centre Position (C)

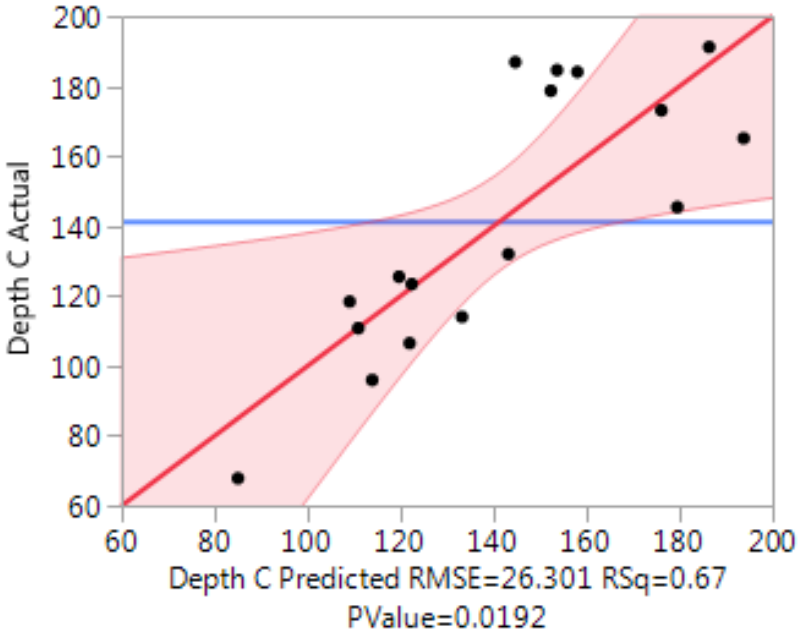


Figure 53: Depth (C) Model Response

Table 31: Depth (C) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	-0.506814	0.155028	-3.27	0.0075*
Total Gas Flow	0.1121785	0.042	2.67	0.0218*
Platen RF Power	0.3218468	0.1671	1.93	0.0803
Coil RF Power	0.012079	0.01671	0.72	0.4849
Platen Temp	-0.073936	0.584851	-0.13	0.9017

Table 31 demonstrates that the feature depth in the centre of the wafer was directly influenced by the interaction between the process pressure and the total gas flow. As the process pressure is raised, the depth of the feature will decrease, while raising the total gas flow will cause the TSV depth to increase. Figure 53 shows an RSq for this model is 0.67 and an RMSE of 26.3, this is a reasonable fit for the calculated results, but the model does not accurately extrapolate results from the data provided.

3.19.2 Depth, Main Flat Position (MF)

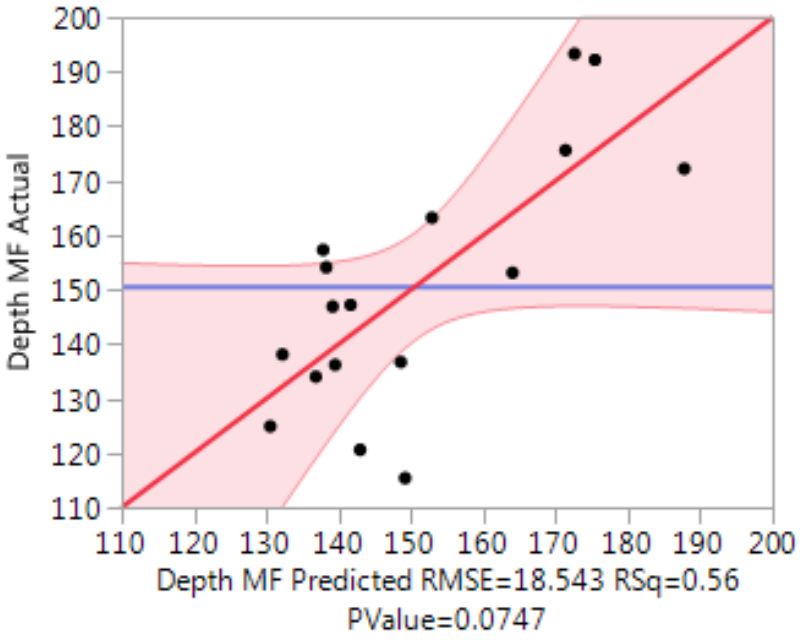


Figure 54: Depth (MF) Model Response

Table 32: Depth (MF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.0793843	0.029612	2.68	0.0214*
Process Pressure	0.1939184	0.109303	1.77	0.1037
Platen Temp	-0.686926	0.41235	-1.67	0.1239
Platen RF Power	0.0785927	0.117814	0.67	0.5185
Coil RF Power	-1.216e-5	0.011781	-0.00	0.9992

Table 32 demonstrates that the feature depth at the main flat of the wafer was directly influenced by the total gas flow. As the gas flow is raised, it will have the effect of causing the TSV depth to increase due to increased numbers of ions and fluorine radicals in the reactor environment.

Figure 54 shows an RSq for this model at 0.56 with an RMSE of 18.54, results with an average fit for the calculated results; the model does not accurately extrapolate results from the data provided.

3.19.3 Depth, Opposite Main Flat Position (OMF)

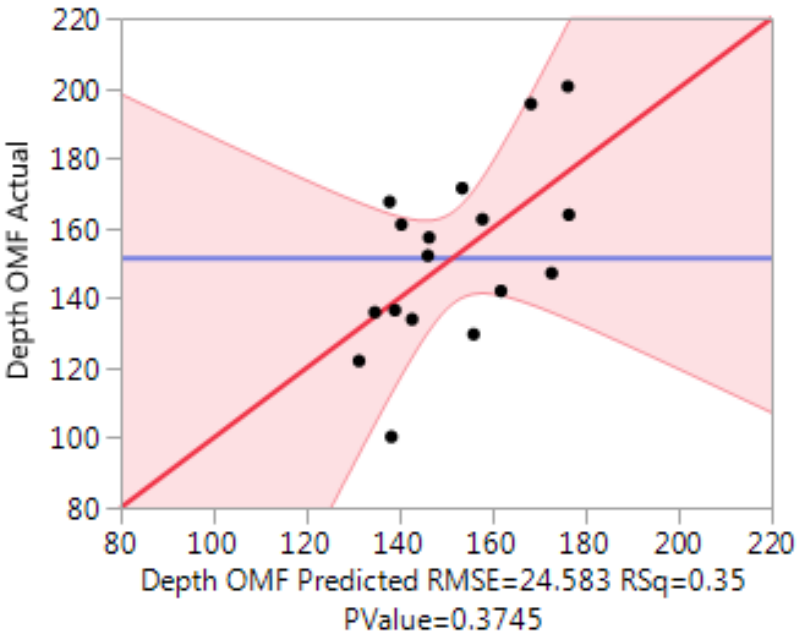


Figure 55: Depth (OMF) Model Response

Table 33: Depth (OMF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.072465	0.039257	1.85	0.0920
Platen RF Power	0.2048356	0.156185	1.31	0.2164
Platen Temp	-0.424076	0.546649	-0.78	0.4542
Process Pressure	0.0609007	0.144902	0.42	0.6824
Coil RF Power	-0.003874	0.015619	-0.25	0.8087

Table 33 shows that the feature depth in the opposite main flat area of the wafer has no obvious direct influences by the data parameters provided, this is likely to be because of the pumping port location which is directly behind this area and will pull etch species away into the pumping system. This is in direct contrast to the MF area which has a definite correlation between raising the gas flow and an increased etch rate.

Figure 55 shows an RSq for this model at 0.35 with an RMSE of 24.58, this is a poor fit for the calculated results, the model cannot extrapolate results from the data provided as there are no predictable parameter interactions.

3.19.4 Depth Uniformity (D Uni)

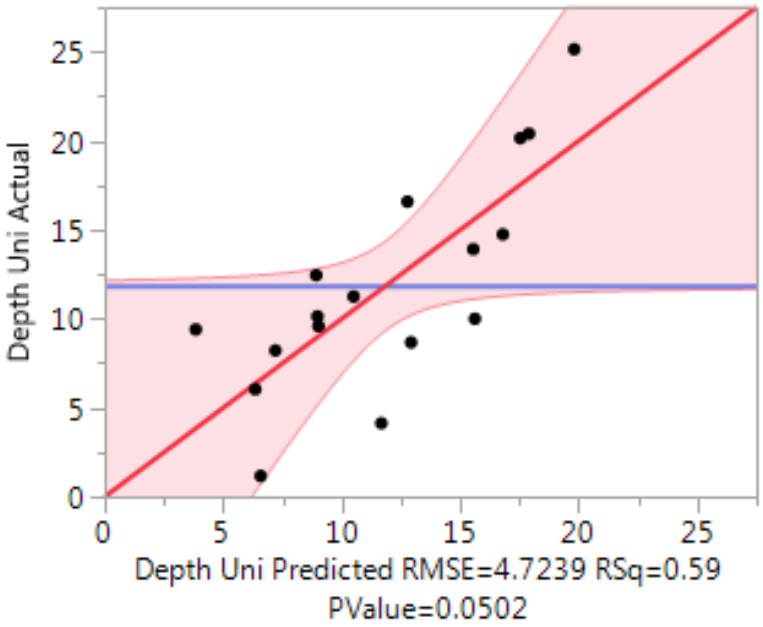


Figure 56: Depth (Uni) Model Response

Table 34: Depth (Uni) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	0.1004911	0.027844	3.61	0.0041*
Platen RF Power	-0.031518	0.030013	-1.05	0.3162
Platen Temp	0.1017858	0.105044	0.97	0.3534
Total Gas Flow	0.0052147	0.007544	0.69	0.5037
Coil RF Power	-0.00168	0.003001	-0.56	0.5868

Table 34 shows that the depth uniformity is directly influenced by process pressure. As the process pressure was raised it causes the across wafer uniformity to increase.

However as shown in Figure 56 the RSq for this model at 0.59 with an RMSE of 7.72, shows an average fit for the calculated results, the model does not accurately extrapolate results from the data provided.

3.19.5 Top Width, Centre Position (C)

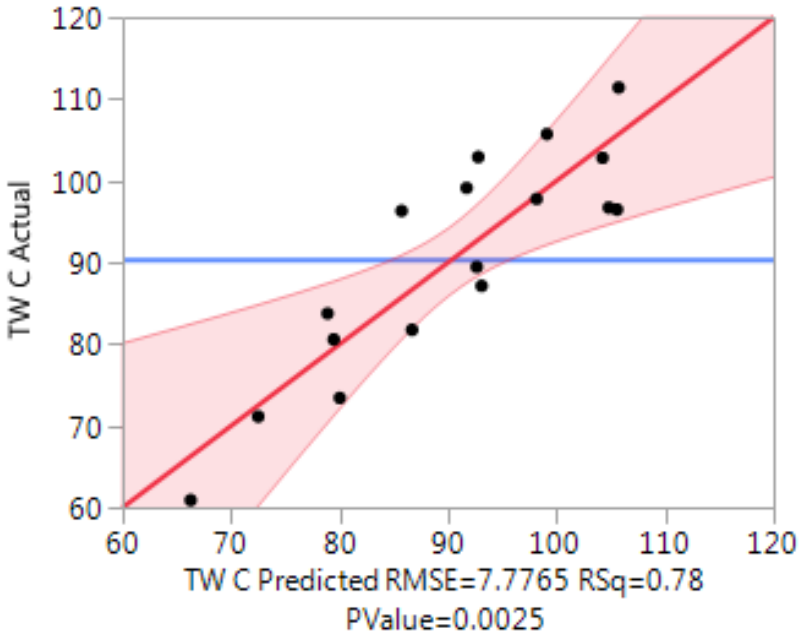


Figure 57: Top Width (C) Model Response

Table 35: Top Width (C) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.0687547	0.012418	5.54	0.0002*
Platen Temp	0.3538403	0.172926	2.05	0.0654
Process Pressure	0.0861244	0.045838	1.88	0.0870
Coil RF Power	0.0006997	0.004941	0.14	0.8899
Platen RF Power	-0.003931	0.049407	-0.08	0.9380

Table 35 states that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow, a value of ~0 Prob>|t| describes an exact correlation between gas flow and the feature top width. As the total gas flow was increased, the dimensions at the top of the TSV will increase.

Figure 57 shows an RSq for this model at 0.78 with an RMSE of 7.78, this indicates a good fit for the calculated results; the model will predict results from the data provided with a good level of accuracy.

3.19.6 Top Width, Main Flat Position (MF)

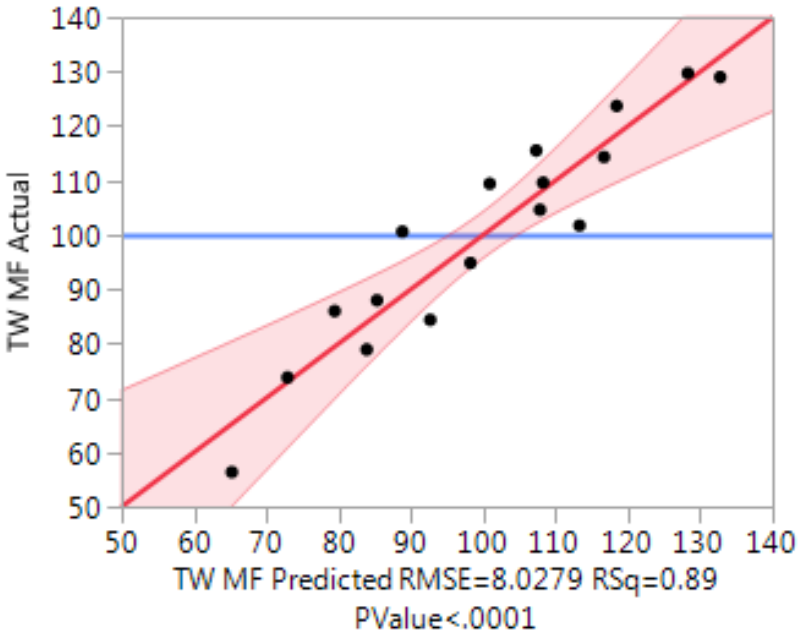


Figure 58: Top Width (MF) Model Response

Table 36: Top Width (MF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.1055219	0.01282	8.23	<.0001*
Process Pressure	0.2170433	0.04732	4.59	0.0008*
Platen Temp	0.1884079	0.178516	1.06	0.3139
Platen RF Power	-0.027655	0.051005	-0.54	0.5985
Coil RF Power	0.0007659	0.0051	0.15	0.8833

Table 36 shows that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow and process pressure, with the values of both very close to ~0 Prob>|t| this scenario describes an almost exact correlation between gas flow, process pressure and the feature top width. As the total gas flow and pressure were increased the dimensions at the top of the TSV also increases.

Figure 58 shows an RSq for this model at 0.89 with an RMSE of 8.03, this indicates a good fit for the calculated results; the model will extrapolate results from the data provided with a good level of accuracy.

3.19.7 Top Width, Opposite Main Flat Position (OMF)

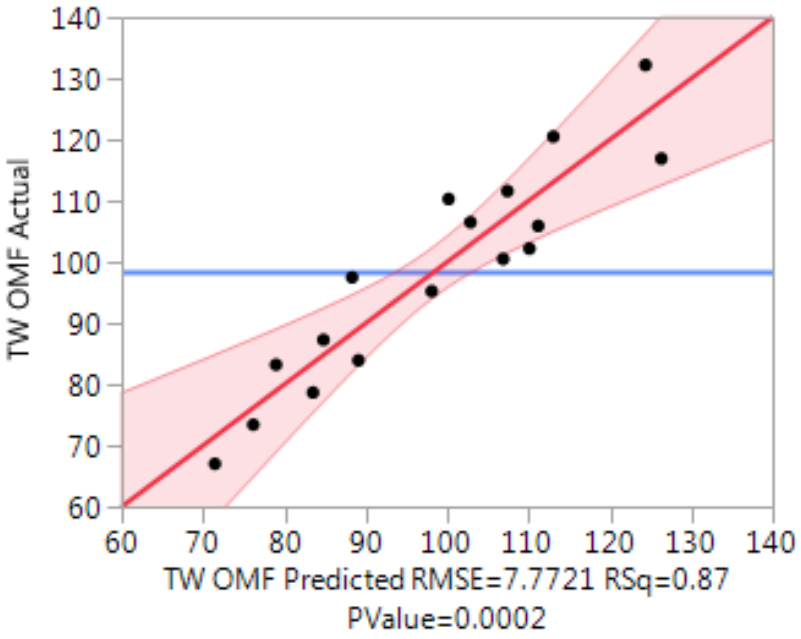


Figure 59: Top Width (OMF) Model Response

Table 37: Top Width (OMF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.0908294	0.012411	7.32	<.0001*
Process Pressure	0.1743475	0.045812	3.81	0.0029*
Platen RF Power	-0.066671	0.04938	-1.35	0.2041
Platen Temp	0.17785	0.172828	1.03	0.3256
Coil RF Power	0.00012	0.004938	0.02	0.9810

Table 37 demonstrates that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow and process pressure, with an almost exact correlation between gas flow, process pressure and the feature top width. It is interesting to note that the positions at the outside of the substrate are consistent with each other, but the centre features are affected less by process pressure and more by platen temperature.

Figure 59 shows an RSq for this model at 0.87 with an RMSE of 7.77, this indicates a good fit for the calculated results; the model will extrapolate results from the data provided with a good level of accuracy.

3.19.8 Top Width, Uniformity (TW Uni)

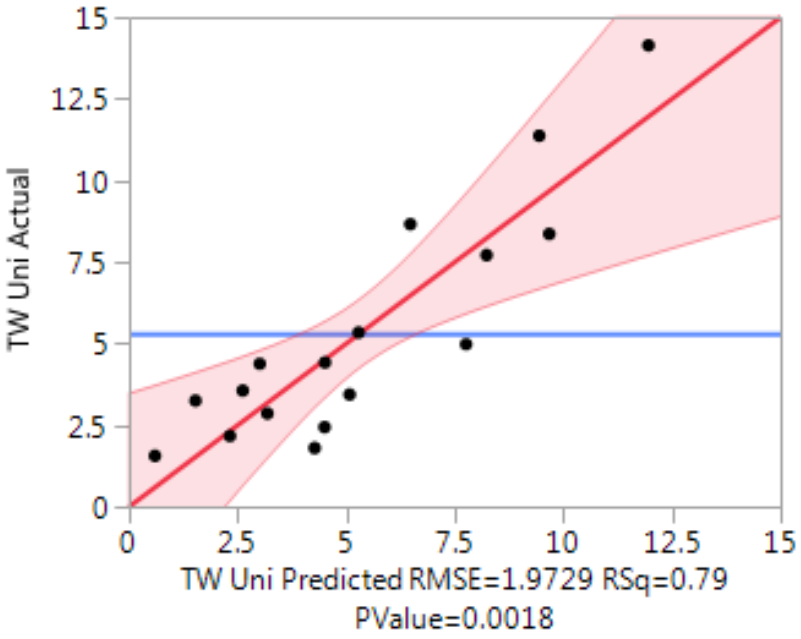


Figure 60: Top Width (Uni) Model Response

Table 38: Top Width (Uni) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Platen Temp	-0.144403	0.043872	-3.29	0.0072*
Process Pressure	0.0364413	0.011629	3.13	0.0095*
Total Gas Flow	0.0096627	0.003151	3.07	0.0107*
Platen RF Power	-0.032672	0.012535	-2.61	0.0244*
Coil RF Power	-0.002024	0.001253	-1.61	0.1346

Table 38 shows that there are multiple factors directly influencing the across wafer uniformity of the top width dimension of the TSV. Platen temperature and platen RF make the uniformity more consistent across the wafer when their values are lowered with the model accurately predicting this effect, whereas process pressure and total gas flow have the opposite effect albeit with a little less certainty

Figure 60 shows an RSq for this model at 0.79 with an RMSE of 2, this indicates a good fit for the calculated results, the model will extrapolate results from the data provided with a good level of accuracy.

3.19.9 Maximum Width, Centre Position (C)

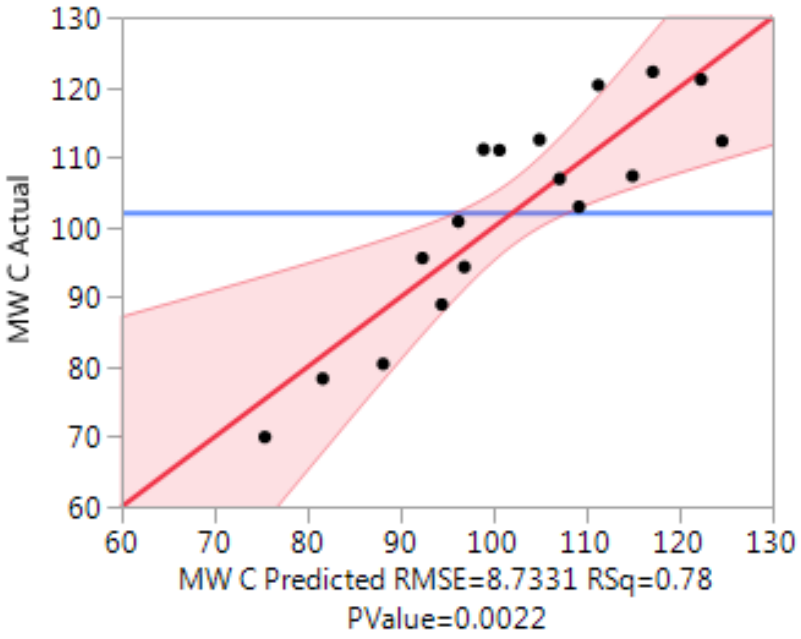


Figure 61: Max Width (C) Model Response

Table 39: Max Width (C) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.0834065	0.013946	5.98	<.0001*
Platen Temp	0.3606643	0.194198	1.86	0.0902
Platen RF Power	0.0411041	0.055485	0.74	0.4743
Process Pressure	0.0180889	0.051477	0.35	0.7319
Coil RF Power	0.0018176	0.005549	0.33	0.7494

Table 39 demonstrates that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow, a value of ~0 Prob>|t| indicates an exact correlation between gas flow and the feature maximum width. As the total gas flow was increased the maximum width of the TSV will increase.

Figure 61 shows an RSq for this model at 0.78 with an RMSE of 8.73, this indicates a good fit for the calculated results, the model will extrapolate results from the data provided with a good level of accuracy.

3.19.10 Maximum Width, Main Flat Position (MF)

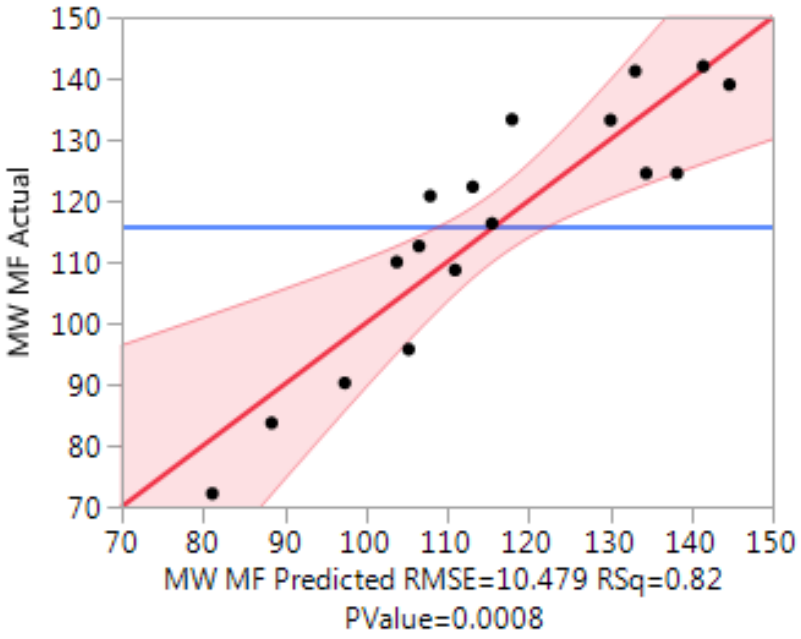


Figure 62: Max Width (MF) Model Response

Table 40: Max Width (MF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.1116851	0.016733	6.67	<.0001*
Process Pressure	0.1122694	0.061765	1.82	0.0964
Platen RF Power	0.1000958	0.066575	1.50	0.1609
Platen Temp	0.1513352	0.233012	0.65	0.5294
Coil RF Power	-0.003105	0.006657	-0.47	0.6501

Table 40 demonstrates that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow, a value of ~0 Prob>|t| shows an exact correlation between gas flow and the feature maximum width. As the total gas flow was increased the maximum width of the TSV increases.

Figure 62 shows an RSq for this model at 0.82 with an RMSE of 10.50, this indicates a good fit for the calculated results, the model will extrapolate results from the data provided with a good level of accuracy.

3.19.11 Maximum Width, Opposite Main Flat Position (OMF)

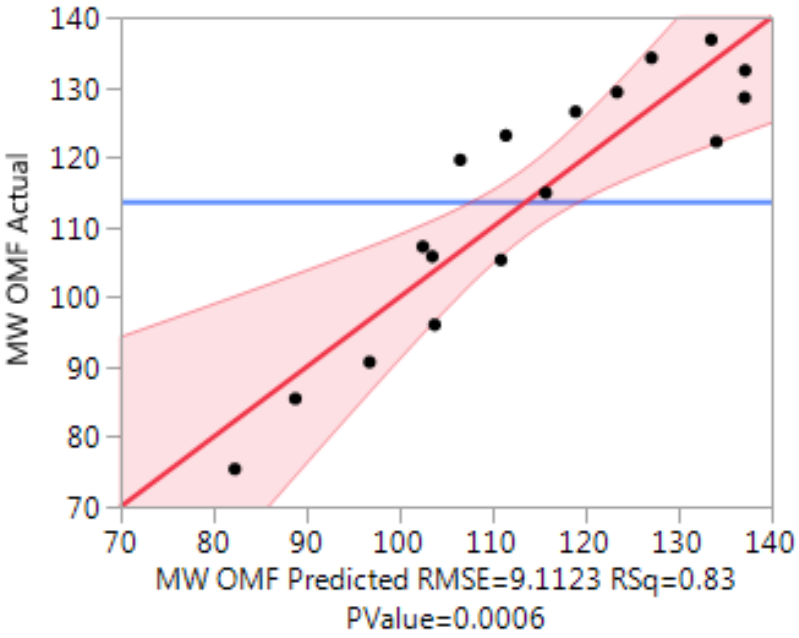


Figure 63: Max Width (OMF) Model Response

Table 41: Max Width (OMF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Total Gas Flow	0.1018807	0.014551	7.00	<.0001*
Process Pressure	0.0983631	0.053711	1.83	0.0942
Platen Temp	0.1910615	0.202629	0.94	0.3660
Platen RF Power	0.0528747	0.057894	0.91	0.3807
Coil RF Power	-0.000584	0.005789	-0.10	0.9215

Table 41 demonstrates that the feature depth at the main flat of the wafer is strongly influenced by the total gas flow, a value of ~0 Prob>|t| describes an exact correlation between gas flow and the feature maximum width. As the total gas flow was increased the maximum width of the TSV increases.

Figure 63 shows an RSq for this model at 0.83 with an RMSE of 9.11, this indicates a good fit for the calculated results, the model will extrapolate results from the data provided with a good level of accuracy.

3.19.12 Maximum Width, Uniformity (MW Uni)

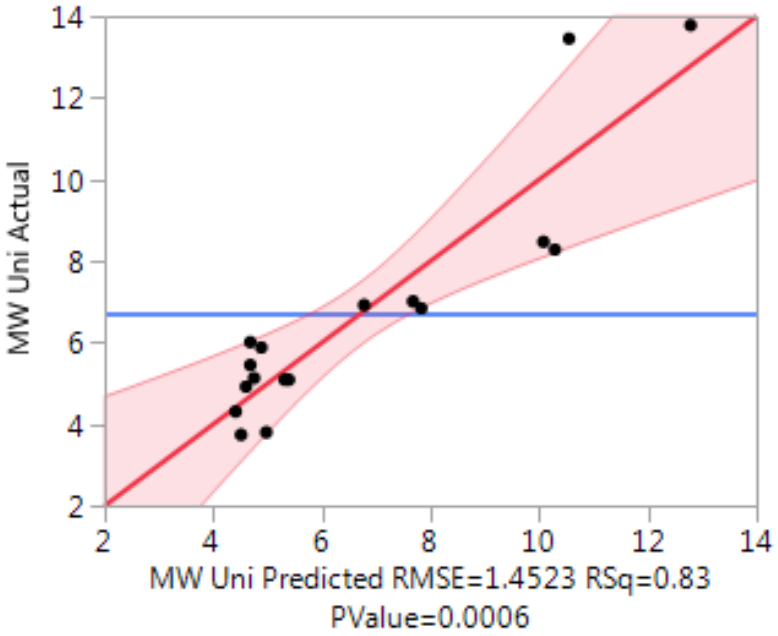


Figure 64: Maximum Width (Uni) Model Response

Table 42: Maximum Width (Uni) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	0.0381832	0.00856	4.46	0.0010*
Total Gas Flow	0.0103107	0.002319	4.45	0.0010*
Platen Temp	-0.116127	0.032294	-3.60	0.0042*
Coil RF Power	-0.000421	0.000923	-0.46	0.6572
Platen RF Power	0.0018066	0.009227	0.20	0.8483

Table 42 shows there are multiple factors that directly influence the across wafer uniformity of the max width dimension, platen temperature makes the size of the non-uniformity more consistent when its value is lowered, whereas the process pressure and total gas flow have the opposite effect, when their values were raised the maximum width uniformity was made more uniform.

Figure 64 shows an RSq for this model at 0.83 with an RMSE of 1.45, this indicates an excellent fit for the calculated outcome, the model will extrapolate results from the data provided with a high level of accuracy.

3.19.13 Bottom Width, Centre Position (C)

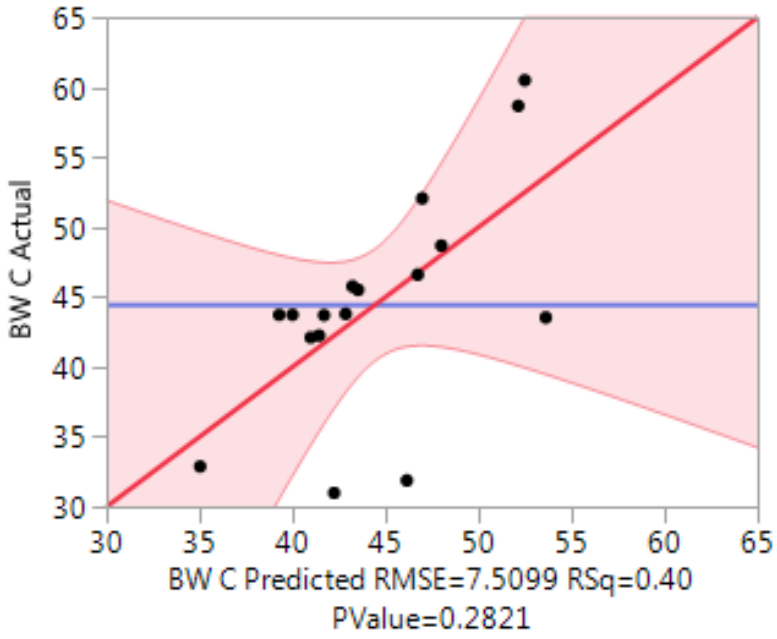


Figure 65: Bottom Width (C) Model Response

Table 43: Bottom Width (C) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	-0.082374	0.044266	-1.86	0.0897
Platen RF Power	0.0825242	0.047713	1.73	0.1116
Total Gas Flow	0.0095523	0.011993	0.80	0.4426
Coil RF Power	-0.001916	0.004771	-0.40	0.6957
Platen Temp	-0.004465	0.166996	-0.03	0.9791

Table 43 demonstrates that the bottom width dimension in the centre of the wafer may be influenced by the process pressure. As the process pressure is raised the size of this feature element will decrease, but the interaction between process pressure and bottom width at the centre of the wafer is minimal.

Figure 65 shows an RSq for this model is 0.4 and an RMSE of 7.5, this is a poor fit for the calculated results, and the model will not accurately extrapolate results from the data provided.

3.19.14 Bottom Width, Main Flat Position (MF)

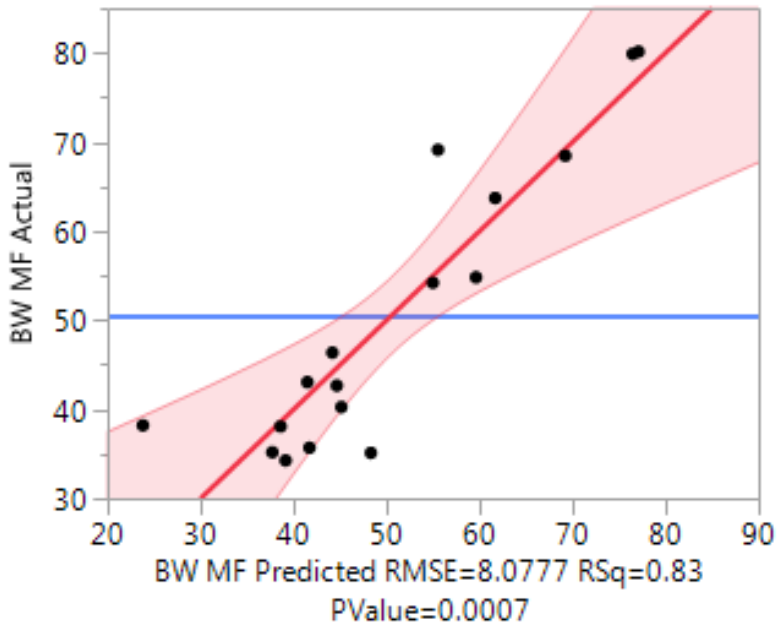


Figure 66: Bottom Width (MF) Model Response

Table 44: Bottom Width (MF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	-0.222706	0.047613	-4.68	0.0007*
Platen RF Power	0.2033159	0.051321	3.96	0.0022*
Total Gas Flow	0.0495903	0.012899	3.84	0.0027*
Coil RF Power	-0.000916	0.005132	-0.18	0.8617
Platen Temp	0.0116556	0.179622	0.06	0.9494

Table 44 shows that there are multiple factors that directly influence the bottom width of the feature at the main flat position, process pressure makes the dimension smaller when its value is increased, whereas the platen RF power and total gas flow will have the opposite effect, where the size of the feature is increased as their values are raised.

Figure 66 shows an RSq for this model at 0.83 with an RMSE of 8, this indicates an excellent fit for the calculated outcome, the model will extrapolate results from the data provided with a high level of accuracy.

3.19.15 Bottom Width, Opposite Main Flat Position (OMF)

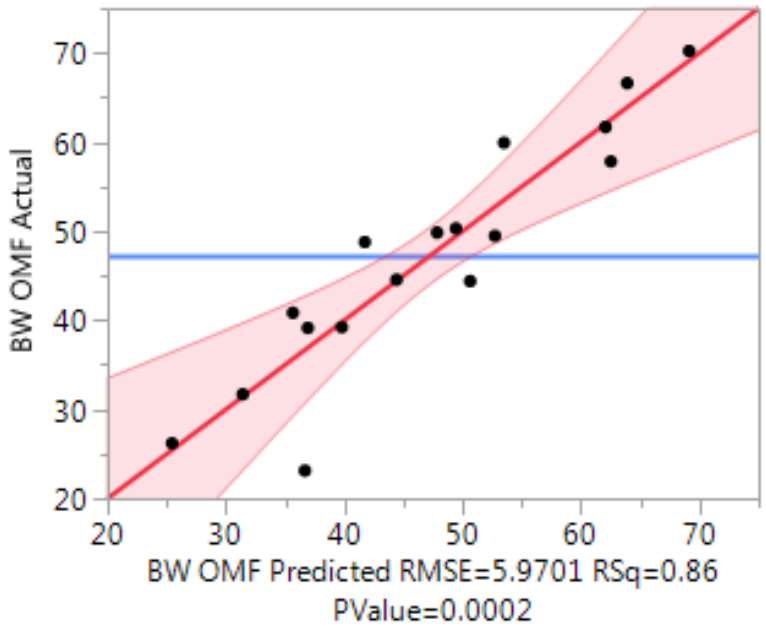


Figure 67: Bottom Width (OMF) Model Response

Table 45: Bottom Width (OMF) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Process Pressure	-0.174723	0.03519	-4.97	0.0004*
Total Gas Flow	0.0419234	0.009534	4.40	0.0011*
Platen RF Power	0.1535049	0.037931	4.05	0.0019*
Coil RF Power	0.0094891	0.003793	2.50	0.0294*
Platen Temp	0.204267	0.132757	1.54	0.1521

Table 45 shows that there are multiple factors that directly influence the bottom width of the feature at the opposite main flat position, process pressure makes the dimension smaller as its value was increased, whereas the platen RF power and total gas flow have the opposite effect, where the size of the feature was increased as their values are raised. Coil RF power also influences the size of the feature, but its influence is much smaller than the other three parameters.

Figure 67 shows an RSq for this model at 0.86 with an RMSE of 6, this indicates an excellent fit for the calculated outcome, the model will extrapolate results from the data provided with a high level of accuracy.

3.19.16 Bottom Width, Uniformity (BW Uni)

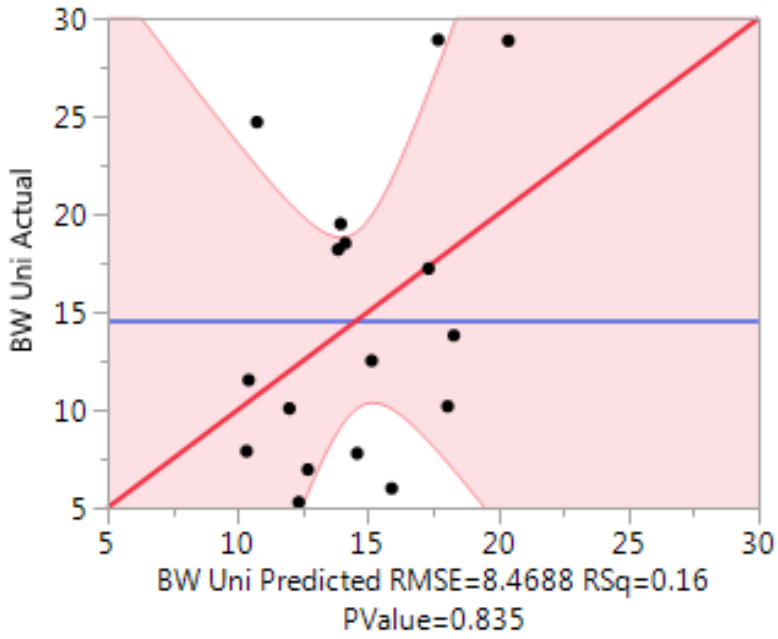


Figure 68: Bottom Width (Uni) Model Response

Table 46: Bottom Width (Uni) Sorted Parameter Estimate

Term	Estimate	Std Error	t Ratio	Prob>|t|
Coil RF Power	-0.007143	0.005381	-1.33	0.2112
Process Pressure	-0.017291	0.049918	-0.35	0.7356
Total Gas Flow	0.0034691	0.013524	0.26	0.8023
Platen RF Power	0.0134835	0.053806	0.25	0.8067
Platen Temp	0.0358923	0.188319	0.19	0.8523

Table 46 demonstrates that the bottom width uniformity across the wafer may be influenced by the coil RF power. As you raise the coil RF power the non-uniformity across the wafer will increase, but the interaction between the RF power and the uniformity is minimal at best.

Figure 68 shows an RSq for this model is 0.16 and an RMSE of 8.4, this shows that that the model cannot predict the resulting bottom width uniformity from the information provided by the samples.

3.20 Prediction Profiler

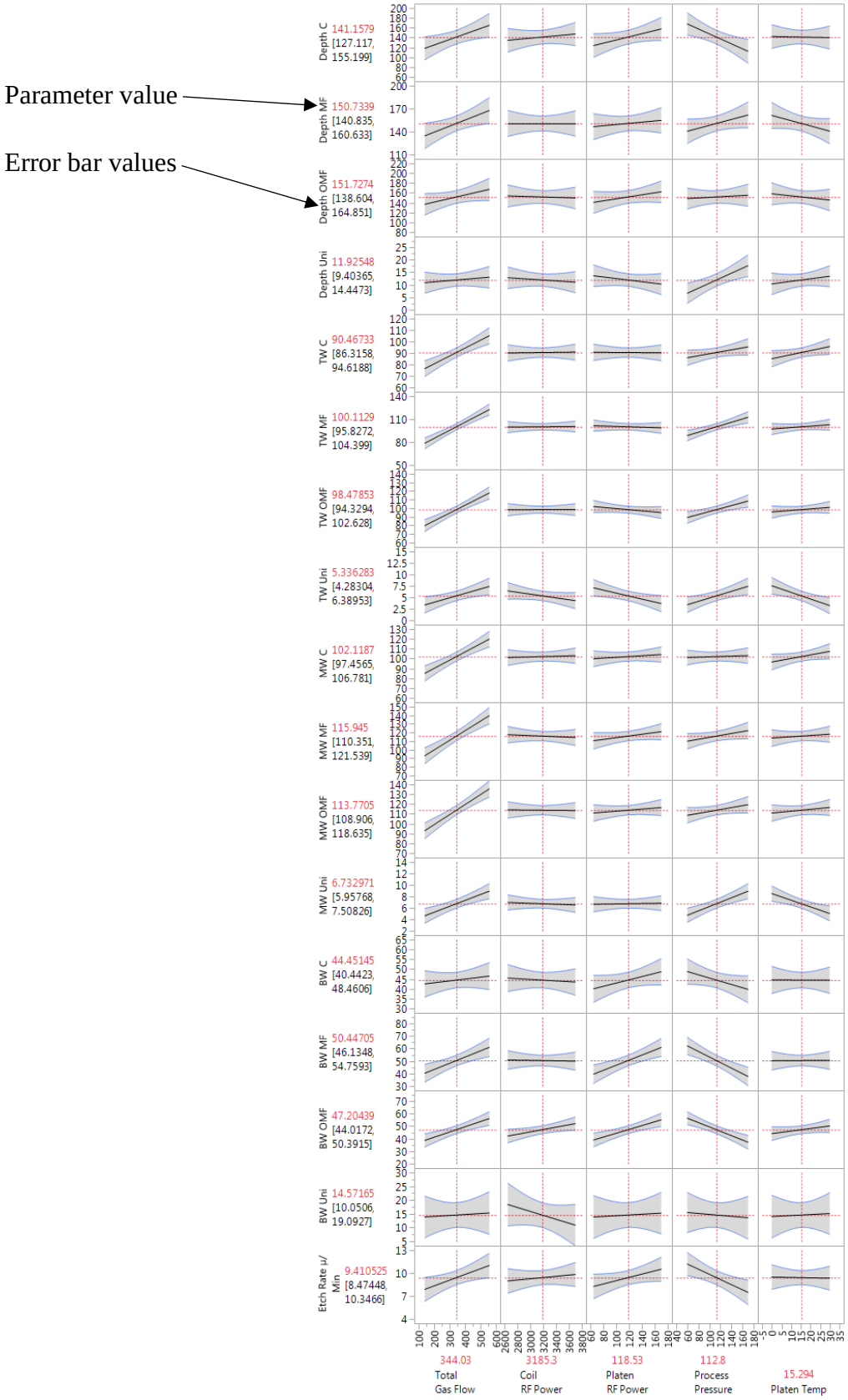


Figure 69: Prediction Profiler

The prediction profiler shown in Figure 69 provides an overview of the model results at a single glance, additionally it acts as a guide to predict changes to the feature dimensions if any of the parameters used in the construct model effects are adjusted. For example, increasing the total gas flow will cause the MW C dimension size to increase rapidly (as indicated by the bar slope), but the same change will have a negligible effect of the BW Uni, conversely increasing the coil power will have almost no effect on MW C but will cause the BW Uni to decrease rapidly.

The prediction profiler can be a useful tool for indicating a path for further optimisation of the device profile, measurements of the sample results will show how far away the TSV shape is from the ideal results and whether the dimensions are inside or outside of proscribed tolerances. Comparing the actual results to the trends shown in Figure 69 will give an idea of how the process conditions can be tuned to achieve the desired product.

As the table clearly shows, each of the process parameters have their own effects on the resulting profile, so consideration must be given to the idea that more than one variable may need to be adjusted to provide the desired outcome. Additionally, it should be noted that adjusting a parameter to tune out one undesirable profile characteristic is likely to influence other areas of the profile, the likely outcome of this is that a balancing act or compromise may be needed to produce a profile that will fit the project requirements but may not be the ideal shape.

There was no objective in this project to investigate the ideal process conditions that would produce the most desirable TSV shape for the baseline process results that are shown in run 1 (Figure 36), however it may be possible to increase the size of the top width dimension to produce a shape that has straighter edges and is closer to the ideal shape. The prediction profiler suggests that increasing the process pressure will have the effect of enlarging the top width dimension, whilst leaving the maximum width dimension largely unchanged, which would be a desirable outcome. Although the profiler also suggests that this change is likely to reduce the overall final depth of the features, additionally it is

probable that this change will make the bottom width dimension smaller and may help the researcher get closer to the ideal profile shape, but this is not guaranteed as the slope may become too oblique.

Overall, the strongest trend shown by the profiler is that variations in the total gas flow have the greatest overall effect on the TSV profile, the trend is generally that an increase in this value is likely to enlarge every measured parameter on the TSV. The other process parameter changes tend to have a mixture of results with some areas of the shape increasing, decreasing, or having no response to the same parameter adjustment.

One change that is worth noting is that increases in platen temperature seem to lower the overall across wafer non uniformity of the top and maximum width dimensions but have little to no effect on most of the other profile measurements, this is a desirable characteristic and an area that is worth further consideration.

Chapter 4 – Computer Modelling

This chapter presents the results from computer modelling trials that were used to identify if there are any statistically relevant effects that are present because of the cooling fluid temperature distribution resulting from the design of the cooling channels located within the body of the electrostatic wafer platform.

4.1 Substrate Platform Cooling Simulation

Observations of the test sample SEM images that are displayed in every one of the process runs shown in the results section, clearly show that the TSV test profiles in the centre of the substrate exhibit radically different geometries to those located at the edge, with both the depth and width of the profiles being strongly dependent on the location of the feature. Unfortunately, the variations in the feature dimensions cannot be predicted as the differences are highly variable, for example Run 1 in the results section shows that the measurements taken at the edge of the wafer have features with greater width and less depth than measurements taken at the centre. However, measurements made in Run 4 in the results section show that these variations have reversed and observations at the centre are showing less depth and greater width when compared to the edge of the substrate.

To identify the possible causes of the profile variations across the substrate, a computer modelling study of the electrostatic chuck assembly that was installed into the etch reactor used for this trial, was performed to ascertain if the effects were a direct result of the plasma variations within the Pegasus process reactor or a product of temperature variations within the temperature-controlled fluid circulating inside the electrostatic wafer platform (Esc).

The temperature control of the substrate platform is achieved by circulating fluid within a closed loop circuit.

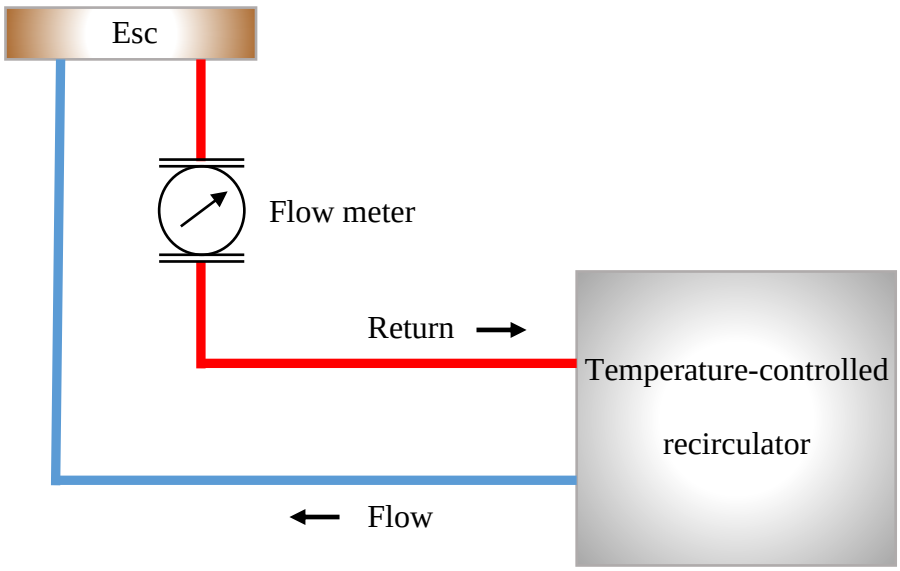


Figure 70: Substrate Platform Cooling Circuit

The temperature-controlled recirculator (chiller) used in the circuit is an SMC® Thermo Chiller™, model HRZ-001, with a temperature range of -20°C to +40°C and a temperature stability of ±0.1°C, using Galden™ HT170 as the cooling fluid.

During the process run the substrate is clamped firmly to the Esc via an electrostatic charge and pressurised helium (He) maintained at set value between 10Torr and 20Torr is injected into the space between the top of the platen and the back surface of the wafer to function as a heat transfer medium.

The platen and wafer were simulated, using the COMSOL Multiphysics® software platform using similar conditions to those present in the reactor during an average process run, allowing the temperature distribution on the surface of the substrate to be modelled. The values for thermal conductivity and wafer surface heat influx of the materials used in the simulation are shown in Table 47, and the simulation was carried out with platen temperature values set at 10°C, 20°C and 30°C. The thermal conductivity of the helium backside cooling (HBC) gas was set at values of 0.05W/mK, 0.075W/mK and 0.1W/mK (W/mK is a value of thermal conductivity and specifies the rate of heat transfer in any homogeneous material) to simulate the changing cooling effects produced by raising the HBC pressure between 10Torr, 12.5Torr and 15Torr [80] (the thermal conductivity values are not precisely known and were estimated to show the potential impact on the temperature distribution).

Table 47: Comsol Simulation Values

Parameter	Value
Heat influx (wafer surface)	1500W*
Thermal conductivity of Alumina	29.3(W/mK)
Thermal conductivity of RTV	0.27(W/mK)
Thermal conductivity of Aluminium	205(W/mK)

*1500W estimation is based upon the maximum heat load of the Pegasus process module of 2000W at full RF power

4.2 Cooling Simulation Results

Figure 71 shows the simulated results for platen temperatures at 10°C (a) and 30°C (b) when the process conditions are set to the values listed in Table 7, the images show that there are no changes to the temperature distribution indicated outside of the expected incremental increases.

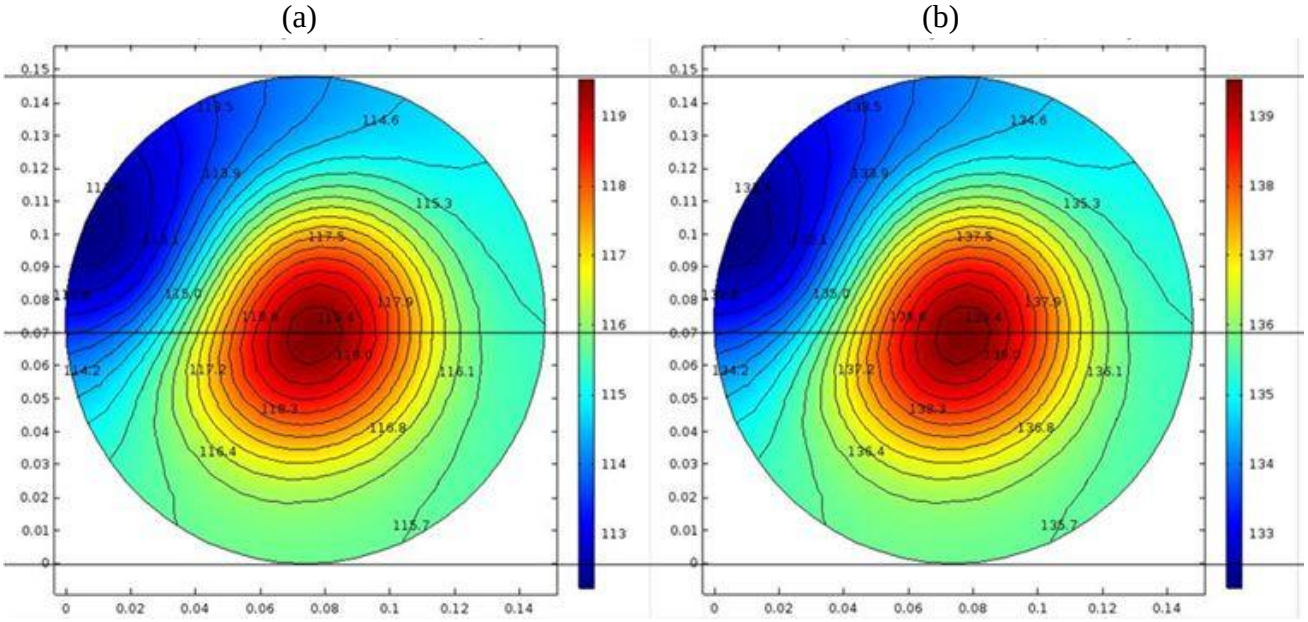


Figure 71: Simulation Temperature Distribution Results

Figure 72 illustrates the impact of changing the HBC conductivity from 0.05 W/mK (a) to 0.075 W/mK(b) and 0.1 W/mK (c). The simulation shows that there is approximately 1°C lowering of the substrate surface temperature when changing from the lowest to highest conductivity values, but the distribution pattern remains similar. The lack of radial symmetry in the heat distribution is caused by the position of the cooling channel inlet and outlet positions as shown in Figure 73.

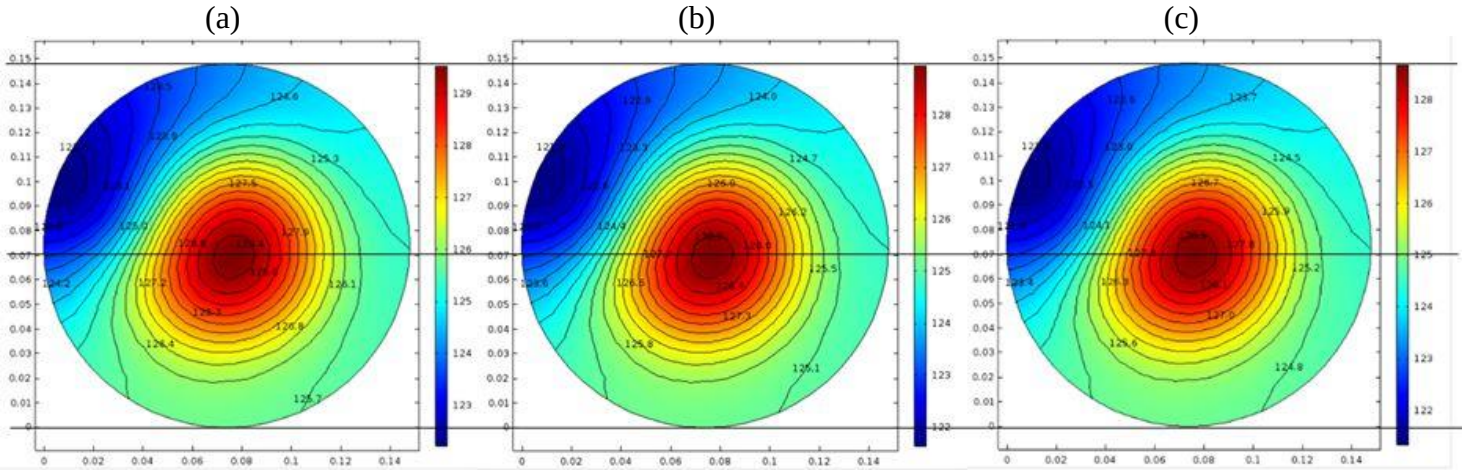


Figure 72: Simulated Results of HBC Conductivity Changes

Figure 73 (a) shows the geometry of the cooling channel within the Esc and the modelled temperature distribution of the cooling fluid as it moves through its course during the simulated process run.

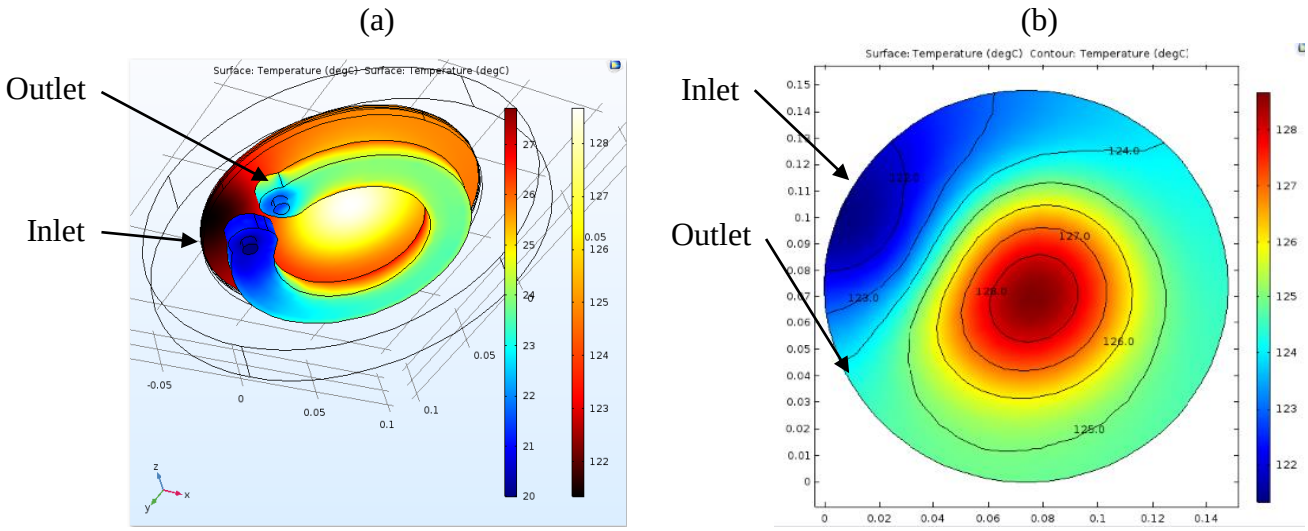


Figure 73: Cooling Channel Performance Simulation

The temperature distribution on the substrate surface is clearly following the warming of the fluid as it progresses through the cooling circuit. The inlet side of the cooling channel is orientated with the main flat of the wafer as shown in Figure 73 (a) and corresponds with the dark blue section in Figure 73 (b). As the fluid travels through the cooling circuit, the rise in temperature can be seen on both the substrate surface and the cooling channel fluid. The drawback with this horseshoe design of circuit can clearly be seen in the hot spot in the centre of the wafer, this area has no direct cooling and is typically around 2°C higher than the surrounding areas. This information could be used for a possible future redesign of the cooling circuit to add active cooling to the centre of the esc area, this is likely to have a positive effect on across wafer non-uniformity as the temperature gradient across the esc surface would be more tightly controlled.

The software simulation is useful to provide an insight into the nature of the esc temperature distribution but is not as accurate as experimental data as certain assumptions and educated guesses

(such as the thermal conductivity of the helium layer) were used to construct the model. Additionally, the trajectory of the etch species will have rotational symmetry about the axis and will be perpendicular to the plane of the wafer. The software simulation suggests that the main flat area is cooler than the opposite main flat area and predicts that the centre is consistently the area of the substrate that exhibits the highest temperature, the cooling channel position is shown in Figure 74, and clearly shows that the centre of the esc is not directly cooled by the circulating fluid. This could part way explain why the experimental results in chapter 3 consistently show a different etch profile to the wafer edges which have a more regular temperature distribution.

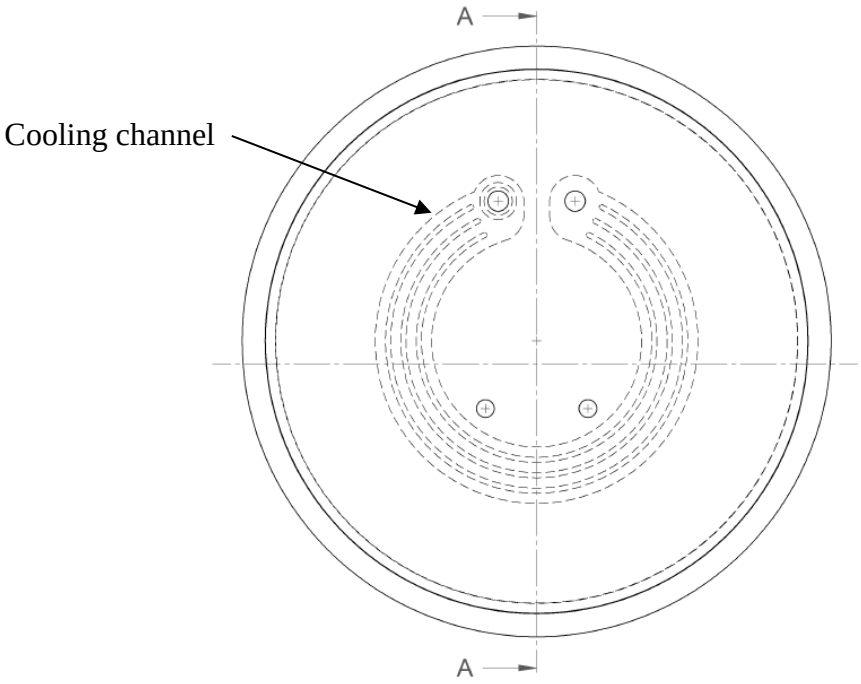


Figure 74: Esc Cooling Channel Illustration (copied with permission of SPTS Technologies)

The computer modelling simulation suggests that there is approximately 6ºC of temperature gradient between the centre of the substrate and the main flat position, this distribution remains roughly consistent across all the temperature and helium backside pressure changes that were modelled. While it is possible that the temperature distribution across the esc is having a small effect on the TSV profile, the fact that the distribution is consistent suggests it is unlikely that there are any significant effects from the cooling channel distribution as there are no obvious patterns that align with these features.

Chapter 5 - Conclusions

This chapter discusses the results from the design of experiments and computer modelling simulation, draws conclusions from the available data sets and attempts to identify areas which will allow the research to be expanded further. The goal is to increase the predictability of the positive profile form to allow for the subsequent manufacturing process results to be anticipated which could result in a decrease in the time and cost of manufacturing these devices.

5.1 Process Parameter Effect on the Undercut

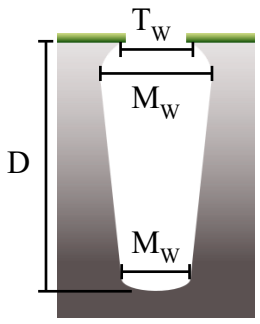
Figure 69 illustrates that the top width, and maximum width dimensions are inextricably linked by the process parameters that were investigated here, any change that adjusts the size of one of these dimensions will alter the others by a similar amount, this effect can be seen in the roughly equal slope angle of the black lines on the prediction profiler. The model indicates that adjusting the process pressure may have the effect of increasing the size of the top width dimension while not increasing the maximum width, but this effect is very limited in scale and is not a tool that could be reliably used to decrease the size of the overhang.

Section 1.7 of this thesis discusses that the overhang feature is normally removed by a second 'thinning' process that allows for the follow-on deposition processes to place an even layer of material along the entire surface of the target features. One of the most critical dimensions for manufacturing processes that come after the thinning step is the uniformity of the features, the closer they are together in size and shape the more predictable the finished results will be in subsequent manufacturing steps. The results model identifies that there is a predictable correlation between decreasing across wafer non-uniformity and an increase in the platen temperature, but crucially the temperature rise has little to no effect on most other parameters.

This effect can be seen in Table 48 which displays the statistically significant effects (p-value of less than ≤ 0.05) that were identified during the results analysis. The arrows in the table show the direction of effect with a single arrow showing a small change and a double arrow showing a larger reaction to a process parameter adjustment, for example you can see from the table that when process pressure is raised it reduces the depth of the features in the centre of the wafer by a large amount, but the same change increases the feature depth at the main flat. It can be clearly seen in Table 48 that there is no definite trend within the scope of this work that would allow a user to solely manipulate the

undercut dimensions, although there is a clear reduction in the top and maximum width measured uniformity values when the platen temperature is increased.

Table 48: Statistically Significant Results

	Process Pressure ↑	Total Gas Flow ↑	Platen Temperature ↑	Coil RF Power ↑	Platen RF Power ↑	Platen RF Power ↓
Depth C	↓↓	↑↑				
Depth MF	↑					
Depth Uni	↑↑					
TW C		↑↑				
TW MF	↑	↑↑				
TW OMF	↑	↑↑				
TW Uni	↑	↑↑	↓↓			↓
MW C		↑↑				
MW MF		↑↑				
MW OMF		↑↑				
MW Uni	↑↑	↑↑	↓↓			
BW MF	↓↓	↑↑			↑↑	
BW OMF	↓↓	↑↑		↑	↑↑	

The general trend with an etch process is that as the platen temperature is increased, the deposition rate of the passivation layer will decrease [81], this will result in the etch rate rising across every dimension in the feature profile. A switched etch process such as the Bosch DRIE process [82] adheres faithfully to this rule as very little lateral etching occurs during the process, but the manifestation of

this effect in a continuous single step etching process that includes a large component of lateral etching is subtly different.

The trend will continue until it reaches a threshold that is dictated by the target feature size and the level of lateral etching required to create the profile shape, once this point has been achieved the reduction of the passivation layer deposition rate causes increased etching across the entire feature area which is significantly larger in a positive profile when compared to a straight profile. As the volume of the via that is being etched increases more of the etch species will be consumed from the reactor environment which consequently slows down the overall etch rate. The results of this effect are visible in the platen temperature column of Figure 69, decreased passivation should show as increased etch rate as per the general trend, but counterintuitively the results in this column are showing either very small increases or actual decreases in the observed etch rate. It is this slowing of the etch rate that is the likely cause of the decrease in across wafer non-uniformity of the features, as the etch rate slows it reduces the effect of etch species variations across the whole substrate surface which homogenises the etch rate and thus making the across wafer features more uniform.

The improvement on across wafer non-uniformity is measured as approximately 1% for every 5ºC increase of platen temperature in the range which was tested as shown in Figure 75, although this trend is likely to be subject to the law of diminishing returns and will not continue improving indefinitely [83]. The non-uniformity can be further reduced by lowering the total gas flow, with an additional improvement of approximately 1% of uniformity for every 100sccm of total gas flow reduction. But it should be appreciated that any reduction in gas flow will have the larger effect of reducing all the other etch profile dimensions except for bottom width uniformity, as a result additional process changes are likely to be required if gas flow is used to further reduce the across wafer non-uniformity.

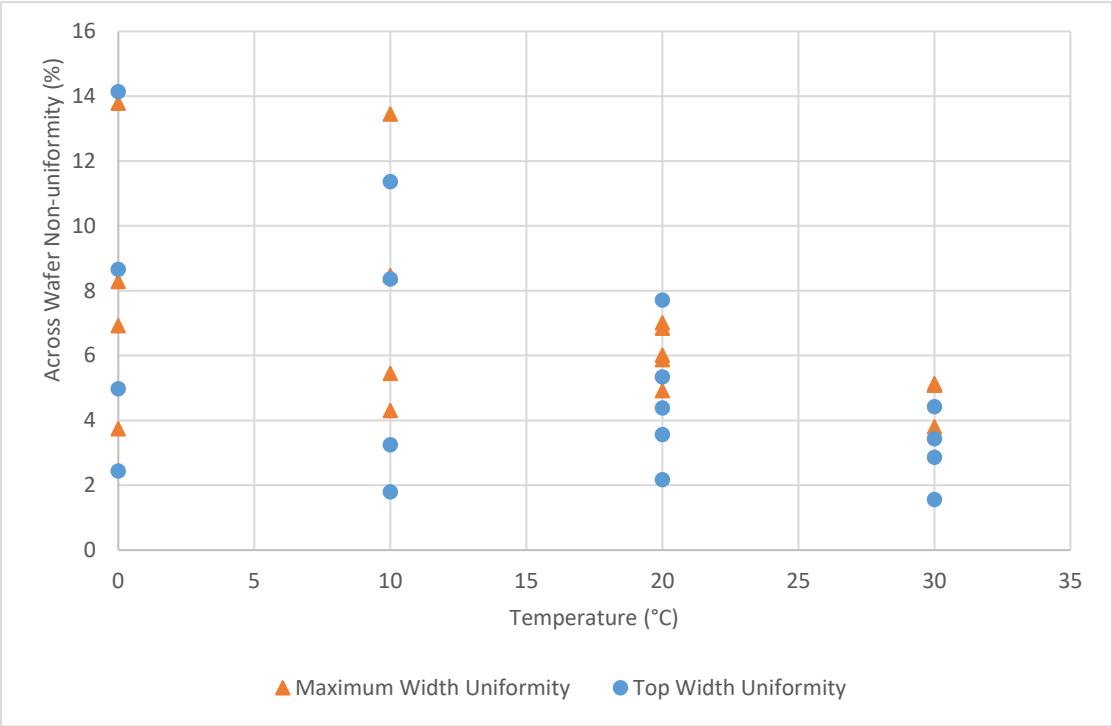


Figure 75: Temperature vs across wafer non-uniformity

It should be noted that the effect that has been identified above is present across the whole surface of the substrate and no large variations were recognised between the centre and edge positions, this would suggest that the cooling channel effects modelled in Chapter 4 are having minimal effects on the across wafer non-uniformity of the TW and MW profile dimensions. It is worth bearing in mind that this an assumption and cannot be established as true due to the low number of locations measured across the wafer surface and is a possible area that could be investigated for future research.

5.2 Data Trend Summary

This project investigated the effect of five process parameters on a positive etch profile and the across wafer non-uniformity of TSVs. Figure 76 shows the effect magnitude of each parameter against the variables assigned for investigation, the parameters are ordered largest to smallest effect and shows that the total gas flow has the greatest effect on the profile shape, followed by process pressure.

Interestingly, the computer model assigns platen temperature as having the second to last effect on the process results as it only has a large effect on uniformity and has little to no effect on the other profile dimensions. If taken in isolation the conclusions of the regression analysis are accurate, but a TSV is not a standalone product as it always part of a much larger assembly with multiple production steps.

One of the major production sequences is the 'thinning' process that is designed to remove the overhang due to the unpredictability of the resulting profile, it is the knowledge that this step exists that changes the way results are interpreted. The most important parameter of the feature profile once the thinning process has occurred is the uniformity of the TSV features across the whole wafer and is crucial for predictable outcomes from the follow-on production steps.

It can be taken from the results shown in Figure 69 that the platen temperature is the parameter that has the greatest effect on the uniformity of the TSV profile. It is therefore reasonable to re-interpret the results of the analysis with respect to this knowledge and assign the platen temperature as the most important parameter, against the results of the trial.

Source	LogWorth		PValue
Total Gas Flow	5.303		0.00000
Process Pressure	3.371		0.00043
Platen RF Power	2.715		0.00193
Platen Temp	2.377		0.00420
Coil RF Power	1.531		0.02942

Figure 76: Most Significant Parameter Summary

5.3 Further Work

This programme of work has proven the link between the temperature of the platen and the non-uniformity of the etched profiles across the wafer, additionally there is the secondary effect on the across wafer uniformity generated by the total gas flow into the chamber. Reducing the total gas flow will reduce the overall uniformity but has the unwanted side effect of decreasing the size of all the dimensions of the profile except for the bottom width. Further investigation into these positive etch profiles could take two paths, the first being the relationship between raising the platen temperature and lowering the total gas flow which were shown to be complimentary effects in the prediction profiler (Figure 69), the second would be researching the relationship between platen temperature and the ratio of the etch and passivation gas which has been identified as having a large effect on the shape of a positive profile TSV [30]. The purpose of the project would be to decrease the across wafer non-uniformity of the TSV's closer to zero, whilst simultaneously adjusting the sidewall profile to maintain the feature dimensions, and ultimately manipulating the sidewall shape to ensure that the top width is always the dimension of maximum width to eliminate the undercut completely and remove the requirement for a thinning process.

The samples run as part of this DoE were processed on the STS Pegasus® deep silicon etcher, at the time of writing this product line had been retired as a current product offering from SPTS Technologies. Further work would be transferred onto the next generation SPTS Rapier® deep silicon

etcher that features a unique dual source design, with two independently driven RF coils allowing some control and steering of the plasma ions providing improved feature tilt control.

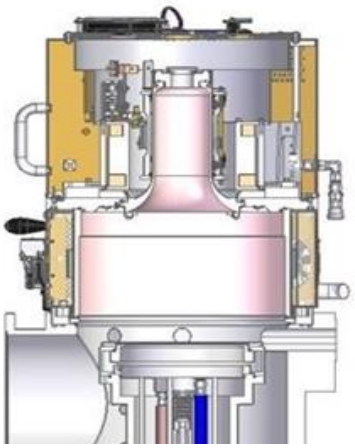


Figure 77: An SPTS Rapier System® (copied with permission of SPTS Technologies)

It is the ability to control the direction of the ions that would be used as part of any future work, as this would offer another process parameter that could be manipulated to fine tune the across wafer non-uniformity of the TSV structures and would provide an ability to counter the effects of edge loading. The edge loading effect is mitigated by the fact that the secondary coil produces a large number of ions when maintaining a plasma that limits the number of radicals that can be formed; it is these radicals that contribute greatly to the edge loading effect [71].

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Chapter 6 – Research Paper

This chapter contains the research paper that was presented to the IMAPS 16th International Conference and Exhibition on Device Packaging in Fountain Hills, Arizona on March 3rd, 2020.

Through silicon via undercut profile optimisation for 3D packaging applications

Paul Gray, Janet Hopkins, Huma Ashraf, Lijie Li.

Presented at IMAPS Device Packing, Arizona. March 3rd 2020

I. Abstract

The key enabling technology for 2.5D and 3D packaging applications is the through silicon via (TSV), this allows integrated circuits and additional component layers to be vertically stacked minimising internal signal connection lengths allowing for faster operation, reduced heat production and lower power consumption. TSV's are commonly formed with a positive profile which minimises void defects during the metal conductor formation. This research was conducted on an SPTS Technologies Ltd Pegasus® deep silicon etcher employing a single step $O_2/SF_6/Ar$ process, the aim was to determine if there is a set of parameters that can be used manipulate the 'undercut' feature that commonly forms at the top of the feature during etch processing. An L16 (4^5) Taguchi Array was used to determine the interaction effects of changing five critical process parameters. The results from the process sample runs were analysed using commercially available statistical analysis software for subtle interactions, which showed that there were no obvious relationships that would facilitate predictable manipulation of the undercut dimensions. However, a clear and predictable trend was observed from the results which showed that increasing the wafer platform temperature results in a decrease in across wafer non-uniformity of critical TSV profile dimensions.

Index Terms – manipulation, non-uniformity, plasma, TSV, undercut

II. Introduction

In recent years through silicon via (TSV) has become a key enabling technology in the production of 3D integrated circuits, these features allow components to be stacked vertically [1] dramatically increasing the device performance while minimising power consumption and overall package size [2]. This study investigated the effects of process parameter changes on the overhang feature dimensions and across wafer non-uniformity in a positive profile TSV using a silicon substrate.

Positive profile features are commonly used for TSV applications as no part of the sidewall overshadows any other point on its internal surface, as can be seen in Figure 78.

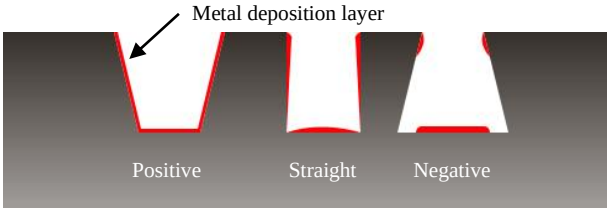

Figure 78: TSV Deposition Layer Coverage

Positive profile TSVs frequently require a second process [3] to remove the 'overhang' or 'undercut' feature (refer to Figure 79) which commonly forms at the top of the profile due to a lateral etching effect [4], which will prevent a continuous metal barrier layer being applied to the TSV, it is critical to the function of the final device [5] that the barrier layer is continuous, as voids in the film will cause defects in the filler material [6].

This research focused on the outcome of the interactions between various process parameters on the across wafer non-uniformity and final profile dimensions of the etched features. The goal of the programme was to determine the process parameter affects that allow the magnitude of the overhang feature to be manipulated in order to prevent its formation or limit its growth.

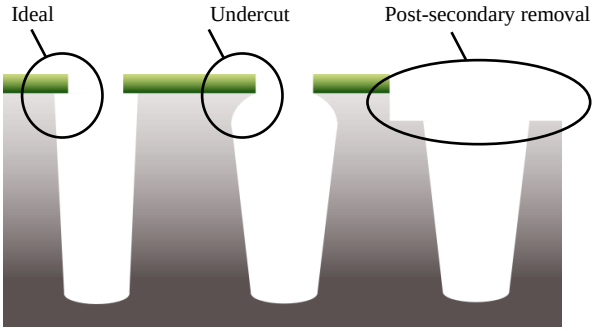

Figure 79 TSV Process Profile Cross Section

The removal of the undercut feature would eliminate the need for any secondary processes required to remove the feature after the completion of the etch [7], which adds cost and time to the manufacturing cycle [8]. M. Boufnichel et al, had observed the presence of the undercut during TSV etching concluded that the presence of the undercut appeared to be dependent on the balance between the relative ion density and fluorine/oxygen gas ratio, with ion density being the key to the relative size of the undercut as increasing the RF power caused the feature to enlarge. The researchers concluded that increasing the RF energy leads to more ion production, but an unanswered question remained as to the mechanism behind the obvious pathway deviation of the ions away from the normal vertical direction of travel [9].

In a follow up study, T. Maruyama et al attempted to discover why the ions appeared to be deviating from their normal vertical path between the plasma and substrate. Their research adjusted the ratio between the O_2 and SF_6 process gases and noted that this led to the size of the undercut being drastically reduced, the research concluded that the major mechanism in the formation of the undercut feature was ion scattering from the edge of the mask [10].

III. Experimental Methodology

The process trials were completed using an SPTS Technologies Ltd Pegasus® deep silicon etch system using 150mm TSV structure test wafers with a 3.28% open area. The etch reactor was cleaned using a 30-minute O_2 plasma to remove any contamination from previous processes runs. After completion of the clean the process chamber was conditioned for 30 minutes using an $SF_6/O_2/C_4F_8$ switched process to passivate the internal chamber walls, thus restricting them from absorbing free fluorine present in the reactor environment and preventing variations in etch rate between the process runs.

Table 49 displays the parameters that were used as a baseline for this research, an L16 (4^5) Taguchi Array [11] design of experiments (DoE) was used to understand the role of parameter changes on the etch profile. The values of the five chosen parameters were centred around the process of record to determine the effect on the etch profile. Each parameter had four data points that were equally divided across the range; the values for each run are shown in Table 50 (run one is the base process). The ratio between the process gasses was fixed for the purposes of this test, Table 51 details the breakdown of the individual gas flows for each total gas flow value.

Table 49 TSV Process Parameters

Recipe Setting	Parameter Value
Process Time	15'00"
Process Pressure	90mTorr
SF_6	156 sccm
O_2	80 sccm
Ar	42.5 sccm
Coil Power	3.35 kW
Platen Power	135 W (13.56 MHz)
Platen Temperature	20ºC
Helium Backside Pressure	10Torr

Table 50 DoE Run Parameters

Run	Total Gas Flow (sccm)	Coil RF Power (Watts)	Platen RF Power (Watts)	Process Pressure (mTorr)	Platen Temp (^{0}C)
1	278.5	3350	135	90	20
2	139.25	2650	65	60	0
3	139.25	3000	100	90	10
4	139.25	3350	135	135	20
5	139.25	3700	170	170	30
6	278.5	2650	100	135	30
7	278.5	3000	65	170	20
8	278.5	3350	170	60	10
9	278.5	3700	135	90	0
10	417.75	2650	135	170	10
11	417.75	3000	170	135	0
12	417.75	3350	65	90	30
13	417.75	3700	100	60	20
14	557	2650	170	90	20
15	557	3000	135	60	30
16	557	3350	100	170	0
17	557	3700	65	135	10

Table 51 Process Gas Flow Values

Total Gas Flow (SCCM)	SF_6 (56%)	O_2 (28.75%)	Ar (15.25%)
139.25	78	40	21.25
278.5	156	80	42.5
417.75	234	120	63.7
557	312	160	122.2

The completed etched profiles were measured at three locations across the wafer surface Centre (C), Main Flat (MF), and Opposite Main Flat (OMF) to gain information about the uniformity and depth of the profile across the substrate surface.

To define the shape of the etched profile, the TSV is measured in four locations as illustrated in Figure 80, these are depth (D), top width (T_W), maximum width (M_W), bottom width (B_W). The mask thickness (M_T) is used to calculate selectivity and does not form part of the feature characteristics.

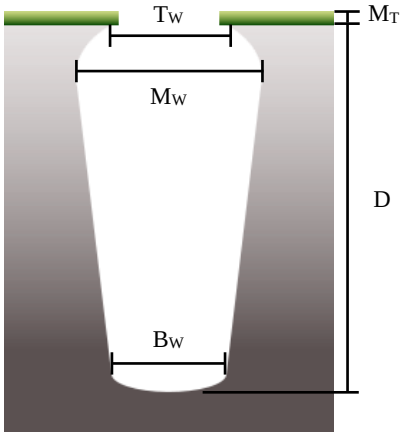

Figure 80 TSV Profile Definition

The results from the sample process runs were measured using a Carl Zeiss Sigma scanning electron microscope (SEM) and were analysed using JMP Statistical Discovery™ software from SAS [12] in order to determine the subtle interplays between the process parameters.

IV. Results

All seventeen runs were processed in an SPTS Pegasus® DRIE etcher using the start conditions shown in Table 49, with the variations for each run being detailed in Table 50 and Table 51. It should be noted that the results from the centre position always appears to be visually different to the MF and OMF positions. This is due to the annular shaped plasma created by the Pegasus reactor which has a lower density region at its centre, this results in the etch rate being 'centre low' when the process is not finely tuned to remove this effect.

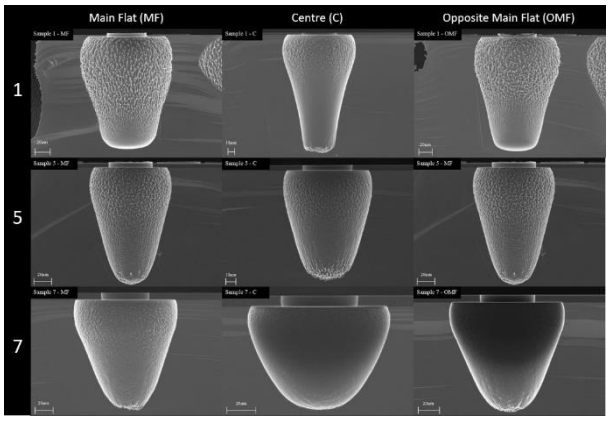

Figure 81 Sample Results (best (5) and worst (7) case

Table 52 (Figure 81) Run Result Dimensions

Run	Position	$T_{W\,(\mu m)}$		$M_{W\,(\mu m)}$	$B_{W\,(\mu m)}$	$D_{\,(\mu m)}$	$M_{T\,(\mu m)}$
1	C	96.31		111.1	46.59	178.7	3.084
	MF	100.6		120.8	69.13	146.9	2.403
	OMF	97.49		119.6	59.92	157.3	2.475
	Uni (%)	1.88		4.14	19.2	9.88	12.82
5	C	81.75		88.92	42.1	110.8	5.492
	MF	84.36		95.72	35.19	136.2	4.906
	OMF	83.92		96.03	44.55	133.9	5.013
	Uni (%)	1.56		3.8	11.52	10	5.7
7	C	89.45		94.29	32.88	67.86	7.366
	MF	104.6		108.7	38.21	115.4	7.606
	OMF	100.5		105.3	26.2	100.3	6.828
	Uni (%)	7.71		7.01	18.51	25.14	5.35

Run 1 in Table 52 shows the TSV etched features after completion of the base process.

Run 5 results clearly show the 'centre low' effect in the incomplete etch depth in run 5C when compared to 5MF and 5OMF. The profile non-uniformity between the three element positions is much reduced (compared to run 1) even with the lower etch rate seen in the centre position. The Coil and Bias RF powers are higher for run 5 than the baseline process which will increase the etch rate, but this is counteracted by the large increase in process pressure

Run 7 is showing large differences in profile shape, the outline of the features has changed from an inverted cone to a more 'strawberry' like shape with a significantly smoother surface texture. These differences are the result of the change from a mainly ion driven process to a more chemical etch. The increased process pressure will allow for the formation of more fluorine radicals due to more numerous collisions within the plasma but will limit the impact power of the ions, as there is a longer mean free path between the plasma and the substrate surface.

V. Discussions

The full set of results obtained from the 17 sample runs were collected and analysed by the JMP Statistical Discovery™ software [12] for predictable interactions between process parameters and profile dimensions. Table 53 shows the statistically significant interactions that were highlighted by the software model as having a p-value of less than ≤ 0.05, a result below this value indicates that the software can reliably predict the outcome of the interaction between the TSV profile dimensions and changes to the process parameters. The table uses ↑↓ to show an increase/decrease in value and a double arrow shows a large reaction to a parameter change.

Table 53 Statistically Significant Process Effects

	Process Pressure ↑	Total Gas Flow ↑	Platen Temperature ↓	Coil RF Power ↑	Platen RF Power ↑	Platen RF Power ↓
Depth C	↓↓	↑↑				
Depth MF	↑					
Depth Uni	↑↑					
TW C		↑↑				
TW MF	↑	↑↑				
TW OMF	↑	↑↑				
TW Uni	↑	↑↑	↓↓			↓
MW C		↑↑				
MW MF		↑↑				
MW OMF		↑↑				
MW Uni	↑↑	↑↑	↓↓			
BW MF	↓↓	↑↑			↑↑	
BW OMF	↓↓	↑↑		↑	↑↑	

Increasing the process pressure has a direct influence on the TSV process, but the results are not consistent across all parameters as can been seen in Table 53. For example, the depth of the feature is reduced in the centre position, yet the reverse is true for the depth MF position and across wafer uniformity. Increasing the process pressure will raise the number of collisions between electrons and molecules which boosts the number of reactive species in the etch environment, enhancing the chemical part of the etch but will supress the physical portion as the mean free path to the substrate is increased [13]. However, this effect is self-limiting as the number of collisions will eventually reach saturation point where the electrons in the process environment will have no space to accelerate and the plasma will collapse.

Increasing the gas flow will affect the dimensions of the TSV, however not all these changes are desirable as the across wafer non-uniformity increases making feature shapes unpredictable. As the flow increases the residence time of the gas within the reactor lowers, this has the effect of causing the argon to release many more energetic electrons, increasing the reaction rate within the plasma. As the SF_6 flow rises, the silicon etch rate will increase raising the number of gas molecules available to be converted into ions and free radicals [14]. However, this phenomenon will only continue until a saturation point is reached where all the available RF power is used to convert gas molecules into etch species, at this point the RF power will need to be increased further to continue the effect.

One of the most critical dimensions for manufacturing processes is the across wafer non-uniformity of the features, the homogeneity of the devices is desirable for subsequent manufacturing steps. The software model shows that there is a good correlation (p-value <0.007) between decreasing non-uniformity and increasing platen temperature, but crucially the temperature increase has little to no effect on the other profile dimensions. The improvement on across wafer non-uniformity was approximately 1% for every 5°C increase of wafer platform temperature for the range tested.

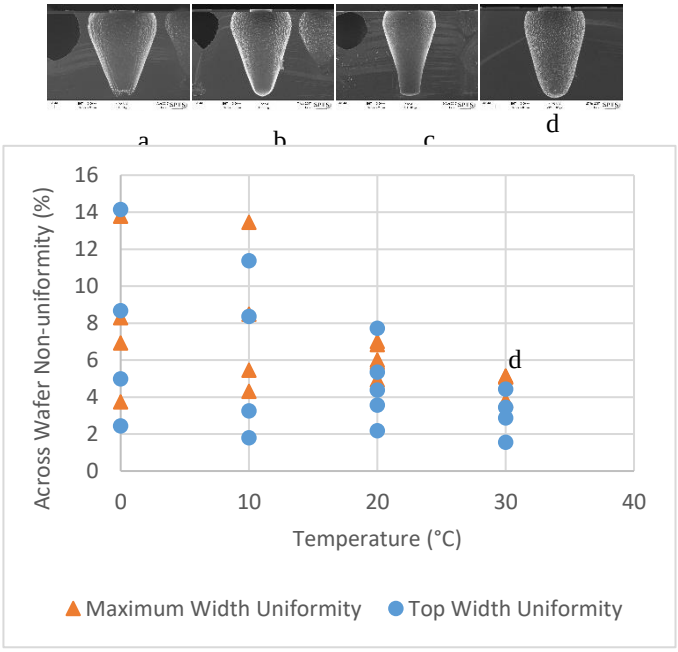

Figure 82 Temperature vs across wafer non-uniformity

Passivation of the substrate surface is dependent upon its temperature [15], as it increases the deposition rate of the passivation layer reduces, typically resulting in a rise of the isotropic and anisotropic etch rates [16]. This effect should clearly show in the measured results; decreased passivation will commonly present as an increased etch rate, but counterintuitively the test results showed either small increases or actual decreases in the degree of vertical etch rate observed.

The slowing of the vertical etch is unexpected when examined in isolation, however when a holistic approach is taken, the etch rate does indeed increase across the whole of the exposed features both laterally and vertically. As the volume of the silicon being etched expands, more of the etch species are being consumed out of the reactor environment by the larger area of the exposed sidewalls, slowing down the vertical etch rate but homogenising the etch making the features more uniform across the substrate.

VI. Conclusions

The purpose of this research was to identify and quantify the dominant process parameter changes needed to predictably eliminate the undercut/overhang feature that normally develops at the top of a positive profile TSV feature during etching. This research identified that a clear framework of adjustments was not discernible from the results, however there was a predictable interaction between raising the bias platen temperature and improvements in across wafer non-uniformity.

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Appendix

1. Sample Process Run Notes:

1) Several test runs were completed to ensure that the process conditions and hardware were stable, each of these results were analysed using the same procedure as the samples in Section 3. It was quickly apparent that the etch profiles in the left (L) and right (R) positions on each wafer were predictably similar to results from the main flat (MF) and opposite main flat (OMF) positions, as a consequence the results from these two positions were not included after run 1 to limit the number of data points that were needed for analysis.
2) The sample runs have shown that the centre position profiles are visibly different from the results obtained in other positions on the substrate, this is due to the construction of the Pegasus reactor chamber. As explained previously the Pegasus has an annular source design that creates a torus (doughnut) shaped plasma, this shape naturally has a space in the centre which creates an area of lower density plasma in the reactor vessel. This low-density area creates local changes in the plasma environment which clearly show as differences in the sample results at the centre position.