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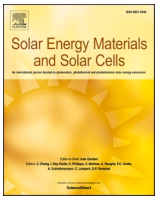

A facile photolithography process enabling pinhole-free thin film photovoltaic modules on soda-lime glass

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A B S T R A C T

Release of the alkaline (mainly sodium) impurities from the soda-lime glass (SLG) substrate can compromise scaling-up of thin film photovoltaic (PV) devices deposited at high temperatures. This does not only degrade electronic device quality but also results in catastrophic effects such as delamination of the semiconductor thin films. Device scale-up can be further hindered by the pinholes that may exist across the large panel areas, causing serious shunt paths. We demonstrate fabrication of uniform CdTe mini-modules on the SLG using a facile photolithography process. This process effectively suppresses sodium release and prevents film delamination from the substrate whilst plugging the pinholes within the semiconductor p-n junction layers. Mini-module devices with repeatable device response are demonstrated using an industrial laser scribing system operating long (microsecond)-pulses of a green laser for thin film scribing.

1. Introduction

Thin film PV solar cells based on CdTe, CIGS, and Perovskite absorbers are commonly studied across many academic and industrial laboratories. Moving from the small-scale solar cell research to large-area device utilization typically requires enlargement of the cell area and interconnection of multiple solar cell diodes in series and/or parallel configuration. This can be achieved by connecting large single cells (often preferred for CIGS and Perovskite) or realizing monolithic interconnection (typical for CdTe [1]).

One of the major obstacles with thin film PV device scale-up is the presence of pinholes that act as sink holes for carriers, impeding utilization of the full coating area. Another serious problem can occur due to the requirement of using the low-cost soda-lime glass (SLG) as the substrate platform. The SLG contains an abundance of alkaline impurities which can be released during high-temperature thin film deposition and/or processing steps. For example, electrical isolation lines scribed within the contact layer on the SLG provide openings that accelerate elemental diffusion between the glass and coating materials. This problem is further enhanced for CdTe PV which suffers from local film delamination effects as a result of excessive grain growth and stress build-up within the CdTe absorber [2,3].

These issues point out the need for providing an effective blockage to the diffusing elements and carrier leakage through isolation scribes or pinholes in the device layers. Deposition of insulative polymers inside these openings can offer a solution. However, it is vital that no insulator must be left over the semiconductor surface restricting top-contact layer formation. Ink-jet deposition is an attractive option providing high material usage and localized application of a polymer ink [4]. However, alignment to the scribe pattern may prove challenging and it is almost impossible to plug the pinholes individually with this method. Thus, global application and localized curing of a polymer film on the PV device e.g. by means of photolithography becomes a more attractive option. In this process, the light absorber layer within PV stack, being opaque to the wavelength range of light that causes the polymer to become insoluble, offers a natural shadow mask for polymer curing.

In this study, we explore a simple photolithography process to fabricate monolithically interconnected CdTe mini-modules on SnO_2:F (FTO)-coated SLG substrate and for its efficacy towards pinhole-plugging and suppression of thin film delamination by alkaline release. Surface treatment by mild oxygen plasma on pre-scribed (P1) and aged devices is shown to be a useful tool to achieve uniform polymer deposition and device response, provided care is taken not to degrade the semiconductor layers. The impact of processing parameters for the mini-module scribing (P2 isolation) step on module performance is also highlighted.

2. Experimental

CdZnS/CdTe pn junction layers were grown by metalorganic chemical vapor deposition (MOCVD) onto pre-cleaned FTO/soda lime glass (SLG) substrates provided by First Solar, Inc. and the junction was

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activated by a $CdCl_2$ heat treatment, as described in previous work [5]. The FTO substrate had a sheet resistance of ~18 Ohm/sq.

All thin film scribes were performed on a ROFIN laser scribing system which is capable of roll-to-roll processing over 80 cm web width. It operates a micro-second pulsed green Nd:YVO4 laser (diode end-pumped, 532 nm wavelength) on a moving X–Y stage controlled by the software Visual Laser Marker. For all scribes produced using this system, laser pulse repetition rate of 1 kHz, scanning speed of 20 mm/s, and pulse width of 10.0 μs were used with an average output power of 15.2 W (measured at the aperture). The laser fluence was controlled via the laser beam current (max. 30 A available) and tuned to achieve selective removal of the front contact materials (P1 scribe) or the p-n junction layers only (P2/P3). Laser fluence was fixed at 22.6 J/cm^2 for all P1 and device separation scribes, as at this fluence full electrical isolation of the FTO film was achievable; meanwhile, it was varied from 16.3 to 19.1 J/cm^2 for P2 and P3 scribing to study its effects on the scribe and device properties. Laser scribing was performed by irradiating the films through the glass-side, which helps to ablate the thin film interfaces and thereby permits uniform processing of films with uneven thickness distribution. Additionally, some complementary thin film scribing experiments were carried out on a research grade laser system at Hacettepe University, employing a Nd:YAG solid-state laser (532 nm wavelength, 20 ns pulse width).

Photolithography was performed following the P1 scribe that removes both the front contact and p-n junction layers. A negative photoresist was applied onto the sample surface and spread over the area with a hand-operated sponge roller in low light conditions at ambient temperature. A soft bake was applied for 3 min at 80°C. A simple home-built curing stage equipped with a UV lamp (Osram Ultra Vitalux 300W) was used to irradiate the resist coated sample through the glass side, whereby CdTe film acts as a natural mask so only the resist filled within the P1 scribe channels and pinholes is cured by UV exposure (time 2 min). Rinsing of the samples in a photoresist developer, which removes the uncured resist, was followed by cleaning in de-ionized water and drying with blowing nitrogen. Resist viscosity was adjusted by mixing it with a thinner (up to 1:4 ratio) to adjust the in-fill depth.

Samples were characterized by scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy (EDS) analysis following the laser scribes. Completed mini-module devices were characterized by current-voltage (IV) measurements using an ABET solar simulator calibrated to AM1.5 irradiation using a GaAs reference cell (ReRa Solutions).

3. Results

The schematic in Fig. 1 describes the scale-up process for CdTe PV devices. A deep pinhole, extending from the CdTe back surface to the transparent conducting oxide (TCO) layer, is also represented due to its importance for technology scale-up. In the first step, the front contact isolation (P1 scribe) is achieved which is postponed until after the deposition of semiconductor layers in order not to expose them to the vertical alkaline diffusion. Unlike the conventional monolithic interconnection process (suitable for alkaline-free substrates [6] or when the cell deposition temperature is low [7,8]) whereby TCO isolation scribing (P1) *precedes* semiconductor deposition, this delayed scribing process on SLG leaves openings within the semiconductor layers and TCO which would allow the back contact metal to contact the TCO, shorting the device. Thus, these *deep-reaching* P1 scribes must be re-filled with an insulator before depositing the back contact metal. In the second step, a negative photoresist is applied globally over the device structure, filling the P1-scribed lines. The sample is then irradiated by UV light through the glass side to cure the resist film within the openings of the semiconductor layers, including pinholes. In the third step, excess (non-crosslinked) resist layer on the absorber surface is dissolved away by soaking in a suitable solvent, i.e. photoresist developer. In the final step, the modular device is completed by performing isolation of semiconductor layers (P2 scribing), back contact metallization, and isolation

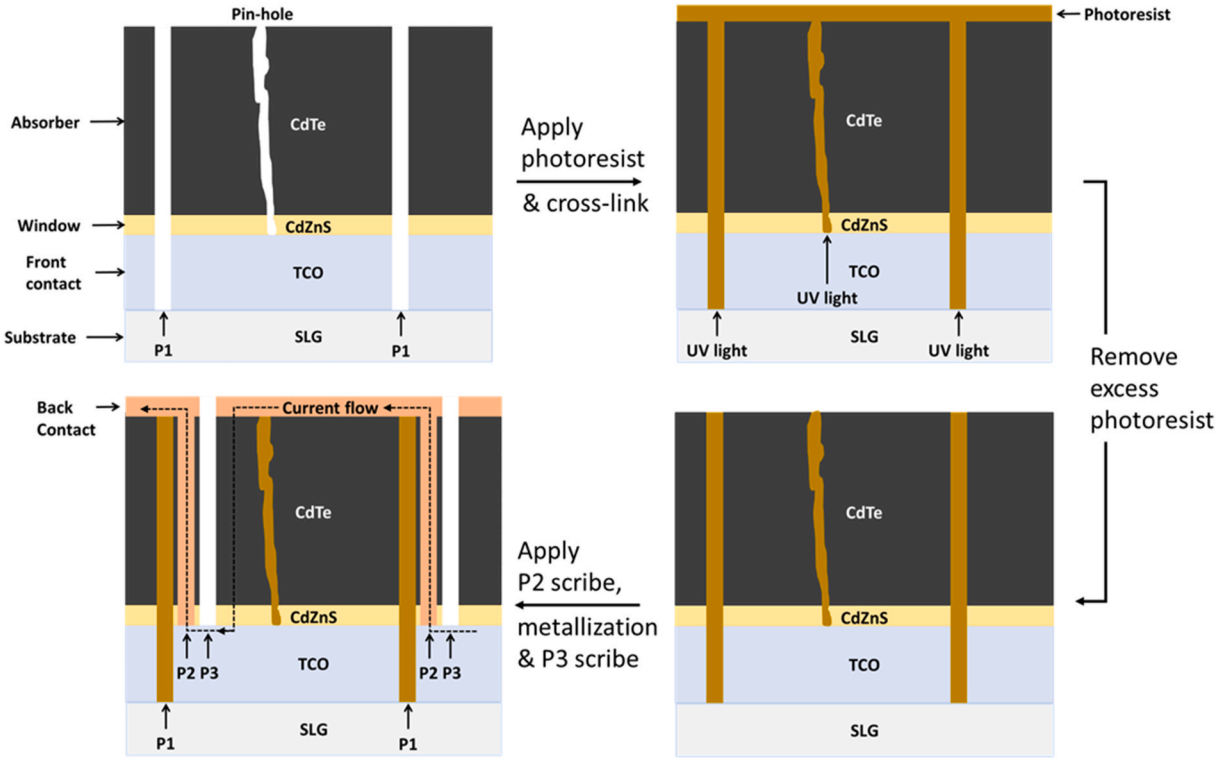

Fig. 1. Schematic of the mini-module fabrication process. TCO isolation (P1) scribes, applied post semiconductor deposition, and the "deep-reaching" pinholes within the semiconductor layers are filled up with the insulating resist by a facile photolithography step. P2 scribing (isolation of semiconductors only) followed by metallization and P3 scribing (isolation of the back contact) completes the module fabrication process.

of the back contact (P3 scribing), as per the conventional process.

A deep pinhole, such as that illustrated in Fig. 1, can easily extinguish the PV response of a solar device by providing a direct shunt path between the front and back contacts. For small-scale/test solar cells, this is actually not an issue since there are typically multiple cells established on a substrate platform, most of which are capable of delivering information on the PV performance of the thin film materials involved. However, for large-area devices such as PV modules, pinholes can have a deleterious effect on device operation. Thus, in order to harvest solar electricity across a large area PV panel it is essential to eliminate any deep pinholes. The photolithography-aided mini-module process described in this paper also delivers a solution to this end; the P1 scribes and any pinholes accessible by the UV light are concurrently filled with an insulator, thereby preventing shunt formation between the contact materials through the pinholes.

A typical 5 cm × 5 cm CdTe mini-module fabricated by the described photolithography-aided interconnection process is exhibited in Fig. 2. An isolation scribe that removes all the thin films from the SLG surface was applied to define three rows of 8 series-connected sub-cells (each 0.5 cm × 1.3 cm). The total width of the P1-P3 scribe region (so-called dead-zone) is around 0.4 mm, corresponding to 8% loss of the geometrical area. A compositional analysis of the P1-P3 scribe region is presented in the Supplementary Information, Fig. S1. Depth of the resist filling with respect to the P1 scribe appeared satisfactory for a single-step photolithography when using 1:3 resist/thinner ratio (Fig. S2).

A large pinhole located within a CdTe mini-module subcell is presented in Fig. 3, along with the performance of this cell following the repair of the pinhole by the facile photolithography process. This pinhole was the biggest found across the mini-module samples studied, and it was further enlarged to approximately 0.5 × 0.5 mm by scraping to gauge the effectiveness of the cell repair. Revealed by the EDS C signal (Fig. 3b), the large pinhole and surrounding smaller pinholes are completely filled with the resist material leaving no voids. The PV performance of the repaired sub-cell was found comparable to other sub-cells that contained no visible pinholes (Fig. 3c). Slight loss of the photocurrent (J_{sc}) with the repaired cell results from the active device area loss due to the pinholes.

For aged device structures, which already underwent P1 scribing, it is observed that the resist did not completely cover the scribe lines due to poor wetting. In order to facilitate this, a mild oxygen plasma treatment was developed that cleaned the exposed glass surface at the base of P1 scribes and thereby permitted uniform resist application (Fig. S3). Further, deposition of the back contact metal on semiconductor layers *prior to* the plasma treatment was found essential, which otherwise increases device series resistance (Table S1). It is believed that oxygen plasma degrades surface chemistry of the semiconductor, e.g. by impact damage or formation of an insulative oxide layer, as the surface color was observed to change after the plasma process. Nevertheless, this step is not necessary in the case of continuous device production as wetting of the newly-scribed sample surface by the photoresist was much superior, leading to uniform coverage of the P1 scribes.

The AM1.5 current-voltage curves of CdTe mini-modules prepared using different laser fluence (16.5–18.6 J/cm^2) for achieving the P2 isolation scribe are shown in Fig. 4a. At low laser fluence, the fill factor (FF) is very low in association with the high series resistance such that a 'rollover' behaviour dominates the IV curve, restricting the PV performance (Fig. 4b). Even though P2 scribe lines appeared fully transparent, it was microscopically observed that the emitter material (CdZnS) was not completely removed at low laser fluence (Fig. 4c and Fig. S4). The low PCE and FF in these cases appear to be linked to the remnant emitter material, which would restrict the current flow between the back and front contacts that should merge inside the P2 scribe. At sufficiently high laser fluence (≥17.8 J/cm^2) exposed TCO surface appeared smoother and free qafrom other thin film materials whereby some loss of FTO in

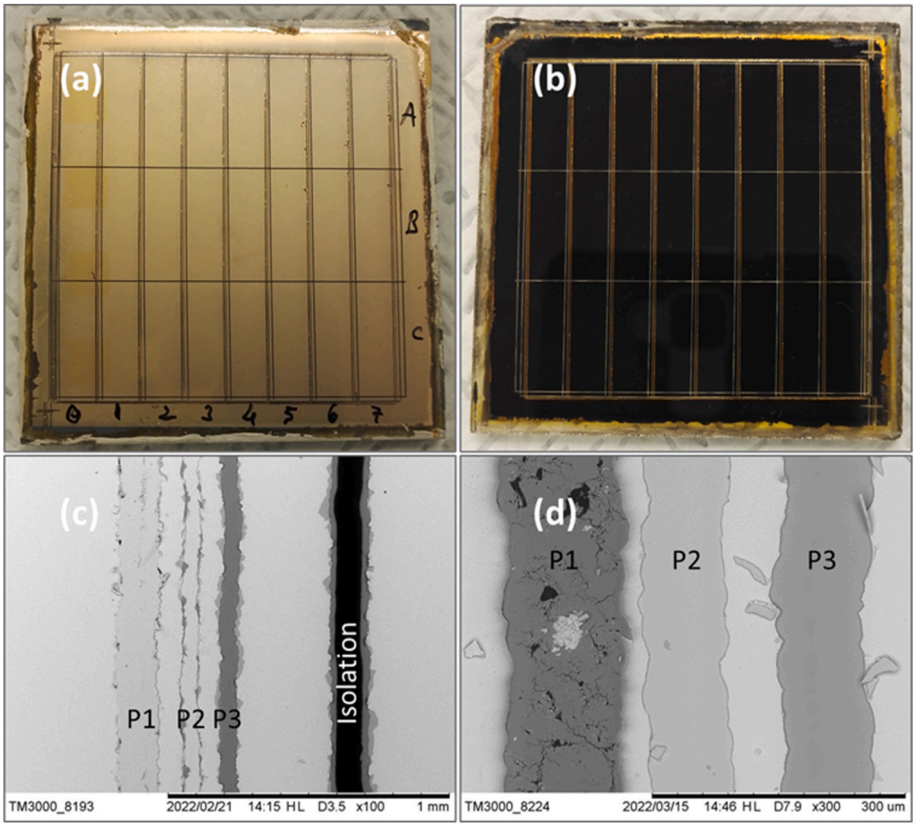

Fig. 2. A 5 cm × 5 cm CdTe mini-module device fabricated on SLG substrate by the photolithography-aided interconnection process. Top-view (a) and through the glass-view (b). SEM image of the P1, P2, P3, and border isolation scribes (c) with a close-up view of the P1, P2, and P3 scribes (d).

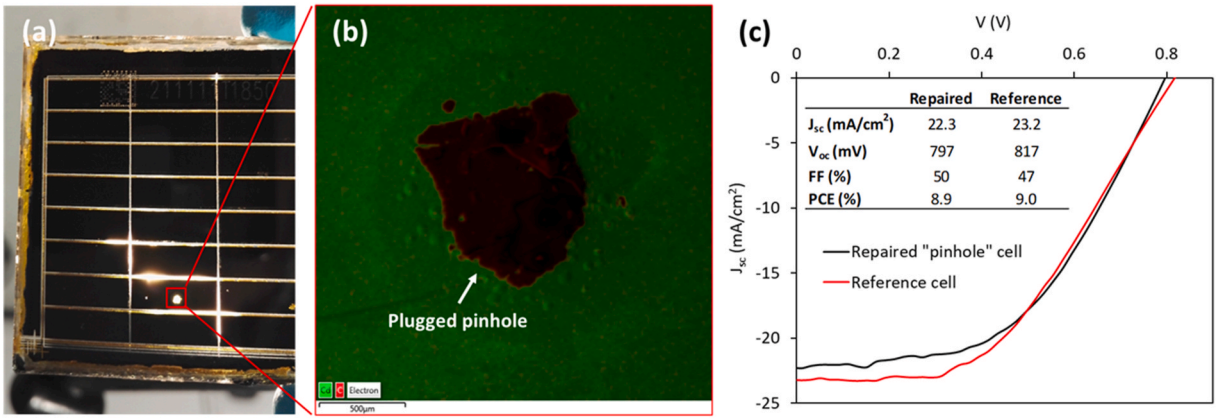

Fig. 3. (a) A mini-module device presenting a large (~0.5 × 0.5 mm) pinhole, (b) EDS map (Cd – green and C – dark red) of the repaired pinhole by photolithography and (c) AM1.5 IV curve of the repaired solar sub-cell and a neighbouring reference cell without visible pinholes. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

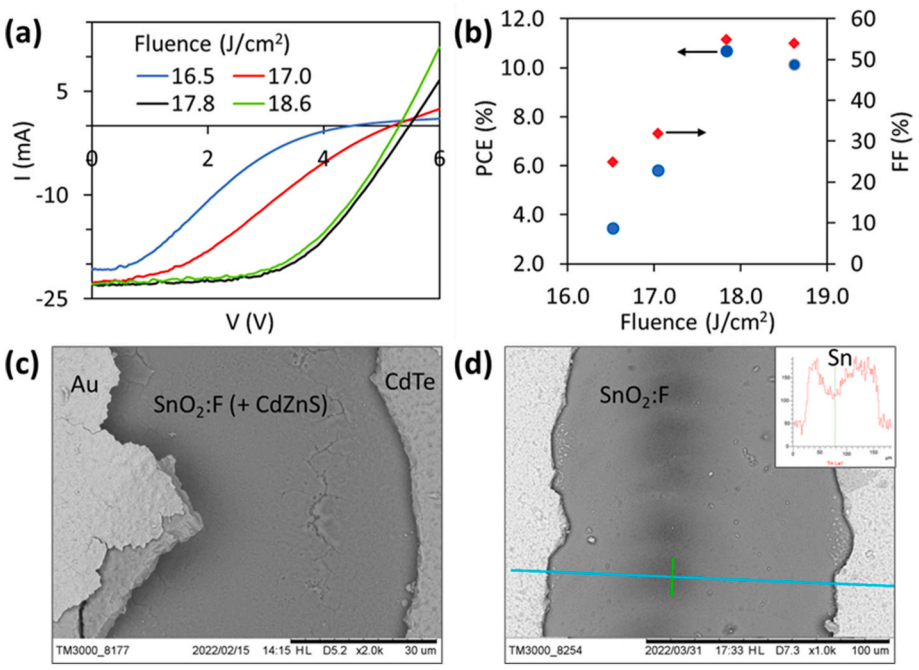

Fig. 4. (a) AM1.5 IV curves and (b) power conversion efficiency (PCE) and fill factor (FF) of CdTe mini-modules (each consisting of eight series-connected 0.5 cm × 1.3 cm subcells) processed with different laser fluence for the P2 isolation scribe. Representative SEM image of the P2 scribe made using fluence of (c) 16.5 J/cm^2 and (d) 17.8 J/cm^2. A skin-like, cracked CdZnS remnant layer is also visible on the exposed FTO surface in (c) (see also Fig. S4). Insert to (d) is the distribution of EDS Sn (L_α) signal across the indicated analysis line, revealing localized thinning effect on the FTO layer by the more-energetic centre of the Gaussian laser beam.

the form of localized film thinning could also be observed (Fig. 4d) at the beam centre. Improvement of the fill factor due to lower contact resistance resulted in relatively high efficiency of PCE ≈11% (active-area).

4. Discussion

Previously, an electrochemical method was described to plug pinholes within a CdS/CdTe solar cell structure [9]. In this method, polyaniline is introduced onto the front contact (SnO_2:F) surface (accessible via the pinholes running down the CdS/CdTe layers) via electrochemical polymerization of aniline. It was demonstrated that satisfactory insulation was provided against the electrical shorts between the front and back contacts of the solar cell. However, aniline is a toxic material and the electrochemical process was seen to mildly etch the CdTe surface. Even though the etching turned out to be a beneficial effect for CdTe devices, resulting in a Te-rich surface that provides Ohmic back contact, it cannot be guaranteed to offer such a benefit (if not detrimental) to other thin film PV technologies. The pinhole-plugging method demonstrated in this paper, however, makes use of UV curing of a non-toxic (standard) negative photoresist and does not cause any degradation to the sample. The excess (uncured) resist can be easily removed by rinsing in a photoresist developer and deionised water. Thus, the current method appears suitable for most superstrate PV technologies.

Properties of a thin film scribe produced via laser ablation depend on the beam parameters selected. The pulse-width and scan speed govern the pulse duration, which in turn determine the *processing time* and hence the ablation depth and width [9]. In this study, a micro-second pulsed industrial laser was used to produce all thin film scribes (P1, P2, and P3) needed to fabricate a monolithic PV mini-module. Compared to a shorter pulse (typically nanosecond) laser scribing, the extended irradiation time due to the extra long pulses is expected to result in wider scribes. This is confirmed by scribing some of our thin films with a research grade ns-pulsed (532 nm) laser scribing tool, where we could obtain tens of μm narrower scribe lines using lower laser fluence (see Fig. S5). This should help decreasing the dead-area and material waste, enhancing the module output power and efficiency of the fabrication process. An improvement to device performance may also be expected by the use of a short-pulsed laser (in particular due to the

superior heat-affected zone (HAZ) properties [10]); however, this needs to be confirmed in a future study.

Finally, glass-side (rather than film-side) irradiation of the pulsed laser was chosen as in this mode the thin film material is ablated at the interface to the underlying film (or substrate), causing its facile delamination rather than direct writing via sublimation. The latter requires high optical quality thin films with even thickness throughout the deposition area for satisfactory processing from the film-side. With glass-side ablation, on the other hand, irregularities in the ablated films' thickness are masked and become negligible, ensuring uniform thin film removal across the processed device area.

In short, the demonstrated process represents a cost- and energy-saving interconnection method to fabricate thin film PV modules on alkaline-rich substrates such as the manufacturing grade SLG while offering benefits such as plugging shunt paths.

5. Conclusion

A simple photolithography-based interconnection method is presented for the preparation of large-area thin film solar module devices. Alkaline release due to the SLG substrate is suppressed by delaying the front contact isolation (P1) till after the deposition of active device layers and by filling these isolation scribes with the insulating photoresist. A unique advantage of this process is that it allows elimination of pinholes existing in device layers by blocking them. CdZnS/CdTe mini-module devices were produced on an industrial scribing system using single wavelength (532 nm) laser with micro-second pulse widths. Devices were optimized by achieving clean removal of the semiconductor layers by optimizing P2 scribe parameters. A mild oxygen plasma treatment is also described for P1 pre-scribed and aged laboratory device structures. Uniform device response is demonstrated following the repair of pinholes, including a particularly large one ($\sim 0.5 \times 0.5$ mm) in a mini-module device. The presented method is simple to perform, adaptable to manufacturing, and considered applicable to other superstrate thin film PV technologies especially where the device growth occurs at high-temperature using an alkaline-rich substrate.

CRediT authorship contribution statement

G. Kartopu: Writing – review & editing, Writing – original draft, Methodology, Investigation, Funding acquisition, Data curation, Conceptualization. **O. Oklobia:** Writing – review & editing, Writing – original draft, Validation, Investigation. **T. Tansel:** Writing – review & editing, Validation, Investigation, Conceptualization. **S. Jones:** Resources, Investigation. **S.J.C. Irvine:** Writing – review & editing, Validation, Supervision, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solmat.2022.112112.

References

[1] A. Bosio, M. Sozzi, D. Menossi, S. Selleris, A. Cucinotta, N. Romeo, Polycrystalline CdTe thin film min-modules monolithically integrated by fiber laser, Thin Solid Films 562 (2014) 638–647.
[2] N. Romeo, A. Bosio, R. Tedeschi, V. Canevari, Growth of polycrystalline CdS and CdTe thin layers for high efficiency thin film solar cells, Mater. Chem. Phys. 66 (2000) 201–206.
[3] G. Kartopu, M. Crozier, A. Brunton, V. Barrioz, S. Hodgson, S. Jones, S.J.C. Irvine, Comparative study of conventional vs. one-step-interconnected (OSI) monolithic CdTe modules, Mater. Res. Innovat. 19 (7) (2015) 488–493.
[4] M.L. Crozier, A.N. Brunton, A. Abbas, W. Bowers, J.D. Shephard, M. Walls, One step thin-film PV interconnection process using laser and inkjet, in: Proceedings of the 39th IEEE Photovoltaic Specialists Conference, Tampa Bay, FL, 2013, pp. 3411–3415.
[5] O. Oklobia, S. Jones, G. Kartopu, D. Lu, W. Miller, R. Mallick, X. Li, G. Xiong, V. Kornienko, A. Abbas, M. Bliss, J.M. Walls, S.J.C. Irvine, Impact of in-situ Cd saturation MOCVD grown CdTe solar cells on as doping and V_{OC}, IEEE J. Photovoltaics (2022), https://doi.org/10.1109/JPHOTOV.2022.3195086.
[6] J.J. Perrenoud, B. Schaffner, S. Buecheler, A.N. Tiwari, Fabrication of flexible CdTe solar modules with monolithic cell interconnection, Sol. Energy Mater. Sol. Cells 95 (1) (2011) S8–S12.
[7] J.J. García-Ballesteros, I. Torres, S. Lauzurica, D. Canteli, J.J. Gandía, C. Molpeceres, Influence of laser scribing in the electrical properties of a-Si:H thin film photovoltaic modules, Sol. Energy Mater. Sol. Cells 95 (2011) 986–991.
[8] S.-J. Moon, J.-H. Yum, L. Löfgren, A. Walter, L. Sansonnens, M. Benkhaira, S. Nicolay, J. Bailat, C. Ballif, Laser-scribing patterning for the production of organometallic halide perovskite solar modules, IEEE J. Photovoltaics 5 (4) (2015) 1087–1092.
[9] B.N. Chicbkov, C. Momma, S. Nolte, F. yon Alvensleben, A. Tiinnermann, Femtosecond, picosecond and nanosecond laser ablation of solids, Appl. Phys. A 63 (1996) 109–115.
[10] T. Bucher, G. Brandal, H. Chen, Y.L. Yao, Quantifying the heat affected zone in laser scribing of thin film solar cells, Manuf. Lett. 13 (2017) 11–14.