Industrially Led MSc by Research Thesis

Testing Methodologies for Power Electronic Devices

With focus on

MOSFETs and IGBTs

Mengsteab Tesfamariam

Student number: [redacted]

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"እቲ ንብጻዩ ዜፍቅር ንሕጊ ፈጺምዎ እዩ እሞ፡ እታ ንሓድሕድኩም ምፍቓር እንተ ዘይኮይና፡
ንገለ እኳ ዕዳ ኣይሃሉኹም።"

መጽሓፍ ቅዱስ ሮሜ 13:8

In the memory of my father and my mother.

**”Owe no one anything, except to love one another;
for he who loves his neighbor has fulfilled the law.”**

Bible Romans 13:8

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Declarations

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

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This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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Abstract

Metal Oxide Semiconductor Field Effect Transistor ($MOSFETs$) and Insulated Gate Bipolar Transistor ($IGBTs$); both are the state-of-the-art semiconductor switching devices.
In this study an in-depth study of Metal Oxide Semiconductor (MOS) physics, cell structure and electrical characterization of MOSFETs and IGBTs has been conducted. The aim is to achieve a further improvement on the reliability and ruggedness of these power electronic devices using findings of the research. These power devices have an extensive industrial and domestic applications, they are the building blocks of nearly all types of power electronic circuits, control systems and advanced digital data storages, laptop and phone chargers, motor drives in electric vehicle, PV converters, Wind converters, industrial heaters. Power electronic monitoring systems including DC to DC converters, DC to AC inverters, AC to DC rectifiers and AC to AC converter.
Silvaco simulation and MATLAB modeling enabled the research to gain a vivid understanding of device operation MOS physics and all relevant electrical characteristics. The practical experiment side of the research includes high power semiconductor devices characterization; testing of fabricated discrete devices comprising: (200V, 40A Silicon MOSFET; 1.2KV, 19A Silicon Carbide MOSFET; 600V, 20A and 40A Silicon IGBT; 1.2KV, 25A Silicon IGBT). Consequently, the research work gained an insight to the semiconductor switching latest technologies that are useful for the optimization consideration of power electronic devices. Observations from published journals enabled to see the existing relevant research gaps and works carried out by other scientists around this field area. Silicon is the working material for this master's by research thesis. Moreover, this paper also looks into the great benefits of using silicon-carbide as a material for the next generation technological innovations.
Therefore, this research contributes towards device optimization in the following way:
Firstly, at a single cell design level. Shielded trench gate geometry architecture outperforms planar gate structure. Secondly, fabricating using a Wide-band-gap material (WBG) enhances device performance greatly.

1 Introduction

In this research endeavor both theoretical and practical work has been carried out on MOSFETs and IGBTs. The summation of efforts will contribute towards the enhancement of the reliability and ruggedness of high-power semiconductor devices. Specific attention was given to Metal Oxide Semiconductor Field Effect Transistor (MOSFETs) and Insulated Gate Bipolar Transistor (IGBTs). In both cases switching conditions under high and low DC supply voltage were measured. The results of two-dimensional numerical analysis on vertical device structures designed with a 200 V; 600 V; and 1200 V voltage ratings are described to validate the above model for the on-state resistance of the power MOSFET structure. Experimental data permit a closer study of the device operation physics, conduction and breakdown electrical characteristics. Subsequently, allowing to calculate the threshold voltage, saturation current and the on-state internal resistance.

1.1 Background

The twenty-first-century marks technological advancements and innovations in the industrial, domestic, and renewable energy engineering sectors. The impetus behind these developments is the enhancement in the reliability and ruggedness of semiconductor devices switching ability. Power electronic circuits can control and regulate the flow of electricity that drives industrial machines and domestic electrical appliances which are used for luxury, public health care and transportation. Thereby, motivating great advancements in electrical power generation, distribution, and management technologies. Silicon MOSFETs have found extensive use in high frequency applications with relatively low operating voltages (< 100 V). The power of research and innovation in the 1980s enabled creation of a new class of devices that combines together MOS physics and bipolar transistor. This resulted in IGBTs which have been the most successful innovative class of device. The IGBT has an advantage of high-power density and ruggedness. These qualities made IGBT the technology of choice for all medium and high-power applications, with perhaps the exception of high voltage DC transmission systems. High power IGBTs are widely used in power electronics applications with inductive load such as power converters, high power klystron modulators and motor drives. Silicon based switching devices; for instance, Thyristors are favoured for the low frequency, high power applications, IGBTs for the medium frequency and power applications, and power MOSFETs for the high frequency applications.

1.1.1 Spectrum of power electronic devices application

Electronic Device Application	Power Range in Watt
Phone chargers	5 - 25 W
Laptop chargers	40 - 100 W
Home Appliances	40 - 100 W
Laptop chargers	100 - 500 W
Charging stations	50 - 500 W
PV string converters	1 - 5 - 100 W
PV micro converters	100 W
PV central converters	> 100 KW
Hybrid Electric Vehicles and Pure EV	50 - 100 kW
Industrial Motor Drives	100 KW - 10 MW
Electric Trains	1 MW
Wind converters	1 - 10 MW
Grid	10 - 100 MW

Table 1: Spectrum of power electronic devices application [2][57].

1.2 Computer based simulations

The software used for the research work are SILVACO and MATLAB.

1. MATLAB modeling; applied in-depth study of MOS physics.
2. SILVACO simulation. Running downloaded learning materials.
3. Wolfson lab testing 'Tektonic Power Curve Tracer' on selected discrete MOSFETs and T-IGBTs.

1.3 Trench gate design architecture cell optimization

Having examined the current literature and identified gaps for next level targets of cell optimization in order to get a lower on-state resistance. Moreover, optimization refers to achieving significant improvements in the overall switching performances and reducing energy dissipation in the form of heat. One way of mitigating this problem is by using shielded trench-gate structure instead of planar gate, which eliminates the JFET region thereby minimizing internal resistance and corresponding power losses. For both MOSFETs and IGBTs shielded trench gate design architecture is highly recommended to avoid wasting of energy; further minimizes channel resistance by making it short and vertical

instead of longer horizontal. Furthermore, rounded trench gate corner architecture would reduce the high electric fields around the lower gate area and a novel shielded Fin MOSFET structure, creating thermal and electrical stability. The lower the on-state resistance (R_{ON}) would mean a very low or minimized forward voltage drop of the device.

1.4 SiC as a material for Power Electronics

Figure 1 below shows Silicon Carbide (SiC) as a material for power electronic switching and control applications. Choosing the right material for the desired power semiconductor device performance is crucial. The fast-growing technology proved an innovation and creativity possible by compounding silicon. Among new compound silicon technology is SiC based devices promises a significant reduction in switching losses and permits far higher switching frequencies than what is possible today using silicon as a material. Furthermore, companies like Infineon and Cree have started fabricating devices using silicon carbide, also commercialized.

1.4.1 Revolutionary silicon carbide

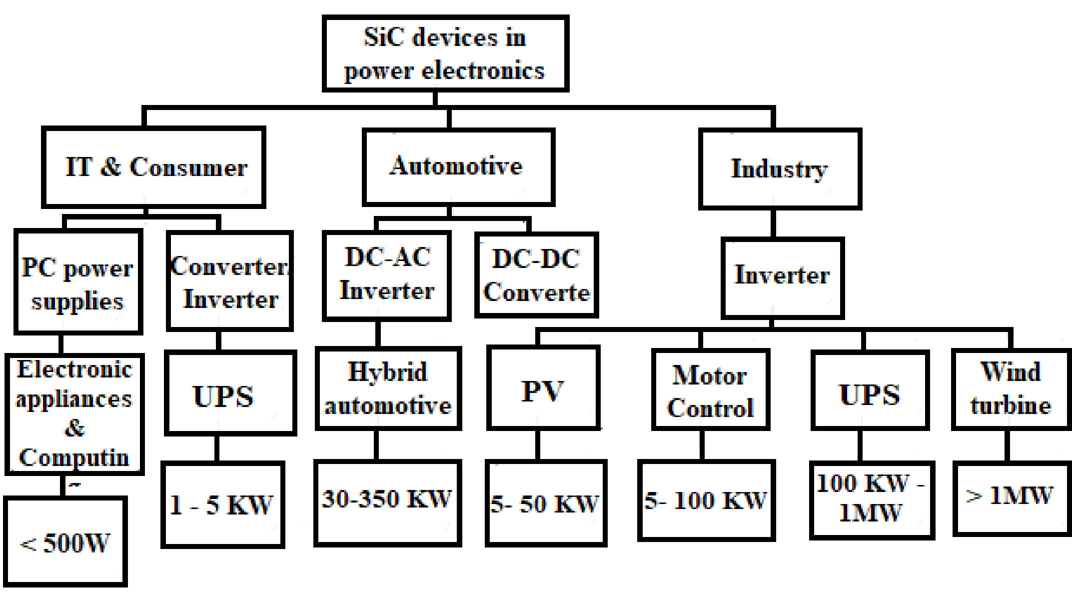


Figure 1: Silicon carbide devices in power electronics [19][58].

1.4.2 Wide bandgap (WBG) semiconductors

Wide band-gap power devices offer potential solutions, see figure 2 below. WBG power devices are better than silicon power devices for high voltage applications ($> 1000V$). Faster, lower losses, higher operating temperatures are the perceived benefits. WBG devices operate by the same physical mechanisms as silicon devices. WBG device geometries are the same as corresponding silicon devices. WBG have much better device characteristics due to superior material properties.

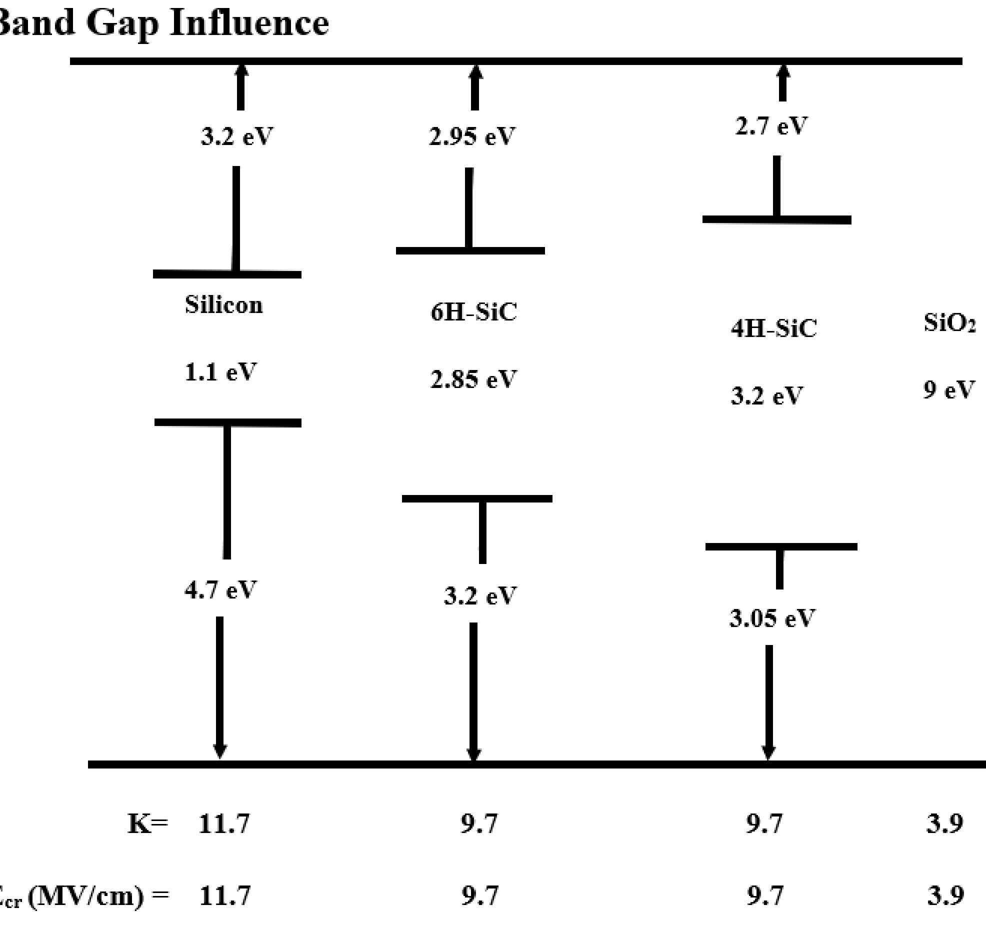


Figure 2: Silicon carbide vs Silicon Band Gap Influence [61][50].

1.5 Importance of power electronic switching devices

1.5.1 The currently in use technologies at Newport Wafer Fab (NWF)

Silicon is the raw material for power electronic devices in general, particularly MOSFETs and IGBTs. Processing silicon has been used for 50+ years. New materials have been developed which have enhanced silicon performance to a huge extent, for higher speeds, lower losses, and lower battery consumption. In addition, they can be used for different applications, such as light sensing and emitting across a large spectrum (photonics), RF applications, sensors, and medical applications where battery life is critical. The company Newport Wafer Fab (NWF) has unprecedented practical knowledge with analogue/advanced power and compound semiconductor technologies. The industrial partner has a monthly manufacturing capacity of 32,000 wafer starts typical minimum feature sizes of 0.18 µm to 0.70 µm wafers with an expansion capability within the existing envelope to 44,000 wafers starts per month. A wide range of advanced semiconductor technologies for power electronic applications were developed under NWF, including, but not limited to, MOSFETs / T-IGBTs using wafer thinning methods. CMOS, analogue, and compound semiconductors have also been developed.

2 Aims

1. To conduct industrially led research on power electronic devices with focus on MOSFETs and IGBTs.

2. To investigate semiconductor devices MOSFET/T-IGBT structure, operation physics and electrical characterization.

2.1 Objectives

1. To further improve the reliability and ruggedness of power electronic devices by using findings of the research.

2. To compare lab demonstration results with company data-sheet.

2.2 MOSFET & IGBT device research approach

1. MATHLAB modelling; studying MOS physics.

2. Silvaco simulation; running the downloaded examples.

3. Wolfson lab testing 'Tektonic Power Curve Tracer' on selected discrete IGBTs.

3 Theory and Literature Review

3.1 MATLAB modelling

MATLAB modelling were used in order to create a virtual representation of a physical semiconductor device that includes fundamental electrical properties and single cell geometrical structure. The specific on state resistance components of this model are driven by mathematical relationships, you can simulate this virtual representation under a wide range of conditions to see how it behaves.

3.2 Power U - MOSFET structure

Power trench gate or U - MOSFET single cell structure with current flow model (grey area) and all seven internal resistances used for analysis of enhanced on state resistance.

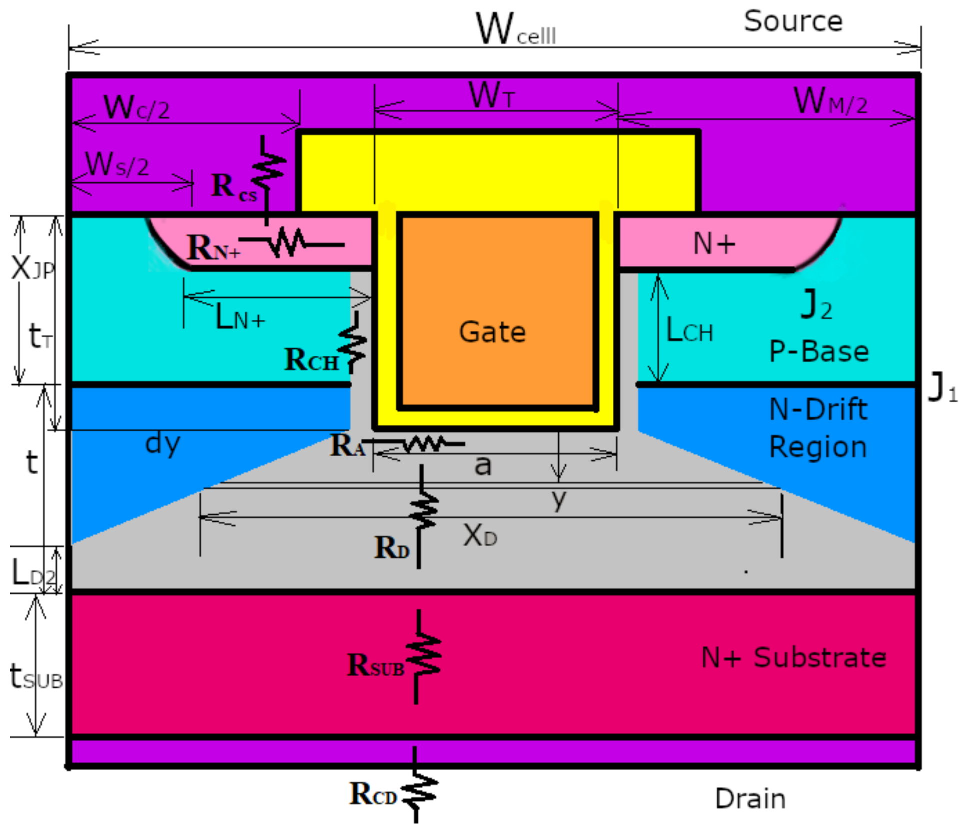


Figure 3: Trench gate MOSFET single cell structure [1][4].

3.3 Specific On-Resistance parameters

Description	Symbol	Unit
Channel length	L_{CH}	Cm
Gate oxide thickness	t_{ox}	Cm
Gate oxide capacitance	C_{ox}	$Farad$
Channel mobility	μ_{fe}	Cm^2/Vs
Drift region mobility	μ_D	Cm^2/Vs
Drift region thickness	t_d	Cm
Drift region doping concentration	N_D	Cm^-3
Drift region resistivity	ρ_D	$\Omega.Cm^2$
Contact to source resistivity	ρ_C	$\Omega.Cm^2$
Source region resistivity	ρ_S	$\Omega.Cm^2$
Substrate resistivity	ρ_{SUB}	$\Omega.Cm^2$
Substrate thickness	t_{SUB}	Cm
Trench gate thickness	t_T	Cm
Trench gate width	W_T	Cm
P - Base junction depth	X_{jp}	Cm
Contact width	W_C	Cm
Source width	W_S	Cm
Metal contact width	W_M	Cm
Cell-pitch	W_{Cell}	Cm
N+ well length	L_{N+}	Cm
Mesa width trench bottom	a	Cm
Division of metal width by 2	b	Cm
Trench gate length	Z	Cm
Threshold voltage	V_{Th}	$Volt$
Gate to source voltage	V_{Gs}	$Volt$
Boltzmann universal constant	K	$1.380649 \times 10^{-23} J/K$
Source to contact resistance	R_{cs}	$\Omega.Cm^2$
N+ source region resistance	R_{sn}	$\Omega.Cm^2$
Channel resistance	R_{CH}	$\Omega.Cm^2$
Accumulation region resistance	R_A	$\Omega.Cm^2$
Drift region resistance	R_D	$\Omega.Cm^2$
Substrate resistance	R_{SUB}	$\Omega.Cm^2$
Drain contact resistance	R_{CD}	$\Omega.Cm^2$

Table 2: Trench gate MOSFET On-resistance parameters [1].

3.4 Specific On-Resistance

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_D + R_{SUB} + R_{CD} \tag{1}$$

3.5 Contact to Source Resistance

$$R_{CS} = \frac{\rho_C.W_{cell}}{W_C - W_S} \tag{2}$$

3.6 N+ Region Resistance

$$R_{N+} = \frac{\rho_{SN+}.L_{N+}.W_{cell}}{2} \tag{3}$$

3.7 Channel Resistance

$$R_{CH} = \frac{L_{CH}.W_{cell}}{2.\mu_{fe}.C_{ox}.(V_{gs} - V_{Th})} \tag{4}$$

3.8 Accumulation Region Resistance

$$R_A = \frac{K_A.(W_G - 2X_{jp}).W_{cell}}{4.\mu_{fe}.C_{ox}.(V_G - V_{Th})} \tag{5}$$

3.9 Drift Region Resistance

$$R_D = \frac{\rho_D.W_{cell}}{2}.log\frac{W_T + W_M}{W_T} + \rho_D(t_D + X_{jp} - t_T - b) \tag{6}$$

3.10 Substrate Resistance

$$R_{SUB} = \rho_{SUB}.t_{SUB} \tag{7}$$

3.11 Contact to Drain Resistance

$$R_{CD} = \rho_C \tag{8}$$

3.12 Specific On-Resistance (MATHLAB MODELLING)

The MATLAB modeling code for the specific on-state resistance is shown at the back of the document. MATLAB CODE one refere appendix.

3.13 Theory buildup of 1D model

The 1-D Poisson equation is given by:

$$\frac{-d^2V}{dx^2} = \frac{dE}{dx} = \frac{Q(x)}{\epsilon_s} \tag{9}$$

Where: E is the electric field; x is the distance; ϵ_s is the permittivity of the semiconductor and $Q(x)$ is the charge density within the depletion region at point x.
The unipolar limit on-state resistance R_{ON} versus breakdown voltage V_{BR} is given by:

$$R_{ON} = \frac{W_{cell}V_{BR}}{2\mu\epsilon_s E_C^2} \tag{10}$$

Where: W_{cell} is cell pitch (μm); V_{BR} is breakdown voltage (V); μ is electron mobility (cm^2/Vs); ϵ_s is the permittivity of the semiconductor and E_C is the critical electric field strength (V/cm).

3.14 Threshold Voltage vs Oxide Thickness Equation

$$V_{Th} = \frac{t_{ox}}{\epsilon_{ox}}\sqrt{4\epsilon_s K N_A \ln\left[\frac{N_A}{n_i}\right]} \tag{11}$$

Where:

Threshold voltage (V_T) in volt Gate oxide thickness (t_ox) in Angstrom Oxide permittivity (ϵ_{ox}) in farad per meter (F/m) Semiconductor dielectric (ϵ_s) in volts per meter (V/m) Doping concentration (N_A) in (cm3) Intrinsic carrier concentration (n_i) in (m^{-3}) Boltzmann universal constant (K) in ($J.K-1$) Temperature (K) in Kelvin

3.14.1 Threshold voltage vs Oxide thickness (MATHLAB MODELLING)

The MATLAB modeling code for the specific on-state resistance is shown at the back of the document. MATLAB CODE two refere appendix.

3.15 Theory IGBT

3.15.1 Blocking characteristics of IGBT

IGBT symmetric structure has forward blocking characteristics in the first quadrant of operation and reverse blocking characteristics in the third quadrant of operation.

3.15.2 Forward blocking characteristics

At the collector terminal a positive bias voltage is applied: Junction 'J_2' becomes reverse biased and Junction 'J_1' becomes forward biased.

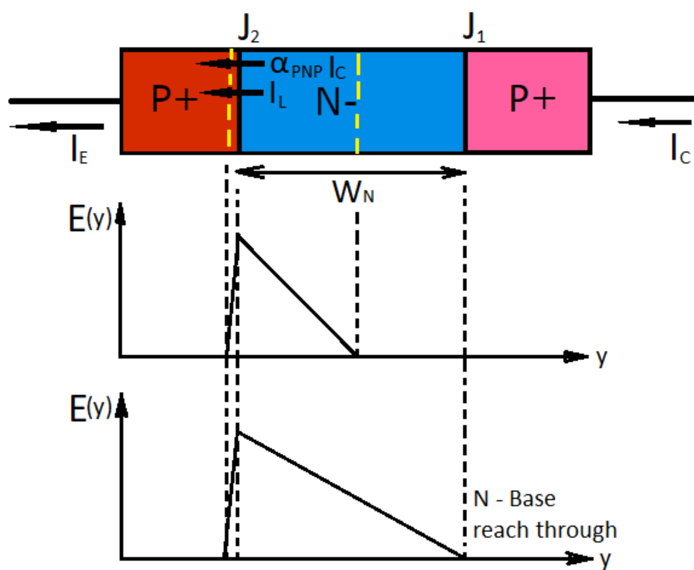


Figure 4: Symmetric IGBT forward blocking mode electric field distribution [1][4].

3.15.3 Reverse blocking characteristics

At the collector terminal a negative bias voltage is applied: Junction 'J_1' becomes reverse biased and Junction 'J_2' becomes forward biased.

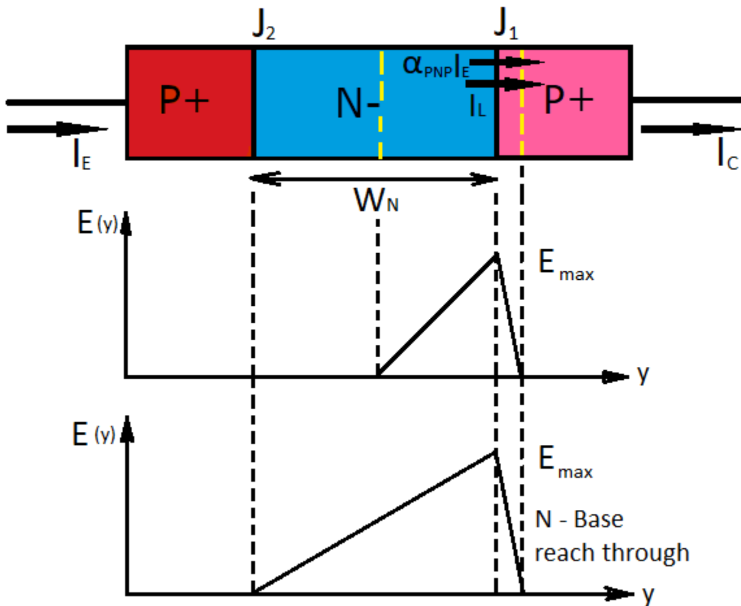


Figure 5: Symmetric IGBT reverse blocking mode electric field distribution [1][4].

3.16 Non-punch-through-Design of IGBT

Symmetric structure forward blocking capability.

High Voltage P-i-N Diode.

Breakdown Voltage of P-i-N Diode

Without N+ buffer layer, IGBT has large reverse blocking capability and it is known as symmetric IGBT.

3.17 Non-punch-through Design Equations

$$W_D = \frac{2V_{BR}}{E_C} \tag{12}$$

$$N_D = \frac{E_C^2 \epsilon_s}{2qV_{BR}} \tag{13}$$

The breakdown voltage V_{BR} for ideal P-i-N diode much higher than just PN diode. At the P+N- junction the critical electric field E_C will increase until it reaches the critical breakdown field. As we apply reverse bias voltage we will mostly deplete in the N- drift region side.

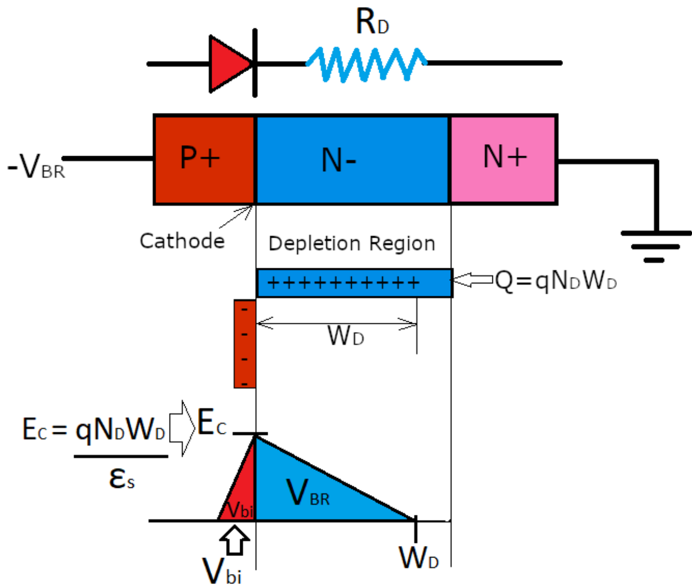


Figure 6: Non-punch-through design of IGBT [1][4].

3.18 Punch through IGBT Cell Cross Section

With N+ buffer layer, junction J_1 has small breakdown voltage and thus IGBT has little reverse blocking capability – anti-symmetric IGBT. The N+ buffer layer speeds up device turn-off.

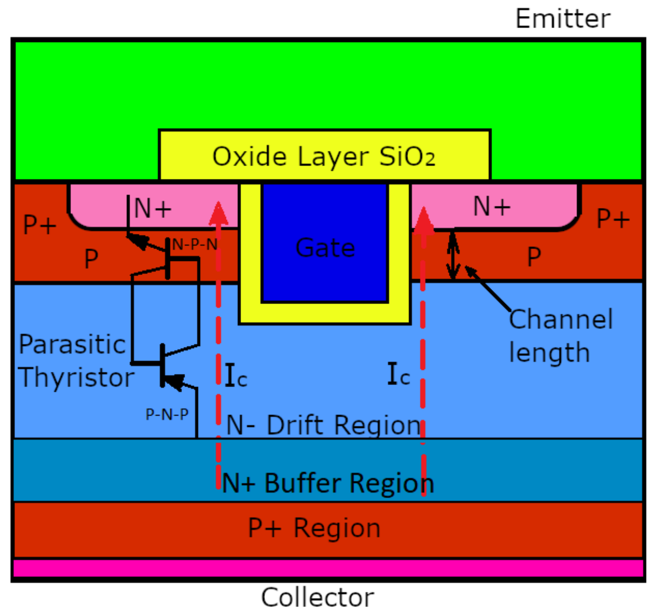


Figure 7: Punch through IGBT single cell cross section [1][4].

3.19 Punch through Design

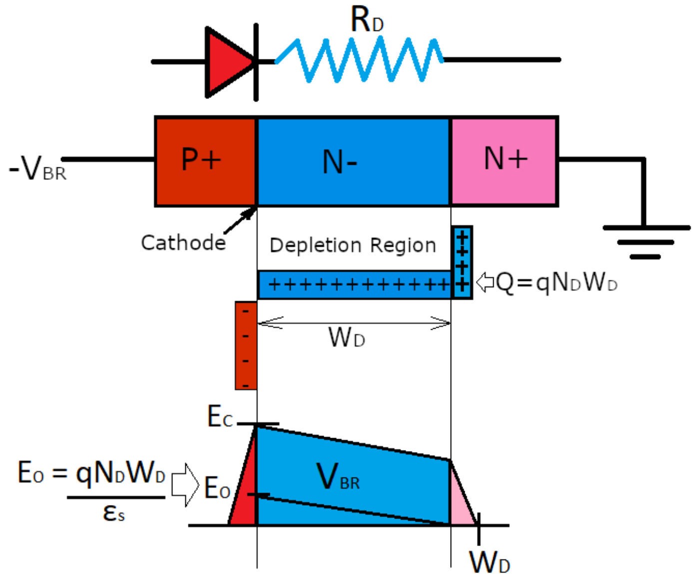


Figure 8: Punch through IGBT equivalent circuit [1][4].

Infinite combinations of doping concentration N_D and drift region width W_D for a given breakdown voltage V_{BR} are possible.
The emitter current for the IGBT structure includes both the hole current flow via the PNP transistor I_p and the electron current via the MOSFET portion I_n:

$$I_E = I_p + I_n \tag{14}$$

$$I_p = \beta I_n = (\frac{\alpha_{pnp}}{1 - \alpha_{pnp}})I_n \tag{15}$$

Substituting equation 15 into equation 14 gives:

$$I_E = (\frac{I_n}{1 - \alpha_{pnp}}) \tag{16}$$

Where:

$$I_{D_{sat}} = \mu_{eff} C_{ox} \frac{W}{2L} \left[(V_G - V_T)^2 \right] = I_n \tag{17}$$

This gives the saturation emitter current equation:

$$I_{E_{sat}} = \mu_{eff} C_{ox} \frac{W}{2L(1 - \alpha_{pnp})} \left[(V_G - V_T)^2 \right] \tag{18}$$

4 Metal Oxide Semiconductor Field Effect Transistor

MOSFET is an acronym for Metal Oxide Semiconductor Field Effect Transistor, alternatively referred as the Metal Oxide Silicon (MOS) transistor, it is a type of Insulated Gate Field Effect Transistor (IG-FET) that is fabricated by the controlled thermal oxidation of a semiconductor, typically silicon. MOSFETs are a special type of field-effect transistor in which the applied voltage determines the conductivity of a device. Power MOSFET is a voltage-controlled device. The electronic switching device begins to operate after a voltage is applied at the gate terminal and a current starts to flow through the drain to source created channel. The figure 9 below shows a chart with two types of N-channel MOSFETs; these are enhancement and depletion - types. The n-channel enhancement type MOSFET is investigated in this section and the device is normally off when the gate-source voltage is zero volts.

4.1 Field Effect Transistors (FETs) Chart

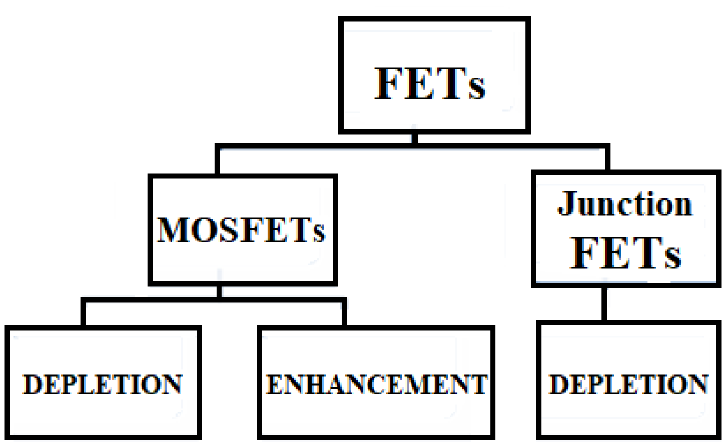


Figure 9: Field Effect Transistors Chart [26][59].

4.2 n-Channel Enhancement type MOSFETs

Lateral gate n-channel enhancement type MOSFETs are usually specified for audio signal amplification purposes. This type of MOSFETs enter their linear phase at a lower bias voltage than vertical MOSFETs. Figure 10 shows lateral gate n-channel enhancement type MOSFET which consists of three terminals: Source (S), Gate (G), Drain (D).

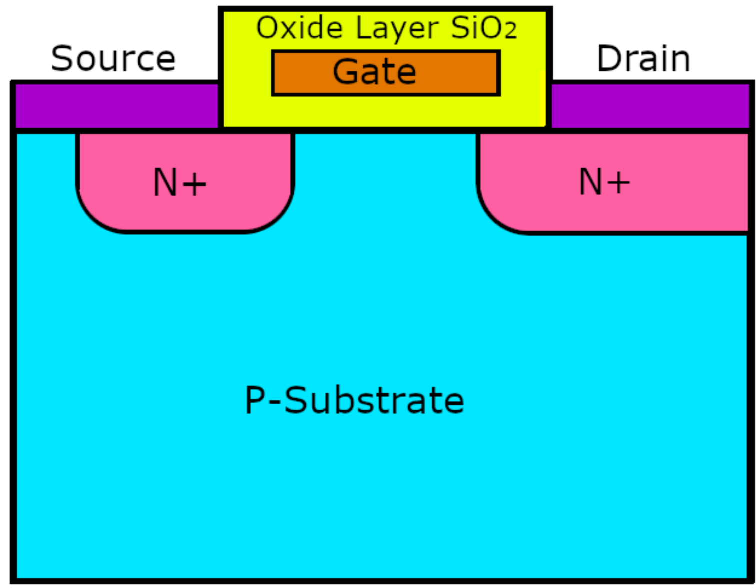


Figure 10: Lateral n-channel MOSFET: Source, Gate, Drain.

Figure 10 above shows the simplest case of a lateral MOS field effect transistor (MOSFET). A positive voltage has the same effect as the positive surface charge: When a sufficiently enough positive voltage at the gate is applied, both n-areas are connected by the created inversion layer or channel. The threshold voltage of a MOSFET is defined as the minimum gate-to-source voltage (V_T) that is applied to create a conducting channel between the source and drain terminals. It is an important MOSFET scaling factor to maintain power efficiency. When the gate voltage exceeds the threshold voltage, $V_G > V_T$, a current will start to flow between the drain and the source. The electrical properties of the created channel determine the on-state resistance (R_{ON}) and the output or I – V characteristics of the device. Through created channel the source and drain are connected; this means that a large current can flow through the conducting surface n-channel. The conductance of this channel can be modulated by varying the gate voltage.

4.3 MOS physics

Investigation of MOSFET channel electrical characteristics using a lateral gate structure.

4.4 Ohmic region:

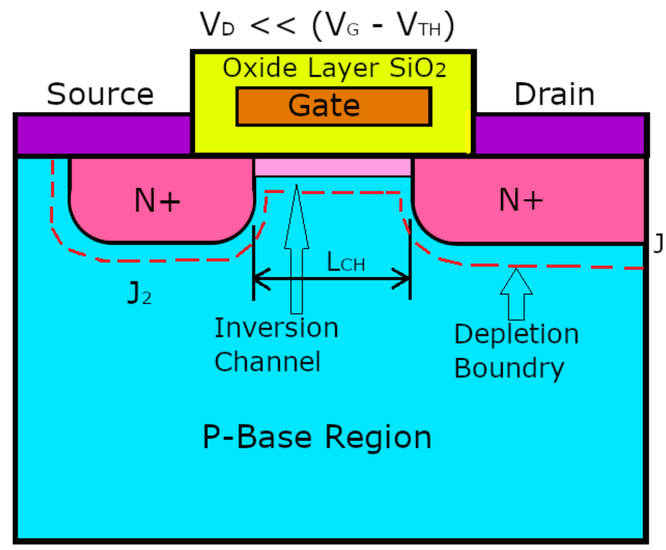


Figure 11: Lateral MOSFET operating at Ohmic or linear region.

Figure 11 shows channel induced under very small drain bias voltages.

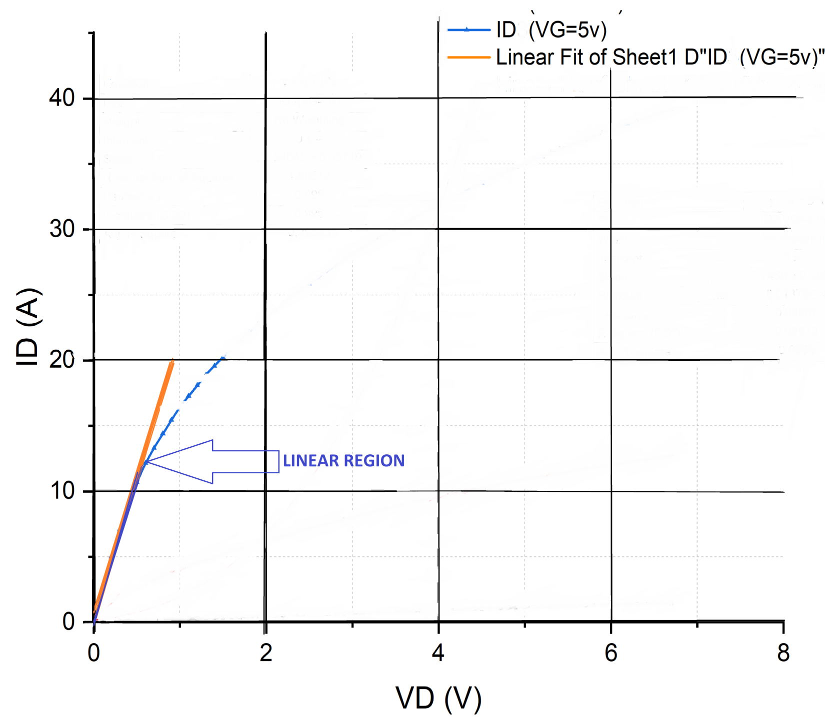


Figure 12: Graph of MOSFET operating at Ohmic or linear region.

I - V curve shows the MOSFET operates like a voltage controlled linear resistor.

The lateral n-channel enhancement type MOSFET structure shown in figure 11 above is made up of N+ source region and N+ drain region, both N+ well regions created in a p-type silicon substrate. The electrical conduction properties of the channel can further be studied by using this basic lateral n-channel MOSFET structure. Furthermore, it can be seen in the figure 11 structure the p-type substrate region and the source contact metal connection are established by overlapping junction (J2) between the N+ source region and p-type substrate. Junction (J_1) becomes reverse biased, this is due to a positive bias voltage applied to the drain electrode, junction one is in between the N+ well drain side and p-type base regions. If there is no gate bias voltage, no drain current can flow in between the source and drain of the lateral n-channel MOSFET, with the voltage supported by Junction (J_1). Nevertheless, if a positive gate bias voltage is applied at the gate terminal greater than the threshold voltage (V_T) for the lateral n-channel MOSFET structure, just underneath the gate a strong inversion layer is formed thereby inducing or creating the channel. This induced region is called an inversion layer or channel, and drain current will start to flow between the source and drain terminals. Therefore, the n-channel enhancement type MOSFET enters inversion mode. Inversion layer charge is uniformly distributed throughout the channel, when the applied drain bias voltage is smaller compared with the gate bias voltage. Consequently, the figure 11 above clearly shows a channel with a uniform thickness along the entire channel.

4.4.1 Linear or triode region CALCULATIONS

The charge in the inversion layer or channel is supported by:

$$(V_G - V_T - V_D) \tag{19}$$

$$Q_i = -C_{ox}(V_G - V_T - V_D) \tag{20}$$

The channel drift current is:

$$I_D = W\mu_{eff}Q_i\epsilon_y \tag{21}$$

Since

$$\epsilon_y = \frac{-dV_G}{dy} \tag{22}$$

Where: ϵ_y is the permittivity.
Substitution gives:

$$I_D = W\mu_{eff}Q_i\Big(\frac{-dV_G}{dy}\Big) \tag{23}$$

$$I_D dy = W\mu_{eff}Q_i(-dV_G) \tag{24}$$

$$I_D dy = W\mu_{eff}(-C_{ox})(V_G - V_T - V_D)(-dV_D) \tag{25}$$

Integrating from $(y = 0)$ to $(y = L)$ on the (Left), and Integrating from $(V_D = 0)$ to $(V_D = V_D)$ on the (Right).
This gives the derived linear region drain current equation:

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_G - V_T)V_D - \frac{1}{2}{V_D}^2\right] \tag{26}$$

V_G: is the gate voltage; V_T: is the threshold voltage; V_T: is the drain voltage Q_i: is the Inversion layer charge; C_{ox}: is oxide capacitance; I_D: is channel drift current W: is channel width; μ_{eff} : electron mobility; ϵ_y: is the permittivity.
Furthermore, the inversion layer or channel resistance R_{CH} is calculated by using following equation:

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{ox}(V_G - V_T)} \tag{27}$$

Where: L_{CH}: is the length of the channel see figure 11 above; Z: is the width of the channel orthogonal to the cross section in the figure 11 above; μ_{ni} : inversion layer electron mobility. The inversion layer or channel resistance R_{CH} for the lateral n-channel MOSFET is a function of the gate bias voltage V_G and drain V_D bias voltages.

4.5 Pinch – off region:

$$(V_D = V_G - V_T) \tag{28}$$

The pinch - off region is observed when the drain voltage VD is equal to the difference between the gate bias voltage VG and the threshold voltage V_T ; i.e. $V_D = V_G$ - V_T. The gate voltage will be neutralized (or equalled) by the increase in the drain voltage and because of this drain voltage increase the inversion layer will eventually disappear (pinches-off) at the drain end of the channel. This phenomenon is called channel pinch off and the continuous increase in the drain voltage brings no significant change in the drain current. Therefore, the drain current enters saturation mode and no more valid is the derived linear region drain current equation 26 above.

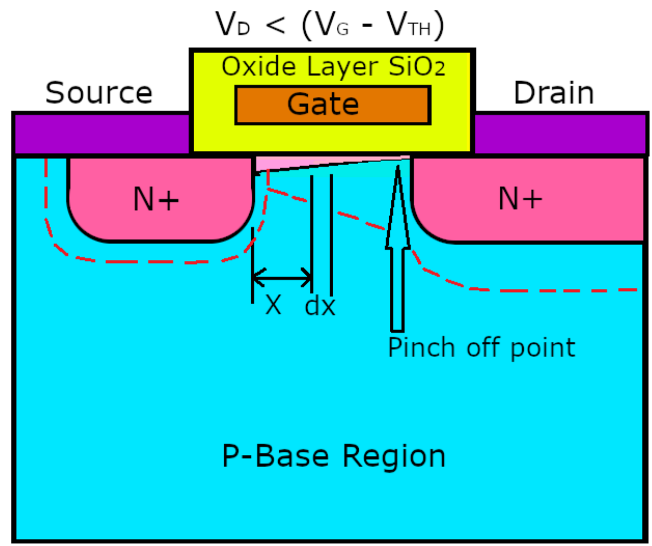
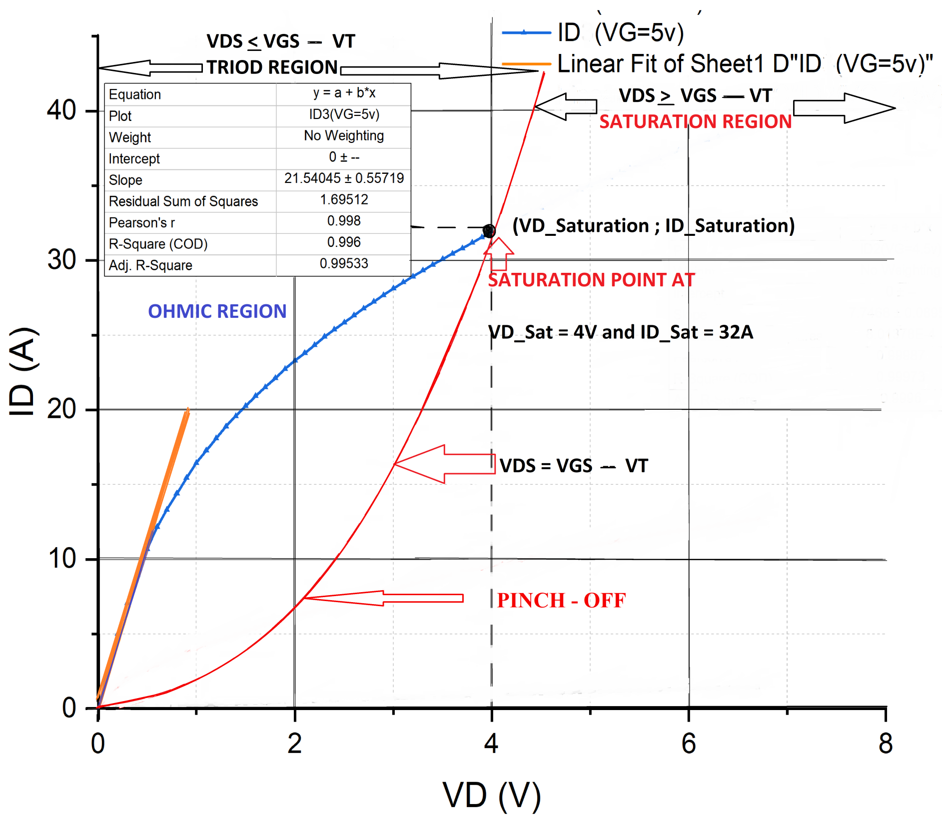


Figure 13: Lateral MOSFET operating at Pinch-off region.



Equation	y = a + b*x
Plot	ID3(VG=5v)
Weight	No Weighting
Intercept	0 ± --
Slope	21.54045 ± 0.55719
Residual Sum of Squares	1.69512
Pearson's r	0.998
R-Square (COD)	0.996
Adj. R-Square	0.99533

Figure 14: Output waveform of MOSFET operating at Pinch-off.

The inversion charge at the drain end:

$$Q_i(L) = -C_{ox}(V_G - V_T - V_D) \tag{29}$$

The onset of the saturation is given by setting inversion layer charge to zero:

$$Q_i = -C_{ox}(V_G - V_T - V_D) = 0 \tag{30}$$

This gives the saturation voltage to be:

$$V_{Dsat} = V_G - V_T \tag{31}$$

Substitution of the saturation voltage into the drain current expression gives the onset saturation current equation:

$$I_{D_{sat}} = \mu_{eff} C_{ox} \frac{W}{2L} \left[(V_G - V_T)^2 \right] \tag{32}$$

When current flowing between drain and source increases; there exist a measurable amount of voltage drop in the created channel because of the finite resistance R_{CH}. The applied gate bias voltage is opposed by the significant positive voltage accumulated in the channel due to current flow. Consequently, the charge in the channel decreases at the drain side of the created channel; in comparison with the charge produced at the source side of the channel. Figurative illustration of the channel in figure 13; the channel region thickness at the drain side is smaller or almost zero in contrast with the source side of the channel. The drain saturation voltage equation as shown in section 4.5, equation 28; is due to the increasing drain current and the corresponding drain bias voltage increasing until its value equals to the gate bias voltage minus the threshold voltage. At the drain saturation voltage there exist no significant voltage difference between the gate and the semiconductor to produce a strong inversion layer at the drain side of the channel.

4.6 Channel length shortening:

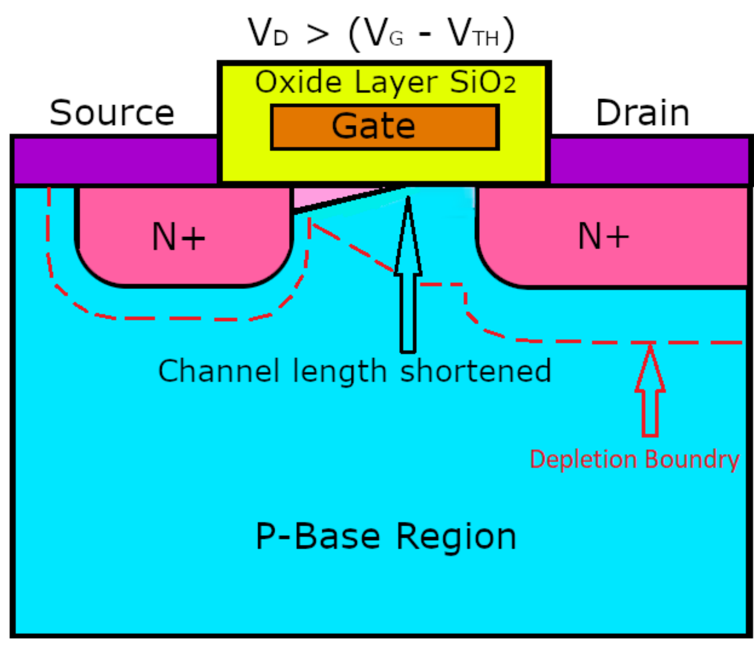


Figure 15: Lateral MOSFET operating with channel length shortened.

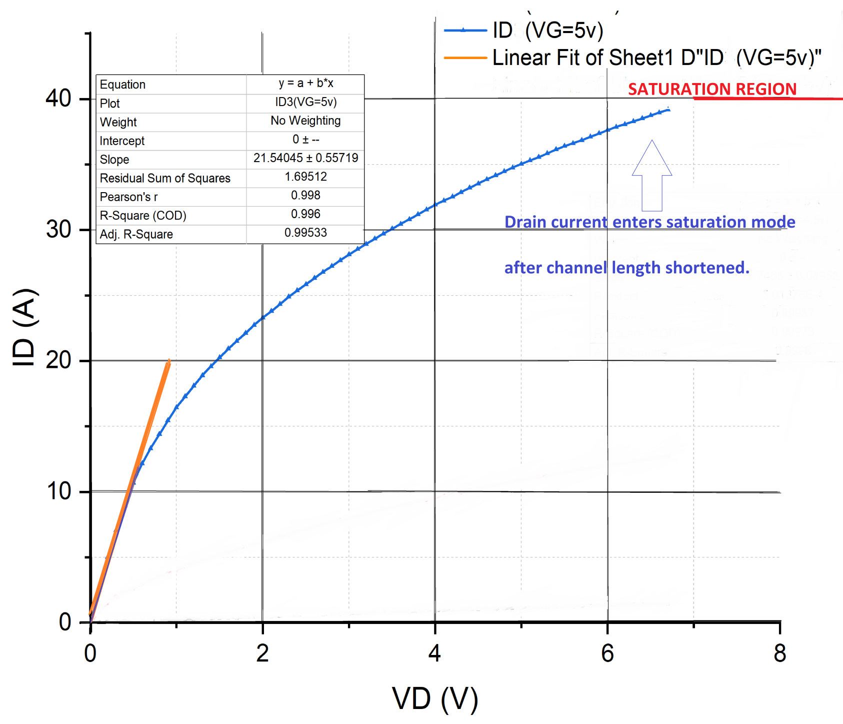


Figure 16: Output of MOSFET operating with channel length shortened.

The channel length shortening or short-channel effect is due to the increase in the drain bias for bigger values of drain biases. The result of channel length modulation is an increase in current with drain bias and a reduction of output resistance. Figure 15 above shows shortened channel length. The basic lateral n-channel MOSFET structure is used here to analyse the short channel electrical characteristics. The drain current goes into saturation mode after the drain voltage is increased well beyond the voltage value needed to create channel pinch-off conditions. The extra drain voltage is supported along the channel with a depletion boundary established in the middle of the end corner of the induced channel and the N+ well drain side, see figure 15 above. Even though the inversion layer does not extend along the whole channel length, there exist a drain current flow due to electrons are conveyed from induced channel end corner through the depletion boundary area by the created lengthwise electrical field. The channel length is shortened due to above stated operating conditions causing definable output resistance for the n-channel MOSFET.

4.7 Planar gate VD - MOSFET

Figure 17 shows Planar gate Vertical Double Diffused Metal Oxide Semiconductor Field Effect Transistor (VD - MOSFET), device design and structure. This type of VD-MOSFET structure has a planar gate, horizontal or lateral channel implanted by photolithography, N+ well, P base, a JFET region formed on the upper N-drift region and N+ substrate.

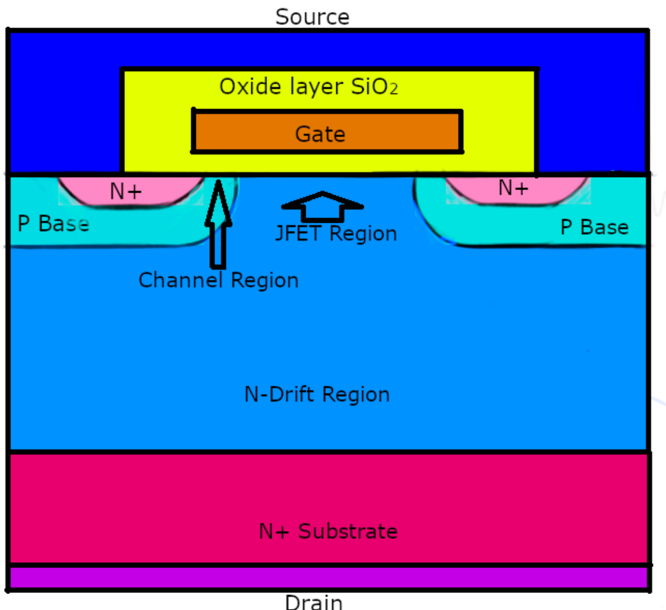


Figure 17: VD-MOSFET single cell structure [1][4].

4.7.1 Planar gate VD-MOSFET Internal Resistance (R_{ON})

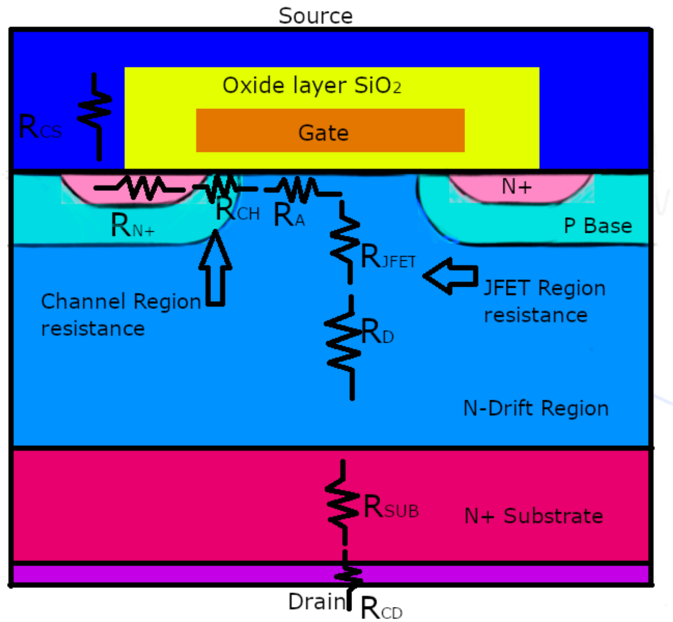


Figure 18: VD-MOSFET structure with all eight internal resistances [1][4].

Summation of all eight Internal Resistance (R_{ON}):

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \tag{33}$$

The total internal on-state resistance (R_{ON}) is the summation of all eight internal resistances; i.e. contact to source resistance R_{CS}; N+ well to source resistance (R_{N+}); channel resistance (R_{CH}); accumulation region resistance (R_A); JFET region resistance (R_{JFET}); drift region resistance (R_D); N+ substrate resistance (R_{SUB}); and drain metal contact resistance (R_{CD}). Figure 18 shows the cross section of a VD-MOSFET and the verticality of the device; it can be seen that the source electrode is placed over the drain electrode, resulting in a current mainly vertical when the transistor is in the on-state. The planar structure exhibits significant amount of internal on-resistance, the JFET region, the drift region and the channel resistances are among the biggest percentage contributors towards the total on-state resistance. This means that we need to find a method to optimize the structure. Nevertheless, trench gate power MOSFETs have a different geometrical structure from the planar VD-MOSFET. The trench gate channel is vertical and not horizontal or planar.

4.8 Trench gate Power MOSFET

Trench gate power MOSFET structure single cell-pitch analysis approach were used in order to achieve the minimum possible on-state resistance.

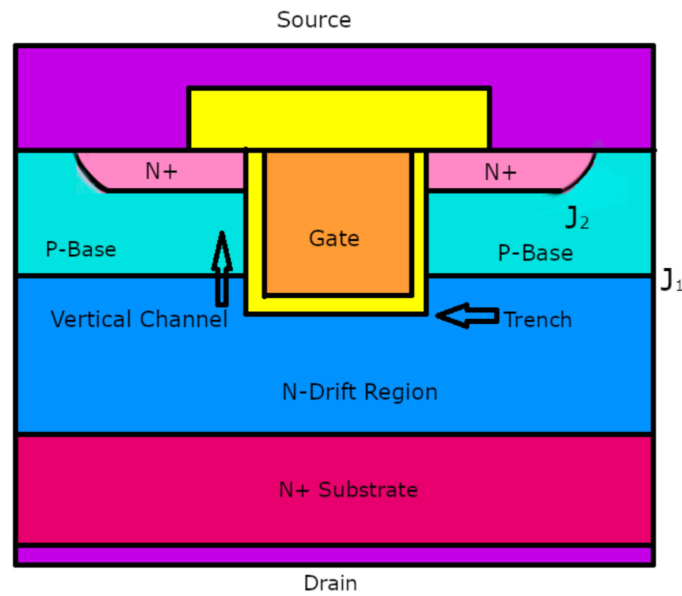


Figure 19: Trench or U – MOSFET single cell structure [1][4].

First and for most elimination of the JFET region for the VD-MOSFET structure shown in figure 18 above is very crucial. This removal of the JFET region will significantly reduce the on-state internal resistance value. Alternatively, designing a structure by deploying trench gate innovative technology can optimize the planar VD-MOSFET structure. This will enable the power VD-MOSFET operation frequency to increase from 100KHZ to 1MHZ range. Figure 19 above shows trench gate or U - MOSFET single cell structure. The structure has got no JFET region this means smaller cell-pitch; because no JFET region many smaller MOSFET channels. The trench gate MOSFET is a lot better than planar D - MOSFET for two reasons; the pitch is very small and the vertical electron mobility is higher than the horizontal. Silicon Carbide trench MOSFETs make sense upto 1700 V devices; however above 1700 V devices drift resistance goes up. For 600 V and 900 V devices operate really good.

4.8.1 Trench gate VD-MOSFET Internal Resistance (R_{DS-ON})

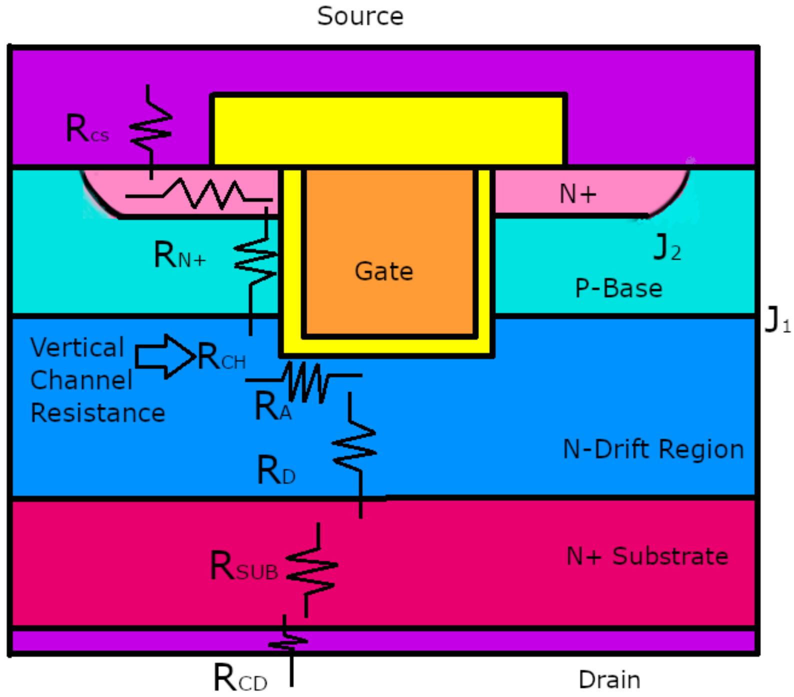


Figure 20: Trench or U – MOSFET structure with internal resistances [1][4].

Summation of all seven internal resistances (R_{ON}) of trench gate MOSFET.

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_{A} + R_{D} + R_{SUB} + R_{CD} \quad (34)$$

4.9 The advantages of trench gate MOSFET

There are several advantages of trench gate MOSFET over planar gate VD-MOSFET structure. Trench gate MOSFET or U-MOS is designed at aiming to increase the channel density by making the channel vertical. High power MOSFETs are fabricated having a vertical structure rather than a planar structure. Power MOSFETs are designed to handle large amount of power levels. The main advantage of a power MOSFET is its high commutation speed and good efficiency when operating at low voltage. The other advantage of the vertical MOSFET is the possibility to prevent short channel effects from dominating the transistor by adding processes that are not easily realized in horizontal transistors, such as a polysilicon (or poly SiGe) source to reduce parasitic bipolar effects or a dielectric pocket to reduce drain current. Trench MOSFETs are suitable power device for low to medium voltage power applications by offering the lowest possible on-state resistance among all MOS devices. As mentioned earlier among the big advantages of

making trench MOSFETs is that we have no JFET region in the structure as a result of this the cell size can be shrinked. This means many small MOSFET gate channels per unit area by reducing the cell-pitch and that reduces on-state resistance (R_{ON}) significantly for both silicon and silicon carbide devices. In the trench gate MOSFET since the p-type region is epitaxially grown; we can easily make submicron channel length by just growing thinner p-epi, for instance 0.1 or 0.2 Microns. The disadvantage of silicon carbide trench gate MOSFET is a high electric field at the trench corner. This is due to the higher breakdown field (2 MV/cm) and if we multiply this figure by a factor of three to get the gate oxide breakdown field (2 MV/cm x 3 = 6 MV/cm) this means that unreliable gate oxide. Therefore, we need to find a solution for this problem. One way of mitigating this problem is rounding the trench corners to distribute the electric field at trench corners.

4.10 Optimization for trench MOSFET vs D - MOS

Optimization of the power trench or U MOSFET structure requires adjustment of the pitch to obtain the lowest possible specific internal on-resistance. Figure 21 shows power U-MOSFET structure with current flow model used for studying and analytically quantifying its internal resistances.

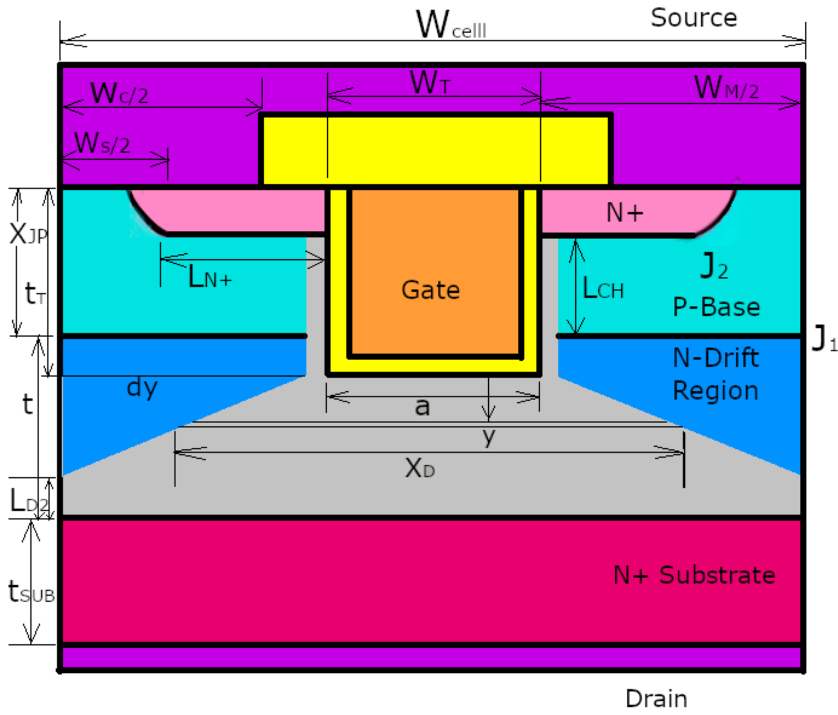


Figure 21: Trench MOSFET structure drift region current flow pattern [1][4].

Figure 21 above showing drift region current flow pattern (grey area) and the corre-

sponding parameters for the trench MOSFET structure. Mathematical calculation was performed to get the structure dimensions by using the relevant equations and the calculated values were implemented in MATLAB modelling. Consequently, the simulation output waveforms (see figure 22) were used in the study of the specific internal resistance versus cell-pitch relationship. The analytical approach used helped to give theoretical low internal on-state resistance. The technique performed were narrowing the gap between multiple trench gates versus cell-pitch geometrically adjustment. The main task is to bring the trench gates as close as possible without triggering a short circuit or accumulation of electric field between successive trench gates. Smaller MOSFET cell-pitch means lower or greatly enhanced internal specific on-state resistance R_{ON}. Smaller cell-pitch also means minimized MOSFET size, i.e. their length, this helps to achieve higher switching speed and cheaper cost. However, as MOSFET size gets smaller the corresponding capacitance is also reduced, this will increase operating speed. More MOSFET dies per single wafer means, dividing the overall cost of a single wafer among more dies. Modern technological innovation on vertical double diffused MOSFETs created a highly reliable with low internal on-state resistance switching device. Furthermore, the most important engineering work needed are trench gate refill planarization, trench corner electric field shielding, sacrificial trench gate oxidation, avalanche protection, and substrate engineering. There exists a limit as to how thin the trench gates can be made. The N+ source region and P+ body region are formed by a double diffusion process, an etched trench of narrow width, for instance (0.8 to 1.5 µm) across is oxidized to form a gate oxide lining the trench and subsequently filled with polysilicon.

4.10.1 MATLAB modelling output family of curves

The specific on-state resistance vs cell-pitch analysis for the trench gate MOSFET structure shown in figure 21. Silicon Carbide Trench MOSFET 1.2 KV, 20 A.

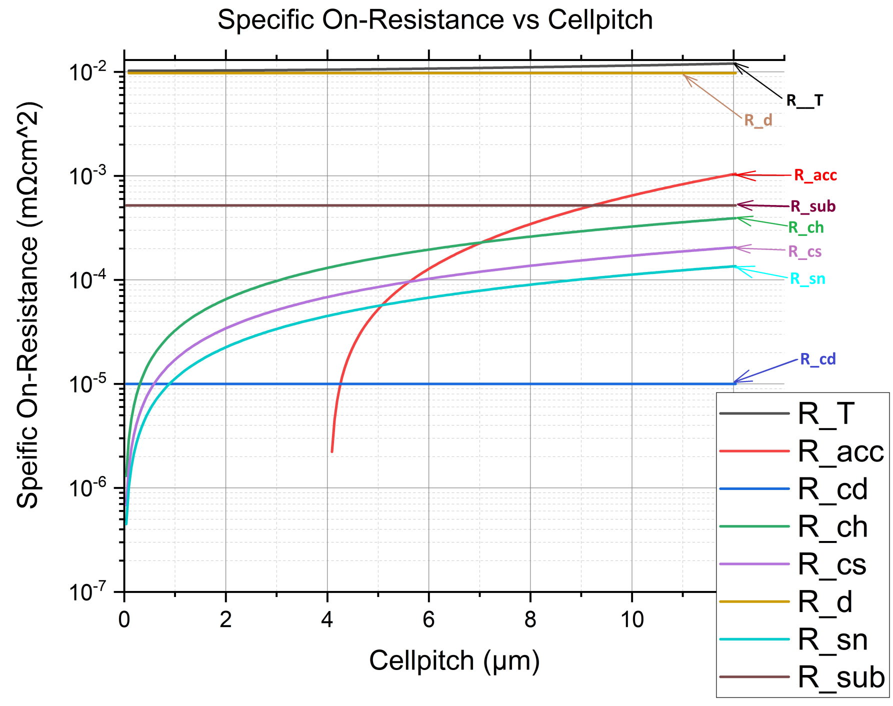


Figure 22: SiC Trench MOSFET 1.2 KV, 20 A, family of curves [60].

For figure 22 curve the MATLAB code (one) is posted on the appendix.

Internal resistance R_{ON}	Absolute contribution ($\Omega.cm^2$)	Percentage Contribution
Source to Contact R_{cs}	0.000206	1.712
Source to N-well R_{sn}	0.000135	1.122
Channel R_{ch}	0.000392	3.258
Drift R_d	0.00972	80.79
Substrate R_{sub}	0.00052	4.332
Accumulation R_{ch}	0.001047	8.703
Drain Contact R_{cd}	0.00001	0.083
Total R_{ON}	0.012030204	100

Table 3: SiC Trench MOSFET R_{ON} Absolute and Percentage Contributions [60].

The figure 22 above shows specific on-resistance vs cell pitch analysis of a trench gate SiC MOSFET simulation output family of waveforms. The total on-resistance R_T is the summation of all seven internal resistances, indicated by the black line at the top of the

curves. The drift region internal resistance indicated by the brown colour is the biggest internal resistance contributor approximately 80.79 % of the overall on-resistance R_{ON}. The accumulation region internal resistance is indicated by the red colour in the middle of the graph 8.703 %. The substrate region internal resistance also labelled in the graph is 4.332 %. The channel internal resistance is shown by the green colour and its percentage contribution is approximately 3.258 % of the overall on-resistance. The source contact internal resistance is shown by the indigo colour in the graph is 1.712 %. The source region internal resistance is shown by the light blue colour in the graph is 1.122 %. The drain contact internal resistance is shown by blue colour line of the graph is 0.083 %.

4.10.2 Optimization for lateral D - MOS

Optimization of double-diffused MOS (D - MOS) structure requires adjustment of cell-pitch. The channel length, L_{CH}, is adjusted by the junction depth formed by the N+ and P-type diffusions underneath the gate oxide. The lateral channel length L_{CH} is the horizontal distance between the N+ P junction and the P-N substrate junction. The channel length can be made to a smaller distance of about 0.5 μm.
MATLAB modelling of the internal specific on-state resistance versus cell-pitch analysis for the lateral gate D - MOS structure is shown in figure 23.
Silicon Carbide lateral gate MOSFET 1.2KV, 20 A.

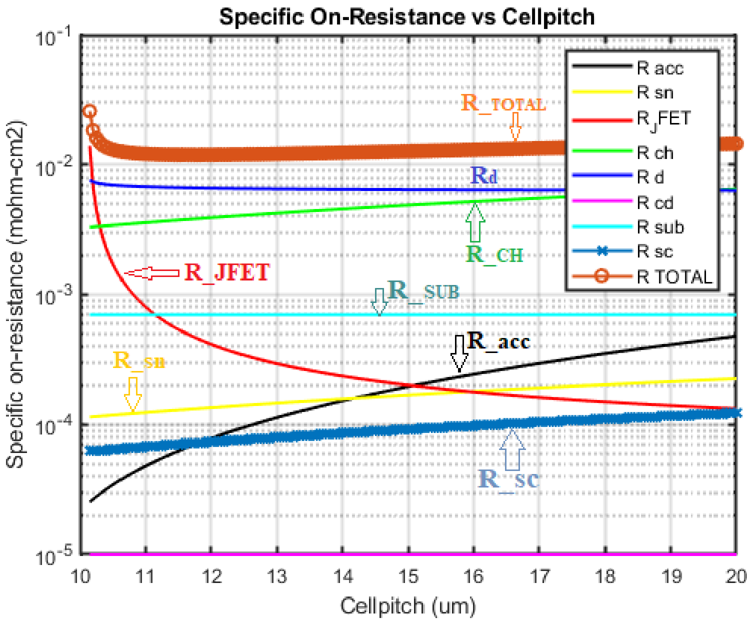


Figure 23: SiC D - MOS 1.2 KV, 20 A, output family of curves [60].

For figure 23 curve the MATLAB code (two) is posted on the appendix.

Internal resistance R_{ON}	Absolute contribution ($\Omega.cm^2$)	Percentage Contribution
Drain Contact R_{cd}	1.0 X 10 $^{-}$5	0.038
Substrate R_{sub}	7.0 X 10^{-}4	2.713
Drift R_d	0.0076	29.457
Accumulation R_{acc}	2.5364 X 10^{-}5	0.098
Channel R_{ch}	0.0033	12.79
Source to N-well R_{sn}	1.1419 X 10^4	0.44
Source to Contact R_{cs}	6.2156 X 10^{-}5	0.2409
JFET region R_{JFET}	0.014	54.263
Total R_{ON}	0.0258	100

Table 4: SiC D - MOS resistance R_{ON} Absolute and Percentage Contributions [60].

As depicted in table 4 the overall internal on-state resistance value of a SiC planar gate D - MOS ($R_{ON} = 0.0258\ \Omega cm^2$) is much higher when compared to SiC trench MOSFET as indicated in table 3 ($R_{ON} = 0.012\ \Omega cm^2$); (2.1446 times greater). This is mainly because of the JFET region resistance contribution ($R_{JFET} = 54.263$ %). The trench gate geometrical design architecture eliminates the JFET resistance. Thereby, the overall result is an optimized internal on-state resistance as anticipated.

4.10.3 Silicon Carbide versus Silicon MOSFET Comparison

SiC and Si Devices R_{ON}	R_{ON} @ 25 degC in ($\Omega.cm^2$)	R_{ON} @ 150 degC ($\Omega.cm^2$)	Current I_D
Si MOSFET 650 V	58	138	21 A
Si MOSFET 1200 V	750	2150	14.5 A
SiC MOSFET 1200 V	80	148	20 A

Table 5: SiC versus Si MOSFET Internal resistanceRONcomparison [62].

The values for the power MOSFETs in table 5 are gained from company CREE datasheet.

The comparison shown in table 5 proves that Silicon Carbide MOSFET outperform both 650 V and 1200V silicon MOSFETs. Higher breakdown voltage margin 10% versus 35% and 14 times lower conduction losses at 150deg Centigrade, further R_{ON} is more stable over temperature. The value of Silicon Carbide power devices must be assesed in terms of benefits at a system level and not at a single component level. This shows that it is more advantageous to use SiC MOSFETs than silicon MOSFET or even IGBTs. Higher switching speed for SiC MOSFETs mean we must follow good design practices when using SiC in any application. Silicon carbide devices are now widely implemented

in the renewable energy; i.e. in solar power inverters, electric vehicles EV chargers and other DC to DC applications.

4.11 Design and simulation of 600V Si and SiC trench MOSFET

The silicon trench MOSFET structure have; N-drift layer thickness ($3X10^-3cm$) and doping ($1.31X10^15cm^-3$); trench depth of ($1\mu m$); gate oxide thickness of 50 nm; Channel mobility 25 (cm^2/Vs); Channel length of ($1\mu m$). Simulation result shows that the total on-state resistance is R_{ON} = 0.0027 Ω. (V_{GS} = 4 V and V_{DS} = 600V). (MATLAB modelling figure 24).

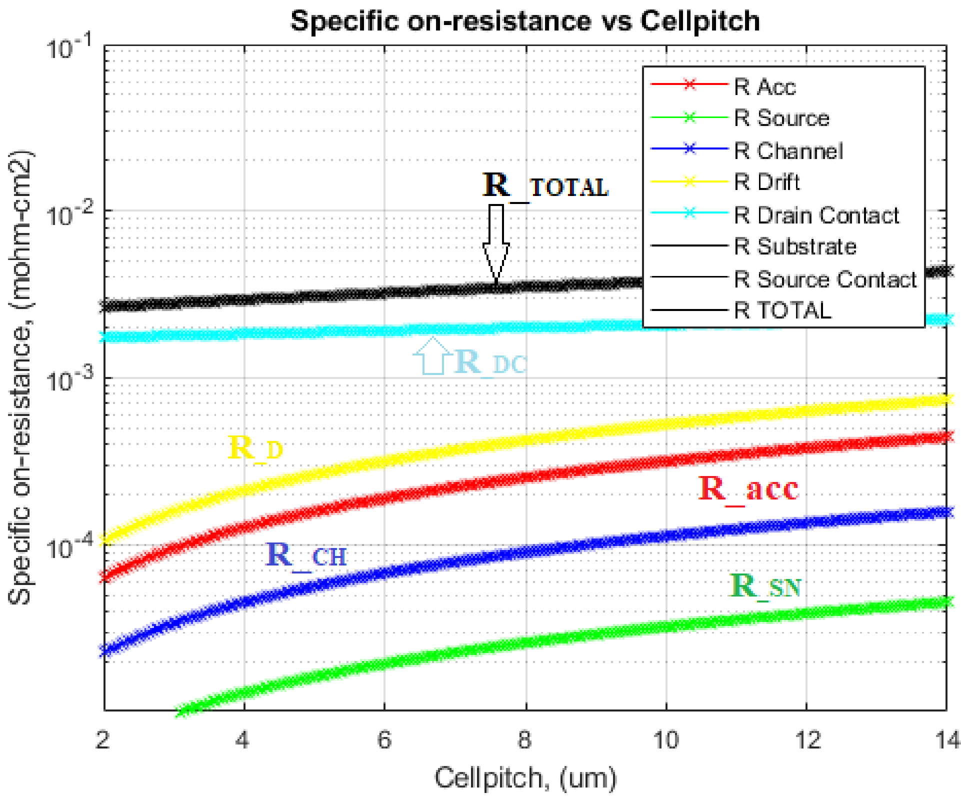


Figure 24: Silicon trench MOSFET 600 V, 20 A, output family of curves [60].

The Silicon Carbide trench MOSFET structure have; N-drift layer thickness ($321.4X\mu cm$) and doping ($1.143X10^17cm^-3$); trench depth of ($1\mu m$); gate oxide thickness of 50 nm; Channel mobility 11 (cm^2/Vs); Channel length of ($0.2\mu m$). Simulation result shows that the total on-state resistance is R_{ON} = ($9.660X^-4$). (V_{GS} = 4 V and V_{DS} = 600V). (MATLAB modelling figure 25).

Both silicon trench MOSFET and trench silicon carbide MOSFET structures have same device architectures. Simulation reveals that the specific on-state resistance when

using SiC as a material is lowered by three fold (X3) compared to silicon. This is due to inherent silicon material properties limitations; i.e. low band-gap energy, low thermal conductivity and limited switching frequency. Wide band gap semiconductors such as SiC provide larger band gaps, higher breakdown electric field and higher thermal conductivity. Therefore, silicon carbide trench MOSFET is a very viable device.

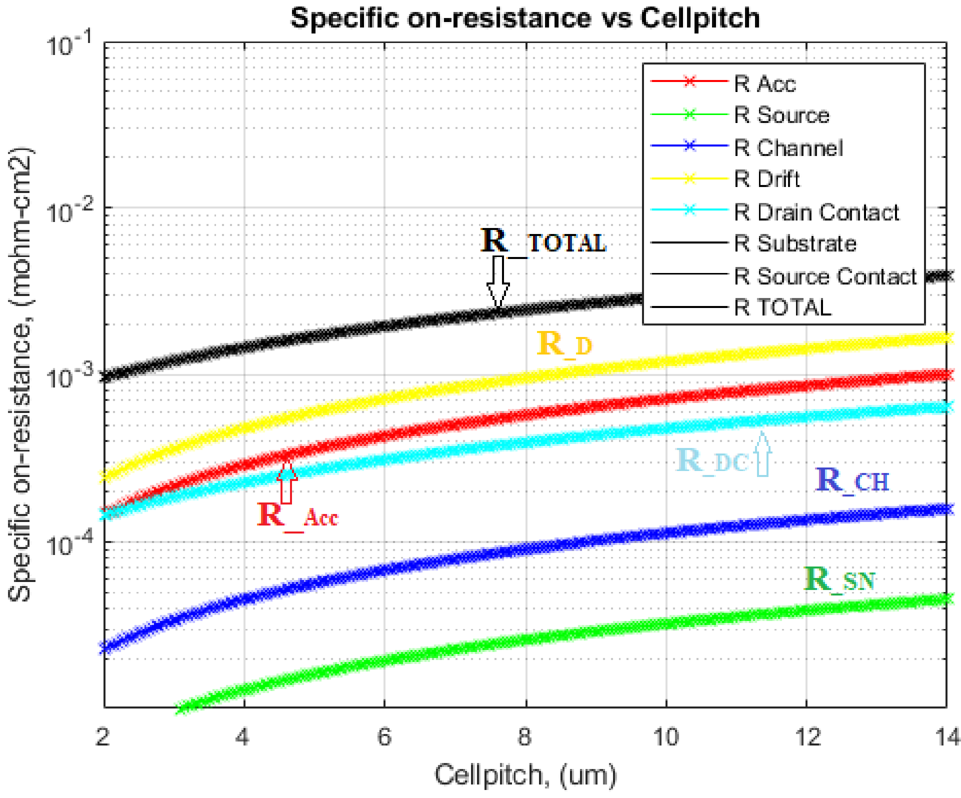


Figure 25: Silicon Carbide trench MOSFET 600 V, 20 A, output family of curves [60].

Internal resistance R_{ON} Ω	Silicon 600 V, 20 A	Silicon Carbide 600 V, 20A
Source to N-well R_{sn}	2.25 X $10^{-}5$	2.25 X $10^{-}5$
Channel R_{CH}	1.0536 X $10^{-}4$	5.2678 X $10^{-}4$
Drift R_D	0.0018	1.4402 X $10^{-}4$
Substrate R_{sub}	7.0 X $10^{-}4$	4.0 X $10^{-}4$
Accumulation R_{ch}	6.3214 X $10^{-}5$	3.1607 X $10^{-}4$
Total R_{ON}	0.0027	9.6608 X $10^{-}4$

Table 6: Si and SiC Trench MOSFET 600V, 20A R_{ON} Absolute Contributions [60].

4.12 Comparison between C-MOS, DT-MOS and SF-MOS

Silvaco simulation were performed to compare three different trench gate structures. The simulation enabled to observe electric field contours as well peak positions and values for (V_{GS} = -5V and V_{DS} = 600V).
The three structures under consideration are conventional trench MOSFET (C-MOSFET), Rohm's double trench MOSFET (DT-MOSFET) and shielded Fin MOSFET (SF-MOSFET). The dimensions of all three MOSFET structures are the same; i.e. N-drift layer thickness ($7\mu m$) and doping concetration of ($7.5 \times 10^{15} cm^{-3}$); trench depth of ($1\mu m$); gate oxide thickness of ($50nm$); the mobility of channel ($11cm^2/V.s$) and the length of channel ($0.4\mu m$). For the shielded Fin- MOSFET structure the doping concentration of JFET region is ($2 \times 10^{16} cm^{-3}$). Therefore, depending on simulation results shielded Fin MOSFET is good structure to reduce electric field at the trench corner.

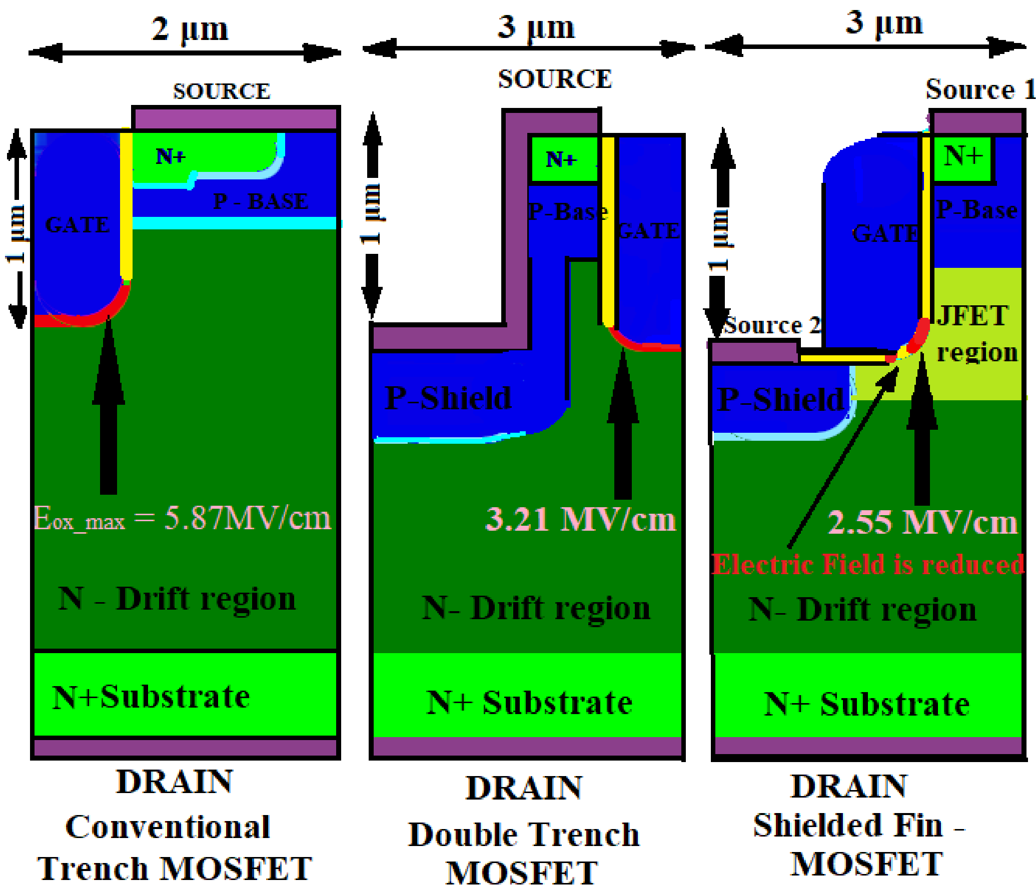


Figure 26: Comparison between C-MOS, DT-MOS and SF-MOS [19][43].

4.13 Power MOSFET threshold voltage

The threshold voltage for actual power MOSFET structure can change because of three reasons:

1. Unequal work function for the gate electrode and the semiconductor.

2. The presence of charge in the oxide.

3. Interface traps.

The doping concentration in the semiconductor substrate is used as a parametric variable to allow application of results to a wide variety of devices. Based up on this equation, the threshold voltage increases linearly with increasing oxide thickness and approximately as the square root of the doping concentration in the semiconductor. This knowledge can be used to improve the design of power MOSFET and IGBT structures.

4.14 Threshold voltage vs Oxide thickness (MATLAB modelling).

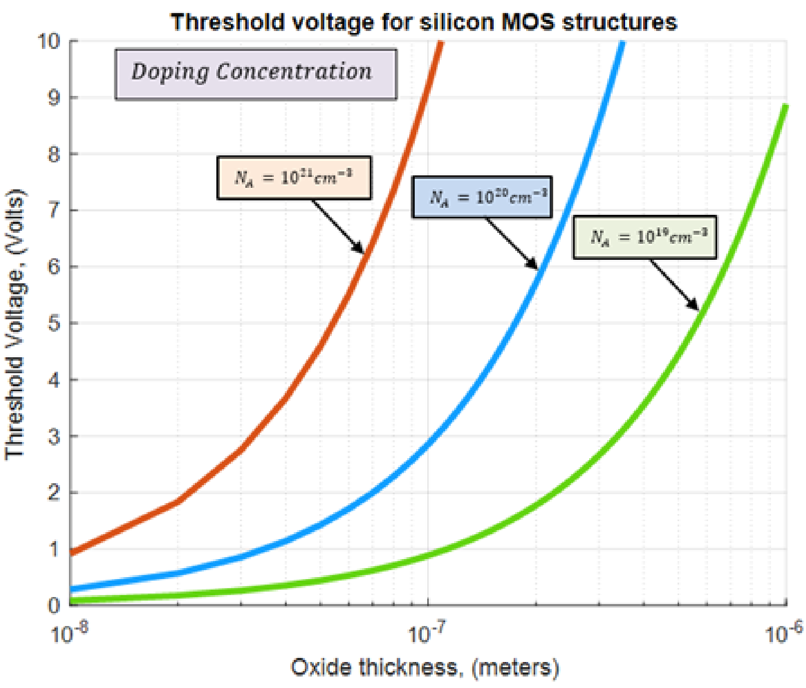


Figure 27: Threshold voltage vs Oxide thickness curves [54][60].

Figure 27 above shows the threshold voltage vs oxide thickness waveforms. And the corresponding amount of doping concentration are labelled on the graph. For figure 27 curve the MATLAB code (three) is posted on the appendix.

4.15 Wide Band Gap materials properties

The properties of the wide band gap semiconductors versus some traditional silicon and compound semiconductors are shown in table 6. WBG semiconductors provide larger bandgaps; this means higher breakdown electric field and higher thermal conductivity. Wide band gap semiconductors comparison between Silicon and Silicon Carbide:

Material	E_g(eV)	$n_i(cm^-3)$	ϵ_r	μ_n $(cm^2/V.s)$	E_c(Mv/cm)	$V_{sat}(cm/s)$	$\lambda(W/cm.K)$
Si	1.12	1.5 x 10^10	11.8	1350	0.2	1x10^7	1.5
GaAs	1.42	1.8 x 10^6	13.1	8500	0.4	1.2x10^7	0.55
2H-GaN	3.39	1.9 x 10^-10	9.9	1000/2000	3.5/3.75	2.5x10^7	1.3
4H-SiC	3.26	8.2 X 10^-9	10	1000/1200	2.8	2x10^7	4.5
3C-SiC	2.36	1.5 X 10^-1	9.7	800	1.4	2.5x10^7	3.2
Diamond	5.45	1.6 x 10^-27	5.5	3800	10	2.7x10^7	22
Ga_2O_3	4.85	-	10	300	8	1.8-2x10^7	0.1-0.3

Table 7: Silicon carbide vs Silicon Material Properties.[16][22][35].

4.15.1 State of the art on Silicon Carbide power devices

Silicon Carbide semiconductor device technology has been known for its huge capability for power electronic switching and controlling applications. Silicon Carbide based power semiconductor solutions are the next step towards an energy smart world. In comparison to long serving silicon technology SiC power switches present many attractive characteristics for high voltage power electronic semiconductor switches. SiC presents higher critical electric field, smaller in size and higher doping concentration, greater voltage blocking capability and reduced power losses during on-state operation. SiC has a wide bandgap, inducing very low intrinsic carrier concentrations even at high temperature, and consequently allows very low leakage currents and off-state power losses. Following are some of the specifics surrounding the process technology of SiC technology, the much higher breakdown field strength and thermal conductivity allow creating devices which outperform by far the corresponding Si ones. This means that unprecedented efficiency levels can be reached both at design levels and manufacturing.

4.16 Power MOSFET operating as a switching device

A typical chopper cell configuration for testing the dynamic characteristics of power devices is shown in figure 28. Here we observe n-channel power MOSFET operating as a switching device with an inductive load.

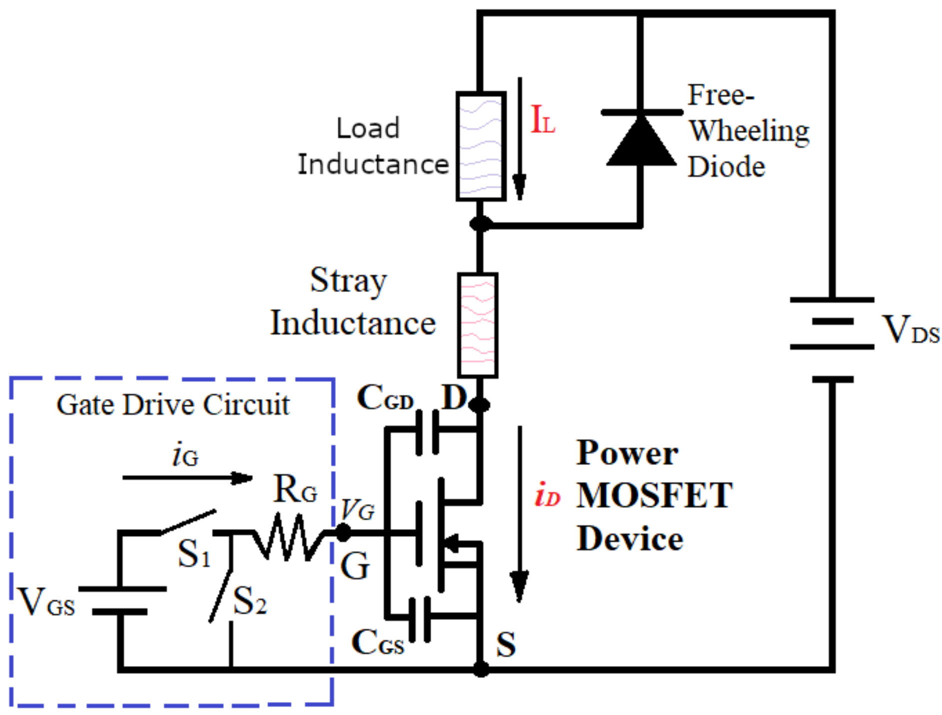


Figure 28: n-channel power MOSFET operating in an inductive load circuit [1][4].

4.17 Turn-on characteristics for the power MOSFET structure

Prior to the turn-on transient, the n-channel power MOSFET device is operating in its off state this is because switch S_2 is closed and switch S_1 is open (see figure 28). The load current is therefore flowing through the free-wheeling diode. The n-channel power MOSFET structures switching characteristics is governed by the gate drive circuit and the nature of the load. The n-channel power MOSFET device frequently is used to control the current in inductive loads, such as the windings of motors, using pulse width-modulation (PWM) control. The figure 28 showing, a free-wheeling diode in the circuit carries the load current during a portion of the operating cycle. The n-channel power MOSFET is switched on and off by a control or gate drive circuit, which can be represented (Thevenin's equivalent) as a DC voltage (V_{GS}) with a series resistance (R_G). During each cycle, the

load current I_L transfers between the n-channel power MOSFET device and the free-wheeling diode. The inductor is charged (i.e., its current increases) when the n-channel power MOSFET device is turned on, it is discharged when the load current flows via the diode. However, the change in the inductor current is small during one 'PWM' cycle allowing the assumption that the current I_L is constant. The stray inductance is included to account for package and board parasitic elements. It can be seen in the figure 28 above circuit, the load current flows through the free-wheeling diode whenever the n-channel power MOSFET device is in the off-state.

4.18 Turn-on waveforms for the power MOSFET structure

Turn-on transient of the n-channel power MOSFET. At the beginning all the current I_L is flowing through the freewheeling diode.
The following is a detailed elaboration on figure 29 turn-on curve.
At time (0 - t_1): The gate voltage VG increases thereby charging the capacitors, i.e. (C_{GS} + C_{GD}), since the gate voltage is less than threshold voltage, i.e. ($V_G < V_T$), no current in the MOSFET can flow.
At time (t_1 - t_2): ($V_G > V_T$), drain current I_D begins to flow. Load current I_L is constant, this means diode current transfers to power MOSFET. The gate voltage rises continuously. Since the diode is on, n-channel MOSFET has to support the entire supply voltage VDS.

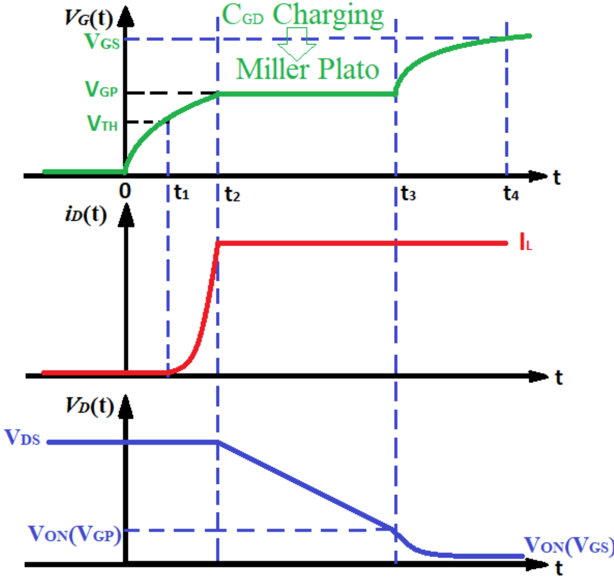


Figure 29: The turn-on waveforms for a power MOSFET [1][4].

At time (t_2 - t_3): Drain current I_D reaches load current I_L and all the freewheeling

diode current is transferred to n-channel MOSFET. The freewheeling diode is reverse biased this allows the drain to source voltage V_{DS} to fall. Since $I_L = I_D$ is constant, the gate to source V_{GS} also remains constant see figure 29.
At time (t_3 - t_4): The n-channel MOSFET enters its linear region, V_{GS} rises and V_{DS} decreases further.

4.19 Turn-off characteristics for the power MOSFET structure.

The operation of the power MOSFET in the off state is ensured by the switch S_2 in the control circuit being in the closed position, while switch S_1 is in an open position. These switches are usually comprised of lateral MOSFET structures within the control (integrated) circuit. The power MOSFET device can be switched on by opening switch S_2 and closing switch S_1 in the control circuit. The current then transfers from the diode to the power MOSFET device. During the turn-off transient, this operation is reversed to transfer the current from the power MOSFET device back to the diode. The inductor is charged (i.e., its current increases) when the power MOSFET switch is turned on, while it is discharged when the load current flows via the diode. Prior to the turn-on transient, the power MOSFET switch is operating in its off state because switch S_2 is closed and switch S_1 is open (see figure 28). Therefore, the load current is flowing through the free-wheeling diode.

4.19.1 Turn-off waveforms for the power MOSFET structure.

The turn-off transients of the n-channel power MOSFET shown in figure 28. During turn-off initial, there exist no circulating current in the freewheeling diode.
The following is a detailed elaboration on figure 28 turn-off curve.
At time (t_0 - t_4): The gate to source voltage decreases because of discharging of (C_{GS} + C_{GD}). There exists no change in drain current I_D and drain voltage V_D until V_{GS} is reduced to VGP required to saturate the drain current I_D to load current I_L.
At time (t_4 - t_5): Drain current I_D remains constant while V_D rises towards the supply voltage value, this is because the load current cannot be diverted to the free-wheeling diode until V_D exceeds power supply voltage V_{DS}. Drain voltage overshoot due to stray inductance. The gate to source voltage V_{GS} also remains constant and gate current discharges the gate to drain capacitance C_{GD}.
At time (t_5 - t_6): The free wheeling diode is turned-on and the drain current I_D is diverted flowing to the freewheeling diode. The gate to source voltage V_{GS} decreases continuously by discharging (C_{GS} + C_{GD}).

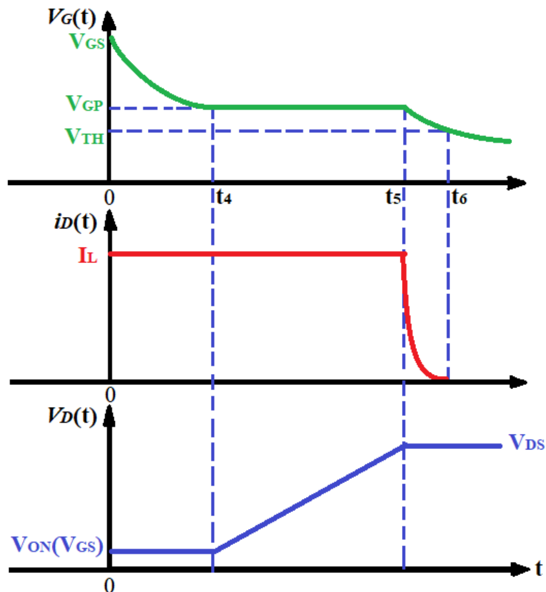


Figure 30: The turn-off waveforms for a power MOSFET [1][4].

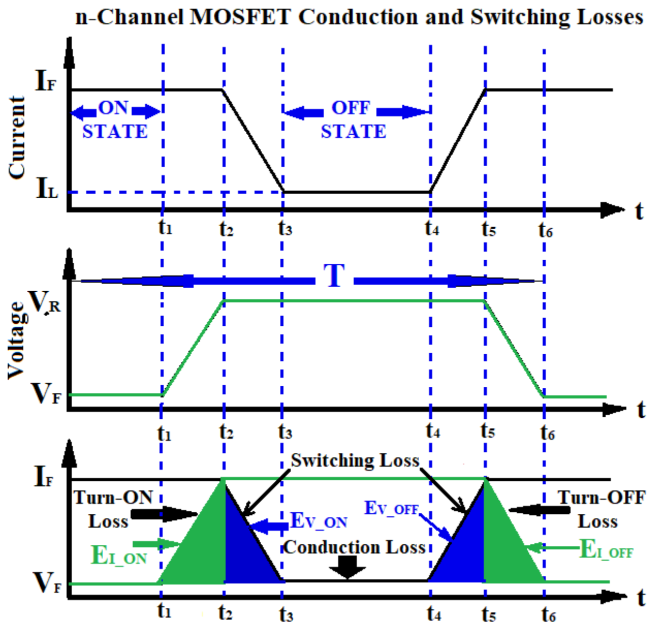


Figure 31: MOSFET Conduction and Switching Losses [1][4].

Conduction Loss:

$\mathrm{P}_L(\mathrm{ON}) = \delta \; I_F \; V_F$; Where: $\delta = \frac{t_1}{T}$

$P_L(\mathrm{OFF}) = (1 - \delta \; I_L \; V_R$

Switching Loss:
P_L(Turn OFF) = 0.5(t_3 - t_1) I_F V_R f; Where: f = $\frac{1}{T}$
P_L(Turn ON) = 0.5(t_6 - t_4) I_F V_R f
Total Power Loss = Conduction Loss + Switching Loss
P_L(Total) = P_L(ON) + P_L(OFF) + P_L(Turn OFF) + P_L(Turn ON) (35)

4.20 Wolfson power lab Experiment

Wolfson power lab experiment on selected semiconductor power switches; i.e. high power MOSFETs and IGBTs. The testing methodology followed by using high power curve tracer proves the reliability and ruggedness of the devices under test.

4.20.1 Devices Under Test 'DUT'

Type of Device	Device Voltage Rating	Device Current Rating
Silicon MOSFET	200 V	40 A
Silicon carbide MOSFET	1.2 KV	19 A
Silicon IGBT	600 V	20 A
Silicon IGBT	600 V	40 A
Silicon IGBT	1.2 KV	25 A

Table 8: Experimental Semiconductor Devices [62].

4.20.2 High Power Semiconductor Device Characterization

1. $I_{DS} - V_{GS}$: Transfer electrical characteristics.
2. $I_{DS} - V_{DS}$: Conduction electrical characteristics.
3. $I_{CE} - V_{GE}$: Transfer electrical characteristics.
4. $I_{CE} - V_{CE}$: Conduction electrical characteristics.
5. $\frac{dV}{dt}$ and $\frac{dI}{dt}$: Breakdown electrical characteristics.
6. Comparison between Wolfson lab testing results & Company Data sheet.

4.20.3 Wolfson Lab testing Experimental Set up

High Power MOSFET devices characterization:
Device Under Test 'DUT': 200V, 40A Si MOSFET and 1.2KV, 19A SiC MOSFET.

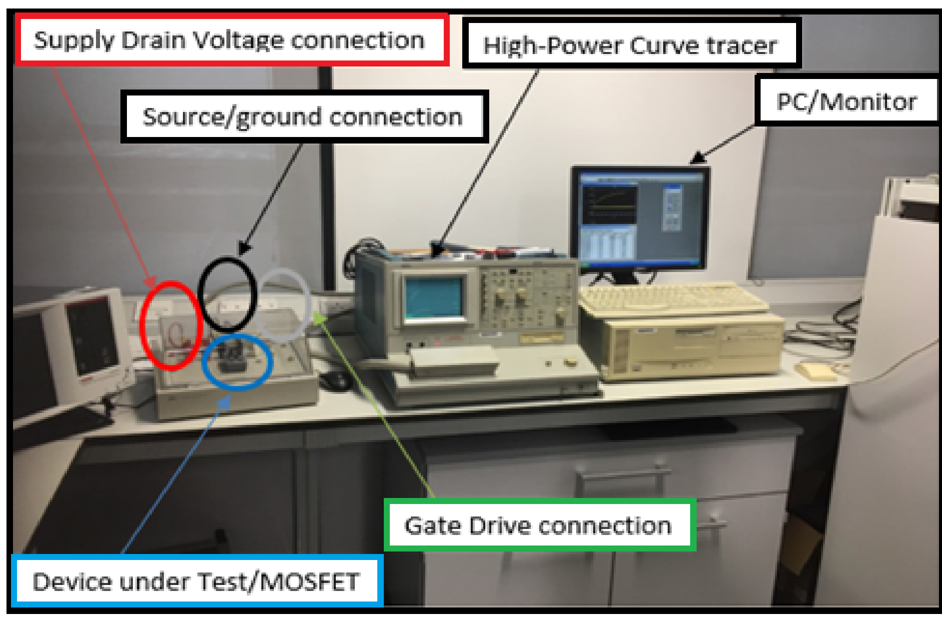


Figure 32: Wolfson Power lab experimental set up.

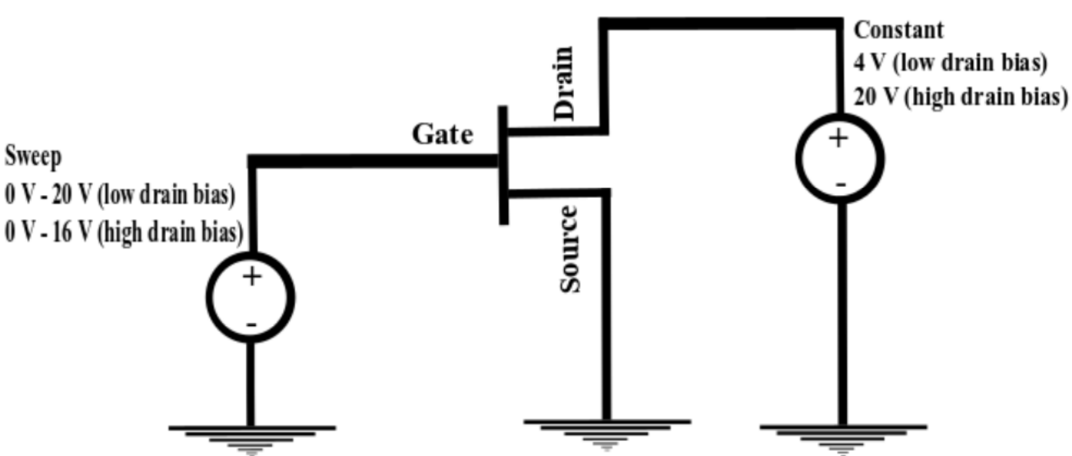
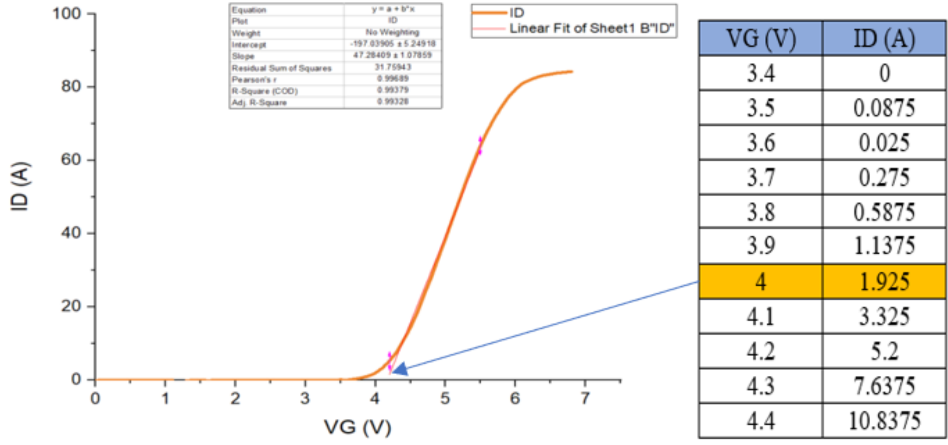


Figure 33: Schematic diagram for $I_D - V_G$ and $I_C - V_C$ transfer characteristics.

4.21 Transfer Electrical characteristics

DUT: Silicon Power MOSFET 200V, 40A.



Equation	y = a + b*x
Plot	ID
Weight	No Weighting
Intercept	-197.03905 ± 5.24918
Slope	47.28409 ± 1.07859
Residual Sum of Squares	31.75943
Pearson's r	0.99689
R-Square (COD)	0.99379
Adj. R-Square	0.99328

VG (V)	ID (A)
3.4	0
3.5	0.0875
3.6	0.025
3.7	0.275
3.8	0.5875
3.9	1.1375
4	1.925
4.1	3.325
4.2	5.2
4.3	7.6375
4.4	10.8375

Figure 34: Transfer electrical characteristics Silicon Power MOSFET 200V, 40A [60]

The figure 34 shows silicon power MOSFET 200V, 40A, begins to operate at a threshold voltage of V_T=4V and drain current of I_D=1.925A.

4.21.1 Lab Experiment Test Conditions for transfer characteristics

Test Conditions	Step generator V_G	Drain Current I_D
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_G	Current I_D - Voltage V_G
Force Conditions Mode	SWEEP	CONSTANT I_D
Start	0V	10V
Stop	7V	10V
Source type	-	High Power High Current

Table 9: Test conditions transfer electrical characteristics.

4.21.2 Trans-conductance of MOSFET

Transconductance for transfer conductance also referred as mutual conductance, is the electrical characteristic relating the drain current through the output of the MOSFET to the gate voltage across the input of the MOSFET. Conductance is the reciprocal of resistance.

$$g_m = \delta \frac{I_D}{V_g} \tag{36}$$

$$g_m = \frac{77.27 - 59.45}{5.9 - 5.4} \tag{37}$$

$$g_m = 35.634 Siemence. \tag{38}$$

4.22 Conduction or Output Electrical characteristics

$I_D - V_D$ output electrical characteristics.
DUT: Silicon Power MOSFET 200V, 40A.

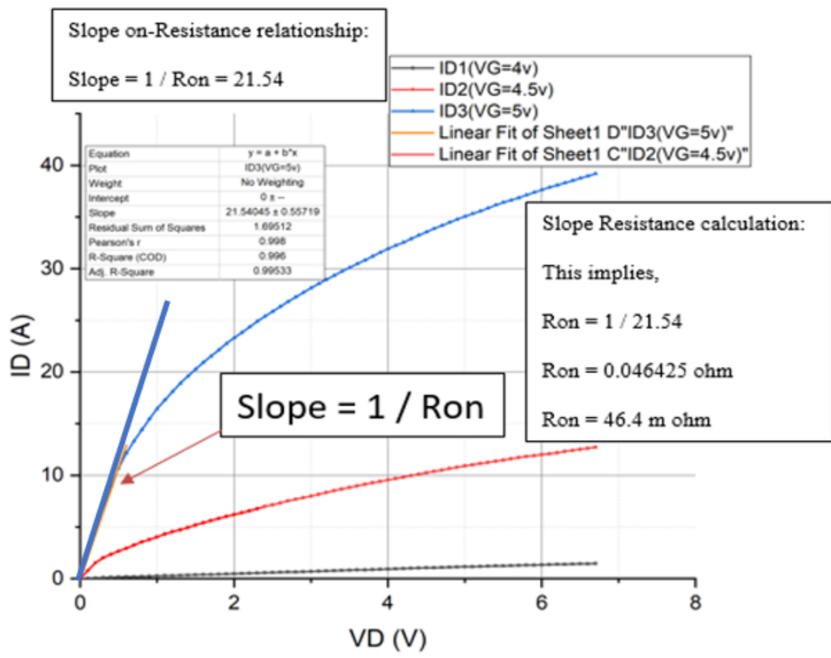


Figure 35: Output electrical characteristics family of curves [60].

The figure 35 shows output electrical characteristics, i.e. linear and saturation regions of the n-channel enhancement type MOSFET. Experimental data enabled to calculate the on-state resistance $R_{DS(ON)}$=46.425mΩ.

4.22.1 Lab test conditions for output characteristics

DUT: Power MOSFETs 200V, 40A and 1200V, 19A

Test Conditions	Step generator V_G	Drain Voltage V_{DS}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_G	Current I_D - Voltage V_D
Force Conditions Mode	STEP	SWEEP V_D - STEP I_D
Start	4V	0V
Stop	5V	20V
Source type	-	High Power High Current

Table 10: Test conditions output electrical characteristics.

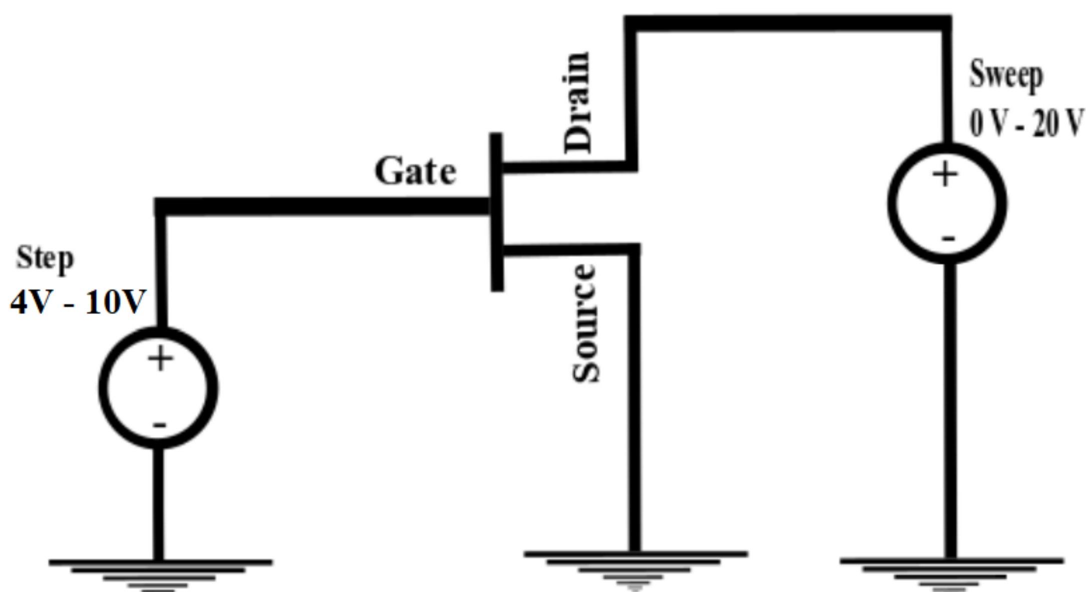


Figure 36: Schematic diagram for I_D–V_D and I_C–V_C transfer characteristics.

4.23 Breakdown Electrical characterization

Wolfson Power LAB Experimental set up for electrical breakdown high power semiconductor characterization. The purpose of the 10K resistor is to protect DUT from surge current see figure 36.

DUT: 200V, 40A Si MOSFET and 1.2KV, 19A SiC MOSFET.

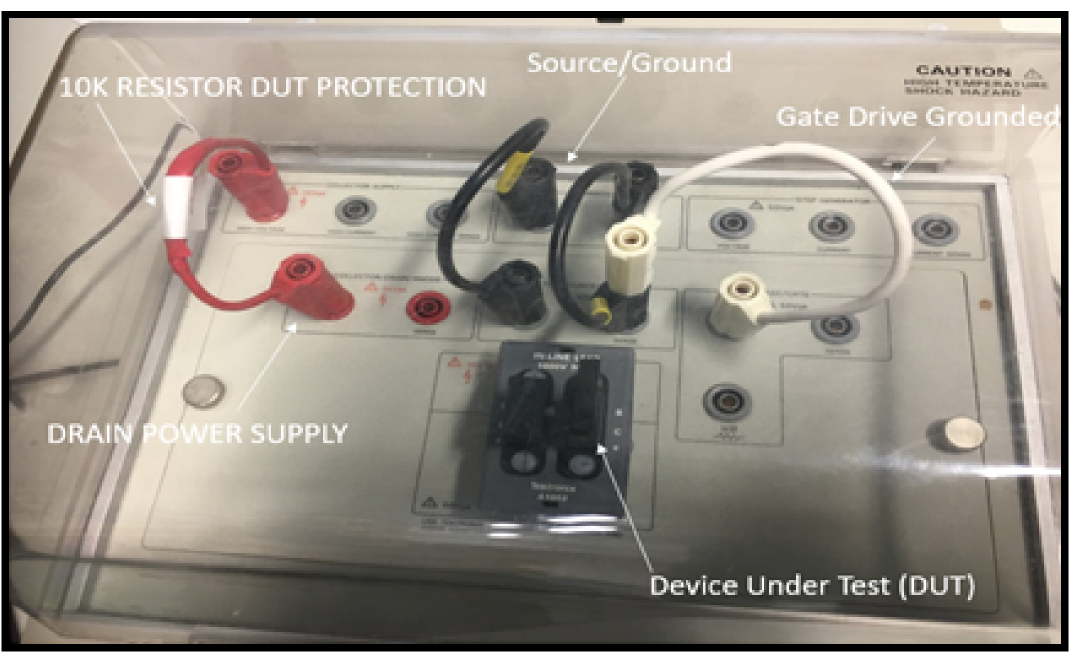


Figure 37: Experimental setup to measure electrical breakdown voltage characteristics.

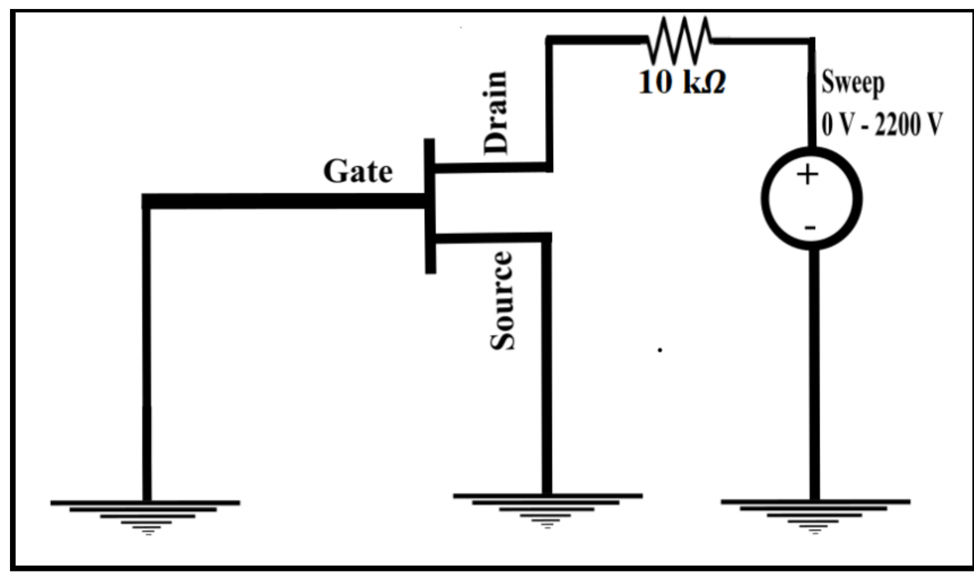


Figure 38: Schematic diagram to measure electrical breakdown voltage characteristics.

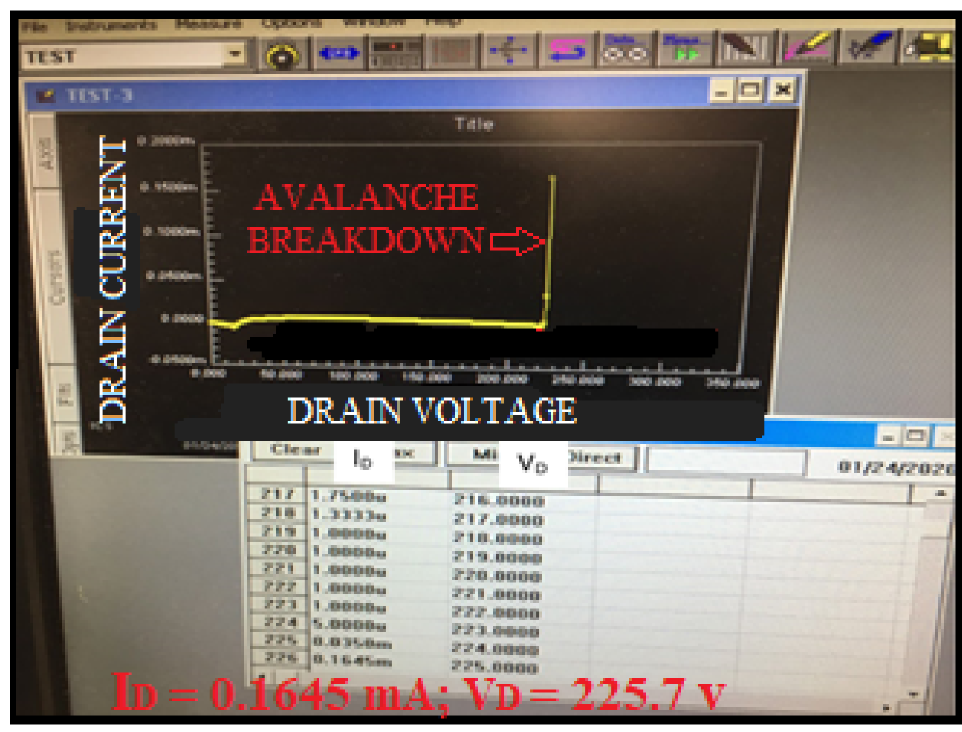


Figure 39: Electrical breakdown voltage V_{BR} power curve tracer snap-shot.

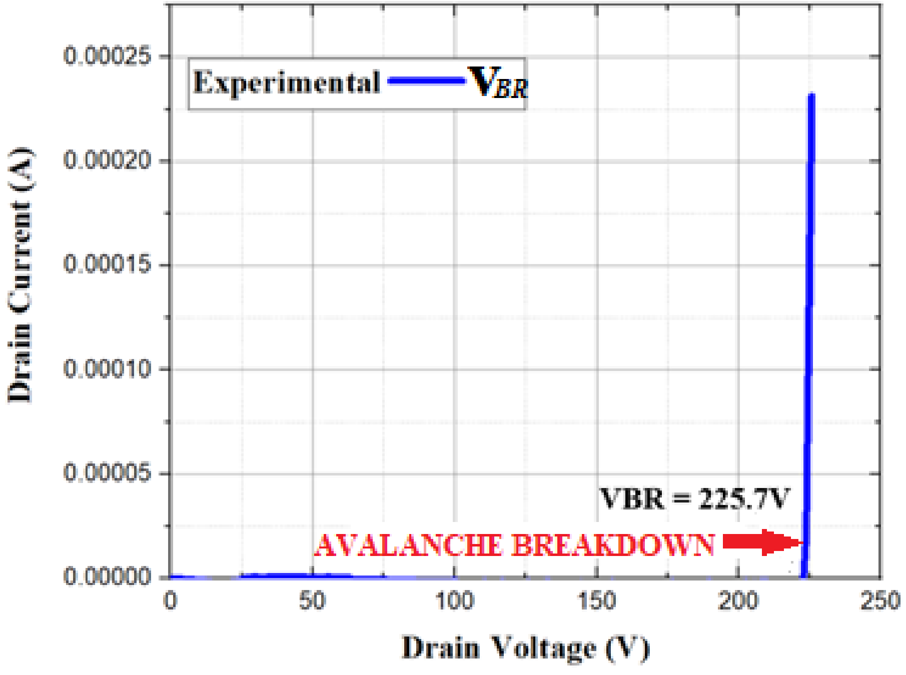


Figure 40: Experimental electrical breakdown voltage [60].

The figure 40 shows power MOSFET electrical breaking voltage V_{BR} = 225.7V. This value is 12.5 % greater than the data-sheet rated voltage value which is 200V, 40A.

4.23.1 Test conditions for electrical breakdown voltage characteristics

Test Conditions	Step generator V_G	Drain Voltage V_D
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_G	Current I_D - Voltage V_D
Force Conditions Mode	CONSTANT	SWEEP V_D - STEP I_D
Start	0V	0V
Stop	0V(Grounded)	250V
Source type	-	High Power High Voltage

Table 11: Test conditions electrical breakdown voltage characteristics.

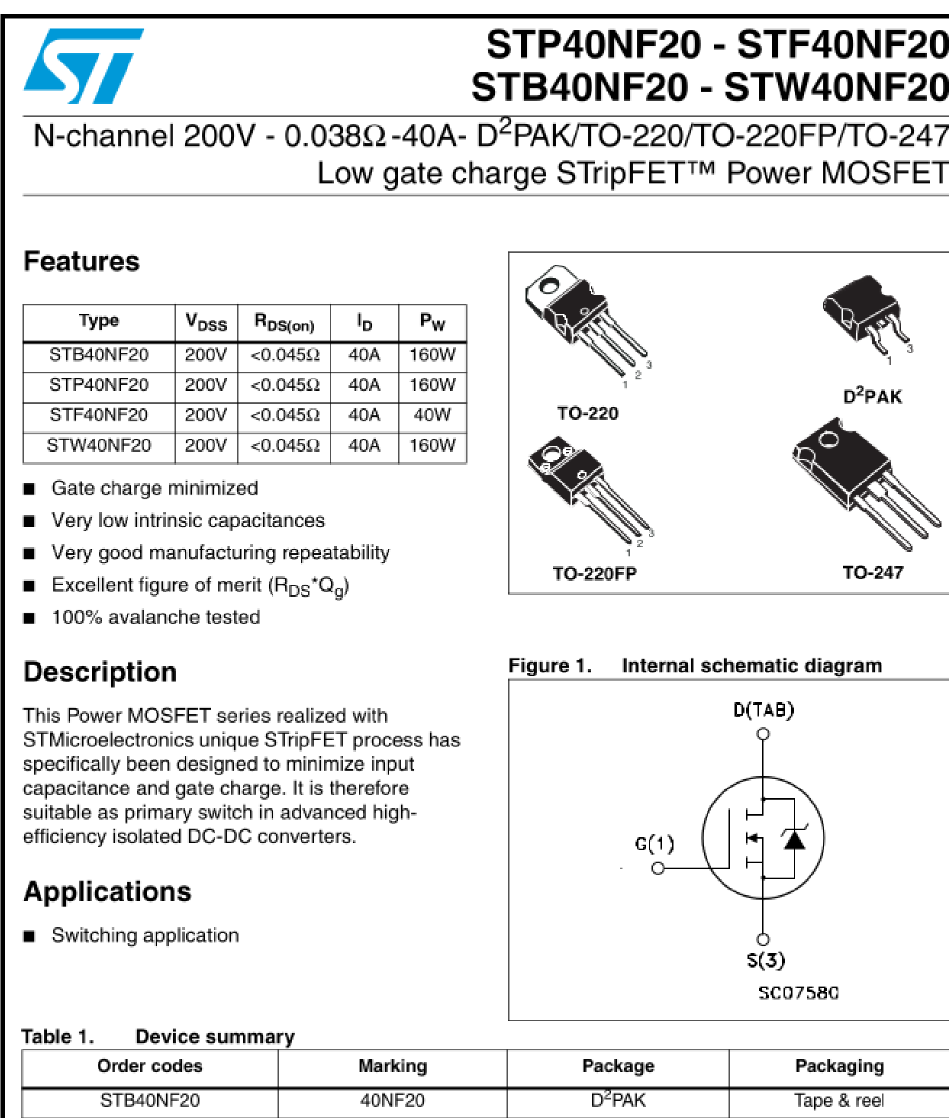
4.23.2 Avalanche breakdown

Avalanche breakdown is a consequence of impact ionization. Impact ionization happens due to electron or hole is more or less ballistically accelerated to high kinetic energy by a strong electric field, such as that in the depletion region of a reverse biased PN junction or Schottky diode.

Avalanche breakdown is caused by impact ionization of electron - hole pairs by carriers that have gained energy by accelerating in the high electric field in the depletion region of a reversed biased PN junction of the diode. The ionization causes a generation of extra more electrons and holes.

4.24 Manufacturer Datasheet

Company datasheet for n-channel Power MOSFET 200 V, 40A.
Experimental: $R_{DS}(\mathrm{ON}) = 0.046\ \Omega$
Datasheet: $R_{DS}(\mathrm{ON}) = 0.045\ \Omega$



STP40NF20 - STF40NF20
STB40NF20 - STW40NF20

N-channel 200V - 0.038Ω -40A- D^2PAK/TO-220/TO-220FP/TO-247
Low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STB40NF20	200V	<0.045Ω	40A	160W
STP40NF20	200V	<0.045Ω	40A	160W
STF40NF20	200V	<0.045Ω	40A	40W
STW40NF20	200V	<0.045Ω	40A	160W

- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Excellent figure of merit (R_{DS}*Q_g)
- 100% avalanche tested

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

Applications

- Switching application

Figure 1. Internal schematic diagram

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB40NF20	40NF20	D^2PAK	Tape & reel
STP40NF20	40NF20	TO-220	Tube
STF40NF20	40NF20	TO-220FP	Tube
STW40NF20	40NF20	TO-247	Tube

Figure 41: Company Datasheet Power MOSFET 200 V, 40A.

4.25 Output electrical characteristics of CoolSiC 1200V.

DUT: CoolSiC MOSFET 1.2KV, 19A.

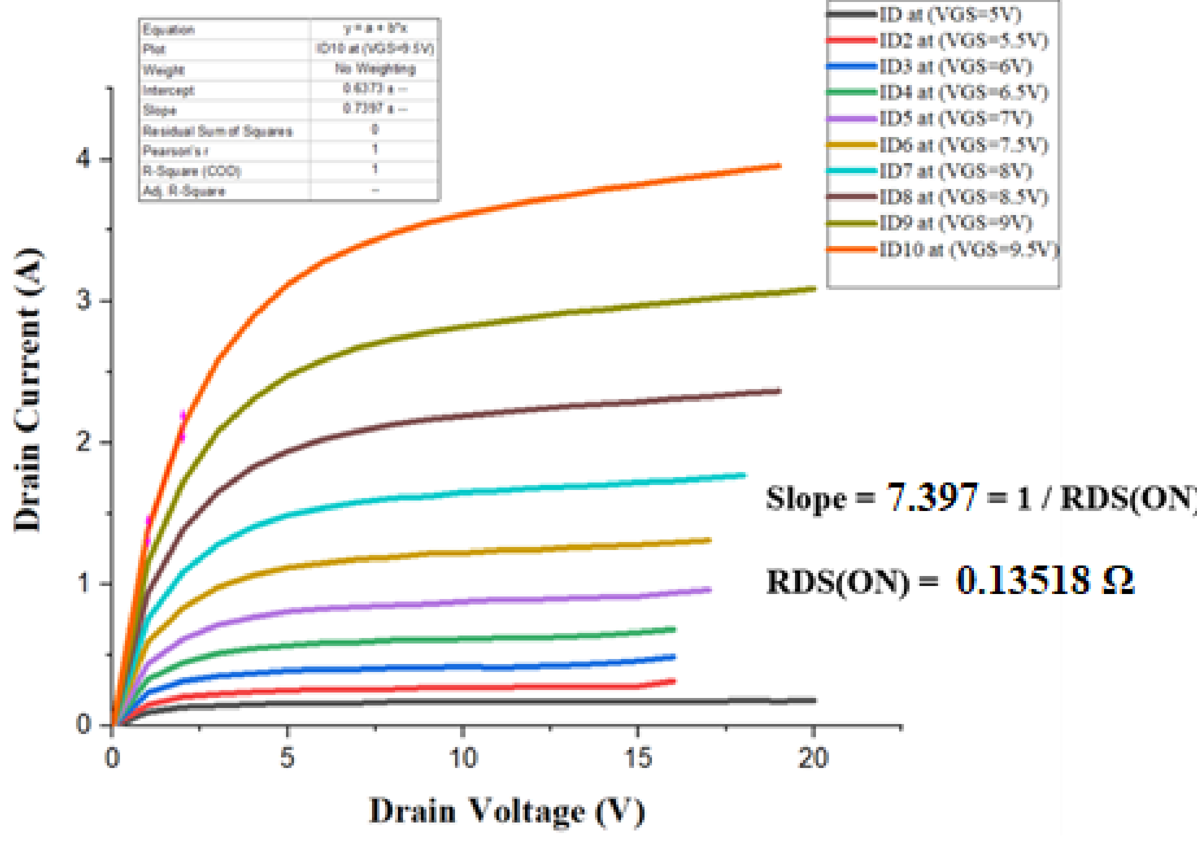


Figure 42: Experimental $I_D - V_D$ output electrical characteristics [60].

The figure 42 above shows conduction electrical characteristics of silicon carbide n-channel power MOSFET 1.2KV, 19A. For various values of gate bias voltage we get a specific electrical output characteristics (curve). For instance the output curve at gate-to-source bias voltage V_{GS} = 9.5V has output curve with a slope m = 7.397. Correspondingly, the calculated on-state resistance R_{DS}(ON) = 0.13518 Ω.

4.26 Manufacturer Datasheet

Company datasheet for CoolSiC Silicon Carbide trench MOSFET 1200 V, 19A.
Experimental result: R_{DS}(ON) = 135.18 mΩ
Datasheet result: R_{DS}(ON) = 140 mΩ

IMZ120R140M1H

infineon

IMZ120R140M1H

CoolSiC™ 1200V SiC Trench MOSFET
Silicon Carbide MOSFET

Features

- Very low switching losses
- Threshold-free on state characteristic
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5V
- 0V turn-off gate voltage for easy and simple gate drive
- Fully controllable dV/dt
- Robust body diode for hard commutation
- Temperature independent turn-off switching losses
- Sense pin for optimized switching performance

Benefits

- Efficiency improvement
- Enabling higher frequency
- Increased power density
- Cooling effort reduction
- Reduction of system complexity and cost

Potential applications

- Energy generation
  - Solar string inverter and solar optimizer
- Industrial power supplies
  - Industrial UPS
  - Industrial SMPS
- Infrastructure – Charge
  - Charger

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC 47/20/22

Note: *the source and sense pins are not exchangeable, their exchange might lead to malfunction*

Table 1 Key Performance and Package Parameters

Type	V_{DS}	I_D T_C = 25°C, $R_{th(j-c,max)}$	$R_{DS(on)}$ T_{vj} = 25°C, I_D = 6A, V_{GS} = 18V	$T_{j,max}$	Marking	Package
IMZ120R140M1H	1200V	19A	140mΩ	175°C	12M1H140	PG-TO247-4

Figure 43: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET.

4.27 Breakdown voltage electrical characteristics

DUT: CoolSiC 1200V, 19A, MOSFET.

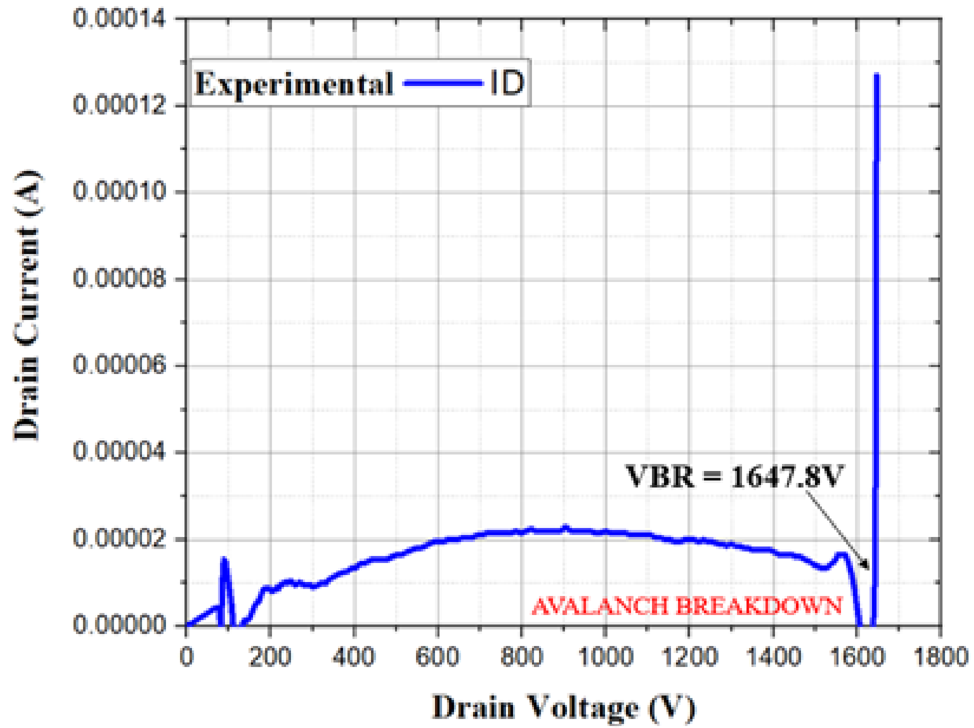


Figure 44: Experimental breakdown voltage V_{BR}=1647.8V [60].

Figure 44 showing 1.2KV, 19A SiC MOSFET electrical breakdown voltage.The power MOSFET is breaking at V_{BR} = 1647.8V. Drain voltage avalanches just before its Breakdown: Starting V_{BR} = 1630V upto final value V_{BR} = 1647.8 V.

The observation made regarding electrical breakdown voltage experiment; the n-channel 1.2KV, 19A CoolSiC MOSFET. The device was exposed to high voltage electrical stress levels which caused electron avalanche in the pn-junction that end up in device breaking. This avalanche breakdown or avalanche effect is a phenomenon that can happen in the real industrial world where semiconductor switches are controlling. During experiment drain current multiplies to produce a very big current that can potentially destroy the device.

5 Insulated Gate Bipolar Transistor - IGBT

5.1 Emphasis on the improved IGBT working principle

IGBT is acronym for Insulated Gate Bipolar Transistor. It is a three-terminal semiconductor switching device which combines the current-carrying capability of a bipolar transistor with the ease of control of that of a MOSFET. IGBTs are widely used for fast switching with high efficiency in many types of electronic devices and for high power ($> 300V$) switching applications. This unique device was developed in the 1980s by combining the physics of operation of bipolar transistors and metal oxide semiconductor field effect transistor MOSFETs. The research focus was set on modern innovations of semiconductor switches such as trench gate power MOSFET and trench gate IGBT device structures. An in-depth investigation was conducted by studying the advantages of using trench gate structure, ruggedness, and reliability. Furthermore, an innovative cell design was made towards achieving an improved forward-bias safe operating area 'SOA' and reverse biased safe operating area 'RBSOA'. The IGBT forward-bias safe operating area 'SOA' defines the collector current and collector voltage conditions for the period while the device is turned-on. The IGBT reverse-bias safe operating area 'RBSOA' defines the collector current and collector voltage conditions during the turn-off period. In addition, DC measurement results achieved from Wolfson power lab testing helped in the understanding of the IGBT device operation and results showing near exact match when compared to manufacturers data sheet.

5.2 The advantages of IGBTs as a switching device

IGBTs are the consequence of a technological advancements in power semiconductor devices. IGBTs are state-of-the-art high-power electronic switch with great advantages in a wide a range of applications, from medium to ultra-high-power applications such as switched mode power supplies (SMPS). In addition, they have extensive use in high power supply switching, for instance variable-frequency drives (VFDs), electric cars, trains, variable speed refrigerators, lamp ballasts, and air-conditioners. IGBTs are becoming increasingly important by creating a more sustainable energy-rich future and a global society with a high standard of living while reducing our impact on the environment and mitigating global warming. Renewable energy plays a vital role in conserving the nation's natural resources. The harnessed energy is controlled by IGBT-based inverters and solar PV generated DC power converting into well-regulated 50 or 60Hz AC power.

5.3 IGBT single cell cross sectional structure

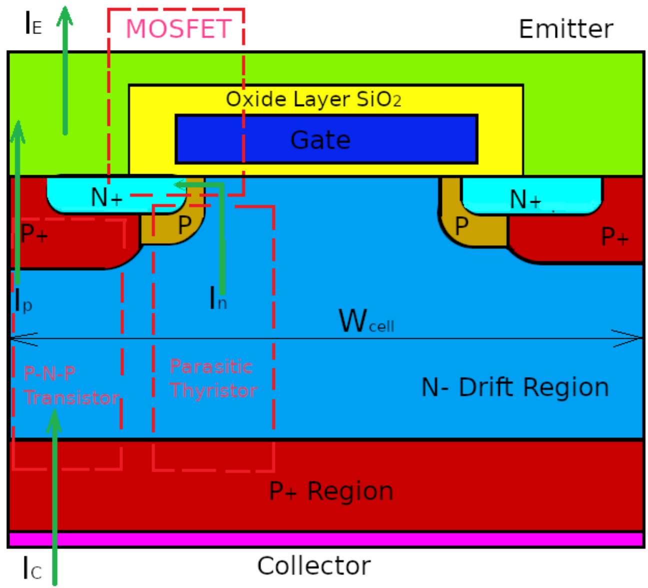


Figure 45: Single cell cross-section of IGBT [1][4].

5.3.1 IGBT equivalent circuit

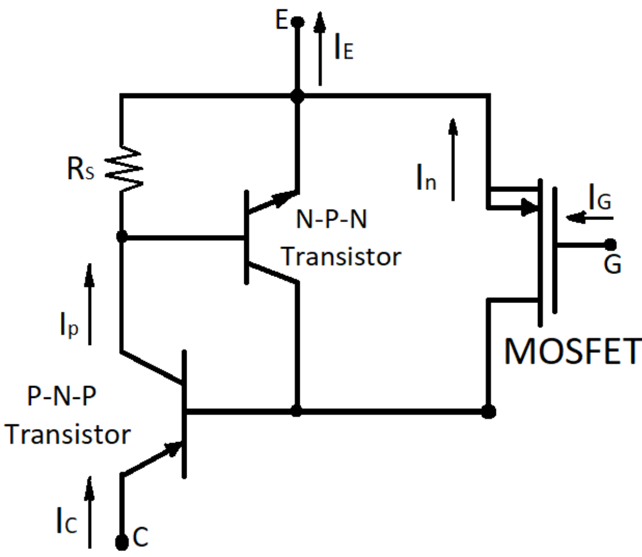


Figure 46: Equivalent circuit of IGBT [1] [4].

5.4 IGBT working principles

The MOSFET section is used to provide the base drive current for the bipolar transistor with the bipolar transistor used to modulate the conductivity of the drift region for the IGBT structure, see figure 45. The structure of the IGBT is very similar to that for the power MOSFET structure; the only difference is the N+ substrate of a MOSFET is substituted with a P+ substrate. However, this substitution creates a four-layer parasitic thyristor (SCR), see figure 43, which was initially considered as an obstacle to enhanced device performance because its latch-up results in destructive failure due to loss of gate control.

Fortunately, the parasitic thyristor can be suppressed by the addition of the P+ region within the cell while retaining the benefits of the P+ substrate for the injection of minority carriers into the N-drift region, resulting in greatly reducing its resistance. This has enabled the development of high voltage IGBT products with high current carrying capability. The on-state voltage drop for the IGBT increases with increasing voltage blocking capability due to the necessity to widen the N-drift region. Punch-through 'PT' IGBT – N+ buffer layer present. Non-punch-through 'NPT' IGBT - N+ buffer layer absent.

5.5 Silicon Trench-Gate IGBT single cell cross-section

Trench-Gate Non-punch-thru IGBT single cell cross-section.

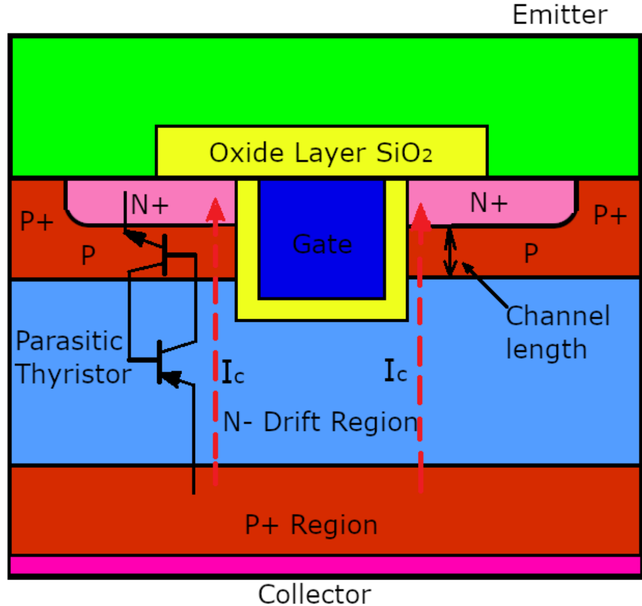


Figure 47: Non-punch-thru trench-gate IGBT single cell cross-section [1] [4].

5.5.1 Trench gate non-punch-through structure and fabrication

This section describes the fabrication process of trench IGBT 'NPT'.
Gate: A trench is etched in the silicon where the gate electrode is embedded. As a result of this the channel becomes vertical. The main advantage of the structure is that it eliminates the JFET effect. The structure name is adopted from the U-shape of the trench.
Gate Oxide: The trench is removed after the etching of silicon and then a thin gate oxide layer is grown on the inside walls of the trench. The gate oxide thickness determines the threshold voltage (V_T), trans-conductance and gate capacitance.
N+ well: Using ion implantation or diffusion process N+ well is formed on p-type substrate.
P well or P body: Introducing or implanting a p-type dopant into an n-substrate the p-wells are formed. The technology behind forming N-well and P-well, follows a technique where n-type diffusion is done over a p-type substrate or p-type diffusion is done over n-type substrate, respectively.
P+ region in P body: P+ highly doped region in P well is formed. This region makes good electrical contact to the well (ohmic, not diode).
Vertical channel: Power IGBTs use a vertical structure with emitter and collector terminals at opposite sides of the cell. The vertical channel adjustment eliminates crowding at the gate and offers bigger channel widths. Furthermore, thousands of transistor cells can be combined into one compact cell, this allows the device to handle the high currents and voltage required.
N- Drift region: During current flow, the N-drift region of the IGBT structure functions with high-level injection condition. This reduces the resistance of the N - base drift region allowing high-current flow with low on-state voltage drop. The reverse breakdown voltage of the IGBT is determined by the drift region width and doping concentration. Furthermore, the drift region absorbs the depletion layer of the reverse biased p+ n- junction. As it is lightly doped, it will add significant ohmic resistance to the diode when it is forward biased. For higher breakdown voltages, the drift region is wide.
P+ Substrate: The P+ substrate, which is also known as the injector layer, due to minority carriers or holes injected into N-drift region. The N-layer in between the P+ & P region serves to accommodate the depletion layer of PN-junction i.e., J_2.

5.6 Parasitic Thyristor

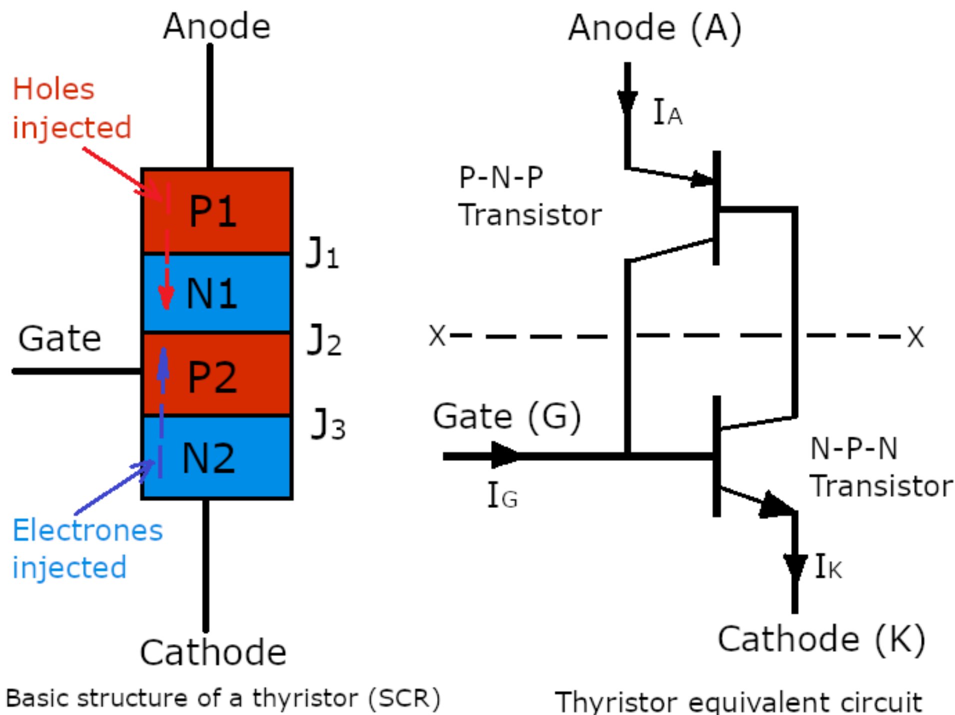


Figure 48: Basic structure of a parasitic thyristor with equivalent circuit [1] [4].

$$I_A = \alpha_{pnp} I_A + \alpha_{npn} I_K + I_L \tag{39}$$

$$I_K = I_A + I_G, so: \tag{40}$$

$$I_A = \frac{(\alpha_{npn} I_G + I_L)}{(1 - \alpha_{pnp} - \alpha_{npn})} \tag{41}$$

I_A : Anode current; I_K : Cathode current; I_L : Leakage current; I_G : Gate current. α_{pnp} : Current gain of p - n - p transistor; α_{npn} : Current gain of n - p - n transistor.
Junction J_1: The boundary between the P substrate and N-drift region.
Junction J_2: The boundary between the N-drift region and the P body.
Junction J_3: The boundary between the P body and N+ well.
Parasitic Thyristor: The parasitic thyristor is formed of four-layers (P-N-P-N). The structure with the outer layers with their electrodes referred to as the anode (p-type) and the cathode (n-type). The four-layer structure is formed by two back to back connected conventional transistors, i.e. P-N-P and N-P-N.
P-N-P transistor: Conventional bipolar transistor that have a P-N-P structure with the

electrodes named collector, base, and anode.
N-P-N transistor: Conventional bipolar transistor that have a N-P-N structure with the electrodes named collector, base, and emitter.

5.7 Thyristor defined

Thyristors also sometimes referred as Silicon-Controlled Rectifiers (SCR), they may appear to be unusual electronics components in many ways, but they are particularly useful for controlling power circuits. Thyristors may be considered a rather an unusual form of electronics component because it consists of four layers (p-n-p-n) of differently doped silicon rather than the three layers of the conventional bipolar transistors. Further, a conventional bipolar transistor may have a p-n-p or n-p-n structure with the electrodes named collector, base, and emitter, whereas the thyristor has a p-n-p-n structure with the outer layers with their electrodes referred to as the anode (p-type) and the cathode (n-type). The control terminal of the SCR is named the gate and it is connected to the p-type layer that adjoins the cathode layer. Thyristors can switch high voltages and withstand reverse voltages making them ideal for electronic switching applications, especially within AC scenarios.

5.7.1 Thyristor operation

During off state no current flows across the device. When supply is connected and a small amount of current injected into the gate, then the device is triggered and begins to conduct current. It will remain in the conducting state until the gate supply is removed. The thyristor equivalent circuit in figure 46 shows how it operates. The equivalent circuit shows two back-to-back connected transistors. The first transistor with its emitter connected to the cathode of the thyristor is an NPN transistor, whereas the second transistor with its emitter connected to the anode of the thyristor, SCR is a PNP transistor. The control gate terminal is connected to the base of the NPN transistor as shown in the equivalent circuit.

5.8 The Impact of Parasitic Thyristor on IGBT operation

Latch-up pertains to a failure mechanism wherein a parasitic thyristor (such as a parasitic silicon-controlled rectifier, or SCR) is inadvertently created within a circuit, causing a high amount of current to continuously flow through it once it is accidentally triggered or turned on. Depending on the circuits involved, the amount of current flow produced by this mechanism can be large enough to result in permanent destruction of the device

due to electrical overstress (EOS). Events that can trigger parasitic thyristors into latchup condition include excessive supply voltages, voltages at the input/output pins that exceed the supply rails by more than a diode drop, improper sequencing of multiple power supplies, and various spikes and transients. Once triggered into conduction, the amount of current flow that results would depend on current limiting factors along the current path. In case where the current is not sufficiently limited, EOS damage such as metal burn-out can occur.

5.9 Parasitic Thyristor mitigation mechanism

The best defense against latch-up is good product design. There are now many design for reliability guidelines for reducing the risk of latch-up, many of which can be as simple as putting diodes in the right places to prevent parasitic devices from turning on. Of course, preventing a device from being subjected to voltages that exceed the absolute maximum ratings is always also to be observed.

5.10 Punch through IGBT Cell Cross Section

With N+ buffer layer, junction J_1 has small breakdown voltage and thus IGBT has little reverse blocking capability – anti-symmetric IGBT. The N+ buffer layer speeds up device turn-off.

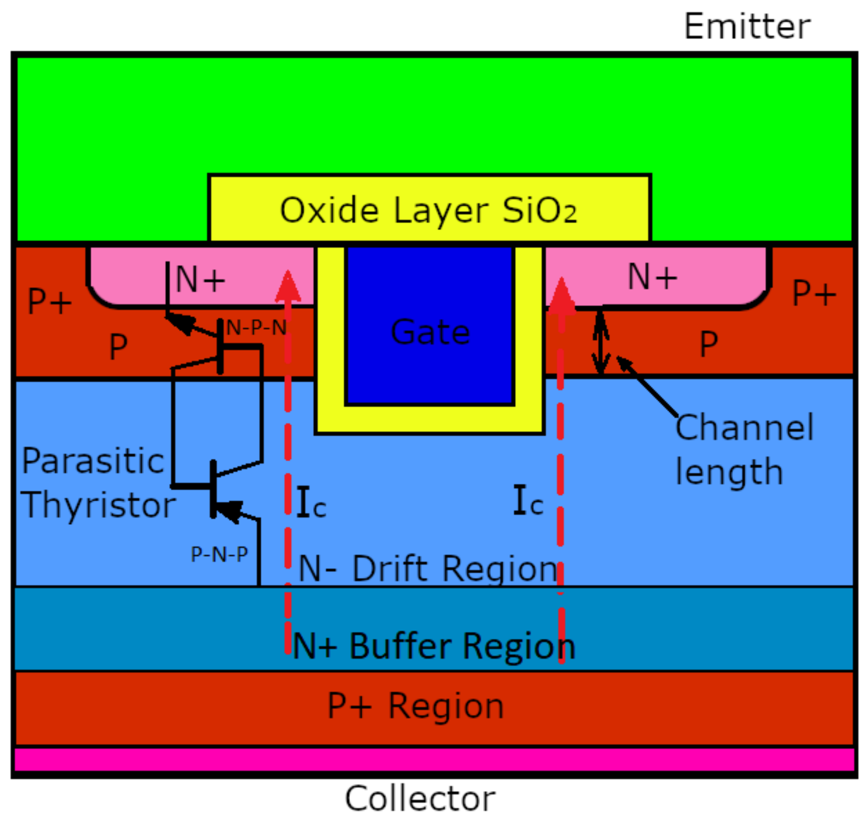


Figure 49: Punch through IGBT Cell Cross Section [1] [4].

5.11 IGBT Blocking Off - State Operation

During the blocking or off - state operation – The Gate to Emitter voltage is less than the Gate to Emitter threshold voltage, i.e. ($V_{GE} < V_{GE}(Threshold)$). Junction J_2 is in blocking mode and N- drift region accommodates depletion layer of blocking junction J_2.

5.12 IGBT On-state Operation

During the forward or on-state operation – The Gate to Emitter Voltage is greater than the Gate to Emitter threshold voltage, i.e. ($V_{GE} > V_{GE}(Threshold)$). The IGBT is designed in a way the MOSFET structure carries most of the collector current. The forward or on-state voltage drop is an aggregate of: the voltage drop at junction one

J_1 plus drift region voltage drop plus channel voltage drop. Mathematically expressed $V_{CE} = V_{J1} + V_{drift} + I_C R_{Channel}$. The amount of minority carriers or holes injected into drift region from substrate junction one J_1 minimizes the drift region voltage drop V_{drift}.

5.13 Static Latch-up of IGBTs

During an over flow of large current the channel region is bypassed and excess current flowing through the p - well into the emitter. Moreover, the big current flowing in the conduction paths causing lateral voltage drops and also turns-on the parasitic thyristor. Junction three J_3 will be forward biased when the lateral voltage drops very large. Parasitic N-P-N bipolar junction transistor will be turned on and this will trigger turning-on of parasitic thyristor. During latch-up a large power is dissipated this can permanently destroy IGBT unless interrupted immediately. The gate control is lost during latch-up, therefore an external circuit must terminate latch - up. The device can not be turned off during latch-up due to the loss of gate control.

5.14 Dynamic Latch-up Mechanism in IGBTs

The rapid turning off of the MOSFET part and depletion layer of junction J_2 expands rapidly into N- drift region, the base region of the P-N-P bipolar junction transistor. The expansion of depletion layer reduces base width of P-N-P bipolar junction transistor and its alpha α_{pnp} increases and current gain factor beta β also increases. More injected holes survive traversal of drift region and become "collected" at junction J_2. Increased P-N-P bipolar junction transistor collector current increases lateral voltage drop in p-base of N-P-N bipolar junction transistor and latch-up soon occurs. Manufacturers usually specify maximum allowable collector current on basis of dynamic latch-up.

5.15 IGBT Turn-on characteristics waveforms

Turn-on waveforms for IGBT are very similar to turn-on waveforms of MOSFETs. Contributions to forward voltage drop due to current tailing. Increase in gate-to-emitter capacitance 'Cge' of MOSFET part at low collector-emitter voltages. Slow turn-on of P-N-P bipolar junction transistor structure.

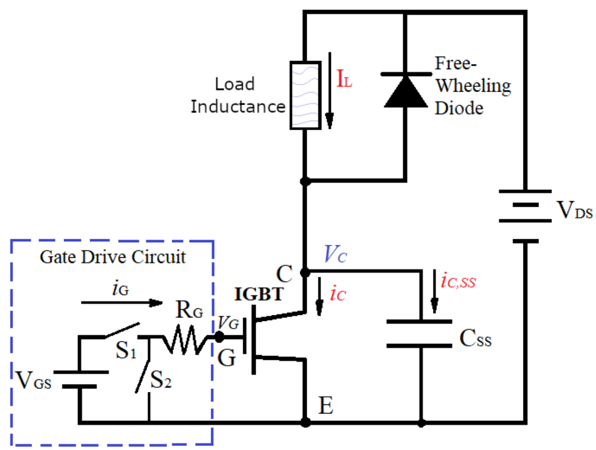


Figure 50: Soft-switching circuit for the IGBT [1]

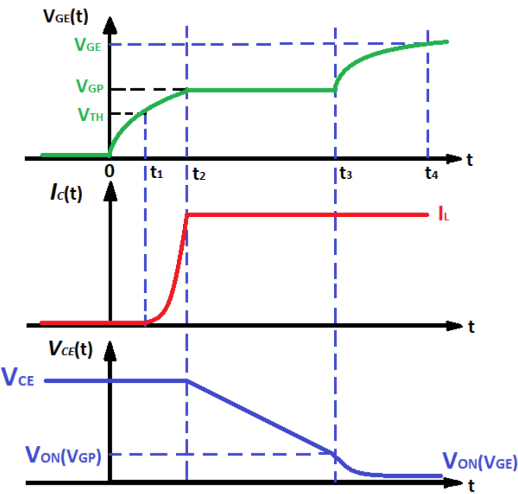


Figure 51: Soft-switching circuit for the IGBT [1] [4]

5.16 Turn off characteristics of an IGBT

The IGBT turn off characteristics is completely different from that of MOSFET turn off, because of the existence of stored charge that need to be removed before the device is turned off safely. This is similar to the PN junction diode, bipolar junction transistor and thyristor, some is extracted before the current falls and the rest gives rise to a current tail which decays through carrier recombination.

During turn off the collector current fall typically has two clearly identifiable stages: a rapid current fall followed by the slow current fall or 'current tail'. The current tailing is due to stored charge trapped in drift region or base of P-N-P bipolar junction transistor

caused by rapid turn-off of MOSFET part. Shorten tailing interval by either reducing carrier lifetime or by putting N+ buffer layer adjacent to injecting P+ layer at drain. The size of the current tail is proportional to the stored charge and also depends on the device design punch-through 'PT' or non-punch through 'NPT'. In the MOSFET part, the collector to emitter voltage V_{CE} must rise before the collector current I_C can fall, because of the freewheel diode. This is accommodated by widening the depletion layer and charging the gate-collector capacitance C_{GC}. A plateau is still seen in the IGBT gate turn-off waveforms during the rise of V_{CE}.

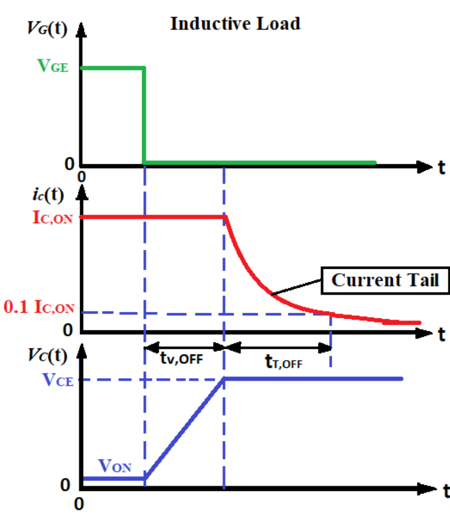


Figure 52: Soft-switching circuit for the IGBT [1]

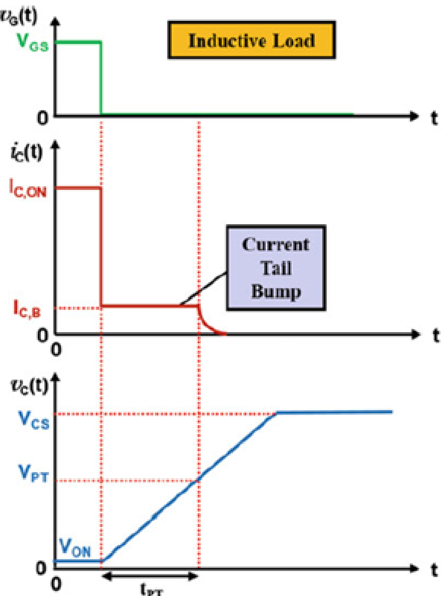


Figure 53: Soft-switching waveforms for the IGBT [1]

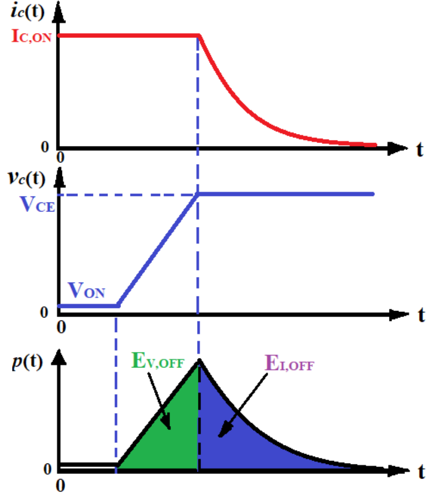


Figure 54: Soft-switching waveforms for the IGBT [1]

The figure 52 shows the IGBT collector current and voltage waveform turn off operation for the typical inductive (motor) control application. The IGBT device losses power because of the reverse recovery characteristics of the freewheeling diode in the soft switching circuit.

5.17 Forward biased Safe Operating Area (SOA)

During the collector current fall collector-emitter voltage V_{CE} is high, so the effective PNP bipolar junction transistor has a narrow un-depleted and conductivity-modulated base. Therefore α_{pnp} is high in the parasitic thyristor structure, and the thyristor will latch up if the current is too high. In modern designs, using good shorting of the p-well, this only occurs at several times rated current and a square turn-off SOA is guaranteed.
Maximum collector-emitter voltages set by breakdown voltage of PNP bipolar junction transistor – 2500V devices available. Maximum collector current set by latch up considerations – 100A for 10 µsec and still turn-off via gate control. Maximum junction temp. 150 degC. Manufacturer specifies a maximum rate of increase of re-applied collector-emitter voltage to avoid latch up.

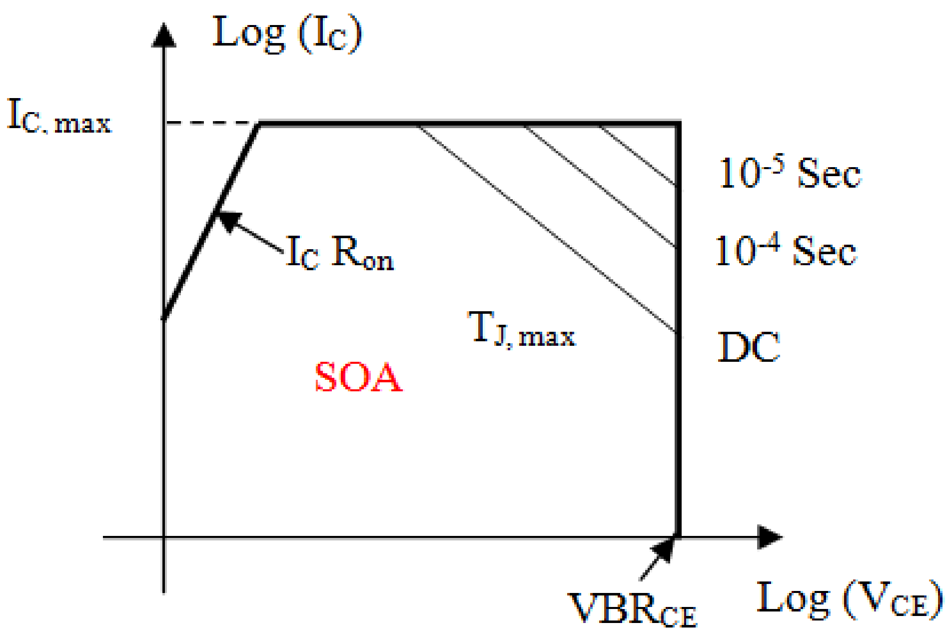


Figure 55: IGBT Forward biased Safe Operating Area (SOA).

5.18 Reverse Bias Safe Operating Area (RBSOA)

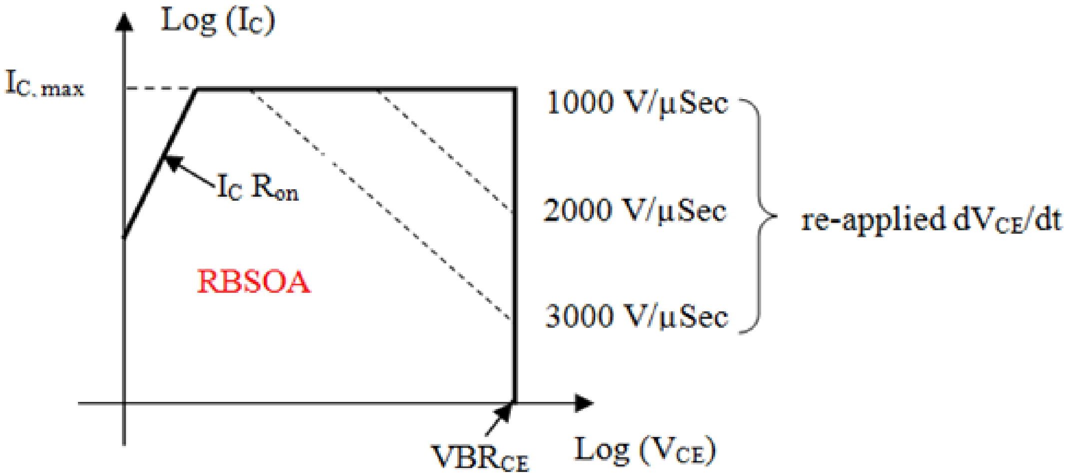


Figure 56: IGBT Forward biased Safe Operating Area (RBSOA).

5.19 Wolfson Lab Testing of power IGBT device

High Power Semiconductor devices characterization: Device Under Test 'DUT': 600V, 20A Si IGBT; 600V, 40A Si IGBT and 1200V, 20A Si IGBT.
Wolfson Lab testing Experimental Set up (same as MOSFET section 4.20.3)

Type of Device	Devive Voltage Rating	Device Current Rating
Silicon IGBT	600 V	20 A
Silicon IGBT	600 V	40 A
Silicon IGBT	1.2 KV	25 A

Table 12: Experimental IGBTs semiconductor power devices.

5.20 Lab Experiment: IGBT Transfer electrical characteristics

DUT: 600 V,20A silicon power IGBT

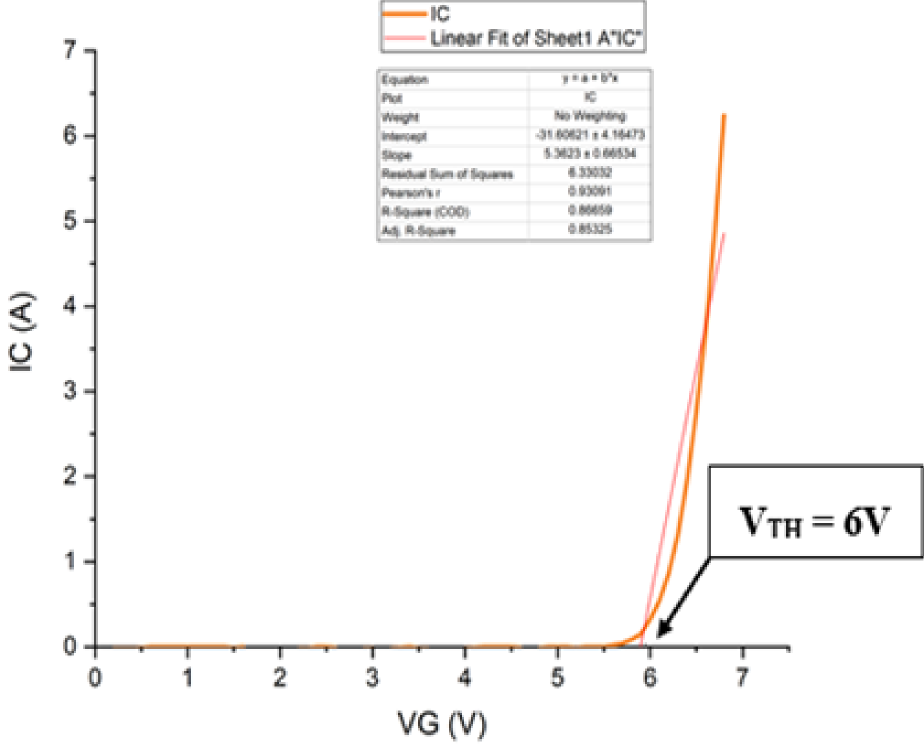


Figure 57: IGBT I_C - V_{GE} transfer electrical characteristics [60].

The figure 57 shows the threshold voltage $V_{TH} = 6\text{V}$ of 600V, 20A silicon power IGBT. This means that the device gets turned on at 6V and starts to conduct collector to emitter current.

5.21 Lab Experiment test conditions for transfer characteristics

Test Conditions	Step generator V_{GE}	Collector Current I_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Current I_{CE} - Voltage V_{GE}
Force Conditions Mode	SWEEP	CONSTANT I_{CE}
Start	0V	10V
Stop	7V	10V
Source type	-	High Power High Current

Table 13: IGBT I_{CE} - V_{GE} test condition transfer characteristics.

5.22 Lab Experiment IGBT output electrical characteristics

DUT: 600 V, 20A silicon IGBT.

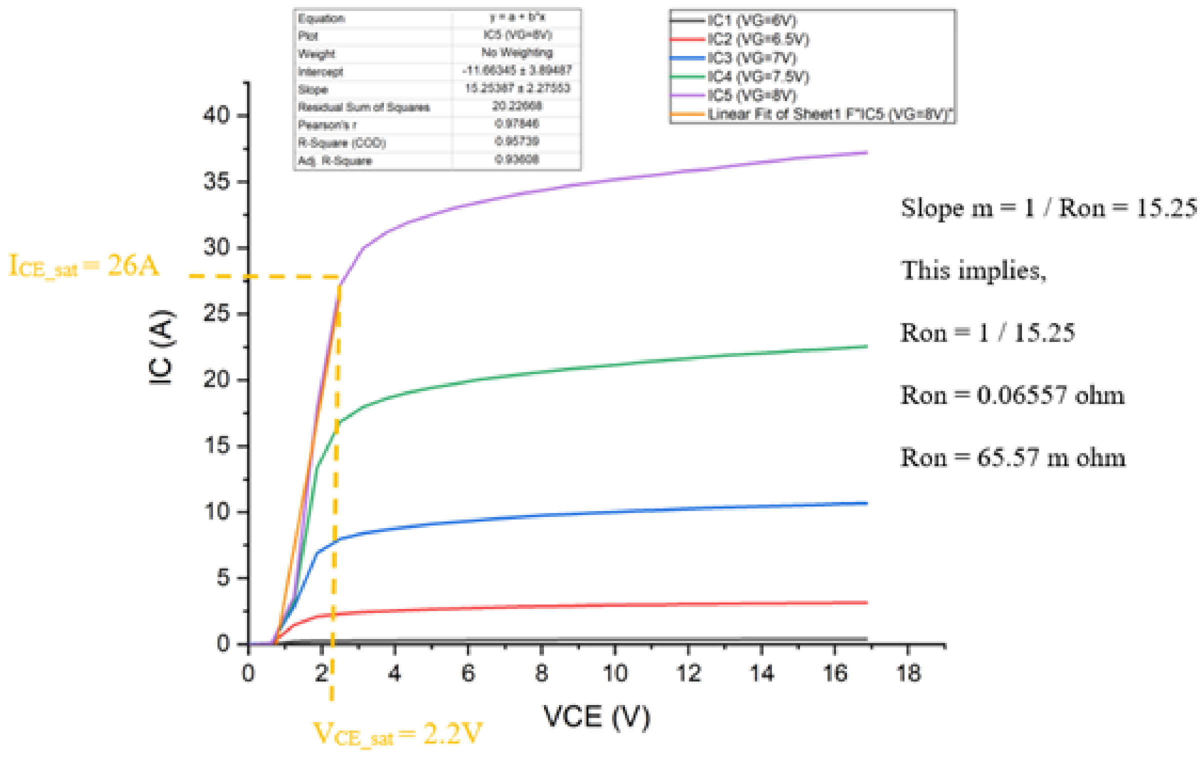


Figure 58: IGBT I_C - V_{CE} output electrical characteristics [60].

5.22.1 Lab test conditions for output characteristics

DUT: 600V, 20A Silicon Power IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Current I_{CE} - Voltage V_{CE}
Force Conditions Mode	STEP	SWEEP V_{CE} - STEP I_{CE}
Start	6V	0V
Stop	8V	20V
Source type	-	High Power High Current (HPHC)

Table 14: IGBT I_C - V_{CE} lab testing conditions for output characteristics.

5.23 Lab Experiment: Electrical breakdown characteristics

DUT: 600V, 20A Silicon Power IGBT. Power curve tracer snap shot.

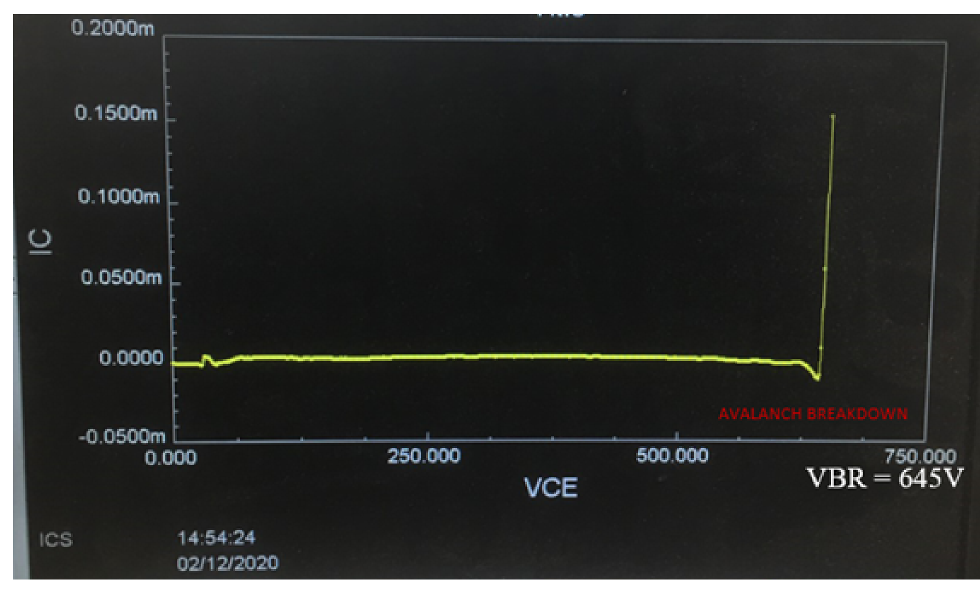


Figure 59: Electrical breakdown test I_{CE} (mA) & V_{CE} (V).

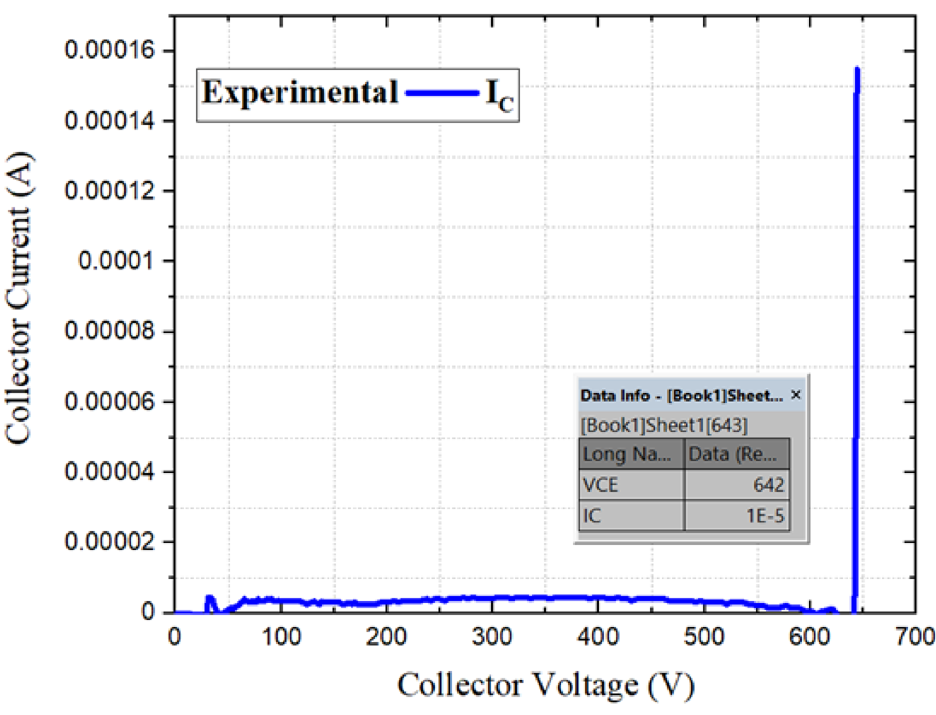


Figure 60: LAB experiment electrical breakdown test I_{CE} (A) & V_{CE} (V) [60].

Device Under Test: 600V, 20A Silicon Power IGBT showing breakdown voltage of V_{BR} = 645V. The breakdown voltage V_{BR} is greater by 7.33% than IGBT rated voltage value 600V, 20A.

5.23.1 Lab experiment test conditions for breakdown characteristics

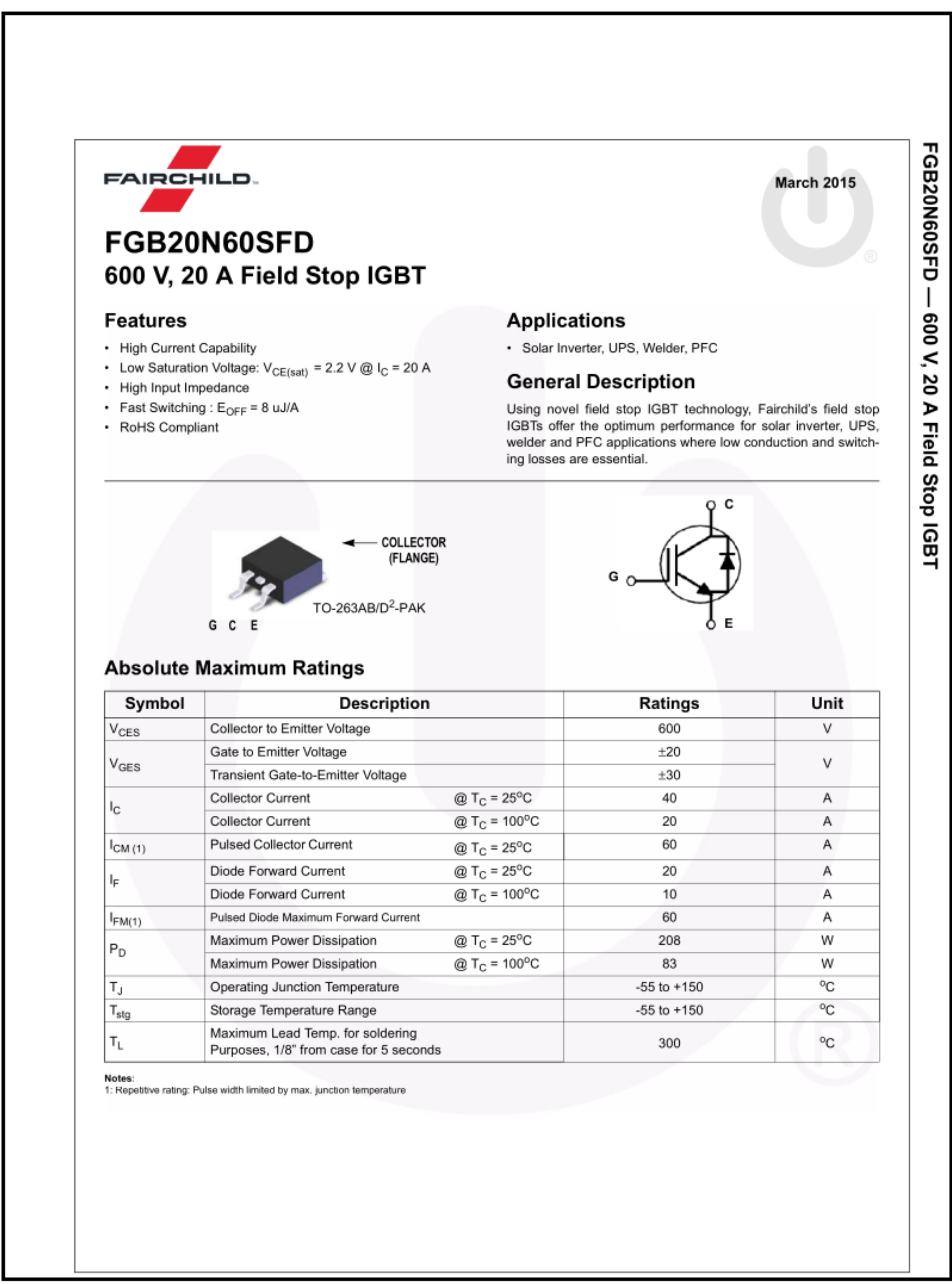
DUT: 600V, 20A Silicon Power IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{CE}
Force Conditions Mode	CONSTANT	SWEEP V_{CE} - STEP I_{CE}
Start	0V	0V
Stop	0V(Grounded)	650V
Source type	-	High Power High Voltage (HPHV)

Table 15: IGBT Experiment Electrical Breakdown Test conditions.

5.24 Manufacturer Datasheet

Company datasheet for IGBT, n-channel fast with diode 600V, 20A, TO247.
Experimental result: $R_{CE(ON)} = 65.57$ mΩ; $V_{CE(SAT)} = 2.2$ V; $I_{CE} = 20$A.
Datasheet result: $V_{CESAT} = 2.2$ V; $I_{CE} = 20$A.



FAIRCHILD

March 2015

FGB20N60SFD — 600 V, 20 A Field Stop IGBT

FGB20N60SFD
600 V, 20 A Field Stop IGBT

Features

- High Current Capability
- Low Saturation Voltage: $V_{CE(sat)}$ = 2.2 V @ I_C = 20 A
- High Input Impedance
- Fast Switching : E_{OFF} = 8 uJ/A
- RoHS Compliant

Applications

- Solar Inverter, UPS, Welder, PFC

General Description

Using novel field stop IGBT technology, Fairchild's field stop IGBTs offer the optimum performance for solar inverter, UPS, welder and PFC applications where low conduction and switching losses are essential.

Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector to Emitter Voltage		600	V
V_{GES}	Gate to Emitter Voltage		±20	V
	Transient Gate-to-Emitter Voltage		±30	
I_C	Collector Current	@ T_C = 25°C	40	A
	Collector Current	@ T_C = 100°C	20	A
$I_{CM\ (1)}$	Pulsed Collector Current	@ T_C = 25°C	60	A
I_F	Diode Forward Current	@ T_C = 25°C	20	A
	Diode Forward Current	@ T_C = 100°C	10	A
$I_{FM(1)}$	Pulsed Diode Maximum Forward Current		60	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	208	W
	Maximum Power Dissipation	@ T_C = 100°C	83	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Notes:
1: Repetitive rating: Pulse width limited by max. junction temperature

Figure 61: Datasheet silicon IGBT 600V, 20A

5.25 Transfer Electrical Characteristics

DUT: IGBT, N CH, FAST, W/DIO, 600V, 40A, TO247

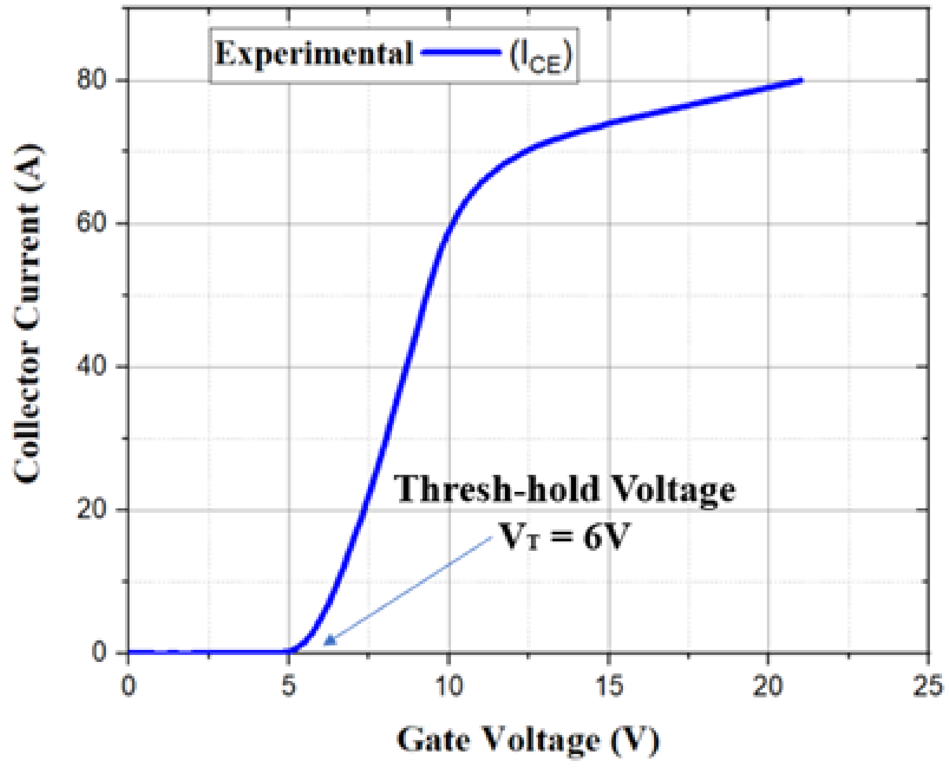


Figure 62: 600V, 40A Silicon IGBT Transfer Electrical Characteristics

5.26 Lab Experiment Test conditions transfer characteristics

DUT: 600V, 40A Silicon IGBT

Test Conditions	Step generator V_{GE}	Collector Current I_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{GE}
Force Conditions Mode	SWEEP	CONSTANT I_{CE}
Start	0V	10V
Stop	7V	10V
Source type	-	High Power High Current 'HPHC'

Table 16: IGBT I_{CE} - V_{GE} test condition transfer characteristics.

5.27 IGBT output Characteristics.

DUT: IGBT, N CH, FAST, W/DIO, 600V, 40A, TO247 test

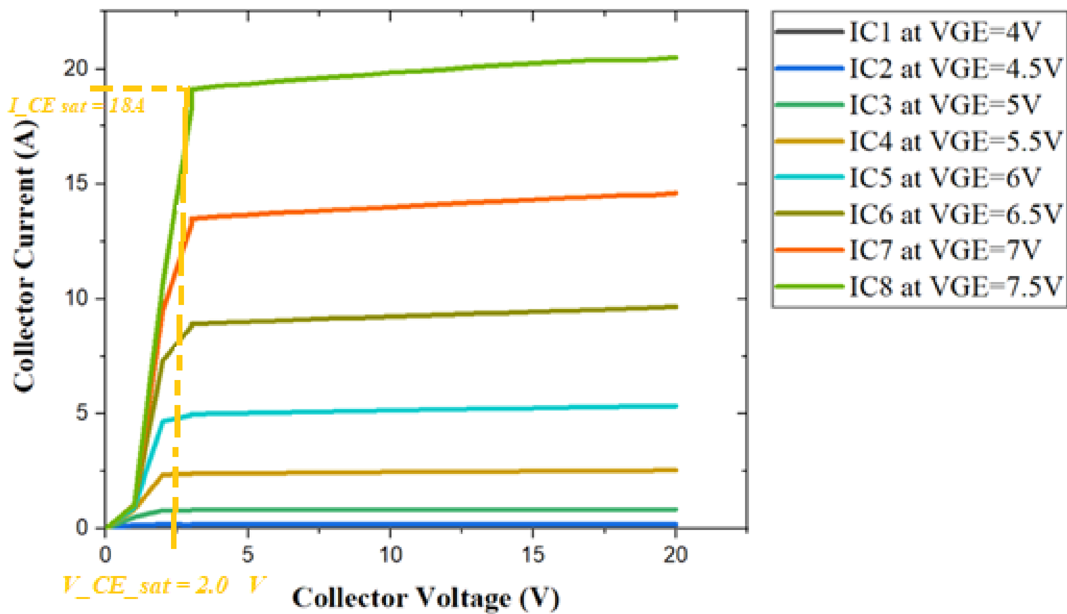


Figure 63: 600V, 40A Silicon IGBT Output Electrical Characteristics [60].

5.28 Lab Experiment Test conditions output characteristics

DUT: 600V, 40A Silicon IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{CE}
Force Conditions Mode	STEP	SWEEP V_{CE} and STEP I_{CE}
Start	4V	0V
Stop	7.5V	20V
Source type	-	High Power High Current 'HPHC'

Table 17: IGBT I_C - V_{CE} lab testing conditions for output characteristics.

5.29 Breakdown Electrical Characteristics

DUT: IGBT, N CH, FAST, W/DIO, 600V, 40A, TO247 test

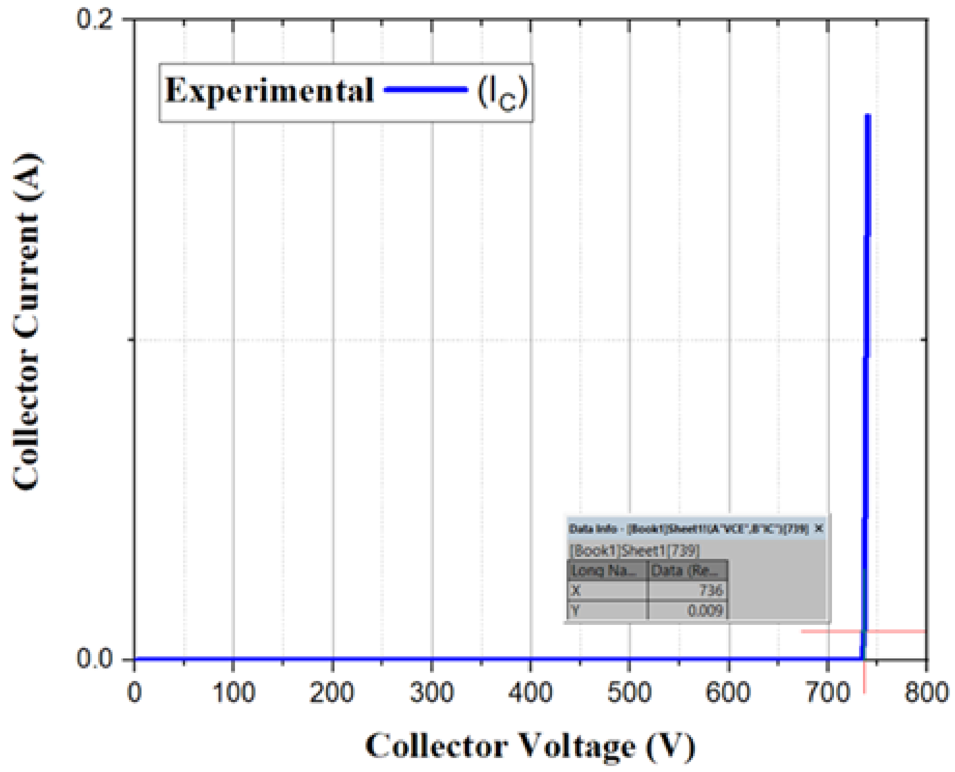


Figure 64: 600V, 40A Silicon IGBT Breakdown Electrical Characteristics [60]

Device Under Test: 600V, 40A IGBT (Si); Showing breakdown voltage of $V_{BR} = 736$V. The breakdown V_{BR} is greater by 22.7 % than IGBT rated voltage, 600V, 40A.

5.30 Lab Test Conditions for breakdown characteristics

DUT: 600V, 40A Silicon Power IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{CE}
Force Conditions Mode	CONSTANT	SWEEP V_{CE} - STEP I_{CE}
Start	0V	0V
Stop	0V(Grounded)	750V
Source type	-	High Power High Voltage HPHV'

Table 18: 600V, 40A Silicon IGBT Breakdown V_{BR} test conditions.

5.31 Manufacturer Datasheet

Company datasheet for IGBT, n-channel fast with diode 600V, 40A, TO247.

Experimental result: $V_{CE(SAT)} = 2.05$ V; $I_{CE} = 40$A.

Datasheet result: $V_{CE(SAT)} = 2.05$ V @ $I_{CE} = 40$A.

UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

40 A, 600 V

HGTG20N60B3D

The HGTG20N60B3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on−state conduction loss of a bipolar transistor. The much lower on−state voltage drop varies only moderately between 25°C and 150°C. The diode used in anti−parallel with the IGBT is the RHRP3060.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

Formerly developmental type TA49016.

Features

- 40 A, 600 V at T_C = 25°C
- Typical Fall Time 140 ns at 150°C
- Short Circuit Rated
- Low Conduction Loss
- Hyperfast Anti−Parallel Diode
- This is a Pb−Free Device

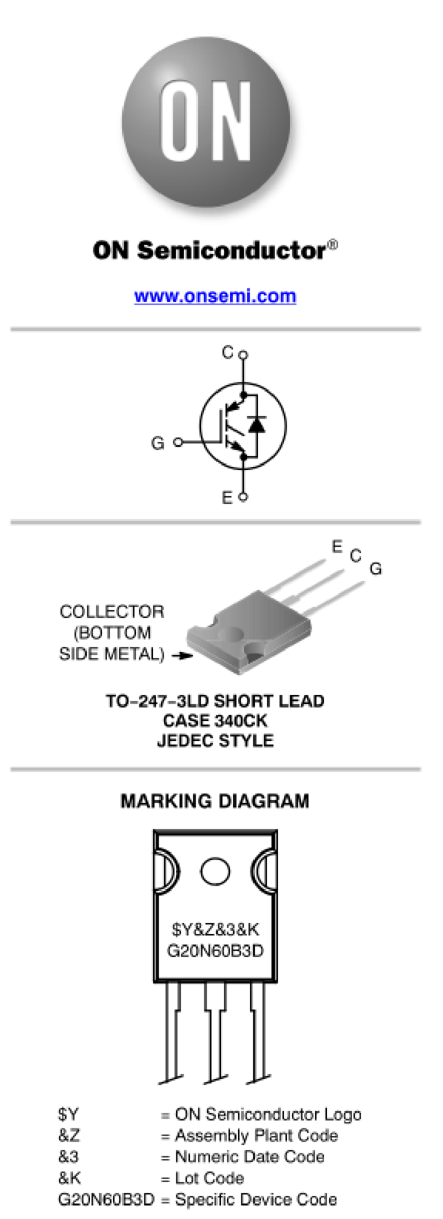


Figure 65: Datasheet silicon IGBT 600V, 40A, TO-247.

5.32 Transfer Electrical Characteristics

DUT: 1200V, 40A Silicon IGBT.

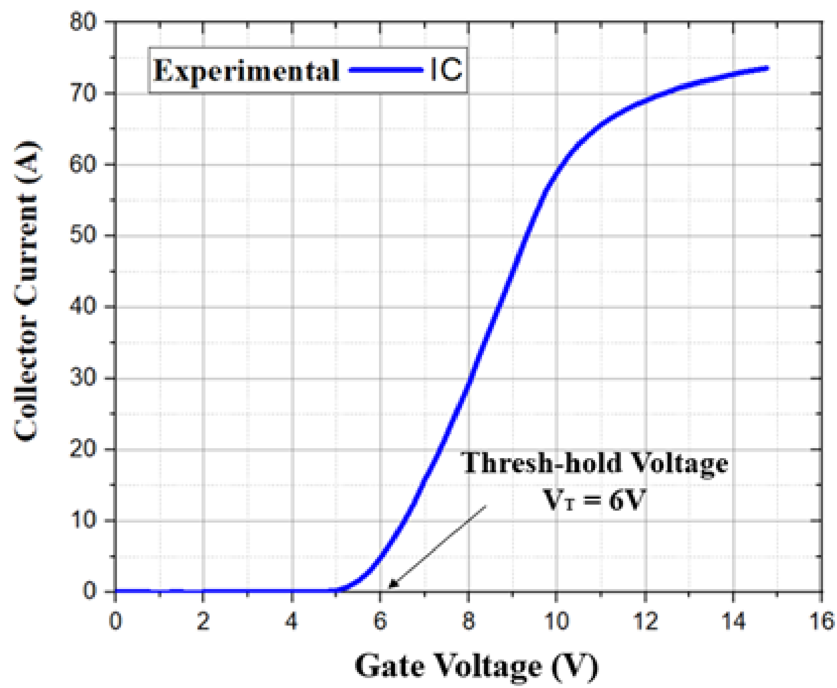


Figure 66: 1200V, 40A Silicon IGBT Transfer characteristics [60].

5.33 Lab Experiment: Test conditions transfer characteristics

Test Conditions	Step generator V_{GE}	Collector Current I_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{GE}
Force Conditions Mode	SWEEP	CONSTANT I_{CE}
Start	0V	10V
Stop	7V	10V
Source type	-	High Power High Current 'HPHC'

Table 19: 1.2KV, 40A silicon IGBT I_{CE} - V_{GE} test condition transfer characteristics.

5.34 Output Electrical Characteristics

DUT: 1200V, 40A Silicon IGBT

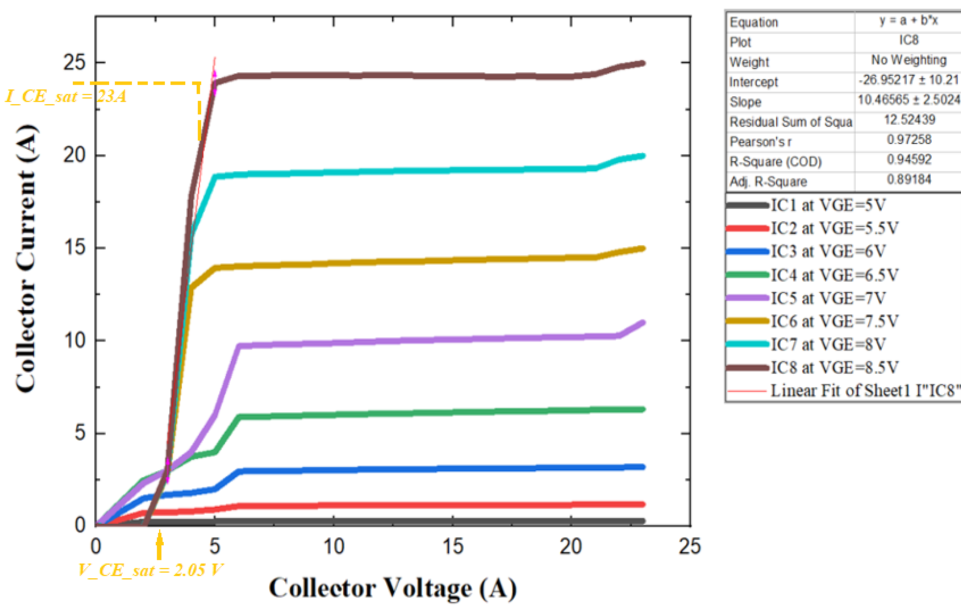


Figure 67: 1200V, 40A Silicon IGBT Output characteristics [60].

5.35 Lab Test Conditions for output characteristics

DUT: 1200V, 40A Power IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{CE}
Force Conditions Mode	STEP	SWEEP V_{CE} and STEP I_{CE}
Start	5V	0V
Stop	8.5V	20V
Source type	-	High Power High Current 'HPHC'

Table 20: 1.2KV, 40A silicon IGBT I_{CE} - V_{CE} test conditions for output characteristics.

5.36 Electrical Breakdown Characteristics

DUT: 1200V, 40A Silicon IGBT

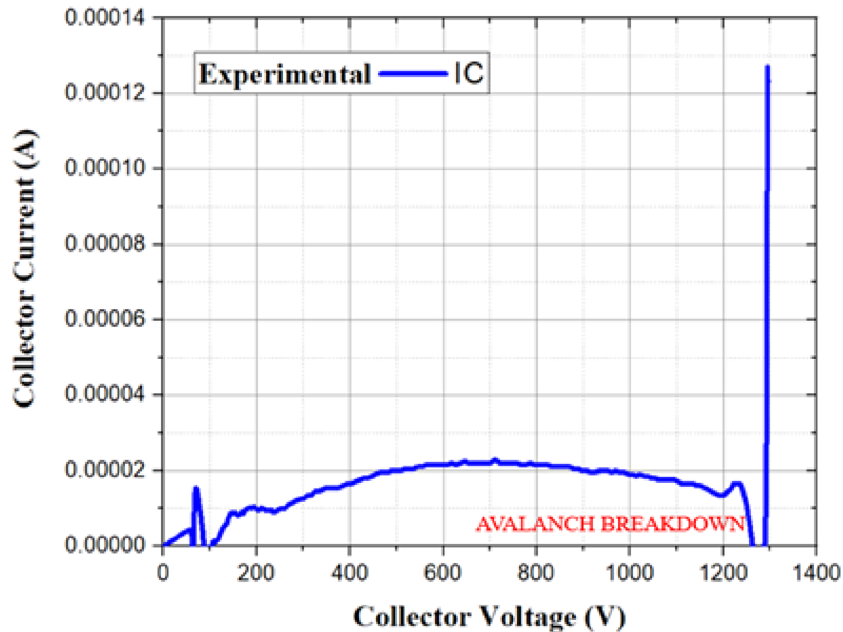


Figure 68: 1200V, 40A Silicon IGBT Breakdown characteristics [60].

Collector voltage avalanches just before its breakdown: Starting V_{BR} = 1270V until it reaches final V_{BR} = 1290.5V; at collector current I_{CE} = 6.899e-6A.
The breakdown voltage V_{BR} = 1290.5V is greater by 14.25% than the IGBT device manufacturer's rated voltage 1200V, 40A.

5.36.1 IGBT Electrical Breakdown Test Conditions

DUT: 1200V, 40A Silicon IGBT

Test Conditions	Step generator V_{GE}	Collector Voltage V_{CE}
Stimulus	Voltage	Voltage
Polarity	Positive	Positive
Measure	Gate Voltage V_{GE}	Collector Current I_{CE} - Collector Voltage V_{CE}
Force Conditions Mode	CONSTANT	SWEEP V_{CE} - STEP I_{CE}
Start	0V	0V
Stop	0V(Grounded)	1400V
Source type	-	High Power High Voltage HPHV'

Table 21: 1.2KV, 40A Silicon IGBT Breakdown V_{BR} test conditions.

5.37 Manufacturer Datasheet

Company datasheet for IGBT, n-channel 1200V, 25A, TO247.

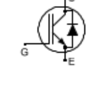
Experimental result: $V_{CE(SAT)} = 2.0$ V; $I_{CE} = 40$A.

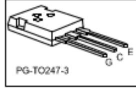
Datasheet result: $V_{CE(SAT)} = 2.05$ V @ $I_{CE} = 40$A.

IKW25N120H3

High speed switching series third generation

High speed DuoPack: IGBT in Trench and Fieldstop technology with soft, fast recovery anti-parallel diode





Features:

TRENCHSTOP™ technology offering
- very low V_{CEsat}
- low EMI
- Very soft, fast recovery anti-parallel diode
- maximum junction temperature 175°C
- qualified according to JEDEC for target applications
- Pb-free lead plating; RoHS compliant
- complete product spectrum and PSpice Models: http://www.infineon.com/igbt/

Applications:
- uninterruptible power supplies
- welding converters
- converters with high switching frequency

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Marking	Package
IKW25N120H3	1200V	25A	2.05V	175°C	K25H1203	PG-TO247-3

Maximum ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current, limited by T_{vjmax} T_C = 25°C T_C = 100°C	I_C	50.0 25.0	A
Pulsed collector current, t_p limited by T_{vjmax}	I_{Cpuls}	100.0	A
Turn off safe operating area V_{CE} ≤ 1200V, T_{vj} ≤ 175°C	-	100.0	A
Diode forward current, limited by T_{vjmax} T_C = 25°C T_C = 100°C	I_F	25.0 12.5	A
Diode pulsed current, t_p limited by T_{vjmax}	I_{Fpuls}	100.0	A
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time V_{GE} = 15.0V, V_{CC} ≤ 600V, T_{vj} ≤ 175°C Allowed number of short circuits < 1000 Time between short circuits: ≥ 1.0s	t_{SC}	10	µs
Power dissipation T_C = 25°C Power dissipation T_C = 100°C	P_{tot}	326.0 156.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s		260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

Figure 69: Datasheet silicon IGBT 1200V, 25A, TO-247.

5.38 IGBT Silvaco simulation single cell cross-section

Figure 70 showing the Gate, Collector and Emitter contacts of the IGBT structure.

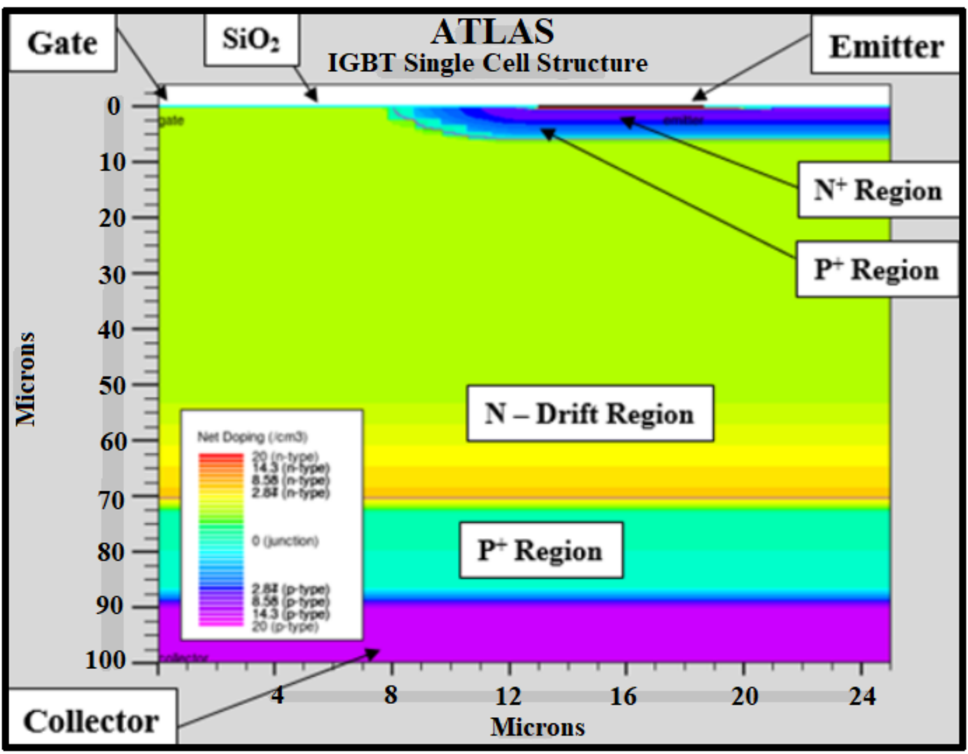


Figure 70: IGBT device single cell structure [43].

5.39 Silvaco simulation IGBT electrical characterization.

The figure above shows conduction or output electrical characteristics of an IGBT structure. Definition of test $I_C - V_{CE}$; the IGBT collector current I_C versus collector voltage V_{CE} output electrical characteristics. Simulation of an IGBT output characteristics is performed by sweeping the collector contact voltage for several discrete values of gate-to-emitter voltage V_{GE}. In this simulation, the collector-to-emitter voltage V_{CE} will be swept from 0 to 20 V for gate-to-emitter V_{GE} voltages of 5 and 10 Volt. This was achieved by first getting a solution at each gate bias of interest with all other electrodes kept at 0 Volt. Subsequently, each gate solution is used as the initial solution for a collector sweep.

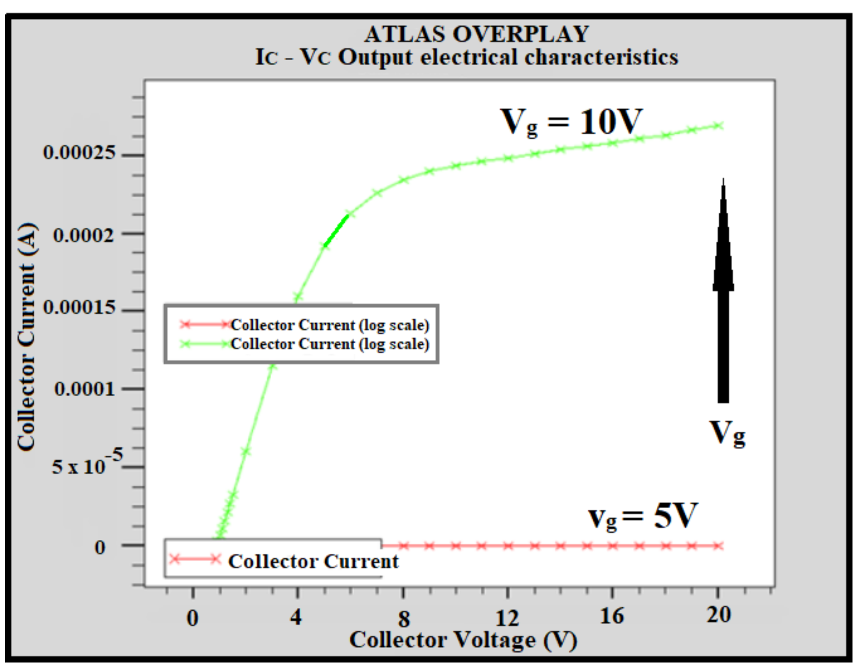


Figure 71: IGBT I_C - V_{CE} characteristics [43].

5.40 IGBT single cell internal Mesh structure

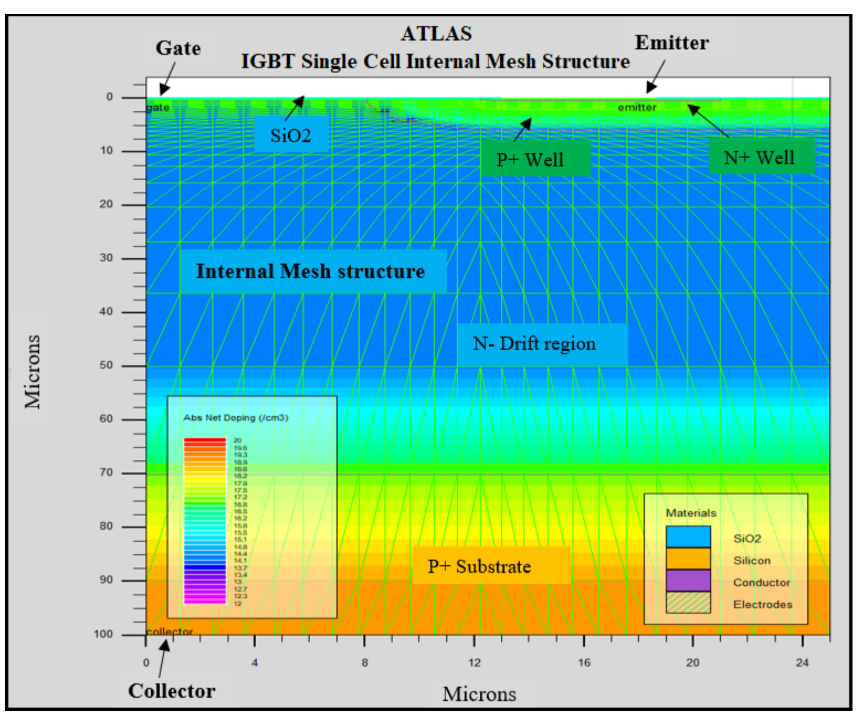


Figure 72: IGBT Single cell a fine rectangular mesh internal structure [43].

IGBT single cell rectangular mesh allows to observe formation of internal structure and useful for easy identification of neighbouring cells and points.

5.41 IGBT Transient Latch-up with Lattice Heating

The figure 73 is simulation of the non-isothermal latch-up of an IGBT structure and waveform showing collector current and maximum temperature of the IGBT versus time. The latch-up happened during transient or switching mode. Because of the high currents during latch-up a significant local heating occurs in the IGBT structure. Hence, the solution of lattice temperature and heat flow must be included.
Transient gate voltage ramp to produce latch-up:
The IGBT structure is defined using Atlas. First, a fine rectangular mesh was defined, and the materials are assigned to regions by using the region command. Then the gate, collector, emitter electrodes and the doping profiles are defined. Furthermore, the structure definition includes specific characteristics of these materials, their electrodes, and the charge carriers within can be modified. In addition, the electron and hole recombination lifetimes in the semiconductor are defined by using the material statement. Further, the work function of the polysilicon electrode, in this case, that of degenerately doped n-type polysilicon is defined using the contact statement.
The model statement is used to enable the physical transport models. The physical transport models must be enabled using the model statement, in order to reflect the different physical effects important to the IGBT device. The analytic physical effects are concentration dependent mobility, lateral electric field dependent mobility, surface mobility degradation, Shockley-Read-Hall recombination, and recombination accounting for high level injection effects. This means that the steady-state characteristics of the IGBT are now solved.
By using the solve 'init.' statement of Atlas simulation, an initial solution is calculated at zero bias. This is the starting point of the Atlas solvers and the succeeding solve statements ramp the IGBT collector voltage from 0V up to 300V in different stages. In all the following stages it uses the previous solution as a predicted starting point. Although other method of initial guessing is also possible in accordance with the Atlas User's manual. It gets fixed to its former value, which is zero volts, if an electrode bias is not specified. The solution will be saved after gaining the solution at 300V. This value will be used as an initial solution in the following transient mode latch-up simulation.
The IGBT transient mode simulation adds three more items, these are thermal contacts, heat flow, and impact ionization. The thermal boundary conditions must be stated because it is the most important part of any non-isothermal simulation. The 'therm-contact' statement is used to specify a constant temperature along the collector contact and the rest contacts and surfaces are assumed to be in thermal isolation. The heat flow is included by adding the 'lat. temp' lattice temperature model into the model statement. By

doing this we are solving the equation of heat flow and the equations of the semiconductor, this means every physical parameter becoming dependent of the temperature. The heat flow and impact ionization play very significant role in the transient mode latch-up of an IGBT. By using the impact statement with 'selb' option was activated impact ionization model. This completes IGBT gate transient simulation.

The latch-up simulation uses as its initial guess the previously saved solution at the collector bias of 300V. Additional or more solution quantities were added to the standard output variables by using the output statement. The IGBT latch-up was caused by the gate voltage that ramped from zero volts to 10 volts in 100 nanoseconds. Then the gate voltage was fixed at the 10 V level until the time reaches 1 micro-second. By using the solve statement these conditions were set and saved the output results using log file. The collector current and maximum temperature of the IGBT versus time waveform enables to closely see the latch-up. The latch-up waveform was plotted by using Tony-Plot command statement. Tony-Plot observation of all output variables is possible and the structure with the solution at the final point is saved.

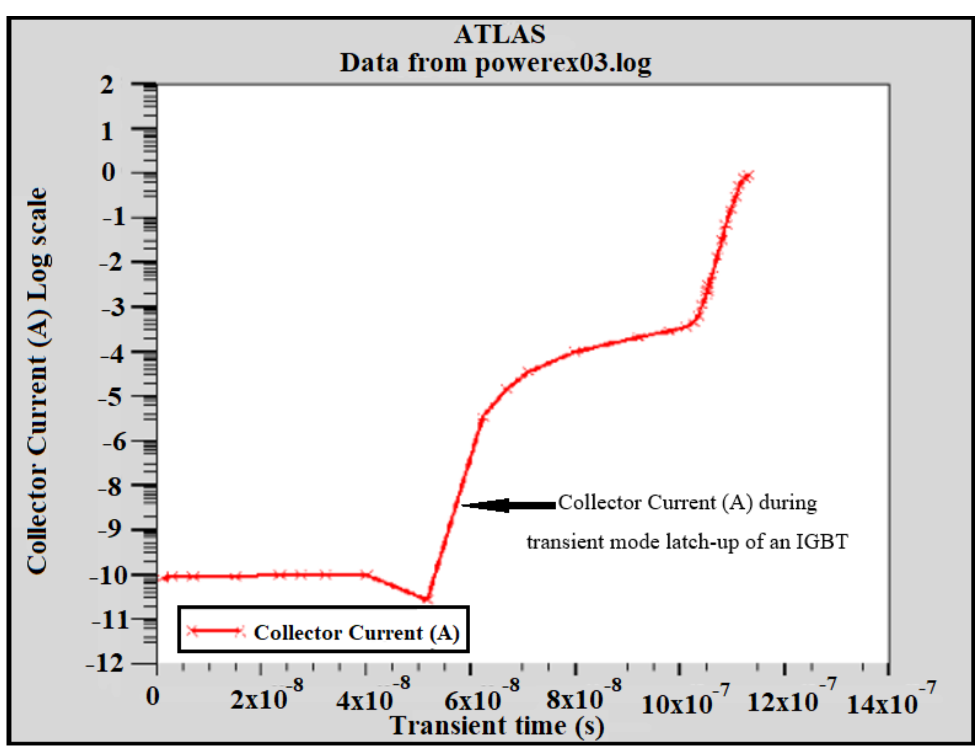


Figure 73: Collector current (A) versus Transient time (Sec.) [43].

5.42 Trench Etching of an IGBT structure

This simulation shows the use of Elite to model trench etching. Wet and dry etching are two types of trench etching techniques:

1. Wet etching where the material is dissolved when immersed in a chemical solution.
2. Dry etching where the material is sputtered or dissolved using reactive ions or a vapour phase etchant.

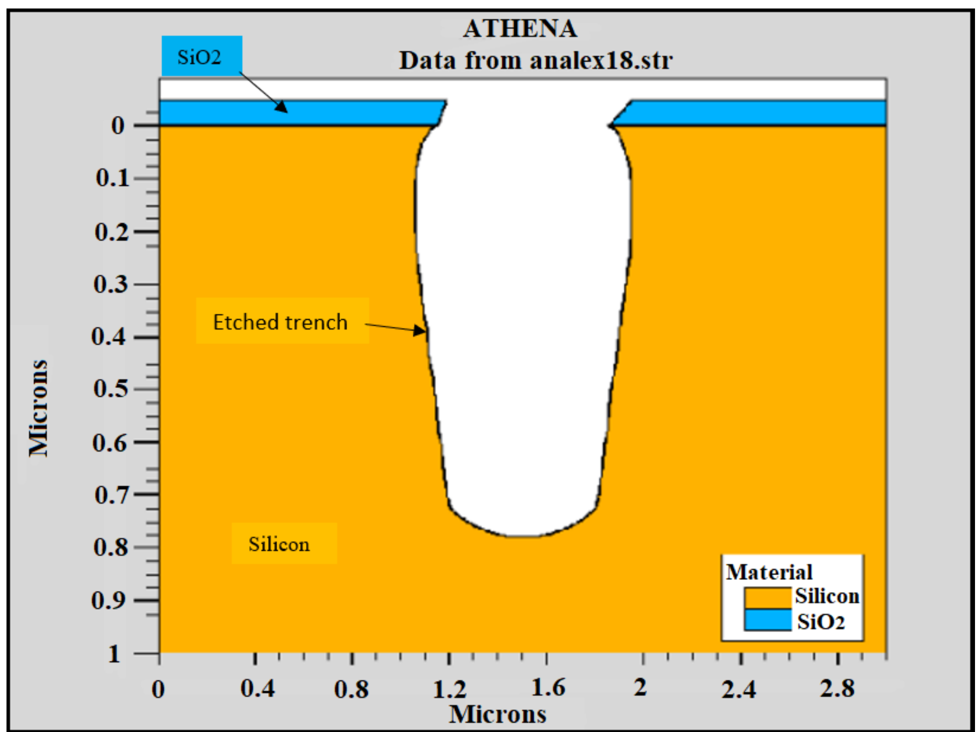


Figure 74: Etched trench gate structure of an IGBT [43].

5.43 Trench gate Oxidation

The figure 75 below shows two different types of etch conditions of modelling the trench process by using Elite. After the formation of the trench gate an oxide layer is grown. When using Elite etch the trench surface may become uneven, however this will not prevent the oxidation simulation process. The final structure was plotted by using Tony-Plot.

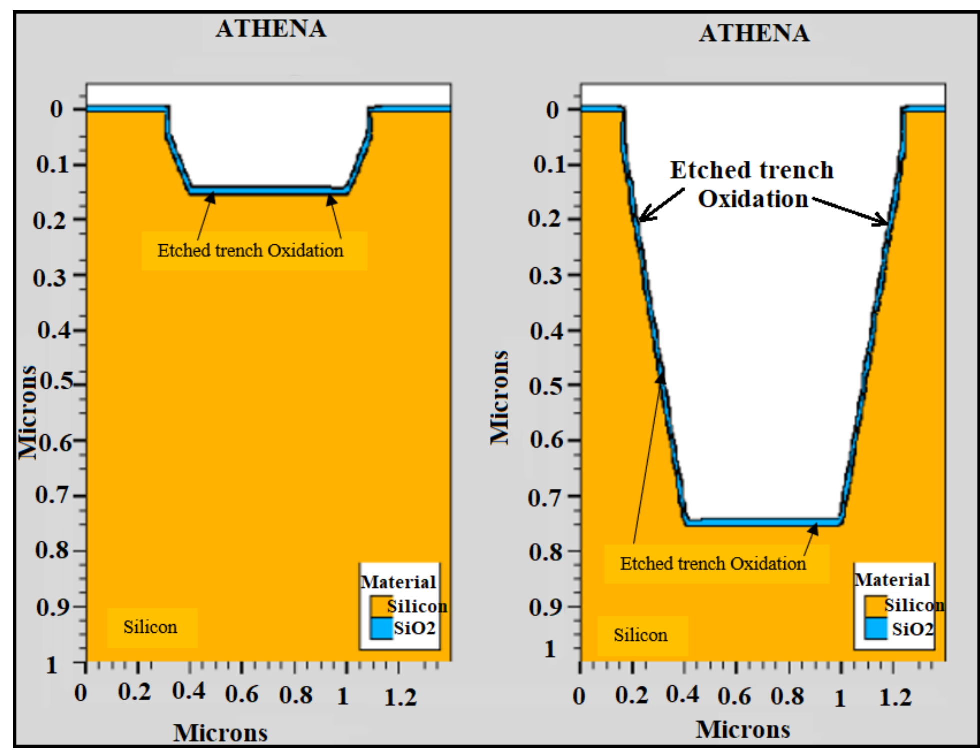


Figure 75: Trench Oxidation of two different etch conditions [43].

5.43.1 Trench Filling and Planarization

Figure 76 below showing demonstration of a simple trench gate filling, planarization, and etch back. The statement 'ETCH' was used to define the profile of the initial trench, with a bottom critical dimension of 0.6 micro-meter and 87deg sidewall slopes.

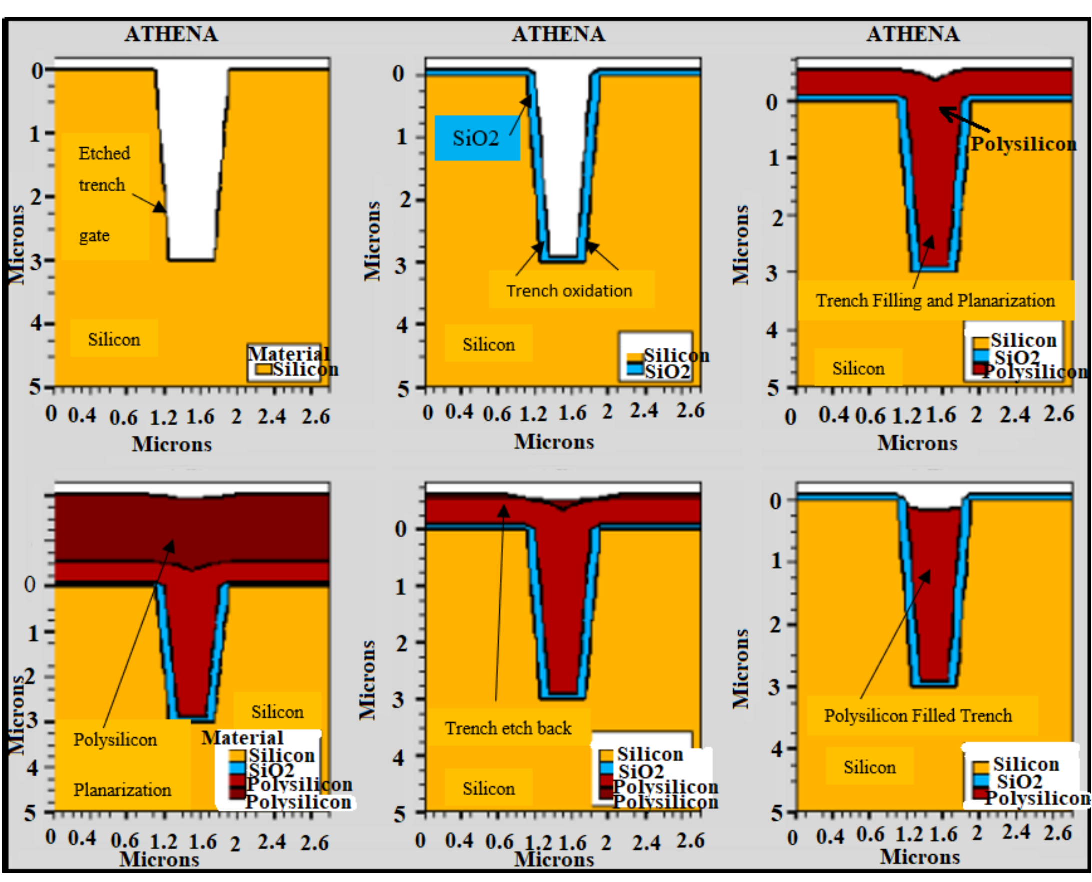


Figure 76: Trench Oxidation of two different etch conditions [43].

5.44 Punch-through test across the trench using Atlas

The figure 77 below showing a demonstration of punch-through between unrelated n+ regions separated by trench gate structure isolation. The trench was formed by using 'ELITE' physical etch models and the trench doping by using 'SSUPREM4' syntax implant models. And the trench fill by using 'ELITE' physical deposition models.
Punch-through test across the trench using Atlas:
The demonstration includes two parts, first construction of the geometry using Athena and doping of two n+ areas separated by trench isolation. Second, simulation of punch through between the two n+ regions by using Atlas. The formation of trench gate using Reactive Ion Etching 'RIE', with different isotropic and anisotropic etch rates for each material present. Implantation of the field is carried out direct inside the trench.
Using Atlas automatic interfacing of the device and selection of impact ionization together with the two-carrier mode. The drain contact is ramped to 20 volts while monitored by the current compliance limit of 3 nano-Amp-per-micro-meter. After the simulation is completed the drain current final contours are plotted, where the current density can be seen to avoid the field implant doping peak. By using the extract statement measurement of design parameters were performed at the end of the Atlas simulation. When defining the parameter, it is the drain voltage needed to get 2 nano-Amp-per-micro-meter of drain current.

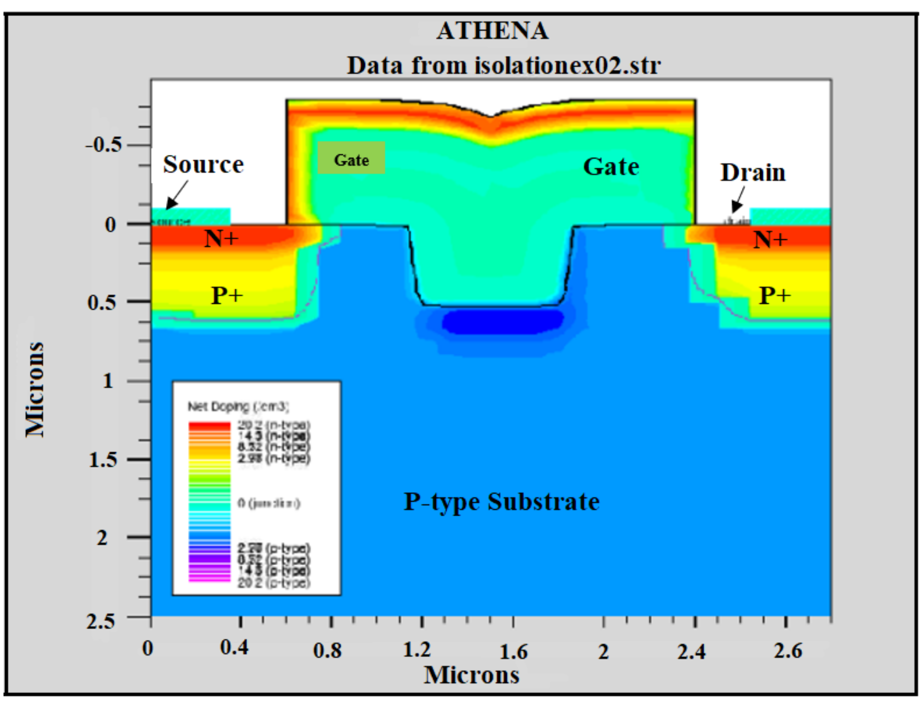


Figure 77: Figure Trench Isolation Structure [43].

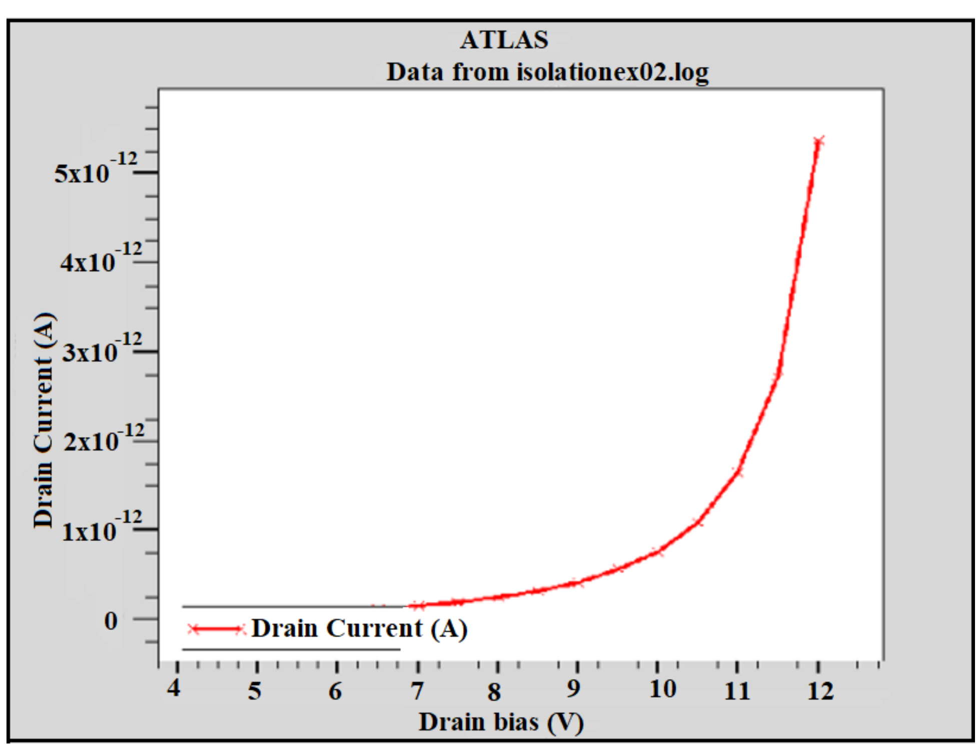


Figure 78: Figure Drain current (A) vs drain bias (V) [43].

5.45 Three-dimensional '3D' Trench IGBT

In the present-day power electronics fabricating power devices using silicon material are still dominant. Moreover, compounding semiconductor produced Silicon Carbide 'SiC', which offers a better material property compared to silicon. Wide bandgap semiconductor SiC has superior thermal conductivity, lower intrinsic carrier concentration and lower on-resistance which is a key figure of merit in power switching technology, and all these features desirable for high power, high-temperature applications.

Simulating a silicon carbide device has more challenge compared to silicon devices. Obviously very low intrinsic concentration together with high doping concentration values have negative impact on convergence. Silicon Carbide exhibits hexagonal crystal structures. Consequently, the anisotropy characteristics in several key physical parameters, for instance impact ionization must be considered.

5.46 Demonstration of 3D trench gate SiC IGBT.

The simulation was performed by using Victory Cell and Victory Device. Victory Cell is a 3D process simulator used in creating a 3D structure. For 3D Silicon Carbide device simulation Victory Cell is the appropriate simulator because it is layout driven, accurate, fast, and easy to use. Also, it takes only few minutes to create a 3D structure in Victoria Cell. The distinctiveness of the device under simulation is to have a drift region with very low doping concentration and drift region thickness of about 160 micro-meters. This means that the device will have a blocking capability of high breakdown voltage.

In this simulation the focus was set on the breakdown voltage and IV characterization, this includes I_C - V_G and I_C - V_C to illustrate a 3D specific effect. From the observation of I_C - V_G characterization curve reveals a 'hump' effect due to non-planar structure. This 'hump' effect of the gate is detected in the I_C - V_G waveform as a parasitic transistor. This can cause negative influence on the power consumption because it increases the off-current. One way of overcoming this drawback includes rounding trench corner rather than 90 deg trench corner. It has minimized the 'hump' effect of the gate, thereby improving the breakdown voltage.

Following completed process simulation to save the 3D structure 'tetrahedron mesh' is used, this way of saving conserves well any shape created during 3D process simulation, further it transfers the created structure to Victory Device for the next step of device simulation. To ensure that low intrinsic carrier concentration is resolved, the device simulation was carried out by making use of extended precision arithmetic, 80 bits or 128-bit depending on the condition of simulation performed.

As indicated in the I_C - V_G and I_C - V_C figures 5.46 shown below it is clear to identify the trench corner effect. A two-dimensional '2D' diagonal plane cut was done on the device trench bottom corner, exactly at the area higher electron current density detected for the Manhattan compared to after rounding the trench corners. Moreover, the trench corner effect has direct influence on the breakdown voltage V_{BV} and after rounding of the trench corner an improved breakdown voltage was achieved approximately 12KV. Furthermore, by plotting the 3D structure it is clear to observe the peak of the Electric Field and the Impact Generation rate gathered at the bottom of the trench.

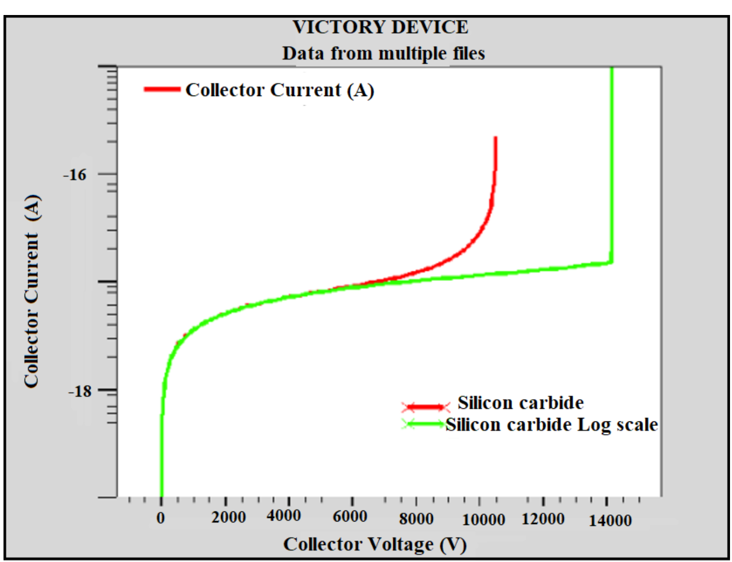


Figure 79: Collector current (A) vs Collector voltage (V) [43].

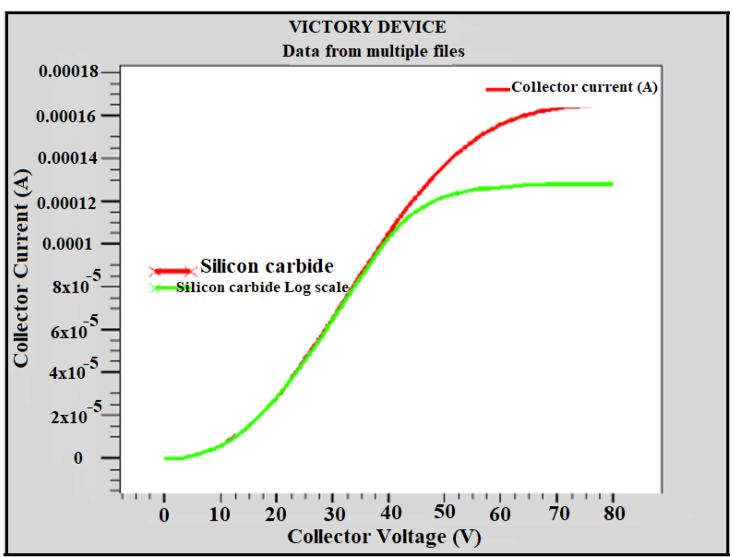


Figure 80: Collector current (A) vs Collector voltage (V) [43].

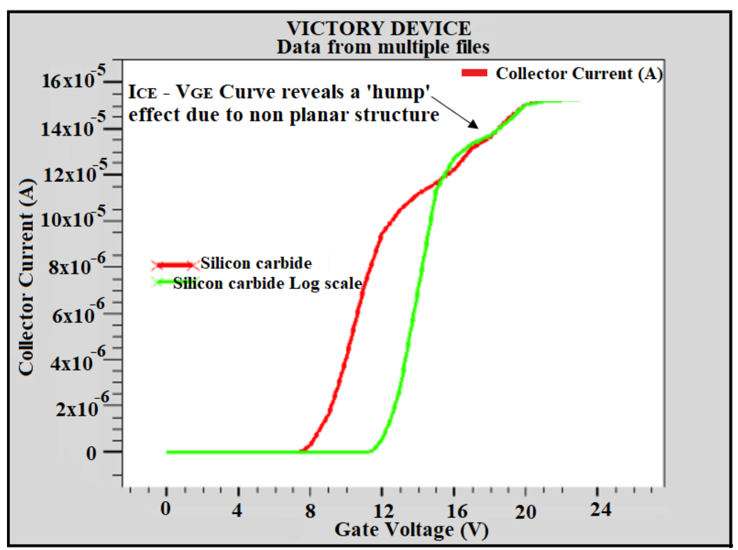


Figure 81: Collector current (A) vs Collector voltage (V) [43].

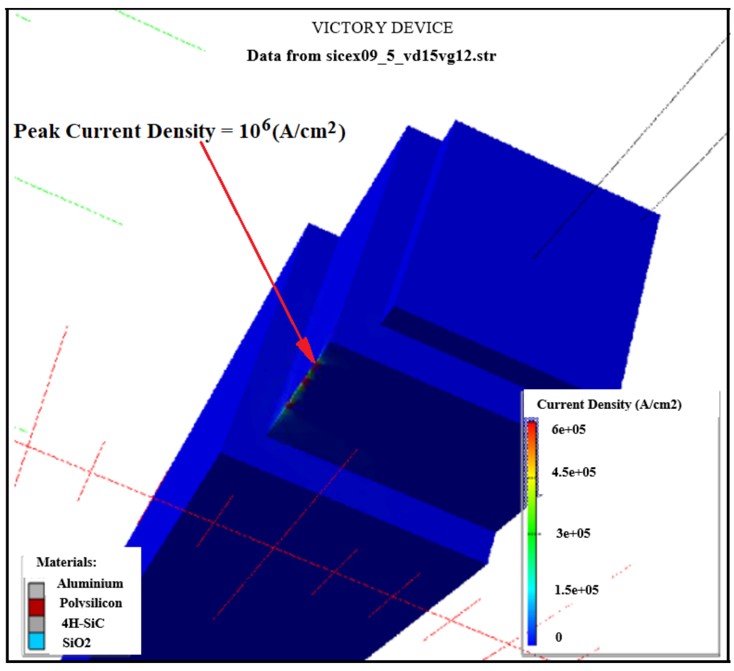


Figure 82: 3D Current Density (A/cm^2) distribution [43].

The electric field is maximum at the corner of the trench.

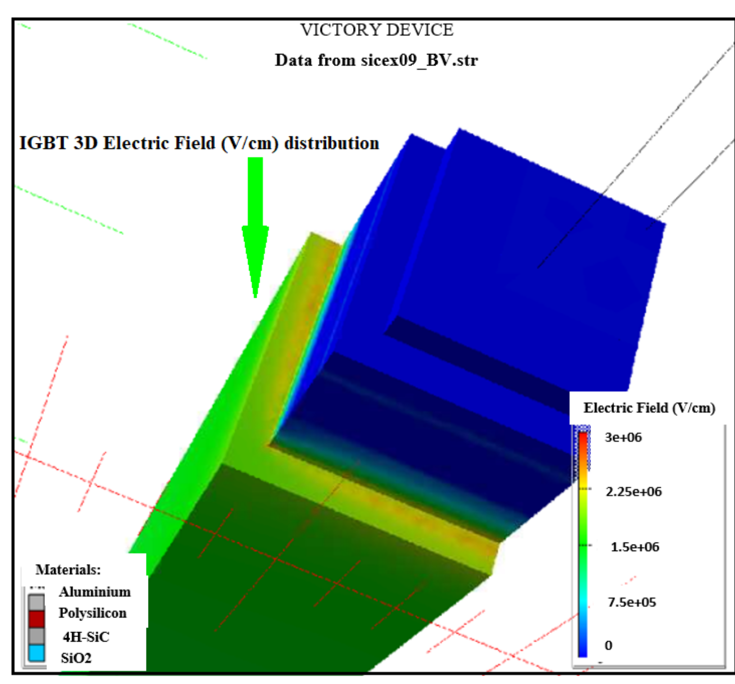


Figure 83: 3D electric field (V/cm) distribution [43].

5.47 3D Trench Shape Effect on IV and BV Characteristics of SiC IGBT

This demonstration helps to closely study the effect of the shape of a trench gate on IV and BV characteristics. At the start using Victory process the 3D layout-driven structure was created. And simulation of 3D device is performed using Victory Device built-in extended precision numeric.
Three different types of structures were compared:

1. The first structure is fully Manhattan, i.e., right angle layout and trench.
2. The second structure having rounded layout.
3. The third structure having rounded layout and angled trench.

A one dimensional '1D' simulation of Aluminium implantation were performed in order to save simulation time in Athena using Monte Carlo implantation before being imported in the 3D structure using the 'PROFILE' statement in Victory Process.
By using a full 3D Delaunay mesh were the '3D' structure saved and using EXPORT victory 'Delaunay' statement in Victory Process. Different options are available to optimize the mesh under the gate and at the PN junction. This 3D refinement is fully automatic. Using Victory Device were the 3D structure loaded. The default 3D Delaunay discretization method combined with a parallelized iterative solver set by 'PAM.MPI' statement in

Victory Device allow good convergence, speed, and accurate results. To make the optical axis parallel to the z-axis for 3D simulation so that the optical axis points toward the SiC surface, it was set 'ZETA' ζ=90 deg and 'THETA' θ=90 deg on the 'MATERIAL' statement.
It can be clearly observed that the effect of the trench shape on the I_C - V_G and BV characteristics. Indeed, known "hump" effect is observed on the I_C - V_G characteristic especially on the device with full Manhattan shape. However, this parasitic effect is removed with the device using rounded layout and angled trench. BV simulation reveals that the breakdown voltage can be increased by 30% using rounded layout and angled trench due to impact ionization not occurring any-more only at the corner of the trench.

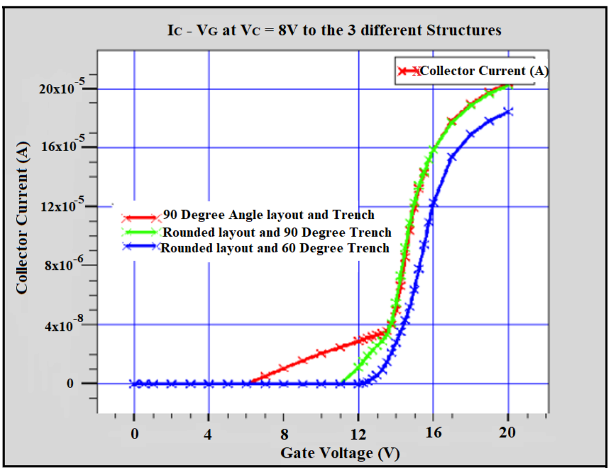


Figure 84: Collector Current (A) vs Gate Voltage (V) [43].

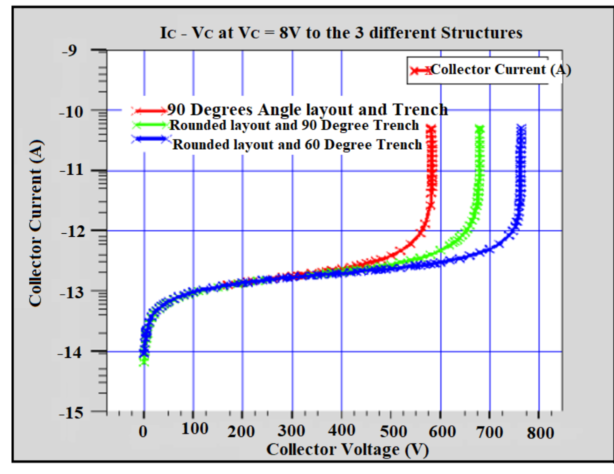


Figure 85: Collector Current (A) vs Collector Voltage (V) [43].

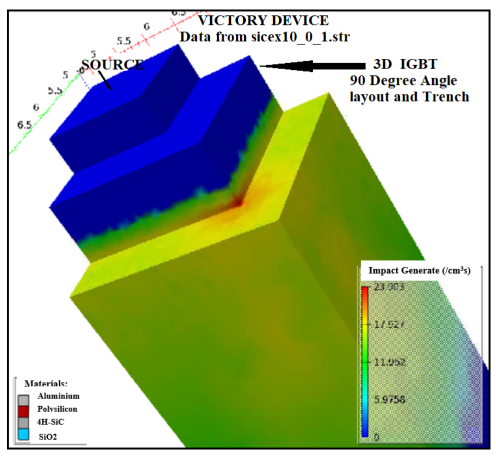


Figure 86: 3D Trench IGBT [43].

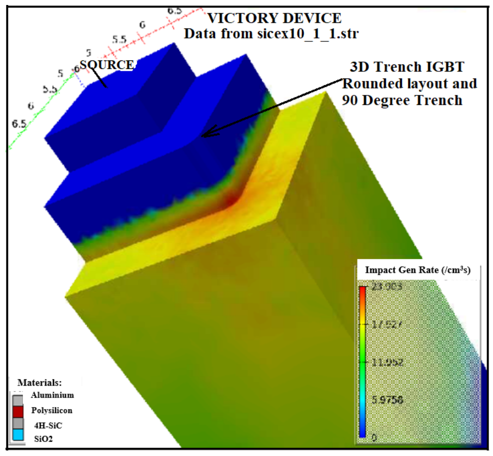


Figure 87: 3D Trench gate IGBT [43].

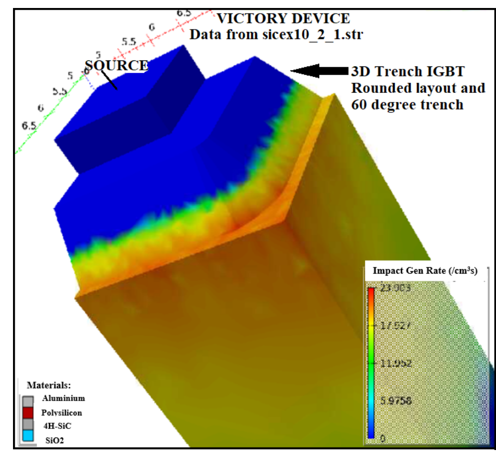


Figure 88: 3D Trench IGBT [43].

6 Conclusion

6.1 General Conclusion

MOS operation physics has been studied. Further conducted Wolfson lab demonstration of vertical MOSFETs and IGBTs. In order to understand the relevant current - voltage 'I-V' & breakdown voltage 'BV' electrical characteristics. Furthermore, a careful observation of the on-state resistance R_{ON} was made as this was the most important figure of merit for power semiconductor switches. The main target is to achieve a lower internal resistance and a robust device by deploying latest available technology. The trench gate design architecture outperforms the planar gate structure because it eliminates the JFET region, smaller pitch, lot of cell per unit area, consequently $R_{ON(Total)}$ is reduced.

Furthermore, the results achieved from Wolfson lab high power semiconductor devices characterization prove great switching performance as anticipated and also specified in manufacturer's data sheet. The analytical analysis of data quantifies the reliability and ruggedness of the MOSFET and IGBT switches under experiment. Data enabled interpretation of waveforms and calculation of transfer, output, and electrical breakdown characteristics. Moreover, experiment show that silicon carbide trench gate 1200V, 19A power MOSFET exhibit the lowest on-state resistance value, $R_{DS(ON)} = 135.18$ mΩ. This indicates that unprecedented advantages of using compound semiconductor silicon carbide as a material for high power switching applications.

In chapter five performance of Insulated Gate Bipolar Transistor IGBT has been investigated. Furthermore, the great benefits of trench gate silicon carbide IGBT has been emphasized. Trench gate IGBTs fabricated using silicon carbide material are capable of higher blocking voltages, higher switching frequencies and higher junction temperatures. The Wolfson lab demonstration of silicon power IGBT devices of 600V, 20A; 600V, 40A; and 1200V, 25A prove reliability and ruggedness. The lab experiment which includes stressing device under test using high DC voltage well beyond the breakdown limits, these switches performed without overheating and resisted up to 12% of V_{BR} more than the rated values.

6.2 Improvement suggestions

For more than a decade power electronics control systems and silicon carbide-based devices attracted huge interest from both academicians and the leading industry. This masters by research work would like to present its recommendations:

Firstly, suggesting transition to newly emerging wide band-gap silicon carbide technology due to its superior physical and electronic properties compared to silicon. Wide

band-gap silicon-carbide based devices outperformed by far their counterpart silicon devices. Silicon material property limitations low band-gap energy, low thermal conductivity and limited switching frequency.

Furthermore, manufacturing power devices using silicon carbide material sustain higher blocking voltage, thinner drift region thickness this means lower $R_{DS,ON}$, higher breakdown V_{BR} field strength and thermal conductivity was achieved. This is a clearer indication of an enhanced or increased performance efficiency levels and in terms of optimized semiconductor device designs.

Secondly, optimization into trench gate architecture for power MOSFETs and IGBTs rather than planar gate structure. This has unattainable advantages, for instance silicon carbide MOSFET with shielded fin - shaped gate structure. This means reduced gate - drain overlap, lower reverse transfer capacitance, lower gate charge and lower switching power losses. Shielded Fin - MOS is very effective in reducing electric field in the trench corner. Silvaco simulation comparison between conventional trench MOSFET, double trench MOSFET and shielded fin - MOSFET. All three structures have same n - drift layer thickness (7 μm) and doping ($7.5 \times 10^{15} cm^{-3}$), trench depth of (1 μm), gate oxide thickness of (50 nm), channel mobility ($11 cm^2/Vs$), channel length of (0.4 μm) and doping concentration of JFET region in shielded fin - MOSFET is ($2 \times 10^{16} cm^{-3}$). The electric field contours as well as peak positions and values for V_{GS} = -5V, V_{DS} = 600V. The electric field in the trench corner for conventional trench MOSFET (E = 5.87 MV/cm), the electric field in the trench corner for double trench MOSFET (E = 3.21 MV/cm), and the electric field in the trench corner for shielded fin - MOSFET (E = 2.55 MV/cm). Therefore, the simulation result indicates that shielded fin - MOSFET is the optimized structure to reduce electric field at the trench corner.

Appendices

MATLAB Code One

```
% The specific on-resistance contributed by the drift region
% in the power Trench or U-MOSFET SiC 1.2KV structure %

%clear;clc;close all;
clear all;

L_ch = 0.9e-4;              %
%       L_ch is channel length (cm)
u_fe = 20;                  %
%       Field-effect mobility (cm2/Vs)
u_d = 1000;                 %
%       Drift Region Mobility (cm2/Vs)
t_ox = 50e-7;               %
%       Oxide Thickness (cm)
rho_c = 1e-5;               %
%       rho_c is contact to source resistivity (ohm.cm2)
rho_sqn = 1500;             %
%       rho_sqn is source region resistivity (ohm.cm2)
rho_d = 0.60;               %
% rho_d is resistivity of (Silicon)
% the drift region in ohm square centi-meter(ohm.cm2)
rho_sub = 0.02;             %
%       rho_sub is substrate resistivity (ohm.cm2)
t_sub = 350e-4;             %
%       t_sub is substrate thickness (cm)
t_d = 10e-4;                %
%       t_d is tickness of the drift region in centi-meter(cm)
t_T = 1e-4;                 %
%       t_T is trench gate thickness in centi-meter (cm)
X_jp = 0.5e-4;              %
%       X_jp is P-base junction depth in centi-meter (cm)
W_c = 0.5e-4;               %
%       W_c is contact width in centi-meter (cm)
```

```
W_s = 1.5e-6;                %
%        W_s is source width in centi-meter (cm)
W_t = 1e-4;                  %
%        W_t is trench width in centi-meter (cm)
W_m = 4e-4;                  %
%
        W_m is mesa width in centi-meter (cm)
W_g = 1.5e-4;                %
%        W_g is gate width in centi-meter (cm)
W_cell = 20e-4;              %
%        W_cell is width of the cell pitch in centi meter(cm)
L_n = 1.5e-4;                %
%        L_n is length of the N+ well (cm)
a = 2e-4;                    %
%        'a' is width of the trench under gate in centi meter (cm)
b = W_m./2;                  %
%        'b' is the division of mesa width by 2
Z = 1e-4;                    %
%        'Z' is length of the gate in (micro meter)
u = 200e-4;                  %
%  'u' is the inversion layer electron mobility in
% (square centimeter per volt second)
c_ox = 6.903e-8;             %
% 'c' is the specific capacitance of the gate oxide
% (for tox oxide thickness 500A or 5*10^-8 meter) in (Farad)
V_th = 5;                    %
% 'v_th' is treshhold voltage in (Volt)
V_gs = 15;                   %
%        'V_gs' is gate to source voltage in (volts)
k_n = u*c_ox*Z;              %
% 'k_n' is channel length divided by the multiplication
% of electron mobility, capacitance and width
K = 0.6;                     %
%        'k_a' is a constant
m = 4e-4;                                    %
%   Gate length. This is a guess not given by Matocha (cm)
L_G = [0e-4:0.05e-4:12e-4];                  %
```

```
%    Variation in spacing m see Kevin Matocha TB (cm)
W_cell = L_G+(2.*m);                    %
%    Cell pitch (cm)



%%% Source to contact Resistance R_cs %%%

R_cs = ((rho_c .* W_cell) .* (1 ./ (W_c - W_s)));

%%% Source Region Resistance R_N+ %%%

R_sn = ((rho_sqn .* L_n .* W_cell) .* (0.5));


%%% Chanel Resistance %%%

R_ch = L_ch.*(W_cell./2).*(1./(u_fe.*c_ox.*(V_gs - V_th)));

%%% Accumulation Resistance R_A %%%

R_acc = ((K) .* (W_g - (2.*X_jp)) .*
% (W_cell./4).*(1./(u_fe.*c_ox.*(V_gs - V_th))));

%%% Drift region Resistance %%%

R_d = (((rho_d*W_cell)./2) .*

% (log((W_t + W_m) ./ (W_t)))) +

%(rho_d.*((t_d) + (X_jp) - (t_T) - (b)));

%%% Substrate Resistance R_subs %%%

R_subs = (rho_sub .* t_sub);
```

```
%%% Drain Contact Resistance R_CD %%%

R_cd = rho_c;



%%%% Internal resistance calculations for %
%trench MOSFET Total resistivity R_total %%%%

R_T = R_cs + R_sn + R_ch + R_acc + R_d + R_subs + R_cd;

%%%%%%%%% Plot Figure %%%%%%%%%%%%%%



figure

semilogy(W_cell*1e4, R_acc, 'r', W_cell*1e4, R_cs, 'g', W_cell*1e4,

%%R_sn, 'blue', W_cell*1e4, R_ch, 'yellow', W_cell*1e4, R_d, 'cyan',

%%W_cell*1e4, R_subs, 'black', W_cell*1e4, R_cd, 'black',

%% W_cell*1e4, %R_T, 'black');


%semilogy(W_cell*1e4, R_acc, 'kx-', W_cell*1e4, R_cs, 'kp-',

%%W_cell*1e4, R_sn, 'bo-', W_cell*1e4, R_ch, 'rs-', W_cell*1e4, R_d,

%%'ro-', W_cell*1e4, R_subs, 'kd-', W_cell*1e4, R_cd, 'kv',

%%W_cell*1e4, R_T, 'rd-');
```

```
%%ylim([1e-5 1e-1])


grid on
title('Specific on-resistance vs Cellpitch')

%%legend('R Acc', 'R Source', 'R Channel', 'R Drift',

%%'R Drain Contact', 'R Substrate', 'R Source Contact', 'R TOTAL')

%xlabel('Cellpitch, (um)')
%ylabel('Specific on-resistance, (mohm-cm2)')
```

MATLAB Code Two

```
        clear;
%%%%%% 1.2KV, 20A, SiC D - MOS total on-state

%resistance calculation %%%

        L_ch = 0.9e-4;
        %   Channel Length (cm)
        u_fe = 20;
        %   Field-effect mobility (cm2/Vs)
        N_d = 1e16;
        %   Drift Layer Doping conc (cm-3)
        t = 100e-4;
        %   Drift layer thickness (cm)
        r_j = 0.7e-4;
        %   Junction Radius of curvature (cm)
        L_nsource = 1.5e-4;
        %   Source Width (cm)
        rho_source = 1500;
        %   Source sheet resistance (ohm/sq)
        t_ox = 50e-7;
        %   Oxide Thickness (cm)
        V_G = 15;
        %   Gate Voltage (V)
```

```
        V_T = 5;
        %   Threshold Voltage (V)
        rho_c = 1e-5;
        %   Contact resistivity (ohm.cm2)
        K = 0.6;
        %   Accumulation layer spreading factor (no units)
        t_subs = 350e-4;
        %   Sustrate thickness (cm)
        rho_subs = 0.02;
        %   Substrate Resistivity (ohm.cm)
        u_d = 1000;
        %   Drift Region Mobility (cm2/Vs)
        x_j = 0.5e-4;
        %   p-base depth. This is a guess not given by %Matocha (cm)
        N_a = 1e17;
%   p-base doping conc. This is a guess not given by

% Matocha (cm-3)
        m = 4e-4;
        %Gate length.This is a guess not given by Matocha (cm)
        u_acc = 1000;
%   Accumulation mobility.This is a guess not given

% by Matocha (cm2/Vs)
        L_G = [0e-4:0.05e-4:12e-4];
        %  Variation in spacing m see Kevin Matocha TB (cm)
        %cellpitch = L_G+(2.*m); %   Cell pitch (cm)

%%%%Universal Constants%%%%%
        q = 1.602e-19;
        %   Electron charge (C)
        BOLTZ = 1.38e-23;
%   Boltzmann Constant 1.38e-23 J/K (kg.m2 s-1) or

% 8.6174e-5 eV/K
        T = 300;
        %   Temperature (K)
```

```
ni = 2e-10;
%   Initrinsic Carrier Conc. @ 300K (cm-3)
eps = 9.7*8.85e-14;
%   Semiconductor dielectric constant (m-3 kg-1 s4 A2)
e_ox=3.9*8.85e-14;
%   oxide permitivitty (m-3 kg-1 s4 A2)




V_bi = ((BOLTZ*T)/q)*log((N_a*N_d)/ni^2);
%   Built in potential (V)
%W_dep = sqrt((2*eps*N_a*V_bi)/(q*N_d*(N_a+N_d)));    %
p-well/n-drift depletion width at zero bias (cm)

rho_d = 1/(q*N_d*u_d);
%   Drift Layer Resistivity (ohm.cm)
c_ox=e_ox/t_ox;
%   Oxide Capacitance (F)
L_T = sqrt(rho_c/rho_source);
%   Transfer Length (cm)



%%%%%%      Drain Contact Resistivity %%%%%%

R_cdrain = rho_c;
R_cdrain=repmat(R_cdrain,1,241);

%%%%%%      Substrate Resistivity %%%%%%

R_subs = rho_subs*t_subs;
R_subs=repmat(R_subs,1,241);

%%%%%%      JFET Resistivity %%%%%%
c=(cellpitch -(2.*m));
%R_jfet = (rho_d.*(cellpitch./2)).*
%((x_j+W_dep)./((L_G./2)-x_j-W_dep));
```

```
%%%%%%     Drift Resistivity %%%%%%%
%b=log((cellpitch)./(rho_d.*(t-m-x_j-W_dep)));
%R_drift =
%(rho_d.*(cellpitch./2)).*
%log((cellpitch)./(L_G-(2.*x_j)-(2.*W_dep)))+
%(rho_d.*(t-m-x_j-W_dep));

%%%%%%     Accumulation Resistivity %%%%%%%

%R_acc = K.*(cellpitch./2).*
%((L_G/2)-x_j).*(1./(u_acc.*c_ox.*(V_G-V_T)));

%%%%%%     Channel Resistivity %%%%%%%

%R_ch = L_ch.*(cellpitch./2).*
%(1./(u_fe.*c_ox.*(V_G-V_T)));

%%%%%%     Source Resistivity %%%%%%%

R_s = rho_source.*L_nsource.*(cellpitch./2);

%%%%%%     Source Contact Resistivity %%%%%%%

R_sc = (rho_c./L_T).*(cellpitch./2);

%%%%%Sort Array to start from a reasonable

% position %%%%%%

for i=1:numel(R_jfet)
if R_jfet(i)<0
k=i+1;
end
end
%k
R_cdrain=(R_cdrain(k:end));
```

```
        R_subs=(R_subs(k:end));
        R_jfet=(R_jfet(k:end));
        R_drift=(R_drift(k:end));
        R_acc=(R_acc(k:end));
        R_ch=(R_ch(k:end));
        R_s=(R_s(k:end));
        R_sc=(R_sc(k:end));
        cellpitch=(cellpitch(k:end));


        %%%%%%      Total Resistivity %%%%%%%

        R_T = R_cdrain+R_subs+R_drift+R_acc+R_ch+R_s+R_sc+R_jfet;

        %%%%%       Plot Figure       %%%%%%%%%

        cellpitch=cellpitch*1e4;

        origin=[cellpitch',R_T',R_jfet',R_drift',R_ch',R_subs

%,R_acc',R_s',R_sc',R_cdrain'];

% assign variable origin to data columns for all

%parameter arrays

        csvwrite('1.2KV_20A_SiC_DMOS_TotalResistance.csv',origin);


        figure

semilogy(cellpitch,R_acc,'k',cellpitch,R_s,'y',cellpit

% ch,R_jfet,'r',cellpitch,R_ch,'g',cellpitch,R_drift,'b'

%,cellpitch,R_cdrain,'magenta',cellpitch,R_subs,'cyan',
```

```
% cellpitch,R_sc,'b',cellpitch,R_T,'O-')

        %xlim([10 20])
        %ylim([0 300])
% grid on
% legend('R acc','R sn','R_JFET','R ch','R d','Rcd',

%'R sub','R sc','R TOTAL')
        title('Specific On-Resistance vs Cellpitch')
        xlabel('Cellpitch (um)')
        ylabel('Specific on-resistance (mohm-cm2)')
```

MATLAB Code Three

```
%%%%% Threshold voltage vs Oxide thickness %%%%%
clear;clc;close all;

N_a = logspace(19,21,3);          %
%   Doping concentration in the semiconductor (m-3)
for i=1:length(N_a)
CTV(N_a(i));
end
function [CTV]=CTV(N_A)
%%% Universal Constants %%%
K = 1.38e-23;            %% Boltzmann Constant
T = 300;                 %% Temperature (K)
ni = 2e-10;              %% Intrinsic Carrier Constant (m-3)
e_s = 9.7*8.85e-14;      %
% Semiconductor dielectric constant (m-3 Kg-1 S4 A2)
e_ox = 3.9*8.85e-14 ;    %% Oxide permitivity (m-3 Kg-1 S4 A2)
%%% Sweep t_ox from 1e2 to 1e4 %%%
%t_ox = linespace(0, t_ox, 10);
t_ox = 1e-8:1e-8:1e-6;
%%% Threshold Voltage V_T %%%
V_T = ((t_ox / e_ox) .*
%(sqrt(4 .* e_s .* K .* T .* N_A .* (log(N_A / ni)))));
```

```
%k

%V_T  = (V_T(k:end));

%

%figure
%semilogy(t_ox*1e4, V_T);
%ylim([1e-5 1e-1])
hold on
grid on
semilogx(t_ox, V_T, 'b')
xlabel ('Oxide thickness, (meters)')
ylabel ('Threshold Voltage, (Volts)')
title ('Threshold voltage for silicon MOS structures')
set(gca, 'XScale', 'log')
axis([1e-8 1e-6 0 10])
end
```

Company Datasheet one

N–channel 200V – 0.038 Ω – 40A Power MOSFET

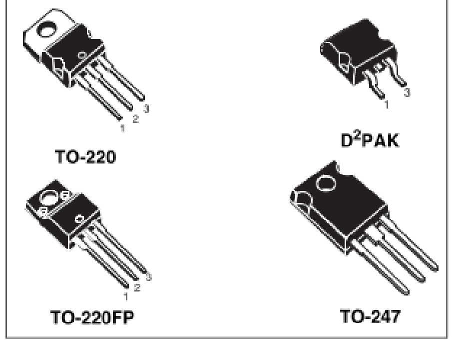
STP40NF20 - STF40NF20
STB40NF20 - STW40NF20

N-channel 200V - 0.038Ω -40A- D^2PAK/TO-220/TO-220FP/TO-247
Low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STB40NF20	200V	<0.045Ω	40A	160W
STP40NF20	200V	<0.045Ω	40A	160W
STF40NF20	200V	<0.045Ω	40A	40W
STW40NF20	200V	<0.045Ω	40A	160W

- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Excellent figure of merit (R_{DS}*Q_g)
- 100% avalanche tested



Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

Applications

- Switching application

Figure 1. Internal schematic diagram

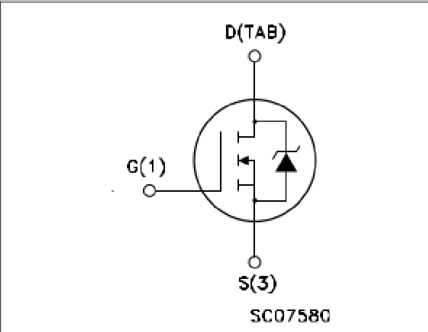


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB40NF20	40NF20	D^2PAK	Tape & reel
STP40NF20	40NF20	TO-220	Tube
STF40NF20	40NF20	TO-220FP	Tube
STW40NF20	40NF20	TO-247	Tube

Figure 89: Company Datasheet Power MOSFET 200 V, 40A

STB40NF20 - STF40NF20 - STP40NF20 - STW40NF20 Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 D^2PAK TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	200		V
V_{GS}	Gate- source voltage	± 20		V
I_D (1)	Drain current (continuous) at T_C = 25°C	40		A
I_D (1)	Drain current (continuous) at T_C = 100°C	25		A
I_{DM} (2)	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at T_C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
dv/dt (3)	Peak diode recovery voltage slope	12		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; Tc = 25°C)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature			

1. Value limited by wire bonding
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 40A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $Tj \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	TO-220 D^2PAK	TO-247	TO-220FP	Unit
Rthj-case	Thermal resistance junction-case max	0.78		3.1	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose (1)	300			°C

1. for 10 sec. 1.6mm from case

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	40	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	230	mJ

Figure 90: Company Electrical ratings of power MOSFET 200 V, 40A

Electrical characteristics STB40NF20 - STF40NF20 - STP40NF20 - STW40NF20

2 Electical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} =0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings@125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 20A		0.038	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 20A		30		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		2500 510 78		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 100V, I_D = 20A R_G = 4.7Ω V_{GS} = 10V (see *Figure 17*)		20 44 74 22		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160V, I_D = 40A, V_{GS} = 10V (see *Figure 18*)		75 13.2 35.5		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Figure 91: Datasheet Electrical characteristics of power MOSFET 200 V, 40A

STB40NF20 - STF40NF20 - STP40NF20 - STW40NF20 Electrical characteristics

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				40 160	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 20A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 20A, di/dt = 100A/µs, V_{DD} = 25V (see *Figure 19*)		192 922 9.6		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 20A, di/dt = 100A/µs, V_{DD} = 25V, T_j = 150°C (see *Figure 19*)		242 1440 11.9		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Figure 92: Datasheet source drain diode of power MOSFET 200 V, 40A

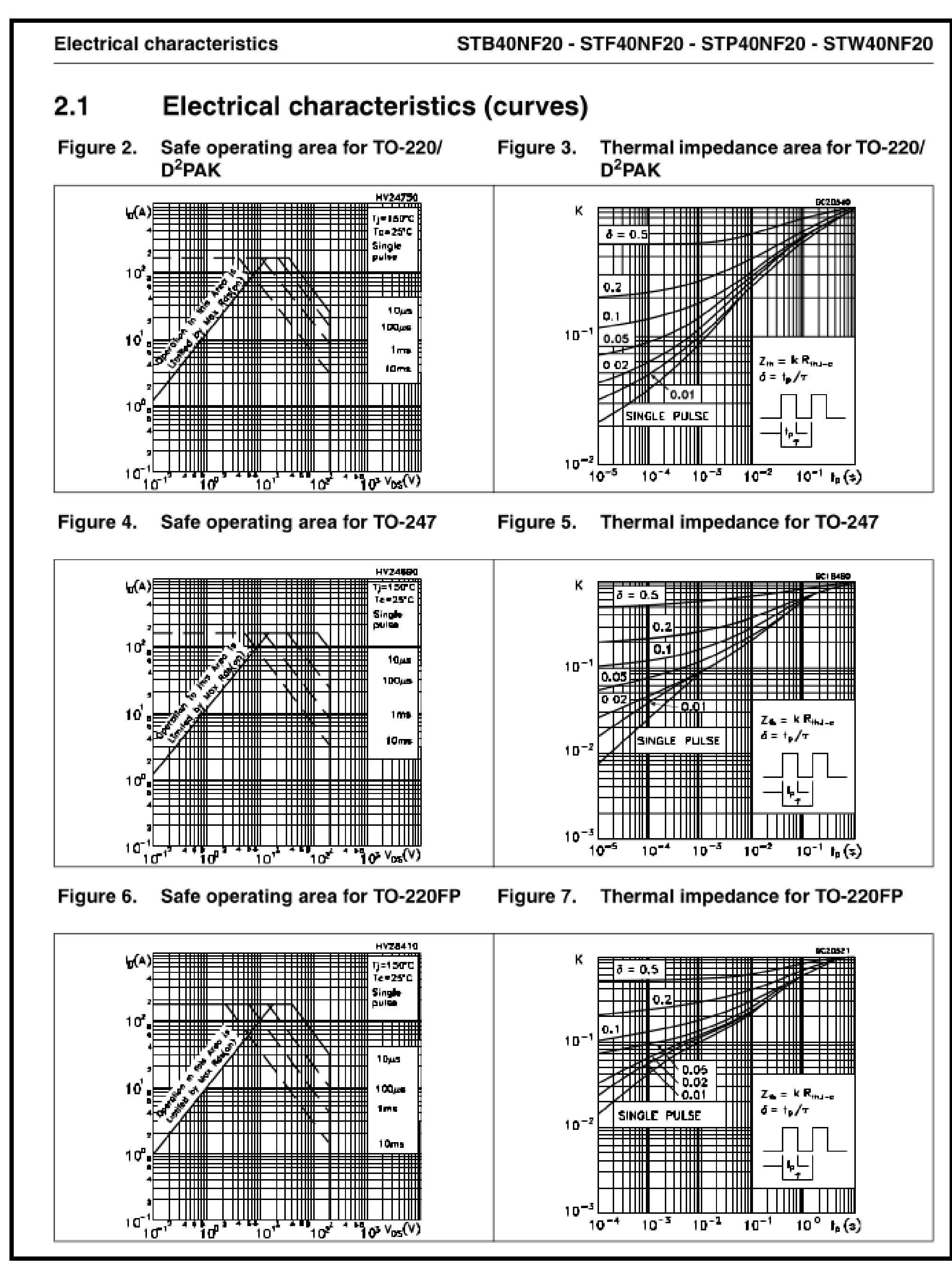


Figure 93: Datasheet Electrical curves of power MOSFET 200 V, 40A

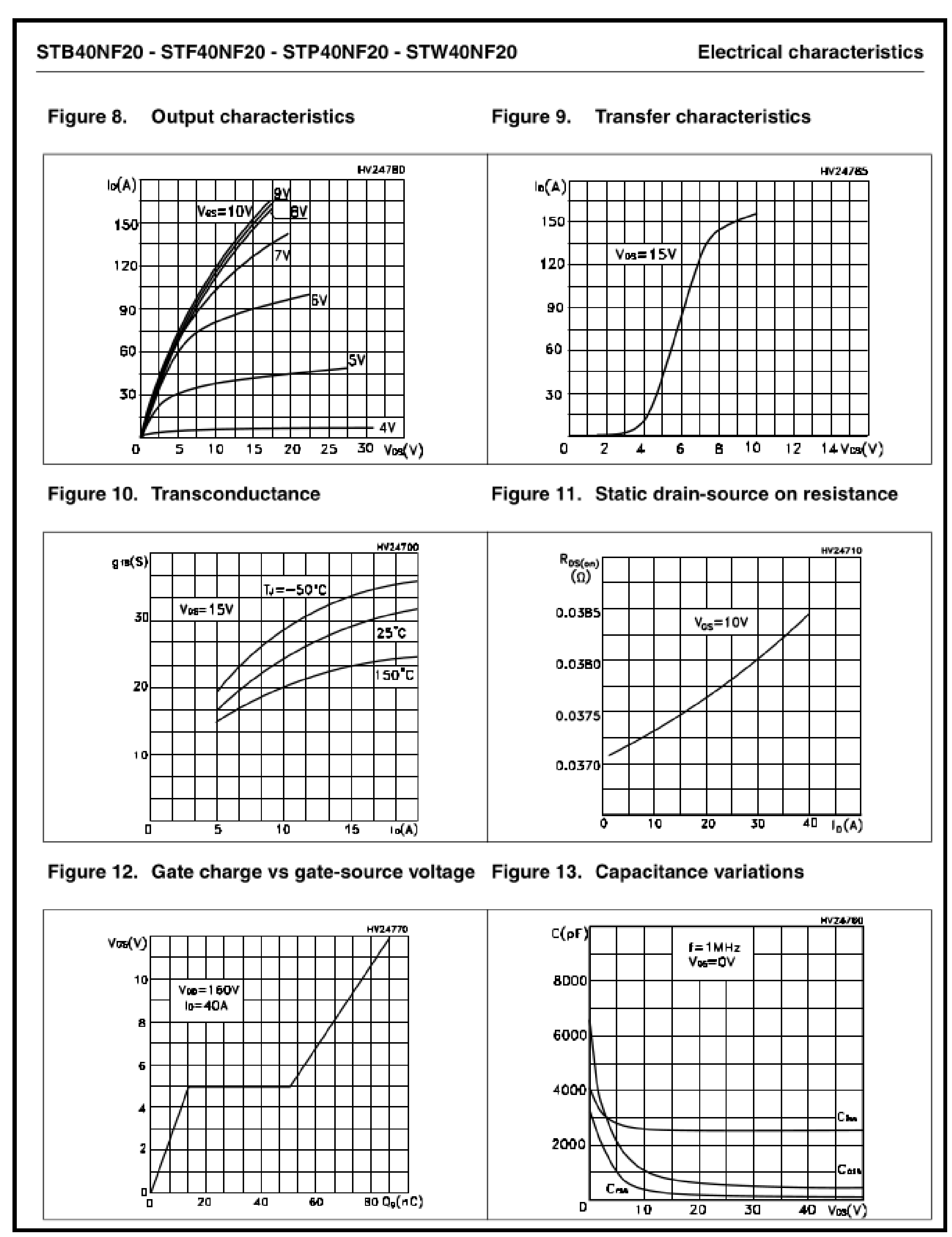
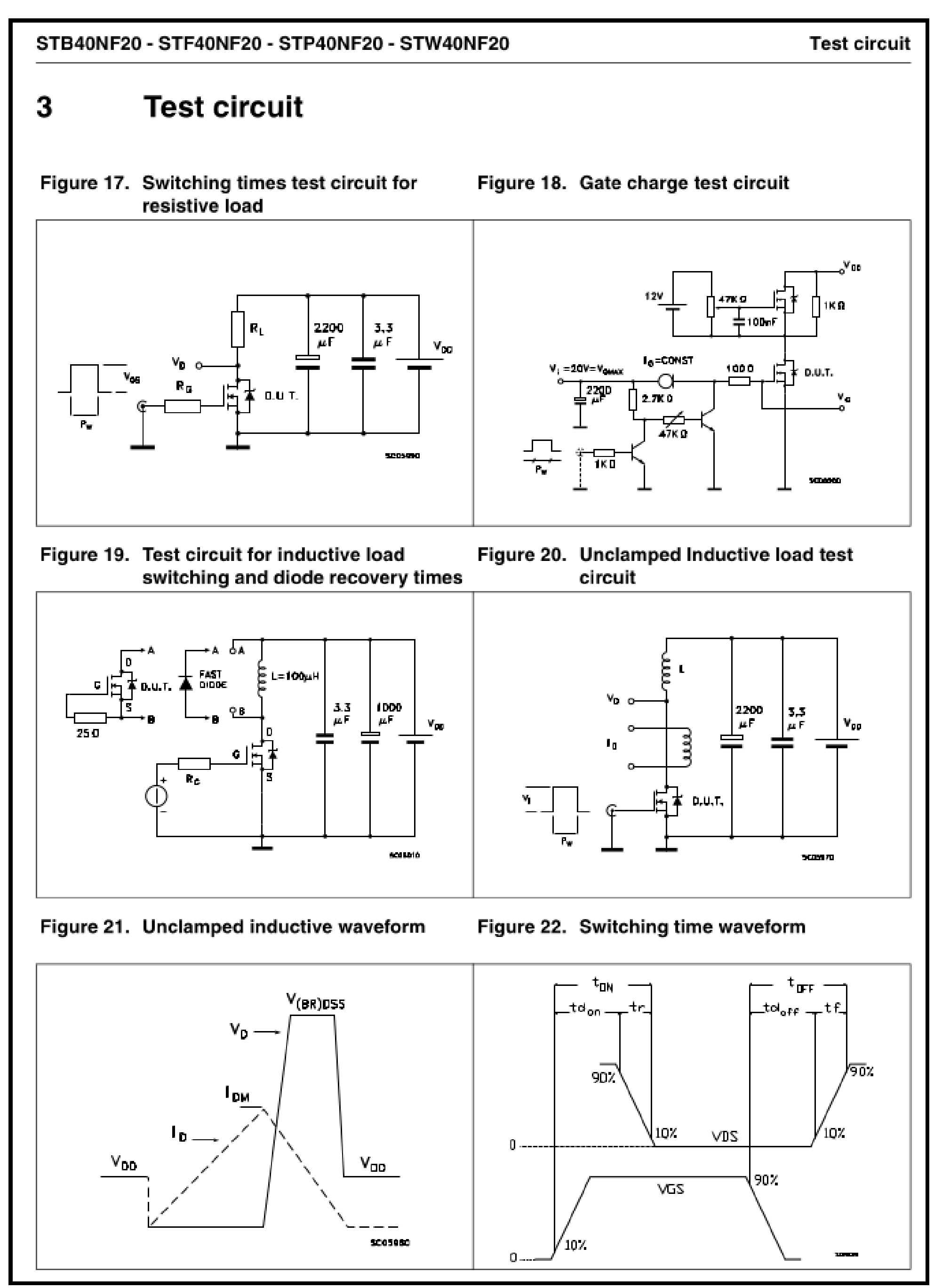


Figure 94: Datasheet output characteristics of power MOSFET 200 V, 40A


STB40NF20 - STF40NF20 - STP40NF20 - STW40NF20 Test circuit

3 Test circuit

Figure 17. Switching times test circuit for resistive load

Figure 18. Gate charge test circuit

Figure 19. Test circuit for inductive load switching and diode recovery times

Figure 20. Unclamped Inductive load test circuit

Figure 21. Unclamped inductive waveform

Figure 22. Switching time waveform

Figure 95: Datasheet test circuit of power MOSFET 200 V, 40A

Company Datasheet two

CoolSiC 1200V, 19A, Silicon Carbide Trench MOSFET

IMZ120R140M1H

IMZ120R140M1H

CoolSiC™ 1200V SiC Trench MOSFET
Silicon Carbide MOSFET

Features

- Very low switching losses
- Threshold-free on state characteristic
- Benchmark gate threshold voltage, $V_{GS(th)} = 4.5V$
- 0V turn-off gate voltage for easy and simple gate drive
- Fully controllable dV/dt
- Robust body diode for hard commutation
- Temperature independent turn-off switching losses
- Sense pin for optimized switching performance

Benefits

- Efficiency improvement
- Enabling higher frequency
- Increased power density
- Cooling effort reduction
- Reduction of system complexity and cost

Potential applications

- Energy generation
  - Solar string inverter and solar optimizer
- Industrial power supplies
  - Industrial UPS
  - Industrial SMPS
- Infrastructure – Charge
  - Charger

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC 47/20/22

Note: *the source and sense pins are not exchangeable, their exchange might lead to malfunction*

Table 1 **Key Performance and Package Parameters**

Type	V_{DS}	I_D ($T_C = 25°C$, $R_{th(j-c,max)}$)	$R_{DS(on)}$ ($T_{vj} = 25°C$, $I_D = 6A$, $V_{GS} = 18V$)	$T_{j,max}$	Marking	Package
IMZ120R140M1H	1200V	19A	140mΩ	175°C	12M1H140	PG-TO247-4

Figure 96: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

IMZ120R140M1H

Maximum ratings

1 Maximum ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Value	Unit
Drain-source voltage, $T_{vj} \geq 25°C$	V_{DSS}	1200	V
DC drain current for $R_{th(j\text{-}c,max)}$, limited by T_{vjmax}, $V_{GS} = 18V$, $T_C = 25°C$ $T_C = 100°C$	I_D	 19 13	A
Pulsed drain current, t_p limited by T_{vjmax}, $V_{GS} = 18V$	$I_{D,pulse}$[1]		A
DC body diode forward current for $R_{th(j\text{-}c,max)}$, limited by T_{vjmax}, $V_{GS} = 0V$ $T_C = 25°C$ $T_C = 100°C$	I_{SD}	 21 12	A
Pulsed body diode current, t_p limited by T_{vjmax}	$I_{SD,pulse}$[1]	32	A
Gate-source voltage[2] Max transient voltage, < 1% duty cycle Recommend turn-on gate voltage Recommend turn-off gate voltage	 V_{GS} $V_{GS,on}$ $V_{GS,off}$	 -7… 23 15… 18 0	V
Power dissipation, limited by T_{vjmax} $T_C = 25°C$ $T_C = 100°C$	P_{tot}	 94 47	W
Virtual junction temperature	T_{vj}	-55… 175	°C
Storage temperature	T_{stg}	-55… 150	°C
Soldering temperature, wavesoldering only allowed at leads, 1.6mm (0.063 in.) from case for 10 s	T_{sold}	260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

Figure 97: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

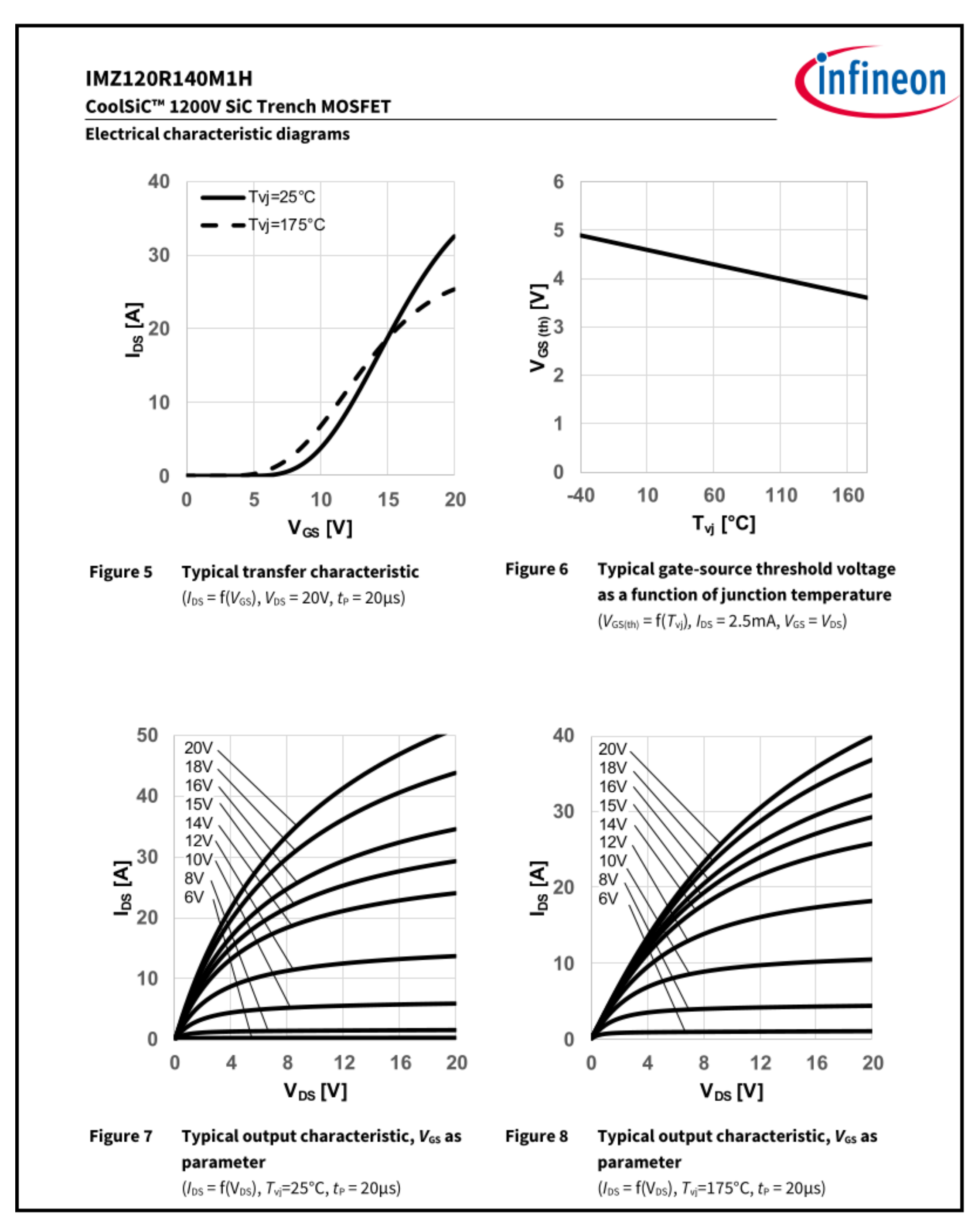


Figure 98: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

IMZ120R140M1H

CoolSiC™ 1200V SiC Trench MOSFET

Electrical Characteristics

3.2 Dynamic characteristics

Table 5 Dynamic characteristics (at T_{vj} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{DD} = 800V, V_{GS} = 0V, f = 1MHz, V_{AC} = 25mV	-	454	-	pF
Output capacitance	C_{oss}		-	25	-	
Reverse capacitance	C_{rss}		-	3	-	
C_{oss} stored energy	E_{oss}		-	9	-	µJ
Total gate charge	Q_G	V_{DD} = 800V, I_D = 6A, V_{GS} = 0/18V, turn-on pulse	-	13	-	nC
Gate to source charge	$Q_{GS,pl}$		-	4	-	
Gate to drain charge	Q_{GD}		-	3	-	
Short-circuit withstand time[3]	t_{SC}	V_{DD} = 800V, $L_σ$ = 80nH, $R_{G,ext}$ = 8Ohm, T_{vj} = 175°C $V_{GS.on}$ = 15V	-	3	-	µs

[3] Verified by design for single short circuit event at $V_{GS,on}$ = 15V.

Figure 99: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

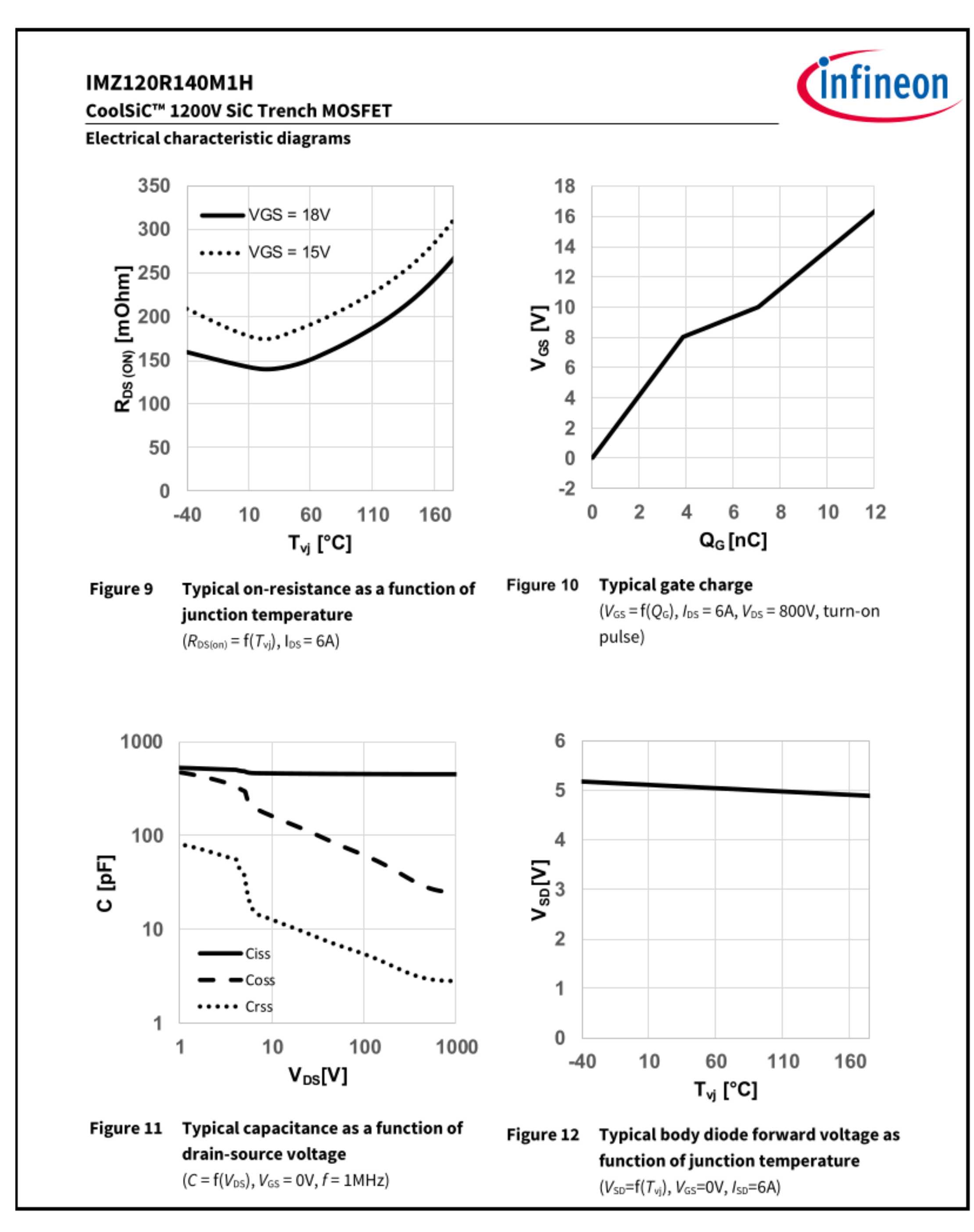


Figure 100: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

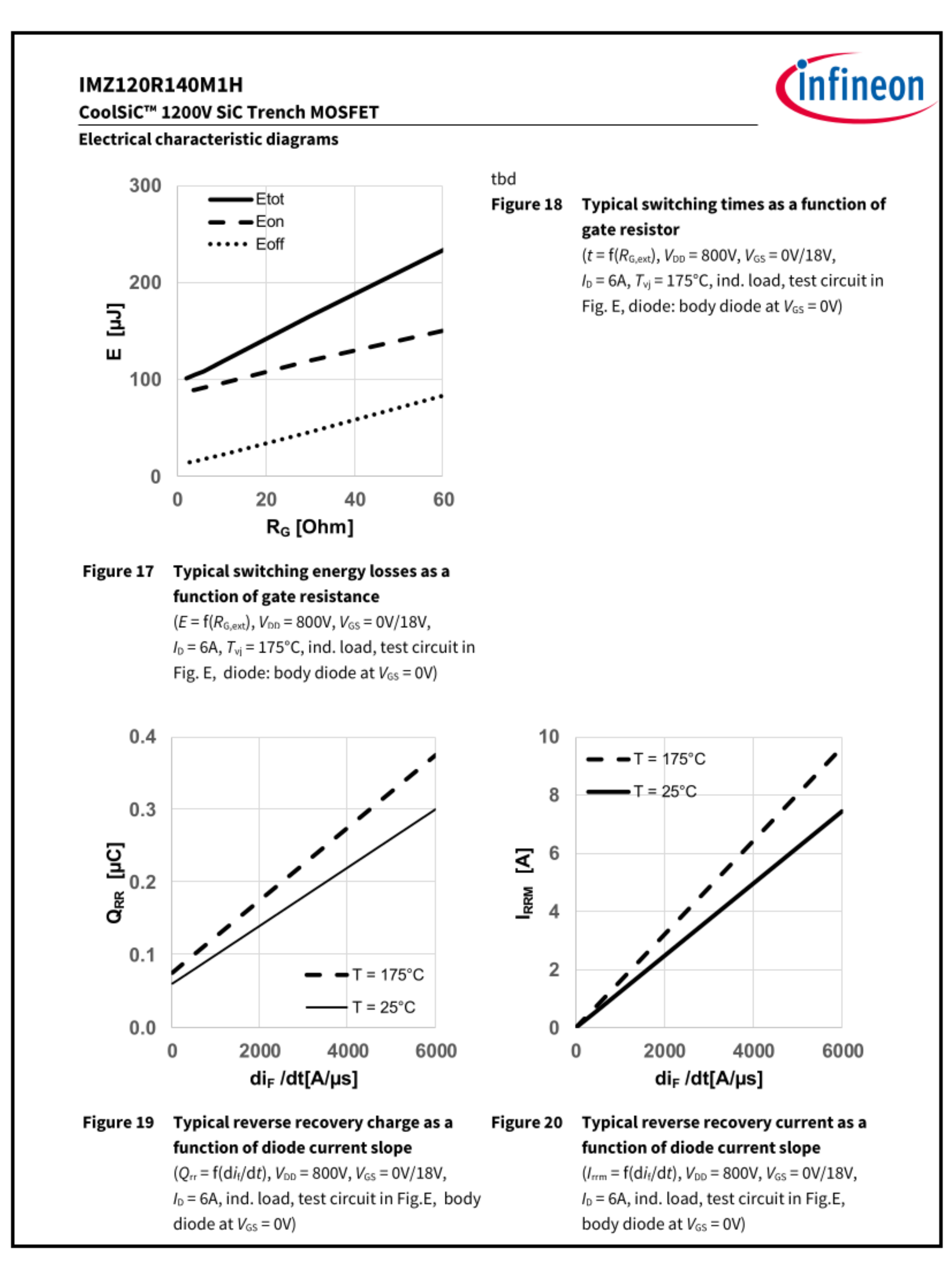


Figure 101: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

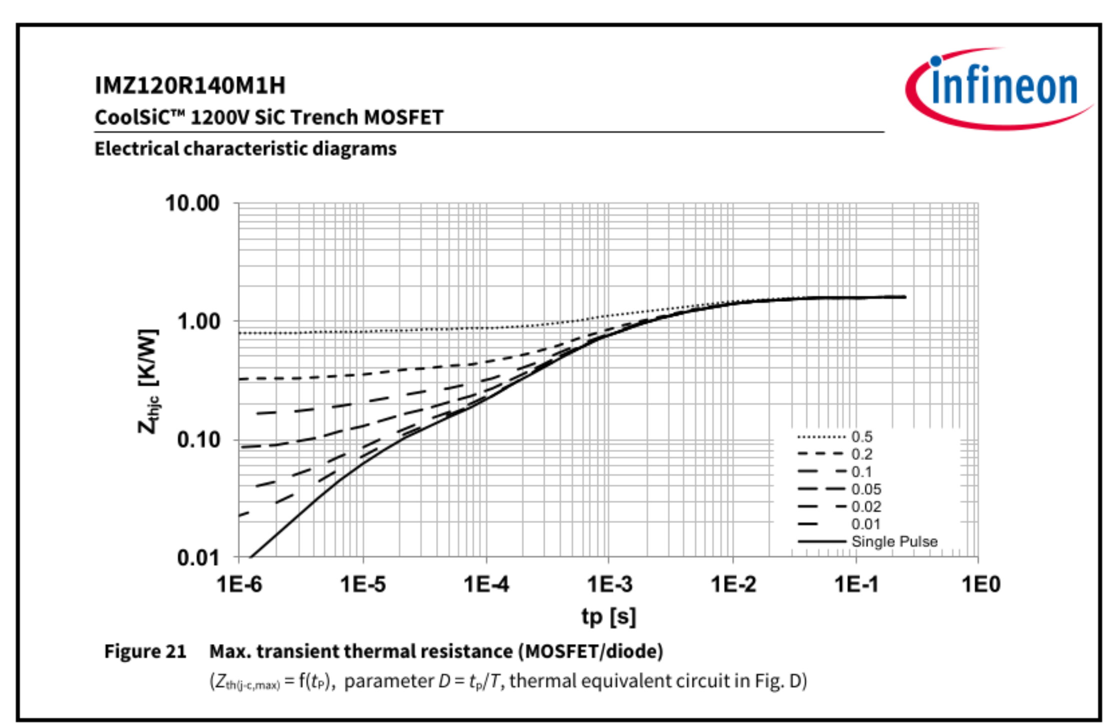
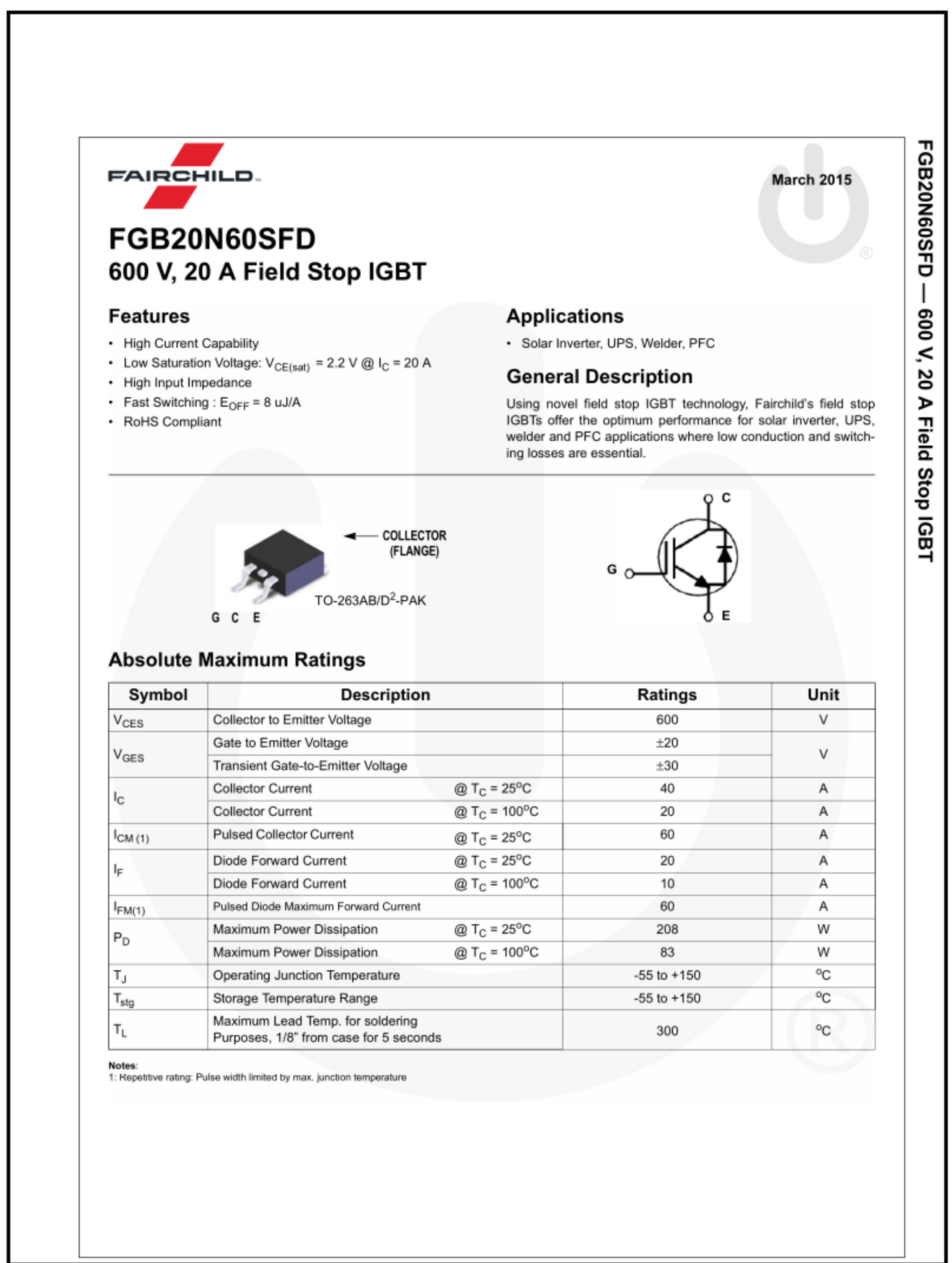


Figure 102: Datasheet CoolSiC 1.2KV, 19A Trench MOSFET

Company Datasheet three

Company datasheet for IGBT, n–channel fast with diode 600V, 20A, TO247.



FAIRCHILD

March 2015

FGB20N60SFD
600 V, 20 A Field Stop IGBT

FGB20N60SFD — 600 V, 20 A Field Stop IGBT

Features

- High Current Capability
- Low Saturation Voltage: $V_{CE(sat)}$ = 2.2 V @ I_C = 20 A
- High Input Impedance
- Fast Switching : E_{OFF} = 8 uJ/A
- RoHS Compliant

Applications

- Solar Inverter, UPS, Welder, PFC

General Description

Using novel field stop IGBT technology, Fairchild's field stop IGBTs offer the optimum performance for solar inverter, UPS, welder and PFC applications where low conduction and switching losses are essential.

Absolute Maximum Ratings

Symbol	Description		Ratings	Unit
V_{CES}	Collector to Emitter Voltage		600	V
V_{GES}	Gate to Emitter Voltage		±20	V
	Transient Gate-to-Emitter Voltage		±30	
I_C	Collector Current	@ T_C = 25°C	40	A
	Collector Current	@ T_C = 100°C	20	A
$I_{CM\ (1)}$	Pulsed Collector Current	@ T_C = 25°C	60	A
I_F	Diode Forward Current	@ T_C = 25°C	20	A
	Diode Forward Current	@ T_C = 100°C	10	A
$I_{FM(1)}$	Pulsed Diode Maximum Forward Current		60	A
P_D	Maximum Power Dissipation	@ T_C = 25°C	208	W
	Maximum Power Dissipation	@ T_C = 100°C	83	W
T_J	Operating Junction Temperature		-55 to +150	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temp. for soldering Purposes, 1/8" from case for 5 seconds		300	°C

Notes:
1: Repetitive rating: Pulse width limited by max. junction temperature

Figure 103: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

FGB20N60SFD — 600 V, 20 A Field Stop IGBT

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$(IGBT)	Thermal Resistance, Junction to Case	-	0.6	°C/W
$R_{\theta JC}$(Diode)	Thermal Resistance, Junction to Case	-	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (PCB Mount)(2)	-	40	°C/W

Notes:
2: Mounted on 1" square PCB (FR4 or G-10 material)

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FGB20N60SFD	FGB20N60SFD	D^2-PAK	Reel	13" Dia	N/A	800

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{CES}	Collector to Emitter Breakdown Voltage	V_{GE} = 0 V, I_C = 250 μA	600	-	-	V
$\Delta BV_{CES} / \Delta T_J$	Temperature Coefficient of Breakdown Voltage	V_{GE} = 0 V, I_C = 250 μA	-	0.6	-	V/°C
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0 V	-	-	250	μA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0 V	-	-	±400	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	I_C = 250 μA, $V_{CE} = V_{GE}$	4.0	5.0	6.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 20 A, V_{GE} = 15 V	-	2.2	2.8	V
		I_C = 20 A, V_{GE} = 15 V, T_C = 125°C	-	2.4	-	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30 V, V_{GE} = 0 V, f = 1 MHz	-	940	-	pF
C_{oes}	Output Capacitance		-	110	-	pF
C_{res}	Reverse Transfer Capacitance		-	40	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 400 V, I_C = 20 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 25°C	-	13	-	ns
t_r	Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	90	-	ns
t_f	Fall Time		-	24	48	ns
E_{on}	Turn-On Switching Loss		-	0.37	-	mJ
E_{off}	Turn-Off Switching Loss		-	0.16	-	mJ
E_{ts}	Total Switching Loss		-	0.53	-	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 400 V, I_C = 20 A, R_G = 10 Ω, V_{GE} = 15 V, Inductive Load, T_C = 125°C	-	12	-	ns
t_r	Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	95	-	ns
t_f	Fall Time		-	28	-	ns
E_{on}	Turn-On Switching Loss		-	0.4	-	mJ
E_{off}	Turn-Off Switching Loss		-	0.28	-	mJ
E_{ts}	Total Switching Loss		-	0.69	-	mJ

Figure 104: Datasheet silicon IGBT 600V, n-channel fast with diode 600V, 20A, TO247.

Electrical Characteristics of the IGBT T_C = 25°C unless otherwise noted

Q_g	Total Gate Charge	V_{CE} = 400 V, I_C = 20 A, V_{GE} = 15 V	-	65	-	nC
Q_{ge}	Gate to Emitter Charge		-	7	-	nC
Q_{gc}	Gate to Collector Charge		-	33	-	nC

Electrical Characteristics of the Diode T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max	Unit
V_{FM}	Diode Forward Voltage	I_F = 10 A	T_C = 25°C	-	1.9	2.5	V
			T_C = 125°C	-	1.7	-	
t_{rr}	Diode Reverse Recovery Time	I_F =10 A, di_F/dt = 200 A/μs	T_C = 25°C	-	34	-	ns
			T_C = 125°C	-	57	-	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	-	41	-	nC
			T_C = 125°C	-	96	-	

FGB20N60SFD — 600 V, 20 A Field Stop IGBT

Figure 105: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

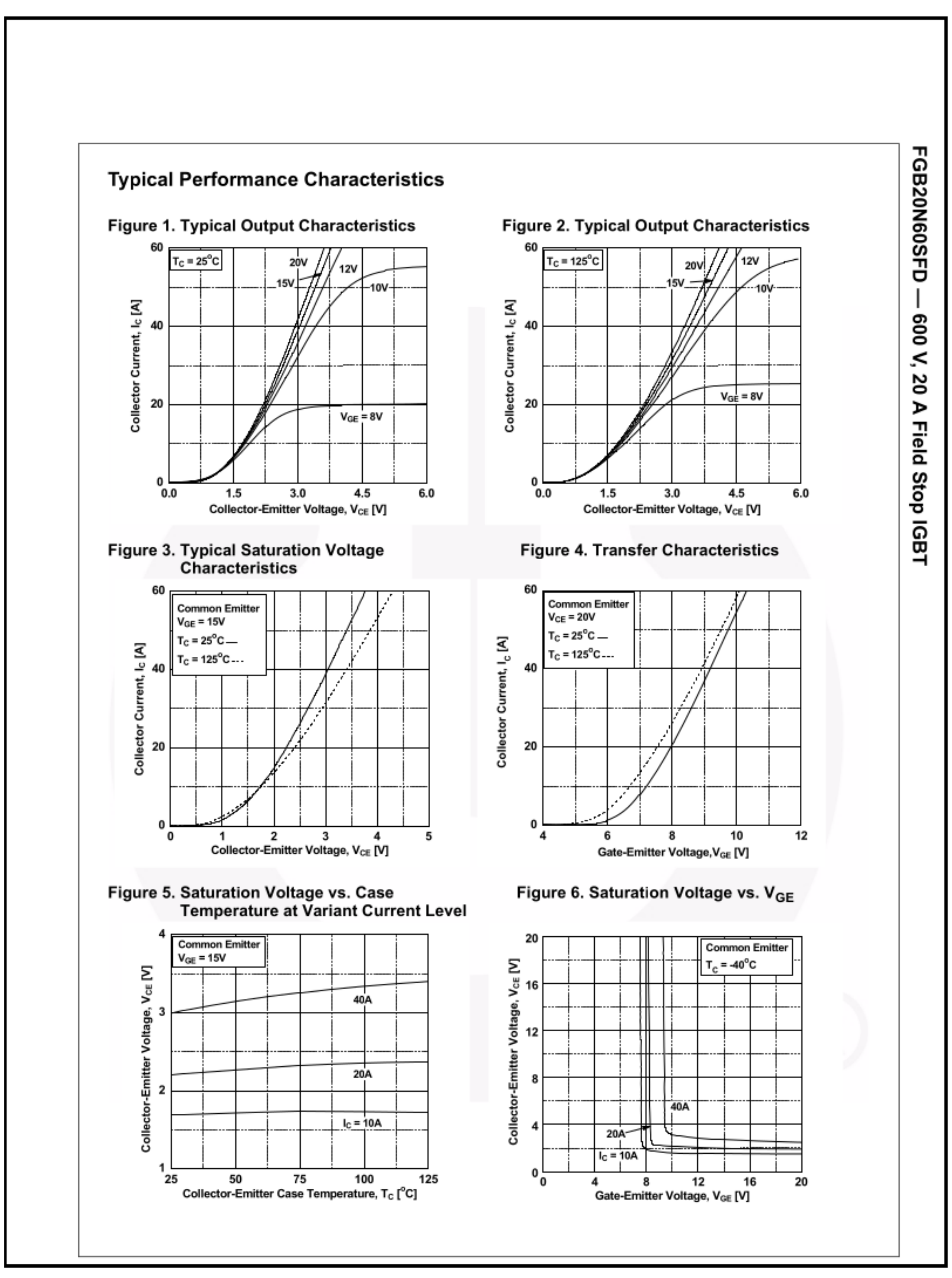


Figure 106: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

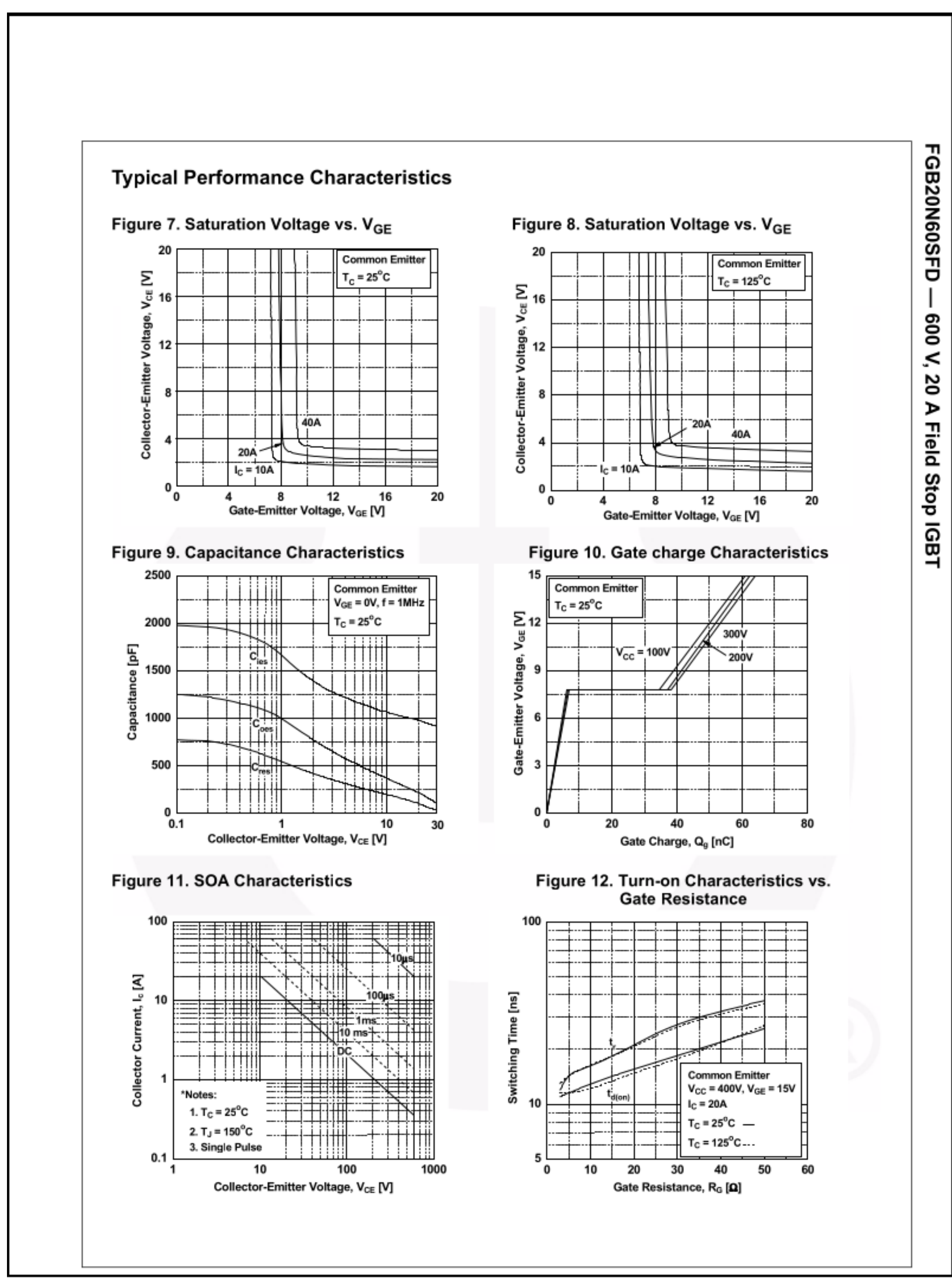


Figure 107: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

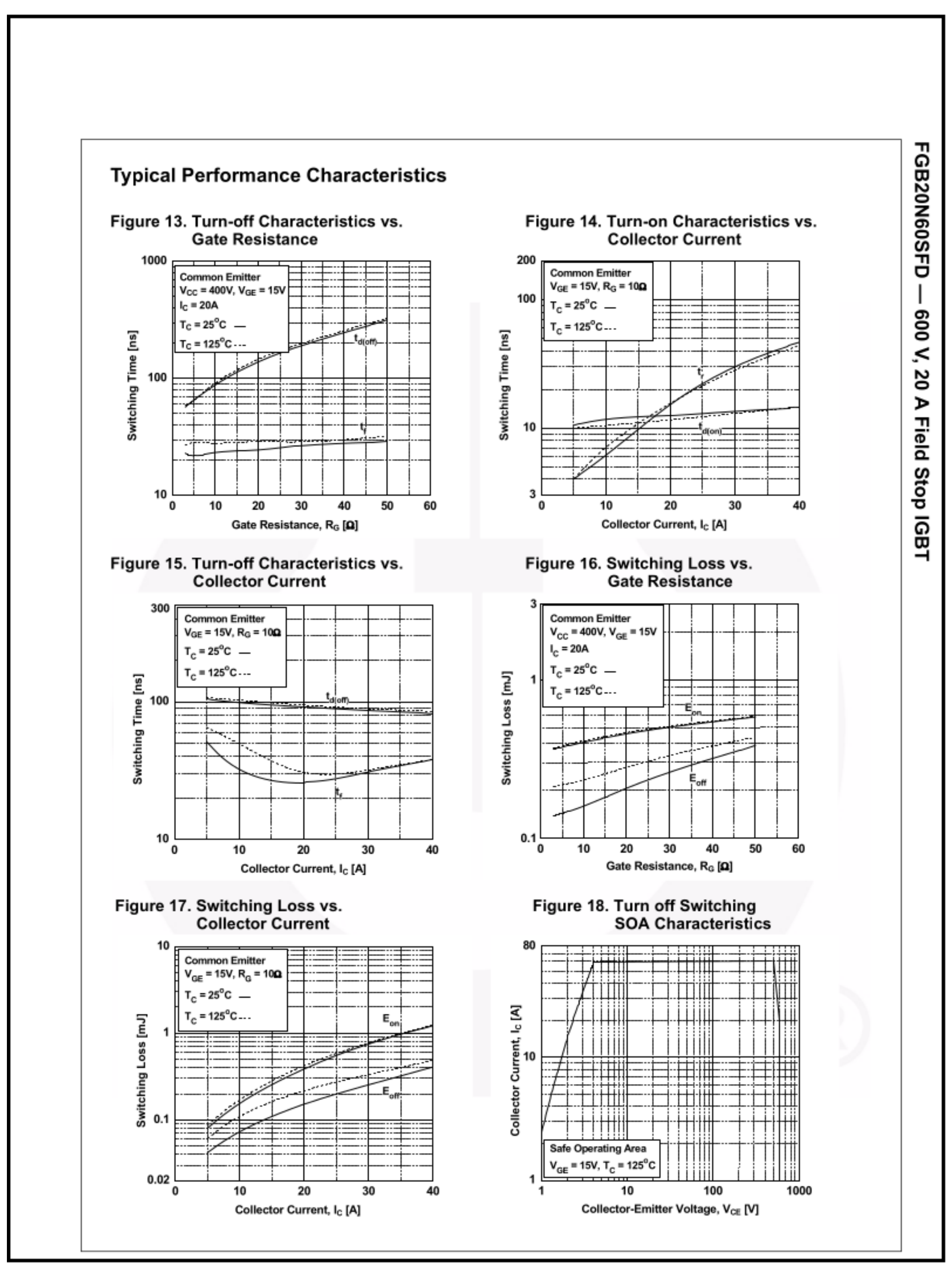


Figure 108: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

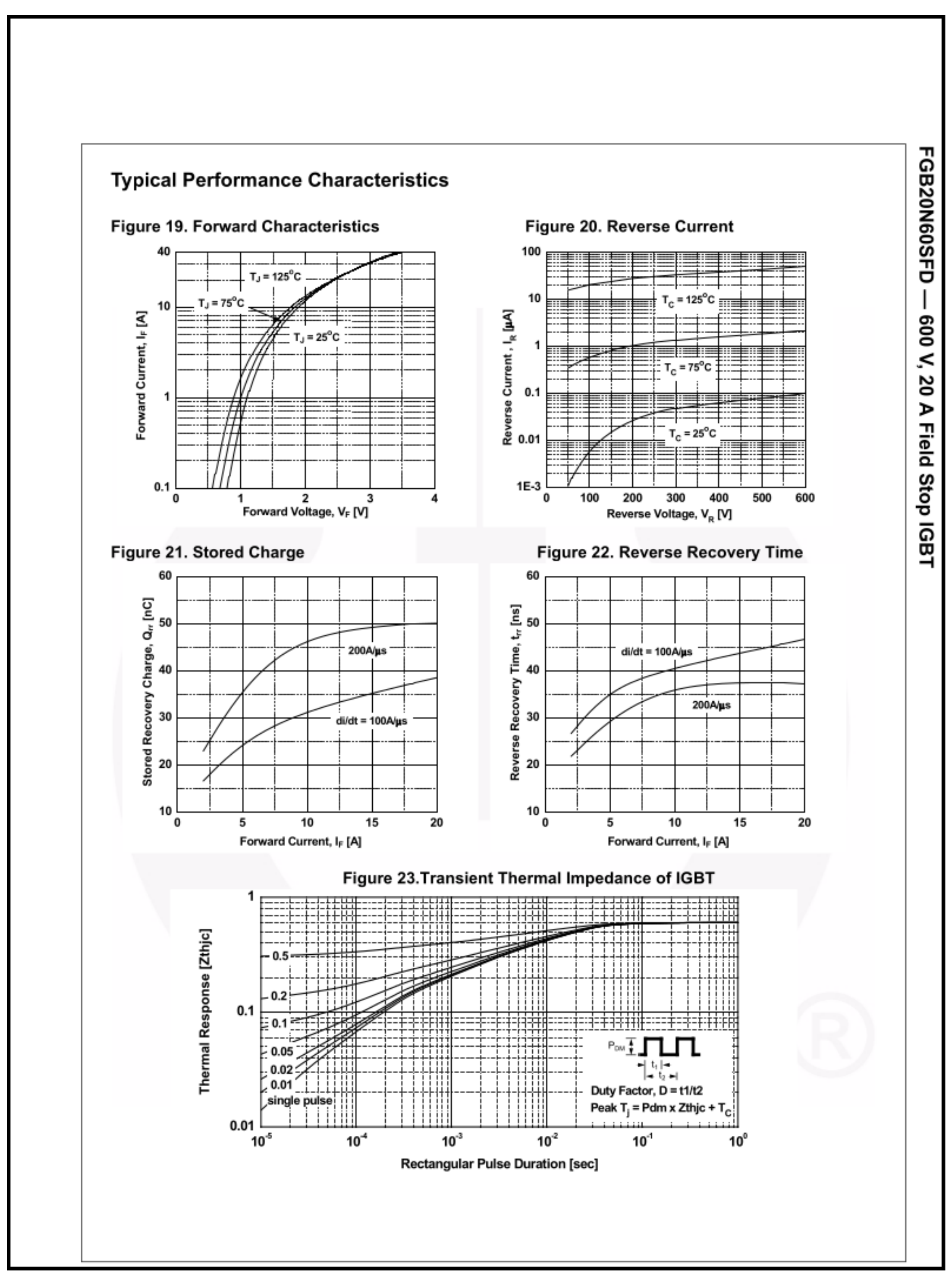
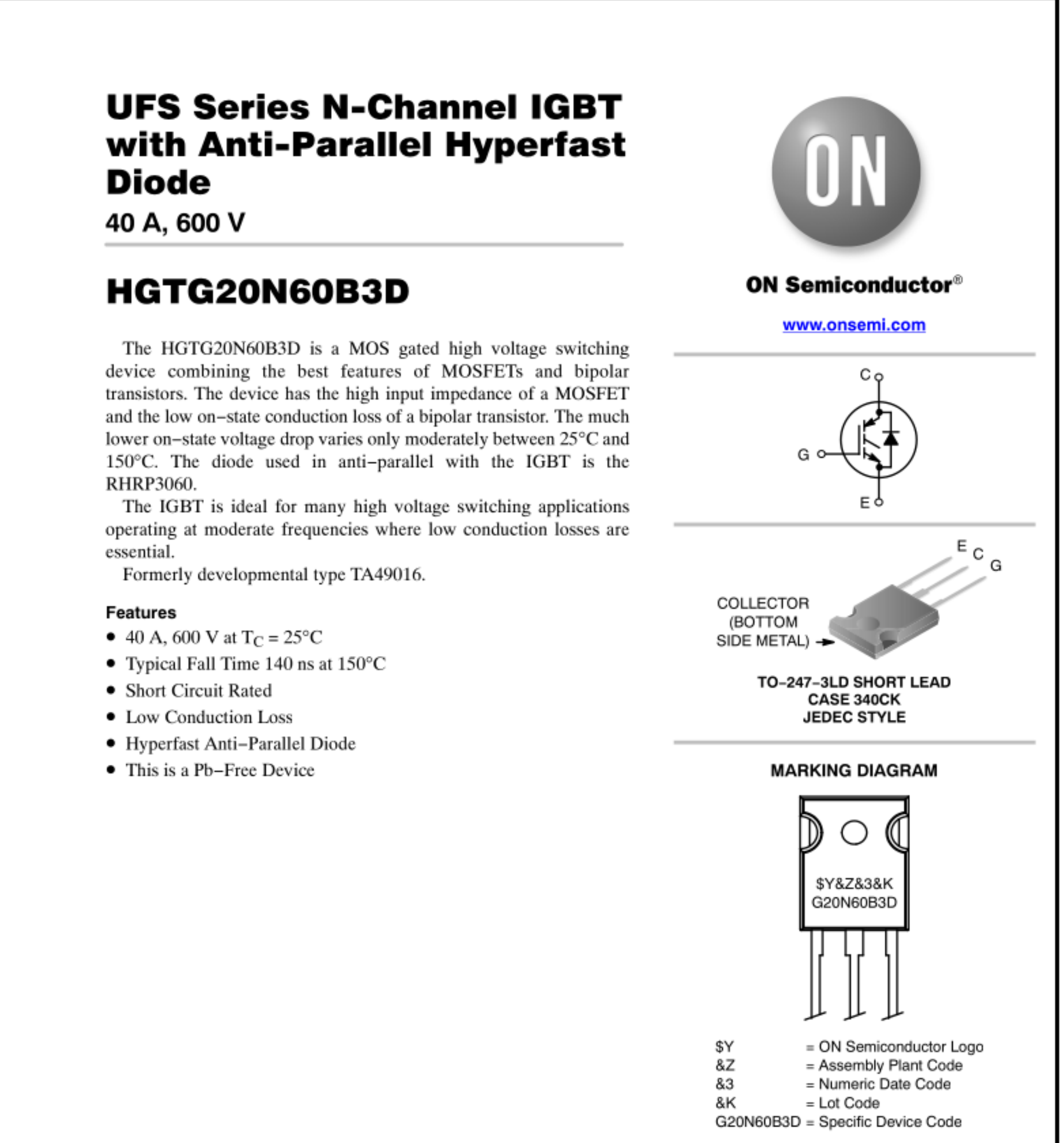


Figure 109: Datasheet silicon IGBT, n-channel fast with diode 600V, 20A, TO247.

Company Datasheet four

Company datasheet for IGBT, n–channel fast with diode 600V, 40A, TO247.



UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

40 A, 600 V

HGTG20N60B3D

The HGTG20N60B3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on–state conduction loss of a bipolar transistor. The much lower on–state voltage drop varies only moderately between 25°C and 150°C. The diode used in anti–parallel with the IGBT is the RHRP3060.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

Formerly developmental type TA49016.

Features

- 40 A, 600 V at T_C = 25°C
- Typical Fall Time 140 ns at 150°C
- Short Circuit Rated
- Low Conduction Loss
- Hyperfast Anti–Parallel Diode
- This is a Pb–Free Device

ON Semiconductor®

www.onsemi.com

TO–247–3LD SHORT LEAD CASE 340CK JEDEC STYLE

MARKING DIAGRAM

$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
G20N60B3D = Specific Device Code

Figure 110: Datasheet silicon IGBT 600V, 40A, TO-247

HGTG20N60B3D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

Parameter	Symbol	HGTG20N60B3D	Unit
Collector to Emitter Voltage	BV_{CES}	600	V
Collector to Gate Voltage, R_{GE} = 1 MΩ	BV_{CGR}	600	V
Collector Current Continuous At T_C = 25°C At T_C = 110°C	 I_{C25} I_{C110}	 40 20	 A A
Average Diode Forward Current at 110°C	$I_{(AVG)}$	20	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_C = 150°C	SSOA	30 A at 600 V	
Power Dissipation Total at T_C = 25°C	P_D	165	W
Power Dissipation Derating T_C > 25°C		1.32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	−40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at V_{GE} = 15 V	t_{SC}	4	μs
Short Circuit Withstand Time (Note 2) at V_{GE} = 10 V	t_{SC}	10	μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. V_{CE} = 360 V, T_C =125°C, R_G = 25 Ω

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Collector to Emitter Breakdown Voltage	BV_{CES}	I_C = 250 μA, V_{GE} = 0 V		600	–	–	V
Collector to Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = 25°C	–	–	250	μA
			T_C = 150°C	–	–	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C110}, V_{GE} = 15 V	T_C = 25°C	–	1.8	2.0	V
			T_C = 150°C	–	2.1	2.5	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250 μA, V_{CE} = V_{GE}		3.0	5.0	6.0	V
Gate to Emitter Leakage Current	I_{GES}	V_{GE} = ±20 V		–	–	±100	nA
Switching SOA	SSOA	T_C = 150°C, V_{GE} = 15 V, R_G = 10 Ω, L = 45 μH	V_{CE} = 480 V	100	–	–	A
			V_{CE} = 600 V	30	–	–	A
Gate to Emitter Plateau Voltage	V_{GEP}	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}		–	8.0	–	V
On−State Gate Charge	$Q_{G(ON)}$	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15 V	–	80	105	nC
			V_{GE} = 20 V	–	105	135	nC
Current Turn−On Delay Time	$t_{d(ON)I}$	T_C = 150°C, I_{CE} = I_{C110}, V_{CE} = 0.8 BV_{CES}, V_{GE} = 15 V, R_G = 10 Ω, L = 100 μH		–	25	–	ns
Current Rise Time	t_{rI}			–	20	–	ns
Current Turn−Off Delay Time	$t_{d(OFF)I}$			–	220	275	ns
Current Fall Time	t_{fI}			–	140	175	ns
Turn−On Energy	E_{ON}			–	475	–	μJ
Turn−Off Energy (Note 3)	E_{OFF}			–	1050	–	μJ
Diode Forward Voltage	V_{EC}	I_{EC} = 20 A		–	1.5	1.9	V
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 20 A, dI_{EC}/dt = 100 A/μs		–	–	55	ns
		I_{EC} = 1 A, dI_{EC}/dt = 100 A/μs		–	–	45	ns

Figure 111: Datasheet silicon IGBT 600V, 40A, TO-247

HGTG20N60B3D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$R_{\theta JC}$	IGBT	–	–	0.76	°C/W
		Diode	–	–	1.2	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Turn−Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0 A) The HGTG20N60B3D was tested per JEDEC standard No. 24−1 Method for Measurement of Power Device Turn−Off Switching Loss. This test method produces the true total Turn−Off Energy Loss. Turn−On losses include diode losses.

TYPICAL PERFORMANCE CURVES

Figure 1. TRANSFER CHARACTERISTICS

Figure 2. SATURATION CHARACTERISTICS

Figure 3. DC COLLECTOR CURRENT vs. CASE TEMPERATURE

Figure 4. COLLECTOR TO EMITTER ON−STATE VOLTAGE

Figure 112: Datasheet silicon IGBT 600V, 40A, TO-247

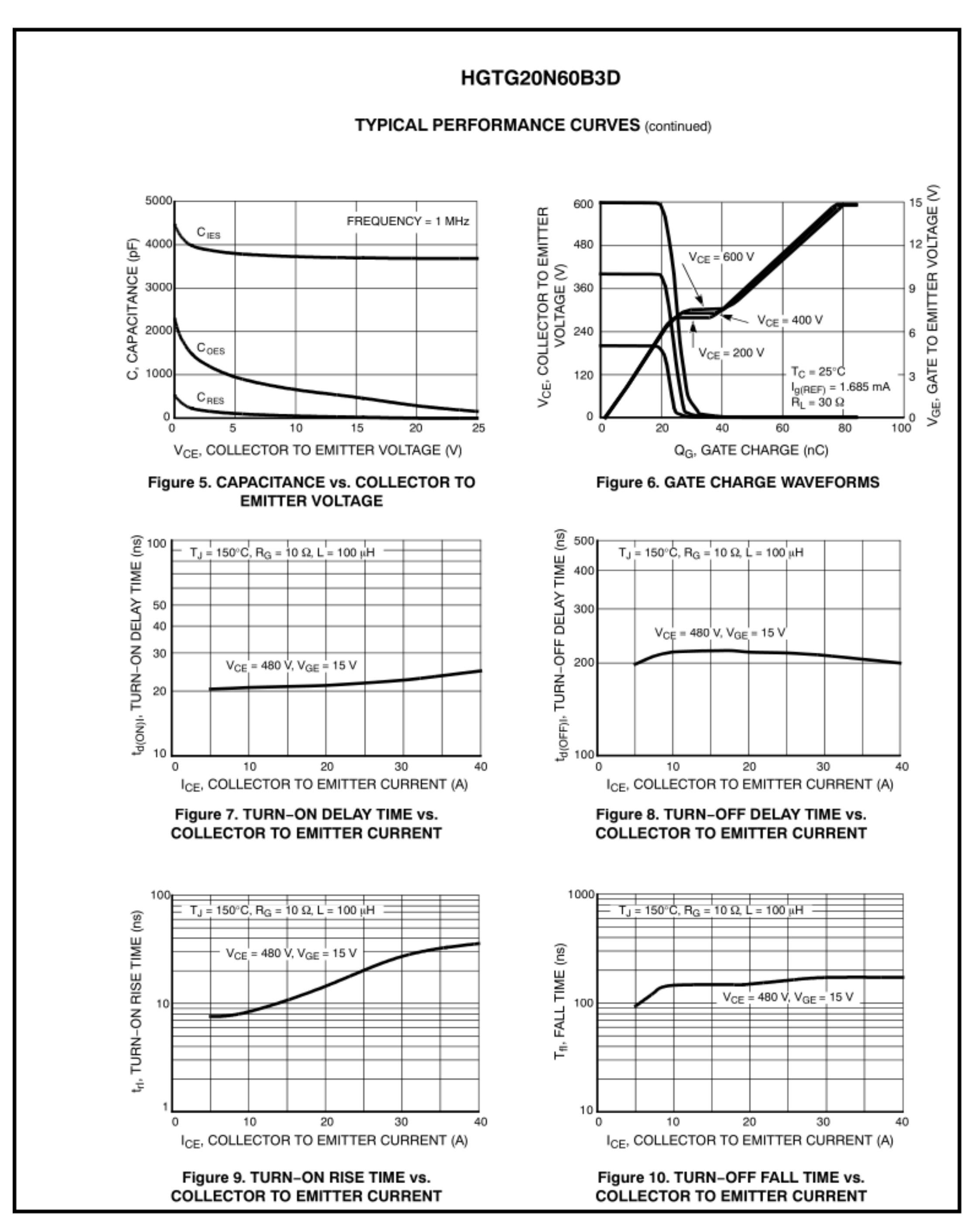


Figure 113: Datasheet silicon IGBT 600V, 40A, TO-247

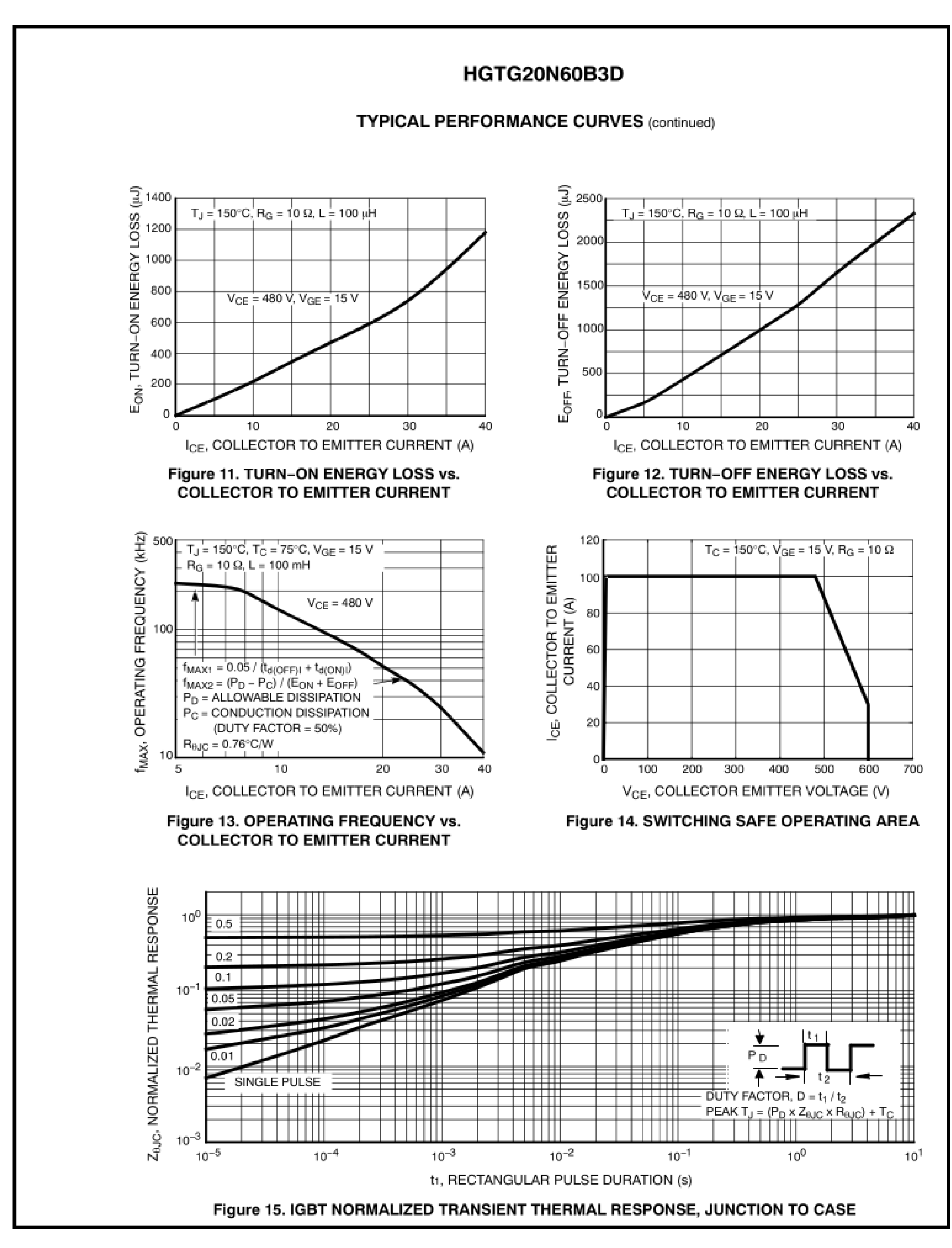


Figure 114: Datasheet silicon IGBT 600V, 40A, TO-247

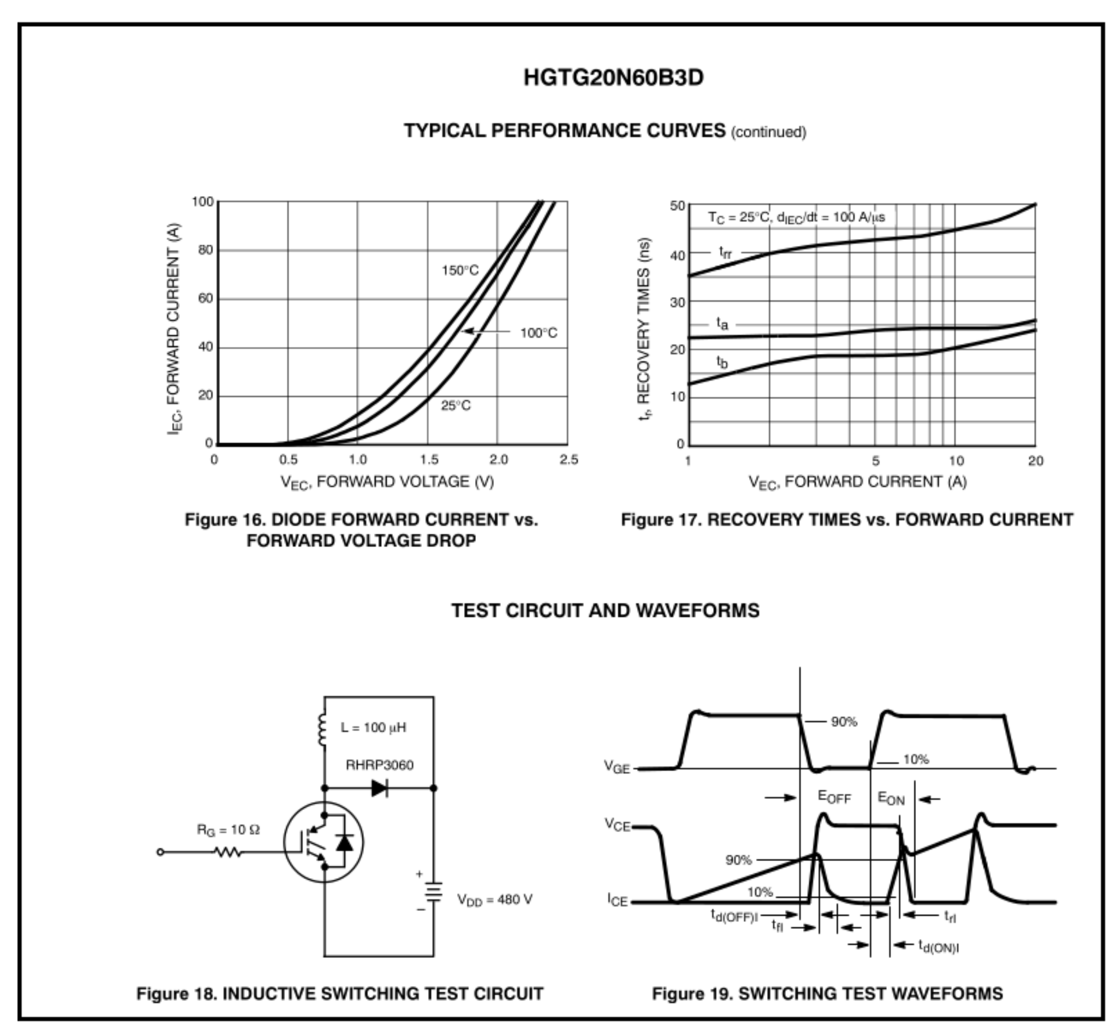


Figure 115: Datasheet silicon IGBT 600V, 40A, TO-247

Company Datasheet five

Company datasheet for IGBT, n–channel 1200V, 40A, TO247.

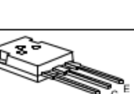
IKW25N120H3

High speed switching series third generation

High speed DuoPack: IGBT in Trench and Fieldstop technology with soft, fast recovery anti-parallel diode

Features:

TRENCHSTOP™ technology offering
- very low V_{CEsat}
- low EMI
- Very soft, fast recovery anti-parallel diode
- maximum junction temperature 175°C
- qualified according to JEDEC for target applications
- Pb-free lead plating; RoHS compliant
- complete product spectrum and PSpice Models: http://www.infineon.com/igbt/



Applications:
- uninterruptible power supplies
- welding converters
- converters with high switching frequency

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Marking	Package
IKW25N120H3	1200V	25A	2.05V	175°C	K25H1203	PG-TO247-3

Maximum ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	1200	V
DC collector current, limited by T_{vjmax} T_C = 25°C T_C = 100°C	I_C	50.0 25.0	A
Pulsed collector current, t_p limited by T_{vjmax}	I_{Cpuls}	100.0	A
Turn off safe operating area V_{CE} ≤ 1200V, T_{vj} ≤ 175°C	-	100.0	A
Diode forward current, limited by T_{vjmax} T_C = 25°C T_C = 100°C	I_F	25.0 12.5	A
Diode pulsed current, t_p limited by T_{vjmax}	I_{Fpuls}	100.0	A
Gate-emitter voltage	V_{GE}	±20	V
Short circuit withstand time V_{GE} = 15.0V, V_{CC} ≤ 600V, T_{vj} ≤ 175°C Allowed number of short circuits < 1000 Time between short circuits: ≥ 1.0s	t_{SC}	10	µs
Power dissipation T_C = 25°C Power dissipation T_C = 100°C	P_{tot}	326.0 156.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s		260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

Figure 116: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

IKW25N120H3

High speed switching series third generation

Thermal Resistance

Parameter	Symbol	Conditions	Max. Value	Unit
Characteristic				
IGBT thermal resistance, junction - case	$R_{th(j-c)}$		0.46	K/W
Diode thermal resistance, junction - case	$R_{th(j-c)}$		1.49	K/W
Thermal resistance junction - ambient	$R_{th(j-a)}$		40	K/W

Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Static Characteristic						
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0V, I_C = 0.50mA	1200	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	V_{GE} = 15.0V, I_C = 25.0A T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 175°C	- - -	2.05 2.50 2.70	2.40 - -	V
Diode forward voltage	V_F	V_{GE} = 0V, I_F = 12.5A T_{vj} = 25°C T_{vj} = 175°C	- -	1.80 1.85	2.35	V
Diode forward voltage	V_F	V_{GE} = 0V, I_F = 25.0A T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 175°C	- - -	2.40 2.60 2.60	3.05 - -	V
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 0.85mA, V_{CE} = V_{GE}	5.0	5.8	6.5	V
Zero gate voltage collector current	I_{CES}	V_{CE} = 1200V, V_{GE} = 0V T_{vj} = 25°C T_{vj} = 175°C	- -	- -	250.0 2500.0	µA
Gate-emitter leakage current	I_{GES}	V_{CE} = 0V, V_{GE} = 20V	-	-	600	nA
Transconductance	g_{fs}	V_{CE} = 20V, I_C = 25.0A	-	13.0	-	S

Figure 117: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

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Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Dynamic Characteristic						
Input capacitance	C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz	-	1430	-	pF
Output capacitance	C_{oes}		-	115	-	
Reverse transfer capacitance	C_{res}		-	75	-	
Gate charge	Q_G	V_{CC} = 960V, I_C = 25.0A, V_{GE} = 15V	-	115.0	-	nC
Internal emitter inductance measured 5mm (0.197 in.) from case	L_E		-	13.0	-	nH
Short circuit collector current Max. 1000 short circuits Time between short circuits: ≥ 1.0s	$I_{C(SC)}$	V_{GE} = 15.0V, V_{CC} ≤ 600V, T_{vj} ≤ 175°C, t_{SC} ≤ 10μs	-	87	-	A

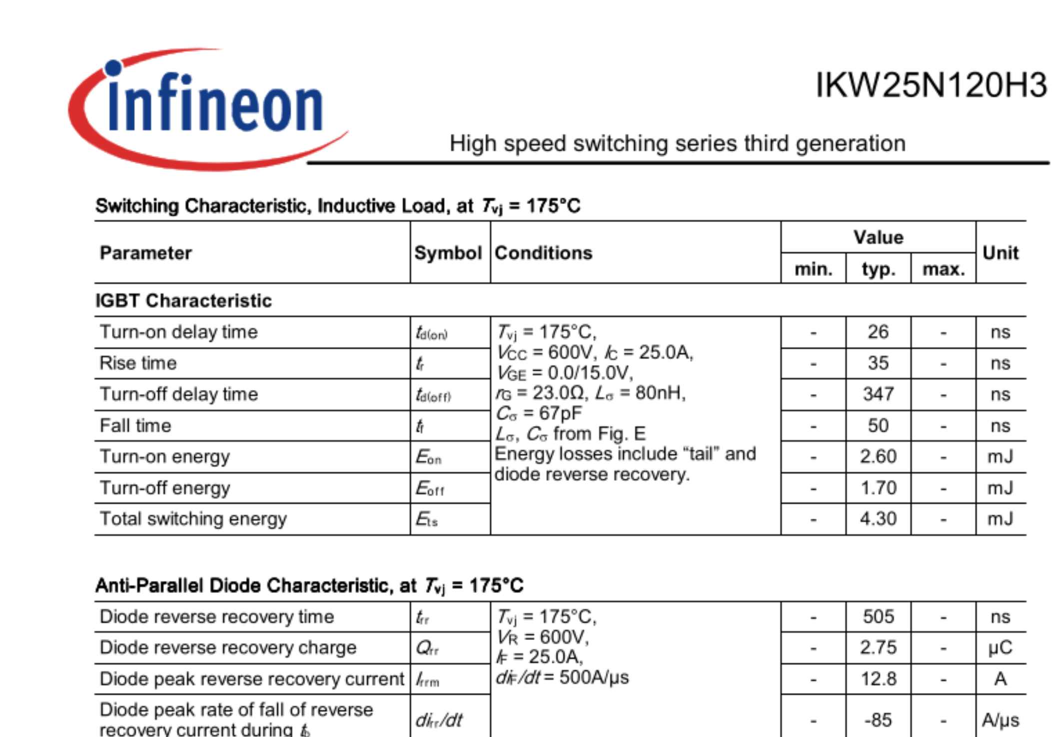
Switching Characteristic, Inductive Load, at T_{vj} = 25°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 25°C, V_{CC} = 600V, I_C = 25.0A, V_{GE} = 0.0/15.0V, r_G = 23.0Ω, L_σ = 80nH, C_σ = 67pF, L_σ, C_σ from Fig. E. Energy losses include "tail" and diode reverse recovery.	-	27	-	ns
Rise time	t_r		-	41	-	ns
Turn-off delay time	$t_{d(off)}$		-	277	-	ns
Fall time	t_f		-	17	-	ns
Turn-on energy	E_{on}		-	1.80	-	mJ
Turn-off energy	E_{off}		-	0.85	-	mJ
Total switching energy	E_{ts}		-	2.65	-	mJ

Anti-Parallel Diode Characteristic, at T_{vj} = 25°C

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode reverse recovery time	t_{rr}	T_{vj} = 25°C, V_R = 600V, I_F = 25.0A, di_F/dt = 500A/μs	-	290	-	ns
Diode reverse recovery charge	Q_{rr}		-	1.20	-	μC
Diode peak reverse recovery current	I_{rrm}		-	10.4	-	A
Diode peak rate of fall of reverse recovery current during t_b	di_{rr}/dt		-	-150	-	A/μs

Figure 118: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.



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High speed switching series third generation

Switching Characteristic, Inductive Load, at T_{vj} = 175°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 175°C, V_{CC} = 600V, I_C = 25.0A, V_{GE} = 0.0/15.0V, r_G = 23.0Ω, L_σ = 80nH, C_σ = 67pF L_σ, C_σ from Fig. E Energy losses include "tail" and diode reverse recovery.	-	26	-	ns
Rise time	t_r		-	35	-	ns
Turn-off delay time	$t_{d(off)}$		-	347	-	ns
Fall time	t_f		-	50	-	ns
Turn-on energy	E_{on}		-	2.60	-	mJ
Turn-off energy	E_{off}		-	1.70	-	mJ
Total switching energy	E_{ts}		-	4.30	-	mJ

Anti-Parallel Diode Characteristic, at T_{vj} = 175°C

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode reverse recovery time	t_{rr}	T_{vj} = 175°C, V_R = 600V, I_F = 25.0A, di_F/dt = 500A/μs	-	505	-	ns
Diode reverse recovery charge	Q_{rr}		-	2.75	-	μC
Diode peak reverse recovery current	I_{rrm}		-	12.8	-	A
Diode peak rate of fall of reverse recovery current during t_b	di_{rr}/dt		-	-85	-	A/μs

Figure 119: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

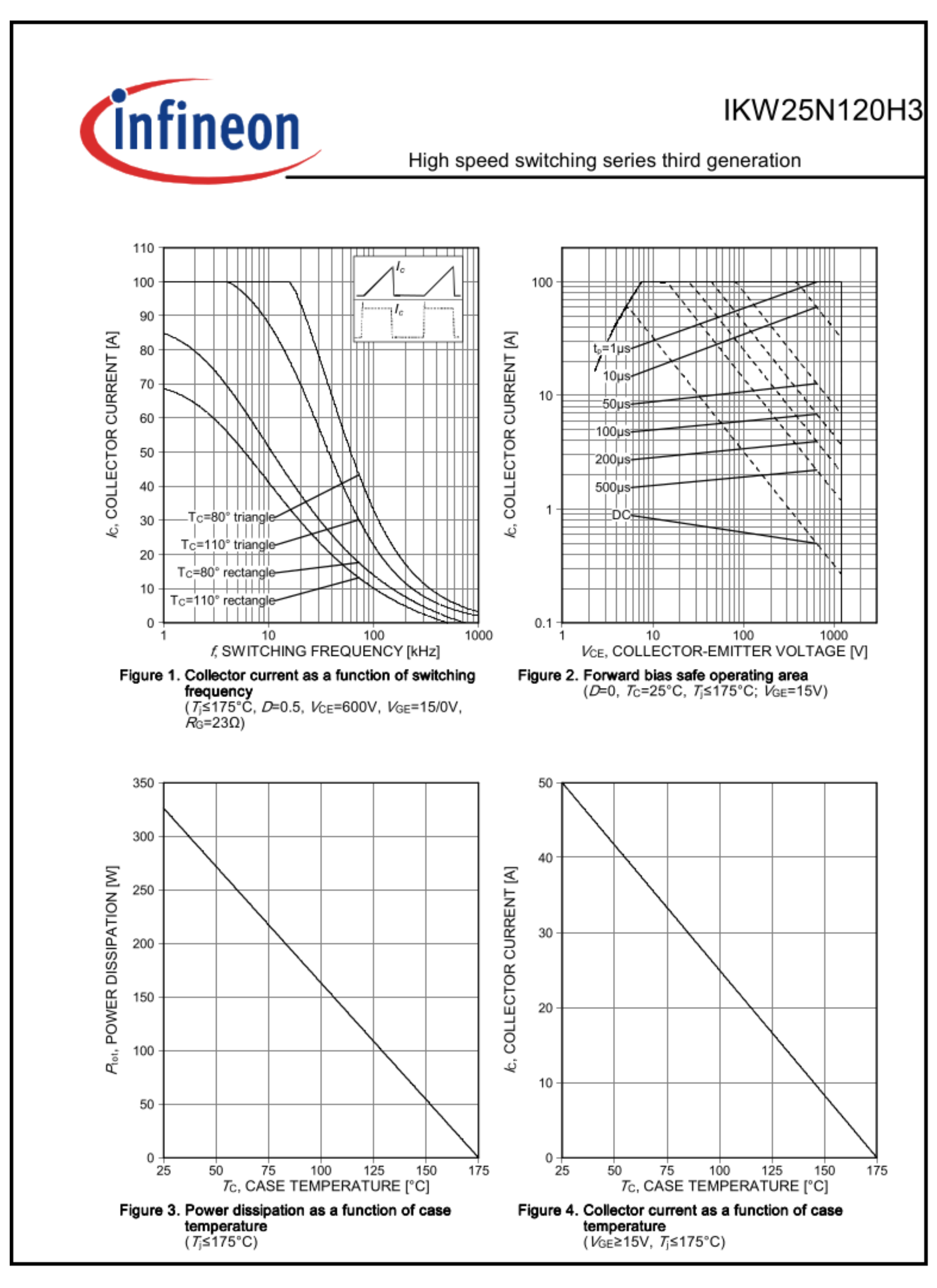

Figure 120: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

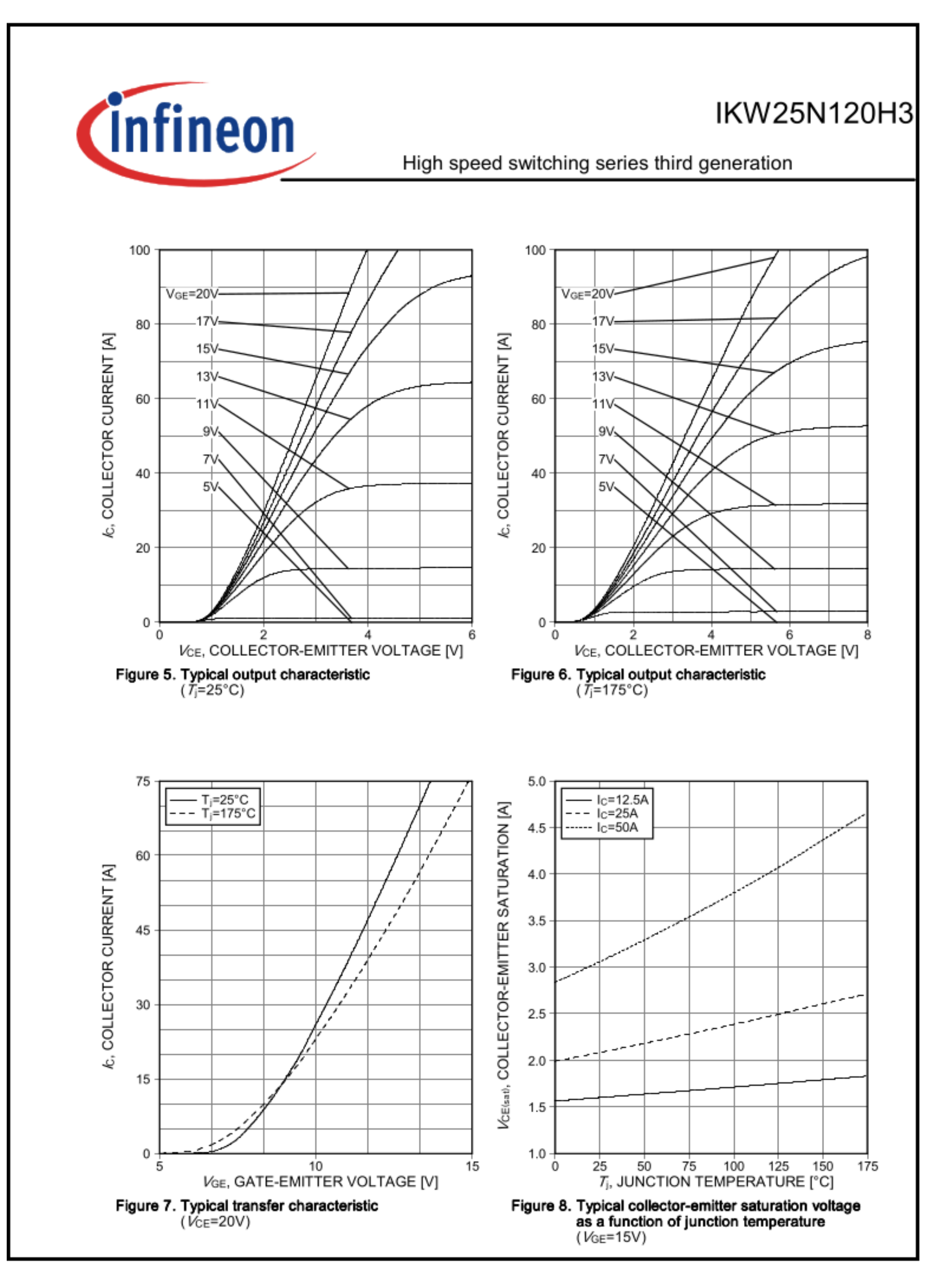

Figure 121: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

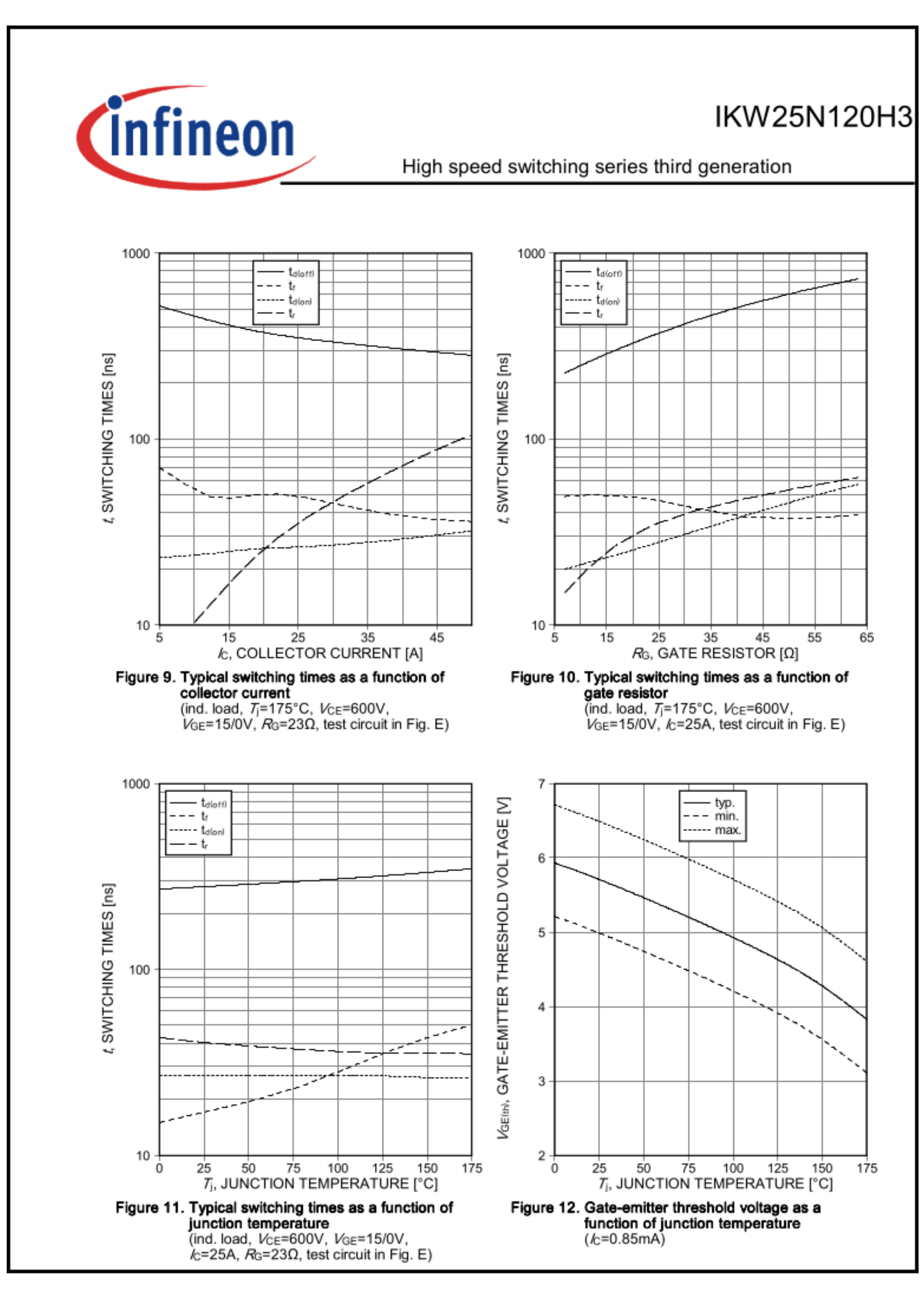

Figure 122: Datasheet silicon IGBT, n-channel 1200V, 40A, TO247.

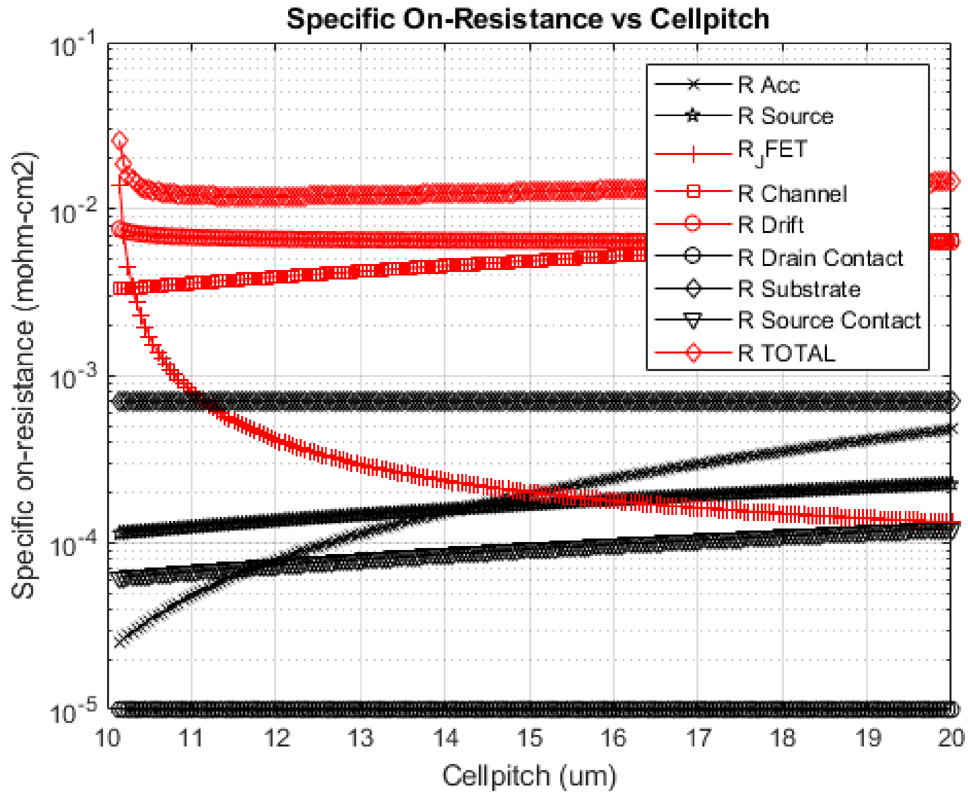

Figure 123: SiC DMOS 1.2 KV, 20 A, family of curves [60].

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