A Dry Etch Approach To Reduce Roughness And Eliminate Visible Grind Marks In Silicon Wafers Post Back-grind

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***Abstract*—3D wafer packaging represents a significant component of the total wafer level processing cost. Replacement of the Chemical Mechanical Polishing (CMP) process step with a corresponding dry etch can yield significant time and cost savings. Incorporating equipment already utilized in the 3D integrated wafer packaging process during the subsequent Through Silicon Via (TSV) reveal step, process efficiencies can be achieved, with overall die yields being maintained. Using dry etch technology to treat a 200nm rough back-ground silicon surface, a smooth surface with a peak to valley roughness of less than 6nm is demonstrated. This patented process differs from other dry etch smoothing techniques in that it aims to eliminate any visual grind marks rather than just reducing the surface roughness. The elimination of visible grind marks is critical in later optical inspection where they are falsely identified as defects. The quality of the surface is equivalent to that of a CMP processed wafer and as such, this process has been implemented in manufacturing replacing the CMP step. The novel process described combines a surface modification followed by a roughness reduction in an iterative manner to produce a smooth surface without visible grind marks post processing.**

***Index Terms*—3D Technology, Advanced Packaging, CMP replacement, Dry Plasma Etch, Smoothing, TSV**

I. Introduction

Through silicon vias (TSV) are advance-packaging, high-performance vertical interconnects. They are used as an alternative to wire-bond and flip chips to create 3D integrated circuit stacks. Vias etched into the silicon wafer allow short, low resistance vertical electrical interconnects between stacked die in 3D integrated circuits, leading to faster operation than conventionally bonded structures such as wire bonding or flip-chip bonding [1].

3D packages utilizing TSV technology reduces IC "footprint" and allows heterogeneous integration of devices in the die stack, for example, combining complimentary metal-oxide semiconductor (CMOS) logic, dynamic random-access memory (DRAM) and group III-V compound materials into a single stack.

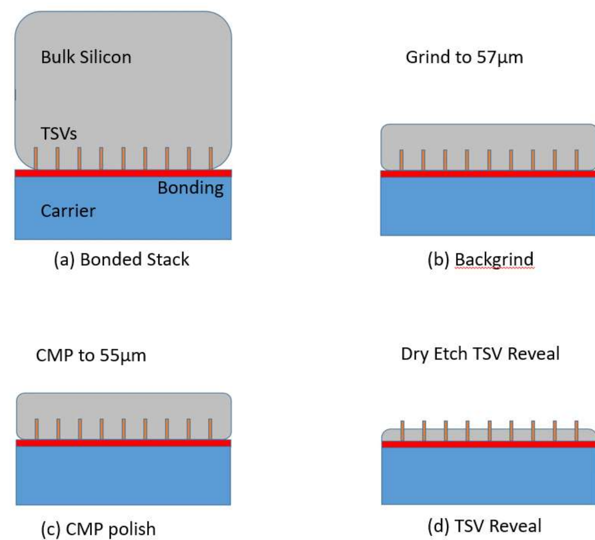

Figure 1: *TSV reveal Process Flow (a) Full thickness wafer with embedded vias is bonded face down on a carrier wafer (b) The wafer undergoes fast back grinding to approximately 57µm leaving grind marks and silicon damage (c) a CMP process is applied which removes visible grind marks and polishes the wafer surface to approximately 5nm surface roughness. It is this step that is replaced by the "Grow & Mow" dry etch (d) A dry etch reveal process removes approximately 15µm of silicon to reveal the TSVs to a uniform height.*

TSV Reveal Process

The conventional TSV reveal process flow (Figure 1) starts with copper-filled vias in a silicon wafer from the via-first or via-middle flows, which is bonded, device side down to a carrier wafer (Figure 1 a). This carrier substrate can be glass or silicon, and bonding can be either adhesive-based, or fusion bonded [2]. Fast back-grinding is used to thin the bulk silicon wafer from approximately 750µm to a remaining silicon thickness (RST) of 57µm. This process is faster than current dry

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etch processes, with some silicon remaining above the TSV (Figure 1 b). The fast grind process leaves abrasion marks on the surface of the wafer, which, depending on the grinding wheels and slurries used can be up to 400nm in depth which are easily seen without magnification. These grind marks are variable in width and depth. Additionally, there are other grooves and pits on the wafer surface caused by grinding tool degradation which are significantly deeper and wider than average. The back-grind process causes subsurface damage and leaves surface particles, which require removal in a post grind clean [3].

The wafers are then Chemical Mechanical Polish (CMP) treated to produce a smooth "mirror finish" surface, removing the grind marks and reducing the subsurface damaged caused by the grind process, removing around 2µm of material (Figure 1 c). However, minimum CMP values are dictated by the surface roughness and maximum removal dictated by the need to avoid breaching the oxide TSV liners. CMP cannot be used to reveal the TSVs due to copper contamination of the silicon as material from the tips of the copper-filled vias would be smeared across the wafer surface. CMP itself is considered a dirty process compared to other semiconductor processes, leaving particles on the substrate from the wafer and also the slurries used for polishing [3]. The patented dry etch process has been developed to reduce roughness and surface damage in this stage of the process [4].

A dry or wet etch TSV reveal process step, typically removing approximately 15µm of silicon is then used to expose the vias to a revealed depth between 1 and 5µm, which ultimately form the interconnects between die stacks (Figure 1 d). The process flow used here uses a patented dry etch thinning step [5], selectively etching the bulk Si, but leaving the thin oxide via casings intact. It is important not to etch through the protective oxide layer encasing the vias as copper sulphate would form from interaction with the etching gas sulphur hexafluoride (SF_6) which causes yield loss in subsequent process steps. The novel approach described here to polish wafers uses the same module and gases as this TSV reveal step. While the smoothing process can be used as a thinning step, the deliberate slow etch rate compared to the TSV reveal means that it is not used to thin and reveal TSVs. It only replaces the CMP polish step (Figure 1 c).

The point at which the copper vias are exposed is a critical part of this wafer thinning step. Some of the risks involved in this step include backside contamination (copper diffusion) due to premature contact with the vias, and poor via fabrication depth uniformity. These can also contribute to issues with RST post-grind and may result in TSVs that are not evenly revealed, and in some cases, not exposed at all.

There has been an interest in life cycle assessment (LCA) with a view to reducing the environmental impact of the semiconductor industry [7]. Such considerations include pollution in air and water along with energy usage [8]. So several advantages in replacing the CMP step in the TSV reveal process are evident: the removal of an expensive CMP toolset from the process flow; introduction of faster, cleaner, more controlled, repeatable [7] and more environmentally friendly dry etch processes with reduced contaminated waste and slurries [9], (dry etch process gases needing simply to be abated [10] [11]). A dry etch process such as TSV reveal, or the replacement smoothing process can also reduce the mechanical stress on wafers, caused by rough back grind. The consequent improvement of die yield and hence wafer yields due to fewer false detections of wafer defects by metrology tools [12] adds to the significant cost benefits [13] of integrating a dry etch polishing process into a general TSV reveal scheme. Generally, there is an optical inspection (using a 2.5 x objective) to ensure product quality prior to covering the TSVs with a pad. Aside from reduction of grind damage without removal of the grind marks there is a strong possibility that this inspection will falsely count grind marks as defects.

Replacement of the CMP process with an integrated dry etch process would reduce material costs associated with CMP (use of expensive slurries [14], polishing pads and critical post-cleaning steps), eliminate the requirement of an expensive CMP toolset with a large fab footprint, and provides greater process control and reduced process variation. In traditional CMP, variation between machines, slurries and pads introduces associated costs due to additional metrology loads [4], which can be reduced or eliminated using this Dry Etch method.

The CMP process step has been reported to be up to 50% of the cost of the TSV reveal process [6]. Any reduction for this step would have a significant impact on the overall cost of the TSV process flow. As the TSV reveal step is completed using a dry etch, there would be a reduction of high-volume manufacturing (HVM) operational costs as the same tool of record (TOR) would be utilized for the integrated dry etch CMP replacement process. The two steps can be processed in the same module, with no break in plasma if required. This reduces wafer loading and unloading steps, leading to cost and time savings. [15] [16]. The two processes combined take approximately ten minutes to complete from wafer loading to unloading for a typical TSV reveal.

With the 3D-stacked IC-package wafer-equivalent market forecast to grow from 2.5 million wafers in 2019 to some 9.5 million wafers in 2025 [17] there is an opportunity for semiconductor manufacturers to make significant cost reductions in relation to TSV reveal – and potentially other process flows.

There are some types of processes that cannot utilize conventional CMP for which this plasma dry etch is suitable. Included within these are extreme wafer thinning processes, where for wafers ground to less than approximately 35µm remaining silicon, traditional CMP causes too high a mechanical stress, resulting in wafer chipping and cracking [16]. A further use within microelectromechanical systems (MEMS) has been to smooth surfaces with topography, such as microneedles, or preparing a surface for mask patterning [18] where the original surface profile needs to be maintained, however these are outside the scope of this paper.

II. Experimental

Etch development was performed using an SPTS Rapier™ XE, a dual source (two separately controlled sources, with primary and secondary gas flows) inductively coupled plasma (ICP) reactor platform - a tool commonly used for TSV reveal processes.

The SPTS Rapier™ XE [19] (Figure 2) uses high power radio frequency (RF) generators, adaptable hardware and large volumes of SF_6 to support high silicon etch rates (~10µm/min for 300mm wafers) and good selectivity to other materials such as photoresist or oxides, for example 100:1 selectivity to oxide. The dual source combined with dual gas inlets allows a significant degree of process tuning to reduce non-uniformity. A helium backside cooling system prevents excessive temperatures on the wafer surface during the exothermic etch process and is used to drive temperature sensitive process parameters.

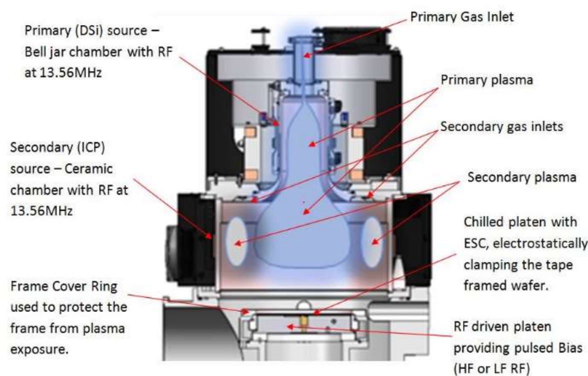

Figure 2: *Cross section schematic of SPTS Rapier XE dual source Deep Reactive Ion Etching (DRIE) module*

The dual source configuration with a total power output of 8kW allows good control of etch rate, which can be used to compensate for incoming material variation, by software and hardware changes. Rapid gas switching is accommodated using high flow, mass flow controllers. Combined with the software control, this rapid switched-etch enables the novel silicon smoothing process, presented in this paper.

Surface characterization was performed using a Zeiss Supra Field-Emission scanning electron microscope (FE-SEM), a Zygo white-light interferometer for 2D and 3D surface analysis, a Fogale T-MAP low coherence infrared interferometer for etch rate and non-uniformity calculations, a Leica DM12000 optical microscope, a Park Systems XE-7 atomic force microscope (AFM) and a Thermo Fisher X-ray photoelectron spectroscope (XPS).

Processing was performed on 300mm bulk silicon substrates, treated with a variety of rough grinds, with most wafers prepared using a Poligrind® method. Poligrind is a type of grinding wheel made by Disco Corporation, used in precision in-line feeders, which allows for smoother, thinner grooves [20]. Some of these processes were also performed on final-product thinned silicon wafers bonded to glass or silicon carriers.

III. "Grow and Mow" Process Development

For a manufacturer to use a different process component in a flow, the minimum requirement is that insertion of the new process must cause no adverse change to the rest of the process flow, equaling or ideally bettering the current process. For instance, the initial back grind thins the mounted wafer to circa 57µm, with the traditional CMP process removing 2µm to leave a RST of 55µm, leaving 10µm of silicon above the buried pins. Therefore, a requirement for the replacement dry etch silicon smoothing process was that a limit of 2µm silicon removal was imposed on process development, even though the back grind could be biased to accommodate a greater or lesser amount of silicon removal and was based on matching reported performance criteria such as material removed, etch rate and process time, from a competitor's wet CMP process. For instance, a criterion imposed by an end user of this process was that the process should be no longer than ten minutes. This was to match reported process times for wet etch smoothing [6].

The process was not conceived as a thinning step, as in this process scheme that was completed using the TSV reveal step. As such, any consideration of adjusting the profile of the incoming wafers was ignored as the subsequent TSV reveal etch, by removing a greater amount of silicon was tuned to reduce any total thickness variation (TTV). It is for this reason that selectivity to the oxide liners on the buried TSVs was not a consideration as the process would never reveal any of them [16]. This is not always the case however as roughness reduction and thinning can be combined in a dry etch of 30-100µm depth [21]. A process using a Bosch cycle has been used for TSV reveal, in a combined thinning and smoothing step, but the revealed surface was rough. It was seen that on a nano scale grind marks were not as obvious as they had been [22]. This points to the need for a process that can smooth a surface on both macro and micro scales.

This material removal constraint is not critical, as the previous grind step can be adjusted to control the thickness of remaining sacrificial silicon, however initial process development often needs to be directly comparable with any processes being replaced, to minimize any additional time consuming and costly requalification of processes.

A polymer-free process was developed to also achieve better integration into the overall process scheme, with longer mean times between cleans (MTBC) [23]; a critical cost of ownership (COO) [24] metric. Polymeric processes have a greater impact on the condition of the etch chamber than non-polymeric processes, due to buildup of deposits on any plasma facing surfaces [25]. This leads to lower MTBC with the requirement

to purchase more tools to compensate for the cleaning related down time.

IV. CONCEPT AND FEASIBILITY

Initial inspection of wafer surfaces showed that ground wafers (Figure 3) were at least one order of magnitude rougher than polished wafers, as can been seen in Table II. A typical polished silicon surface has a peak to valley roughness of around 6nm, and an R_a of 0.5nm whereas Poligrind has a peak to valley roughness approaching 100nm and an R_a of 2.6nm, with fine grind wafers averaging twice these figures. Thus, a significant reduction in surface roughness would need to be achieved using the dry etch smoothing process in order to reclaim a smooth surface, comparable with a CMP finished wafer.

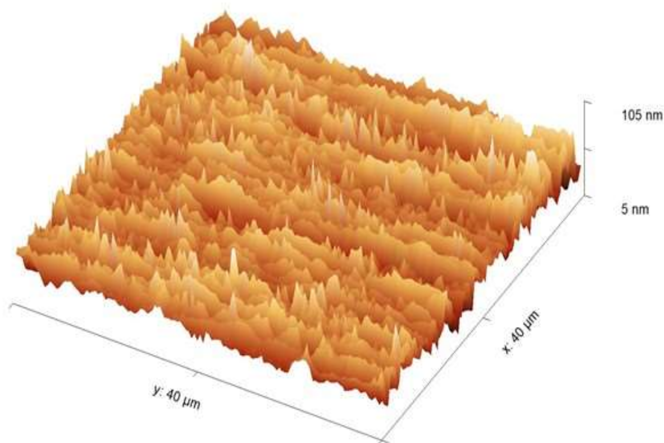

Figure 3: *AFM topographical image of a pre-etch Poligrind wafer surface, from wafer centre 40µm x 40µm scale. Z axis scale is in nanometers.*

Dry etching of silicon generally has two modes, isotropic, where a chemical etch, using available free radicals, propagates in all directions equally, and anisotropic, a more physical etch, which is more directional, due to the acceleration of ions within the plasma influenced by an external electric field [26]. Dry etch processes are a combination of both isotropic and anisotropic etching, with a trend towards line-of-sight etching [27]. The isotropic mode is chemical in nature relying on available free radicals. Using these two modes, several different etch approaches were trialed (Table I).

The baseline process was a high pressure (85mT) etch, using only SF_6. This was based on the TSV reveal thinning step used in the current process flow [5]. The Baseline Process (Table I) produces an RMS surface roughness of 5.6nm when used on a previously CMP polished wafer of similar roughness. This indicates that etching a polished wafer with this process does not increase the wafer's overall surface roughness. With chemical etching the dominant etch mode, silicon removal is isotropic. With no constraining species transport factors such as in trenches and vias there is no increase in overall morphology and topography.

TABLE I

PARAMETERS OF SELECTED PROCESS DEVELOPMENT TRAILS

Run	Process	Roughness (Peak to Valley) nm	R_a nm
Base	TSV Reveal Process on Polished silicon wafer	5.6	0.49
1	TSV Reveal Etch 90 seconds	110	-
2	TSV Reveal Etch, no bias, 20 loops	66	-
3	RIE oxide etch using CF_4	29	2.49
4	RIE oxide etch using C_4F_8 / Ar / O_2	33	3.35
5	Non switched C_4F_8 / SF_6 etch	36	3.65
6	Oxidation with etch back	36	2.99
7	Sloped non switched etch	191	15.51
8	ICP polishing recipe	666	47.77
9	High Ar, low SF_6 etch	51	4.64
10	Quasi Bosch Etch	21	1.93
11	20s BT plus run #10	56	4.59
12	20s RIE oxide etch plus run #10	27	2.49
13	TSV reveal but $CF_4/O_2/N_2$	25	3.06
14	5 mins of $CF_4/O_2/N_2$	17	2.18
15	Using OES to match etch / dep cycles of run #10	16	1.50

When this process is applied to a ground wafer (Table I, Process 1), an increase in roughness is seen post etching (110nm) compared to the pre-etch roughness (80nm) of a Poligrind wafer. This is unexpected as an isotropic etch would be predicted to smooth out any topography as the expanding wave fronts will etch any roughness from either side, etching this faster than any horizontal surface and is contrary to expected results of both roughness and grind mark reduction [16].

A variant of this process, with no applied bias on the chuck (Table I, Process 2) yielded a reduction in surface roughness, both with respect to the biased process and the pre-etch wafer surface roughness.

After trialing the baseline process, attention turned towards other possible approaches, such as Reactive Ion Etching (RIE) (Table I, Processes 3 & 4), where it was felt that a slow silicon etch might round features to produce a flatter surface.

Process 5 used a non-switched mixed gas approach, where a balance of deposition (C_4F_8) and etch (SF_6) gases could be adjusted to either etch cleanly or imperfectly. This approach has been used [22] for vertical TSV scallop reduction, but was not successful in eliminating grind marks.

Further to the reactive ion etch approach, an oxidation and etch back approach was tried (Table I, Process 6) as this has been successfully used to reduce TSV sidewall roughness [28]. This approach proved unsatisfactory, as no significant oxide growth

was found or measurable, and no reduction of surface roughness was observed, with grind marks still evident.

A Bosch-type process [29], a cyclical regime of alternating deposition and etching phases, was investigated. This was designed to fill any valleys with polymeric material, and then etch back this material, along with any protruding silicon that became exposed during the etch phase. This yielded significant improvements in surface roughness (from 80nm to 21nm). In practice this approach did smooth the surface of the wafer, though clearly visible grind marks remained obvious. (Table I, Processes 10,11,12 & 15)

It was realized that to obtain a smooth surface, the grind pattern must be removed or disrupted, and a subsequent smoothing process then applied. Usually when smoothing processes are used grind marks are still visible, acting as diffraction gratings or Fresnel lenses. The main concern was not only the roughness of the surface post etch, but that the grind marks are wrongly seen as process defects by automatic inspection equipment leading to false yield loss.

Several processes achieved disruption of the regular grind pattern, including: a TSV reveal etch without applied chuck bias (Table I Process 2, and Figure 6), a similar ICP based process (Table I Process 8) and a polymeric process using CF_4/ O_2 and N_2 (Table I Process 14). All these processes resulted in a cloudy wafer surface (no mirror-finish) being produced, with the increased, but random surface roughness incoherently scattering light incident on the wafer surface. For example, a Poligrind wafer etched for 5 minutes in a $CF_4/O_2/N_2$ bias-less process (Table I Process 14 & Figure 4) eliminated the grind marks, but had an Average Roughness (Ra) of 2.17 compared to a polished wafer Ra of 0.5 (Table I)

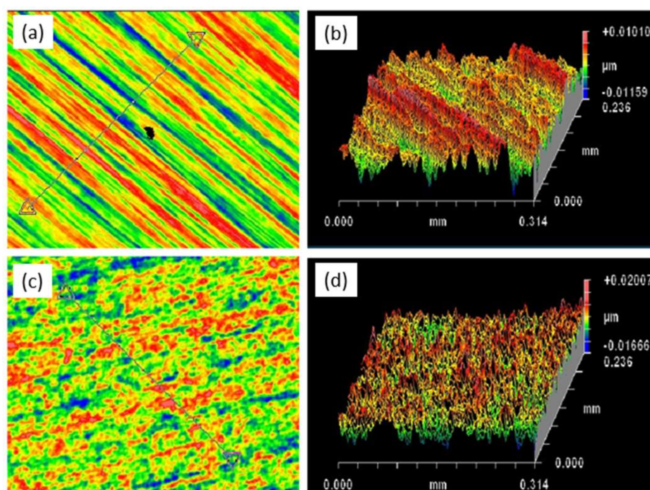

Figure 4: *White light interferometry (a) Pre-smoothing 2D with visible grind marks (b) Pre-smoothing 3D with visible grind marks (c) post-smoothing 2D with grind mark pattern disrupted (d) post-smoothing 3D with grind mark pattern disrupted*

This work led to the conclusion that the smoothing process needed to have two components: an initial etch that disrupted the regular spaced grind marks, and a second etch that then smoothed this new surface texture in an iterative scheme, in an iterative, looped process.

To reduce complication and provide commonality of gases and toolsets a process using only SF_6, O_2 and Argon was chosen as this matched the subsequent TSV reveal step. This had the additional benefit of retaining an extended MTBC as no polymeric gases such as C_4F_8 were needed.

Figure 5 shows pre and post "Grow" step images of a fine grind wafer having been subjected to 5 minutes of high pressure (>200mT) SF_6 based bias-less processing. The grind pattern is disrupted post etch (Figure 5b), resulting in an altered and smoother topography, devoid of linear grind marks, and an optically cloudy surface.

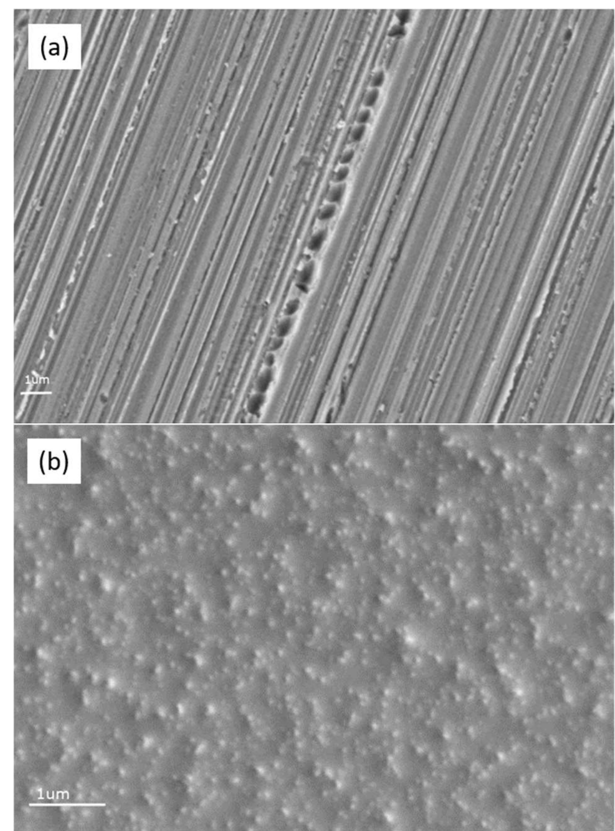

Figure 5: *(a) Pre-etch Fine Grind wafer surface 1µm scale bar(b) Post grow-step only wafer surface showing chaotically rough surface having disrupted the grind marks 1µm scale bar*

The process creates micro-masking on the surface of the ground wafer, with the resulting surfaces being etched in a chaotic manner (Figure 5b). A similar effect results on any type of bare silicon wafer etched with this process (Figure 6). Surface roughening occurs in SF_6-only plasmas, so it is suggested that either a silicon sulphide or a sulphur complex on the surface of the wafer causes the micro-masking effect. Sulphur containing compounds have been shown previously to create a haze on silicon wafers [30], however this has proved difficult to confirm; on wafers being in contact with atmosphere post etch

a strong sulphureous smell is observed, which dissipates in a short time. Following this initial surface roughening [5], a secondary smoothing process can then be applied.

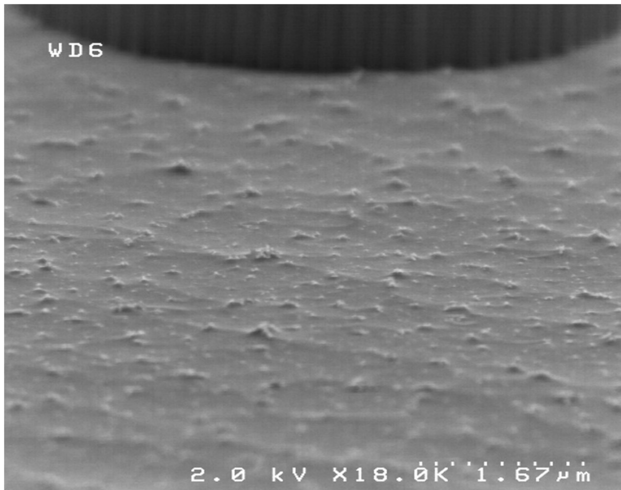

Figure 6: *Rough silicon surface of TSV reveal when etched with no applied bias, with edge of revealed TSV at top of image*

The combination of initial surface roughening, to remove grind marks, followed by a surface smoothing step had the desired effect of reducing the grind marks but did not produce a completely mirrored surface.

Thus, a modified process was developed which used a switched, iterative process, consisting of alternating steps of roughening and smoothing, which can be likened to 'Growing' silicon grass and 'Mowing' back, with an optimized 3:1 cycle time ratio between 'Mow' and 'Grow'. As the tool set has already been modified to use switched process, it is highly suitable for implementing the "Grow & Mow" process step.

V. Results

This program of work consists of a zero applied bias, high pressure, SF_6 / O_2 plasma etch, (the "Grow" step), followed by a high bias, low pressure, SF_6 / argon process (the "Mow" step) to remove any micro-masking and preferentially remove any silicon grass (as shown in Figure 4c, Figure 4d and Figure 5b) that had formed during the previous etch step.

The initial high pressure etch was designed to reduce ion bombardment of the wafer surface and to maximize deposition of micro-masking material. The oxygen component of the process gas mixture acts as a non-reactive carrier gas to reduce the amount of silicon material being etched during this step.

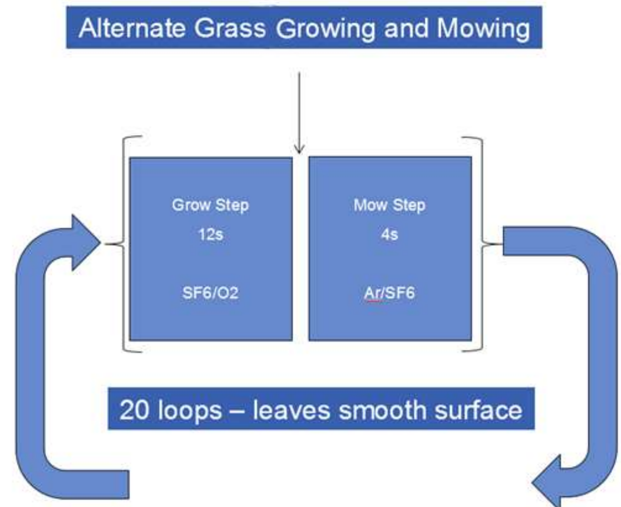

Figure 7: *Representative smoothing process for eliminating back-grind abrasion marks and reduction of surface roughness consisting of a grow step (making the surface chaotically rougher) of 12 seconds and a mow step (to eliminate surface roughness) of 4 seconds, looped 20 times to produce an optically smooth surface*

During optimization, an SF_6-only process produces a milky surface, whereas and SF_6/ oxygen process does not. The milky surface is an indication of micro-roughening of the wafer surface and a step towards the disruption of the regular grind marks as seen in Figure 5a. Whilst oxygen can interact with the surface to create a thin oxide, it does not etch the silicon surface. In contrast fluorine radicals readily reacts with silicon in an exothermic process, creating pits in between the micro-masked areas, which is the beneficial mechanism necessary to disrupt the regular grind marks and create a chaotically rough surface. This has been designated the "Grow" step, as whilst not growing a layer on the surface of the substrate the effect was to create a more randomly rough surface than that seen pre-etch.

The corresponding step was called the "Mow" step, as it is an analogue to mowing grass. It was designed to apply as much surface bombardment as possible to remove any surface deposits created in the previous step. This was achieved with a high applied bias, lower pressure and the addition of argon which provided additional physical bombardment without chemical etching. The free radical fluorine produced during SF_6 dissociation [31] reacts with the surface silicon to create volatile etch by-products such as SiF_4 which are then pumped away, with a low flow to reduce silicon loss.

Figure 8 shows the obvious improvement between the wafer post back grind (Figure 8a) with highly visible and present grind marks and the wafer after treatment with "Grow & Mow". This can also be seen clearly using optical microscopy on the same surface shown in Figure 9, which shows images at x500 magnification pre (Figure 9a) and post etch (Figure 9b). It is these grind marks, even with sub 10nm roughness, which are not addressed by other dry etch smoothing or thinning schemes and which are characterized as defects in later inspection stages.

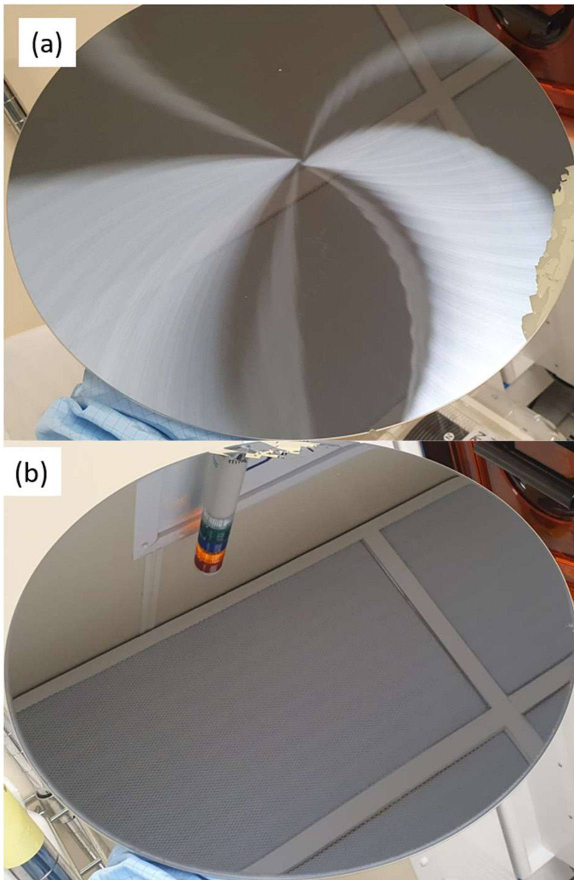

Figure 8: *(a) Poligrind wafer showing grind marks prior to "Grow & Mow". Silicon at edge of wafer removed for analysis (b)Poligrind wafer showing smoothed surface free of grind marks post "Grow & Mow"*

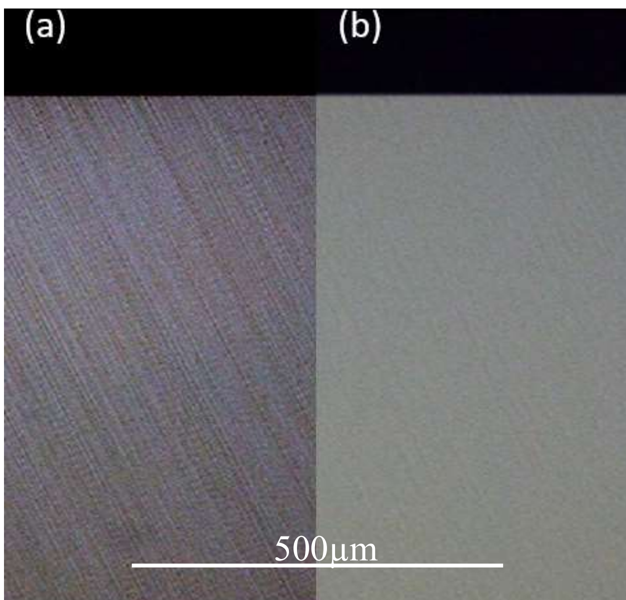

Figure 9: *(a) Pre-Smoothing Optical Image of Poligrind wafer (x500) (b) Post Smoothing Optical Image of Poligrind wafer (x500)*

Initial surface roughness analysis was performed using a Zeiss Supra FE-SEM and corroborated using a Park Systems XE-7 AFM in non-contact mode. Figure 10a shows typical debris on the surface from the prior grind step which are almost always observed. The presence or absence of this debris is highly dependent on the quality of the clean post grind, if a clean is in place [3]. Figure 11a shows the comparative surface, when measured using the AFM.

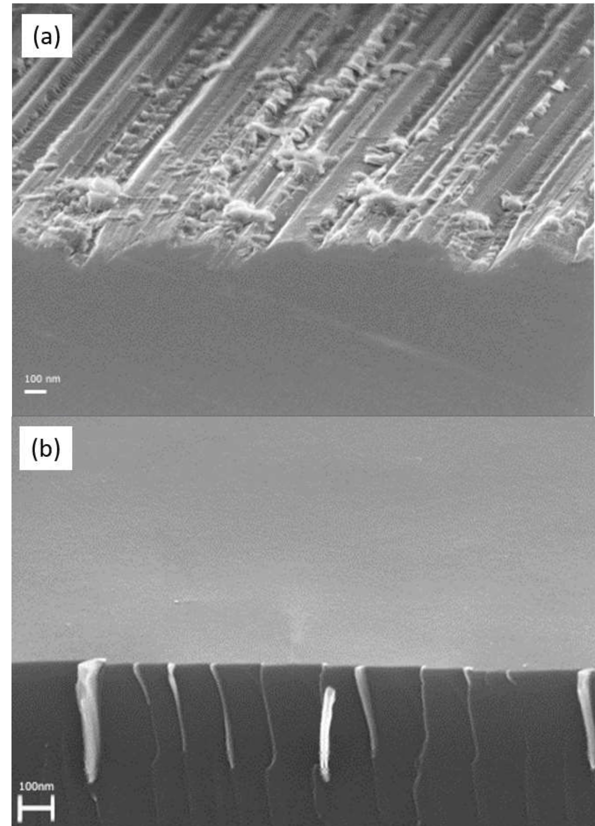

Figure 10: *(a)FE-SEM image of a back-ground wafer showing quasi-parallel grind marks, skitter marks (from broken grind diamonds) and surface debris. Scale bar 100nm (b) FE-SEM of a wafer surface after Grow & Mow process showing significant reduction in grind marks and surface roughness. Scale bar 100nm*

Figure 10b shows the wafer post "Grow & Mow", where the wafer surface is significantly smoothed with the grind marks no longer evident (Figure 10). The process was applied to wafers with an initial roughness of 80-500nm and results in a post etch roughness of between 8 and 20nm.

Figure 11b shows a 40µm x 40µm scan of a wafer surface post etch, with an initial peak to valley roughness of 200nm and a post etch roughness of 6nm, clearly showing minimization of the grind pattern.

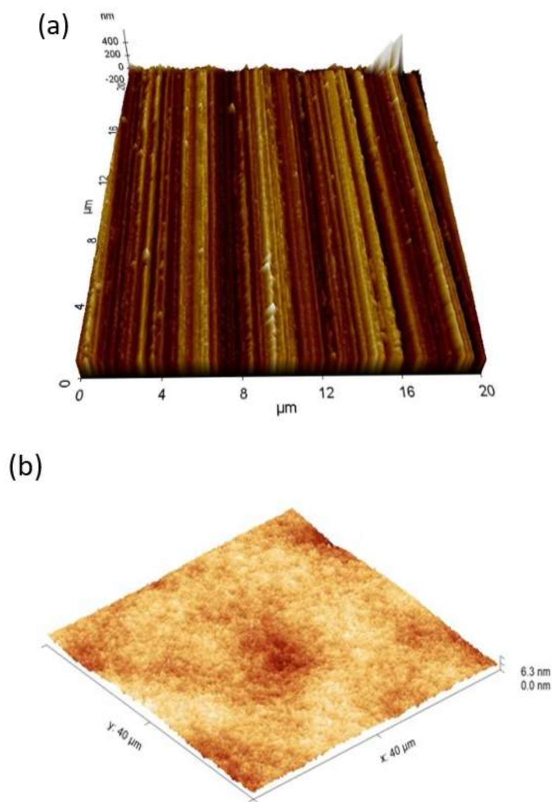

Figure 11: *(a) AFM scan of a back-ground wafer pre-smoothing on a 20µm x 20µm scale showing quasi-parallel grind marks and undulations with initial roughness of approximately 200nm (b) AFM of a wafer post Grow & Mow process on a 40µm x 40µm scale showing elimination of grind marks and a final roughness of <10nm*

Table II shows that there is a substantial reduction in localized roughness and a significant, if smaller improvement in R_a with the optimized smoothing process, leading to comparable levels of surface roughness with respect to conventionally polished silicon.

TABLE II
SURFACE ROUGHNESS (PEAK TO VALLEY) AND R_A VALUES

Surface	**Roughness (Peak to Valley) nm**	**R_a nm**
Polished Silicon	5.6	0.49
Poligrind	80-100	2.63
Fine Grind	180-200	8.79
Post “Grow & Mow” Smoothing	6	1.89

VI CONCLUSION

A replacement CMP process has been developed using an all-dry plasma etch. The patented [4], optimized process uses an initial step to remove regularly spaced, quasi-parallel linear grind marks, followed by a second smoothing process in a loop. There were two separate issues to consider while developing this process. Firstly, the actual smoothing of the silicon surface lowering roughness to below 10nm. Secondly, and more importantly, the optical properties of creating interference-type effects. Here very shallow trenches with a period between peaks large enough to disrupt light incident to the surface of the wafer cause image distortion. This means that when inspecting wafers post TSV reveal the grind marks are still visible and are wrongly categorized as defects leading to false yield loss.

Existing work looking at TSV reveal or smoothing processes using dry etch techniques have not specifically addressed the subject of post back-grind damage and the visibility of the grind-marks as a direct CMP replacement and report much longer smoothing times than the process described here [15, 21, 22], or looked at achieving smooth vertical sidewalls during TSV formation.

Neither of the two steps processed in isolation achieve a smooth wafer surface and grind marks remain visible after etching. However, the novel combined approach of randomly roughening the surface, before subsequent smoothing, destroying the regular pattern caused by the bulk grind and then producing a mirror finish surface was highly effective, which is not seen in other smoothing etches.

It is believed that the “Grow” step creates a roughened surface resulting in a hazy or milky surface. Rather than a build-up of material on the surface, the unbiased O_2/SF_6 uses random, localised micro masking to etch small pits in the wafer surface and create a large number of protrusions from the wafer surface [4]. This disrupts the regular grind marks left by the rough back-grind process.

The pitted surface created by the “Grow” step is subsequently “Mown” by the low pressure, high bias argon / SF_6 step [4]. The pits are dimensionally of the same order (100nm) as the roughness induced by the grind, and the process affects the wafer plane surface to a greater extent than the valleys of the grind marks and at least partial etches the protrusions [4]. With repeated cycling of Grow and Mow steps, along with parameter ramping, the surface is planarized and the grind marks are eliminated.

The process scheme successfully eliminated grind marks and produced a flat surface with roughness (6nm) comparable to a CMP treated wafer of 5.6nm (Table II). The process is completed in 320 seconds, allowing some process flexibility within the 600 seconds originally allowed. The process removed the target silicon loss of 2µm and uses the gases and process module needed for the subsequent TSV reveal step. The process is highly repeatable, and any gases can be abated. The process has been implemented in manufacturing, replacing an existing CMP step.

There are several process-flows for which this novel process provides advantages. This includes MEMS such as microneedles [18], where existing topography needs to retain its shape after smoothing, which is not possible using traditional

CMP. Another use would be to polish thinned, or ultra-thinned wafers prior to plasma Dicing After Grind (DAG) to improve die strength where CMP would contribute to chipping and cracking [32].

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