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An Optimized Switching Strategy Based on Gate Drivers with Variable Voltage to Improve the Switching Performance of SiC MOSFET Modules

Jixiang Tan * and Zhongfu Zhou

Department of Electronic and Electrical Engineering, Faculty of Science and Engineering, Swansea University Bay Campus, Swansea SA1 8EN, UK; z.zhou@swansea.ac.uk
* Correspondence: 979921@swansea.ac.uk

Abstract: This paper proposes an optimized switching strategy (OSS) based on a silicon carbide (SiC) MOSFET gate driver with variable voltage, which allows simultaneous variations in several different parameters to optimize the switching performance of semiconductor devices. As a relatively new device, the SiC MOSFET shines in the field of high power density and high-frequency switching; it has become a popular solution for electric vehicles and renewable energy conversion systems. However, the increase in voltage and current slope caused by high switching speeds inevitably increases the overshoot and oscillation in a circuit and can even generate additional losses. The principle of this new control strategy is to change the voltage and current in the turn-on and turn-off stages by changing the gate driver's voltage. That is, we reduced the drive's voltage after a certain time delay and maintained it for a period of time, thus directly controlling the slopes of di/dt and dv/dt. This study focused on the optimization of the SiC MOSFET by changing the time delay preceding the decrease in the voltage of the gate driver, analyzing and calculating the optimal time delay before the decrease in the voltage of the gate driver, and verifying the findings using LTspice simulation software. The simulated results were compared and analyzed with hard-switching strategies. The results showed that the proposed OSS can improve the switching performance of SiC MOSFETs.

Keywords: optimal-switching strategy; gate driver circuit; silicon carbide MOSFET; voltage and current overshoot; LTspice

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1. Introduction

Silicon carbide (SiC) MOSFETs offer a range of advantages over silicon-based switches, including faster switching, higher efficiency, higher operating voltages, and higher temperatures, enabling smaller and lighter designs [1,2]. Thus, significant progress has been made in the power semiconductor industry. These advantages allow SiC MOSFETs to be applied in a range of automotive and industrial applications. However, the excessively fast switching speed of SiC MOSFETs causes high values of di/dt and dv/dt [3]. At the same time, due to the existence of parasitic inductance and parasitic resistance in circuits, SiC MOSFETs are prone to overshoots and oscillations in current and voltage during switching, thus generating additional switching losses. These losses can even cause device damage. Therefore, reducing or even eliminating the overshoot, oscillation, and electromagnetic interference (EMI) of silicon carbide MOSFETs during switching is a priority in improving their working efficiency [4].

Current and voltage overshoots are the biggest obstacles in SiC semiconductor applications. Stray inductance and parasitic capacitance are the main contributors to current and voltage overshoots [5,6]. When a SiC MOSFET works at a high frequency, the switching speed becomes too fast and the di/dt and dv/dt slopes increase. Thus, current and voltage overshoots are amplified due to stray inductance and parasitic capacitance [7]. When the voltage and current overshoots exceed the breakdown voltage of the SiC MOSFET and the

maximum recovery current of the freewheeling diode, the SiC is destroyed. However, the parasitic elements in the actual circuit cannot be eliminated [8–11]; so, the overshoot can only be eliminated by other means.

Solving the problems of overshoots and oscillations is key to improving the efficiency of SiC MOSFETs.

In the traditional approach, slowing the switching speed in the case of high gate resistance [12] can alleviate the SiC MOSFET's overshoots and oscillations. However, this solution means the power losses become greater with longer switching times [6]. Adding an RC snubber circuit is also a common method [13,14] to eliminate overshoot and oscillation problems. Although highly efficient snubber circuits have been proposed, snubber circuits affect the overall efficiency of the system. In particular, extra devices increase the power loss of the overall circuit. Active gate driver (AGD) solutions have been developed to increase the efficiency of power devices. The main advantages of these gate drivers are reduced oscillations and overshoots. However, the extra components not only increase the volume of the SiC system but also increase the circuit's power loss [15–21]. In [21], a new active gate driver was proposed that could effectively suppress overshoots and oscillation and reduce losses without compromising EMI. The main strategy of the proposed AGD was to reduce the current and voltage slope by reducing the gate driver's voltage. However, its main disadvantages were that the process of calculating the parameters of the transformer was complicated, an additional printed circuit board was required, and the implementation of the circuit was complicated and expensive. As such, configurable digital gate drivers (DGDs) are the latest technological development in this sphere [22]. The strengths of DGDs are their programmability, support for a wide variety of power devices, and ease of use [23]. A key element of this technology is the ability to configure the turn-on and turn-off processes, which provides a series of steps to control the voltage level at specific times [24–28]. This allows designers to digitally configure the turn-on and turn-off curve through software without requiring changes to the hardware.

In this paper, an optimized switching strategy based on gate drivers with variable voltage (OSS) was proposed to improve the switching performance of SiC MOSFETs. This switching strategy was based on and optimized for an AGD in [21] and a DGD in [22]. There is no doubt that the AGD performed well in [21]. However, the gate driver circuits were too complex and too large. The ease of operation of the DGD in [22] is very attractive. Therefore, this article aimed to combine the advantages of the voltage gate drivers of AGDs and DGDs in waveforms to further optimize the algorithm and control and reduce overshoots and oscillations in SiC MOSFETs through an OSS. Finally, we used the LTspice simulation software to verify the feasibility of our switching strategy. Compared with AGDs and DGDs, an OSS can control more variables to achieve more precise and optimal circuit control. Due to space limitations, this article focused on the impact of delay time on switching performance and lists the formula to calculate the delay time for a given calculated decrease in voltage. At the same time, the decrease in the voltage and the time of this decrease were also considered. The development potential of the OSS is significant. Compared with other switching strategies, which can only change one or two variables, the OSS can control three variables simultaneously, namely, the delay time before a decrease in voltage, the decrease in voltage itself, and the time duration of the decrease in voltage. More variables mean better control performance. However, due to various limitations, this paper only considered the influence of the delay time before a decrease in voltage on switch performance and analyzed the relationship between voltage drop and switch performance. In our next work, we will produce more simulations and experimental results to prove the advanced nature of the OSS.

This paper is organized as follows. Sections 2 and 3 present the control principle, circuit model, and related formulations of the proposed switching strategy. In Section 4, the simulation setup and simulation results are introduced and analyzed. Finally, in Section 5, the conclusions and a discussion of this simulation are given.

2. Operation Principle of the OSS

The working principle of the OSS is to improve the switching performance of the SiC MOSFET by controlling the voltage drop delay time, voltage drop, and voltage drop time. Compared with traditional AGDs and DGDs, the advantage of an OSS is that it has more control parameters, which means that the semiconductors can be optimally controlled. In this section, the general schematic circuit and working principle of the proposed OSS will be introduced in detail. Figure 1 shows a circuit schematic of the SiC MOSFET and Figure 2 shows a timing chart of the SiC MOSFET with an optimized switching strategy.

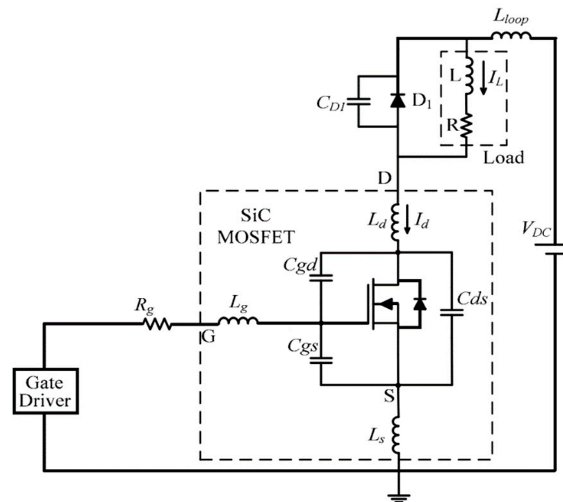

Figure 1. Circuit schematic of the SiC MOSFET under test.

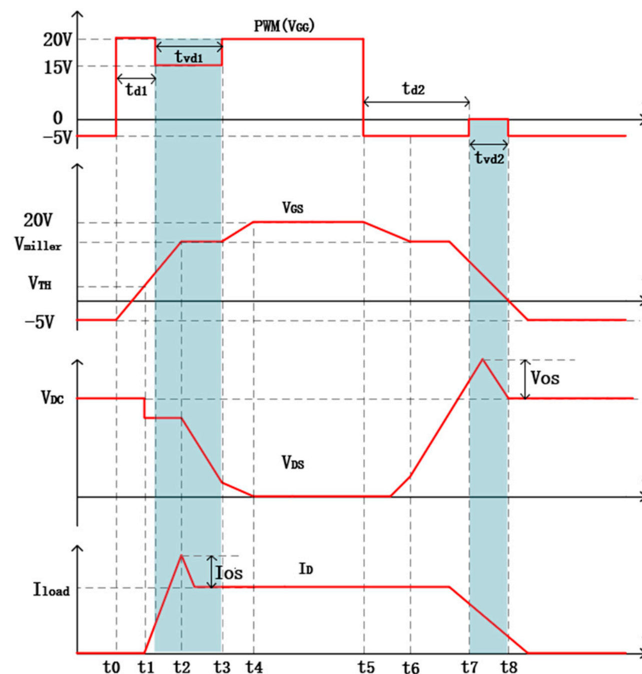

Figure 2. Timing chart of the SiC MOSFET with the OSS.

2.1. Operation Modes

As shown in Figure 1, the OSS circuit was mainly composed of three parts: the gate drive circuit, silicon carbide MOSFET, and DC bus power supply. The model of the SiC MOSFET, including junction capacitances (C_{gd}, C_{gs}, C_{ds}) and module intrinsic parasitic inductances (Ls, Lg, Ld), is also depicted in Figure 1.

In [21], the gate drive voltage used by the AGD was 20 V/−5 V; also, 15 V and 0 V were used as dropped voltages to optimize the switching performance of the SiC MOSFET. Because it used a switching bridge, it could generate four gate drive voltages (i.e., 20 V, 15 V, 0, and −5 V) from two drive power supplies (20 V and 5 V) through different combinations. In this design, the gate drive voltage waveform design of the AGD was still used. The purpose was to control variables and only explore the influence of the voltage drop delay time (t_d) on the performance of SiC MOSFETs.

2.2. Operation Principle

Figure 2 shows the timing chart of the SiC MOSFET with an optimized switching strategy. The whole process could be split into two steps: turn on and turn off. The blue interval represents the gate driver voltage in the stage of the voltage drop delay time.

2.2.1. Turn-On Stage

When the pulse width modulation (PWM) signal changed from low to high at t_0, a high value gate drive voltage V_{GG} of 20 V was applied to the SiC MOSFET. Then, a high gate current was generated to charge the input capacitance $C_{iss} = C_{gs} + C_{gd}$ with R_g, which meant the V_{GS} started to increase. When the V_{GS} reached the threshold voltage V_{TH} at t_1, the I_D began to conduct. After a time delay t_{d1}, the lower V_{GG} was activated and a lower gate current was generated because the V_{GG} was reduced to 15 V.

In this interval, I_D continued to rise and a current peak value I_{OS} appeared due to the freewheeling diode effect. The V_{GS} reached the Miller plateau voltage and stopped rising. At the same time, the V_{DS} started to drop. After the voltage fall time t_{vd1}, the V_{GS} came out of the Miller plateau and continued to rise. Finally, the SiC MOSFET was fully turned on at t_4. From [21], the current slope of I_D and the voltage slope of the V_{DS} during the turn-on stage could be expressed as:

$$\frac{dI_D}{dt} = \frac{V_{GG} - V_{TH} - I_D/g_m}{(C_{iss} \cdot R_{on})/g_m + L_s} \tag{1}$$

$$\frac{dV_{DS}}{dt} = -\frac{V_{GG} - V_{Miller}}{C_{GD} \cdot R_{on}} \tag{2}$$

where g_m is the transconductance of the SiC MOSFET and C_{gd} is the gate-drain capacitance of the SiC MOSFET.

2.2.2. Turn-Off Stage

When the signal from the voltage source changed from high to low at t_5, a negative voltage (i.e., −5 V) was generated to discharge the C_{iss} with R_g. The V_{GS} started to drop from 20 V until it reached the Miller voltage at t_6. The V_{DS} rose rapidly and caused a voltage overshoot V_{OS} due to stray inductance. After a delay time t_{d2}, the V_{GG} increased to 0 V and remained there until I_D was fully turned off at t_8. After t_8, the gate voltage stabilized at −5 V to ensure that the SiC MOSFET was always in the off state. The voltage slope could be calculated as:

$$\frac{dI_D}{dt} = g_m \cdot \frac{V_{TH} + (I_D/g_m) - V_{GG}}{(C_{iss} \cdot R_{off})/g_m + L_s} \tag{3}$$

$$\frac{dV_{DS}}{dt} = \frac{V_{GG} - V_{Miller}}{C_{GD} \cdot R_{off}} \tag{4}$$

According to (1)–(4), changing the instantaneous slope of current and voltage could be achieved by changing the V_{GG}. In the turn-on stage, the change was reducing the gate diver voltage while in the turn-off stage, the change was increasing the gate diver voltage.

3. Calculation for Voltage Drop Delay Time

An OSS can change the switching performance through unlimited control of the voltage drop delay time, voltage drop, and voltage drop time, aiming to obtain the best data for the switching performance through countless permutations and combinations. However, this is difficult to carry out. In fact, the best data can be derived by equation. The main research direction of this paper was to explore the influence of the voltage drop delay time on the switching performance and to explore the influence of different voltage drops and different voltage drop times on the switching performance. Thus, the content of this chapter focuses on deriving the best voltage drop delay time by equation.

3.1. Equivalent Slope for Current and Voltage

The slope of the current and voltage is an important factor affecting the overshoot and oscillation during the switching process of the SiC MOSFET. It can be seen from Figure 2 that the I_{OS} in the turn-on stage and the V_{OS} in the turn-off stage were obvious and large. However, the slope of the voltage and current in the SiC MOSFET with the OSS method was not constant because of the variable gate drive voltage; so, the equivalent slope was proposed and applied in the calculation, with the aim of writing the voltage drop delay times, t_{d1} and t_{d2}, into the equation.

In Figure 3, when the V_{GG} was 20 V, the slope of the current was dI_D/dt_1; when the V_{GG} was 15 V, the slope of the current was dI_D/dt_2. Similarly, dV_{DC}/dt_1 and dV_{DC}/dt_2 represented the value of the voltage slope under the V_{GG} of −5 and 0 V. In addition, ton represented the increase in the current I_D and toff represented the increase in the voltage V_{DS}; t_{on1} and t_{off1} were the rising times under dI_D/dt_1 and dV_{DC}/dt_1, respectively. Moreover, dI_D/dt represented the actual current slope with OSS and dV_{DC}/dt was the current slope with OSS, in actuality. Additionally, dI_D/dt_{eq} was the equivalent slope at the turn-on stage and dV_{DC}/dt_{eq} represented the equivalent slope at the turn-off stage; t_{on2} and t_{off2} were the actual running times for the turn-on stage and turn-off stage. In [21], the slope of the current was used in both the turn-on and turn-off stages because it was convenient for the subsequent calculations. In this paper, in order to fit reality, the voltage slope was used in the turn-off stage. According to the equivalent principle shown in Figure 3, the following equation could be obtained:

$$I_L = |dI_D/dt_1| \cdot t_{on} + |dI_D/dt_1| \cdot (t_{d1} - t_{on}) + |dI_D/dt_2| \cdot (t_{on2} - t_{d1}) = \left|dI_D/dt_{eq}\right| \cdot t_{on2} \quad (5)$$

and the equivalent rising time t_{on2} of the current can be expressed as:

$$t_{on2} = (I_L - (|dI_D/dt_1| - |dI_D/dt_2|) \cdot t_{d1}) / |dI_D/dt_2| \quad (6)$$

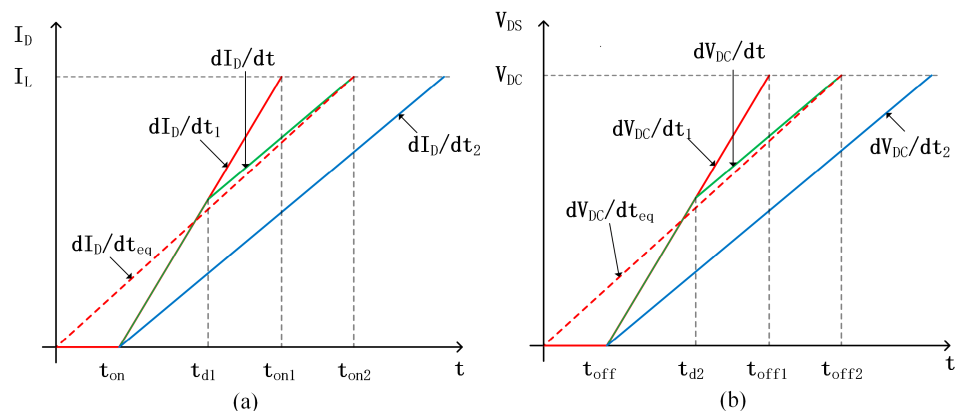

Figure 3. Schematic diagram of the equivalent slope. (**a**) Current slope on the turn-on stage. (**b**) Voltage slope on the turn-off stage.

Thus, according to (5) and (6), the value of the equivalent current slope at the turn-on stage can be expressed as:

$$\left|dI_D/dt_{eq}\right| = I_L \cdot |dI_D/dt_2| / (I_L - (|dI_D/dt_1| - |dI_D/dt_2|) \cdot t_{d1}) \tag{7}$$

Similarly, at the turn-off stage, the equations of t_{off2} and voltage slope are:

$$V_{DC} = |dV_{DS}/dt_1| \cdot t_{off} + |dV_{DS}/dt_1| \cdot (t_{d2} - t_{off}) + |dV_{DS}/dt_2| \cdot (t_{off2} - t_{d2}) = \left|dI_D/dt_{eq}\right| \cdot t_{off2} \tag{8}$$

$$t_{off2} = (V_{DC} - (|dV_{DS}/dt_1| - |dV_{DS}/dt_2|) \cdot t_{d2}) / |dV_{DS}/dt_2| \tag{9}$$

$$\left|dV_{DS}/dt_{eq}\right| = V_{DC} \cdot |dV_{DS}/dt_2| / V_{DC} - (|dV_{DS}/dt_1| - |dV_{DS}/dt_2|) \cdot t_{d2} \tag{10}$$

3.2. Power Losses in the Turn-On and Turn-Off Stages

The turn-on and turn-off losses of the power device could be calculated by (11) and (12), which were derived in []:

$$E_{ON} = E_{on,dI_D/dt} + E_{on,dV_{DS}/dt} + E_{Irr} + E_{Ls} \tag{11}$$

$$E_{OFF} = E_{off,dI_D/dt} + E_{off,dV_{DS}/dt} + E_{Ls} \tag{12}$$

where E_{Ls} is the energy generated by the current passing through L_S and E_{Irr} is the energy loss of the device generated by the reverse recovery effect, which can be calculated by (14) [29]:

$$E_{Ls} = \frac{1}{2} \cdot L_S \cdot {I_{loop}}^2 \tag{13}$$

$$E_{Irr} = \left(I_L \cdot \sqrt{Q_{rr}/|dI_D/dt|} + Q_{rr}\right) \cdot V_{DC} \cdot (1 - \sigma) \tag{14}$$

where L_{loop} is the stray inductance in the power loop, Q_{rr} is the reverse recovery charge, and σ is the overshoot ratio, which can be defined as:

$$\sigma = \frac{V_{OS}}{V_{DC}} = \frac{L_{loop} \cdot |dI_D/dt|}{V_{DC}} \tag{15}$$

During the turn-on transient processes, the energy losses during the current and voltage changes can be expressed as:

$$E_{on,dI_D/dt} = \frac{1}{2} \cdot I_L \cdot \left(V_{DC} - L_{loop} \cdot |dI_D/dt|\right) \cdot \frac{I_L}{|dI_D/dt|} \tag{16}$$

$$E_{on,dV_{DS}/dt} = \frac{1}{2} \cdot I_L \cdot V_{DC} \cdot \frac{V_{DC}}{|dV_{DS}/dt|} \cdot (1 - \sigma)^2 \tag{17}$$

Therefore, according to Formulas (11) and (13)–(17), the energy loss during the turn-on stage can be expressed as:

$$E_{ON} = \frac{V_{DC} \cdot {I_L}^2}{2} \cdot \left(\frac{1 + (1 - \sigma)^2}{|dI_D/dt|}\right) + \left(I_L \cdot \sqrt{\frac{Q_{rr}}{|dI_D/dt|}} + Q_{rr}\right) \cdot V_{DC} \cdot (1 - \sigma) - \frac{1}{2} \cdot L_S \cdot {I_{loop}}^2 \tag{18}$$

Similarly, according to (12), the energy loss can be expressed as:

$$E_{OFF} = \frac{I_L \cdot {V_{DC}}^2}{2} \cdot \frac{1 + (1 + \sigma)^2}{|dV_{DS}/dt|} + \frac{1}{2} \cdot L_S \cdot {I_{loop}}^2 \tag{19}$$

3.3. Calculation of the Voltage Drop Delay Time

In order to simplify the calculation model, it was assumed that the change of power consumption was only related to overshoot and was positively correlated. Therefore, during the turn-on stage of the SiC MOSFET, the change in power consumption is positively correlated with the change in current overshoot [21]. Similarly, in the turn-off phase, the change of power consumption is positively correlated with the change of voltage overshoot. The formula can be expressed as:

$$\frac{|E_{ON}\ (t_{d1}) - E_{ON}\ (0)|}{|E_{ON}\ (t_{on2}) - E_{ON}\ (0)|} = \frac{|I_{OS}(t_{d1}) - I_{OS}(0)|}{|I_{OS}(t_{on2}) - I_{OS}(0)|} \quad (20)$$

$$\frac{|E_{OFF}\ (t_{d2}) - E_{OFF}\ (0)|}{|E_{OFF}\ (t_{off2}) - E_{OFF}\ (0)|} = \frac{|V_{OS}(t_{d2}) - V_{OS}(0)|}{|V_{OS}(t_{off2}) - V_{OS}(0)|} \quad (21)$$

In the turn-on phase, the most important factor affecting power consumption is the overshoot of the current; so, Equation (21) can be abbreviated as:

$$E_{ON} = \frac{{I_L}^2 \cdot V_{DC}}{2} \cdot \frac{1 - \sigma}{|dI_D/dt|} \quad (22)$$

Because the main cause of current overshoot is the reverse recovery effect [21], the current overshoot can be expressed as:

$$I_{OS} = I_{rr} = \sqrt{Q_{rr} \cdot |dI_D/dt|} \quad (23)$$

According to (25) and (26), (11) can be expressed as:

$$\frac{|dI_D/dt_{eq}|}{|dI_D/dt_1|} = \frac{\sqrt{Q_{rr} \cdot |dI_D/dt_1|}}{\sqrt{Q_{rr} \cdot |dI_D/dt_{eq}|}} \quad (24)$$

Similarly, in the turn-off stage, the formula can be obtained:

$$E_{OFF} = \frac{{V_{DC}}^2 \cdot I_L}{2} \cdot \frac{1 + \sigma}{|dV_{DS}/dt|} \quad (25)$$

$$\frac{|dV_{DS}/dt_{eq}|}{|dV_{DS}/dt_1|} = \frac{L_{loop} \cdot |dV_{DS}/dt_1|}{L_{loop} \cdot |dV_{DS}/dt_{eq}|} \quad (26)$$

According to (1)–(4), (7), and (24), an equation expressed by t_{d1} could be obtained. Similarly, according to (1)–(4), (10), and (26), an equation expressed by t_{d2} could be obtained. Therefore, the optimal voltage drop delay times, t_{d1} and t_{d2}, could be calculated.

4. Simulation Verification

In order to evaluate the performance of the proposed OSS, a double-pulse simulation test of the SiC MOSFET was performed using the software LTspice. The power device used in the test was CREE's 1.2 KV/115 A SiC MOSFET module (C3M0016120D). In the simulation, the tested module was first modeled in LTspice to ensure that the simulation results would be closer to the experimental data and then the circuit was built and simulated. The detailed parameters of the tested modules in the experiment are shown in Table 1.

The comparison of the OSS's performance under different time delays was simulated to verify whether the calculated time delay was the best. To further compare the performance of the OSS, it was compared with hard switching (HS) and a digital gate driver (DGD) from Agileswitch.

Table 1. Parameters of the SiC MOSFET C3M0016120D (TCJ = 25 °C).

Symbol	Parameter	Value	Unit
V_{DS} V_{GS} V_{TH}	Drain—Source Voltage Gate—Source Voltage Gate Threshold Voltage	1200 −8/+19 2.5	V
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	6085 230 13	pF
t_r	Rise Time	28	ns
t_f	Fall Time	27	ns
$R_{DS(on)}$	Drain-Source On-State Resistance	16	mΩ
$R_{G(int)}$	Internal Gate Resistance	2.6	Ω
I_D	Continuous Drain Current	115	A
Qrr	Reverse Recovery Charge	604	nC
gm	Transconductance	53	S

4.1. SiC MOSFET Device

In order to facilitate future experiments based on this simulation, this simulation used the existing silicon carbide semiconductor module in the laboratory as the test equipment. The detailed parameters of the tested modules in the experiment are shown in Table 1. Figure 4 shows the device.

Figure 4. C3M0016120D device.

4.2. Simulation Modeling

To improve the simulation, we chose LTspice as the simulation software. As shown in Figure 5, and according to Figure 1, a simulation circuit was built. The main purpose of this simulation was to verify the effect on the switching performance of the OSS and compare it with other switching strategies. It was firstly particularly important to verify whether it was necessary to study the OSS in depth. A simulation can obtain more accurate results and save time. Once the excellent switching performance of the OSS was confirmed, the next step was to build and experiment with actual circuits. According to (24), (26), and data from Table 1, we calculated an optimized delay time t_{d1} of 21 ns and t_{d2} of 41 ns; t_{vd1} and t_{vd2} used the rise time (t_r) and fall time (t_f) in the device data sheet for the simulation, respectively.

Table 2 shows the parameters of some components in the analog circuit. Among them, C_1 and C_4 represent C_{ds}, C_2 and C_5 represent C_{dg}, and C_3 and C_6 represent C_{gs}. In order for the oscillation in the simulation results to be closer to the actual situation, L_S, L_D, and L_G were adjusted.

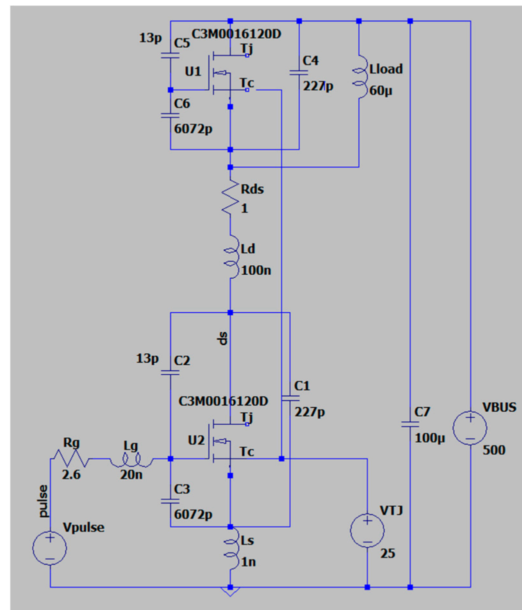

Figure 5. Simulation circuit in Ltspice.

Table 2. Parameters of the SiC MOSFET and associated circuit in LTspice.

Parameters	Value
C_1, C_4	227 pF
C_2, C_5	13 pF
C_3, C_6	6072 pF
C_7	100 µF
L_D	100 nH
L_G	20 nH
L_S	1 nH
L_{load}	60 µH
$R_{DS(on)}$	1 Ω
R_G	2.6 Ω
V_{BUS}	500 V
V_{TC}	25 V

Because the double-pulse simulation of the SiC MOSFET was carried out using the software LTspice, it was necessary to simulate the double-pulse signal, as shown in Figure 6. Because of the convenience of the simulation software, the voltage waveform from the voltage source could be edited directly. When the SiC MOSFET was simulated with the OSS, the waveform could also be adjusted directly at the voltage source, which required corresponding devices in the actual experiments.

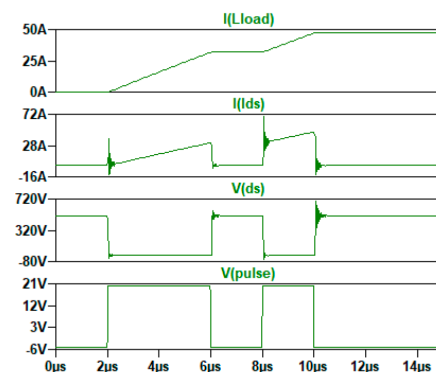

Figure 6. Switching waveforms for the SiC MOSFET with double-pulse switching.

4.3. Simulation Results

In order to verify the feasibility of the proposed OSS, the simulation was run with the gate resistance 2.6 Ω, both at the turn-on stage and turn-off stages; the dc bus voltage was 500 V and the drain current was 30 A. The voltage drop delay times t_{d1} of 21 ns and t_{d2} of 41 ns were calculated by Equations (11) and (12). Meanwhile, as visible from Table 1, the t_{vd1} was 28 ns and the t_{vd2} was 27 ns.

It can be seen in Figure 7a that when the turn-on signal arrived, first, a high V_{GG} (i.e., 20 V) was applied to the gate terminal. After the delay time t_{d1}, which was calculated to be 21 ns, the I_{DS} started to rise and the V_{GG} dropped to 15 V. After the delay time t_{vd1} (i.e., 28 ns), the high V_{GG} restarted to charge the SiC MOSFET. At the turn-off stage, the SiC MOSFET was first discharged by −5 V. After the delay time t_{d2}, which was calculated to be 41 ns, the V_{DS} started to rise from 0 V and the V_{GG} became 0 V. After the delay time t_{vd2} (i.e., 27 ns), the V_{DS} reached the peak value and the negative V_{GG} was discharged again.

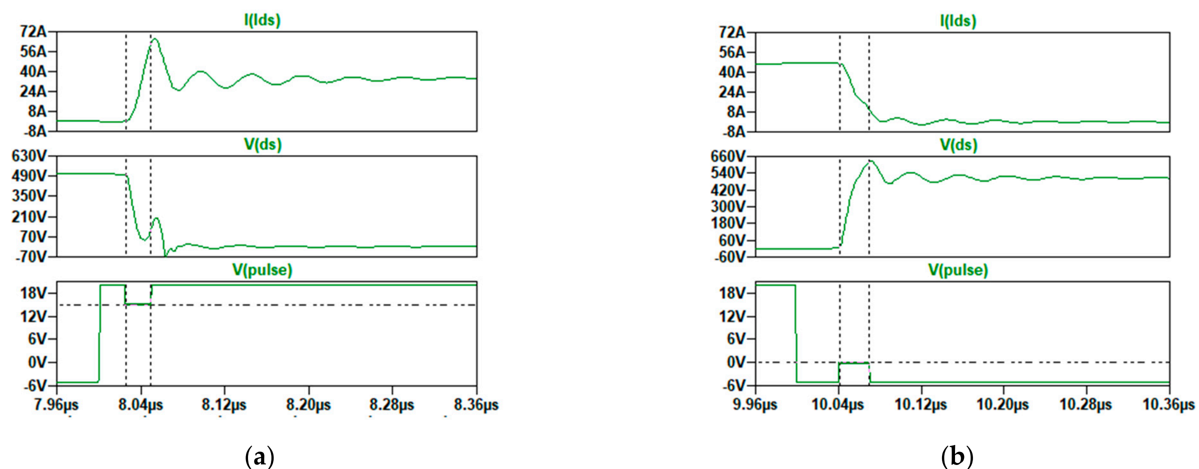

Figure 7. Switching waveforms for the SiC MOSFET with the OSS. (**a**) Turn-on stage, (**b**) turn-off stage.

As mentioned in Section 2, the voltage drop delay times, t_{d1} and t_{d2}, are very important because they can affect the switching performance of the SiC MOSFET. In order to verify the relationship between the delay time and the performance of the switch, and to further the accuracy of the calculation results in the previous chapter, more experiments were carried out. As shown in Figure 8, around the calculation result (i.e., t_{d1} = 21 ns t_{d2} = 41 ns) at an interval of 10 ns, a total of four other data points were taken before and after each transition and were simulated. Then, the simulation results were compared.

For the turn-on transition, because the calculation result of t_{d1} was 21 ns, the five testing data points were 11 ns, 21 ns, 31 ns, 41 ns, and 51 ns, respectively. The reason t_{d1} was not set to 0 was that this waveform was equal to the switching strategy of the digital gate driver. It can be seen from Figure 8a that there was no obvious difference and the V_{DS} and I_{DS} waveforms generated by the five different t_{d1} were not notably different. When t_{d1} was 11 ns, the overshoot of the I_{DS} was the smallest but the overshoot produced by the V_{DS} was the largest.

For the turn-off transition, since the calculation result of t_{d2} was 41 ns, the five test data points were 31 ns, 41 ns, 51 ns, 61 ns, and 71 ns, respectively. It can be seen from Figure 8b that there was an obvious difference and the V_{DS} and I_{DS} waveforms produced by the five different t_{d1} showed little difference. When t_{d1} was 41 ns, the overshoot and oscillation of the I_{DS} were the smallest; the overshoot and oscillation of the V_{DS} were also the smallest.

As the delay time increased or decreased, the calculation results in both cases were the best. However, a trade-off between the V_{DS} and I_{DS} could be achieved when a t_{d1} of about 21 ns at turn on and t_{d2} of about 41 ns at turn off were, respectively, applied.

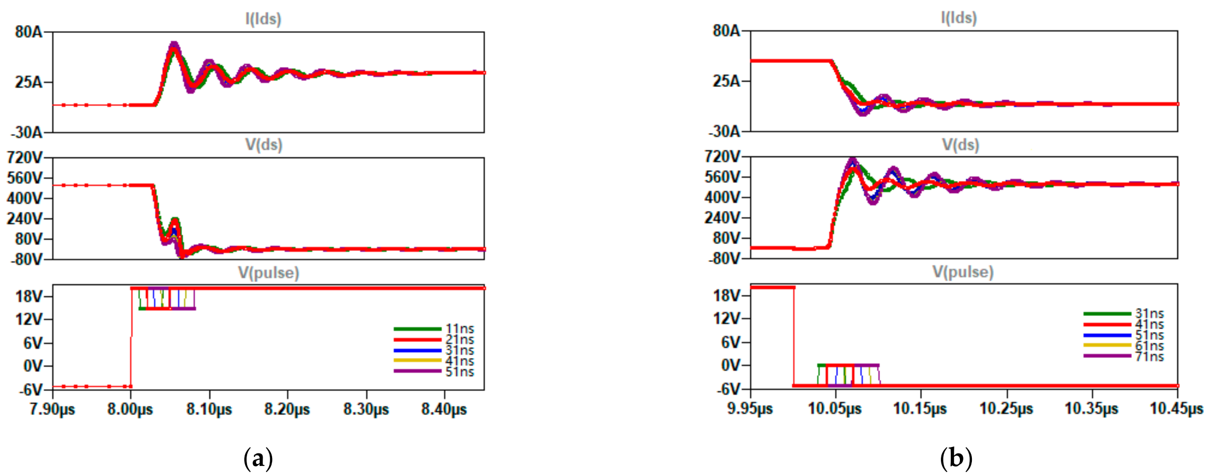

Figure 8. The switching performance of the SiC MOSFET with different gate voltage drop time delays. (**a**) Turn-on stage, (**b**) turn-off stage.

4.4. Comparison with Other Switching Strategies

After determining the optimal time delay of the OSS, it was necessary to compare the OSS with other switching strategies. First, we compared the OSS with the hard-switching (HS) strategy to confirm its advantages and improvements. Then, we compared it with a digital gate driver (DGD), which is widely used in teaching and research, to further verify the advantages of the OSS. A detailed experimental comparison of these different switching strategies follows.

4.4.1. Compared to the Hard-Switching Strategy

In order to demonstrate the excellent switching performance of the OSS in terms of overshoot and oscillation, more simulations were performed and the results were compared with the switching performance of hard switching. It can be seen from Figure 9a that during the turn-on stage, the peak value of the I_{DS} dropped from 70.04 A to 60.23 A, a decrease of 14%, and the oscillation was also significantly reduced. However, the overshoot of the V_{DS} increased, which will increase the power loss; although, this will not affect the peak value of the V_{DS}.

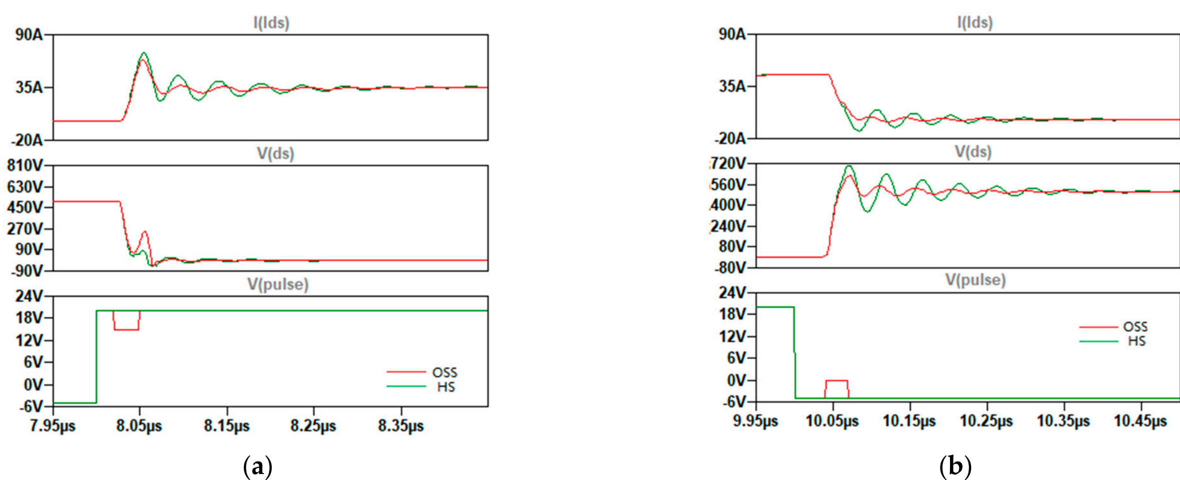

Figure 9. Switching performance comparison of the SiC MOSFET between HS and the OSS. (**a**) Turn-on stage, (**b**) turn-off stage.

Unlike in the turn-on process, the OSS successfully reduced the oscillation and peak value during the turn-off process, not only regarding the I_{DS} but also the V_{DS}. It can be

seen from Figure 9b that the overshoot of the V_{DS} reduced from 704.56 V to 577.52 V, a drop of 18.03%.

Combining the two processes of turn on and turn off, it can be clearly seen that the OSS effectively reduced the overshoot and oscillation of the I_{DS} and V_{DS} in the SiC MOSFET switch, thereby reducing the overshoot and power consumption of the entire circuit.

4.4.2. Compared to Digital Gate Driver

The digital gate drive system from Agileswitch is a product with a wide range of applications. It can control the voltage drop and voltage drop time of the gate voltage without limitation to affect the switching performance of semiconductors. The control strategy of the DGD is also very advanced. However, the existing DGD control strategy is still unable to design more complex gate drive waveforms, especially the voltage drop after a delay time, like an AGD. Therefore, it was necessary to compare the OSS with existing digital gate driver strategies.

Figure 10 shows the V_{DS} and I_{DS} comparison of the OSS and DGD at the same turn-on time. Compared with the hard-switching strategy, the overshoot of the DGD was reduced by 19%, which was better than the OSS's 14%. Although the DGD was slightly better at reducing the I_{DS} overshoot and oscillation, the overshoot of the V_{DS} was larger, which seriously increased the power losses of the circuit. Although the two switching strategies were both effective in reducing overshoot, they increased power consumption and were low in cost performance. This is why the first generation of DGDs cannot adjust the pulse shape during turn on.

Figure 10 shows the comparison of the V_{DS} and I_{DS} for the OSS and DGD at the same turn-off time. Compared with the hard-switching strategy, the DGD had no advantage and even increased power consumption due to the longer switch-off process.

In order to better compare two different switching strategies, the closing time of the DGD was extended from 68 ns to 88 ns and was then simulated and compared. The new waveform comparison is in Figure 11. Compared with Figure 10b, the DGD effectively suppressed the overshoot and oscillation of the V_{DS} and the overshoot was reduced by 11%. Compared with the OSS, the DGD was inferior. Continuing to extend the turn-off time of the DGD will make the optimization more effective; but, this will inevitably increase power consumption and reduce the frequency of the semiconductor device.

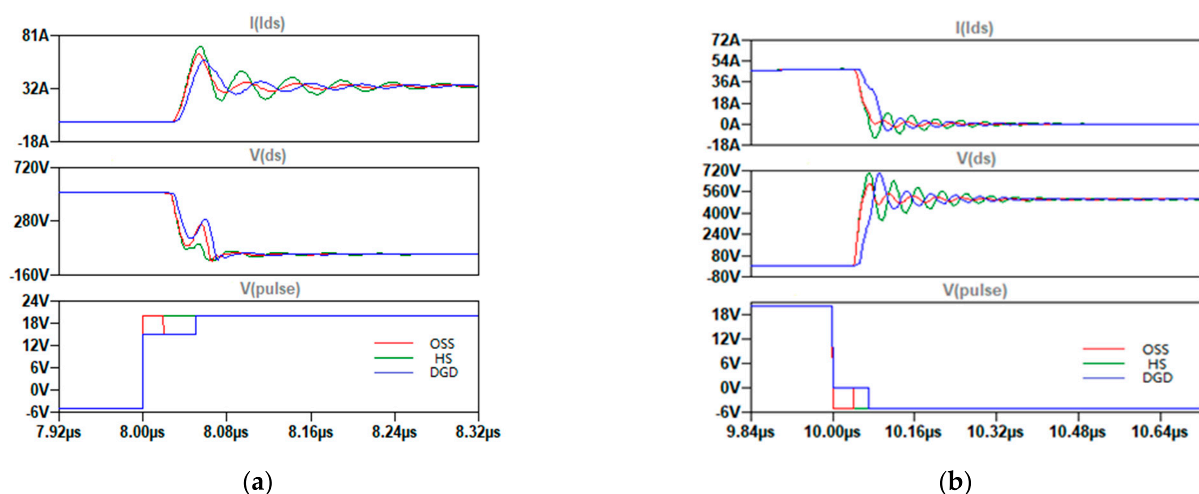

Figure 10. Switching performance comparison of the SiC MOSFET between the DGD, HS, and OSS. (**a**) Turn-on stage, (**b**) turn-off stage.

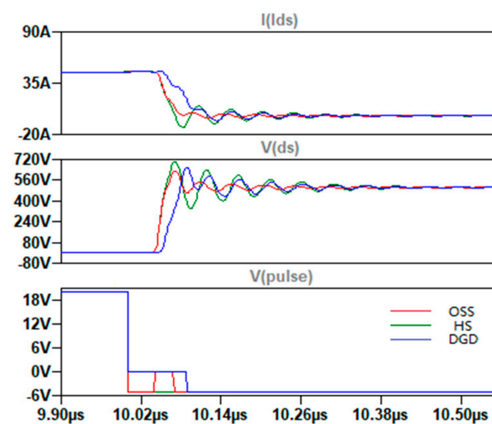

Figure 11. Turn-off switching performance comparison of the SiC MOSFET between the DGD, HS, and OSS when the the DGD time delay was 88 ns.

4.5. Comparison with Different Drop Voltages

The OSS can become more complex and diverse. The previous chapter mainly considered the influence of the voltage time delay on switching performance; this section attempts to study different voltage drops.

It can be seen from Figure 12 that, whether in the on state or the off state, the larger the voltage drop, the less overshoot. Because the increase in the voltage drop reduces the slope of the current and voltage, this proves that the formula in Section 3 is valid. However, during the turn-off process, with the increase in the voltage drop, the oscillation of the voltage and current was obviously increased.

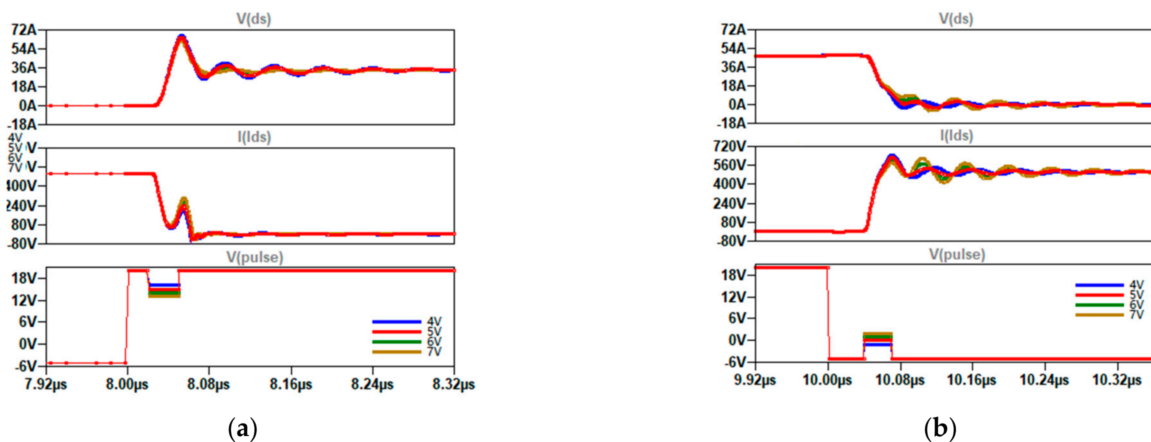

Figure 12. Switching performance of the SiC MOSFET with different drop voltages. (**a**) Turn-on stage, (**b**) turn-off stage.

4.6. Comparison with Different Voltage Drop Times

In the previous simulation, in order to simplify the complexity of the simulation, the voltage drop time (t_{vd}) used the rise time (t_r) and fall time (t_f) in the device datasheet. However, in the OSS, the voltage drop time is also an important parameter, similar to the delay time and voltage drop. Therefore, in this subsection, the effect of the voltage drop time on the switching performance was studied by simulation.

For the turn-on transition, because the t_r was 28 ns, five testing data points were chosen: 18 ns, 28 ns, 38 ns, 48 ns, and 58 ns. It can be seen from Figure 13a that different voltage drop times did not have much influence on the switching performance at the turn-on stage.

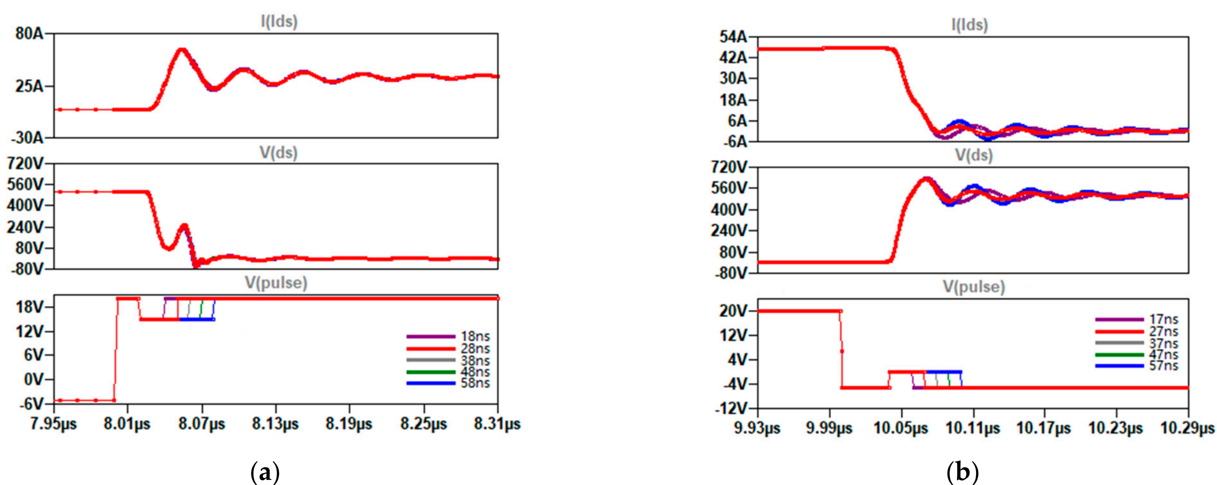

Figure 13. Switching performance of the SiC MOSFET with different voltage drop times. (**a**) Turn-on stage, (**b**) turn-off stage.

For the turn-off transition, because the t_f was 27 ns, five testing data points were chosen: 17 ns, 27 ns, 37 ns, 47 ns, and 57 ns. It can be seen from Figure 13b that in the turn-off stage, different voltage drop times had an impact on the switching performance. When the voltage drop time was 27 ns, the switching achieved the best performance. As the voltage drop time increased, the suppression effect of the OSS on voltage oscillations began to weaken. On the contrary, as the voltage drop time decreased, the voltage oscillation was suppressed; but, a larger reverse current was generated.

4.7. Power Loss Comparison

To determine whether a switching strategy is good or bad, in addition to observing whether it effectively reduces overshoot and oscillation, another important criterion is whether power consumption increases. Due to the advanced nature of LTspice, the product of current and voltage can be quickly integrated directly from the simulated circuit. Table 3 records the power losses from simulation models in one turn-on and turn-off round.

Table 3. Power losses for the simulations in LTspice.

Subsection	Switching Strategy	Power Losses (µJ)
4.4	HS	494.43
	OSS	520.21
	DGD	704.52
	DGD (extended)	681.03
4.5 Different voltage drop	Voltage drop 7 V	675.11
	Voltage drop 6 V	604.05
	Voltage drop 5 V	536.85
	Voltage drop 4 V	473.72
4.6 Different voltage drop time	Voltage drop time −10 ns	491.56
	Voltage drop time 0 ns	539.26
	Voltage drop time +10 ns	582.92
	Voltage drop time +20 ns	606.19
	Voltage drop time +30 ns	686.85
4.3 Different voltage drop delay time	Voltage drop delay time −10 ns	559.25
	Voltage drop delay time 0 ns	518.93
	Voltage drop delay time +10 ns	582.87
	Voltage drop delay time +20 ns	658.26
	Voltage drop delay time +30 ns	743.88

It can be seen from Table 3 that, compared with HS and the DGD, the power consumption of the OSS was slightly higher than that of HS. However, combined with Figure 11, the optimization effect of the OSS remained obvious.

In the comparison of different voltage drops, it can be concluded that the smaller the voltage drop, the smaller the power consumption. However, combined with Figure 12, it can be seen that the smaller the voltage drop, the smaller the suppression effect of the OSS on the circuit overshoot. Similarly, in the comparison of different voltage drop times, it can be concluded that the shorter the voltage drop time, the smaller the power consumption. However, combined with Figure 13, it can be seen that the smaller the voltage drop, the smaller the effect of the OSS on circuit oscillation suppression.

Finally, in the comparison of different voltage drop delay times, it can be concluded that when the voltage drop time is the calculated value, the power consumption is close to the minimum.

5. Conclusions and Discussion

In this paper, an optimal-switching strategy was proposed for improving the switching performance of high-power SiC MOSFETs under hard-switching conditions. In addition, considering the trade-off between switching loss and switching overshoot, the voltage drop delay time was analyzed and calculated. By optimizing the voltage drop delay time of the turn-on and turn-off stages, the OSS can effectively minimize overshoot and suppress oscillation. The simulation results showed that the OSS can reduce the current overshot at the turn-on stage and minimize the voltage overshoot at the turn-off stage. In addition, compared with the hard-switching strategy, the current overshoot in the turn-on phase decreased by 14% and the voltage overshoot in the turn-off phase decreased by 18.03%. This showed that the OSS achieved a more comprehensive control strategy and better switching performance. Compared with digital gate drivers, although each has its own advantages, the OSS is more advanced and suffers less power losses.

The next step in this research is to make the actual circuit and test it. The contribution of this paper is limited due to simulation constraints. The optimization of the OSS in this paper was limited to the control voltage drop delay time; the control strategy could not be fully tested. Only the influence of a single variable of the OSS on the switching performance was tested. In future studies, multivariable control, such as delay time, voltage drop, voltage drop time, etc., could be tested in an actual circuit and jointly controlled to optimize semiconductor switching performance. However, we can confirm that the proposed OSS is promising compared to other methods.

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References

1. Castellazzi, A.; Fayyaz, A.; Romano, G.; Yang, L.; Riccio, M.; Irace, A. SiC power MOSFETs performance, robustness and technology maturity. *Microelectron. Reliab.* **2016**, *58*, 164–176. [CrossRef]
2. Biela, J.; Schweizer, M.; Waffler, S.; Kolar, J.W. SiC versus Si Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors. *IEEE Trans. Ind. Electron.* **2011**, *58*, 2872–2882. [CrossRef]
3. Oswald, N.; Anthony, P.; McNeill, N.; Stark, B.H. An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation with Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations. *IEEE Trans. Power Electron.* **2014**, *29*, 2393–2407. [CrossRef]
4. Hazra, S.; Ankan, D.; Cheng, L. High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications. *IEEE Trans. Power Electron.* **2016**, *31*, 4742–4754.
5. Chen, H.; Divan, D. High speed switching issues of high power rated silicon-carbide devices and the mitigation methods. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015.
6. Wang, J.; Chung, H.S.; Li, R.T. Characterization and Experimental Assessment of the Effects of Parasitic Elements on the MOSFET Switching Performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590. [CrossRef]

7. Sayed, H.; Zurfi, A.; Zhang, J. Investigation of the effects of load parasitic inductance on SiC MOSFETs switching performance. In Proceedings of the IEEE International Conference on Industrial Technology (ICIT), Toronto, ON, Canada, 22–25 March 2017.
8. Nayak, P.; Hatua, K. Modeling of switching behavior of 1200 V SiC MOSFET in presence of layout parasitic inductance. In Proceedings of the IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Trivandrum, India, 14–17 December 2016.
9. Liu, T.; Ning, R.; Wong, T.Y.; Shen, Z.L. Modeling and analysis of SiC MOSFET switching oscillations. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 747–756. [CrossRef]
10. Yang, B.; Ge, Q.; Zhao, L.; Zhou, Z.; Cui, D. Influence of parasitic elements of busbar on the turn-off voltage oscillation of SiC MOSFET half-bridge module. In Proceedings of the IECON 2017—43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, China, 29 October–1 November 2017.
11. Fabre, J.; Ladoux, P.; Piton, M. Characterization and implementation of Dual-SiC MOSFET modules for future use in traction converters. *IEEE Trans. Power Electron.* **2015**, *30*, 4079–4090. [CrossRef]
12. Rujas, G.; Lopez, V.M.; Mir, L.; Nieva, T. Gate driver for high power' SiC modules: Design considerations, development and experimental validation. *IET Power Electron.* **2018**, *11*, 977–983. [CrossRef]
13. Liang, M.; Li, Y.; Chen, Q.; Lu, Y. Research on an improved DC-side snubber for suppressing the turn-off overvoltage and oscillation in high speed SiC MOSFET application. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017.
14. Jahdi, S.; Alatise, O.; Ortiz Gonzalez, J.A.; Bonyadi, R.; Ran, L.; Mawby, P. Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules. *IEEE Trans. Ind. Electron.* **2016**, *63*, 849–863. [CrossRef]
15. Zhang, Z.; Wang, F.; Tolbert, L.M.; Blalock, B.J. Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration. *IEEE Trans. Power Electron.* **2014**, *29*, 1986–1997. [CrossRef]
16. Riazmontazer, H.; Mazumder, S.K. Optically Switched-DriveBased Unified Independent dv/dt and di/dt Control for Turn-Off Transition of Power MOSFETs. *IEEE Trans. Power Electron.* **2015**, *30*, 2338–2349. [CrossRef]
17. Yamaguchi, K.; Sasaki, Y.; Imakubo, T. Low loss and low noise gate driver for SiC-MOSFET with gate boost circuit. In Proceedings of the IECON 2014—40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014.
18. Riazmontazer, H.; Rahnamaee, A.; Mojab, A.; Mehrnami, S.; Mazumder, S.K.; Zefran, M. Closed-loop control of switching transition of SiC MOSFETs. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015.
19. Nayak, P.; Hatua, K. Active gate driving technique for a 1200 V SiC MOSFET to minimize detrimental effects of parasitic inductance in the converter layout. *IEEE Trans. Ind. Appl.* **2017**, *54*, 1622–1633. [CrossRef]
20. Paredes, A.; Ghorbani, H.; Sala, V.; Fernandez, E.; Romeral, L. A new active gate driver for improving the switching performance of SiC MOSFET. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017.
21. Yang, Y.; Wen, Y.; Gao, Y. A Novel Active Gate Driver for Improving Switching Performance of High-Power SiC MOSFET Modules. *IEEE Trans. Power Electron.* **2019**, *34*, 7775–7787. [CrossRef]
22. Katada, R.; Hata, K.; Ymauchi, Y.; Wang, T.W. Digital Gate Driving (DGD) is Double-Edged Sword: How to Avoid Huge Voltage Overshoots Caused by DGD for GaN FETs. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 10–14 October 2021.
23. Miyazaki, K.; Abe, S.; Tsukuda, M.; Omura, I.; Wada, K.; Takamiya, M.; Sakurai, T. General-purpose clocked gate driver IC with programmable 63-level drivability to optimize overshoot and energy loss in switching by a simulated annealing algorithm. *IEEE Trans. Ind. Appl.* **2017**, *53*, 2350–2357. [CrossRef]
24. Anthony, P.; McNeill, N.; Holliday, D. High-Speed Resonant Gate Driver with Controlled Peak Gate Voltage for Silicon Carbide MOSFETs. *IEEE Trans. Ind. Appl.* **2014**, *50*, 573–583. [CrossRef]
25. Chen, L.; Peng, F.Z. Switching loss analysis of closed-loop gate drive. In Proceedings of the Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 21–25 February 2010.
26. Regnat, G.; Jeannin, P.O.; Frey, D.; Ewanchuk, J.; Mollov, S.V.; Ferrieux, J.P. Optimized power modules for silicon carbide MOSFET. *IEEE Trans. Ind. Appl.* **2018**, *54*, 1634–1644. [CrossRef]
27. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer: Berlin/Heidelberg, Germany, 2008.
28. Liao, X.; Li, H.; Yao, R.; Huang, Z.; Wang, K. Voltage Overshoot Suppression for SiC MOSFET-Based DC Solid-State Circuit Breaker. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2019**, *9*, 649–660. [CrossRef]
29. Lobsiger, Y. Closed-Loop IGBT gate driver and current balancing. Ph.D. Thesis, Department of Information Technology and Electrical Engineering, ETH-Zurich, Seedorf, Switzerland, 2014.

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