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On short channel effects in high voltage JFETs: A theoretical analysis

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ABSTRACT

In this work, the impact of Short Channel Effects (SCEs), particularly Drain Induced Barrier Lowering (DIBL) on the performance of a high voltage Silicon Carbide (SiC) JFET has been thoroughly investigated. Drift-Diffusion simulations of on-state current-voltage characteristics and breakdown performance have been completed for different gate junction depths (x_j) and mesa widths (MW). Due to the short channel length, realistic implant doping profiles extracted from experimentally calibrated Monte-Carlo based SRIM simulations have been used. Two suitable designs to eliminate premature DIBL-induced failure have been found: $x_j = 0.7$ μm for MW=1.75 μm, and $x_j = 1$ μm for MW=2 μm. We found that a 0.3 μm junction depth has a breakdown voltage of only 50 V due to collapse of the source-drain barrier at a relatively low drain bias. Threshold voltage (V_{th}) decreases with increasing junction depth, approaching 0 V. This is due to a combination of greater lateral straggling of implanted ions and improved electrostatic control of the channel. Our calculations demonstrate that the most robust option to mitigate DIBL and consequently early breakdown is to maintain $x_j \geq 1$ μm. At this depth, the threshold voltage has a weak dependence on drain bias, indicating diminishing SCEs. Decreasing the mesa width mitigates early breakdown but requires a mesa width of less than 1.75 μm, which poses fabrication challenges.

1. Introduction

Due to its wide bandgap, SiC has excellent electrical properties for power electronics. As a result, SiC devices have begun to supplant silicon devices in applications, particularly in the 650–1200 V range. Such applications include automotive power-trains and renewable energy infrastructure. Another application where SiC devices may excel is circuit protection or solid state circuit breaker (SSCB) products. SiC devices, particularly SiC JFETs have been demonstrated in SSCBs (Miao et al., 2015; Urciuoli et al., 2011).

The SiC JFET device structure has a key benefit of not requiring a gate oxide unlike SiC MOSFETs, which has posed an issue due to high density of near interface traps at the SiC/SiO2 interface (Kobayashi et al., 2016). This can lead to parameter shift such as V_{th} over device lifetime, reducing MOSFET reliability (Lelis et al., 2008). As a result, SiC JFETs are excellent candidates for high temperature, high reliability SSCBs.

As the channel length of the FET reduces, the gate loses control of the channel, degrading device performance. These so-called SCEs manifest in variety of ways, such as gate induced drain leakage, sub-threshold source/drain leakage and DIBL (Maurya and Bhowmick, 2022). SCEs are particularly prevalent in planar logic MOSFETs due to their extreme miniaturisation, and have limited the further scalability of these devices (Panchanan et al., 2021). This has resulted in a design shift towards double-gate or even tri-gate architectures such as FinFETs to mitigate SCE effects. Recent studies have thoroughly explored SCEs in logic MOSFETs, examining how different design parameters can impact the degree of DIBL that a device may undergo (Chakrabarti et al., 2022; Madadi and Orouji, 2020; Narendar et al., 2020).

The effect of SCEs on V_{th} and sub-threshold slope in SiC JFETs has been investigated previously for logic devices (Kaneko et al., 2020). The above paper and most existing literature addressing DIBL and other SCEs consider logic devices, and mainly concentrate on the device performance in the on-state. Therefore, there is a lack of existing studies regarding the influence of DIBL on the breakdown performance of high-voltage SiC JFETs. High-voltage JFETs are required to consistently withstand elevated blocking voltages while maintaining a stable V_{th}. Should a high voltage JFET fail prematurely in an actual application, it has the potential to cause damage to the entire circuit or, in more severe cases, lead to catastrophic failures owing to the substantial voltages and currents involved.

Experimental work by Wang et al. (2020) and Veliadis et al. (2008) on high voltage SiC JFETs speculate that SCEs, specifically DIBL contributed to the observed premature breakdown. It is well known that

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DIBL may induce an early collapse of the barrier between source and drain electrodes. This will occur before the device reaches avalanche breakdown, and thus will result in a premature failure of the device. This highly undesirable effect must be eliminated. Preliminary theoretical work by the authors identified DIBL as a failure mechanism causing early breakdown in high voltage SiC JFETs, but did not address mitigation (Monaghan et al., 2023).

In this work, we investigate and mitigate the impact of DIBL on the blocking performance of a high voltage 4H-SiC JFETs. Due to the small junction depths investigated, realistic doping profiles were used. The relation between different parameters such as x_j, MW and applied V_g on the blocking performance were studied. In addition, the impact of SCEs on the JFET linear region and V_{th} were carried out. The hold off voltage (V_{ho}) as a function of negative gate voltage is examined.

Furthermore, our outcomes in addressing SCEs correspond qualitatively to the conclusions presented by Kaneko et al. (2020) in their experimental study. However, the observed threshold voltage shift is larger. This is due to the inherent two-dimensional nature of the P+ doping profile in the channel within our vertical device architecture, where the channel thickness is not constant.

Section 2 discusses the device structure used for this work, alongside realistic implantation schedule design for P+ gate region formation. Additionally, physical models used for TCAD simulation are presented. Section 3 initially presents on-state characterisation of JFET with varying x_j and MW. Secondly, blocking performance is investigated in detail as a function of x_j, MW and V_g.

2. Device design and simulation methods

2.1. JFET device structure

The JFET structure used for this work is shown in Fig. 1. The target voltage rating for this device is 1200 V. All relevant parameters and dimensions of the design are shown in Table 1. The device dimensions used have been chosen to closely resemble prior fabricated high voltage SiC JFETs (Li et al., 2008). The device has been designed with a 5 μm 4H-SiC substrate, with an N-type doping concentration of 1×10^{19} cm^{-3}. At high voltage rating such as 1200 V, drift and JFET channel resistance dominate, thus for this work substrate resistance is considered as negligible. The total drift region thickness has been set to 15 μm, with a doping concentration of 1×10^{16} cm^{-3}. A 100 nm thick N+ region with a doping concentration of 1×10^{19} cm^{-3} to enable formation of a source ohmic contact located on top of the drift region. The MW has been set at 2 μm unless stated otherwise. The total cell pitch is 5 μm. Mesa height has been set to 2 μm.

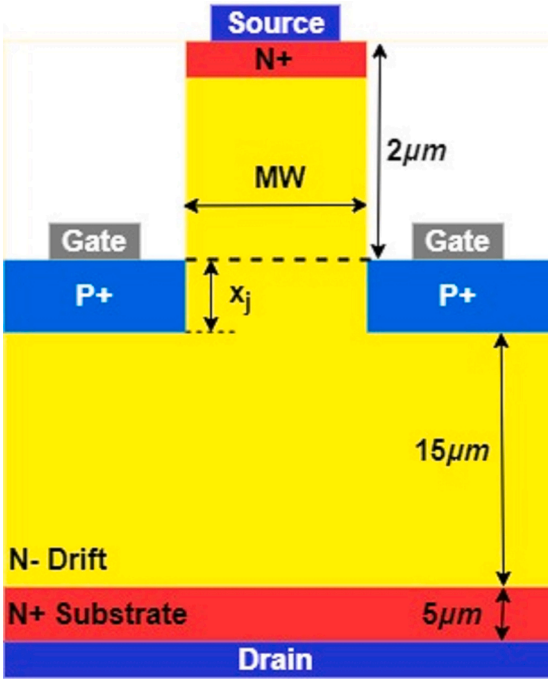


Fig. 1. Cross-section of JFET unit cell used for TCAD simulation.

Table 1
JFET unit cell parameters used in TCAD simulation.

Parameter	Value	Units
Cell pitch	5	μm
Mesa Width	2	μm
Mesa Height	2	μm
Drift Region thickness	15	μm
N+ thickness	0.1	μm
Substrate thickness	5	μm
Drift region doping	1×10^{16}	cm^{-3}
N+ doping	1×10^{19}	cm^{-3}
Substrate doping	1×10^{19}	cm^{-3}

2.2. Implantation profiles

Monte-Carlo implantation methodology has been used to simulate the aluminium P-type implantation in the JFET gate region (Tian, 2008). This methodology is based on the statistical Binary Collision Approximation (Tian, 2003). As the P+ gate region must form an ohmic contact, the target concentration is $\geq 1 \times 10^{19}$ cm^{-3}. A box profile of this target concentration is achieved using an implant schedule of multiple individual implants. Four different schedules have been simulated using SRIM to achieve different maximum junction depths: A (300 nm), B (500 nm), C (700 nm) and D (1000 nm). Fig. 2 shows the doping profiles generated from SRIM for each of the four designs. The figure shows that there is considerable doping fluctuation especially for design D, which exhibits a large tail-off in concentration between 800 nm and 1000 nm. All implant parameters for the respective schedules are shown in Table 2, which shows beam dose and energy. It should be noted that it is possible to achieve equivalent depths with lower implantation energies by utilising the channelling effect (Wada et al., 2022), but in this work standard random implantation at an angle of at 0° is used.

To fabricate this structure in practice, using the higher implantation energies required to achieve depths approaching 1 μm will require thick

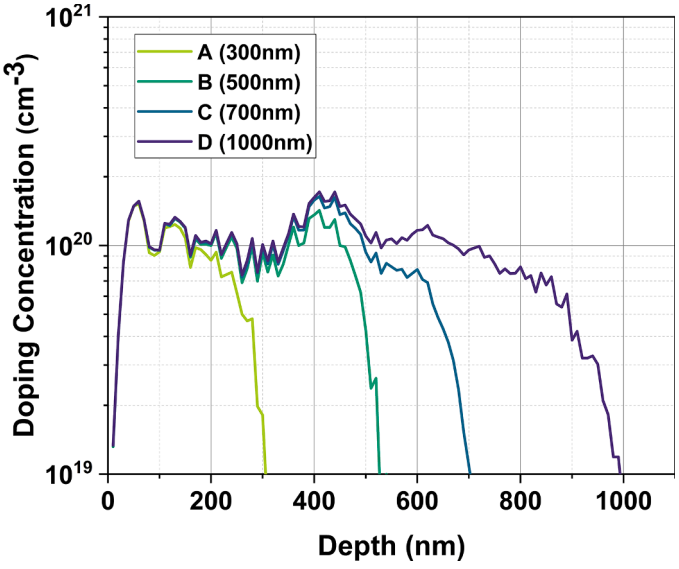


Fig. 2. Simulated SRIM depth profiles for each of the proposed implantation schedules shown in Table 2.

Table 2
Implantation parameters used for each of the four different schemes: A,B,C and D.

Implant	40 keV	100 keV	180 keV	350 keV	520 keV	680 keV	880 keV
A	6×10^{14} cm^2	9×10^{14} cm^2	1.1×10^{15} cm^2	–	–	–	–
B	6×10^{14} cm^2	9×10^{14} cm^2	1.1×10^{15} cm^2	2.5×10^{15} cm^2	–	–	–
C	6×10^{14} cm^2	9×10^{14} cm^2	1.1×10^{15} cm^2	2.5×10^{15} cm^2	1.7×10^{15} cm^2	–	–
D	6×10^{14} cm^2	9×10^{14} cm^2	1.1×10^{15} cm^2	2.5×10^{15} cm^2	1.7×10^{15} cm^2	1.4×10^{15} cm^2	1.4×10^{15} cm^2

oxide hardmasks, or even metal masks as used in Zhao et al. (2003).

2.3. Simulation methodology and physical models

The calculation of I-V characteristics uses the drift-diffusion formalism in conjunction with the Poisson Equation. Anisotropic, temperature and doping dependent effects on the carrier mobility are considered (Schaffer et al., 1994). Due to the high carrier concentrations present ($\geq 1 \times 10^{19}$ cm^{-3}) in the active region in the device on-state, Fermi-Dirac statistics and a bandgap narrowing model are included (Lades, 2002). To model carrier recombination at high carrier concentrations, both Shockley-Read-Hall and Auger models are employed (Galeckas et al., 1997). The Okuto-Crowell impact ionization model is used for breakdown simulations, taking into account the effect of the 4H-SiC lattice anisotropy (Niwa et al., 2014). Finally, incomplete ionization is used with aluminium activation set to $E_{a,Al} = 265$ meV, and nitrogen to $E_{a,N} = 100$ meV.

3. Results and discussion

3.1. On-state characterisation

In this section, drain current-gate voltage (I_d - V_g) characteristics were calculated to assess how threshold voltage varies depending on the junction depth and mesa width. Fig. 3 shows the transfer characteristics for design A, B, C and D at room temperature for two different drain bias values (0.05 V and 2 V). All devices have a MW of 2 µm. At a fixed drain voltage, as junction depth increases from design to design, V_{th} trends towards 0 V. The corresponding threshold voltages were extracted at a current density of 1×10^{-13} A/cm^2. The extracted threshold voltage values for designs A, B, C, and D at V_d= 2 V are determined as follows: -10.9 V, -6.5 V, -4.75 V, and -2.6 V, respectively. It is also noted that sub-threshold slope decreases with junction depth, indicating better electrostatic control of the channel. Furthermore, it is important to highlight that an increase in the channel length correlates with a reduction in the observed threshold voltage shift (ΔV_{th}) as V_d varies. This qualitatively agrees with findings presented for SiC logic JFETs (Kaneko et al., 2020) and elsewhere.

However, the amplified lateral straggling of implanted aluminium dopants, resulting from an increased number of implantation events (Jiang et al., 2018), also plays a significant role in the V_{th} shift. This can be seen in Fig. 4, which shows the doping profiles in the channel regions of designs A and D. The design A (Fig. 4a) shows less lateral straggling compared to design D (Fig. 4b). The doping profile of design D, due to the afore mentioned straggling has an effective channel region thickness (a) of 890 nm, compared to 1490 nm for design A. This is almost a 60 %

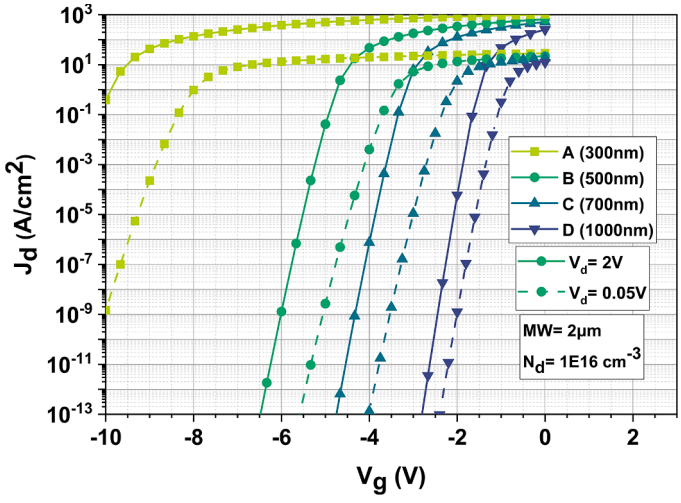


Fig. 3. Simulated transfer characteristics for all four designs at $V_d = 2$ V in solid lines, $V_d = 0.05$ V in dashed lines.

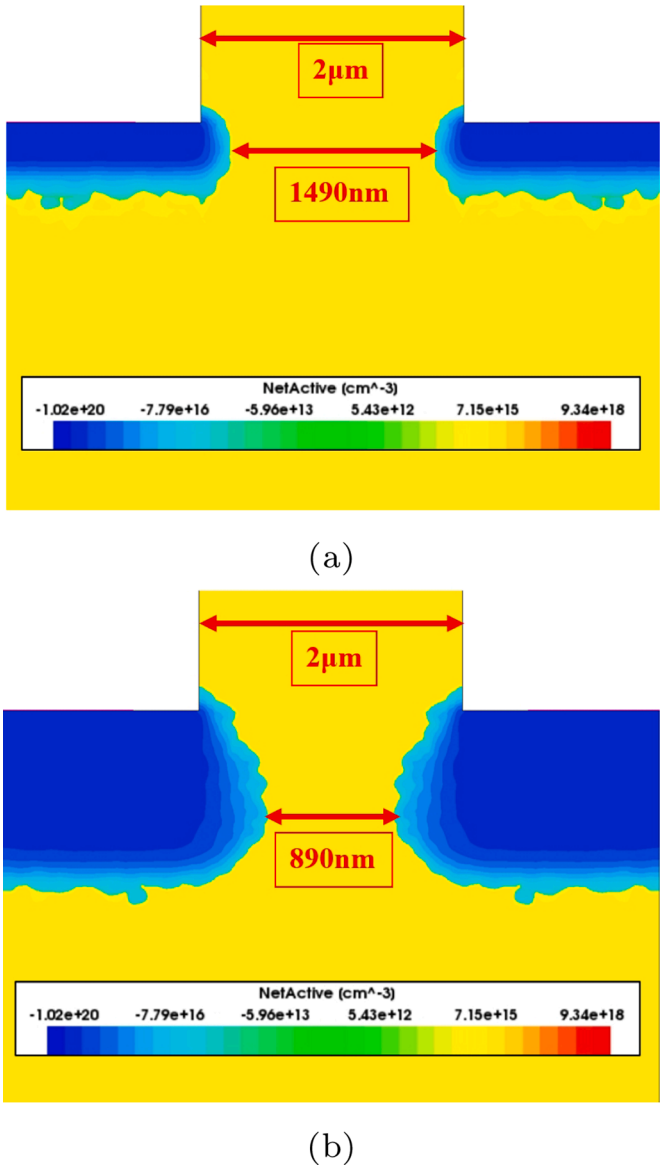


Fig. 4. Lateral straggling of implanted aluminium dopants in the channel region for (a) Design A (b) Design D.

reduction in effective channel thickness. It has been demonstrated that lateral straggling due to implantation can result in a reduction in the spacing between adjacent P-type regions in MOSFETs, subsequentially causing the channel to pinch off prematurely (Yun et al., 2020).

Previous studies on logic JFETs have shown a clear correlation between SCEs, and thus channel length with V_{th} and sub-threshold slope. However, the straggling effects shown in Fig. 4 are not present for a device with uniform channel thickness. Therefore, as the JFET experiences a reduction of both channel thickness and SCEs as x_j increases, it is difficult to separate the contributions of each effect to the shift of V_{th} towards 0 V. Nevertheless, this qualitatively agrees with the design rule proposed in Kaneko et al. (2020) indicating that as the ratio $\frac{x_j}{a}$ increases, the mitigation of SCEs becomes more effective.

Fig. 5 shows V_{th} for design B with varying mesa width for $V_d = 0.05$ V. When varying MW between 1.75 μm–2.25 μm, V_{th} is observed to reduce from − 10.9 V at 2.25 μm to − 5.6 V at 2 μm, and to − 3.8 V at 1.75 μm. This is due to the channel region thickness being reduced. When the channel thickness decreases, the depletion regions do not need to extend as far horizontally from the adjacent gate junctions to pinch off the channel, and thus exhibit a lower V_{th}.

Fig. 6 a and b show output characteristics at $V_g = 0$ V for varying junction depth and mesa width, respectively. As the effective channel length is greater in devices with deeper implants, it is expected that channel resistance and thus specific on-state resistance ($R_{on,sp}$) will increase linearly with junction depth. However, the straggling into the channel region at larger junction depths will result in a smaller effective channel thickness, and thus an additional increase in resistance. This is reflected in Fig. 6a, where $R_{on,sp}$ values have been extracted at $V_d = 0.5$ V. Design A has the lowest $R_{on,sp}$ of 1.79 mΩ.cm^2, compared to designs B and C which exhibit values of 2.43 and 3.08 mΩ.cm^2, respectively. In general, linear behaviour is observed between effective channel length and $R_{on,sp}$, but not for design D, which has a considerably increased $R_{on,sp}$ of 4.63 mΩ.cm^2. This is explained by the significantly increased degree of straggling for design D, as shown previously in Fig. 4b.

In turn, reduced MW causes a higher $R_{on,sp}$, as shown in Fig. 6b. For design B, $R_{on,sp}$ is increased to 3.00 mΩ.cm^2 for MW=1.75 μm, 24.6% higher than when MW=2 μm. Conversely, increasing MW to 2.25 μm for design B reduces $R_{on,sp}$ to 1.75 mΩ.cm^2 - comparable to design A with a 2 μm mesa width. Designs A and C exhibit a 24%, 244% increase in $R_{on,sp}$, when reducing MW to 1.75 μm, respectively. The significant increase for design C is due to the channel being close to pinched off, as reflected by the designs V_{th} of − 1.32 V. Furthermore, due to the effect of lateral straggling, design D acts as normally-off for MW=1.75 μm, and thus $R_{on,sp}$ can not be extracted for the $V_g = 0$ V condition. This is also reflected in the positive V_{th} of 0.4 V. Table 3 shows the extracted V_{th} and

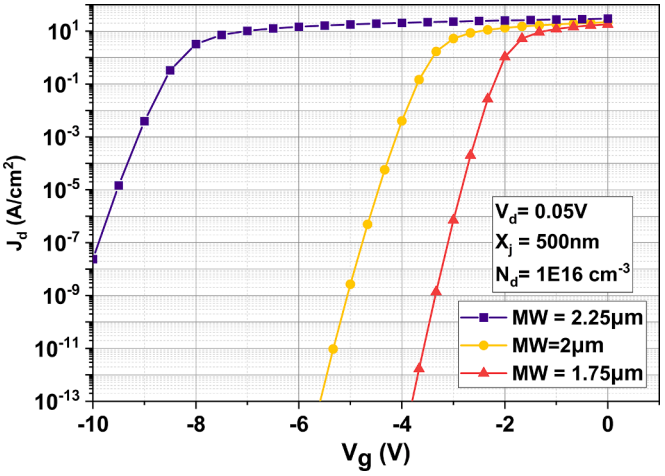


Fig. 5. Design B with varying MW, with V_{th} approaching 0 V at smaller MWs.

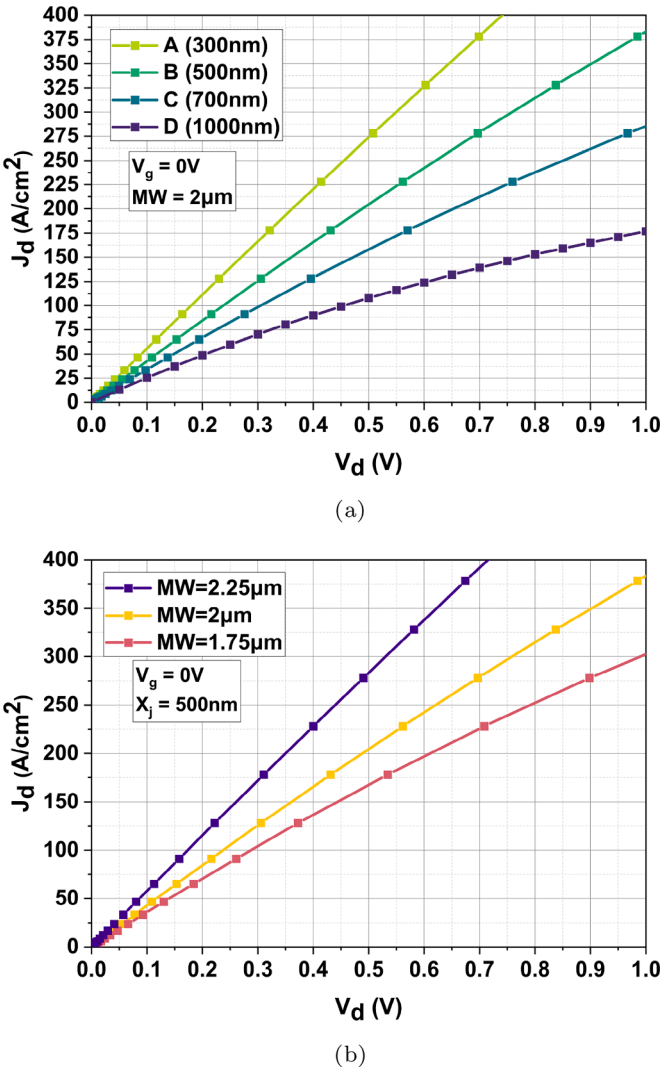


Fig. 6. Output characteristics at V_g=0 V of (a) each of the 4 designs, with $R_{on,sp}$ increasing with x_j, and (b) Design B with varying MW, with $R_{on,sp}$ reducing at larger MWs.

$R_{on,sp}$ for all four designs with MW= 1.75 μm and 2 μm.

In general, these increases in $R_{on,sp}$ between the different designs are negligible from the technological point of view, however as is shown in the next section, the breakdown behaviour of the different designs are quite dissimilar, and represent a significant reduction in blocking capabilities.

3.2. Breakdown performance and DIBL

Fig. 7 shows the breakdown voltage of all four designs at $V_g = -20$ V. The corresponding extracted breakdown voltage values for each design are shown in Table 3 alongside results from the previous section. In the off-state, JFET breakdown voltages are taken at a V_g of − 20 V (Qorvo, 2018). Fig. 7 shows that the shallower junction designs have severely degraded blocking voltage capability. Designs A, B and C fail at Vd =50 V, 230 V and 630 V, respectively. These values are 3%, 13.8% and 37.7% of the ideal blocking voltage for the drift region used (Baliga, 2010).

This suggests that this premature failure mechanism is induced by SCEs. However, design D fails at 1390 V, just 83% of the ideal blocking voltage of the drift region. Our simulations confirm that at the point of failure, the current path in designs A, B and C is between the source-drain electrodes. This is opposed to the expected current path between

Table 3
Steady-State characteristics of each junction depth for MW=1.75 μm and 2 μm. $R_{on,sp}$ values are taken at $V_g = 0$ V, V_{th} at $V_d = 0.5$ V and breakdown voltages at $V_g = -20$ V. *$R_{on,sp}$ not extracted due to normally-off operation.

	MW=1.75 μm				MW=2 μm			
Implant	$R_{on,sp}$ (mΩ.cm^2)	V_{th} (V)	BV (V)	Failure Type	$R_{on,sp}$ (mΩ.cm^2)	V_{th} (V)	BV (V)	Failure Type
A	2.22	− 6.75	155	PT	1.79	− 10.90	50	PT
B	3.00	− 3.80	735	PT	2.43	− 6.50	230	PT
C	7.42	− 1.82	1367	AV	3.08	− 4.75	630	PT
D	–*	0.40	1430	AV	4.63	− 2.60	1390	AV

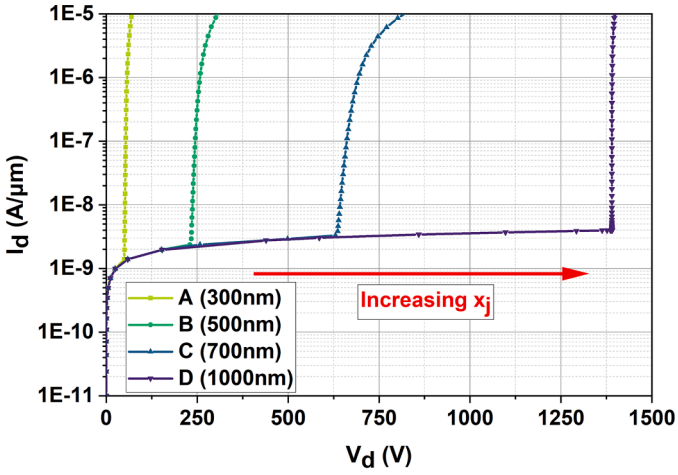


Fig. 7. Breakdown characteristics for each design tested at $V_g = -20$ V, with breakdown voltage increasing with x_j.

the gate and drain electrodes if avalanche breakdown occurred.

The positive correlation between x_j and breakdown voltage observed in Fig. 7 is explained by the lengthening of the channel region which in turn heightens of the potential barrier, and provides more electrostatic control of the channel. The barrier height relative to the source (in the centre of the channel region) for design A at $V_d = 0$ V, $V_g = -20$ V is equal to 5.57 eV, but becomes close to 0eV at the point of failure. Conversely, design D has an initial 15.43 eV barrier height at the same bias, and 4.9 eV at failure. This larger initial barrier height in design D prevents premature failure.

Validation of the devices' failure method can be obtained by plotting the electron-hole generation rate of carriers in the device. Fig. 8a shows the 2D profile of impact ionization rate of design A. The highest generation of electron-hole pairs is occurring in the centre of the channel, at a low rate of 1×10^4 cm^{-3}s^{-1}. This rate would not induce an avalanche generation of carriers. Conversely, Fig. 8b shows impact ionization rate for design D, which is highest at the gate-drain junction boundary at a significantly larger rate of 5×10^{26} cm^{-3}s^{-1}, which is indicative of avalanche breakdown. Table 3 also shows the failure method of each design, with PT denoting a premature punch-through, and AV denoting avalanche breakdown.

Furthermore, the electric field profile at the point of failure can provide further insight into the method of failure. Fig. 9a shows the electric field profile at breakdown, highlighting the location of a horizontal cut-line. The results of the cut-line for each of the four designs is shown in Fig. 9b. For designs A, B and C the magnitude of the electric field at the gate junction was less than the critical field strength for 4H-SiC (2.8 MV/cm), where carrier generation would be expected to become significant. Design D however has a peak field value of 2.76 MV/cm.

Fig. 10 shows that breakdown voltage for design B with varying MW. A MW=2.25 μm results in a breakdown voltage of 72 V, compared to 735 V for MW=1.75 μm. However, it should be noted that for MW=1.75 μm, design B still suffers from the punch-through failure mechanism,

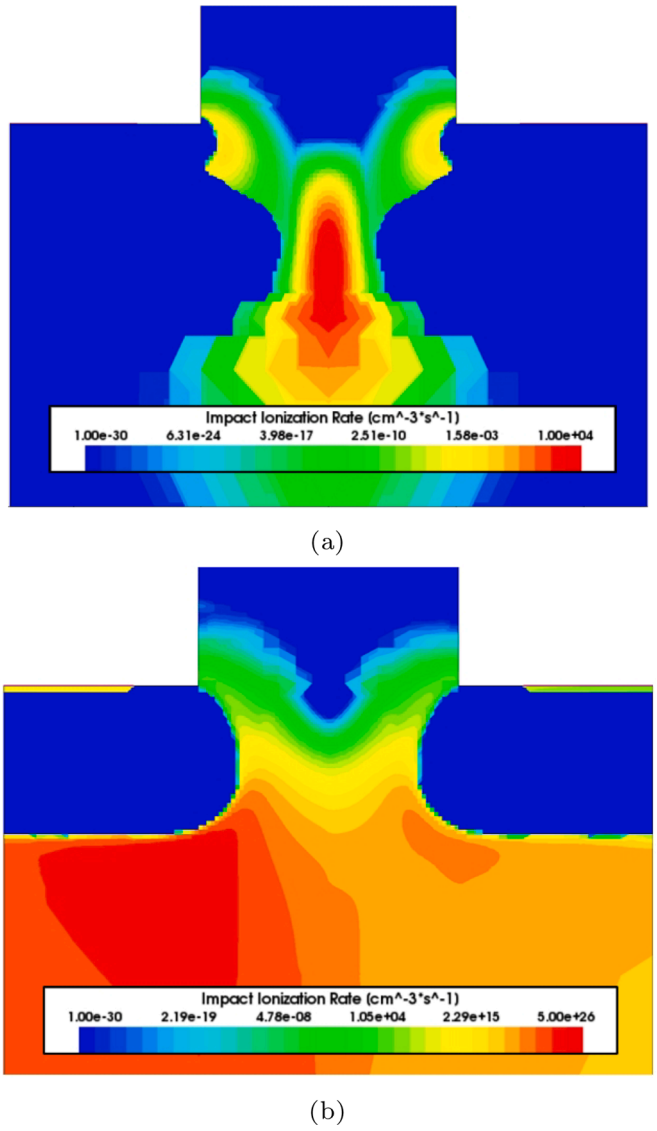
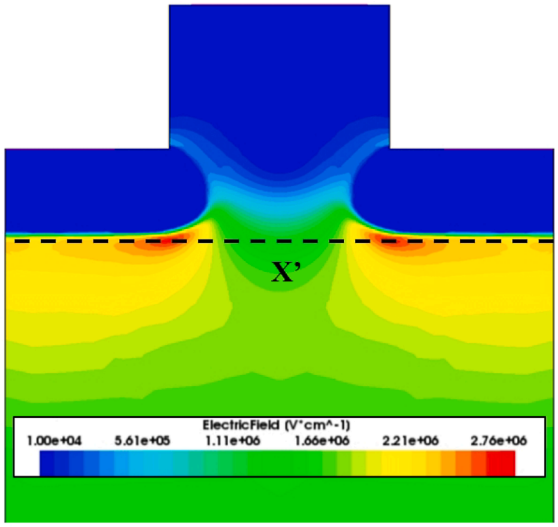


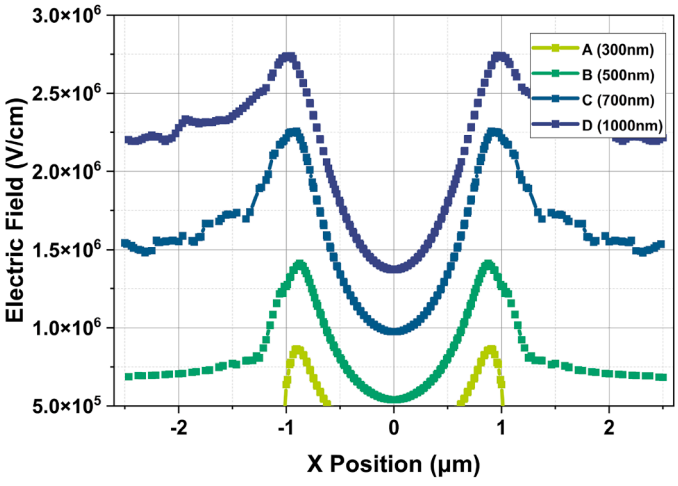
Fig. 8. Electron-hole pair generation rates at the point of failure for (a) Design A and (b) Design D.

reaching only 44% of the ideal blocking voltage for the drift region. Therefore, to fully mitigate DIBL induced punch-through failure, designs with shallow junction depths will likely require MW ≤1.75 μm at this doping concentration. It is important to note, however, that using sub-1.75 μm mesa widths does not guarantee complete elimination of SCEs during the on-state.

Gate bias is also related to breakdown voltage, as an increasingly negative V_g will also raise the potential barrier. The effect of increasing V_g on breakdown voltage for design B is shown in Fig. 11. Increasing V_g from − 20 V to − 40 V results in a 1020 V increase in breakdown



(a)



(b)

Fig. 9. (a) Electric field profile of design D in the off-state, showing the position of cut-line X' (b) Electric field magnitude along cut-line X' for all four designs at their respective points of failure.

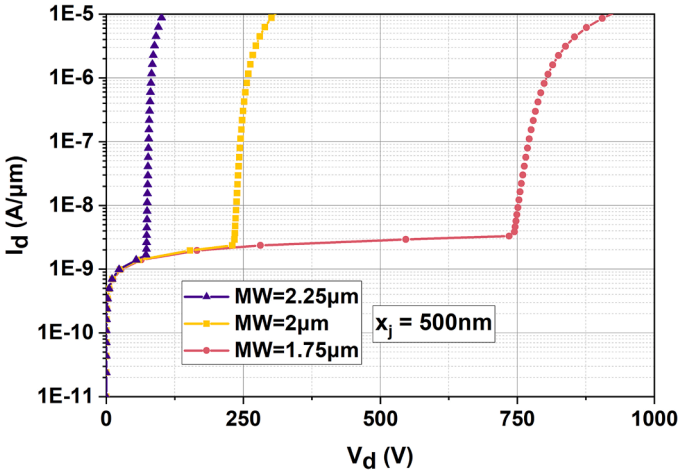


Fig. 10. Breakdown characteristics for Design B with varying V_g, with breakdown voltage increasing at larger V_g.

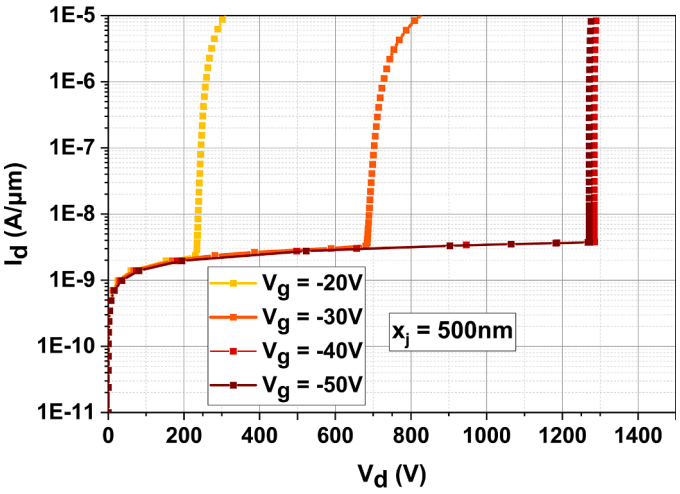


Fig. 11. Breakdown characteristics for Design B with varying MW, with breakdown voltage increasing at smaller MWs.

voltage, from 230 V to 1250 V. Concurrently, it is observed that at $V_g = -40$ V the failure mechanism has transitioned to punch-through from avalanche. However, it must be noted that although this appears an attractive solution, in practice large V_g biases below -20 V are highly unfeasible for gate driver circuitry to supply, and therefore optimising junction depth and MW must be prioritised.

Hold off voltage has been proposed in previous literature for JFETs, and is defined as the required V_g to enable the JFET to fail via avalanche Wang et al. (2020). Gate bias above V_{ho} has a minimal effect on breakdown performance, as shown in Fig. 10 where increasing to $V_g = -50$ V results in similar a breakdown voltage to $V_g = -40$ V. Hold off voltage for varying MW and x_j is shown in Fig. 12. As expected, designs A and B with small junction depths require significantly larger V_g values to prevent punch-through failure; at MW=2 μm V_{ho} is -70 V and -40 V for designs A and B, respectively. Conversely, design D exhibits a V_{ho} lower than the standard -20 V used for JFET breakdown measurements; -10 V for MW=1.75 μm and -14 V for MW=2 μm. Increasing MW for all junction depths results in an increase in V_{ho} due to larger V_g required to form a suitably sized potential barrier.

Although deeper junctions and smaller MW values are evidentially the best design choices for the off-state performance, consideration of

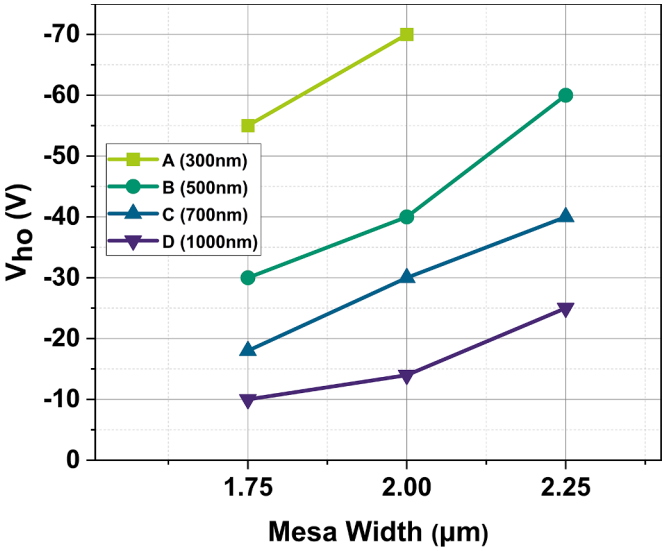


Fig. 12. V_{ho} plotted for varying MW for all four designs, with V_{ho} increasing at smaller x_j.

on-state performance is of equal importance; eliminating DIBL comes at the cost of V_{th} shifting towards 0 V.

One promising design choice would be to utilise tilted implantation to achieve P-type doping on the mesa sidewall. This would enable longer channels to be formed without requiring high energy implantation, and thus potentially minimising the straggling effect observed. However, utilising tilted implantation would require double the amount of implantation events as a standard design to achieve full coverage on both sidewalls of the mesa.

4. Conclusion

In this work, a drift-diffusion study of the on-state and breakdown performance of a high voltage 4H-SiC JFET has been carried out. Realistic gate junction doping profiles has been designed using SRIM. Analysis of the effect that DIBL can have on the breakdown performance of the device has completed. Two feasible designs have been proposed for the structure considered: $x_j = 700$ nm with a MW=1.75 μm, or $x_j = 1000$ nm for MW=2 μm. Of the three parameters tested, gate junction depth has the strongest correlation with improved breakdown performance. However, due to lateral straggling associated with high energy implantation, channel thickness at high junction depth is restricted, resulting in V_{th} approaching 0 V, in some cases resulting in normally-off behaviour. It is noteworthy that while both viable designs experience failure attributable to avalanche breakdown rather than DIBL, both still exhibit SCEs during the on-state. An excellent candidate for mitigating DIBL whilst minimising V_{th} shift is artificially increasing junction depth via mesa sidewall implantation. This removes the need for high energy implantation, and thus reduces the impact of lateral straggling. Albeit tilted implantation adds a further degree of complexity to device and process design, which must be considered.

CRediT authorship contribution statement

F. Monaghan: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Writing – original draft, Writing – review & editing. **A. Martinez:** Conceptualization, Investigation, Methodology, Supervision, Validation. **J. Evans:** Formal analysis, Investigation, Writing – review & editing. **C. Fisher:** Investigation, Writing – review & editing. **M. Jennings:** Funding acquisition, Investigation, Resources, Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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