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Impact of Dimensions and Doping on the Breakdown Voltage of a Trench 4H-SiC Vertical JFET

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Abstract. In this paper we study the feasibility of the design/fabrication of a vertical trench 4H-SiC Junction Field Effect Transistor (JFET), assuming realistic constraints of the depth of the P+ implantation. The P+ doping profile is obtained using a Monte Carlo implantation simulation. The calculation used a drift-diffusion approach. The JFET aims to achieve a threshold voltage of -3V. We found that this constraint in concomitance with the proposed structure limits the breakdown voltage to approximately 200V. This is the result of a premature breakdown induced by short channel effects, namely Drain Induced Barrier Lowering (DIBL). However, a negative increase in the gate bias represses this short channel effect and improves the breakdown voltage to roughly 1800V. At this gate bias, the breakdown is induced by reaching the critical field strength of 4H-SiC at the gate P+/N junction, which causes avalanche generation of carriers. In addition, we have calculated the dependence of the threshold voltage on the drift doping and pillar width. This work also shows the vulnerability of the design to random fluctuation in the doping profile.

Introduction

Due to continued improvement in fabrication processes and technology, SiC devices have established a strong market presence in the 650V+ range. Although the bulk of the SiC device market is focussed on normally-off devices, there is also potential for normally-on SiC devices to replace the silicon depletion-mode MOSFET (DMOS). The ideal candidate to substitute these silicon devices in Cascode configurations & in solid state circuit breaker products are SiC Junction Field Effect Transistors (JFETs). The JFET structure has the benefit of not requiring a gate oxide unlike MOSFETs, which has posed issues due to the fact that the SiO_2/SiC interface is renowned for a high density of interface traps and positive fixed charge[1]. As a result of not requiring a gate oxide, JFETs are excellent candidates for high reliability, high temperature applications, whilst also providing a considerable reduction in on-state resistance ($R_{ds,on}$) compared to their silicon DMOS counterparts.

The design of vertical JFET SiC structures such as that represented in Fig. 1.1, in which the depth of the P+ doping acts as an effective channel length (or the region which controls the active channel of the device). It is well known that a deep P+ implant will improve the control of the drift or channel region. However, this depth is limited by the constraints of the SiC lattice, namely
(i) poor diffusion of dopants in SiC and (ii) because deep implants require very high ion energies. This has the consequence that there is a limit to the maximum length attainable for the effective channel of ~0.5μm. It must be noted that there is existing literature on channelled implantation methods which can achieve greater depths than 0.5μm.[2] However, reducing the channel width or the drift doping for a fixed depth will improve channel control. But these parameters are intertwined with other design requirements. In addition a small channel width is vulnerable to doping fluctuations in both the N- drift region and the P+ gate implant. In the case of the drift region, some wafer manufacturers quote a ± 20% epitaxy doping tolerance for N-type.[3]

In this work, using the constraint that the threshold voltage (V_{th}) must be $V_{th} \approx$ -3V, the impact of the pillar width (W_{pillar}) shown on Fig.1.2. Alongside the drift doping concentration (N_d) on the performance of a normally-on vertical SiC JFETs is investigated using Sentaurus TCAD. Threshold voltage and breakdown voltage (V_{br}) are both extracted from simulations. We aim to find the

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corresponding values of W_{pillar} and N_d for the target $V_{gs} \approx -3V$ mentioned, whilst maximizing V_{br}. In addition, the interrelation of the threshold voltage and doping is also studied.

The next section presents the simulation methodology, alongside the device structure and its respective dimensions and doping. The following section presents the calculation results and discussion of said results. Finally, the conclusion section presents the highlights and the summary of this work.

Device and Simulation Methodology

This section presents the physical models and parameters used in the simulations; and the device structure, doping and dimensions. Fig. 1.1. shows the vertical trench JFET cell structure, highlighting its main features, including the two P+ regions in contact with the gate electrodes and the source electrode located on the top of the pillar.

Fig. 1.2. Shows the Monte Carlo simulated [4] aluminium P+ gate implants which have been set at a depth of 0.5µm. Aluminium P+ implants in SiC have a maximum depth of between 0.3-0.8µm, depending on the desired active concentration.[5] As mentioned previously, literature does exist where implantation depths can be improved to ~1µm. Therefore, an implant depth of ~0.5µm was chosen to give a realistic assessment of the practical viability of the device. The desired implant profile is high ($1x10^{19}$ cm^{-3}) concentration near the surface to achieve an ohmic contact, with this concentration continuing as deep as possible to extend the length of the JFET region. To calculate the P+ implant profile, the Monte Carlo simulator calculates the depth that an implanted ion reaches within the SiC lattice based on a statistical approximation named the Binary Collision Approximation.[6] The Monte Carlo method is used to select essentially two random processes: first the initial distribution of started ion trajectories and the second one the position deviation of the lattice atoms due to the thermal vibrations.

There are two processes stopping the ions: (i) screened Coulomb interaction with the nucleus of the host atoms. [2] This includes the deviation from the atoms equilibrium position due to the thermal vibrations (ii), the energy lost by implanted ions due to the electrons (this is the most important energy loss process especially at high implant energies [3]). This process can be local i.e. related to the selected target atom, or non-local depending on the length of flight. Another effect in SiC is the plane of the material being targeted by implantation, as some have denser atomic lattices than others. This is important to consider when angled implantation is being used.

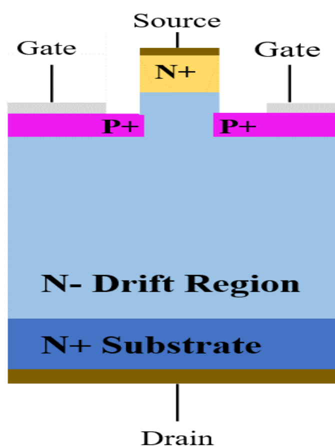

Fig. 1.1. Diagram of a trench JFET unit cell.

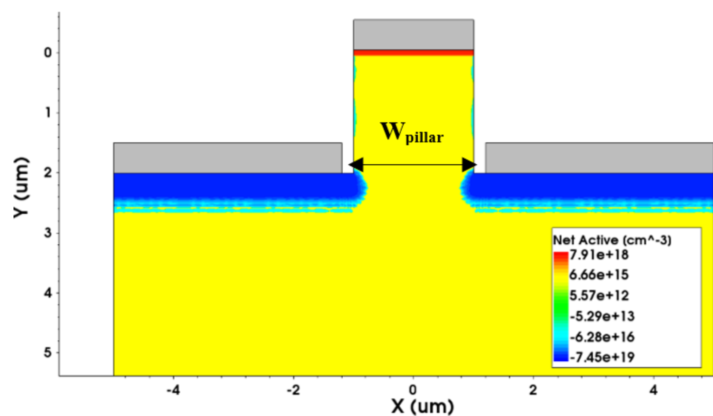

Fig. 1.2. Trench JFET unit cell modelled in Sentaurus TCAD showing Monte Carlo implantation for P+ regions.

The calculation of the current voltage characteristics uses the drift-diffusion formalism in concomitance with Poisson equation.[7] Fermi-Dirac statistics are used due to the high carrier concentrations (>10^{19} cm^{-3}) in the active region of the device in the on-state. Bandgap narrowing is also active.[8] Both Shockley-Read-Hall and Auger carrier recombination models are used to model recombination at high carrier concentrations.[9] The effects of impurity scattering, interface degradation & velocity saturation on the carrier mobility are enabled, including the effects of anisotropy due to the 4H-SiC lattice.[6, 7] The Okuto-Crowell impact ionization model is used for breakdown simulations.[8, 9] Incomplete ionisation models were not used in these simulations.

The threshold voltage calculations have been completed at a constant drain bias of V_{ds} = 1V. The threshold voltage has been extracted at the point of maximum transconductance, also known as the transconductance-change method.[14] For the V_{br} measurements, the gate was set at the given V_{gs} value between -20V and -60V before the drain ramp was completed.

Results and discussions

In order to design a JFET with the target V_{th} of -3V, it is necessary to investigate the dependence of the V_{th} on N_d and W_{pillar}. Fig. 2.1. depicts the results of the calculations of V_{th} as a function of both N_d and W_{pillar}. Three N_d values are used to reflect the potential ±20% variance in drift doping: $3.2x10^{15}$ cm^{-3}, $4x10^{15}$ cm^{-3} and $4.8x10^{15}$ cm^{-3}. As can be seen from the figure, increasing W_{pillar} whilst keeping N_d constant results in a large (more negative) V_{th}. When keeping W_{pillar} constant and varying N_d, the same effect is observed. The drift region thickness used for all simulations was 11µm.

Anomalous behaviour is observed at W_{pillar} = 2.4µm, where V_{th} reduces when compared to a thinner W_{pillar} = 2.3µm. This demonstrates the sensitivity of V_{th} to the realization of disorder in the distribution of the implanted P+ regions doping profile. Fig.2.2. and Fig. 2.3. show the doping profiles for W_{pillar} = 2.3µm and W_{pillar} = 2.4µm, respectively. The minimum distance between the P+ regions has been measured and is actually slightly smaller in the W_{pillar} = 2.4µm structure. This example shows the vulnerability of the JFET to the random fluctuation of dopants which can significantly impact the reliability of the threshold voltage. Some encroachment into the pillar by the P+ can be observed in Fig. 2.2. and Fig. 2.3. This is due to the trench etch and P+ implant being modelled as self-aligned processes. It may be possible to reduce this encroachment by increasing the thickness of the oxide mask that has been used.

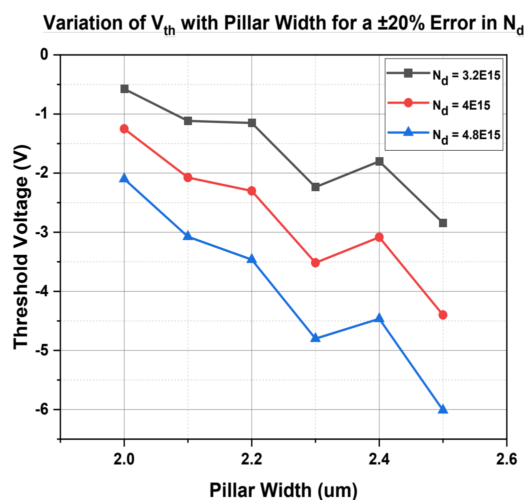

Fig. 2.1. Variation of the threshold voltage with W_{pillar} and N_d.

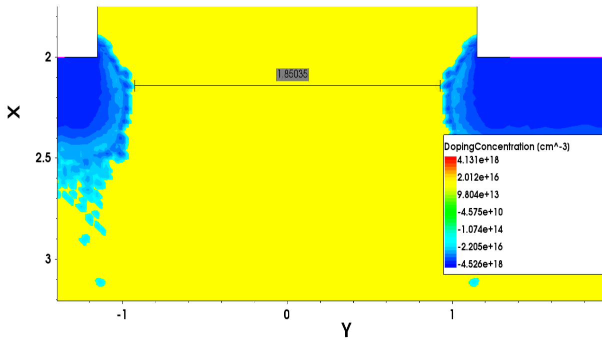

Fig. 2.2. Measured distance of 1.85μm between adjacent P+ implants for W_{pillar} = 2.3μm.

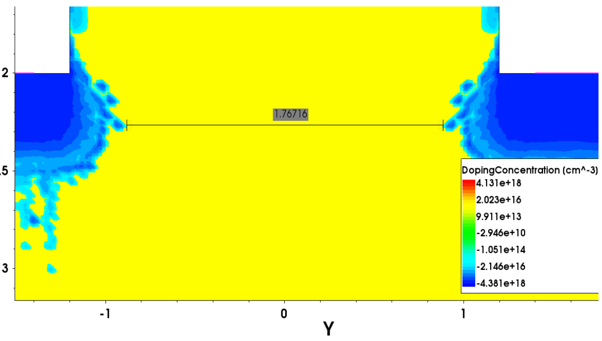

Fig. 2.3. Measured distance of 1.77μm between adjacent P+ implants for W_{pillar} = 2.4μm.

Additionally, to illustrate how W_{pillar} and applied V_{gs} influence the current level of the device in the on-state, I_{ds}-V_{ds} characteristics have been calculated for both W_{pillar}=2.2μm and 2.4μm for V_{gs} = 0V, -1V and -2V; for all simulations, the N- drift doping was $4x10^{15}$ cm^{-3}. These current-voltage characteristics are shown in Fig. 3. The smaller W_{pillar} results in a smaller current per unit length at a given V_{ds} & V_{gs}. The calculations show that a reduction of 0.2μm in $W_{channel}$ results in a ~33% reduction in drain current at V_{ds} = 10V. In addition, a more negative V_{gs} reduces the effective channel width as the depletion region of the gate P/N junctions extends further into the channel.

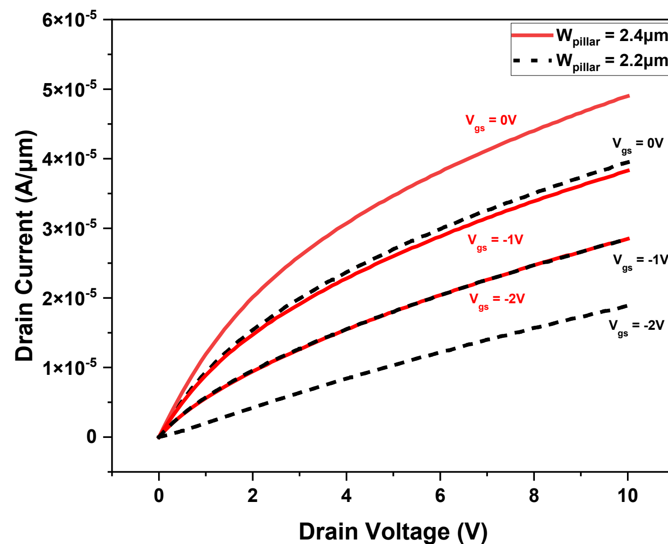

Fig. 3. Output characteristics for W_{pillar} = 2.2μm and 2.4μm at V_{gs} = 0V, -1V and -2V. When negative V_{gs} is increased, the magnitude of the drain current decreases.

Breakdown voltage calculations have been completed for a JFET structure with N_d = $4x10^{15}$ cm^{-3} and W_{pillar} = 2.4μm. This combination of values has been chosen as it provided the closest threshold voltage fit to the target $V_{th} \approx -3V$ whilst maximizing the pillar width. For the fabrication of the testing device it is preferable to have larger pillars to avoid the need of tight lithography tolerances. These breakdown calculations are shown in Fig. 4 which plots $I_{ds(off)}$ - V_{ds}. As can be seen in the figure, the drain voltage at which this failure occurs increases with the V_{gs} applied. This dependence of V_{br} on V_{gs} in vertical JFETs has been presented in existing literature [15]. However, what cannot be inferred from Fig.4. is the failure mechanism of the JFET, and if this varies depending on the V_{gs} applied. In order to illustrate this point, The 2D current density profile at the point of breakdown for V_{gs} = -20V is shown in Fig. 5.1. The figure shows a large current going from source to drain instead of the standard gate-drain breakdown at the P+/N junction due to high electric field, resulting in avalanche generation of carriers. This can be confirmed by the fact that the maximum electric field observed at

breakdown is less than 1 MV/cm. Fig. 5.2. shows the 2D profile of the electric field magnitude at the point of breakdown for V_{gs} = -20V.

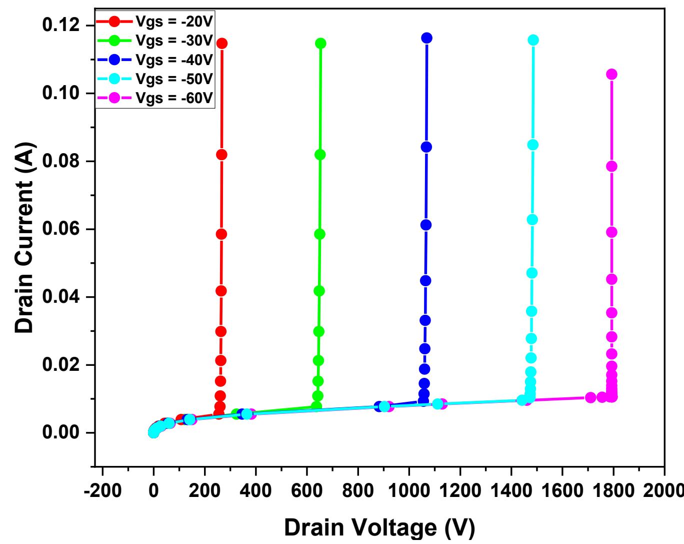

Fig. 4. JFET breakdown voltage calculations at V_{gs} values ranging from V_{gs} = -20V to -60V (W_{pillar} = 2.4µm, N_d = 4x10^{15} cm^{-3}).

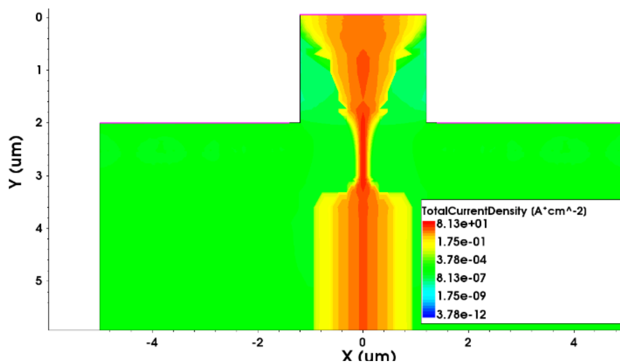

Fig. 5.1. Total Current Density magnitude at point of breakdown for V_{gs} = -20V (W_{pillar} = 2.4µm, N_d = 4x10^{15} cm^{-3}).

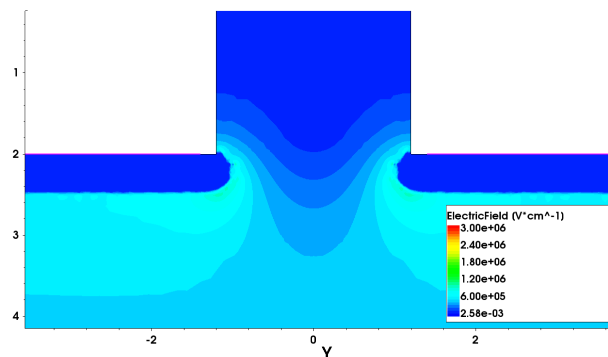

Fig. 5.2. Electric Field magnitude at point of breakdown for V_{gs} = -20V (W_{pillar} = 2.4µm, N_d = 4x10^{15} cm^{-3}).

We do not observe the standard failure mechanism until V_{gs} = -60V, where we observe the current path between the gate and drain as shown in the 2D current profile in Fig. 6.1. When plotting the 2D electric field profile, it is evident that the critical electric field magnitude for 4H-SiC (~3MV/cm) has been reached, and avalanche generation of carriers has occurred. This is illustrated in Fig. 6.2. It must be noted that the scale used for both Fig. 5.2. and Fig. 6.2. has been adjusted to 3 MV/cm for ease of viewing. The breakdown occurs first in the left gate junction. This asymmetry is a result of the difference in the P+ doping profile configuration between the left and right gate and the non-linearity of the avalanche breakdown mechanism.

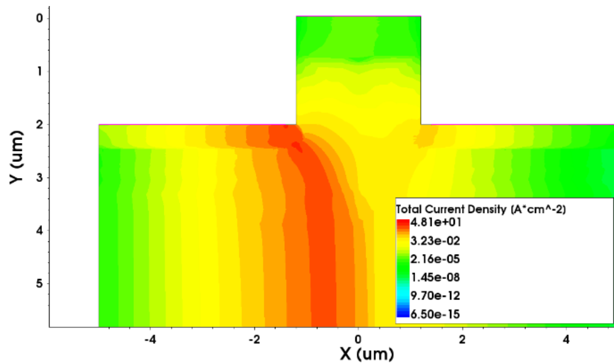

Fig. 6.1. Total Current Density magnitude at point of breakdown for V_{gs} = -60V (W_{pillar} = 2.4µm, N_d = 4x10^{15} cm^{-3}).

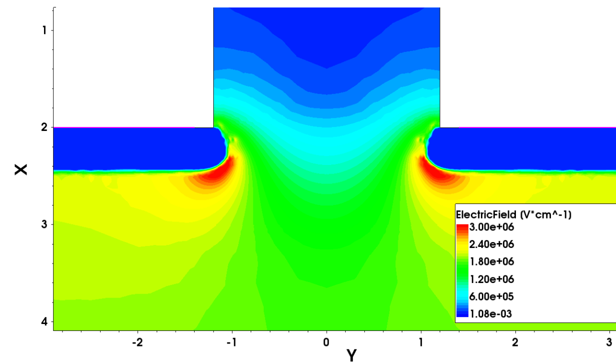

Fig. 6.2. Electric Field magnitude at point of breakdown for V_{gs} = -60V (W_{pillar} = 2.4µm, N_d = 4x10^{15} cm^{-3}).

The explanation for this premature failure mechanism is a short channel effect named Drain Induced Barrier Lowering (DIBL) [16]. DIBL is caused by the length of the blocking region of the JFET being equal to the depth of the P+ region (0.5µm). As the blocking region of the device is so short, the barrier height established when the JFET is turned off is not sufficient to prevent band bending caused when high drain bias is applied. Thus, the barrier cannot effectively block the channel, causing a low resistance current path to be established and the JFET to cease blocking voltage. This short channel effect can also be seen in the output characteristics shown in Fig.3. previously, as there is not a clearly defined saturation region. However, by applying larger negative gate voltage the blocking voltage can be dramatically improved e.g. V_{gs} = -60V results in a 1800V breakdown voltage, a 9-fold increase compared with the V_{gs} =-20V result.

Conclusions

We have carried out drift diffusion simulations of Vertical JFET using a realistic implant doping profile. The device has been designed to achieve a threshold voltage of -3V. In addition, we have calculated the effect of the drift region doping and width of the pilar on the V_{th}. Then for a selected doping and pillar width, the dependence of the V_{br} on V_{gs} have been illustrated. We observed two different failure mechanisms. At large negative V_{gs} we obtained the standard failure in the P+/N junctions, however at low negative V_{gs}, the poor channel control induced by the short effective channel length causes the failure. Therefore, we can conclude that using this vertical JFET design constrained by the P+ junction depth, it is unfeasible to have a threshold voltage greater than or equal to -3V whilst also providing acceptable blocking capability larger than 200V. However, for devices which aims to block around 200 volts, this JFET offers better power handling and compactness compared to its Si counterpart. If the application allows, increasing this negative gate bias can provide much improved blocking performance. The main highlight of this paper is that the junction depth of 0.5µm is incredibly vulnerable to doping fluctuations and short channel effects for moderate gate and drain biases.

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