Development of Silicon Carbide Devices for Next-Generation Surge Protection and Power Electronics

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This dissertation is submitted for the degree of
Engineering Doctorate

June 2025

Declaration

Declarations

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

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This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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June 2025

Acknowledgements

Firstly, I would like to thank both of my EngD supervisors: Professor Mike Jennings and Associate Professor Antonio Martinez. Without both of them, completing this EngD in the exciting field of Silicon Carbide power devices, which has exposed me to cutting edge technology and physics would not have been possible. In particular, I'd like to thank Mike for always having an open door to offer guidance, and for lending his extensive expertise in SiC during many insightful conversations. Mike - I can't thank you enough, I look forward to working with you in the future!

I also must give huge thanks to Antonio, who showed me (and schooled me) in the art of simulating semiconductor devices. The extensive meetings and whiteboard drawings in his office definitely taught me almost all of what I have learnt and understand about semiconductor physics. Antonio - I hope one day I can pass this knowledge onto someone else, and I'm at least half as good at it as you.

Next, I must also thank Dr Jon Evans, who's insight and help with mask and process design was invaluable. Jon has offered me guidance on all aspects of my fabrication and characterisation work, and I have benefited greatly from his knowledge and assistance in the cleanroom and in the electrical test lab. I hope our professional relationship will continue long into the future, even if involves GaN.

For critiquing my lunch choices and educating me on sumo wrestling, I would like to thank Dr Ryan Bigham, Mark Williams and Dan Winkley. Dan may be the terror of the Tesco's reduced section, but him and Gareth Blayney almost single-handedly kept the building lights on, and us cleanroom users alive - thank you both.

I would also like to extend my gratitude to internal collaborators Nick Burridge, and Dr. Ahmed Ben Khaial for assisting me with wafer dicing and metal deposition requirements respectively throughout the project. I also wish to thank our outside collaborators at IMB-CNM Barcelona, lead by Dr Amador Peréz-Tomás for assistance with SiC activation annealing.

Finally, I would like to thank my family for the never-ending support and inspiration for me to finish this degree. Without you, I would've never been able to come this far without your understanding and help. You've always believed in me, and I can't thank you enough.

Abstract

Silicon Carbide (SiC) power devices are becoming popular in a variety of different applications, however one un-tapped sector for SiC is the circuit protection market. Specifically depletion-mode SiC JFETs could be utilised in over-current/voltage protection products such as Bourns' *Transient Blocking Unit* (TBU®) product line to enhance efficiency, and penetrate previously unfeasible high voltage markets.

This thesis investigates and begins the development of 4H-SiC JFETs specifically designed for the TBU® application. Extensive optimisation of the JFET cell and termination design are explored using finite-element simulations. The trade-off between JFET off-state performance and design parameters is identified.

For the first time, Short Channel Effects (SCEs) are comprehensively shown to affect JFET behaviour when the channel length is short. In particular, JFET breakdown voltage can be degraded to only 50V for a 1200V drift region if channel length is short. It is demonstrated that by introducing sidewall P-type implants, the JFET channel can be extended without requiring high implantation energies, and completely eliminates the premature device failure caused by SCEs. This is demonstrated to improve breakdown voltage by 1000V in some cases.

A new 4H-SiC JFET design integrating a temperature sensor on the semiconductor surface is also demonstrated using finite-element simulations. The sensor consists of a lateral P-type resistor formed simultaneously with the P+ gate junction. Electrothermal simulations were employed to consider device self-heating effects showed the sensor had an R^2 of 0.996, which is comparable to other 4H-SiC temperature sensors. The sensor was also shown to be stable under high drain bias when blocking, with I_{sens} only varying by 4% between V_d= 0V and 1000V.

Process optimization was also completed on three key elements of the JFET fabrication process: carbon capping layers used for surface protection, P-type implant activation, and P-type ohmic contacts. The P+ gate junction is a fundamental part of the JFET unit cell structure. It was found that T_{anneal}= 1700°C resulted in the highest percentage of implanted dopants becoming electrically, with 26.9% activation. Furthermore, it was also found that

ohmic contacts using the Ti/Al/Ni metal scheme offered the lowest specific contact resistivity of $4.91 \times 10^{-6} \Omega cm^2$, which was achieved after annealing at 1050°C for 2 minutes.

List of Publications

Journal Publications

[1] F. Monaghan, A. Martinez, J. Evans, C. Fisher, and M. Jennings, "On short channel effects in high voltage jfets: A theoretical analysis," *Power Electronic Devices and Components*, vol. 7, p. 100057, 2024.

[2] F. Monaghan, A. Martinez, J. Evans, C. Fisher, and M. Jennings, "A 4h-sic jfet with a monolithically integrated temperature sensor," *Power Electronic Devices and Components*, vol. 8, p. 100069, 2024.

[3] F. Li, F. Roccaforte, G. Greco, P. Fiorenza, F. La Via, A. Pérez-Tomas, J. E. Evans, C. A. Fisher, F. A. Monaghan, P. A. Mawby, *et al.*, "Status and prospects of cubic silicon carbide power electronics device technology," *Materials*, vol. 14, no. 19, p. 5831, 2021.

Conference Publications

[1] F. Monaghan, A. Martinez, C. Fisher, and M. Jennings, "Impact of dimensions and doping on the breakdown voltage of a trench 4h-sic vertical jfet," *Key Engineering Materials*, vol. 948, pp. 69–75, 2023.

[2] F. Monaghan, A. Martinez, J. E. Evans, C. Fisher, O. J. Guy, and M. Jennings, "Design of monolithically integrated temperature sensors in 4h-sic jfets," *Key Engineering Materials*, vol. 984, pp. 47–54, 2024.

[3] B. Jones, J. Mitchell, J. Evans, F. Monaghan, M. Jennings, C. Bolton, K. Riddel, H. Ashraf, and O. J. Guy, "Introducing foundry-compatible sic and gan trench processing technologies for reliable automotive application," in *Materials Science Forum*, vol. 1062, pp. 582–587, Trans Tech Publ, 2022.

[4] B. Jones, A. Croot, J. Mitchell, C. Bolton, J. E. Evans, F. Monaghan, K. Riddell, M. Jennings, O. J. Guy, and H. Ashraf, "Demonstrating sic in situ rounded trench processing technologies for future power trench mosfet applications," *Solid State Phenomena*, vol. 359, pp. 163–170, 2024.

[5] J. Evans, J. Patel, A. Ben Khaial, N. Burridge, R. Hyndman, F. Monaghan, M. Jennings, H. Ashraf, R. Harper, and M. Elwin, "Fabrication of quasi-vertical gan-on-sic trench mosfets," *Key Engineering Materials*, vol. 945, pp. 61–66, 2023.

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Nomenclature

Greek Symbols

ε_s	Relative Dielectric Constant
η	Diode Ideality Factor
μ	Carrier Mobility (cm^2/Vs)
ϕ_b	Schottky Barrier Height (eV)
ρ	Resistivity (Ωcm)
ρ_c	Specific Contact Resistance (Ωcm^2)
ρ_d	Drift Region Resisitivty (Ωcm)
ρ_{2DEG}	HEMT 2DEG Resistivty (Ω/sq)
ρ_{JFET}	JFET Region Resistivty (Ωcm)
ρ_{N+}	N+ Source Region Resistivty (Ωcm)
ρ_{sub}	Substrate Resisitvity (Ωcm)

Subscripts

ΔI_{sens}	Variation in Sensor Current (%)
A_c	Contact Area (cm^2)
BV_{pp}	Parallel Plane Breakdown Voltage (V)
D_{it}	Near Interface Traps ($cm^{-2}eV^{-1}$)
E_c	Critical Electric Field (MV/cm)

E_g	Bandgap Energy (eV)
E_{00}	Charcteristic Energy (eV)
E_{act}	Dopant Activation Energy (eV)
$E_{av,lat}$	HEMT Average Lateral Electric Field (MV/cm)
$E_{ion,0}$	Ionization Energy of Isolated Impurity Centre (eV)
E_{ion}	Dopant Ionization Energy (eV)
I_a	Anode Current (A)
I_f	Diode Forward Current (A)
I_r	Diode Reverse Current (A)
I_s	Saturation Current (A)
$I_{d,off}$	Off-state Drain Current (A/μm)
I_{sens}	Sensor Current (A)
J_d	Drain Current Density (A/cm^2)
J_n	Electron Current Density (Acm^{-2})
J_p	Hole Current Density (Acm^{-2})
L_d	HEMT Drain Contact Length (μm)
L_g	HEMT Gate Length (μm)
L_g	Mesa Spacing (μm)
L_s	HEMT Source Contact Length (μm)
L_T	Transfer Length (μm)
L_{gd}	HEMT Gate-Drain Spacing (μm)
L_{gs}	HEMT Gate-Source Separation (μm)
m_h	Hole Effective Mass (kg)
N_a	Acceptor Doping Concentration (cm^{-3})

N_c Density of states of the conduction band (cm^{-3})

N_d Doping Concentration (cm^{-3})

n_i Intrinsic Carrier Concentration (cm^{-3})

N_v Density of states of the valence band (cm^{-3})

N_{csl} Carrier Storage Layer Doping Concentration (cm^{-3})

p_{corr} Corrected free hole concentration (cm^{-3})

q_{ox} Oxide Charge (cm^{-2})

R_c Contact Resistance (Ω)

R_g HEMT Gate Resistance (Ωcm^2)

R_H Hall coefficient

r_H Hall scattering factor

R_T TLM Resistance (Ω)

$R_{cd,sp}$ Drain Contact Resistace (Ωcm^2)

$R_{cs,sp}$ Source Contact Resistance (Ωcm^2)

$R_{drift,sp}$ Drift Region Resistance (Ωcm^2)

R_{gd} HEMT Gate-Drain Resistance (Ωcm^2)

R_{gs} HEMT Gate-Source Resistance (Ωcm^2)

$R_{JFET,sp}$ JFET Region Resistance (Ωcm^2)

$R_{N+,sp}$ N+ Source Region Resistance (Ωcm^2)

$R_{on,ideal}$ Ideal Specific On-resistance (Ωcm^2)

$R_{on,JFET}$ JFET On-state Resistance (Ω)

$R_{on,MOSFET}$ MOSFET On-state Resistance (Ω)

$R_{on,sp(HEMT)}$ HEMT On-state Resistance (Ωcm^2)

$R_{on,sp}$ Specific On-state Resistance (Ωcm^2)

R_{on} On-state Resistance (Ω)

R_{semi} P-type Bulk Resistance (Ω)

R_{sens} Sensor Resistance (Ω)

R_{sh} Sheet Resistance (Ω sq)

T_i Intrinsic Temperature (K)

T_j Junction Temperature (K)

T_{anneal} Activation Anneal Temperature (°C)

$T_{contact}$ Contact Anneal Temperature (°C)

t_{imp} Implanted Layer Thicknesss (nm)

t_{sub} Substrate Thickness (μm)

V_a Anode Voltage (V)

V_c Cathode Voltage (V)

V_f Diode Forward Voltage (V)

V_g Gate Voltage (V)

V_H Hall Voltage (V)

V_{bi} Built-in Potential (V)

V_{br} Diode Breakdown Voltage (V)

$V_{ds,MOSFET}$ MOSFET Drain Voltage (V)

$V_{gs,JFET}$ JFET Gate Voltage (V)

V_{s1} Sensor Contact 1 bias (V)

V_{s2} Sensor Contact 2 bias (V)

V_{th} Threshold Voltage (V)

W_0 Zero Bias Depletion Width (μm)

W_{cell} Cell Pitch (μm)

W_{cs} Source Contact Width (μm)

W_{JFET} JFET Region Width (μm)

W_{pp} Parralel Plane Depletion Width (μm)

x_j Gate junction depth (nm)

x_{JFET} JFET Region Length (μm)

x_{N+} N+ Source Region Thickness (μm)

Other Symbols

A Region Area (μm^2)

a Effective JFET Region Width (μm)

$A^\star$ Richardson's Constant ($/cm^2K^2$)

A_{diode} Diode Area (cm^2)

C CTLM Correction Factor

d TLM Spacing (μm)

G Net Carrier Generation Rate ($cm^{-3}s^{-1}$)

h Plancks' Constant (Js)

k Boltzmann constant (J/K)

L Region Length (μm)

n Free Electron Concetration (cm^{-3})

p Free Hole Concentration (cm^{-3})

q Electron Charge (C)

R Net Recombination Rate ($cm^{-3}s^{-1}$)

r CTLM Contact Radius (μm)

S	Adjacent Field Ring Spacing (μm)
T	Temperature (K)
t	Drift Region Thickness (μm)
Z	TLM Contact Height (μm)

Acronyms / Abbreviations

β-Ga_2O_3	Gallium Oxide
O_2	Oxygen
SiO_2	Silicon Dioxide
2DEG	2-dimensional Electron Gas
AFM	Atomic Force Microscopy
AI	Artificial Intelligence
BFOM	Baliga's Figure of Merit
BPD	Basal Plane Dislocation
BV	Breakdown Voltage
C	Carbon
CMOS	Complementary Metal-Oxide Semiconductor
CSL	Carrier Storage Layer
CTLM	Circular TLM
DIBL	Drain Induced Barrier Lowering
FE	Field Emission
FFR	Floating Field Ring
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

IPA Isopropyl Alchohol

JBS Junction Barrier Schottky

JFET Junction Field Effect Transistor

JTE Junction Termination Extension

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MW JFET Channel Width

Ni Nickel

NO Nitric Oxide

PL Photoluminescence

$POCl_3$ Phosphorous Oxychloride

PR Photoresist

RCA Radio Corporation of America

RIE Reactive Ion Etching

RTA Rapid Thermal Annealing

RT Room Temperature

SBD Schottky Barrier Diode

SBI Schottky Barrier Height Inhomogenity

SCE Short Channel Effects

SCR Specific Contact Resistance

SEM Scanning Electron Microscopy

SF Stacking Fault

SH Self-Heating

SiC Silicon Carbide

SIMS	Secondary Ion Mass Spectrometry
Si	Silicon
SJ	Super Junction
SMU	Source Measure Unit
SRIM	Stopping Range of Ions in Matter
SSF	Shockley Stacking Fault
TBU	Transient Blocking Unit
TCAD	Technology Computer-Aided Design
TED	Threading Edge Dislocation
TE	Thermionic Emission
TFE	Thermionic Field Emission
TLM	Transfer Length Method
TSD	Threading Screw Disloaction
TSEP	Temperature Sensitive Electrical Parameter
VDP	Van Der Pauw
WBG	Wide Band Gap

Chapter 1

Introduction

1.1 Background

Society is becoming increasingly dependent on electricity due to a number of factors. These include the widespread adoption of technology in everyday life: from your mobile phone and smart watch, to electric vehicles and their charging stations. Furthermore, the increased digitization of technology has resulted in data centres becoming increasingly important. Also, the recent mega-trend of Artificial Intelligence (AI), while promising to advance us as a species is placing further demand on existing energy infrastructure. A key example of this is utilising machine learning and to develop large language models, such as ChatGPT.

Increased use of electricity can certainly be seen as a net good, especially when trying to reduce our reliance on fossil fuels. However, all of the trends stated above are contributing to a massive increase in global electricity demand. In fact, the International Energy Agency has forecast data centre and AI power consumption to double by 2026 [2]. In the UK, data centre power use is expected to increase by six-fold in the next 10 years [3]. Overall, worldwide energy demand is expected to increase 57% from 2020 levels to 35407TWh in 2040 [4].

Although increased electricity generation capacity is certainly required, making the transmission systems which supply all of these applications more efficient is equally, if not more important. This involves power electronic systems. It is estimated that 50% of the world's electricity is controlled by a power electronic system [5].

Unfortunately, current power electronics infrastructure is not optimal, leading to energy is losses during transmission because of the limited efficiency of power semiconductor devices. Take for example the AC/DC converter contained within a laptop charger. Due to the non-ideal efficiency of the power devices used in the charger, energy is lost as heat causing the charger to get warm and requiring more energy.

Another category of power electronic circuits expected to experience increased demand due to the boom in data centre growth is circuit protection products, such as Bourns' *Transient Blocking Unit* or *TBU*® product line. The TBU provides valuable over-current and over-voltage surge protection for the telecoms industry, and server banks used in data centres.

To improve the performance of various power electronic circuits, including the TBU, it is essential to improve the performance of the transistors utilized in these circuits. For the past 60 years, power transistors have almost exclusively been fabricated using silicon. However, the performance limits of silicon devices is fast approaching. Replacing silicon with wide bandgap (WBG) semiconductors can result in substantial performance improvements due to the superior material properties of WBG materials. This, in turn will significantly boost system efficiency and reduce energy waste in both converter and circuit protection applications.

1.2 Wide Bandgap Semiconductors: Comparing to Silicon

1.2.1 Preface

This section analyses how semiconductor material properties translate to device efficiency. The two commercially ready WBG materials: Silicon Carbide (SiC) and Gallium Nitride (GaN) are directly compared to silicon to quantify the potential performance improvements they can provide.

Table 1.1 shows the most relevant electrical properties for each of the materials, with a select number plotted in the radar diagram shown in figure 1.1. It should be noted that SiC has over 250 polytypes [6], but the 4H polytype is the only polytype which is commercially available. Therefore, 4H-SiC is the only polytype of SiC considered in this comparison.

Although the potential benefits of using these materials are very attractive to device and system designers alike, both materials are relatively immature and expensive when compared to silicon, which has been used for over 60 years. Thus, a review of the current state of the art in SiC and GaN is completed, particularly focused on the popular device types including SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Junction Field Effect Transistors (JFETs) and GaN High Electron Mobility Transistors (HEMTs).

1.2.2 Bandgap Energy

In semiconductors, between the lower (valence) and upper (conduction) energy bands, there exists a forbidden region in which states can not exist. The separation between the lowest conduction band and upper-most valence band is defined as the *Bandgap Energy* (E_g) [7].

Table 1.1 Comparison of fundamental material properties for silicon, 4H-SiC and GaN.

Property	Silicon	4H-SiC	GaN
Bandgap Energy (eV)	1.11	3.26	3.44
Critical Electric Field (MV/cm)	0.2	2.5	3.3
Relative Dielectric Constant	11.7	10	10.4
Bulk Electron Mobility (cm^2/Vs)	1360	1140	1000
Saturation Velocity (10^7cm/s)	1	2	2.5
Thermal Conductivity (W/cmK)	1.5	4.5	1.3
DOS of Conduction Band (cm^{-3})	2.8×10^{19}	1.23×10^{19}	2.3×10^{18}
DOS of Valence Band (cm^{-3})	1.04×10^{19}	4.58×10^{19}	4.6×10^{18}

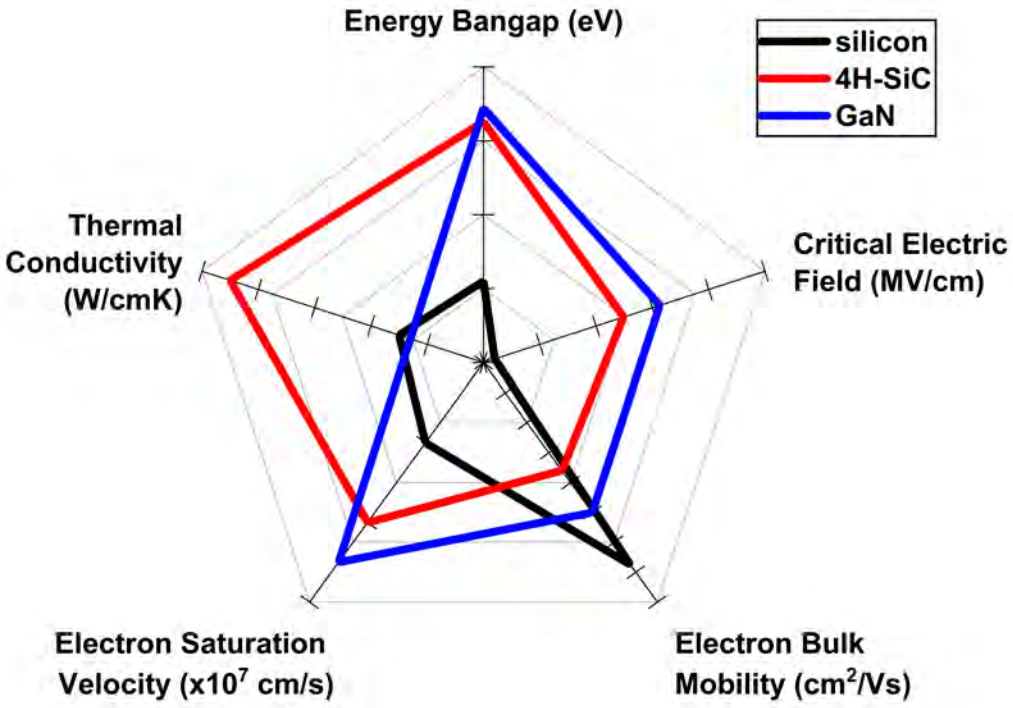


Fig. 1.1 Radar plot of key material properties of all three semiconductors, using values from table 1.1.

Electron-hole pairs are thermally generated across the bandgap. The concentration of thermally generated electron-hole pairs is known as the *intrinsic carrier concentration* (n_i), which can be calculated using equation (1.1) below, where N_c and N_v are the density of states for the conduction and valence bands, respectively. The Boltzmann constant is denoted as k, and T is the lattice temperature.

$$n_i = \sqrt{N_c N_v} \exp\left(\frac{-E_g}{2kT}\right) \tag{1.1}$$

In practice, the larger E_g is, the smaller n_i becomes. This means that materials with larger bandgaps will have lower intrinsic carrier concentrations at any given temperature. This is significant because when n_i approaches the magnitude of the doping concentration in a semiconductor, thermal generation of carriers becomes the dominant carrier generation mechanism. The temperature which this occurs is the intrinsic temperature (T_i).

Above T_i, carrier concentration increases exponentially, which leads to a sudden massive increase in current density [7]. Increased current density results in large power dissipation within the device, due to its internal resistance. This power is dissipated as thermal energy, heating the device up. This becomes a positive feedback loop, which causes thermal runaway and destructive failure of devices [8]. The intrinsic carrier concentration for all three materials is plotted as a function of temperature below in figure 1.2.

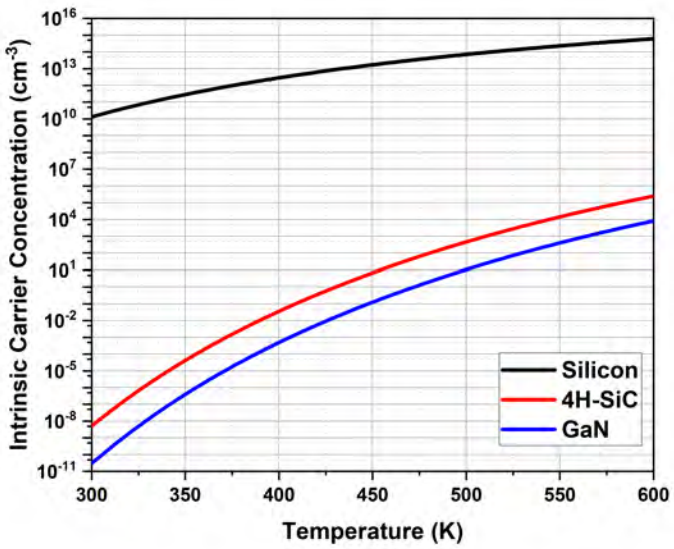


Fig. 1.2 Intrinsic carrier concentration plotted against temperature for silicon, 4H-SiC and GaN.

As shown in Figure 1.2, at 300K SiC has an intrinsic carrier concentration of $5.1 \times 10^{-9} cm^{-3}$, while for GaN has a $n_i = 2.93 \times 10^{-11} cm^{-3}$. In contrast, silicon has a n_i of $1 \times 10^{10} cm^{-3}$ at the same temperature. At 500K, these values increase to $7.35 \times 10^{13} cm^{-3}$ for silicon, $457 cm^{-3}$ for SiC, and $10.5 cm^{-3}$ for GaN. The substantial difference n_i between the WBG materials and silicon can be attributed to the Bandgap Energy, which is approximately three times larger than that of silicon.

If the doping concentration (N_d) in a device is $1 \times 10^{14} cm^{-3}$, silicon becomes intrinsic around 514K. In contrast, both SiC and GaN do not come remotely close to 10^{14}, even at 1000K. Therefore, devices made from wide bandgap materials such as GaN and SiC can theoretically operate at higher temperatures than their silicon counterparts.

A second and arguably more important property which is heavily influenced by n_i is the leakage current when the device is blocking voltage, also known as the *off-state leakage*. Ideally, when the device is off no current will be conducted at all. Practically, this isn't possible due to leakage paths in the device, and intrinsic carriers. Therefore, the smaller n_i of SiC results in SiC devices having lower off-state leakage current than silicon counterparts. This is highly desirable for designers, as reduced leakage current improves system efficiency.

1.2.3 Electric Field and Breakdown Voltage

Ideally, semiconductor devices would be able to block an infinite voltage when they are turned off. However, in reality, there is a material limit to the amount of voltage that a semiconductor layer of a given thickness can withstand, due to the electric field E within the layer. The electric field within the layer arises from the fundamental expression $E = \frac{\partial V}{\partial x}$. The maximum electric field that a semiconductor can withstand before failing is material dependent. If higher electric fields can be supported, thinner, highly doped layers can be used. This combination enables a device to have lower resistance, which leads to significant efficiency improvements when the device is conducting current.

The maximum electric field that a material can sustain before failing is known as critical electric field strength (E_c). Silicon Carbide and GaN have E_c values of 2.5 MV/cm and 3.3 MV/cm which are 12.5 and 16.5 times higher than silicon, respectively. Approximations for parallel-plane breakdown voltage (BV_{pp}) as a function of N_d for each of the three materials have been calculated by Baliga [5], using experimentally fitted parameters. These approximations are shown in equations 1.2 - 1.4, and are plotted across a range of N_d values in figure 1.3.

$$BV_{pp}(Silicon) = 4.43 \times 10^{13} N_d^{-0.75} \tag{1.2}$$

$$BV_{pp}(4H - SiC) = 1.7 \times 10^{15} N_d^{-0.75} \tag{1.3}$$

$$BV_{pp}(GaN) = 2.82 \times 10^{15} N_d^{-0.75} \tag{1.4}$$

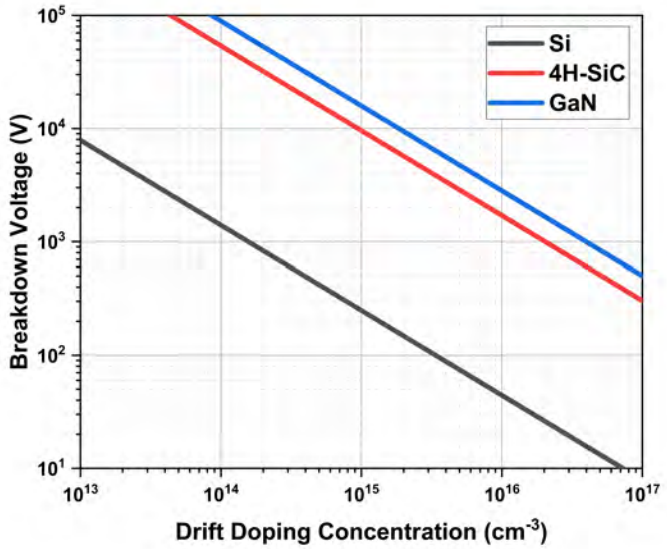


Fig. 1.3 Parallel plane breakdown voltage plotted as a function of drift doping concentration for silicon, 4H-SiC and GaN.

Figure 1.3 shows that SiC and GaN devices can utilise much higher doping concentrations for a given BV_{pp} compared to silicon due to their higher E_c values. To support a voltage of 1000V, silicon requires N_d= $1.6 \times 10^{14} cm^{-3}$, while SiC requires N_d= $2.04 \times 10^{16} cm^{-3}$ and GaN requires N_d= $3.98 \times 10^{16} cm^{-3}$. Practically, being able to use a higher N_d to support a given voltage reduces both the resistivity and layer thickness.

In practice, the resistivity (ρ) of the layers can be calculated using the fundamental resistivity equation is shown below in equation 1.5, where μ is carrier mobility and q is electron charge. When using the N_d values required to block 1000V shown above, resistivity is equal to 28.7Ωcm for silicon, 0.27Ωcm for SiC and 0.16Ωcm for GaN. The resistivity for silicon is 106 and 179 times higher than SiC and GaN, respectively.

$$\rho = \frac{1}{q\mu N_d} \tag{1.5}$$

The layer thickness must at minimum be as large as the depletion region at BV_{pp}, which is known as the parallel-plane depletion width (W_{pp}). Parallel-plane depletion width is related to doping concentration and BV_{pp}, as shown in equation 1.6. The approximations for W_{pp} are shown in equation 1.7 - 1.9.

$$W_{pp} = \sqrt{\frac{2\varepsilon_s BV_{pp}}{qN_d}} \tag{1.6}$$

$$W_{pp}(Silicon) = 2.39 \times 10^{10} N_D^{-0.875} \tag{1.7}$$

$$W_{pp}(4H - SiC) = 1.37 \times 10^{11} N_D^{-0.875} \tag{1.8}$$

$$W_{pp}(GaN) = 1.8 \times 10^{11} N_D^{-0.875} \tag{1.9}$$

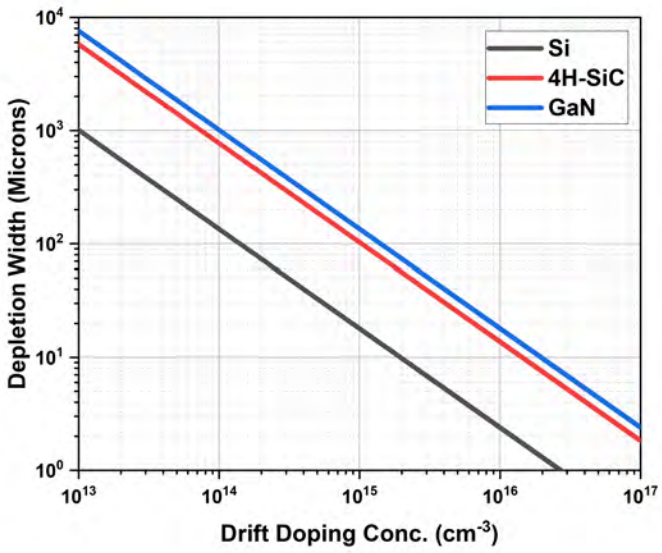


Fig. 1.4 Parallel plane depletion width plotted as a function of drift doping for silicon, 4H-SiC and GaN.

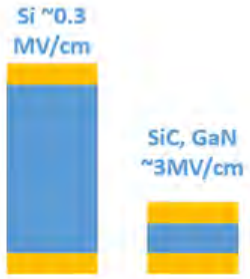


Fig. 1.5 Example cross-section of silicon, SiC and GaN layers designed to block the same voltage.

Figure 1.4 shows equations (1.7) - (1.9) plotted as a function of N_d. Lower doping concentrations deplete further at a given bias. Therefore, as silicon devices require lighter doping concentrations to block a given voltage as shown in figure 1.3, they also require thicker layers due to larger W_{pp}. For example, for the doping concentrations required to support 1000V, W_{pp}= 89μm for silicon, W_{pp}= 7.4μm for SiC and W_{pp}= 5.4μm for GaN. Figure 1.5 visualises what this practically looks like, as SiC and GaN drift layers can be ≤10% of the thickness required in silicon to block the same voltage.

1.2.4 Unipolar Limit

A useful method to assess the potential performance of a semiconductor is to calculate the ideal specific on-resistance ($R_{on,ideal}$), also known as *Baliga's Figure of Merit* (BFOM). This is the area-dependent resistance a layer will have when supporting a given voltage. This is essentially the theoretical performance limit of a unipolar device made of a given semiconductor, and is shown in equation 1.10 [9]. The relative dielectric constant is denoted as ε_s, and the electron mobility as μ_n. Electron mobility is used in this equation as electrons are the majority carrier for the vast majority of power devices.

$$R_{on,ideal}(BFOM) = \frac{4BV_{pp}^2}{\varepsilon_s \mu_n E_c^3} \tag{1.10}$$

This figure of merit takes into account the E_c of a material, and therefore N_d required to block a given voltage. Doping concentration and carrier mobility affect the resistivity of the material. However, as E_c has a cubic relationship, this is by far the most dominant parameter. The BFOM has been plotted as a function of BV_{pp} for silicon, 4H-SiC and GaN in figure 1.6 using values for E_c, ε_s and μ_n from table 1.1.

Ultra wide bandgap materials Gallium Oxide ($\beta - Ga_2O_3$) and Diamond are also plotted in figure 1.6 for reference. Both of these materials are relatively immature technologies, and as such suffer from significant material related problems such as highly defective substrates, which limits substrate size. In practice, although the theoretical performance limits of both materials are excellent, the actual performance of devices fabricated using these materials fall significantly short of these theoretical limit, and remain a long distance from commercial viability. Therefore, both Diamond and $\beta - Ga_2O_3$ are not considered going forward in this project.

Due to the far larger E_c values of SiC and GaN, the improvement in $R_{on,ideal}$ is substantial across the whole voltage range plotted in figure 1.6. At 650V silicon has a $R_{on,ideal}$ of 5.35Ωcm^2, compared to 58mΩcm^2 for SiC and 41mΩcm^2 for GaN. At 1200V, another key voltage rating for electric vehicle applications, $R_{on,ideal}$ = 18.2Ωcm^2, 197mΩcm^2 and

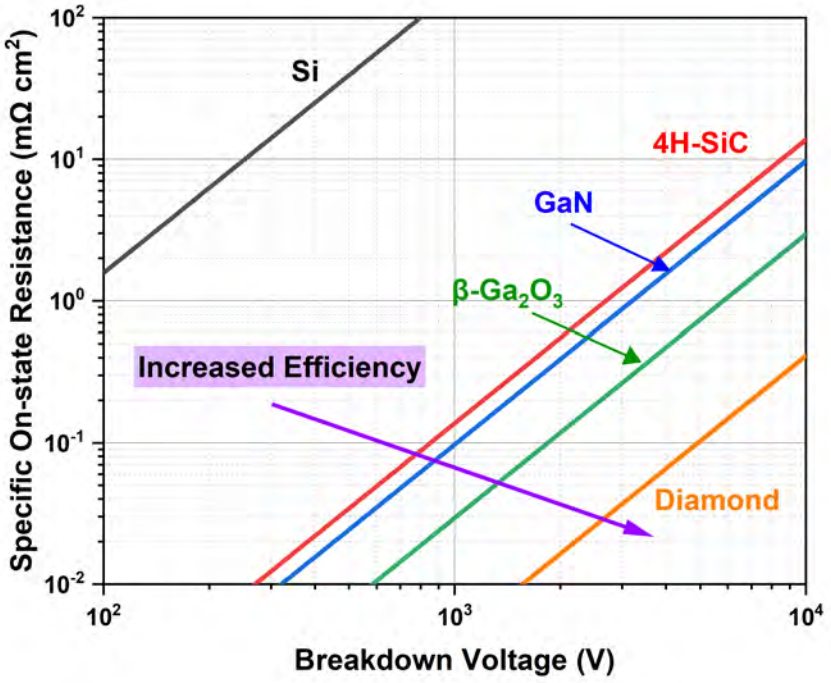


Fig. 1.6 The theoretical performance limits of unipolar devices for silicon and assorted wide bandgap materials.

139mΩcm^2 for silicon, SiC and GaN respectively. Therefore, the theoretical lowest resistance of a SiC device is 92 times lower than silicon at 1200V.

Silicon super-junction (SJ) MOSFETs have the benefit of being a unipolar device, while using charge-balancing to enable higher doped regions than normally possible to be used. This results in a device which breaks the unipolar limit, but can still switch at MOSFET frequencies. Silicon SJ MOSFETs are industry standard as of today, and are competing with SiC MOSFETs and GaN HEMTs, especially at 650V.

Figure 1.7 shows various reported specific on-resistance ($R_{on,sp}$) and breakdown voltages for different device types plotted against the unipolar limits for silicon, 4H-SiC and GaN HEMTs. Devices shown include: GaN HEMTs [10–15], Si SJ MOSFETs [16–21], SiC JFETs [22–30], Schottky barrier diodes (SBDs) [31–36], Junction barrier Schottky (JBS) diodes [37–39] and MOSFETs [40–46].

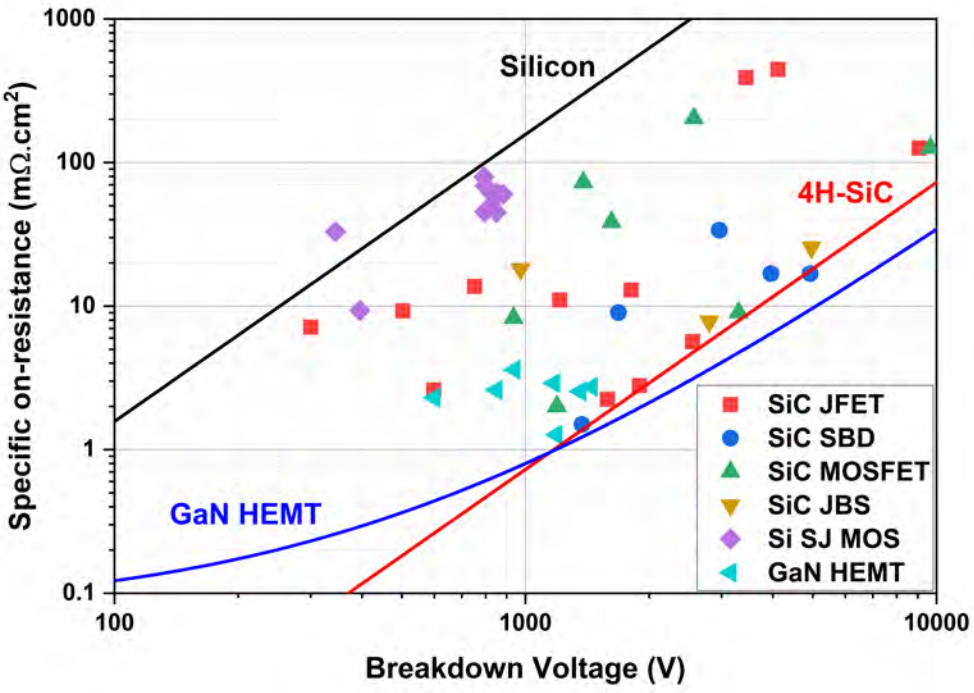


Fig. 1.7 Reported specific on-state resistance and breakdown voltages for GaN HEMTs, Si SJ MOSFETs and various SiC unipolar device types.

1.2.5 State of the Art: GaN

GaN HEMTs

While Gallium Nitride boasts a larger bandgap and higher critical field compared to SiC, it also offers a distinctive advantage: the formation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction. The 2DEG layer forms due to polarization effects in both materials - spontaneous and piezoelectric polarization. The polarization effects lead to an electric field with the material, and therefore an associated charge density [47]. Piezoelectric polarization occurs due to strain exerted on the lattices, as the materials have different lattice constants. Spontaneous polarization occurs even when the lattice is not strained, and has been observed to be significant in wurtzite group-III nitrides such as GaN and AlN [48]. The difference between the polarization effects in the materials causes a high density of polarization charge to form at the AlGaN/GaN interface, known as the 2DEG [49].

Electrons contained in this 2DEG layer have far higher mobility than the bulk mobility of GaN, typically around $2000 cm^2/Vs$. Electron mobilities of up to $2700 cm^2/Vs$ for GaN 2DEGs have been reported [50]. Gallium Nitride devices which utilise this 2DEG have

impressively low $R_{on,sp}$. These devices are known as HEMTs. These devices by nature are lateral devices, fabricated using GaN-on-Si wafers. This provides some key benefits such as monolithic integration of gate drivers, or even with Complementary Metal-Oxide Semiconductor (CMOS) [51, 52]. GaN HEMTs with integrated gate driver Integrated Circuits (ICs) have been commercialised by Cambridge GaN Devices [53].

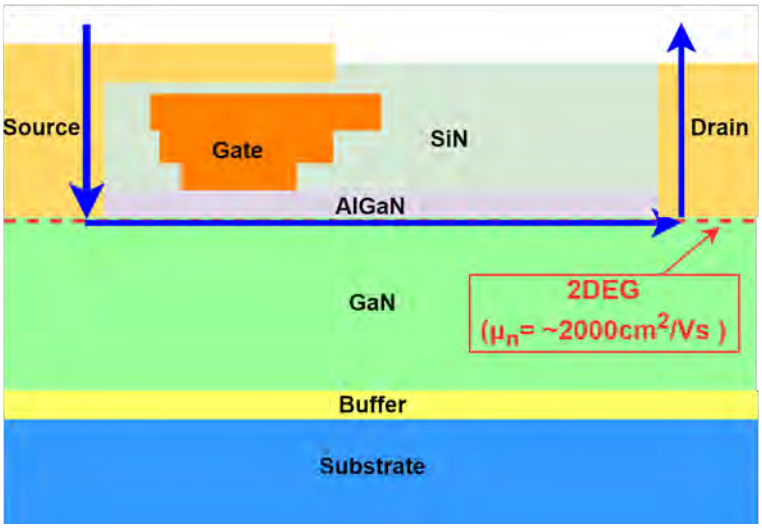


Fig. 1.8 Cross section of a typical depletion-mode GaN HEMT, with the current path indicated by blue arrows.

HEMTs are by default normally-on (depletion mode) devices, requiring negative gate voltage to be applied to turn the device off. Figure 1.8 shows the typical structure of a HEMT, highlighting the current flow in blue. Normally-on devices do not "fail open", which means if the gate driver fails the device doesn't conduct current. As HEMTs don't "fail-open", this means if the controlling driver fails, there is a chance of a short-circuit event which could be catastrophic. Techniques have been proposed to make HEMTs operate as normally-off (enhancement mode), which are "fail-open" devices. Enhancement mode devices are highly preferred by system designers. These include a P-type region under the gate, a recessed MOS gate and Fluorine implants [12, 54, 55]. Another alternative method of achieving normally-off operation is to use a cascode configuration. This involves using a low voltage silicon MOSFET in combination with a normally-on HEMT. This is discussed in more detail in section 1.4.

Multiple different manufacturers offer power HEMT products. Some focus on normally-off designs such as Infineon [56] and STMicroelectronics [57], while others including Transphorm [58] and Nexperia [59] use the cascode configuration.

When scaling HEMTs for higher voltage ratings, their lateral configuration poses several challenges, particularly when managing surface electric fields which requires field plate

structures [10, 60]. Increasing the gate-to-drain distance to support higher voltages results in impractically large devices, making them commercially unviable due to cost and yield issues.

Additionally, growing GaN on foreign substrates such as silicon introduces significant a lattice mismatch between materials, limiting the thickness of GaN layers and causing potential breakdowns through buffer layers [61, 62]. While 1200V HEMTs have been demonstrated on sapphire substrates by Transphorm [63], it is unlikely they will become competitive above this voltage. Other issues are still areas of active research in HEMTs, such as current collapse and dynamic on-resistance [64, 65].

Vertical GaN

At higher voltages, vertical devices such as power MOSFETs become more efficient to use than a lateral device like a HEMT. Furthermore, MOSFETs are normally-off devices and are seen as more of a "drop-in" replacement for silicon MOSFETs, unlike HEMTs.

Vertical GaN devices are currently a very active area of research. However, substrate sizes remain small (≤100mm). Both Vertical GaN PN diodes and SBDs have been reported with $R_{on,sp}$ values close to the GaN unipolar limit [66, 67]. Transistors, including 1200V JFETs [68] and trench MOSFETs [69, 70] have been reported. However, poor electrical activation of P-type currently hinders the channel mobility of GaN MOSFETs, with the record activation for traditional Rapid Thermal Annealing (RTA) at only 8.2% [71].

1.2.6 State of the Art: SiC

SiC MOSFETs

Silicon Carbide MOSFETs are now relatively mature devices, with commercial devices having been available since 2011, when Cree (now Wolfspeed) released the CMF20120D [72, 73]. Furthermore, both trench and planar MOSFETs are for sale, with manufacturers such as STMicroelectronics [74] sticking with planar designs, while Infineon [75] and Rohm [76] have developed trench products. Advanced device concepts such as SJ MOSFETs have been demonstrated by research groups [77, 78]. The typical structure of a trench MOSFET is shown in figure 1.9.

The Primary area of weakness for SiC MOSFETs is the poor quality of the SiC-Silicon dioxide ($Si0_2$) gate interface. The presence of a high density of near-interface traps (D_{it}) results in effects such as threshold voltage (V_{th}) drift over operational lifetime [79], which is deeply concerning for system designers. The D_{it} of commercial SiC MOSFETs has been measured as $9.3 \times 10^{12} cm^{-2} eV^{-1}$ by Yu et al. [80], which is 100 times higher than in Si MOSFETs. In practice, a positive shift in V_{th} can result in an increased on-state resistance,

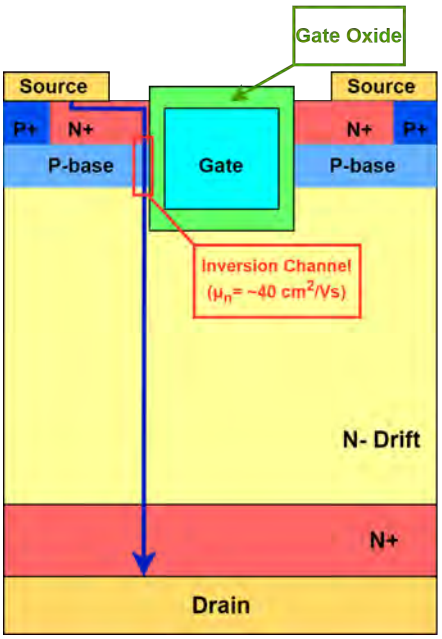


Fig. 1.9 Cross section of a Trench MOSFET device, with the current path shown indicated by a blue arrow.

whilst a negative shift could increase leakage current in the off-state or even cause device failure [81]. Furthermore, increased D_{it} can degrade channel mobility significantly. To protect the SiC MOSFET gate, most devices are limited to a maximum operating temperature of 150°C.

The weakness of the gate oxide of SiC MOSFETs also causes issues for application spaces where radiation effects are present i.e. aerospace or space. When exposed to irradiation effects i.e. gamma rays, heavy ions or protons, additional charged traps can be generated at the gate interface increasing leakage current and reducing breakdown voltage [82]. Critically, single event burnout of devices caused by heavy ions or neutrons can occur when the MOSFET is operating at just half of its rated voltage [83]. Effectively, this results in significant de-rating of SiC MOSFETs (i.e. using a higher voltage part for a given application) to ensure no burnouts occur.

Various annealing processes have been attempted to improve the quality of the gate interface, such as annealing with nitric oxide (NO) [84–86], nitrogen [87] and phosphorous oxychloride ($POCl_3$) [88]. Attempts to improve the inversion channel mobility by optimisation of gate trench processing have also been reported [89, 90]. Currently, channel mobility is expected to be roughly $40 cm^2/Vs$ in commercial devices. Alternative "high-κ", dielectrics which have elevated ε_s also have potential to replace thermally grown oxides in the future [91].

Integration of SBDs has been demonstrated to handle reverse recovery current [92, 93]. Monolithic integration of temperature sensors has also been achieved, using a lateral SBD [94] and also a lateral P-type resistor [95].

SiC JFETs

SiC JFETs are exclusively sold by UnitedSiC, now Qorvo. As SiC JFETs are inherently normally-on devices like HEMTs, Qorvo also offer SiC JFETs in a cascode configuration, marketed as "SiC FETs" [96]. Attempts have been made to fabricate normally-off JFETs [97–99], however normally-off JFETs are not commercially available. The typical structure of a SiC JFET is shown in figure 1.10.

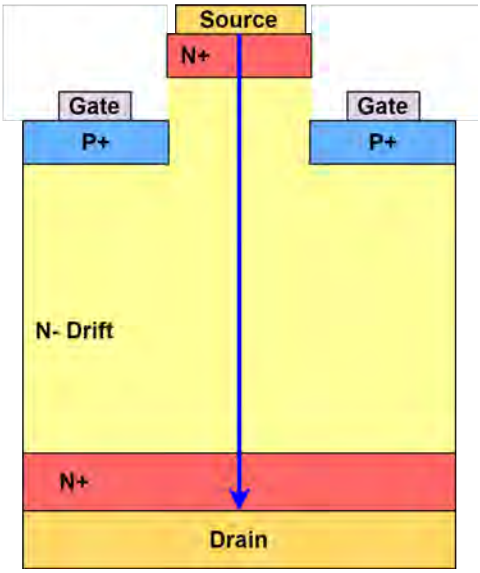


Fig. 1.10 Cross section of a JFET device, with the current path shown indicated by a blue arrow.

Unlike MOSFETs, the JFET structure does not require a gate oxide. Thus, SiC JFETs are incredibly well suited to extreme environment, high reliability applications as they do not feature the defective SiC/SiO_2 interface. SiC JFETs have been demonstrated to have no V_{th} shift up to 175°C [100], and only a -0.8V shift at 600°C [101]. SiC JFET based ICs have been shown to operate at 981°C, and survive 60 days in a Venus-like atmosphere by NASA [102, 103]. Additionally, 4H-SiC JFETs have been shown to be able to withstand both gamma ray and proton irradiation [104], although high radiation doses have been demonstrated to gradually shift V_{th} [105].

At low temperature, the conductivity of SiC layers (and thus $R_{on,sp}$) is primarily defined by electron mobility. However, at temperatures below 200K a large percentage of N and

P-type dopants are not ionized, an effect known as *carrier freeze-out*. In particular, the freeze-out of N-type dopants at 200K result in more resistive SiC N-type layers. In the case of JFETs, this also causes the JFET channel to narrow due to increased depletion of the gate junction, influencing V_{th}. This was verified by Cheng et al. who reported that the minimum measured $R_{on,sp}$ for an experimental 4H-SiC JFET over a temperature range of 30-473K was at 190K, and that a JFET with V_{th}= -1V at 300K had a V_{th} of 3.6V at 30K [106].

As the JFET gate configuration is a reverse biased PN junction, the gate leakage is expected to be very small (<10nA). Therefore, at low frequencies where resistive effects dominate, JFET input impedance will be of the order of MΩ - GΩ. Comparatively, MOSFETs will have higher input impedance due to the gate oxide, which will reduce gate leakage current further.

Furthermore, power JFETs are primarily vertical devices, and thus do not encounter the same issues when scaling for breakdown voltage as HEMTs. Vertical SiC JFETs have been demonstrated with breakdown voltages of 9kV [107] and 11kV [27]. Super-junction JFETs have been demonstrated by Wang et al. [100, 108], although the reported $R_{on,sp}$ did not break the 4H-SiC unipolar limit. Integration of a SBD to reduce reverse recovery losses has also been proposed [109].

Where fabrication is concerned, JFETs can be considered simpler to manufacture than MOSFETs as they don't require additional processing steps needed to create the gate oxide interface in a MOSFET. Simultaneous formation of gate regions and edge termination structures by ion implantation for 4H-SiC JFETs has also been demonstrated by Veliadis et al. [110], which can further reduce the complexity of fabricating 4H-SiC JFETs.

1.3 Overview of Surge Protection Technology

To protect valuable equipment or electronic systems from voltages and currents which are outside of their safe operating area, surge protection must be used. Surge voltages and currents are commonly generated by faults, lightning strikes or short circuits.

Their are two primary methods to implement surge protection: blocking the surge, or diverting (shunting) the surge [111]. Different components, semiconductor or otherwise each have their own benefits and drawbacks, and as such are suited to protecting from different types of surges. This section discusses some of the commercial circuit products that are available to purchase today.

Gas Discharge Tubes (GDT) are tubes filled with gas, that conduct during high voltage transients. When the voltage is high enough, the gas contained in the tube ionizes, which essentially creates a short. When this happens, the surge current is diverted through the GDT

to ground, removing the high surge voltage from the protected circuitry [112]. GDTs can handle very large currents but are slower to react, with typical response time of a GDT being 1-5μs.

Another option to protect from surge voltages are Transient Voltage Suppressor (TVS) diodes. These semiconductor devices are silicon Zener diodes, which are designed to fail via Zener breakdown rather than avalanche breakdown. When the reverse bias voltage reaches the breakdown voltage of the diode (typically less than 6V), the voltage is clamped at this value regardless of the current conducted by the diode [113]. This protects the circuit from over voltage events. As a semiconductor solution, the response time of a TVS diode is to the order of nanoseconds (1×10^{-9}s). However, TVS diodes are limited to low clamping voltages, and do not protect against current surges.

Another option to limit voltage surges are Metal Oxide Varistors (MOV). These are made from zinc oxide alongside other metals. During operation, a MOV has non-linear behaviour, with incredibly high resistance at normal voltage levels. When voltage spikes during a surge, the MOV resistance drops causing the excess current to pass through the MOV rather than the other circuit components. As voltage drops back to normal levels, the MOV resistance increases again. Typically, a GDT is connected in series to a MOV to prevent thermal runaway of the MOV during prolonged surge events [114]. The industry standard response time for MOVs is in single μs. MOVs handle larger amounts of energy than TVS diodes, but are less precise and degrade after repeated surges.

Mechanical circuit breakers protect circuitry by physically breaking the connection, preventing the surge from entering the circuit. The circuit breaker contact moves to close or open (make or break) the circuit. Mechanical circuit breakers can protect from over-current or short-circuit events. To sense over-current events, a thermal element i.e. a bimetallic strip is used. When large current is conducted through the strip, it heats up and expands which in turn trips the circuit breaker, opening the circuit. Alternatively, a solenoid can be used to trip the circuit breaker magnetically when a large current flows through the breaker [115]. Mechanical circuit breakers are robust and well understood components but are relatively slow compared to solid state solutions, with a millisecond response time.

Circuit breakers can be configured in a "normally-on" or "normally-off" state. A normally-on breaker allows current to flow unless a surge is detected causing the breaker to trip. Conversely, a normally-off breaker does not allow current to flow unless manually switched on. Most circuit breakers are normally-on such as ones found in residential homes. The benefit of normally-on breakers is that it does not require user interaction before the circuit may be used. However, normally-off breakers enable the circuit to only conduct current

intentionally, which is useful in the case of emergency systems i.e. backup lighting when mains power is lost.

Solid-state circuit breakers (SSCB) replaces the moving parts found in a mechanical breaker with semiconductor devices. Using semiconductor devices results in SSCBs have response time in the nanosecond to microsecond scale compared to milliseconds for mechanical breakers [116]. Furthermore, they are more robust - enduring many more surge events than mechanical breakers. However, the resistance of SSCBs is typically much higher than mechanical breakers, especially as the voltage rating increases. This is due to semiconductor device becoming more resistive as a consequence of blocking higher voltage. A key benefit of using SiC devices instead of silicon devices for the SSCB is their significantly lower resistance even at higher voltage ratings, which removes this problem.

It is common practice to use a combination of protection technologies to provide a circuit with multi-layer protection. An example of a SSCB circuit architecture is shown in figure 1.11. The figure shows that a MOV (or a TVS diode) is also included to assist with absorbing inductive energy from load inductance when the current surge occurs [116]. RC snubbers (R_{snub} and C_{snub}) are also included. Most importantly, the transistors are arranged in a *cascode* configuration. This is the optimal way to utilise a low resistance normally-on device, but drive it using a standard gate driver. The cascode configuration is explained in the next section.

1.4 Introduction to Cascodes

Although SiC JFETs are appealing because they lack a gate oxide interface, thereby avoiding the associated reliability issues of SiC MOSFETs, their normally-on behaviour makes them less desirable to system designers due to safety concerns. To address this, Baliga [117] proposed using a high-voltage SiC JFET in conjunction with a low-voltage silicon MOSFET, combining the superior on-state performance of the SiC JFET with the normally-off behaviour of the silicon MOSFET. Another key benefit of the cascode JFET is that the silicon MOSFET has an excellent gate oxide interface, providing designers with a familiar, reliable gate from which to drive the device.

This configuration is known as the "cascode" or "Baliga-pair" configuration. Although this was initially designed with the use of SiC JFETs in mind, it has also been demonstrated using normally-on GaN HEMTs [118]. The configuration of the cascode is shown in figure 1.12.

As figure 1.12 shows, the source electrode of the SiC JFET is connected to the drain of the silicon MOSFET, and the JFET gate is connected to the source of the MOSFET. The gate

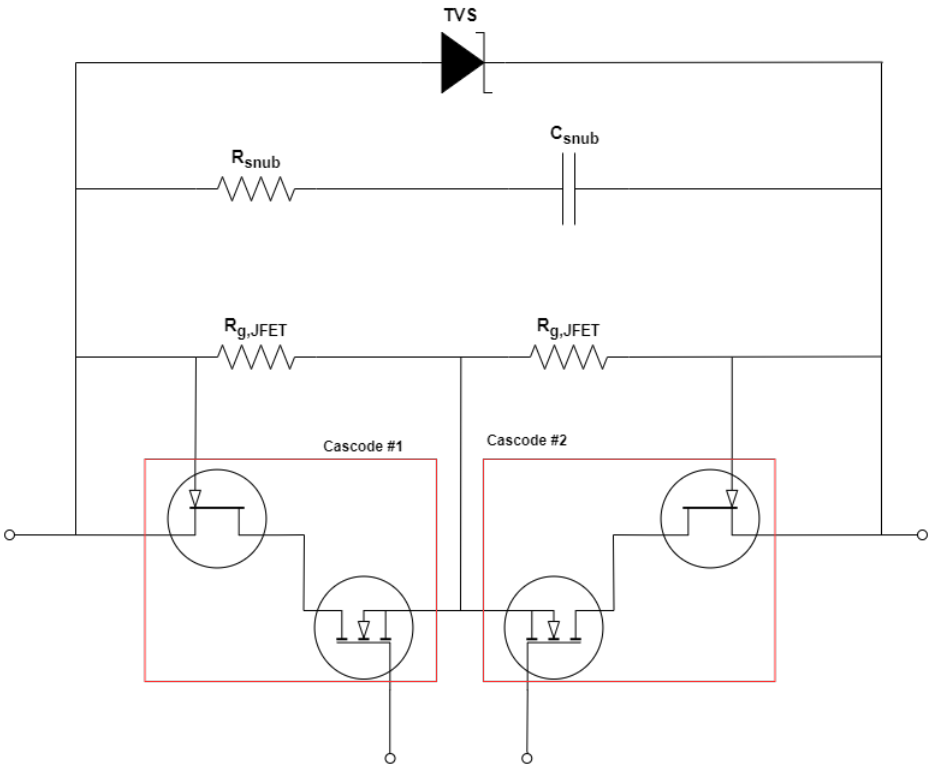


Fig. 1.11 Example circuit architecture of a Solid-state Circuit Breaker.

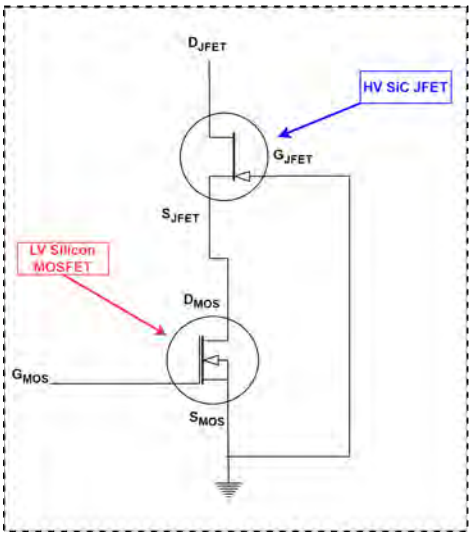


Fig. 1.12 The cascode circuit configuration of a SiC JFET and a low voltage silicon MOSFET.

of the silicon MOSFET is independently connected, while the drain of the JFET is connected to the load. A visualisation of how the cascode operates in the on and off-state is shown in figure 1.13a and 1.13b.

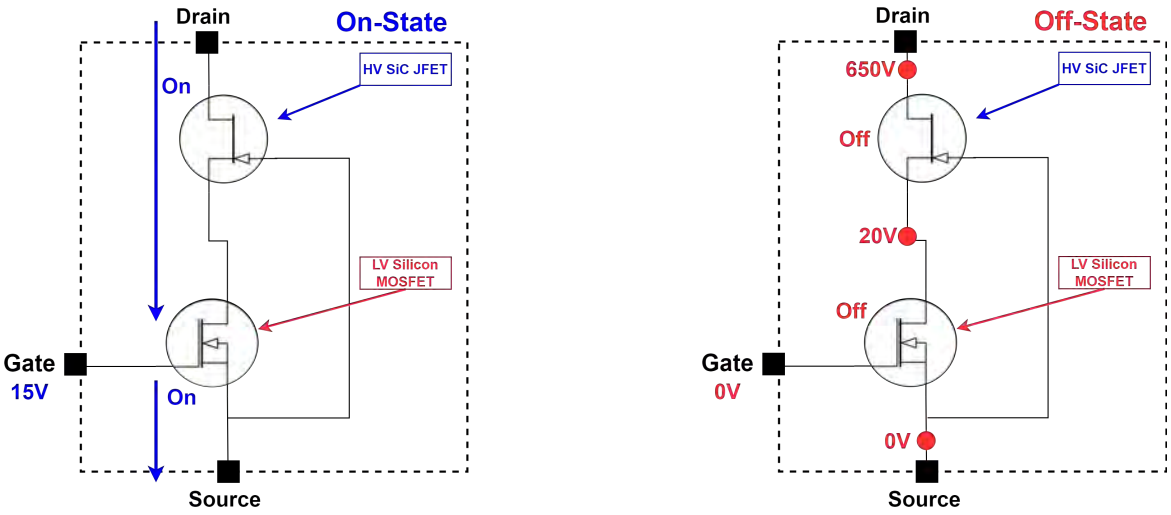


Fig. 1.13 A 650V Cascode in the (a) on-state, with current flow indicated by blue arrows, and (b) off-state, with potential at different points in the circuit indicated in red.

In the off-state, the gate of the silicon MOSFET is grounded. As the JFET gate is connected to the silicon MOSFET source, the JFET gate voltage ($V_{gs,JFET}$) is equal to the negative of the silicon MOSFET drain ($V_{ds,MOSFET}$). For example, in figure 1.13b as $V_{ds,MOSFET}$= 20V, $V_{gs,JFET}$= -20V. This reverse biases the JFET gate junction, depleting the channel region and turning the JFET off.

Once the JFET is turned off, it supports any further voltage above its V_{th}, keeping the voltage supported by the silicon MOSFET to low values. The key criteria which must be met is that the silicon MOSFET must have a breakdown voltage (BV) at least equal to SiC JFET threshold voltage (i.e. $BV_{MOSFET} \geq |V_{th,JFET}|$).

When in the on-state, the silicon MOSFET gate is biased to a standard positive gate voltage such as 15V. The silicon MOSFET turns on, which means that there is negligible positive bias at the MOSFET drain, and thus at the JFET gate. Therefore, as the JFET gate electrode is near 0V, the JFET is also turned on. The total on-state resistance (R_{on}) of the cascode is a sum of the JFET on-state resistance ($R_{on,JFET}$) and MOSFET on-state resistance ($R_{on,MOSFET}$).

Commercial cascode JFETs by Qorvo are a competitive alternative to other power devices, including SiC MOSFETs. Currently the best in-class 120A, 1200V cascode JFET has a R_{on} of 9mΩ [119], compared to 20mΩ for 151A MOSFET by Onsemi [120]. For comparison, a silicon depletion-mode MOSFET such as the one currently used in the TBU manufactured by IXYS which is rated to 1kV, 10A has a R_{on} of 1.5Ω [121]. As the high voltage depletion-mode device in a cascode is in the on-state 99% of the time, it is imperative to reduce the

R_{on} of this device. The key benefit of replacing a silicon MOSFET with an equivalent SiC JFET is the significantly lower R_{on} of the SiC device, which in turn will reduce the overall R_{on} of the cascode.

It has been also found that by Gonzalez et al. that when switching SiC FETs under an inductive load using a double-pulse switching test, SiC FETs had the lowest total switching energy out of all devices tested, including SiC MOSFETs, Si SJ MOSFETs and silicon Insulated Gate Bipolar Transistors (IGBTs) [122]. This indicates that the switching performance of SiC FETs is excellent, even when compared to stand-alone devices. Cascode SiC JFETs have been shown to have great potential in Electric Vehicle power trains [123] and solid-state circuit breakers [124].

1.5 Motivation

As discussed, 4H-SiC JFETs are currently commercially available and are very competitive with other device types when utilised in a cascode configurations. It is the intention of this work to assess current 4H-SiC JFET technology, and develop an optimized JFET design which meets tailored requirements for the TBU. Further process development work will be carried out to assist Bourns' with developing JFET prototypes which can be used build prototype TBUs using said JFETs.

By implementing the JFET designed in this thesis into the TBU, it is expected that a considerable improvement in R_{on} can be achieved. This will make the TBU more attractive to current Bourns' customers, and likely will result in more design-wins. Additionally, higher voltage markets could be penetrated because of the impressively low R_{on} of SiC devices at high voltages, which isn't feasible with the current silicon device used.

Solid state circuit breakers such as the TBU have different voltage and current requirements compared to power devices to be used in converters, such as off the shelf SiC JFETs from Qorvo, which have a minimum current rating of 32A, and a typical V_{th} of -11.5V [125]. The TBU requires a low current of 3A, with a low V_{th} of -3V, Thus, the JFET designed in thesis will keep these requirements in mind.

1.6 Thesis Overview

Chapter 2 explains the operational principles of JFETs and GaN HEMTs, presenting analytical models of the various contributions to the specific on-state resistance ($R_{on,sp}$) for each device. Using these $R_{on,sp}$ models, a comparative analysis is conducted between SiC JFETs and GaN HEMTs to justify replacing the silicon MOSFET currently used in the TBU

with a SiC JFET. Finally, the chapter also describes all the physics-based models employed in finite element Technology Computer-Aided Design (TCAD) simulations discussed in the subsequent chapters.

Chapter 3 presents the optimisation of the JFET cell and termination design using Synopsys TCAD simulations. The relationships between various design parameters and device performance including JFET R_{on}, V_{th} and BV are discussed. Special attention is given to undesirable breakdown mechanism caused by Short Channel Effects (SCEs), which is investigated in detail. Additionally, an optimized termination design is demonstrated to ensure the JFET achieves the rated BV of the drift region. The chapter concludes by presenting an optimised JFET design which eliminates this unwanted breakdown mechanism and without compromising other key performance indicators.

In **Chapter 4**, a novel JFET design which monolithically integrates a temperature sensor with a JFET is demonstrated using Synopsys TCAD, building upon the work in Chapter 3. A first principles model is utilized to accurately replicate the sensor's behaviour in simulations. The different design parameters for the sensor are discussed to minimize cross-talk between the active JFET and the sensor. Furthermore, electrothermal and transient simulations are carried out to examine the sensor's temperature response and its performance under self-heating, and dynamic conditions.

Chapter 5 investigates how material defects in 4H-SiC epitaxial layers can adversely affect the performance of unipolar devices such as JFETs and SBDs fabricated on the locations of these defects. This study involved the fabrication of Nickel (Ni) SBDs across two 150mm 4H-SiC wafers which had been mapped for material defects, and the locations of said defects recorded. A semi-automated probe station was used to characterize the wafers, and Python code was developed to automate data analysis and generate heat maps to illustrate the variation in diode characteristics across the wafers.

The process development of carbon caps, activation anneals for implanted aluminium dopants and subsequent Ohmic contacts are both presented in **Chapter 6**. All of these fabrication steps are essential to the overall JFET fabrication process, particularly for the JFET gate. To optimize the Specific Contact Resistance (SCR) of the Ohmic contact, various contact anneal temperatures and metal stacks were evaluated using Transfer Length Method (TLM) measurements. Furthermore, Hall and TLM measurements were utilized to determine the optimal activation anneal temperature in relation to the percentage of activated dopants.

Finally, **Chapter 7** presents the conclusions of this thesis, alongside suggestions of future work to build upon this Thesis.

Chapter 2

Analytical Modelling and Physical Models

2.1 Preface

In this chapter, a comparison of normally-on SiC JFETs and GaN HEMTs is completed using analytical models of $R_{on,sp}$. This is carried out to assess at which device is theoretically optimal for different voltage ratings. Furthermore, the premise of introducing a Carrier Storage Layer into the JFET structure to improve $R_{on,sp}$ is evaluated.

The second section of the chapter discusses physical models used in for Drift-Diffusion TCAD simulations which are subsequentially presented in chapter 3 and 4 of this thesis.

2.2 Analytical Modelling

To effectively compare the two competing WBG devices which could be used to replace the silicon depletion mode MOSFET in the TBU, specific on-resistance models can be used. These models take into account all resistance sources within the device, and can show realistic performance limits of the devices at different voltage ranges. These models are markedly different to the Baliga figure of merit (BFOM) discussed in chapter 1. The BFOM only takes into account the performance limit of the material, while these models consider the whole device.

2.2.1 JFET Resistance Model

$$R_{on,sp}(JFET) = R_{cs,sp} + R_{N+,sp} + R_{JFET,sp} + R_{drift,sp} + R_{sub,sp} + R_{cd,sp} \tag{2.1}$$

The calculation of total specific on-state resistance $R_{on,sp}$ is given by equation 2.1. It should be noted that specific resistances i.e. resistances as a function of device area are used

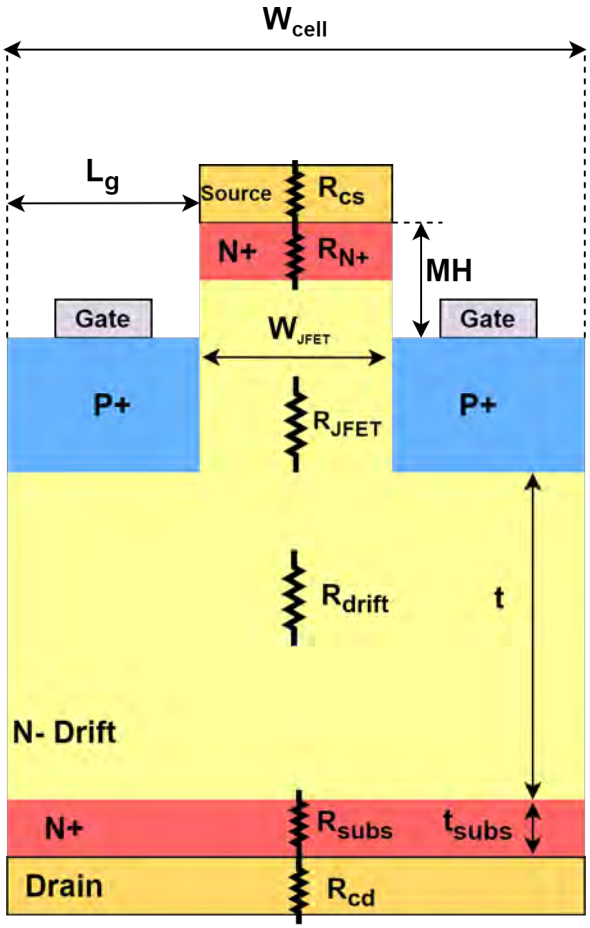


Fig. 2.1 A cross section of a JFET unit cell showing all resistance sources and relevant dimensions.

throughout this chapter. The equations for each resistance source is given by Baliga [9]. JFET region resistance is denoted as $R_{JFET,sp}$, and drift resistance as $R_{drift,sp}$. Source contact, drain contact and substrate resistance are denoted as $R_{cs,sp}$, $R_{cd,sp}$ and $R_{sub,sp}$, respectively. Finally, the N+ source resistance is denoted as $R_{N+,sp}$. Figure 2.1 shows the JFET structure with all sources of resistance and dimensions marked.

$$R_{cs,sp} = \frac{\rho_c W_{cell}}{W_{cs}} \tag{2.2}$$

Equation 2.2 is used to calculate $R_{cs,sp}$, where W_{cell} is the cell pitch, W_{cs} is the source contact width, and ρ_c is the specific contact resistance.

Where W_{cell} is equal to:

$$W_{cell} = 2L_g + W_{JFET} \tag{2.3}$$

Where L_g is the mesa spacing, and W_{JFET} is the JFET region width.

$$R_{N+,sp} = \frac{\rho_{N+} x_{N+} W_{cell}}{W_{JFET}} \tag{2.4}$$

Secondly, equation 2.4 may be used to calculate $R_{N+,sp}$ where ρ_{N+} and x_{N+} are the resistivity and thickness of the N+ region, respectively.

$$R_{JFET,sp} = \frac{\rho_{JFET} x_{JFET} W_{cell}}{a} \tag{2.5}$$

Equation 2.5 can be used to calculate R_{JFET}, where ρ_{JFET} and x_{JFET} are the resistivity and length of the region, respectively. The effective width of the JFET region is denoted by a which is expressed as:

$$a = W_{JFET} - 2W_0 \tag{2.6}$$

The zero bias depletion width (W_0), is computed by using the doping concentrations in the P-type gate (N_a) and the N-type doping in the JFET region N_d:

$$W_0 = \sqrt{\frac{2\varepsilon_s N_a V_{bi}}{qN_d(N_a + N_d)}} \tag{2.7}$$

Where V_{bi} is the built-in potential of the junction, which is related to the doping concentrations on both the P and N side of the junction:

$$V_{bi} = \frac{kT}{q} \log\left(\frac{N_a N_d}{n_i^2}\right) \tag{2.8}$$

$$R_{drift,sp} = \frac{\rho_d W_{cell}}{2} \ln\left(\frac{W_{cell}}{a}\right) + \rho_d (t + 0.5a - 0.5W_{cell}) \tag{2.9}$$

Equation 2.9 is used to calculate the drift region resistance $R_{drift,sp}$, where t and ρ_d are the drift region thickness and resistivity, respectively. It is assumed that current spreads at a 45°angle, and overlaps with the current flow from adjacent unit cells.

$$R_{sub,sp} = \rho_{sub} t_{sub} \tag{2.10}$$

Substrate resistance $R_{sub,sp}$ is calculated using equation 2.10, where ρ_{sub} is the resistivity of the substrate, and t_{sub} is the substrate thickness.

$$R_{cd,sp} = \rho_c \tag{2.11}$$

Finally, drain contact resistance $R_{cd,sp}$ is defined as the specific contact resistance ρ_c.

The values used for all associated parameters in equations 2.2 - 2.11 are shown in table 2.1.

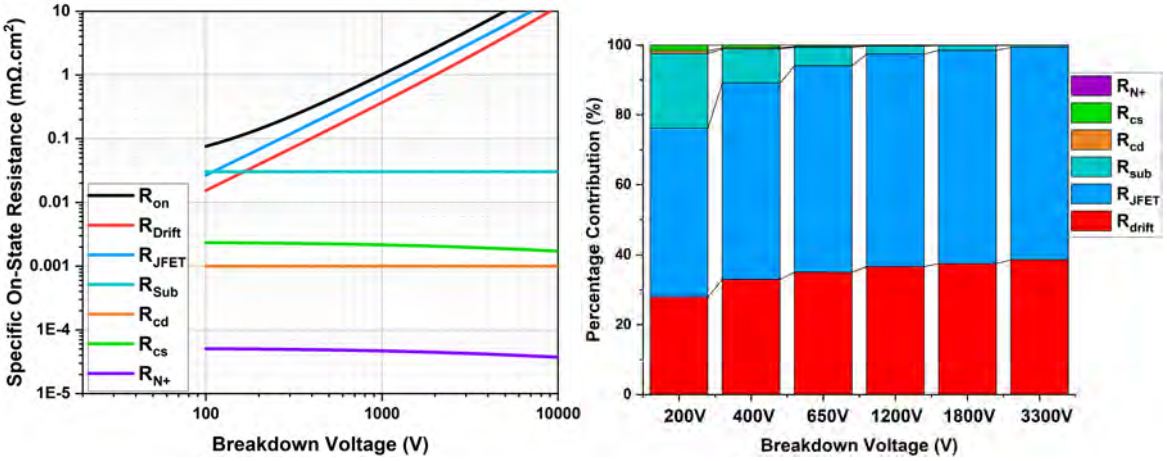
Table 2.1 Dimensions and doping concentrations used for JFET $R_{on,sp}$ model.

Symbol	Value	Unit
W_{cell}	5	μm
a	2	μm
x_{JFET}	3	μm
x_{N+}	0.25	μm
t_{sub}	350	μm
N_a	1×10^{19}	cm^{-3}
N_d	1×10^{16}	cm^{-3}
N_{sub}	1×10^{19}	cm^{-3}
ρ_c	1×10^{-6}	Ωcm^2

By using the N_d and W_{pp} values calculated using equations 2.12 and 2.13 in combination with the above $R_{on,sp}$ model enables the resistance to be plotted as a function of breakdown voltage for a SiC JFET.

$$BV_{pp}(4H-SiC) = 1.7 \times 10^{15} N_d^{-0.75} \tag{2.12}$$

$$W_{pp}(4H-SiC) = 1.37 \times 10^{11} N_D^{-0.875} \tag{2.13}$$



(a) (b)

Fig. 2.2 (a) All sources of resistance plotted as a function of BV (b) Percentage contributions of each resistance at selected BV values.

The contribution of all individual resistance terms for BV_{pp} values between 100-10kV are plotted in figure 2.2a, while figure 2.2b displays the percentage contribution of each resistance at a selection of relevant voltages.

As substrate and drain contact resistance do not vary with N_d or W_{JFET}, they remain constant at 0.03mΩcm^2 and 0.001mΩcm^2,respectively. As breakdown voltage increases, N_d reduces. Therefore, as N_d is inversely proportional to ρ_d, both drift and JFET resistance increase with voltage. At 200V, substrate resistance is still significant, making up 21.5% of $R_{on,sp}$. Comparatively, $R_{drift,sp}$ and $R_{JFET,sp}$ are 0.039mΩcm^2 and 0.067mΩcm^2 making up 48.1% and 30% of $R_{on,sp}$, respectively.

As voltage increases further, $R_{drift,sp}$ and $R_{JFET,sp}$ become progressively more dominant, where at 1800V drift resistance is 0.856mΩcm^2 and JFET resistance is 1.39mΩcm^2. Together, they make up 93.5% of the total device resistance.

As a is kept constant in this model, W_{JFET} must increase as doping in the JFET region reduces. As the source region ($R_{N+,sp}$) and source contact resistance ($R_{cs,sp}$) both depend on W_{JFET}, both of these experience minor reductions in resistance.

Figure 2.3 compares the theoretical performance limit of the JFET as calculated by the above analytical model to the unipolar limit for 4H-SiC which was shown in figure 1.6. As expected, the JFET model has a higher resistance than the unipolar limit, and begins to diverge away from the limit at higher voltages.

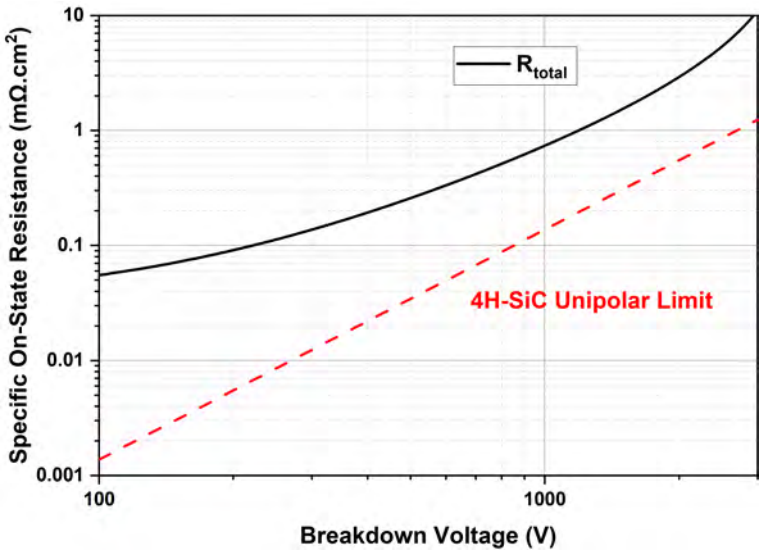


Fig. 2.3 A comparison of JFET $R_{on,sp}$ as calculated by the analytical model to the 4H-SiC unipolar limit.

JFET Threshold Voltage

The required effective JFET width a is dependant on the zero bias depletion width W_0 and JFET region width W_{JFET}. Normally-on devices such as JFETs and HEMTs control their conductive channels via depletion regions, hence the name "depletion mode". In the case of the JFET, negative bias is applied to the gate which reverse biases the PN junction, extending the depletion region into the channel. The threshold voltage (V_{th}) of a JFET is defined as the gate voltage (V_g) require to cause the adjacent gate depletion regions to merge in the centre of the channel, switching the device off. The width of the depletion region as a function of V_g can be calculated using equation (2.14):

$$W_{depl} = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_{gs})}{qN_d}} \tag{2.14}$$

By applying the threshold voltage condition $a = 2W_{depl}$ to equation (2.14), threshold voltage is:

$$V_{th} = V_{bi} - \frac{qN_D a^2}{8\varepsilon_s} \tag{2.15}$$

Therefore, V_{th} can be controlled by two design parameters - W_{JFET} and N_d. By combining the equation (2.12) and equation (2.15), threshold voltage as a function of breakdown voltage is be plotted in figure 2.4.

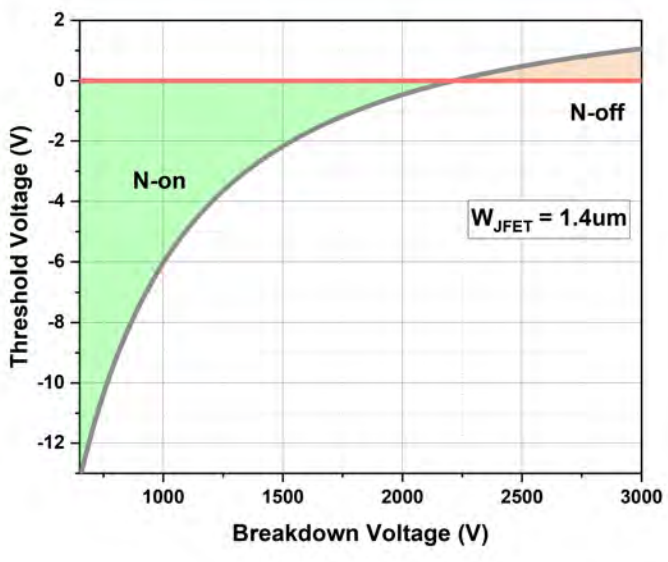


Fig. 2.4 Threshold voltage plotted as a function of BV_{pp} for a constant W_{JFET} of 1.4μm.

Figure 2.4 shows V_{th} as a function of breakdown voltage for W_{JFET}= 1.4μm. It can be seen that as doping concentration reduces to block higher voltage, V_{th} approaches 0V. At 650V, N_d= $3.6 \times 10^{16} cm^{-3}$ which corresponds to a V_{th} of -13.2V. At 3000V, N_d= $4.7 \times 10^{16} cm^{-3}$ resulting in a threshold voltage of +1.06V. When W_{JFET}= 1.4μm, using a drift region designed for over 2213V results in the JFET becoming normally-off.

To target the -3V threshold voltage required by the TBU, effective JFET width a must be kept constant and therefore W_{JFET} varies. This is the approach taken in the JFET model displayed in figures 2.2a and 2.2b.

Figure 2.5 shows the required W_{JFET} to achieve V_{th}= -3V when targeting different breakdown voltages between 650-3000V. As the figure shows, W_{JFET} can be made increasingly large as N_d is reduced. At 650V, W_{JFET} is only 0.86μm, while a 2.38μm width can be used at 3000V. As cell pitch increases, so does total cell pitch, as shown by equation 2.3.

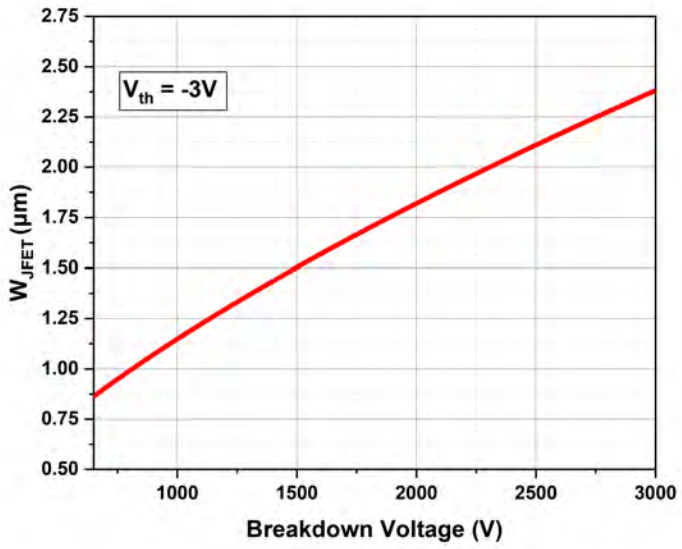


Fig. 2.5 JFET region width required for V_{th}= -3V for BV_{pp}= 650 - 3000V.

2.2.2 A Carrier Storage Layer

Larger W_{JFET} values and consequently larger cell pitches are undesirable because they decrease the cell density of the entire device. This necessitates larger die areas to conduct a given current. Commercially, larger die areas are unfavourable since they reduce the number of dies per wafer, thereby lowering profit margins. Furthermore, larger devices are more likely to contain a killer material defect, rendering the device inoperable.

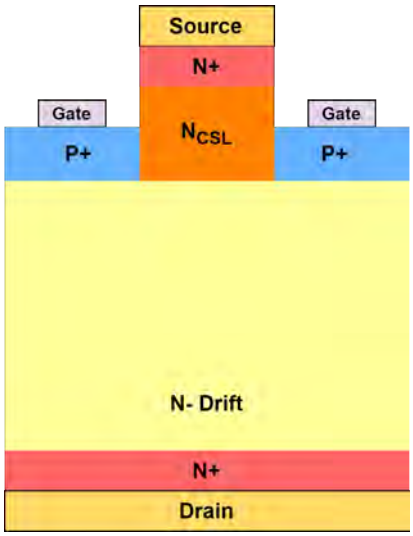


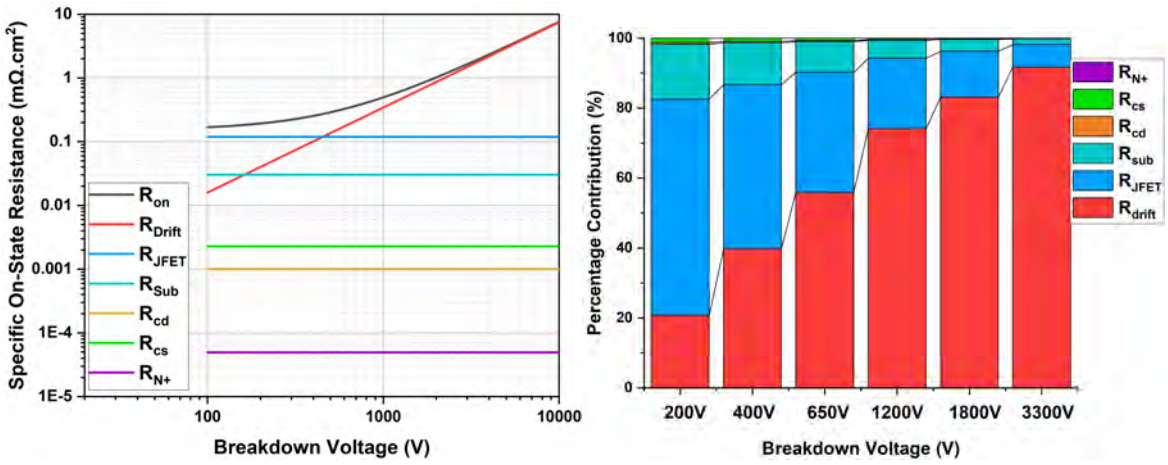
Fig. 2.6 Cross section of a JFET unit cell, with a carrier storage layer introduced in the JFET Mesa region.

To minimise W_{cell}, JFET width must also be minimised. To remove the relationship between W_{JFET} and V_{th}, a *Carrier Storage Layer* (CSL) can be used. In this design, the JFET region is doped independently to the drift region. This CSL is typically highly doped, which enables W_{JFET} to be small for a given V_{th}, and also reduces ρ_{JFET} significantly. Qorvo have stated that they use a CSL design in early generations of their JFET products [126]. Figure 2.6 shows a cross section of a CSL JFET, where the doping concentration in the CSL is denoted as N_{CSL}.

Utilising the same resistance model described for the standard JFET, but using a carrier storage layer doping (N_{CSL}) of $10^{17}cm^{-3}$ to calculate ρ_{JFET} results in figure 2.7a. All other parameters are kept equivalent to the standard JFET model, as shown in table 2.1.

Unlike the standard JFET $R_{JFET,sp}$ remains constant over the whole voltage range at $0.12\text{m}\Omega cm^2$, as shown by figure 2.7a. Drift resistance still rises at the same rate as in the standard JFET model, and thus the percentage contribution of $R_{drift,sp}$ increases significantly from 20.7% at 200V to 83.1% at 1800V. The total resistance of the CSL JFET is evidentially lower than the standard JFET because $R_{JFET,sp}$ does not increase - at 1800V $R_{on,sp}$(standard) = $2.28\text{m}\Omega cm^2$ and $R_{on,sp}$(CSL) = $0.9\text{m}\Omega cm^2$. Furthermore, cell pitch and W_{JFET} remain constant, enabling higher cell densities.

To create a CSL layer in practice requires either a more complicated epitaxy structure, or high energy N-type implantation, both of which may add considerable cost to the total fabrication process. Furthermore, using high doping concentrations in the JFET region will require very small W_{JFET} values to achieve the target threshold voltage of -3V. To achieve



(a) (b)

Fig. 2.7 (a) All sources of resistance plotted as a function of BV for the CSL JFET (b) Percentage contributions of each resistance at selected BV values.

these small W_{JFET} regions, complex lithography equipment such as a stepper may have to be used.

2.2.3 HEMT Resistance Model

Resistances in HEMTs include the gate-source resistance (R_{gs}), gate resistance (R_g) and the gate-drain resistance (R_{gd}), alongside the contact resistances $R_{cd,sp}$ and $R_{cs,sp}$. Figure 2.8 shows a HEMT unit cell, with all resistances and relevant dimensions displayed. The total specific on-resistance of the HEMT ($R_{on,sp}$) is equal to the sum of all resistances, as shown in equation (2.16).

$$R_{on,sp(HEMT)} = R_{cs,sp} + R_{gs,sp} + R_{g,sp} + R_{gd,sp} + R_{cd,sp} \tag{2.16}$$

The source contact resistance is a function of the contact length (L_s), cell pitch (W_{cell}) and the specific contact resistance (ρ_c). The same equation is used to calculate drain contact resistance, but using the drain length L_d.

$$R_{cs,sp} = \frac{\rho_c W_{cell}}{L_s} \tag{2.17}$$

The resistance contributed by the area between the gate and source $R_{gs,sp}$ is a function of the 2DEG resistivity (ρ_{2DEG}), and the distance between contacts (L_{gs}):

$$R_{gs,sp} = \rho_{2DEG} L_{gs} W_{cell} \tag{2.18}$$

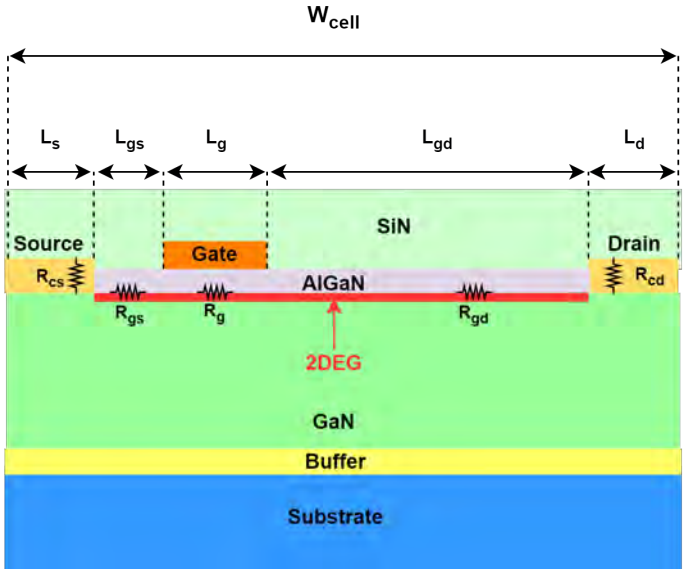


Fig. 2.8 A standard depletion-mode HEMT unit cell, with all sources of resistance identified.

The gate resistance $R_{g,sp}$ is governed by the gate length (L_g). Equation (2.19) is used to calculate R_g:

$$R_{g,sp} = \rho_{2DEG} L_g W_{cell} \tag{2.19}$$

The HEMT is a lateral device, and therefore supports voltage in the off-state laterally. This is unlike a JFET, which supports voltage vertically across its drift region. In the off-state, the drain contact has high bias applied, while the gate is held at a negative voltage. The source is grounded. Therefore, the voltage and thus the electric field is supported between the gate and drain electrodes in a HEMT.

As electric field E is equal to $-\frac{\partial V}{\partial x}$, where x is the horizontal distance, increasing the spacing between the two electrodes will increase the breakdown voltage. The source electrode is typically connected to the substrate in the third dimension to ground the substrate to create a reference point [5]. However as the critical electric field of GaN is above 3 MV/cm, it is unlikely that the HEMT will fail vertically through the GaN epitaxy rather than laterally.

To support increased voltage, the gate-drain spacing (L_{gd}) must increase. Figure 2.9 shows a typical electric field profile for a HEMT in the off-state. The average lateral electric field experienced by the HEMT is defined as $E_{av,lat}$. Mitigating electric field in the dielectric layers between the gate and drain is the primary motivation to use field plate structures.

To calculate the correct gate-drain spacing, equation 2.20 is used. The maximum average electric field strength between the two electrodes is typically given as 1MV/cm. In theory, this value could be considerably increased, because dielectrics such as SiO_2 have critical

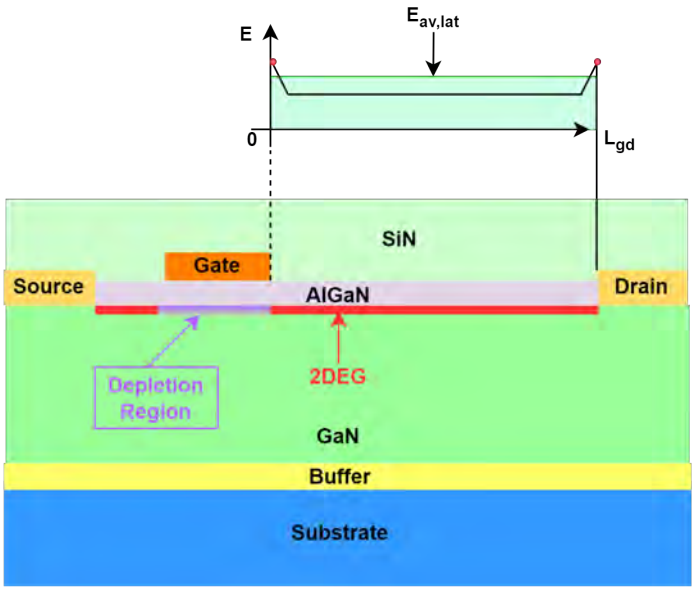


Fig. 2.9 HEMT in the off-state, showing an average electric field profile between the gate and drain electrodes.

field values near 10MV/cm. However, being subject to higher electric fields may lead to higher surface leakage. Furthermore, failure of dielectrics is a destructive failure mechanism i.e. the HEMT is destroyed if the dielectric fails. Therefore, reliability of the dielectric used is critical, and as such the electric field it is subjected to must be kept to a minimum. This is not the case in vertical devices containing PN junctions such as JFETs, which fail via avalanche breakdown, which is non-destructive and recoverable.

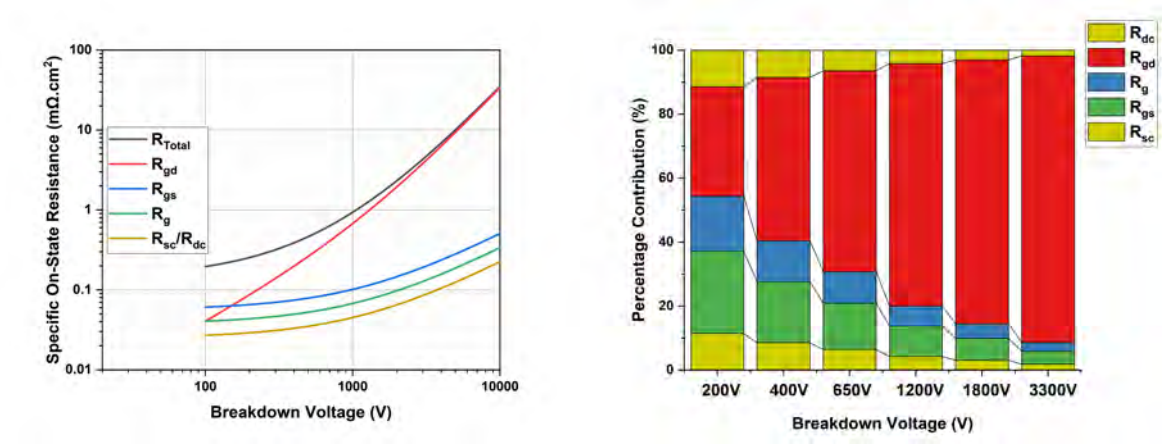
$$L_{gd} = \frac{BV}{E_{av,lat}} \tag{2.20}$$

The gate-drain resistance $R_{gd,sp}$ can be calculated using equation (2.21):

$$R_{gd,sp} = \rho_{2DEG} L_{gd} W_{cell} \tag{2.21}$$

Using the figures found in table 2.2, each of the resistance contributions for a GaN HEMT are calculated as a function of breakdown voltage between 100-10kV. This is shown in figure 2.10a, with percentage contributions of each resistance parameter at select voltages shown in figure 2.10b.

As figure 2.10a shows, at all voltages above 200V R_{gd} dominates - contributing 34.3% at 200V and 82.4% at 1800V. This is due to L_{gd} increasing linearly with breakdown voltage. As L_{gd} increases so does W_{cell}, which causes of all other resistances to increase.



(a) (b)

Fig. 2.10 (a) All sources of resistance plotted as a function of BV for a GaN HEMT (b) Percentage contributions of each resistance at selected BV values.

Table 2.2 Dimensions and doping concentrations used for HEMT $R_{on,sp}$ model.

Symbol	Value	Unit
L_s	5	μm
L_{gs}	1.5	μm
L_g	1	μm
L_d	5	μm
ρ_{2DEG}	300	Ω/sq
$E_{av,lat}$	1	MV/cm

Unlike JFETs, the threshold voltage of HEMTs is not geometrically dependant. Therefore V_{th} does not change with breakdown voltage for HEMTs.

2.2.4 Comparing SiC JFETs and GaN HEMTs

The total on-resistance of the standard JFET, the CSL JFET and GaN HEMT calculated by their respective models that have been detailed in the previous sections are compared in figure 2.11. To illustrate the significance of the $E_{av,lat}$ value used in the GaN HEMT model, total resistance for $E_{av,lat}$= 1MV/cm and 2MV/cm are both calculated.

Figure 2.11 shows that the standard JFET has a R_{on} over double that of the CSL design at 1000V. This improvement in resistance is also mirrored in HEMTs when doubling $E_{av,lat}$ to 2MV/cm.

When comparing the standard JFET and HEMT with $E_{av,lat}$= 1MV/cm, the HEMT performs slightly better at 650V, 1000V and 1800V, with R_{on} lower by 0.017mΩcm^2,

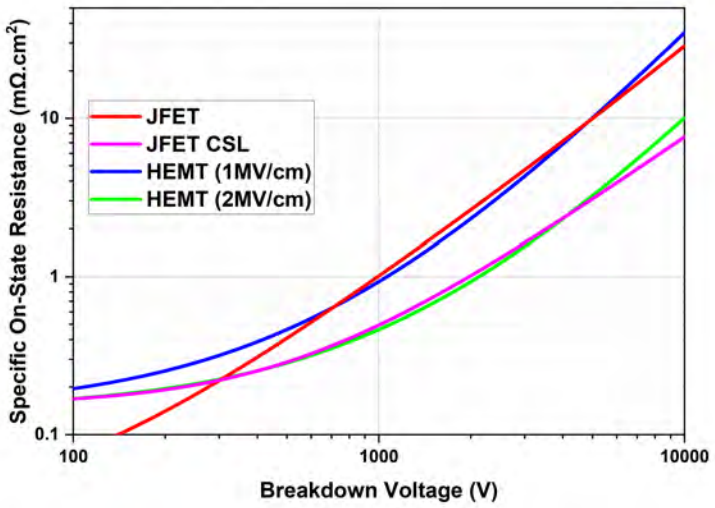


Fig. 2.11 Total specific on-resistance R_{on} plotted against breakdown voltage for the standard JFET, CSL JFET and HEMT models.

0.03mΩcm^2 and 0.28mΩcm^2, respectively. When comparing the CSL JFET and the HEMT with $E_{av,lat}$= 2MV/cm at the same voltages, the HEMT shows R_{on} reductions of 0.01mΩcm^2, 0.028mΩcm^2 and 0.075mΩcm^2.

Although the HEMT offers marginal performance improvement, the cell pitch of the device is also significant as discussed previously. Figure 2.12 shows the cell pitch of the different device models as they scale with breakdown voltage. The total cell pitch for the JFET models is equal to the sum of W_{JFET} and the width of all other features within the cell. It has been assumed that the sum of all the other widths is equal to 5.6μm, and remains constant. The JFET width varies with breakdown voltage, as already discussed.

As the HEMT must scale laterally with breakdown voltage, cell pitch increases rapidly. At 650V, the HEMT has W_{cell} of 19μm for $E_{av,lat}$=1MV/cm, and 15.75μm for $E_{av,lat}$=2MV/cm. At 1000V this increases to 22.5μm and 17.5μm, respectively, and at 1800V it further increases to 30.5μm and 21μm, respectively. This presents a significant issue for HEMTs at higher voltages, as die sizes must increase. Increased die size results in less die per wafer, increase cost per die and reducing profit margins. Furthermore, larger die are more likely to contain either a killer material or process defect, which will damage the wafer yield, further eroding profit margins.

Comparatively, as the JFET scales vertically with breakdown voltage, cell pitch does not change significantly. For the standard JFET, to keep V_{th} constant W_{JFET} rises, which results in cell pitch increasing from 10.2μm at 650V to 10.8μm at 1800V. As the CSL JFET has a

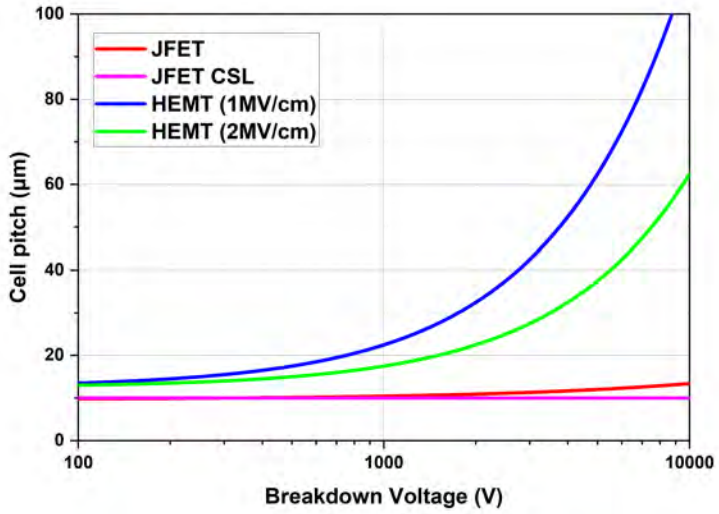


Fig. 2.12 Cell pitch plotted against breakdown voltage for the standard JFET, CSL JFET and HEMT models.

JFET region which is doped independently, this results in cell pitch remaining constant at 9.97μm for all voltages.

Overall, although GaN HEMTs do theoretically offer marginal resistance gains, the large cell pitch required at higher voltages is a significant downside. At the TBU target voltage rating of 800V, HEMT cell pitch for $E_{av,lat}$= 1MV/cm is roughly double that of the standard JFET. In practice, this means that HEMT devices to conduct the required 3A for the TBU may be almost double the size of the equivalent JFET device. Therefore, HEMTs are a more attractive choice for lower voltages, where the cell pitch is not excessively large, but are not suitable for the TBU.

Furthermore, the reliability issues associated with the failure mechanisms of HEMTs are unattractive for high reliability applications such as the TBU, where the primary application is protection of other circuitry. To ensure acceptable reliability, significant de-rating of HEMTs is likely required to reduce $E_{av,lat}$.

2.3 Physical Models used in Drift-Diffusion Simulations

2.3.1 The Anisotropic Nature of 4H-SiC

As a compound semiconductor, SiC consists covalently bonded Silicon (Si) and Carbon (C) atoms. The crystal structure of silicon and carbon atoms is formed of close-packed hexagonal

lattices. There are three possible that Si-C bilayers can form, denoted as A, B and C in figure 2.13.

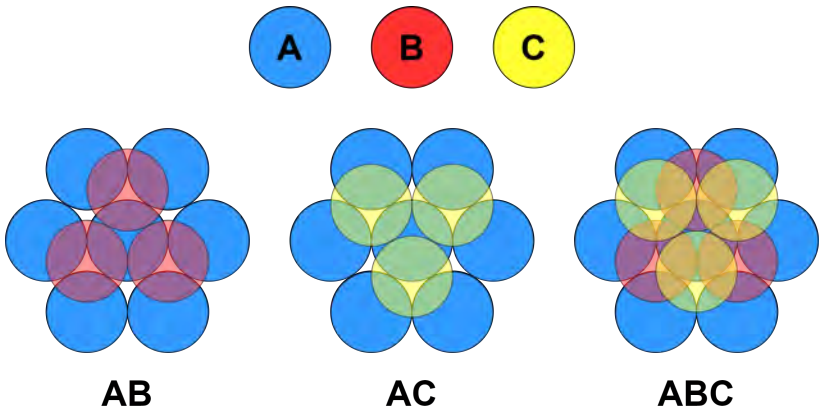


Fig. 2.13 The hexagonal packing arrangement in SiC consists of an initial SiC bilayer labelled as A, followed by subsequent bilayers that can occupy either the B or C positions.

Although all polytypes of SiC have an identical number of covalently bonded silicon and carbon atoms, each polytype has a different stacking sequence. In the case of the 4H polytype, this stacking sequence repeats every four layers (ABCB) , hence the "4" in 4H. This polytype is also possesses hexagonal sites, hence the "H". Hexagonal sites do not necessarily exist in every polytype, including 3C-SiC which just has cubic sites (hence the "C").

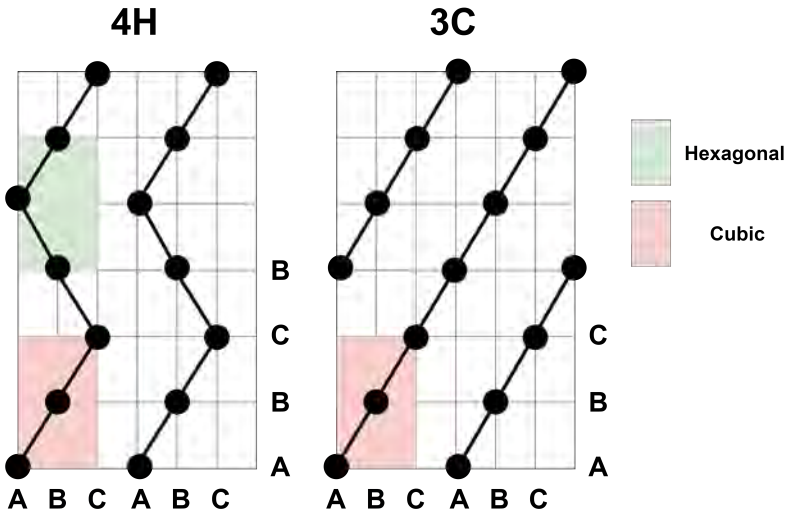


Fig. 2.14 The different stacking arrangements of the 4H and 3C polytypes of SiC.

In 4H-SiC, the split between cubic and hexagonal sites is exactly 50:50. This means that there is significant anisotropy in the lattice, and thus in the material characteristics in different planes of direction. For example, carrier mobility and thermal conductivity are different in

the [0001] plane parallel to the c-axis, compared to the [11$\bar{2}$0] plane perpendicular to the c-axis. Anisotropy is considered in many of the models described in this section.

2.3.2 Drift Diffusion and Current Continuity

Charge Conservation and Current Density

The local conservation of charge in a volume of a semiconductor can be expressed as for free electron concentration (n) and hole concentration (p):

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q} \bigtriangledown \cdot J_n \tag{2.22}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q} \bigtriangledown \cdot J_p \tag{2.23}$$

Where J_n and J_p represent the electron and hole current densities entering and exiting the region respectively, while G and R denote the net generation and recombination rates per unit time of the carriers within that region.

The electron or hole current density is a sum of the diffusion current density ($-D_i \bigtriangledown i$) and the drift current density ($i\mu_i E$), where i is the carrier type. Therefore, the current density for both electrons and holes can be expressed as:

$$\vec{J_n} = qn\mu_n E + D_n \bigtriangledown n \tag{2.24}$$

$$\vec{J_p} = qp\mu_p E - D_p \bigtriangledown p \tag{2.25}$$

Where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the diffusion constants for each carrier. These are defined by the Einstein relationships:

$$D_n = \frac{\mu_n kT}{q} \tag{2.26}$$

$$D_p = \frac{\mu_p kT}{q} \tag{2.27}$$

Electric field E is given by:

$$E = - \bigtriangledown \psi \tag{2.28}$$

Where ψ is the electrostatic potential. When the Einstein relation holds, equations (2.24) and (2.25) can be written as:

$$\vec{J_n} = -nq\mu_n \bigtriangledown \phi_n \tag{2.29}$$

$$\vec{J_p} = -nq\mu_p \bigtriangledown \phi_p \tag{2.30}$$

Where ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials, respectively.

Quasi-Fermi Potential

Quasi-Fermi potentials for electrons and holes can be found by rearranging the following equations:

$$n = N_c \exp\left(\frac{E_{f,n} - E_c}{kT}\right) \tag{2.31}$$

$$p = N_v \exp\left(\frac{E_v - E_{f,p}}{kT}\right) \tag{2.32}$$

Where:

$$E_{f,i} = -q\phi_i \tag{2.33}$$

Poisson Equation

The potential distribution, and therefore the electric field are related to the charge contained in the region by Poisson's equation, shown below in equation (2.34). This enables calculation of E based on the charge distribution in the device (assuming ε_s is constant).

$$\bigtriangledown \cdot E = \frac{q(p - n + N_d^+ - N_a^-)}{\varepsilon_s} \tag{2.34}$$

Where N_d^+ and N_a^- are the ionized donor and acceptor concentrations.

2.3.3 Carrier Recombination

Shockley-Read-Hall

The electron-hole recombination process through deep defect or trap levels within the forbidden gap is known as *Shockley-Read-Hall* (SRH) recombination. The SRH recombination rate is defined as:

$$R_{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{2.35}$$

Where τ_n and τ_p are the carrier lifetimes, while n_1 and p_1 can be expressed as:

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right) \tag{2.36}$$

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{kT}\right) \tag{2.37}$$

Where E_{trap} is the difference between the trap and intrinsic level. The effective intrinsic density ($n_{i,eff}$), including bandgap narrowing is expressed as:

$$n_{i,eff} = n_i \exp\left(\frac{E_{bgn}}{2kT}\right) \tag{2.38}$$

Where E_{bgn} is the narrowing effect of the bandgap energy. This effect is discussed in more detail further on in this section.

The doping dependence of carrier lifetimes (τ_{dop}) is modelled using the Scharfetter relationship:

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 - \left(\frac{N_{A,0}+N_{D,0}}{N_{ref}}\right)^{\gamma}} \tag{2.39}$$

The parameters used to calculate electron and hole lifetimes in equation (2.39) are shown in table 2.3 [127]:

Table 2.3 Model parameters for calculating carrier lifetimes.

Parameter	electrons	holes	unit
τ_{min}	0	0	s
τ_{max}	2.5×10^{-6}	0.5×10^{-6}	s
N_{ref}	3×10^{17}	3×10^{17}	cm^{-3}
γ	0.3	0.3	1

Auger Recombination

At high doping concentrations, band-to-band electron-hole recombination occurs across the forbidden gap in addition to SRH recombination. During Auger recombination an electron recombines with a hole, with the excess energy transferred to another free electron or hole

[128]. This process is described by the Auger model, shown in equation (2.40). The values used for C_n and C_p are $5 \times 10^{-31} s^{-1}$ and $2 \times 10^{-31} s^{-1}$, respectively [129].

$$R_A = (C_n n + C_p p)(np - n_{i,eff}^2) \tag{2.40}$$

Bandgap Narrowing

The bandgap energy is reduced as temperature is elevated, primarily because of two effects: thermal expansion of the semiconductor lattice, and the temperature dependence of electron-phonon interactions. This is captured by the Varshni equation [130].

Furthermore, high doping concentrations result in E_g reducing further - this additional reduction is known as *Bandgap Narrowing*. Equation 2.41 combines the Varshni equation with the bandgap narrowing effect, denoted as E_{bgn}.

$$E_{g,eff}(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} - E_{bgn} \tag{2.41}$$

Where $E_g(0)$ is the size of the bandgap at 0K, whilst α and β are material dependant parameters. The bandgap narrowing effect (E_{bgn}) is given by the Slotboom model [131], shown below in equation 2.42. For 4H-SiC, N_{ref}= $1 \times 10^{17} cm^{-3}$, while E_{ref}= 0.009eV for p-type and 0.002eV for n-type [132, 133]. The values used for equations (2.41) and (2.42) can be found in table 2.4. Due the minor disparity in E_{bgn} at low doping concentrations, the difference in E_g between n and p-type SiC remains negligible. However, at higher doping concentrations, p-type SiC experiences significantly more bandgap narrowing.

$$E_{bgn} = E_{ref}\left[\ln\left(\frac{N_{tot}}{N_{ref}}\right) + \sqrt{\ln\left(\frac{N_{tot}}{N_{ref}}\right)^2 + 0.5} \right] \tag{2.42}$$

Table 2.4 Parameters used to calculate bandgap energy as a function of temperature, and doping. *n-type **p-type

Parameter	electrons	unit
E_{ref}	0.002* 0.009**	eV
N_{ref}	1×10^{17}	cm^{-3}
α	0.033	eV/K
β	1×10^{-5}	K

2.3.4 Impact Ionization

The only significant carrier generation effect that must be modelled is impact ionization. Other carrier generation methods, such as optical generation are considered negligible.

At high electric field strengths, carriers can accelerate to very high energies between collision events. At such high kinetic energy, when a collision occurs it can generate electron-hole pairs, leading to a rapid increase in charge and resulting in device breakdown. This phenomenon is known as *avalanche generation* of carriers.

The generation rate due to impact ionization (G_{ii}) is expressed as:

$$G_{ii} = \frac{1}{q}(\alpha_n|\vec{J_n}| + \alpha_p|\vec{J_p}|) \tag{2.43}$$

where α_n and α_p are the impact ionization coefficients for electrons and holes. The Okuto-Crowell model is used to determine α [134], which is shown in equation 2.44. The parameters used by the simulator for this model can be found in [135] for [0001], and [136] for $[11\bar{2}0]$.

$$\alpha = a(1 + c(T - T_0))\exp\left(-\frac{b[1 + d(T - T_0)]}{E}\right) \tag{2.44}$$

Table 2.5 Parameters used in the Okuto-Crowell Impact Ionization Model.

	[0001]		$[11\bar{2}0]$		
Parameter	electrons	holes	electrons	holes	unit
a	2.1×10^7	2.96×10^7	1.76×10^8	3.41×10^8	V^{-1}
b	1.7×10^7	1.6×10^7	3.3×10^7	2.5×10^7	V/cm
c	0	7.511×10^{-3}	0	7.511×10^{-3}	K^{-1}
d	0	1.381×10^{-3}	0	1.381×10^{-3}	K^{-1}

2.3.5 Incomplete Ionization

Incomplete ionization is a mechanism by which a percentage of dopants are not ionized at a given temperature. Taking a n-type doped semiconductor as an example, at low temperatures there is insufficient thermal energy to release electrons bound to donor sites. As temperature and thermal energy contained in the lattice increases, these donor sites become "active", donating their electrons to the conduction band [137]. Eventually, at an elevated temperature all donor sites will be active. The energy required to ionize a dopant (E_{ion}) determines the number of dopants active at a given temperature.

This effect is more pronounced in SiC compared to silicon because dopants sit deeper in its large bandgap (E_{ion} is larger), particularly for acceptors. For typical donor doping concentrations in the drift region of SiC devices ($N_d = 1 \times 10^{16}\text{cm}^{-3}$), incomplete ionization of donors can be considered negligible at temperatures of 300K and above.

The number of active acceptors (N_a^-) and donors (N_d^-) at a given temperature is shown below.

$$N_a^- = \frac{N_a}{1 + g_a \exp\left(\frac{-E_{f,p} - E_v}{kT}\right)} \tag{2.45}$$

$$N_d^+ = \frac{N_a}{1 + g_d \exp\left(\frac{E_{f,n} - E_c}{kT}\right)} \tag{2.46}$$

Where g_a and g_d are shown below in equations (2.47) and (2.48). The constant values of 4 and 2 are the degeneracy of acceptors and donors, respectively.

$$g_a = 4 \exp\left(\frac{E_{ion} - E_v}{kT}\right) \tag{2.47}$$

$$g_d = 2 \exp\left(\frac{Ec - E_{ion}}{kT}\right) \tag{2.48}$$

At high doping concentrations, E_{ion} is reduced. The most common approach to this, which agrees with the Pearson-Bardeen model is based on average impurity separation distance ($N^{\frac{1}{3}}$). This model is shown below in equation 2.49, where $E_{ion,0}$ is ionization energy of an isolated impurity centre, ΔE_{ion} is reduced ionization energy and α is an empirical fitting parameter [138].

$$\Delta E_{ion} = E_{ion,0} - \alpha N^{\frac{1}{3}} \tag{2.49}$$

Common 4H-SiC donor species, such as nitrogen and phosphorous can occupy two different sites within the semiconductor lattice: cubic or hexagonal. Each of these types have their own E_{ion} and α values, which are shown below in table 2.6 [139, 140].

Aluminium (Al) and boron are the most common dopant species used to achieve P-type doping in 4H-SiC. Aluminium has a ionization energy of 265meV [141]. The level used for Boron has been reported between 285 - 310meV[142–144]. Therefore, an averaged value of 293meV is used.

Aluminium has a higher solubility limit than boron, and thus normally the preferred P-type species [145]. Table 2.7 shows the values for E_{ion} and α for both dopants.

Table 2.6 Ionization energies for common donor species in 4H-SiC.

Dopant	Nitrogen		Phosphorous	
Site	Cubic	Hexagonal	Cubic	Hexagonal
E_{ion} (meV)	70.9	123.7	102	55
α	3.38×10^{-8}	4.65×10^{-8}	5.79×10^{-6}	6.386×10^{-9}

Table 2.7 Ionization energies for common acceptor species in 4H-SiC.

Dopant	Aluminium	Boron
E_{ion} (meV)	265	293
α	3.6×10^{-8}	0

2.3.6 Carrier Mobility

Temperature and Doping Dependence

The Arora model is used to describe the dependence of carrier mobility on doping and temperature. This model specifically addresses mobility at low field strengths. This results in a decrease in mobility as temperature rises and as the net doping concentration increases. The Arora model is defined as:

$$\mu_{Arora} = \mu_{min}\left(\frac{T}{300}\right)^{\alpha_m} + \frac{\mu_d}{1 + \left(\frac{N_{dop}}{N_{ref}}\right)^{A^*}} \tag{2.50}$$

Where:

$$\mu_d = \mu_{max}\left(\frac{T}{300}\right)^{\alpha_d} \tag{2.51}$$

$$N_{ref} = A_N\left(\frac{T}{300}\right)^{\alpha_N} \tag{2.52}$$

$$A^* = A_a\left(\frac{T}{300}\right)^{\alpha_a} \tag{2.53}$$

$$N_{dop} = N_d + N_a \tag{2.54}$$

Furthermore, similar to impact ionization, the anisotropic nature of the 4H-SiC lattice leads to varying maximum mobility values (μ_{max}) along different crystal planes. Specifically, the mobility perpendicular to the c-axis ($[11\bar{2}0]$) is 83% and 87% of the electron and hole

mobility, respectively, compared to the mobility parallel to the c-axis ([0001]). Table 2.8 shows the parameters used in equations (2.50)-(2.54) for electrons and holes along the [0001] plane [146]. Both carrier types experience significant degradation in mobility as temperature increases, especially at low doping concentrations such as $10^{16}\ cm^{-3}$. As doping concentration increases, mobility is reduced at all temperatures.

Table 2.8 Arora model parameters for electrons and holes for the [0001] plane.

Parameter	Electrons	Holes	unit
μ_{min}	40	0	cm^2/Vs
α_m	-1.536	-0.57	1
μ_{max}	910	113.5	cm^2/Vs
α_d	-2.397	-2.6	1
A_N	2×10^{17}	2.4×10^{18}	cm^{-3}
α_n	0.75	2.9	1
A_a	0.76	0.69	1
α_a	0.722	-0.2	1

2.3.7 High Field Saturation

At high electric fields, the drift velocity of carriers saturates at a material specific value (v_{sat}). Thus carrier drift velocity is no longer proportional to electric field.

The Canali model, which originates from the Caughey-Thomas formula describes this effect. The model uses the low field mobility value calculated by the Arora model (μ_{Arora}) to find the high field mobility μ_{hfs}:

$$\mu_{hfs} = \frac{(\alpha+1)\mu_{Arora}}{\alpha+\left[1+\left(\frac{(\alpha+1)\mu_{Arora}E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{2.55}$$

The exponent β is a temperature dependant parameter:

$$\beta = \beta_0\left(\frac{T}{300}\right)^{\beta_{exp}} \tag{2.56}$$

Anisotropy has also been observed in v_{sat}, like in μ_{max}. However, in this case v_{sat} is 16% larger in along $[11\bar{2}0]$ at 2.2×10^7cm/s compared to 1.9×10^7cm/s for the [0001] plane. This value is the same for both electrons and holes.

Table 2.9 Canali model parameters used to model velocity saturation.

Parameter	Electrons	Holes	unit
β_0	1.2	1.2	1
β_{exp}	-1.536	-0.57	1
α	0	0	1

2.3.8 Thermodynamic Model

To model device self-heating, the temperature gradient ($P \bigtriangledown T$) must be included in equations (2.29) and (2.30), which use drift-diffusion ($-nq\mu_n(\bigtriangledown\phi_n)$) to calculate current density. This results in equations (2.57) and (2.58):

$$\vec{J_n} = -nq\mu_n(\bigtriangledown\phi_n + P_n \bigtriangledown T) \tag{2.57}$$

$$\vec{J_p} = -pq\mu_p(\bigtriangledown\phi_p + P_p \bigtriangledown T) \tag{2.58}$$

Where P_n and P_p are thermoelectric powers.

Thermal Conductivity

Heat is conducted by phonons in the semiconductor lattice. As temperature increases, the occurrence of phonon-phonon scattering events rises. This reduces the mean free path of phonons ($\imath$) between collisions, which in turn reduces the thermal conductivity (κ) according to the Debye equation, where C is lattice heat capacity, υ is average particle velocity [147]:

$$\kappa = \frac{C\upsilon\imath}{3} \tag{2.59}$$

In the simulator, the temperature dependence of κ is expressed as:

$$\kappa(T) = \frac{1}{a + bT + cT^2} \tag{2.60}$$

The corresponding values for constants a, b and c can be found in table 2.10 below for the [0001] plane. Due to anisotropy, $\kappa_{11\bar{2}0}$ has been found to be 70% of κ_{1100} [132].

Table 2.10 Model parameters for thermal conductivity.

a	b	c
2.5×10^{-3}	2.75×10^{-4}	1.3×10^{-6}

Calculating Lattice temperature

The lattice temperature is calculated using:

$$\begin{aligned} c\frac{\partial T}{\partial t} - \bigtriangledown \cdot (\kappa \bigtriangledown T) = - \bigtriangledown \Big[& (P_n T + \phi_n)\vec{J_n} + (P_p T + \phi_p)\vec{J_p} \\ & - \frac{1}{q}(E_c + 1.5kT)(\bigtriangledown \cdot \vec{J_n} - qR_{\text{net},n}) \\ & - \frac{1}{q}(E_v + 1.5kT)(- \bigtriangledown \cdot \vec{J_p} - qR_{\text{net},p}) \Big] \end{aligned} \tag{2.61}$$

Where $R_{net,n}$ and $R_{net,p}$ are the net recombination rates of electrons and holes, respectively.

2.4 Conclusion

To conclude, this chapter has presented both JFET and HEMT cell designs, and identified all sources of resistance within the cells. Furthermore, by calculating the magnitude of each resistance component, an analytical model was created for both devices. This model was employed to analyse how $R_{on,sp}$ scales with breakdown voltage, and enabled an effective comparison between the two devices at key voltage rating battlegrounds such as 650V and 1200V. Both devices had comparable $R_{on,sp}$ values across the voltage range tested.

It was found that by introducing a CSL into the JFET cell structure, $R_{on,sp}$ could be significantly improved, whilst removing the undesirable effect of V_{th} varying with BV. On the other hand, the cell pitch the HEMT was demonstrated to increase significantly as BV increased, making HEMTs unfeasible to manufacture at scale for high voltage ratings. Therefore, it is concluded that JFETs are better suited to high voltage applications, particularly above 650V.

Finally, all relevant physics models which are used to describe device behaviour in finite element simulations were presented, and discussed. These models will by employed in the next two chapters to achieve an optimized JFET design.

Chapter 3

Design and Simulation of 4H-SiC JFETs

3.1 Preface

This chapter investigates which design parameters such as mesa width, mesa height and gate junction depth influence the on and off-state behaviour of SiC JFETs using Synopsys TCAD. Optimisation of floating field ring edge termination structures is also completed. The body of work in this chapter has been published in the journal *Power Electronic Devices and Components*, under the title "*On Short Channel Effects in High Voltage JFETs: A Theoretical Analysis*" [148]. Additionally, further work on the same topic included in this chapter was also presented at ICSCRM 2022, which has subsequently been published in *Key Engineering Materials*, titled "*Impact of Dimensions and Doping on the Breakdown Voltage of a Trench 4H-SiC Vertical JFET*" [149].

3.2 Calibrating Simulations

The simulations completed using Synopsys TCAD must first be calibrated by comparing existing experimental data that has been reported in literature for 4H-SiC JFETs to a simulation of the same device. This is essential to ensure that the current-voltage characteristics calculated by the simulator are accurate and representative of real devices. To complete this, the results of Zhao et al. [28] were chosen to be replicated in TCAD. This structure utilises P-type doping on the sidewall of the mesa, as shown by Figure 3.1, which also shows most of the relevant dimensions of the JFET unit cell. Parameters not shown in figure 3.1 which are used for simulation can be found in table 3.1.

To achieve the P+ gate doping profile, kinetic Monte-Carlo implantation methodology has been used [150]. This methodology is based on the statistical Binary Collision Approximation

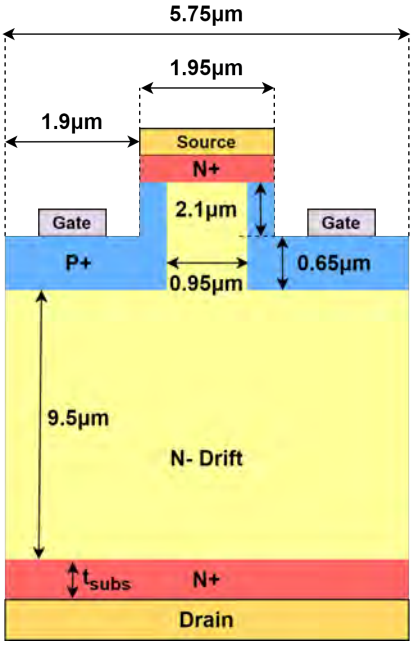


Fig. 3.1 The cross-section of the JFET unit cell reported by Zhao et al. to be replicated in Synopsys TCAD to calibrate simulations.

Table 3.1 Further parameters used to simulate the JFET unit cell reported by Zhao et al.

Symbol	Value	Unit
N_d	7×10^{15}	cm^{-3}
N_+	1×10^{19}	cm^{-3}
t_{subs}	350	μm

Table 3.2 Details of implantation scheme used to replicate the P+ gate doping profile of Zhao et al.

Implant number	Energy (keV)	Dose (cm^{-2})
1	25	3×10^{12}
2	100	1.2×10^{13}
3	260	3.3×10^{13}
4	360	3.3×10^{13}
5	460	3.3×10^{13}
6	560	3.3×10^{13}
7	600	3.3×10^{13}

[151]. The target aluminium concentration for the P+ region is $\geq 1\times10^{18} cm^{-3}$, with a depth

of 0.65μm. Table 3.2 shows the simulated implantation schedule used to achieve the doping profile. All implants were simulated with a 55° tilt angle.

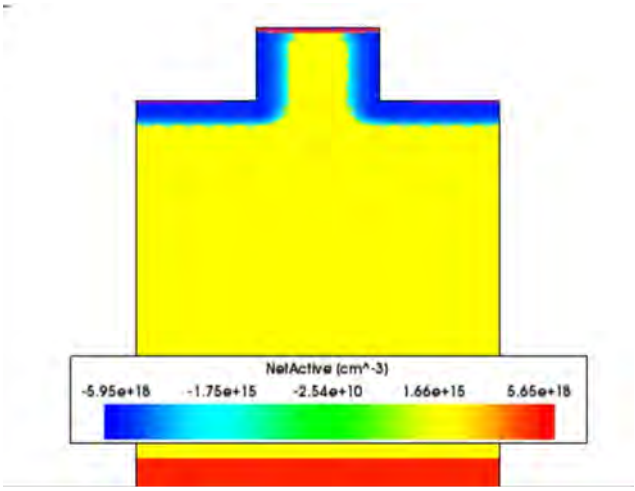
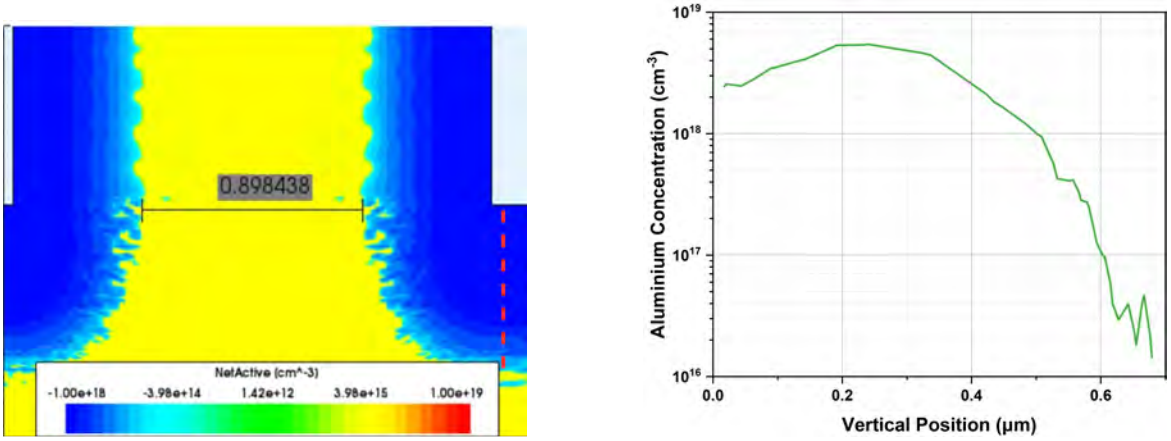


Fig. 3.2 The JFET unit cell of Zhao et al. recreated in TCAD, showing the net doping profile.

The resulting JFET unit cell doping profile is shown in figure 3.2. Figure 3.3a shows the channel region enlarged, with the position of a vertical cut-line shown. The JFET channel width is measured as 0.89μm, which is marginally smaller than the 0.95μm specified by Zhao. When inspecting the aluminium concentration along the cut-line, the doping concentrations peaks at $5.3 \times 10^{18} cm^{-3}$, and remains above $10^{18} cm^{-3}$ until 0.5μm. The doping concentration stays above $10^{17} cm^{-3}$ until a depth of 0.6μm.



(a) (b)

Fig. 3.3 (a) A zoomed in image channel region of the JFET show in figure 3.2 , showing the measured channel width of 0.89μm and the position of the vertical cut-line indicated by a red dashed line (b) The aluminium concentration plotted along the length of the cut-line.

To effectively compare the output characteristics, the simulated cell is scaled to have the same active area as the experimental device, which is $9.38 \times 10^{-4} cm^2$. Figure 3.4 shows the experimental and simulated output characteristics at V_g= 1.5V, 2V and 2.5V.

Good agreement is found between the simulated and experimental curves for all gate biases, although the simulated characteristics at V_g=1.5V and 2V are noticeably lower than the experimental data. This may be explained by the narrower JFET channel width in the simulated device. To achieve this agreement, the bulk electron mobility has been set as $1140 cm^2/Vs$. Threshold voltage is not reported by Zhao et al. and therefore cannot be compared to simulation.

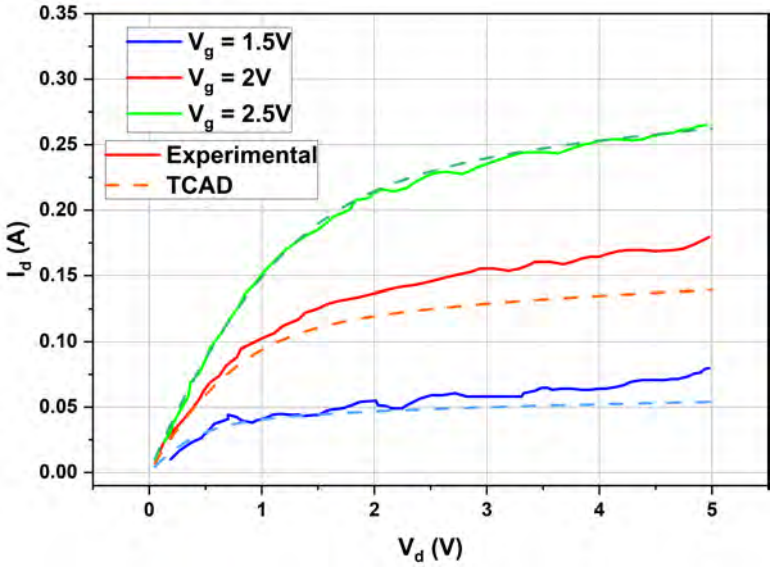


Fig. 3.4 Comparison of the experimental results of Zhao et al. and the simulated output characteristics using TCAD, at V_g= 1.5V, 2V and 2.5V. Bulk electron mobility has been set as 1140 cm^2/Vs.

3.3 Short Channel Effects in JFETs

This section investigates the on and off-state performance of SiC JFETs with different channel lengths and widths. Specifically, the relationship between channel length and width, and their impact on breakdown performance is evaluated.

The channel region of a transistor is arguably the area of most importance within the device. This behaviour of this region is how the current flow in the device is controlled, and how the device may be switched between the on and off-state. The length of the channel region is a highly important parameter in JFETs and MOSFETs. It has been observed that a

short channel region can lead to numerous negative effects, including reduction of threshold voltage [152]. This negative effect is known as *Short Channel Effects* (SCEs).

In MOSFETs, the channel length is broadly equal to the gate length. In CMOS found in ICs, the gate lengths are traditionally very short as the are logic devices, and thus are quite small. It has been observed that SCEs are prevalent in planar CMOS for gate lengths ≤90nm [153]. These effects have effectively limited further scalability of planar logic CMOS [154], with logic devices transitioning to FinFETs or in the near future GAAFETs to avoid SCEs at smaller gate lengths [155].

Short channel effects manifest in a variety of ways, including elevated drain leakage, reduction in V_{th} and Drain Induced Barrier Lowering (DIBL) [156, 157]. When a transistor is turned off, a potential barrier is formed in the channel which prevents current flow. When the channel length is small, source and drain fields penetrate into the centre of the channel, lowering the potential barrier [158]. When high off-state voltage is applied, the smaller potential barrier in the short channel can be collapse, which device switches on causing the device to fail. This is known as DIBL. Additionally, the lowered potential barrier causes in the V_{th} of the device to be sensitive to the drain bias applied. For instance, V_{th} will be significantly lower if V_d= 5V compared to V_d= 1V [157].

The effect of SCEs, including DIBL have been investigated in low voltage SiC JFETs for logic applications [159]. However, most literature for low voltage logic devices investigate how DIBL affects on-state performance. Very little work exists exploring how SCEs affect high voltage JFETs, especially concerning the effect of DIBL on breakdown voltage. Experimental works on high voltage SiC JFETs have theorised that DIBL contributed to premature breakdown with respect to the drift regions used [23, 100].

3.3.1 Device Structure

The device structure used for this work differs from structure used in the calibration work. The target rating for this device is 1200V, and it does not include sidewall implantation. Figure 3.5 shows the cross section of the unit cell used for this work. The two variables which are used for this work are the junction depth of the P+ gate region (x_j) and the JFET channel width, referred to as "MW" in figure 3.5. The value of the parameters which remain constant can be found in table 3.3.

In this work, the target P+ gate region doping concentration is $\geq 1 \times 10^{19} cm^{-3}$. Ideally, this profile should be a box profile. To achieve box profiles for P+ junction depths, an implant schedule comprising of multiple individual implants must be used.

Four different schedules have been designed using the Stopping Range of Ions in Matter (SRIM) software package [160]: schedule A (300nm), schedule B (500nm), schedule C

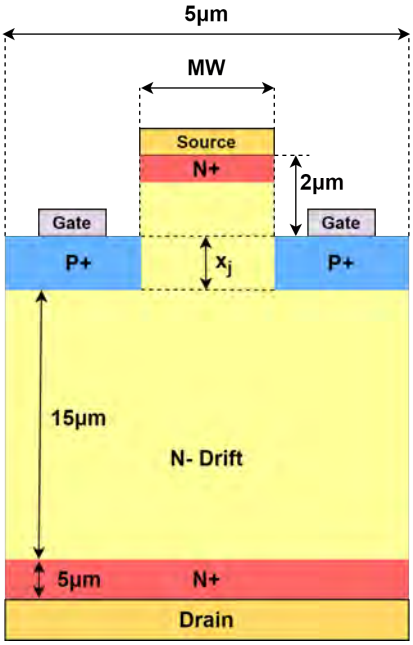


Fig. 3.5 The cross-section of the JFET unit cell used for TCAD simulation.

Table 3.3 JFET unit cell parameters used in TCAD simulation to investigate the relationship between channel dimensions and DIBL.

Parameter	Value	Units
Cell pitch	5	μm
Mesa Height	2	μm
Drift Region thickness	15	μm
N+ thickness	0.1	μm
Substrate thickness	5	μm
Drift region doping	1×10^{16}	cm^{-3}
N+ doping	1×10^{19}	cm^{-3}
Substrate doping	1×10^{19}	cm^{-3}

(700nm) and schedule D (1000nm). These implantation schemes were then implemented in Synopsys TCAD. The aluminium concentration of each schedule as calculated by SRIM is shown in figure 3.6.

The implantation beam dose and energy of each implant used in the different schedules is shown in table 3.4. It should be noted that the channelling effect may be used to achieve

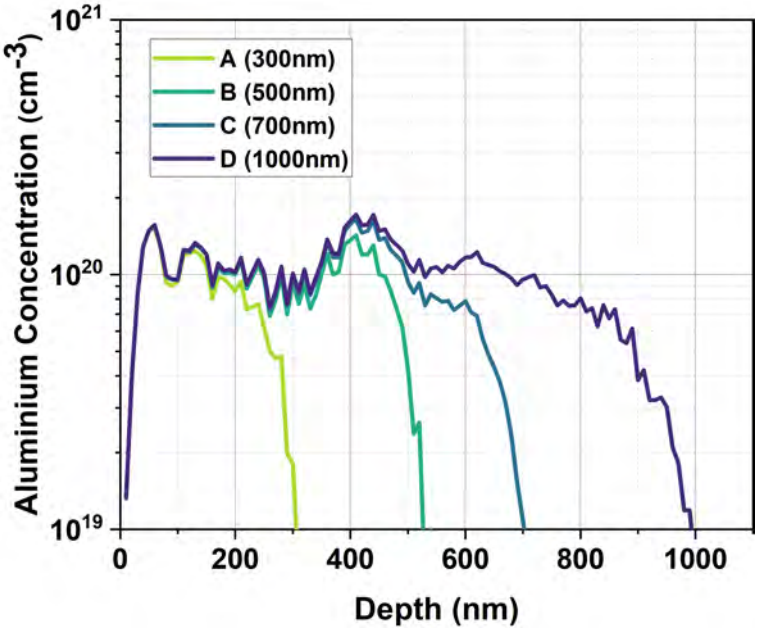


Fig. 3.6 Simulated SRIM depth profiles for each of the proposed implantation schedules shown in table 3.4.

equivalent implant depths with lower implantation energies [161]. Channelling implantation of aluminium ions has been successfully used to create deeper P+ junctions in SiC JBS diodes, improving blocking performance [162]. However, in this work a implant angle of 0° is used, which does not result in channelling.

Table 3.4 Implantation parameters used for each of the four different schedules: A,B,C and D. The unit of implant dose is cm^{-2}. Additional implantation events were required to achieve greater junction depths.

Implant	40 keV	100keV	180keV	350keV	520keV	680keV	880keV
A	6×10^{14}	9×10^{14}	1.1×10^{15}	-	-	-	-
B	6×10^{14}	9×10^{14}	1.1×10^{15}	2.5×10^{15}	-	-	-
C	6×10^{14}	9×10^{14}	1.1×10^{15}	2.5×10^{15}	1.7×10^{15}	-	-
D	6×10^{14}	9×10^{14}	1.1×10^{15}	2.5×10^{15}	1.7×10^{15}	1.4×10^{15}	1.4×10^{15}

The resulting unit cell structure after process simulation for design A (x_j = 300nm) using its respective implantation schedule is shown in figure 3.7 below.

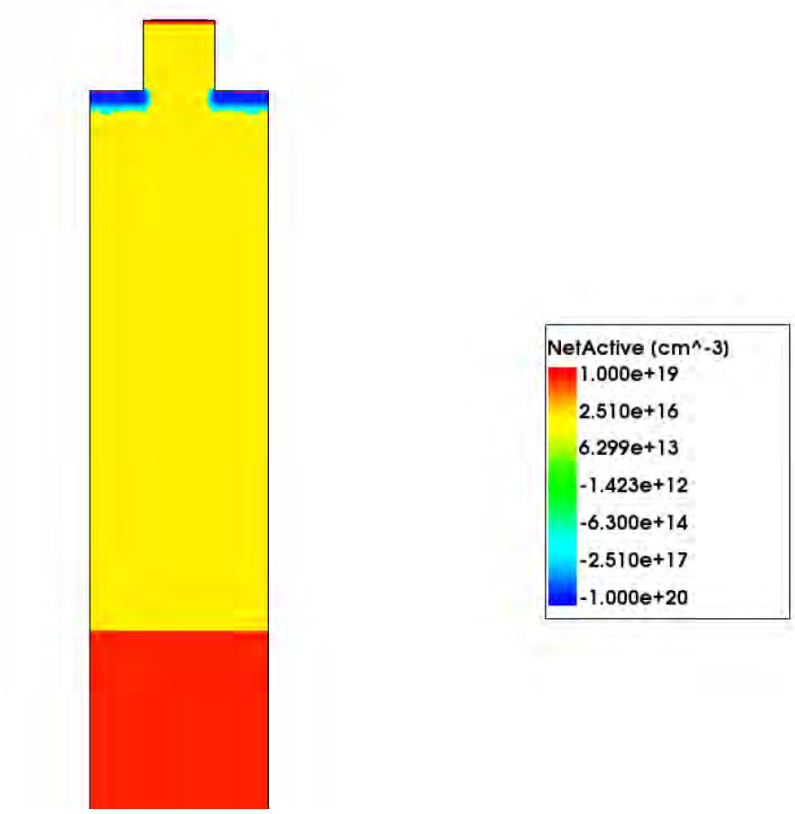


Fig. 3.7 Process simulated JFET unit cell with x_j= 300nm.

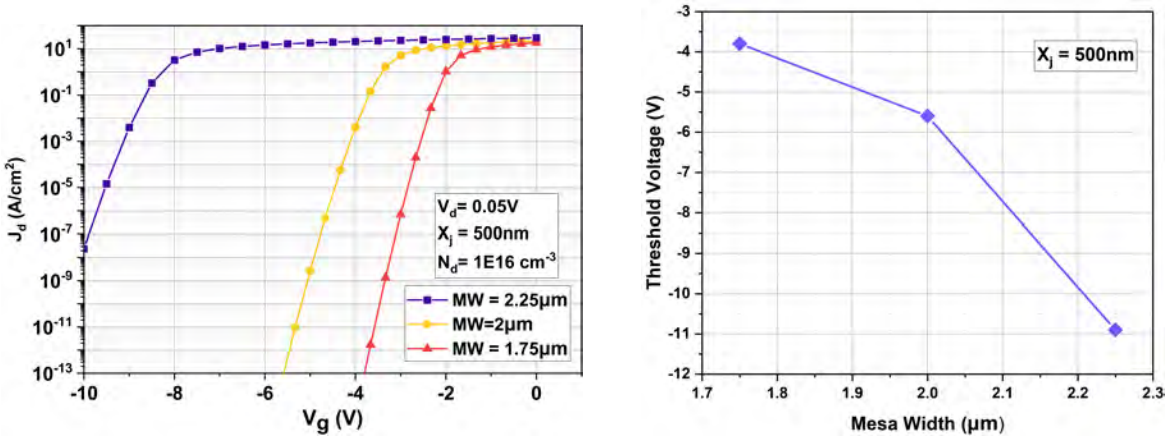
3.3.2 On-State Characterisation

Threshold Voltage

Firstly, a transfer characteristic (J_d - V_g) was calculated to assess if simulations agree with the relationship between V_{th} and MW which was discussed in chapter 2. The analytical relationship between V_{th} and JFET mesa width discussed in chapter two (equation 2.15) is repeated below in equation 3.1.

$$V_{th} = V_{bi} - \frac{qN_D(MW - 2W_0)^2}{8\varepsilon_s} \tag{3.1}$$

Drain current density (J_d) has been used instead of drain current. Threshold voltage was extracted at a current density of $10^{-13} A/cm^2$. For implantation schedule B where x_j= 500nm, MW was varied between 1.75 - 2.25μm. The drain voltage was set at 0.05V. Figure 3.8 illustrates that as MW increases, threshold voltage gets progressively more negative. Specifically, for a mesa width of 1.75μm, V_{th} is -3.8V; for mesa width of 2μm V_{th}= -5.6V and for MW= 2.25μm threshold voltage is -10.9V. This qualitatively agrees with the analytical relationship shown in equation 3.1.



(a) (b)

Fig. 3.8 (a) Transfer characteristics of design B (x_j= 500nm) with MW= 1.75μm, 2μm and 2.25μm (b) The corresponding V_{th} values extracted for each mesa width tested. As MW increases, the JFET becomes increasingly harder to switch off.

When calculating V_{th} for each of the different junction depths tested, MW was fixed at 2μm. Figure 3.9 plots the transfer characteristics of all four designs, at both low (V_d= 0.05V) and high (V_d= 2V) drain bias. The extracted threshold voltage values for designs A,B,C and D at V_d= 2V are determined as follows: -13.5V, -6.5V, -4.75V and -2.6V, respectively. In practice, to safely turn off the JFET, the applied V_g must be more negative than V_{th}.

A more negative V_{th} means that the gate driver must supply a more negative voltage, and have a broader operating range e.g. instead of 0 to -20V, the driver may have to be able to supply between 0 to -30V. This increases the gate driver complexity, and thus the cost. Furthermore, in the case of a surge event, a JFET with a more negative V_{th} may take longer to switch off than a JFET with a V_{th} closer to 0V as the gate voltage must transition from 0V (on-state) to a more negative V_g (off-state) to switch the JFET off.

It is noted that the sub-threshold slope becomes steeper at larger junction depths, which indicates better electrostatic control of the channel. This agrees with previous findings that there is a correlation between SCEs and the ratio of x_j to MW [159].

A smaller shift in threshold voltage (ΔV_{th}) as V_d increases from 0.05V to 2V is observed for deeper junctions. Specifically, design B (500nm) experiences a ΔV_{th} of -0.9V, while design D (1000nm) only experiences ΔV_{th} of -0.25V. To further elucidate the relationship between x_j and the severity of DIBL, the DIBL factor (γ) is defined as the change in V_{th} divided by the change in V_d, as shown in equation 3.2 below [159, 163]:

$$\gamma = -\frac{\Delta V_{th}}{\Delta V_d} \tag{3.2}$$

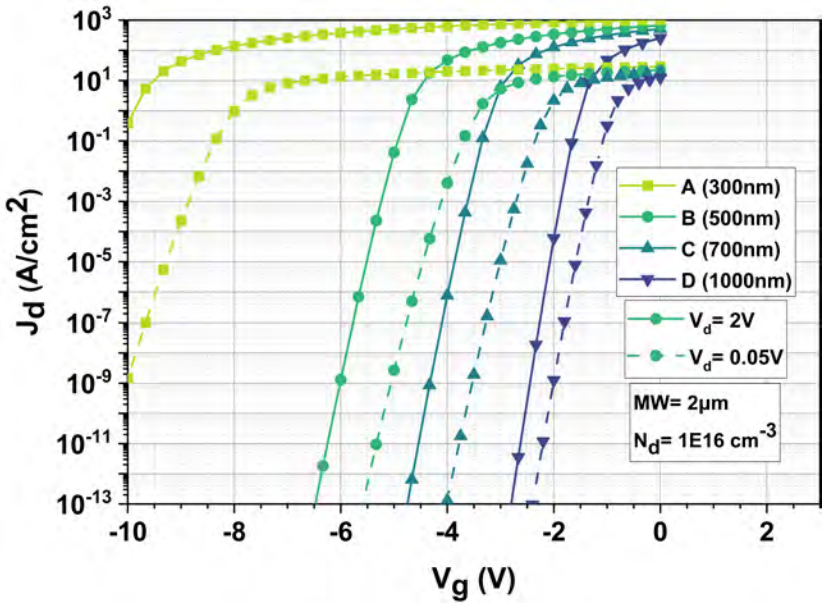


Fig. 3.9 Simulated transfer characteristics for all four designs at V_d=0.05V and V_d=2V. Larger channel lengths result in V_{th} trending towards 0V. Longer channel lengths are also less sensitive to applied V_d, indicating a reduced effect of DIBL.

Figure 3.10 subsequentially plots γ as a function of X_j. A larger value of γ indicates that the design in question has a ΔV_{th} , and thus has poorer electrostatic control of the channel region. As figure shows, γ= 1.33 for the shortest 300nm channel, whilst both the 500nm and 700nm have γ similar values of 0.38 and 0.36, respectively. Finally, the longest channel which is 1000nm long only exhibited a γ of 0.1, further verifying the importance of channel length. This trend qualitatively agrees with findings for logic SiC JFETs by Kaneko et al. [159], and in silicon CMOS [152].

The shift in V_{th} at larger junction depths can partially be attributed to lateral straggling of the implanted aluminium ions, which encroach into the channel region. Elevated numbers of implantation events coupled with high beam doses has been found to result in significant lateral straggling in SiC [164]. The doping profiles of design A and D are shown in figure 3.11a and 3.11b, with measured channel widths shown. Due to the afore mentioned lateral straggling, design D has an effective channel width of 890nm, compared to 1490nm for design A. This is an effective 60% reduction in channel width, which also causes V_{th} to shift towards 0V. It has been demonstrated that lateral straggling of P-type implants used in SiC planar MOSFETs can reduce the spacing between adjacent P-type regions, causing the channel to pinch off prematurely [165].

Therefore, the shift in V_{th} towards 0V at larger junction depths is due to a combination of channel width reducing, but also a reduction of DIBL. As the effect of lateral straggling

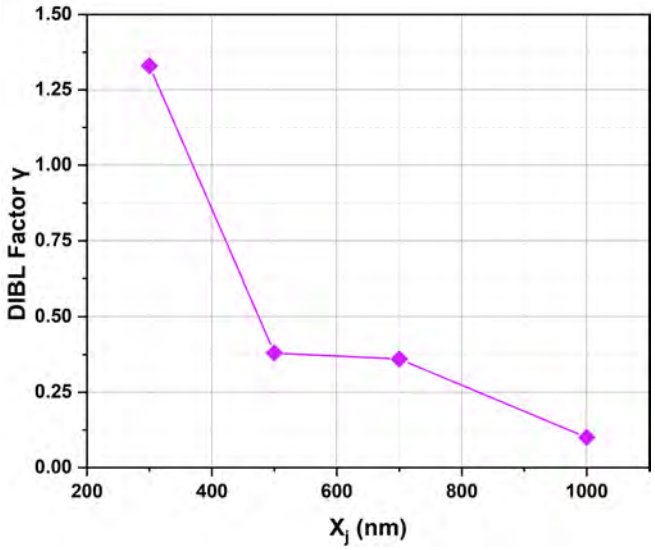
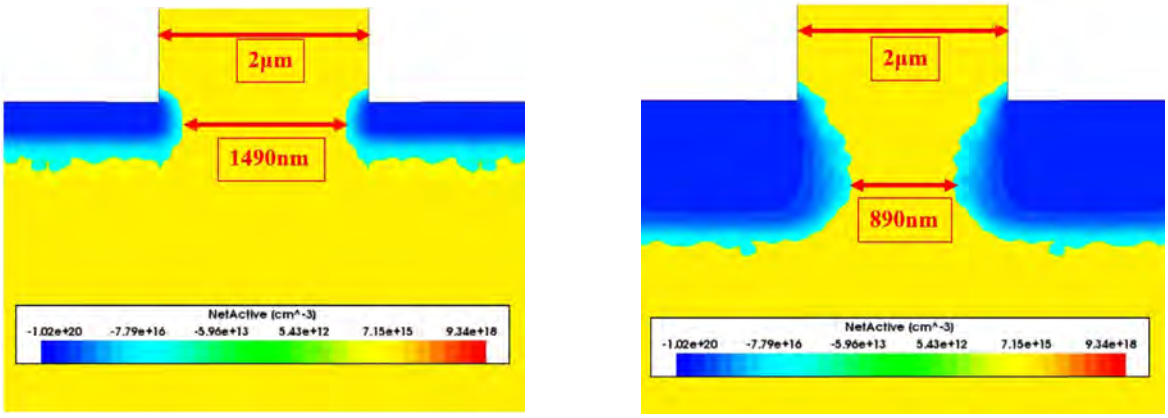


Fig. 3.10 Calculated DIBL factor γ plotted as a function of X_j. Increasing X_j significantly reduces γ towards 0.



(a) (b)

Fig. 3.11 Doping profile of the JFET channel region of (a) Design A (b) Design D.

increases with junction depth, it becomes challenging to distinguish the individual contributions of each effect to the shift of V_{th} towards 0V. The lateral double-gate JFETs reported by Kaneko et al. do not have to consider the straggling effect, as the channel is lateral rather than vertical. Nevertheless, this qualitatively agrees with the design rule proposed by Kaneko et al. that as the ratio $\frac{x_j}{MW}$ increases, mitigation of DIBL becomes more effective.

3.3.3 Isolating the Effect of Junction Depth

Although the results in the previous section demonstrated that a deeper junction makes the JFET easier to switch off, this observation is also influenced by lateral straggling of the gate implant during the process simulation. To isolate the impact of x_j from lateral straggling, an identical JFET unit cell was created using Synopsys Structure Editor, with the P-type gate region designed as a box. Unlike the implanted gate junction, this box profile eliminates lateral straggling, enabling an accurate assessment how x_j affects V_{th} and the level of DIBL. Figure 3.12 shows the half-unit cell structure designed in structure editor, with a 300nm gate junction.

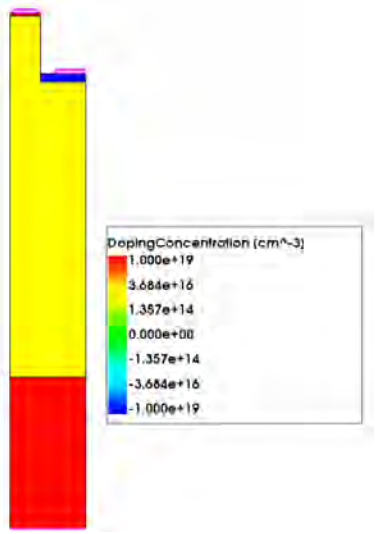


Fig. 3.12 The JFET half unit cell designed using Structure Editor to isolate the effect of x_j from lateral straggling caused by implantation.

The same transfer characteristic sweeps with V_d= 0.05V and 2V were repeated from this structure, and can be seen in figure 3.13. Firstly, it is evident that V_{th} for all designs has become significantly more negative compared to the process simulated results. For example, when x_j= 300nm threshold voltage was -13.5V when V_d= 2V for the previous structure, whilst V_{th} = -18.4V for the structure editor design. This large shift can be explained by the fact that the JFET region width in this simulation is exactly 2μm, compared to 1.49μm according to figure 3.11a, which is only 75% as wide.

Secondly, it is also observed that the trend of V_{th} shifting towards 0V when x_j is larger is replicated. Threshold voltages when V_d= 0.05V are -18.4V, -15.1V, -13.2V and -11.1V for x_j= 300nm,500nm,700nm and 1000nm , respectively. However, the magnitude V_{th} shift is similar to the process simulation: when increasing x_j from 500nm to 700nm, V_{th} moved by +1.9V compared to +1.75V in the process simulation. The lone outlier to this trend is the

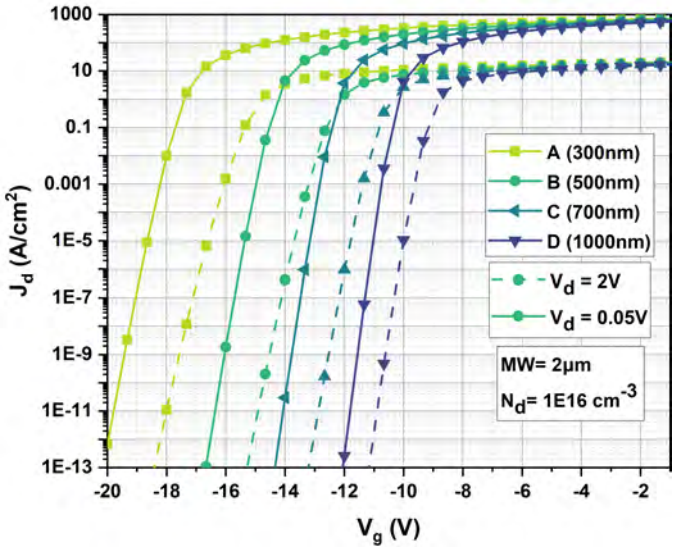


Fig. 3.13 Transfer characteristics of the JFET designed in structure editor for all values of x_j at V_d= 0.05V and 2V.

shift from 300nm to 500nm, which was +7V in the process simulation compared to +3.3V here.

Additionally, the change in V_{th} when V_d was increased to 2V was also found to follow the same trend: as x_j increases, ΔV_{th} reduces which indicates improved control of the channel region. To further elucidate this, figure 3.14 plots the DIBL factor using the V_{th} values extracted from figure 3.13.

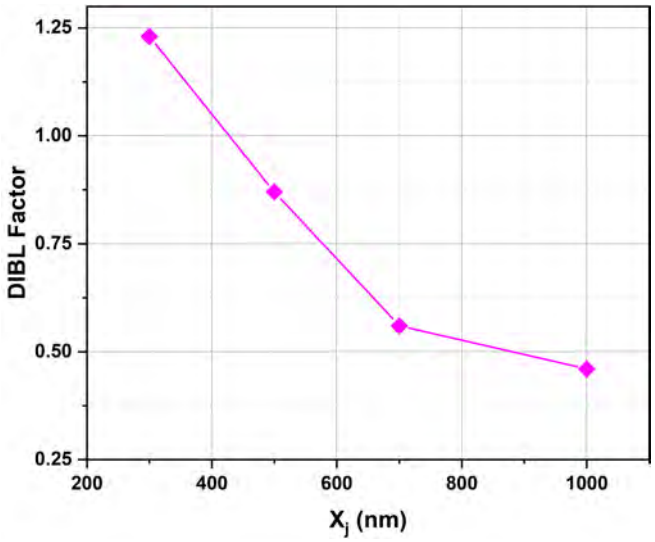


Fig. 3.14 The calculated DIBL factor for the ideal gate junction, plotted as a function of X_j.

As figure 3.14 shows, γ reduces linearly with x_j between 300nm and 700nm from 1.23 down to 0.56. The DIBL factor for 300nm of 1.23 is similar to the 1.33 for the process simulation. However, the values for the remaining 3 junction depths is higher than the previous simulation. This can be attributed to these designs suffering from more pronounced lateral straggling as x_j increases. Nevertheless, the results indicate that although narrowing of the channel region does help mitigate DIBL, this effect is secondary to the dominant role of x_j.

On-State Resistance

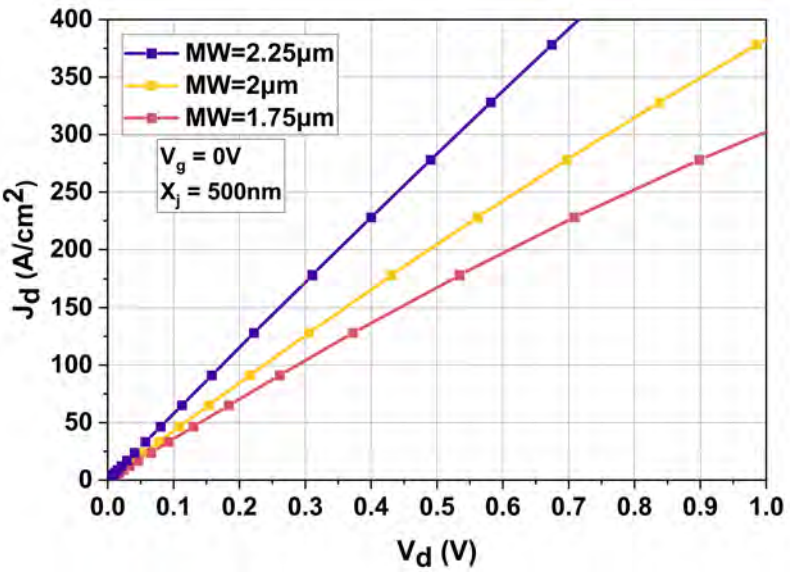


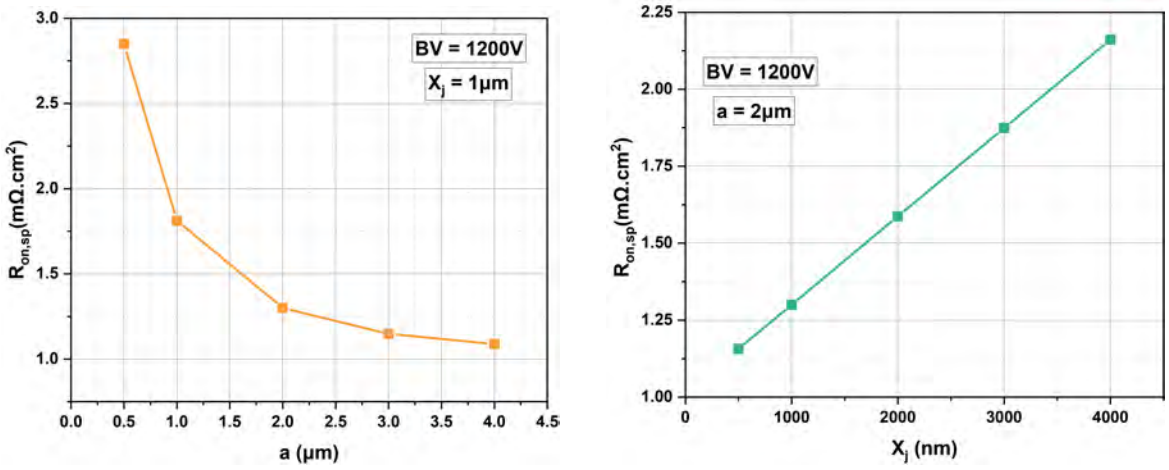
Fig. 3.15 Output characteristics at V_g= 0V for design B with varying mesa width. $R_{on,sp}$ reduces at larger channel widths.

The shape of the channel region, including its width and length also affect the on-state resistance of the JFET. To demonstrate the relationship between channel dimensions and the total resistance, figure 3.16 shows R_{total} as calculated by JFET analytical model presented in Chapter 2 with different x_j and MW values.

$$R_{JFET,sp} = \frac{\rho_{JFET} x_j W_{cell}}{a} \tag{3.3}$$

where a is the effective JFET region width, and W_0 is the zero-bias depletion width of the gate P-N junction:

$$a = MW - 2W_0 \tag{3.4}$$



(a) (b)

Fig. 3.16 Total device resistance $R_{on,sp}$ plotted for different (a) JFET region lengths (x_j) and (b) Mesa Widths as calculated by the analytical model presented in Chapter 2. Lengthening and narrowing the JFET region causes R_{JFET}, and therefore $R_{on,sp}$ to increase.

As shown by figure 3.16a, a narrow JFET region significantly increases R_{JFET} due to constricting the current path. A 500nm wide JFET region will result in $R_{on,sp}$ being over 2.5 times higher than a region which is 3μm wide. Furthermore, 3.16b demonstrates that the JFET region length is directly proportional to R_{JFET} and therefore $R_{on,sp}$.

The output characteristics ($J_d - V_d$) can be used to calculate $R_{on,sp}$. As with the transfer characteristics, J_d has been used in place of I_d. In this case, using J_d enables calculation of $R_{on,sp}$. Figure 3.15 shows the output characteristics design B (x_j = 500nm) with varying mesa widths between 1.75μm - 2.25μm. Specific on-resistance values were extracted at V_d= 0.5V.

Smaller mesa widths result in narrower channels which restrict the width of current flow. This is evident in the specific on-resistance: when MW= 1.75μm, $R_{on,sp}$ is 3mΩcm^{-2}; at MW=2μm, $R_{on,sp}$ is 2.43mΩcm^{-2}; and for MW=2.25μm $R_{on,sp}$ is 1.75mΩcm^{-2}. An example of the 2D current density profile observed at V_d= 1V is shown in figure 3.17 for MW=2μm.

As the channel length in a vertical JFET is equal to the gate junction depth x_j, it is expected that $R_{on,sp}$ will increase linearly with x_j as shown in figure 3.16b. However, due to lateral straggling the channel is also inadvertently narrowed, which further increases in $R_{on,sp}$. This is reflected in figure 3.18, which shows the output characteristics for all four designs at V_g= 0V. Design A has the lowest $R_{on,sp}$ of 1.79mΩcm^{-2}, compared to designs B and C which exhibit values of 2.43mΩcm^{-2} and 3.08mΩcm^{-2}, respectively. Design D has a

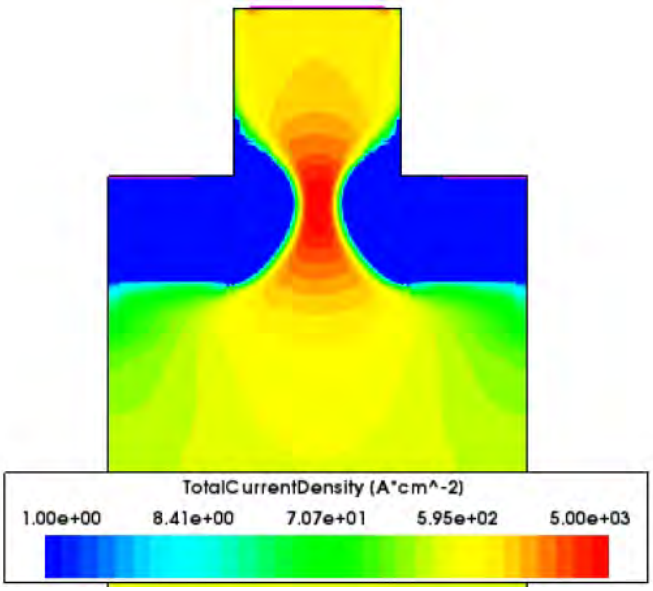


Fig. 3.17 Current density profile for design B at V_d= 1V, V_g= 0V. The highest current density it found in the centre of the JFET channel region.

considerably increased $R_{on,sp}$ of 4.63mΩcm^{-2}, explained by the significant lateral straggling of this design observed previously in figure 3.11b.

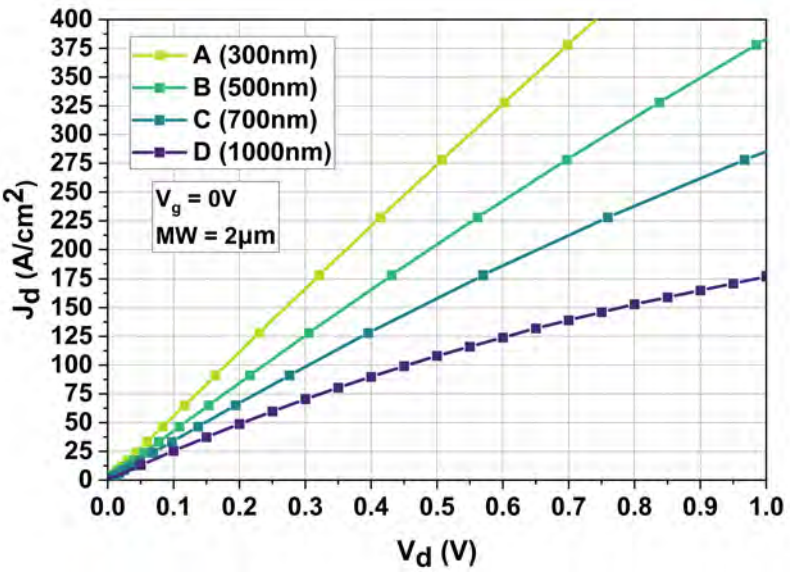
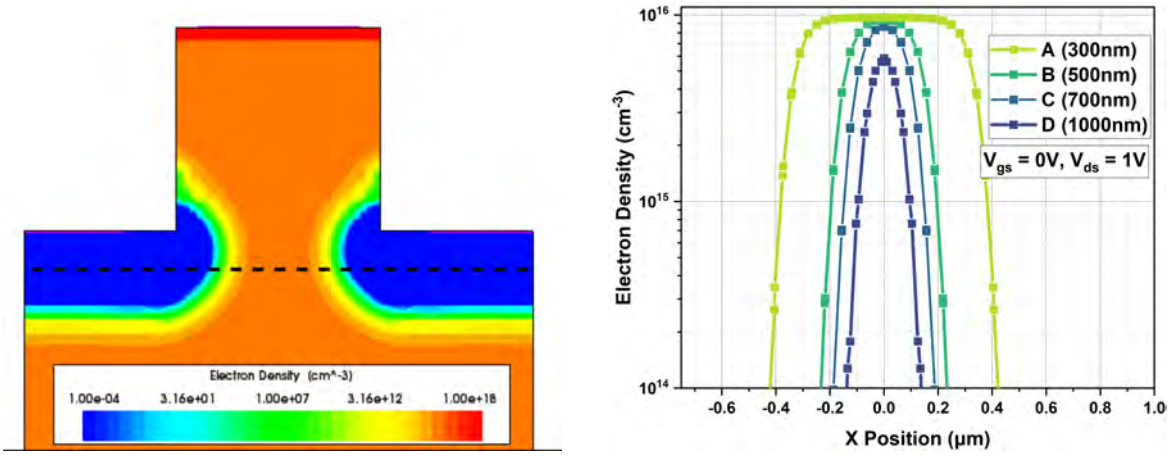


Fig. 3.18 Output characteristics at V_g= 0V of each of the four designs, showing $R_{on,sp}$ increasing with channel length.

Figure 3.19a shows the 2D electron density of design B at V_g= 0V and V_d= 1V, indicating the position of a horizontal cut-line. The resulting electron density along the cut-line for each



(a) (b)

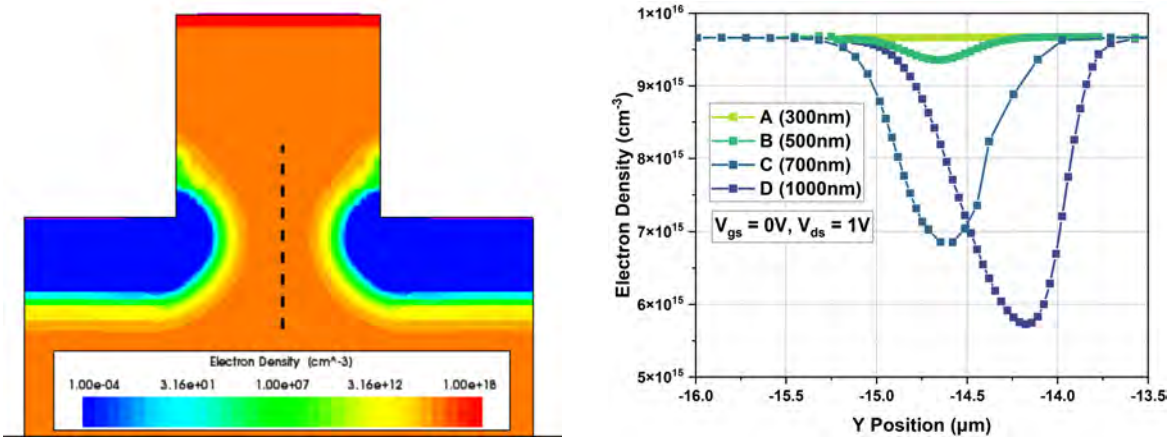
Fig. 3.19 (a) 2D electron density of design A at V_g= 0V, V_d= 1V, with the position of a horizontal cut-line shown by a black dashed line (b) Electron density along the horizontal cut-line for all four designs. As channel length increases, elevated lateral straggling results in a narrower channel width.

design is shown in figure 3.19b. The cut-line clearly shows that the width of electron density above $10^{15} cm^{-3}$ becomes narrower as junction depth increases, due to the lateral straggling effect. For design A, this width is 0.75μm, whilst for design B it is 0.4μm. Comparatively, this width is only equal to 0.2μm for design D.

The electron density within the channel also significantly impacts the channel resistance, and thus $R_{on,sp}$. Figure 3.20a shows the 2D electron density of design B at V_g= 0V & V_d=1V, indicating the position of a vertical cut-line in the centre of the channel. The resulting electron density along the cut-line for each design is shown in figure 3.20b.

At larger junction depths, electron density drops significantly in the centre of the channel to $6.85 \times 10^{15} cm^{-3}$ for design C, and $5.73 \times 10^{15} cm^{-3}$ for design D, compared to design A which has no drop in electron density within the JFET channel compared to the bulk. This indicates that for deeper junctions the JFET channel is actually partially depleted at V_g = 0V, which results in a further increase in $R_{on,sp}$.

The specific on-resistance of designs A and C increase by 24% and 244% when mesa width is reduced to 1.75μm, respectively. The significant increase in $R_{on,sp}$ for design C indicates that the channel is close to being pinched off at V_g= 0V, which is reflected in the low threshold voltage of -1.32V. Furthermore, design D acts as normally-off when MW= 1.75μm, and therefore $R_{on,sp}$ cannot be extracted when V_g= 0V. The calculated threshold voltage for design D with MW= 1.75μm is +0.4V. Table 3.5 shows extracted threshold voltage and on-state resistance for all four designs with mesa widths of 1.75μm and 2μm.



(a) (b)

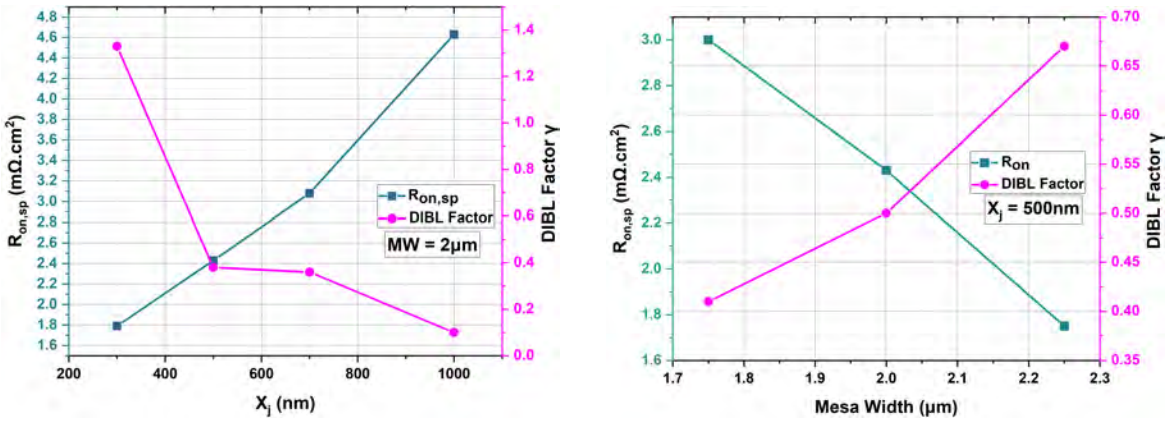
Fig. 3.20 (a) 2D electron density of design A at V_d= 1V, with the position of a vertical cut-line shown by a black dashed line (b) Electron density along the vertical cut-line for all four designs. Longer channel lengths experience partial depletion in the centre of the channel, with the 1000nm long channel having ≤60% of the electron concentration of a 300nm channel.

Table 3.5 Steady-State characteristics of each junction depth for MW=1.75μm and 2μm. $R_{on,sp}$ values are taken at V_g = 0V, V_{th} at V_d = 0.5V and breakdown voltages at V_g = -20V. *$R_{on,sp}$ not extracted due to normally-off operation.

	MW=1.75μm				MW=2μm			
Design	$R_{on,sp}$ (mΩ.cm^{-2})	V_{th} (V)	BV (V)	Failure Type	$R_{on,sp}$ (mΩ.cm^{-2})	V_{th} (V)	BV (V)	Failure Type
A	2.22	-6.75	155	PT	1.79	-13.50	50	PT
B	3.00	-3.80	735	PT	2.43	-6.50	230	PT
C	7.42	-1.82	1367	AV	3.08	-4.75	630	PT
D	-*	0.40	1430	AV	4.63	-2.60	1390	AV

Overall, there is evidently a trade-off between threshold voltage and on-state resistance. To achieve a V_{th} which is closer to 0V, deeper junctions must be used. Designs C and D provide more electrostatic control of the channel, and also effectively narrow the channel due to lateral straggling of dopants. To illustrate the influence of x_j and MW on $R_{on,sp}$ and DIBL, figures 3.21a and 3.21b plot both parameters as a function of x_j and MW, respectively.

By comparing the trends in figure 3.21, it is evident that junction depth has a stronger influence on both $R_{on,sp}$ and DIBL than mesa width. Particular in the case of DIBL factor, increasing x_j almost completely eliminates DIBL at 0.1, whilst reducing MW to 1.75μm still has a value of 0.41. Nevertheless, mesa width still has a strong influence on both parameters, and can be used in combination with x_j to achieve a good design trade-off.



(a) (b)

Fig. 3.21 Specific on-resistance and calculated DIBL factor plotted as a function of (a) junction depth and (b) mesa width. Deeper junctions, and narrower mesas result in a reduced DIBL effect, but at the cost of higher $R_{on,sp}$.

3.3.4 Breakdown Voltage

Channel Length

Breakdown voltage should increase with channel length, as DIBL is eliminated. Narrower channel widths should also improve blocking performance. Figure 3.22 shows the breakdown characteristics ($I_{d(off)}$ - V_d) for all four designs at V_g= -20V. This is the standard gate bias condition used for JFET breakdown voltage measurements by Qorvo [166]. Breakdown is judged to have occurred when $I_{d,off}$ is larger than 10^{-7}A/μm. Extracted breakdown voltages for all designs with MW= 1.75μm and 2μm are displayed in table 3.5.

Figure 3.22 shows that for small channel lengths, the blocking ability of the JFET is significantly degraded. Designs A, B and C fail at V_d= 50V, 230V and 630V, respectively. These values are 3%, 13.8% and 37.7% of the ideal blocking voltage for the drift region used according to the approximation in equation 3.5. This suggests that another failure mechanism other than avalanche breakdown is occurring when JFET channel length is small. Conversely, design D fails at 1390V, which is 83% of the ideal blocking voltage.

$$BV_{pp}(4H-SiC) = 1.7\times10^{15}N_d^{-0.75} \tag{3.5}$$

Figure 3.23a and 3.23b show the current density at breakdown for designs A and D. The current path is established between the source and drain electrodes for designs A, B and C opposed to between the gate and drain as is expected if avalanche had occurred. Conversely, design D fails gate-drain, which is expected when avalanche breakdown occurs.

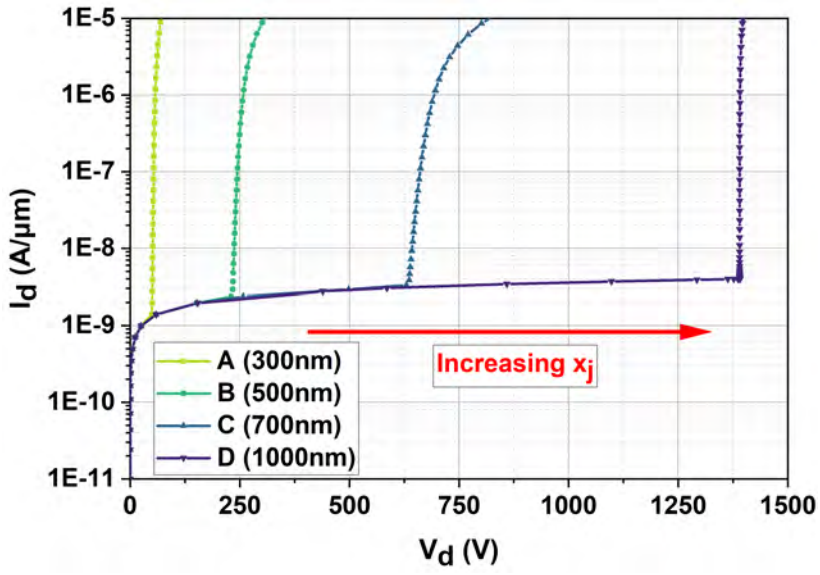
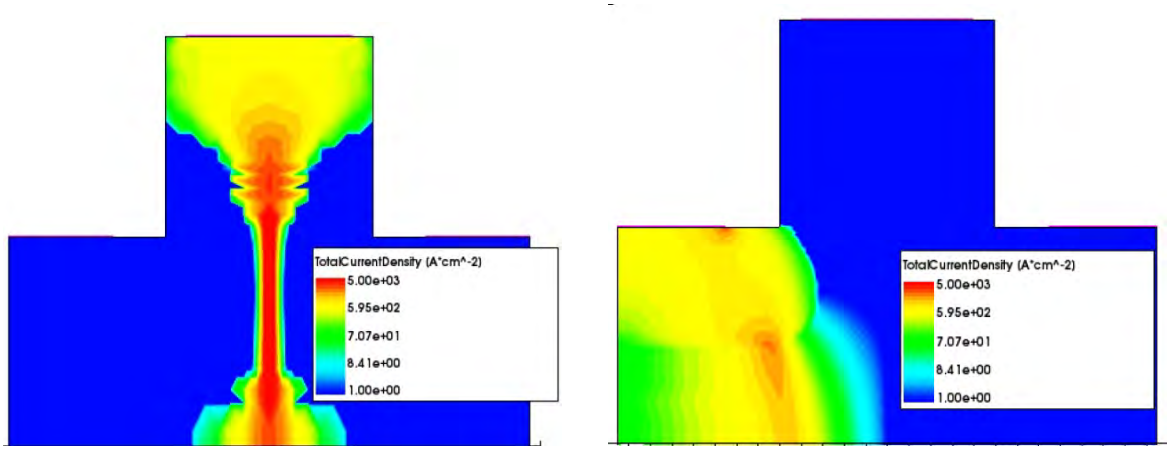


Fig. 3.22 Breakdown characteristics for each design tested at V_g= -20V, with breakdown voltage increasing with junction depth. As junction depth and thus channel length increases, breakdown voltage significantly improves to 1390V for 1000nm.



(a) (b)

Fig. 3.23 Two dimensional current density profile at the point of breakdown for (a) Design A (300nm) showing a current path established between the source and drain electrodes, and (b) Design D (1000nm) showing a current path between the gate and drain electrodes through the gate PN junction.

The positive correlation between x_j and BV indicates that the source-drain failure mechanism observed for designs A, B and C is likely caused by DIBL. At larger junction depths, the channel is lengthened and narrowed due to lateral straggling, which results in the potential barrier in the centre of the channel being larger at V_g= -20V. To illustrate this, figure

3.24 shows the position of a vertical cut-line taken through the centre of the channel. The corresponding potential barrier along the cut-line at V_g = -20V & V_d= 0V is shown in figure 3.25 for all four designs.

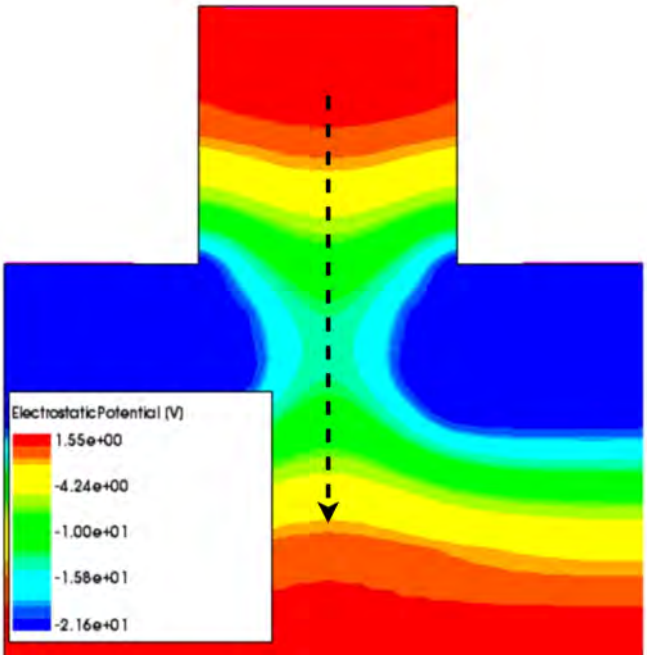
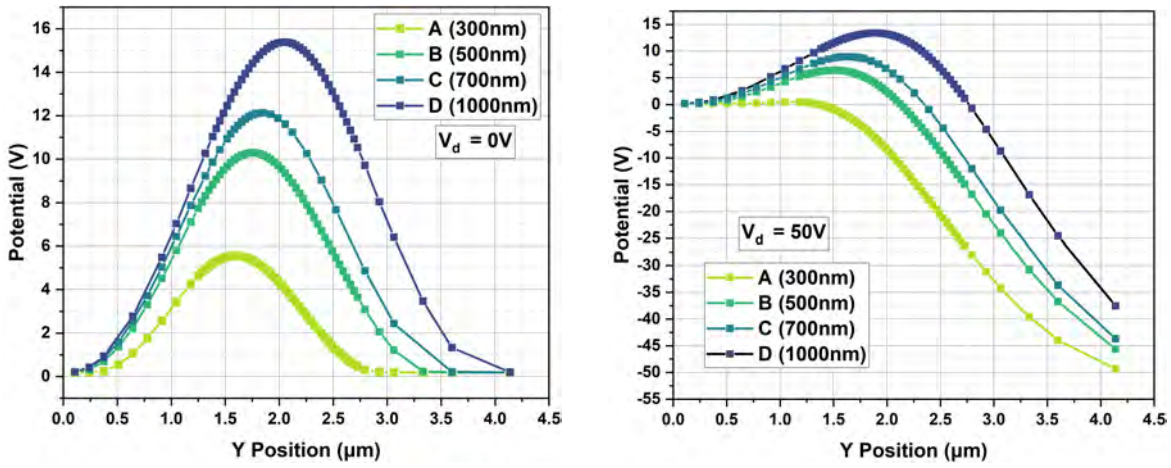


Fig. 3.24 Cross-section of the electrostatic potential profile of design D (1000nm) at V_g=-20V, V_d= 0V. The position of the vertical cut-line is indicated by an arrow.

It can be observed from figure 3.25a that increasing the channel length results in a higher, broader potential barrier. For design A, the maximum height of this barrier is 5.57eV, compared to 10.3eV and 12.13eV for designs B and C, respectively. Design D has the largest barrier at 15.37eV. Figure 3.25b plots the potential along the same cut-line when V_d is increased to 50V. The barrier of design A has collapsed nearly 0eV, which explains why design A fails source-drain at this voltage. The barrier height is also reduced for the remaining designs, which have maximum barrier heights of 6.41eV, 8.95eV and 13.3eV. Therefore, it is concluded that short channel devices experience significant lowering of the potential barrier within the JFET channel due to DIBL, which eventually results in a collapse in the barrier, causing a source-drain current path to be established. This occurs before the JFET has reached the voltage at which avalanche occurs for all designs apart from design D.

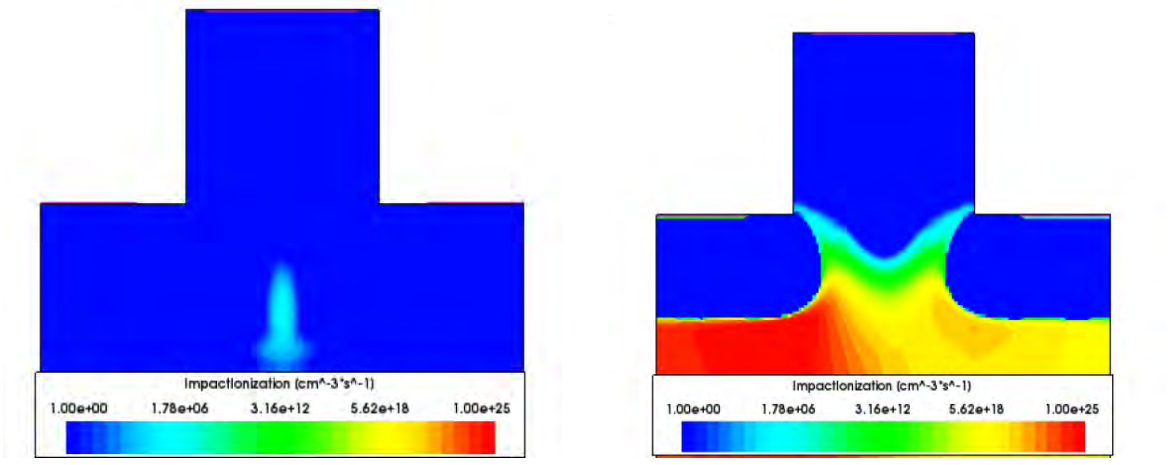
Further validation that DIBL induced failure is occurring in short channel devices can be obtained by plotting in the impact ionization rate (electron-hole pair generation rate) at breakdown. Figure 3.26a and 3.26b show the 2D profile of impact ionization rate of design A and D, respectively. For design A, the highest generation rate is $1 \times 10^4 cm^{-3} s^{-1}$.



(a) (b)

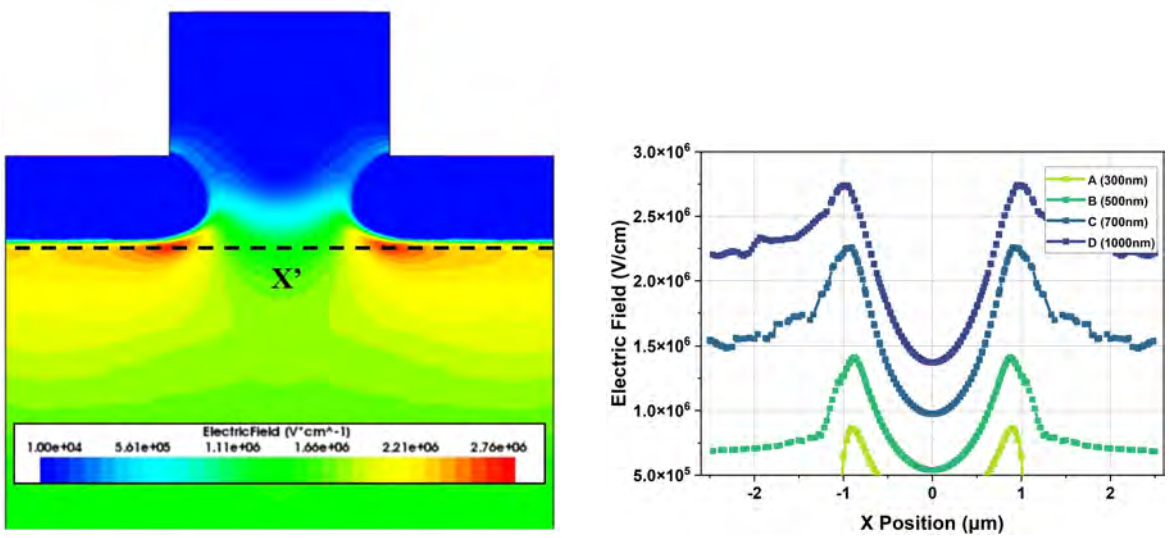
Fig. 3.25 Potential barrier height in the centre of the channel region V_g= -20V with (a) V_d= 0V and (b) V_d= 50V for all four designs. As channel length increases, initial barrier height is larger, and experiences less reduction due to DIBL when V_d rises.

This generation rate is not significant enough to result in avalanche breakdown. Conversely, figure 3.26b shows that the impact generation rate is highest at the gate PN junction at $5 \times 10^{23} cm^{-3} s^{-1}$, which is indicative of avalanche breakdown. Table 3.5 also shows the failure method of each design, where PT denotes DIBL induced punch-through and AV denotes avalanche breakdown.



(a) (b)

Fig. 3.26 Electron-hole pair generation rates at the point of breakdown for (a) Design A and (b) Design D. Design A has a very low impact ionization rate, indicating that avalanche generation of carriers has not occurred. Design D has a significant impact ionization rate of $5 \times 10^{23} cm^{-3} s^{-1}$, verifying that avalanche breakdown has occurred.



(a) (b)

Fig. 3.27 (a) Electric field profile of design D, indicating the position of a cut-line X' (b) Electric field magnitude along cut-line X' for designs A,B,C and D at their respective breakdown voltages. The peak electric field in the designs A, B and C is below the expected E_c of 2.8MV/cm, further verifying that avalanche breakdown has not occurred for these short channel devices.

This conclusion is also supported by observing the Electric field magnitude at the point of breakdown for all designs. Figure 3.27a shows the electric field profile of design D at breakdown, indicating the position of a horizontal cut-line at the gate PN junction corner. The corresponding electric field magnitude along the cut-line for all four designs is shown in figure 3.27b.

The critical field strength of 4H-SiC where avalanche breakdown occurs is around 2.8MV/cm. As seen in figure 3.27b, the only design where this threshold is reached is design D, which fails via avalanche as seen in figure 3.26b. All other designs which fail via punch-through do not reach 2.8MV/cm.

Mesa Width

The impact of DIBL on the breakdown performance of affected designs can be partially mitigated by narrowing mesa width. Figure 3.28 shows the breakdown performance of design B with varying mesa width between 1.75μm - 2.25μm. A mesa width of 2.25μm results in a breakdown voltage of 72V, compared to 735V for MW= 1.75μm. Although the effect of DIBL is not eliminated, by narrowing the mesa the potential barrier height at V_d= 0V, V_g=

-20V is marginally increased. All three mesa widths simulated fail via source-drain punch through rather than avalanche breakdown.

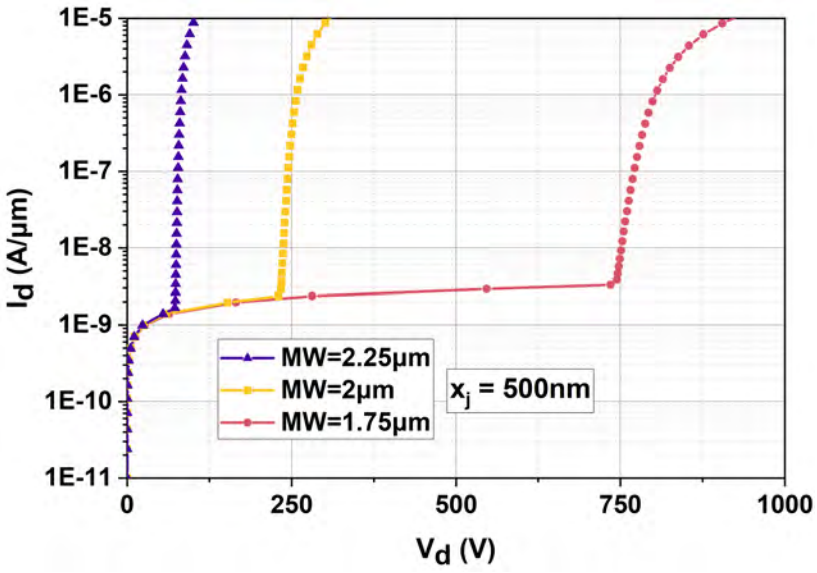
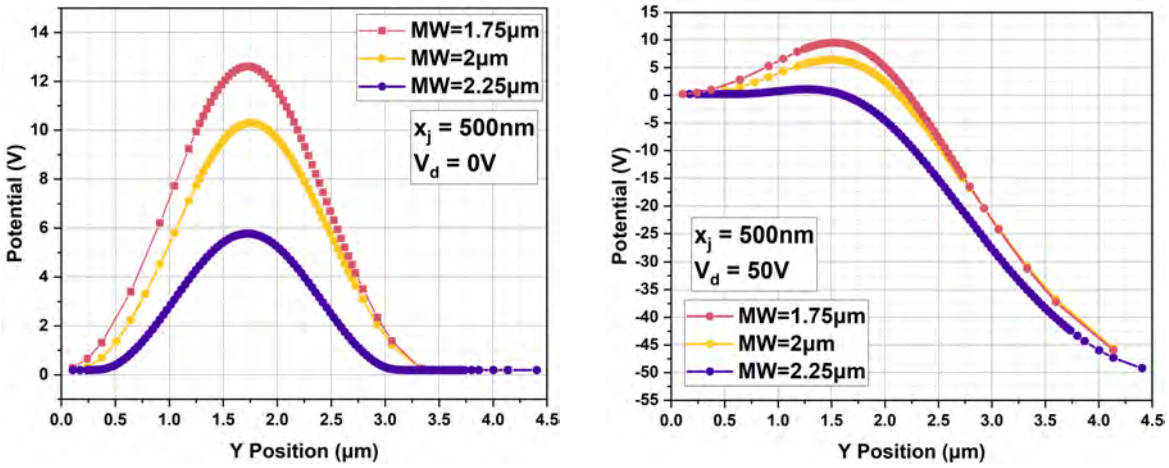


Fig. 3.28 Breakdown characteristics for design B with varying mesa widths between 1.75μm to 2.25μm. Breakdown voltage increases at smaller mesa widths as the initial potential barrier height is increased. Breakdown voltage for MW= 1.75μm is only 735V, which indicates that DIBL induced failure is still occurring.

As when varying the channel length, the same vertical cut-line shown in figure 3.25 was taken for each of the three mesa widths simulated at V_g= -20V with V_d= 0V and 50V applied. Figure 3.29a shows the potential barrier height at V_d= 0V, where the 1.75μm mesa has a 12.6eV barrier, the 2μm mesa 10.3eV and the 2.25μm mesa has a 5.77eV barrier. When V_d is increased to 50V, these barriers reduce to 9.48eV, 6.41eV and 1.07eV, respectively. Since barrier height decreases less with V_d for smaller mesa widths, it can be concluded that reducing mesa width partially mitigates DIBL. However, this effect is less pronounced than that achieved by increasing channel length.

The strength of the effect varying channel length and mesa width has on breakdown voltage can be observed in figure 3.30, using the values reported in table 3.5. As previously discussed, breakdown voltage increases rapidly as the channel elongates. However, this trend is stronger when mesa width is reduced to 1.75μm. In fact, a 700nm channel fails via avalanche if MW= 1.75μm, which is only possible for a 1000nm long channel is MW = 2μm. Thus, a sub-2μm mesa combined with a channel length of ≥700nm would be an acceptable design choice. This approach leverages both x_j and mesa width to mitigate the DIBL failure mechanism, helping to avoid complications such as V_{th} nearing 0V in long channels, and process challenges when the mesa width is too small.



(a) (b)

Fig. 3.29 Potential barrier height for design B (500nm) with varying Mesa Width at V_g = -20 and (a) V_d= 0V, (b) V_d= 50V. Narrowing mesa width results in a larger potential barrier, which increases the voltage at which the device fails between the source and drain electrodes.

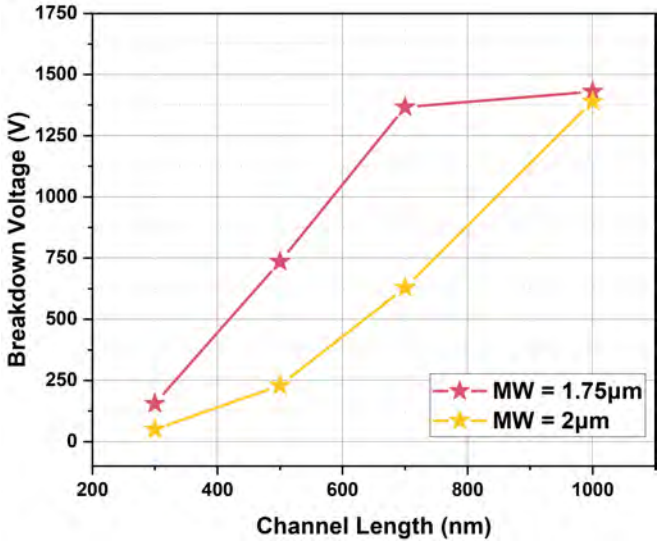


Fig. 3.30 JFET breakdown voltage plotted as a function of channel length for MW=1.75μm and 2μm, using the values found in table 3.5. Breakdown voltage increases with x_j at a greater rate when MW=1.75μm.

Nevertheless, the breakdown performance of most designs results in a poor trade-off between $R_{on,sp}$ and breakdown voltage. This is illustrated below in figure 3.31, which plots $R_{on,sp}$ against breakdown voltage for both MW=2μm and 1.75μm using the values shown in table 3.5. Increasing X_j appears to result in a better trade-off than reducing MW, which is

shown by the 1000nm channel for a 2μm mesa achieving the same breakdown voltage as the 700nm/1.75μm combination, whilst having a 3mΩcm^2 lower $R_{on,sp}$.

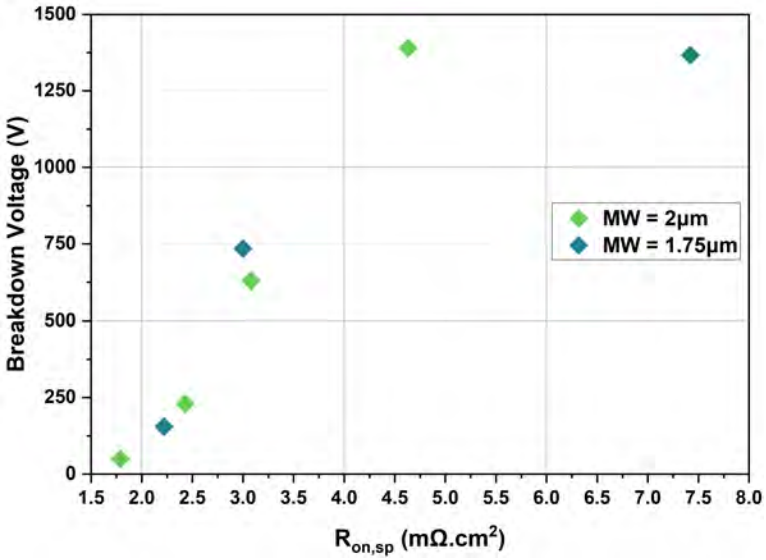


Fig. 3.31 The trade-off between $R_{on,sp}$ and breakdown voltage for both MW= 1.75μm and 2μm.

Hold-off Voltage

By making the gate bias increasingly negative, the barrier height in the channel may also be increased. Figure 3.32 shows the breakdown voltage of design B at different V_g values. By increasing V_g from -20V to -40V, breakdown voltage is increased from 230V to 1250V. It is also observed that at V_g= -40V, the failure mechanism has transitioned from punch-through to avalanche. However, applying increasingly large negative bias is not an attractive solution to system designers, as it is unfeasible for gate driver circuity to supply such voltages.

Hold off voltage (V_{ho}) has been proposed in previous JFET literature, and has been defined as the required gate bias for the JFET to fail via avalanche opposed to punch-through [100]. Any further V_g above V_{ho} will have a minimal effect on breakdown performance. Figure 3.32 shows this, as increasing V_g to -50V does not result in any breakdown voltage increasing compared to V_g= -40V.

Hold off voltage for varying mesa width and x_j is shown in figure 3.33. As expected, due to their small junction depths, designs A and B require significant applied V_g to fail via avalanche; at MW= 2μm hold off voltage is -70V and -40V for designs A and B, respectively. On the other hand, design D does not even require gate bias to be -20V to fail via avalanche; V_{ho}= -10V and -14V for MW= 1.75μm and 2μm, respectively. Increasing mesa width results

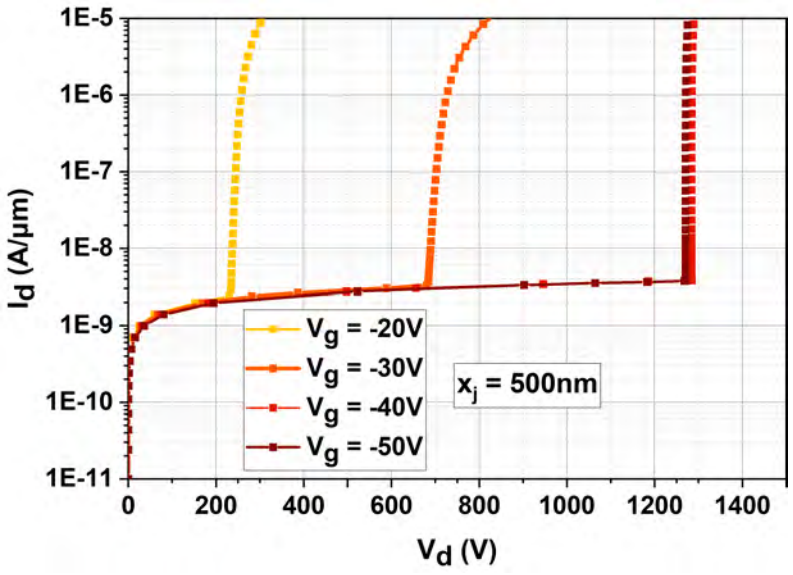


Fig. 3.32 Breakdown characteristics for design B with varying V_g, with breakdown voltage increasing at larger V_g. Breakdown voltage saturates between V_g= -40V to -50V as avalanche breakdown has begun to occur.

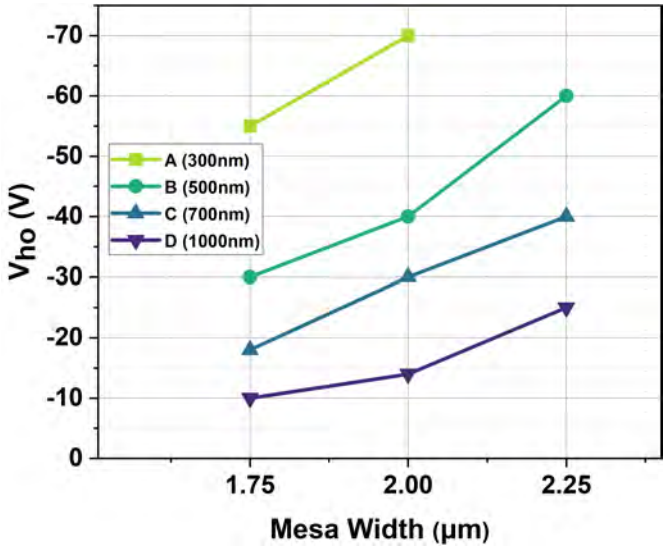


Fig. 3.33 Hold off voltage plotted for varying mesa width for all four designs, with V_{ho} reducing at larger x_j. Hold-off voltage is smallest for the 1000nm channel with a mesa width of 1.75μm, which is V_{ho}= -10V.

in an increase in V_{ho} for all designs, as larger V_g is required to form a significant potential barrier.

3.3.5 Summary

Drain-induced barrier lowering has been shown to be prevalent in SiC JFETs with channel lengths of less than 1000nm when channel width is 2μm. In the device on-state manifests as an increasingly negative V_{th} which is highly sensitive to applied V_d. Breakdown voltage is severely reduced in short channel devices by DIBL induced punch-through of the JFET channel. Increasing x_j is the preferred solution to eliminate DIBL induced failure, and achieve acceptable breakdown voltage.

An additional complication unique to vertical SiC JFETs is the lateral straggling of implanted ions. To achieve larger x_j values, more high energy implantation events are required. High energy, high dose implants result in significant lateral straggling into the JFET channel region, reducing channel width. This in turn shifts V_{th} towards 0V, and increases $R_{on,sp}$. This effect is not present in lateral SiC JFETs demonstrated by [159]. The effect of the channel width reducing via lateral straggle is difficult to separate from DIBL in longer channel devices.

JFET mesa width can also be narrowed to shift V_{th} towards 0V, and to improve breakdown voltage. This also increased $R_{ds,on}$. However, DIBL induced punch-through remains the failure mechanism rather than avalanche breakdown. Applying negative gate voltage above V_g = -20V can be used to achieve avalanche breakdown in short channel designs, however this is highly unattractive for system designers. The hold-off voltage demonstrates that only channel lengths of 700nm or 1000nm can be feasibly used when limited to V_g= -20V.

3.4 Introducing Sidewall Implantation

3.4.1 Introduction

This section discusses the design approach of implementing sidewall P-type doping into the JFET structure to increase the channel length without requiring high energy implantation. This design is compared to the JFET without sidewall doping presented in the previous section. The potential benefits of this design are weighed against the additional complexity of fabricating such a device.

The findings of the previous section clearly show that to achieve acceptable breakdown voltage performance, DIBL induced punch-through failures must be eliminated. The previous section showed that three methods can be used to achieve this: larger junction depths, narrower mesa widths and making applied gate bias more negative. Of the three, increased junction depth is the most viable option at the device design level - using narrower mesa

widths is challenging to achieve with contact lithography, which may result in requiring dimensions $\leq 1\mu$m, which would require a stepper to achieve.

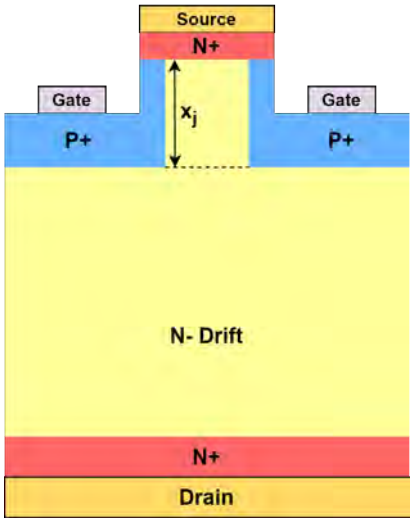


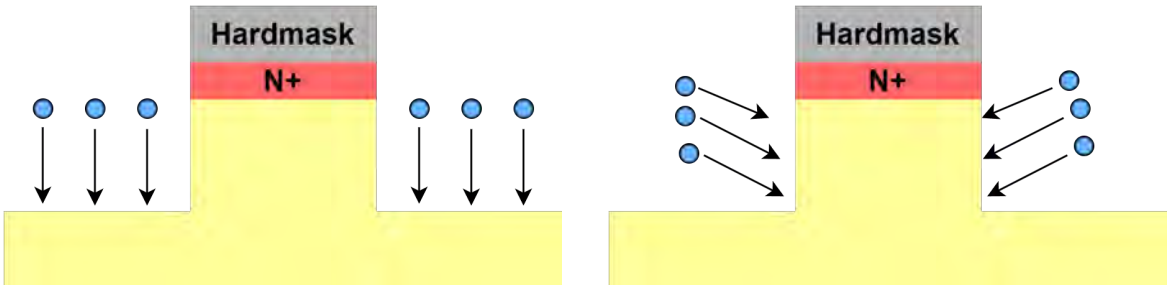
Fig. 3.34 The cross-section of a JFET unit cell with P-type doping on the mesa sidewall. Introducing sidewall doping significantly increases the JFET channel length without requiring high energy implantation.

However, deeper junctions result in the narrowing of the channel region due to lateral straggling of implanted ions, significantly increasing $R_{on,sp}$ and affecting V_{th}. In the JFET design tested, the depth of the gate junction x_j is equal to the channel length. As making x_j larger is not viable both from the perspective of $R_{on,sp}$ and practically due to required implantation energies, alternative solutions should be investigated.

The most promising option to artificially increase the channel length is P-type implantation of the mesa sidewall. This avoids the need for high energy implantation, while increasing the JFET region length. Therefore, it should increase breakdown performance, whist also reducing the impact of lateral straggling at high implantation energies. Figure 3.34 shows the unit cell cross-section of a JFET with sidewall implantation. This design approach has been used by Qorvo in their previous generations of JFETs [167]. To achieve implantation of a 90° sidewall, tilted implantation must be used. A visualisation of the difference between tilted and standard implantation at 0° is shown in figure 3.35.

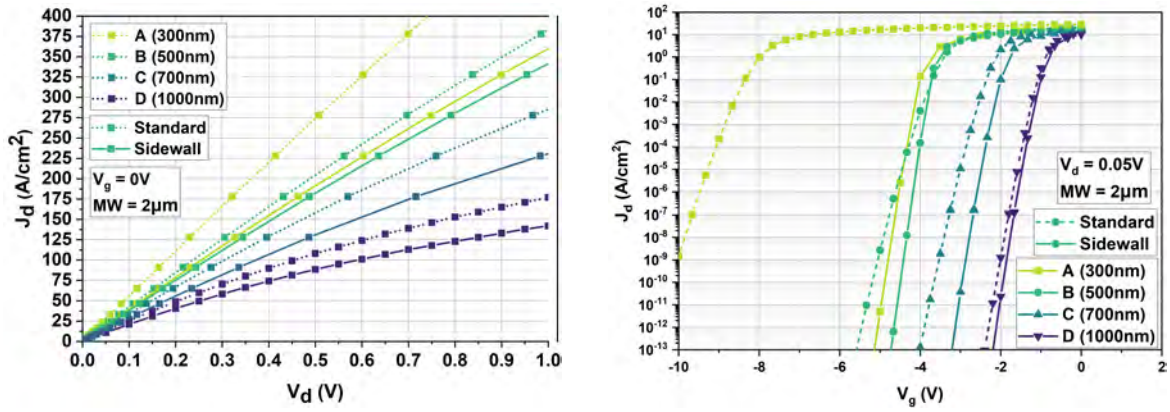
3.4.2 Comparison to Non-Sidewall Implanted JFET

To simulate this, the first two implantations detailed in table 3.4 (40keV and 100keV) were repeated with a tilt angle of 30°. Figure 3.36a shows the output characteristics of all four designs with and without the additional sidewall implantation. Due to the increased channel



(a) (b)

Fig. 3.35 Visualisation of (a) standard implantation at 0°and (b) sidewall implantation at a arbitrary tilt angle. Tilted implantation is required to achieve P-type doping on the mesa sidewalls. Additionally, two tilted implantation events must occur for each energy - one to implant each sidewall.



(a) (b)

Fig. 3.36 Comparing all four designs with and without sidewall implantation for (a) output characteristics, where sidewall implantation increases $R_{on,sp}$ for all designs and (b) transfer characteristics, where V_{th} is shifted significantly towards 0V for small junction depths.

length in the sidewall design, channel resistance is increased. Consequentially, for design B on-state resistance rises to 2.74mΩcm^2, an increase of 12.8%.

Threshold voltage is significantly shifted towards 0V for small junction depths as seen in figure 3.36b; design A shifts by +5.75V and design B by +1.8V. As JFET channel width is not significantly affected by sidewall implantation, this highlights the significant affect DIBL has on threshold voltage for short channel lengths. For designs C and D, the threshold voltage shifts by only +1.51V and +0.4V, respectively.

The breakdown performance of all four designs with and without sidewall implantation is shown in figure 3.37. Breakdown voltage is significantly increased by implementing sidewall implantation for designs A, B and C to 1275V, 1302V and 1373V, respectively. Furthermore,

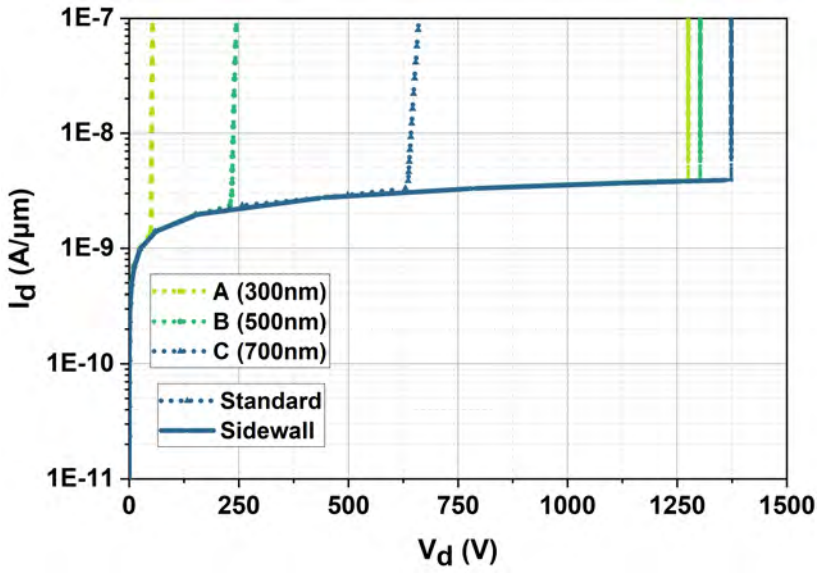


Fig. 3.37 Breakdown performance of designs A,B and C with and without sidewall implantation. Breakdown voltage increases by over 1000V for a 300nm gate junction depth when sidewall implantation is used. With sidewall p-type doping, all designs fail via avalanche rather than DIBL induced punch through. The design with a 1000nm junction depth does not experience an improvement in BV as it already failed via avalanche, and thus is not shown.

the failure mechanism of all three designs has transitioned from DIBL induced punch-through to avalanche breakdown. Since design D was not originally prone to DIBL, introducing sidewall implantation did not result in any improvement in breakdown voltage. This indicates by lengthening the channel in the vulnerable designs, DIBL has been successfully suppressed.

To further verify this, the trade-off between $R_{on,sp}$ and breakdown voltage for both the sidewall and non-sidewall implanted JFET is shown in figure 3.38. The graph clearly shows that there is not a significant trade-off between $R_{on,sp}$ and breakdown voltage for the sidewall implanted JFET, with all designs exhibiting a breakdown voltage of over 1250V.

Figure 3.39 displays how the potential barrier is higher and broader by introducing sidewall doping in design B. The standard design has a barrier which is greater than 5eV for 1.9μm with a maximum height of 10.28eV. On the other hand, when sidewall implantation is included the barrier remains above 5eV for 2.4μm, with a peak of 14.26eV. For the sidewall design, the channel region is effectively equal to the sum of implantation depth and mesa height, which for design B is 2.5μm.

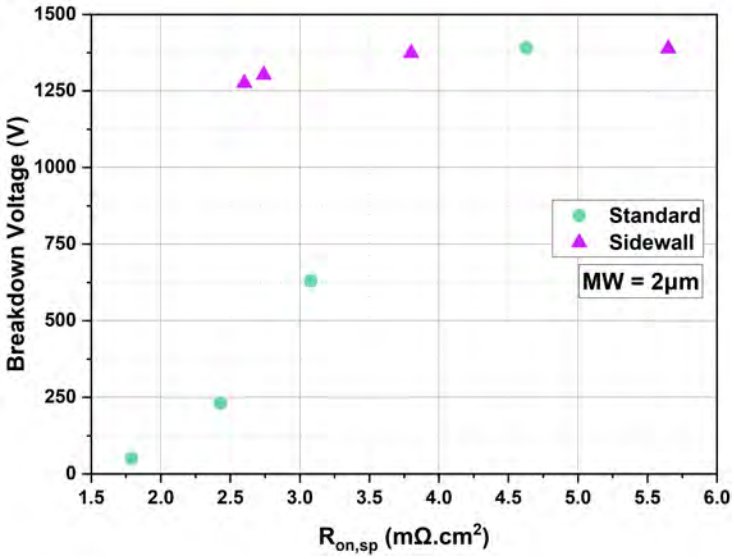


Fig. 3.38 Trade-off between $R_{on,sp}$ and breakdown voltage for both the sidewall and non-sidewall implanted JFETs. By implementing sidewall implantation the trade-off is significantly improved.

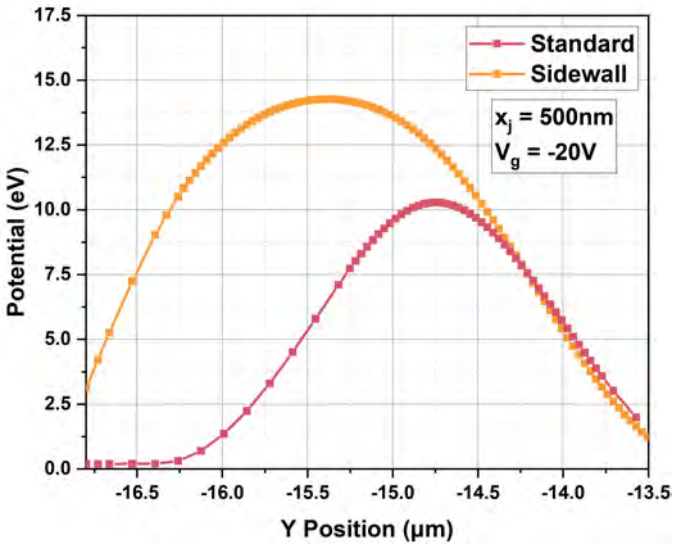


Fig. 3.39 Potential barrier height of design B at V_d=0V, V_g= -20V. By introducing sidewall P-type doping, the potential barrier is larger, and broader.

3.4.3 Varying Mesa Height

It has clearly been shown that the influence of DIBL on breakdown performance is primarily dependant on the JFET channel length. Therefore, when utilising sidewall implantation the channel length is dependant on the height of the JFET mesa. Thus, it is likely that there is a minimum mesa height (MH) to result in avalanche breakdown and consequentially good

Table 3.6 Steady-State characteristics of comparing each design with an without sidewall implantation. Mesa width is 2μm. $R_{on,sp}$ values are taken at V_g = 0V, V_d= 0.5V, V_{th} at V_d = 0.05V and BV at V_g = -20V.

	No Sidewall				Sidewall			
Design	$R_{on,sp}$ (mΩ.cm^{-2})	V_{th} (V)	BV (V)	Failure Type	$R_{on,sp}$ (mΩ.cm^{-2})	V_{th} (V)	BV (V)	Failure Type
A	1.79	-13.50	50	PT	2.60	-5.15	1275	AV
B	2.43	-6.50	230	PT	2.74	-4.70	1302	AV
C	3.08	-4.75	630	PT	3.80	-3.24	1373	AV
D	4.63	-2.60	1390	AV	5.65	-2.20	1388	AV

breakdown performance. Smaller mesa heights can be easier to achieve via dry etching processes in practice.

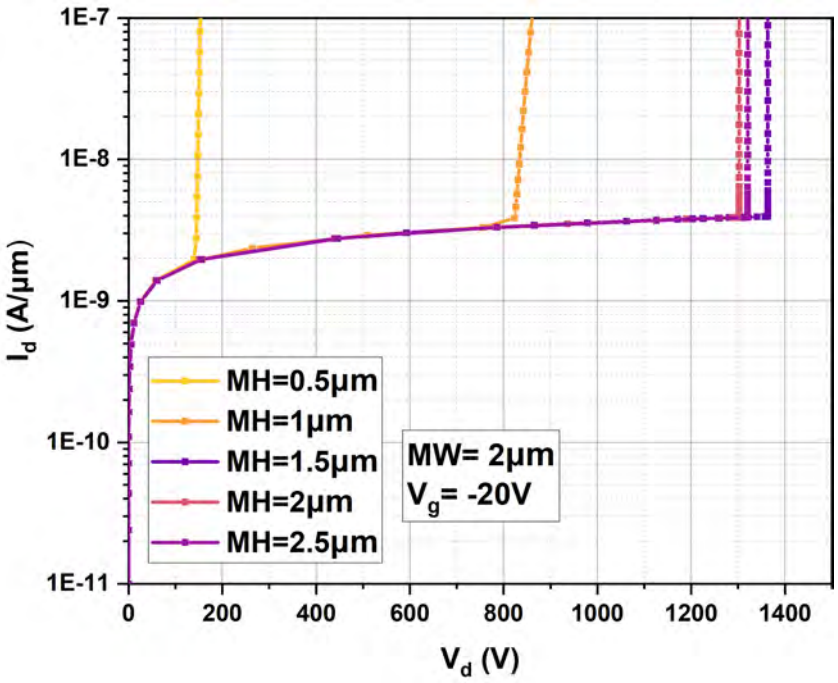


Fig. 3.40 Breakdown characteristics for the sidewall implanted design B (500nm), with varying mesa height. Breakdown voltage significantly reduces when mesa height is small because the channel length is reduced.

Figure 3.40 shows the off-state characteristics of the design B with additional sidewall implantation, with mesa height varying between 0.5μm - 2.5μm and a mesa width of 2μm. A mesa height of 0.5μm results in a breakdown voltage of only 140V, whilst when MH = 1μm the voltage increases to 824V. It should be noted that designs with both of these mesa heights fail via punch-through rather than avalanche. However, a mesa heights of 1.5, 2 and 2.5μm fail via avalanche at 1302V, 1320V and 1363V, respectively. This suggests that a the mesa

must have a minimum aspect ratio of 0.75:1 to ensure avalanche breakdown. Increasing the aspect ratio above 1:1 does not appear to result in any significant performance improvement.

3.4.4 Achieving Sidewall Doping Without Tilted Implantation

Overall, sidewall implantation is an excellent method to lengthen the JFET channel region and eliminate DIBL induced failure mechanisms. The increase in on-state resistance is at most 25%, whilst increasing breakdown voltage by up to 1200V for shallow junction depths, such as in design A and B.

Achieving implantation of a 90° sidewall can be challenging in practice. In the results shown previously for the sidewall design, a 30° implantation angle was used. Although not considered for a unit cell such as the one simulated, shadowing effects caused by adjacent mesas may result in uneven coverage of the sidewall, not to mention the fact that two tilted implants are required for every standard 0° implant (one implant for each side of the mesa). Uneven coverage of P-type dopants on the mesa sidewall will result in wild variation of electrical performance of devices across a wafer. Additionally, doubling the amount of implantations required will add additional cost and time to the fabrication process. Figure 3.41 illustrates how the shadowing effect can occur when using tilted implantation.

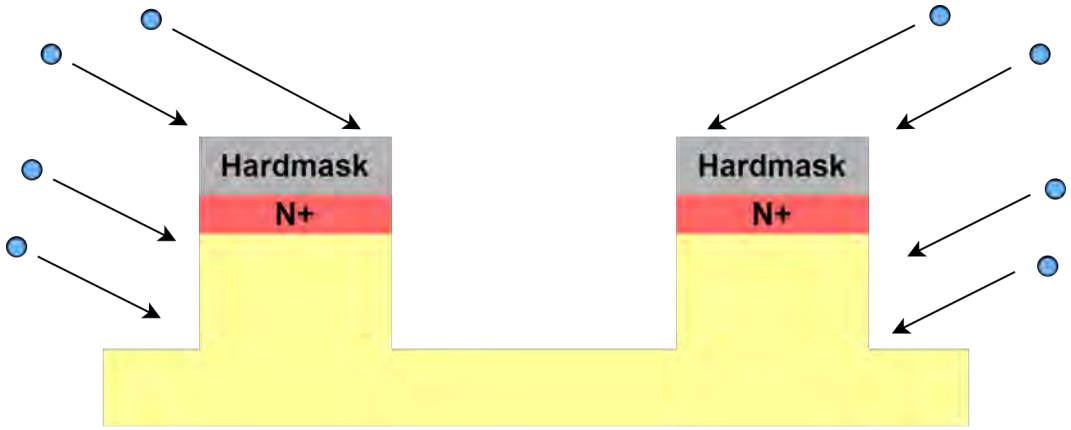


Fig. 3.41 Schematic illustration of how adjacent mesas can cause the shadowing effect when using tilted implantation.

One solution which may be cost-effective is the use of a mesa with an acute sidewall angle. This enables standard 0° implantation to be used, avoiding all the associated problems with tilted implantation, whilst also achieving good coverage of the mesa sidewall. Figure 3.42 shows how by using standard implantation for a JFET with an acute mesa sidewall will result in sidewall doping.

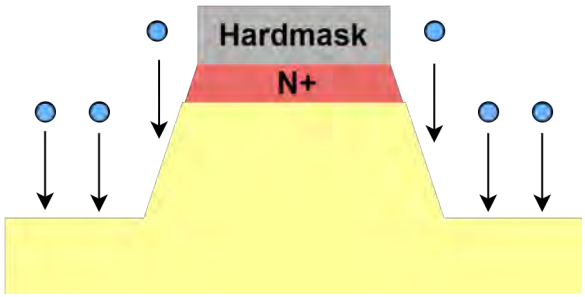
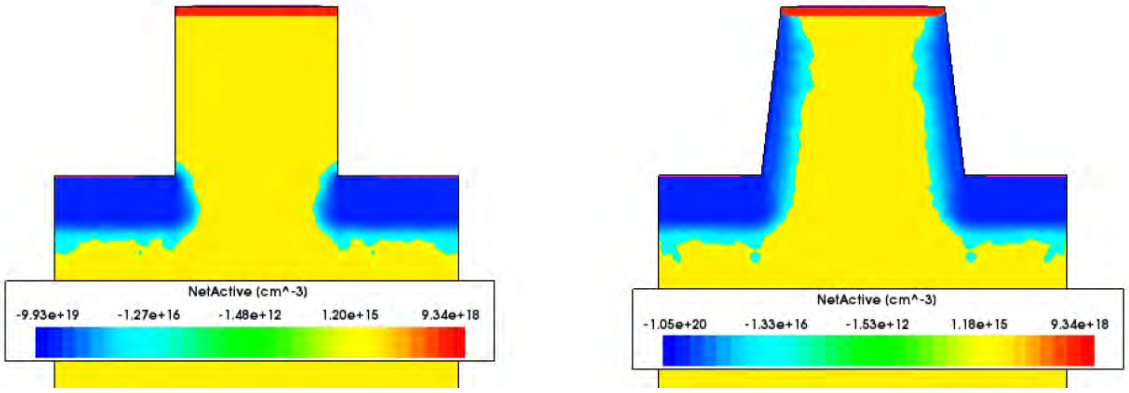


Fig. 3.42 Schematic visualising coverage of the angled mesa sidewall when using standard 0° implantation.

Figure 3.43 compares the doping profiles of the standard 0° implantation design with different sidewall angles. As expected, the vertical sidewall has minimal P-type coverage on the sidewall, whilst the 85° design has significant coverage.



(a) (b)

Fig. 3.43 Doping profiles of design B when using 0° implantation with (a) a 90° sidewall (b) a 85° sidewall.

As already shown in the previous section, increasing the length of the JFET channel significantly enhances the breakdown voltage. Figure 3.44 shows that a more acute sidewall angle results in marginally poorer blocking performance, with an 83° sidewall blocking 1217V and a 87° sidewall blocking 1323V. All sidewall angles tested fail through avalanche breakdown. Compared to the tilted implantation design shown in figure 3.37, the breakdown voltage of the slanted sidewall design is within 100V for all angles tested.

As with the sidewall design achieved by tilted implantation, the lengthening of the channel region does increase on-state resistance. For a 87° sidewall, $R_{on,sp}$ is increased to 2.81mΩcm^2 compared to 2.43Ωcm^2 for the vertical sidewall. There is very little difference in on-state resistance between the different angles tested.

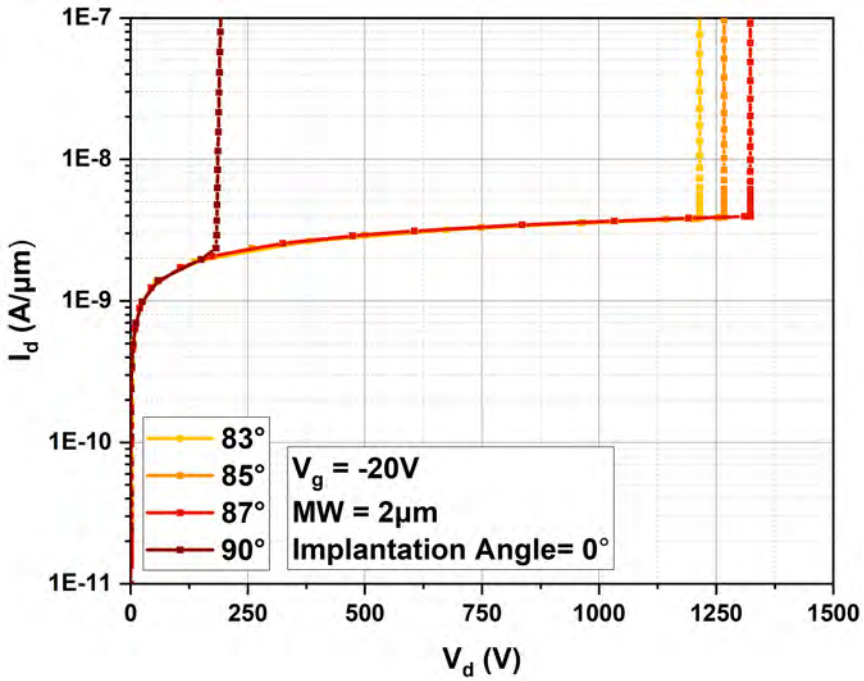


Fig. 3.44 Breakdown characteristics for standard 0° implantation for different mesa sidewall angles. By making the angle acute, P-type coverage of the sidewall is achieved with 0°implantation, resulting in a longer channel not affected by DIBL.

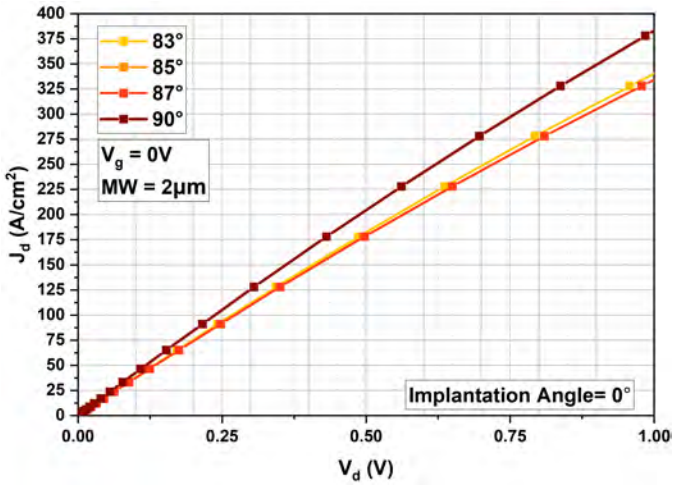


Fig. 3.45 Output characteristics for standard 0° implantation for different sidewall angles. Using an acute sidewall angle increases the channel length, which increases $R_{on,sp}$.

3.4.5 Summary

Introducing P-type doping on the JFET mesa sidewall to increase the channel length has been proven to be an effective method to eliminate DIBL without requiring high implantation

energies. All junction depths tested fail via avalanche rather than DIBL induced punch-through with sidewall implantation. Breakdown voltage increased by over 1000V for a 300nm gate junction depth. Threshold voltage also shifted towards 0V significantly for small junction depths (300nm and 500nm), indicating that these designs were significantly affected by DIBL in the on-state also. As the channel length is increased in this design, $R_{on,sp}$ increases as expected compared to the initial design, by 45% for a 300nm gate junction depth. Other designs with deeper gate junctions only experience a maximum 22% increase in $R_{on,sp}$.

To fabricate this design, tilted implantation must be used. This necessitates two tilted implants for each energy - one to cover each side of the JFET mesa. Thus, the fabrication process required to realise this design is more complex than the standard JFET. Additional care must be taken to prevent shadowing caused by adjacent mesas, which could lead to uneven dopant profiles on mesa sidewalls. Nonetheless, these challenges are justified by the significant improvement in device performance achieved.

Using a JFET mesa with an acute sidewall angle will enable sidewall P-type doping to be achieved without requiring tilted implantation, removing the added complexity from the fabrication process. Using a 87°sidewall with a 0°implant schedule (as originally used in the previous section) resulted in a breakdown voltage of 1323V. On-state resistance was only increased marginally compared to the 90°design.

3.5 Edge Termination: Floating Field Rings

Up to now, all simulations have been conducted on a JFET unit cell. While unit cells are effective for capturing device behaviour such as V_{th} and $R_{on,sp}$, they do not fully represent the behaviour of a realistic JFET device. In a realistic device using a stripe configuration, there is always a final device cell. The gate PN junction of this edge cell experiences significant electric field crowding due to the absence of an adjacent PN junction to evenly distribute the field. Figure 3.46 illustrates the doping profile of the JFET edge cell. Due to this crowding effect, the breakdown voltage of a edge cell will be significantly lower than a unit cell. In the case of the JFET, the un-terminated cell shown below in figure 3.46 has a breakdown voltage of 484V.

To improve breakdown performance, edge termination structures are used to mitigate the electric field crowding on the outer device cells. These structures are essential to achieve breakdown voltages close to the rated voltage of the drift region. Figure 3.47a shows the electric field of the JFET edge cell at 450V. As seen in figure 3.47b, the electric field at the outer gate junction is over 1MV/cm higher than the inner junction.

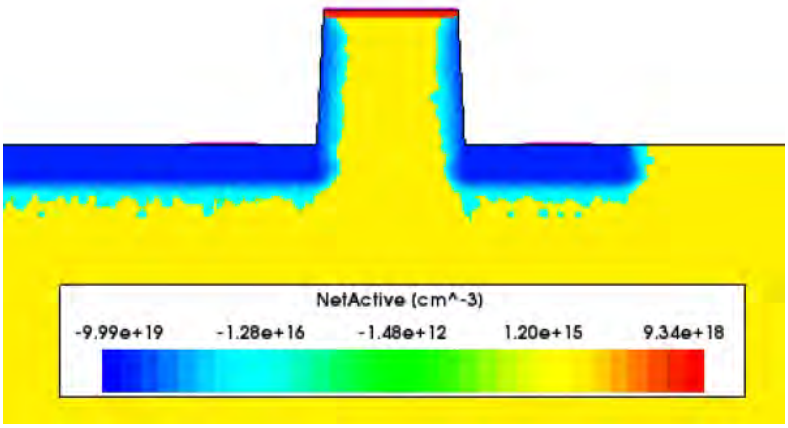
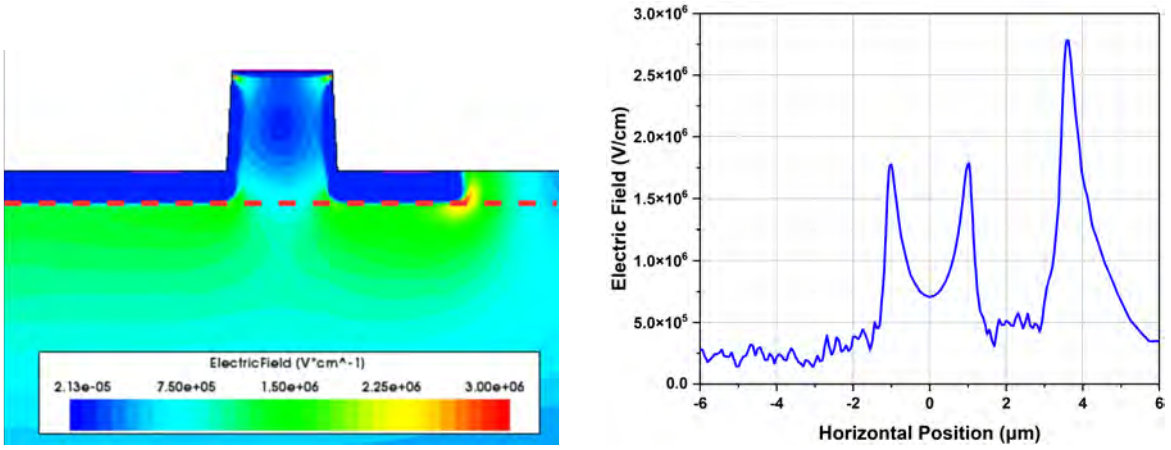


Fig. 3.46 Doping profile of design B (500nm) JFET edge cell, showing the outer gate junction at the extremity of the die.



(a) (b)

Fig. 3.47 (a) Electric field profile of the JFET edge cell with an un-terminated gate junction at V_d= 450V, showing the location of a horizontal cut-line (b) Electric field magnitude along the horizontal cut-line, showing a disproportionately large peak at the outermost gate junction due to field crowding.

For the remainder of this section, it is assumed that the JFET is failing via avalanche breakdown as a result of correct design of the JFET channel region (i.e. sidewall implantation). As avalanche occurs at the gate PN junction, only the gate PN junction is simulated for efficiency.

One of the most common termination structures that is used are Floating Field Rings (FFRs). Floating field rings consist of highly doped P-type regions adjacent to the main junction that are not connected to a contact. Under reverse bias, as the depletion region

extends the FFRs assist in the spreading of the depletion region. This effectively reduces the high electric field at the main junction.

The key benefit of FFRs in the context of a JFET is that they can be simultaneously formed with the main gate junction via implantation. This has been demonstrated by Veliadis et al. [110]. This is not necessarily possible when fabricating MOSFETs, as the P-body implant is not as highly doped. In a fully optimised FFR termination structure, the electric field would be shared equally between the FFRs and the main junction [168].

Higher voltage ratings require more extensive edge termination structures. For a 4500V PiN diode, 35 adjacent rings which is equal to a width of 180μm has been demonstrated [169]. For comparison, 100 adjacent rings with a total width of 528μm were utilised to achieve a 7.9kV breakdown voltage for a SiC planar MOSFET [170]. Termination region widths approaching 800μm have been used to for a SiC MOSFET with a breakdown voltage of 13kV has been demonstrated by the same group [165]. Fortunately for a breakdown voltage of 1200V, termination structures take up a relative small fraction of the total die area.

3.5.1 Constant Ring Spacing

There are two key parameters which must be optimised for FFR structures - the number of rings (n) and the spacing between adjacent rings (S). It has been shown by simulation that ring width does not significantly affect breakdown voltage [171], therefore the ring width remains constant at 2μm. The optimum values for both parameters is dependant on the drift region doping concentration used. Therefore, the drift region remains the same as in the rest of this chapter (N_d=$10^{16} cm^{-3}$, thickness = 15μm). The P-type implantation scheme used to form the main junction and FFRs is a box profile of $N_a \geq 10^{19} cm^{-3}$ which is 500nm deep, that is detailed in table 3.4. Additionally, a 1μm thick SiO_2 layer has been deposited on the SiC surface post-implantation.

For this optimisation procedure, three values of n were tested: 3 rings, 6 rings and 12 rings. The spacings between adjacent rings was varied between 1.2μm - 2.2μm. Table 3.7 shows the extracted breakdown voltage values of each combination of n and S. The efficiency of the FFR structure is compared to the JFET unit cell breakdown voltage with an 87° sidewall, which is 1322V.

The breakdown voltages for each design found in table 3.7 have been plotted in figure 3.48. For the 3 ring design, it was found that breakdown voltage increased with spacing up to 690V at S= 2.2μm. However, this is remains only just 52.2% of the unit cell breakdown voltage. When increasing to 6 rings, an optimum spacing of 2μm was found, with a breakdown voltage of 807V, which corresponds to an efficiency of 61%. Finally, the 12 ring design has an optimum spacing of 1.8μm, which resulted in a breakdown voltage of 1003V, equal to

Table 3.7 Extracted breakdown voltages for different combinations of ring number n, and adjacent ring spacing S. The breakdown voltage increases with n. The optimum value of S for a 12 ring design is 1.8μm.

	n= 3		n= 6		n= 12	
S	BV (V)	Efficiency (%)	BV (V)	Efficiency (%)	BV (V)	Efficiency (%)
1.2	380	28.7	407	30.8	465	35.2
1.3	412	31.2	435	32.9	529	40.0
1.4	443	33.5	466	35.3	607	45.9
1.5	455	34.4	532	40.2	785	59.4
1.6	474	35.9	593	44.9	842	63.7
1.7	510	38.6	641	48.5	984	74.4
1.8	550	41.6	702	53.1	1003	75.9
1.9	589	44.2	771	58.3	951	71.9
2.0	631	47.7	807	61.0	884	66.4
2.1	673	50.9	756	57.2	855	64.7
2.2	690	52.2	683	51.7	782	59.2

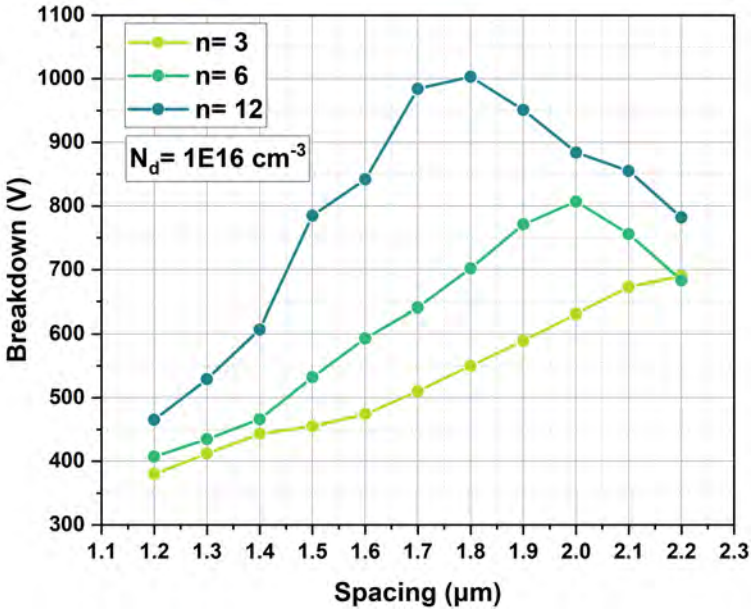
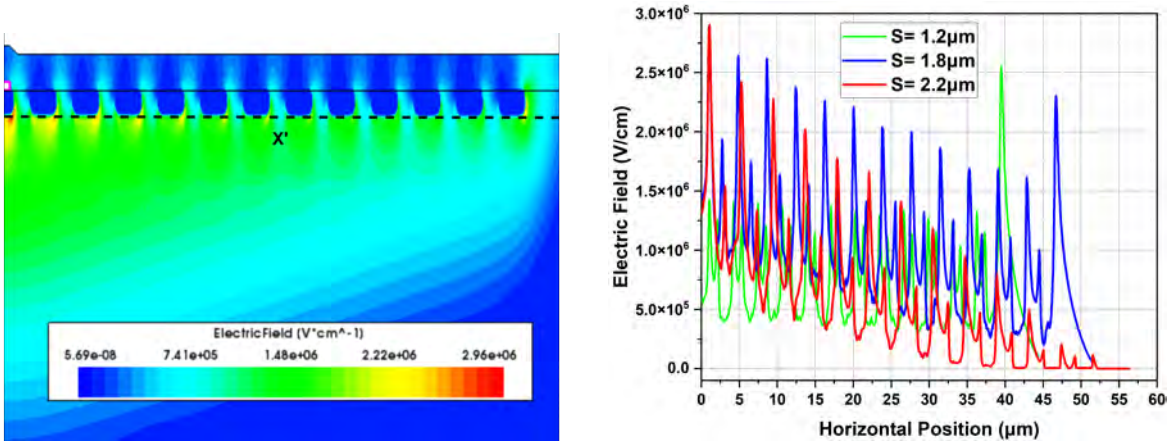


Fig. 3.48 Breakdown voltage values for the 3,6 and 12 ring designs for the range of spacings between 1.2-2.2μm. The optimum value of S reduces as more rings are introduced. The 6 and 12 ring designs exhibit high sensitivity to variation in S away from the optimum value.

75.9% efficiency. Spacings larger than 1.8μm for this design resulted in a steady decay in breakdown voltage down to 782V for S= 2.2μm.

Increasing the number of rings used improves breakdown voltage for all spacings used. The only anomaly found was that for n=6 with S= 2.2μm, the breakdown voltage was 7V lower than the 3 ring design with the same spacing.

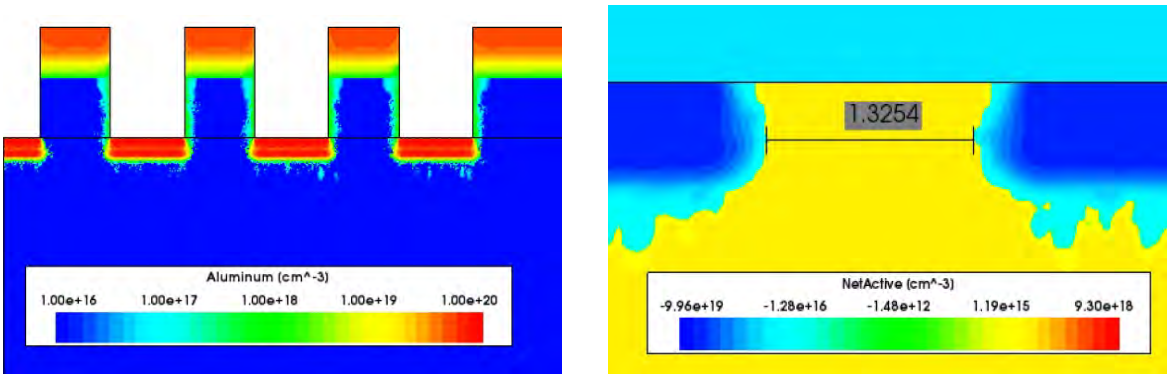
Figure 3.49a shows the electric field profile of the 12 ring design with S = 1.8μm at the point of breakdown. The position of the horizontal cut-line $X^{'}$ is indicated. The magnitude of the electric field along $X^{'}$ for 12 ring designs with S= 1.2μm, 1.8μm and 2.2μm at breakdown is plotted in figure 3.49b. Ideally, each of the field rings should share the electric field equally. If the spacing between rings is too small, and the outer most ring will experience significant crowding. This is clearly occurs for S=1.2μm. On the other hand, if the spacing is too large, then the termination doesn't effectively spread the depletion region, resulting in peak electric field at the main junction and many of the rings not experiencing significant electric field, as seen for S= 2.2μm. The outer most ring for the optimum spacing of S= 1.8μm still experiences significantly higher electric field than inner rings, indicating this design is not fully optimised.



(a) (b)

Fig. 3.49 (a) Electric field profile of S= 1.8μm at the point of breakdown, with the position of the horizontal cut-line X' indicated (b) Electric field magnitude along X' at breakdown for S = 1.2μm, 1.8μm and 2.2μm.

Upon inspection of the doping profile of the field rings, lateral straggling of implanted aluminium ions is evident, as seen in figure 3.50a. The distance between adjacent rings for a designed spacing of 2μm was found to be 1.3μm on average. Similarly, when S= 1.8μm the distance was an average of 1.1μm. Therefore, it is assumed that due to lateral straggling of implanted ions, the actual spacing between rings is 0.7μm smaller than designed.



(a) (b)

Fig. 3.50 (a) Aluminium concentration profile post-implantation, showing lateral straggling under the masking material (b) measured spacing of 1.3μm between the adjacent floating field rings for a designed spacing of 2μm.

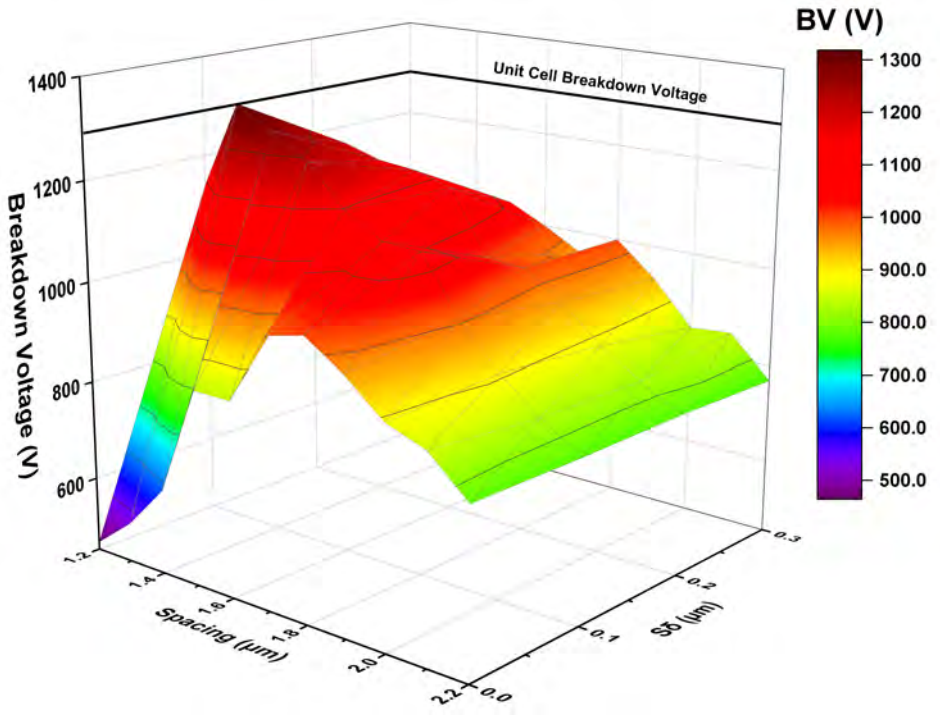


Fig. 3.51 A heat-map for the 12 FFR design, plotting initial and incremental spacing with breakdown voltage. Optimum combinations are found at smaller values of S, with S_δ=0.1μm.

3.5.2 Incremental Ring Spacing

It has been suggested to gradually increase the spacing between the rings to optimize the electric field distribution, rather than maintaining a uniform spacing S [165, 170, 172, 173].

This incremental increase in spacing is expressed in equation (3.6), where S_n is the nth spacing, S_δ is the incremental spacing and n is the number of rings.

$$S_n = S + S_\delta(n-1) \tag{3.6}$$

Different S_δ values have been proposed, from 0.08μm [165] to 0.3μm [172]. Therefore, an optimisation procedure was carried out for all values of S already tested, but with S_δ varying between 0.1μm - 0.3μm for the 12 ring design. A heat-map of the results is shown in figure 3.51.

As seen in the heat-map, smaller spacings benefit significantly from incrementally increasing the spacing between rings. Introducing a S_δ value of 0.1μm resulted an improvement in breakdown voltage of over 100V for all spacings apart from S= 1.8μm - 2.2μm. This indicates that the initial spacing was too large. This agrees with the electric field profiles of S= 1.8μm and 2.2μm shown in figure 3.49b.

Breakdown voltage is far more sensitive to S than S_δ. Decreasing initial spacing from 1.3μm to 1.2μm when S_δ= 0.1μm reduces breakdown voltage by 177V. Without incremental spacing for S= 1.2μm, 1.3μm and 1.4μm their breakdown voltages are only 465V, 529V and 620V, respectively.

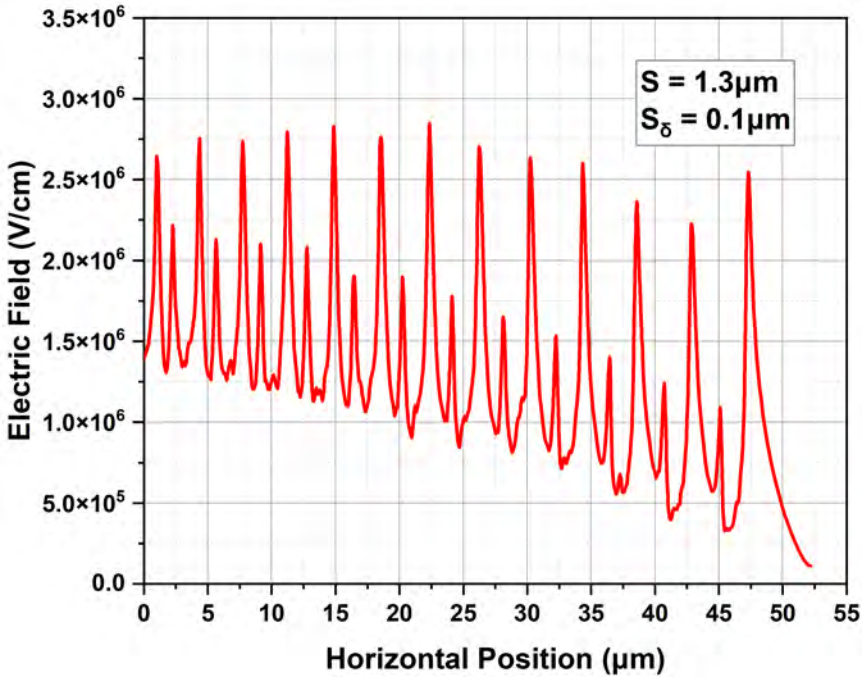


Fig. 3.52 Electric field profile along horizontal cut-line X' for the optimum combination of S= 1.3μm,S_δ= 0.1μm.

The optimum design was found to be S= 1.3μm with S_δ= 0.1μm, which had a breakdown voltage of 1317V. This is ≥99% of the unit cell breakdown voltage. This indicates that this design is fully optimised. Large incremental spacings of S_δ= 0.2μm and 0.3μm did not improve breakdown voltage further. To verify that the combination of S= 1.3μm and S_δ= 0.1μm, a horizontal cut-line is taken in the same position as has already been used for figure 3.49b. This is shown in figure 3.52 where the electric field magnitude at each ring is within 2.2-2.8MV/cm.

3.5.3 Sensitivity to Interface Charge

As termination structures mitigate field by screening charge away from the main junction, it follows that as fixed interface charge affects depletion region shape, it will also effect termination efficiency. It has been found that a positive charge densities ($q_[ox]$) at the SiC/SiO_2 interface has negatively impacted the blocking performance of Junction Termination Extensions (JTEs) [174]. Positive charge densities have been shown to be prevalent at the material interface [80, 174]. In practice, if the FFR termination should be highly sensitive to charge build-up at the material interface, breakdown voltage could reduce as the JFET gets repeatedly stressed in reverse bias.

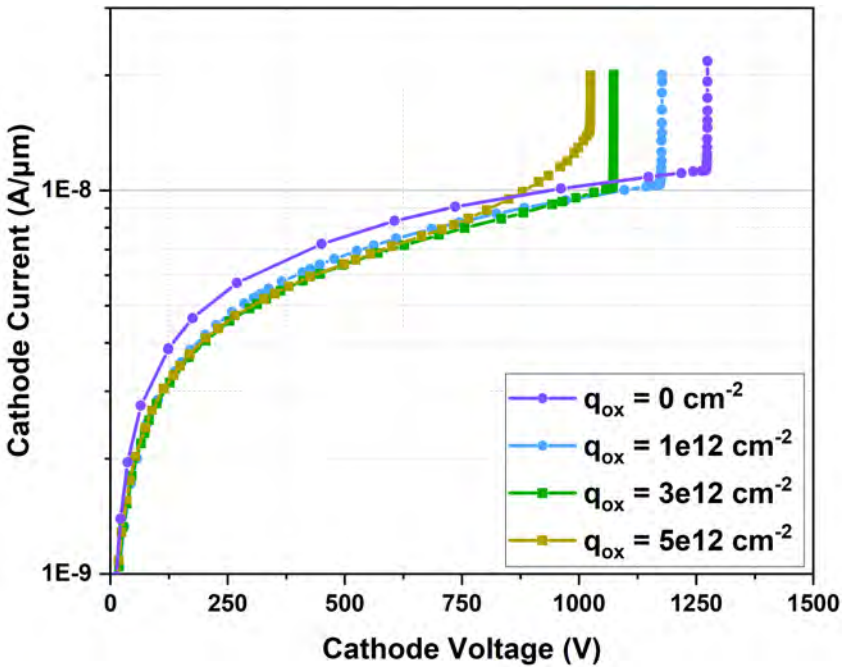


Fig. 3.53 Breakdown characteristics for the S= 1.4μm, S_δ= 0.1μm design with varying positive fixed charge at the SiC/SiO_2 interface. Breakdown voltage reduces as positive charge increases.

To assess the sensitivity of FFRs to positive interface charge (q_{ox}), breakdown simulations were carried out on the S= 1.4μm , S_δ= 0.1μm tested in the previous section with different q_{ox} values between $10^{12}cm^{-2}$ - $5\times10^{12}cm^{-2}$. This design has a breakdown voltage of 1274V with no interface charge.

As figure 3.53 shows, breakdown voltage does reduce significantly with large q_{ox} values. When q_{ox}= $10^{12}cm^{-2}$, breakdown voltage is 1177V, a reduction of 97V compared to the ideal case with no interface charge. Increasing q_{ox} results in breakdown voltage lowering further to 1024V when q_{ox}= $5\times10^{12}cm^{-2}$. This is a 250V degradation in breakdown voltage, which is equal to a 18.9% drop in termination efficiency for the JFET unit cell which as a breakdown voltage of 1322V.

Figure 3.54 shows the electric field profile along the cut-line X' for the design with q_{ox} = 0 cm^{-2} and $5\times10^{12}cm^{-2}$. It is evident that the introduction of positive fixed charge causes the depletion region to not spread as effectively. This results in the outer FFRs to not support any electric field, and consequentially more crowding at the main junction which reduces the breakdown voltage.

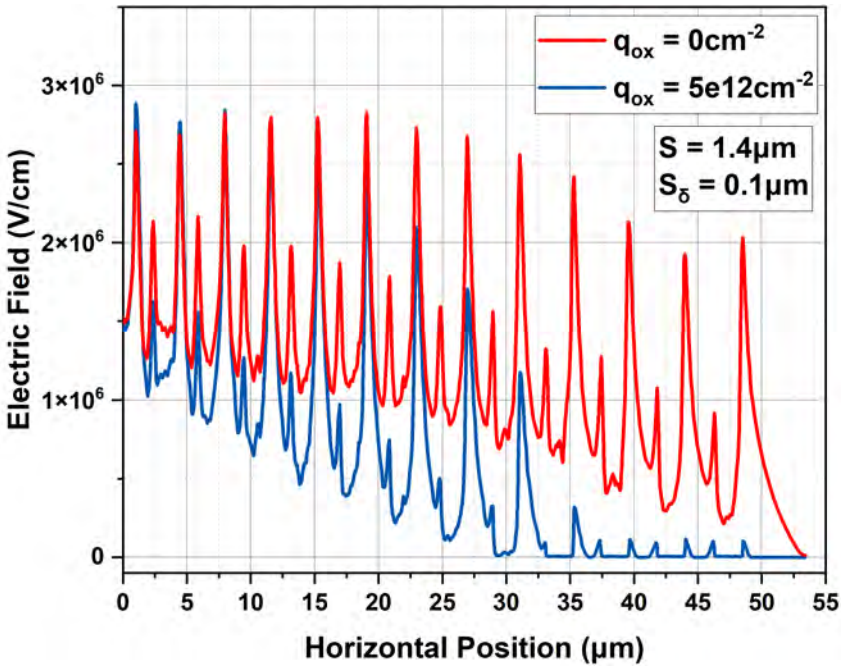


Fig. 3.54 Electric field magnitude along the horziontal cut-line X' for the S= 1.4μm, S_δ= 0.1μm design with q_{ox}= $0cm^{-2}$ and $5\times10^{12}cm^{-2}$. Introduction of positive fixed charge causes the outer most rings to not support electric field equally.

Overall, FFRs can provide excellent field management which results in 99% of the unit cell breakdown voltage. However, the process window for these structures is incredibly small - misalignment by 0.1μm can result breakdown voltage reducing by over 100V in some

cases. Furthermore, the performance of FFR structures is sensitive to any fixed charge in any dielectric deposited on the SiC surface. This can also reduce breakdown voltage. Hybrid termination structures which consist of both JTEs and FFRs have been proved to have wider process windows, and less sensitivity to interface charge [169, 170, 175]. However, these would require dedicated mask layers to fabricate in practice.

3.6 Conclusion

This chapter has comprehensively investigated the relevant design parameters which must be considered for SiC JFETs. It was found that the JFET performance is highly sensitive to the gate junction depth and mesa width, especially in the off-state. In fact, DIBL induced punch-through causes premature failure of the JFET if both parameters are not correctly optimised. In general, larger junction depths and smaller mesa widths are required to prevent this punch-through mechanism. If not correctly optimised, this can result in breakdown voltages of only 50V when using drift region rated for at least 1200V.

Lateral straggling of implanted aluminium ions artificially narrows the JFET channel width. This effect is particularly prevalent at large junction depths, when the required implantation energies are high. Straggling shifts V_{th} towards 0V, and may assist with preventing punch-through failures. Unfortunately, achieving the large junction depths required for acceptable breakdown performance can result in the JFET becoming normally off.

An alternative to large junction depths is to implant the mesa sidewall via tilted implantation. By utilising tilted implantation, smaller implantation energies can be used to achieve large equivalent junction depths (and thereby JFET channel lengths). This resulted in breakdown performance improvement of over 1000V for some designs tested. However, tilted implantation does require double the implantation events to cover both sides of the mesa. A promising solution is to use mesas with acute sidewall angles. This enables standard 0° implantation to be used to achieve mesa sidewall coverage.

Edge termination structures are essential to prevent field crowding at the die extremities, which causes breakdown voltage to significantly decrease. Floating Field Rings are an edge termination design approach which can be formed concurrently with the main JFET gate P+ junction. Therefore, FFRs can be seamlessly integrated into a JFET process flow. The spacing between adjacent FFRs significantly impacts the performance of the rings and, consequently, the device's breakdown voltage. An initial spacing of 1.3μm, with an increment of 0.1μm per ring resulted in a breakdown voltage ≥99% of the unit cell's value. However, there is a very narrow optimum window for spacing values, which could easily be missed by misalignment

in practice. Positive fixed charge introduced by depositing dielectrics on the wafer surface can also significantly hamper the FFRs ability to negate field crowding effects.

Chapter 4

A JFET with a Monolithically Integrated Temperature Sensor

4.1 Preface

This chapter discusses the device design of a novel SiC JFET with a monolithically integrated temperature sensor by utilising the gate P+ implant to form a lateral resistor. The sensor performance at a range of temperatures, and its interaction with the JFET is investigated using Synopsys TCAD. This involves electrothermal simulations to model device self-heating effects, and transient simulations to monitor sensor behaviour under switching conditions.

Work in this chapter was presented at ICSCRM 2023, which has been published in *Key Engineering Materials* titled "*Design of Monolithically Integrated Temperature Sensors in 4H-SiC JFETs*" [176]. Subsequentially, this work was expanded upon and published in the journal "*Power Electronic Devices and Components*" under the title: "*A 4H-SiC JFET with a monolithically integrated temperature sensor*" [177].

4.2 A Review of SiC Temperature Sensors

Accurate monitoring of internal device temperature (T_j) in an application is highly desired for industries that operate at high temperatures such as the oil, automotive and aerospace industries [178, 179].

The approach of most semiconductor temperature sensors is to monitor a Temperature Sensitive Electrical Parameter (TSEP). Most commonly this TSEP is the forward voltage (V_f) of a Schottky Barrier Diode (SBD) or a PN diode. Silicon Carbide SBD temperature sensors have been demonstrated [180, 181]. Using two SiC SBDs in parallel for temperature

sensing purposes has also been demonstrated up to 700K [182]. Furthermore, SiC PN diodes have been utilized as temperature sensors, with excellent linearity between 176-802K [183].

Ideally, temperature sensors should be integrated on the same chip as the active device - this is known as *monolithic integration*. Being located on the same chip as the JFET will result in highly accurate and responsive T_j monitoring. In contrast, sensors placed outside the device package (i.e. on the same PCB) will be less accurate and responsive due to the different thermal conductivity of packaging materials. For successful monolithic integration, the temperature sensor must be electrically isolated from the main device, with minimal interference (cross-talk) between the two.

Monolithic integration of temperature sensors in SiC has been through various methods. These include a MOSFET with utilizing a lateral SBD as a sensor [94] and incorporating an integrated gate resistor [184]. Additionally, a lateral resistor created concurrently with the main MOSFET P-body has also been demonstrated [95]. Using the MOSFET P-body implant offers a unique advantage of other methods, as the sensor is formed concurrently with the main device, and does not require additional fabrication steps.

4.3 Integrating a Temperature Sensor with a SiC JFET

As previously discussed, the key benefit on SiC JFETs compared to SiC MOSFETs is the absence of a gate oxide. This eliminates the reliability issues associated with the SiC/SiO_2 interface. The high D_{it} values of this interface can manifest as positive or negative bias temperature instability under bias stress [185], which causes V_{th} drift over the devices lifetime. Threshold voltage drift can result in increased on-state resistance, increased off-state leakage [81, 186, 187]. Due to these issues, most commercial SiC MOSFETs have a maximum operating temperature of 150°C. Conversely, SiC JFETs are highly suitable for high-temperature, high-reliability applications where SiC MOSFETs may not be appropriate due to these reliability concerns.

SiC JFETs have been demonstrated to have no V_{th} shift up to 175°C [100], and only a -0.8V shift at 600°C [101]. SiC JFET ICs have been shown to operate at 981°C, and survive 60 days in a Venus-like atmosphere by the same group [102, 103].

To the best of the authors knowledge, no attempts have been made to design or fabricate a SiC JFET with a monolithically integrated temperature sensor. Furthermore, the method of forming a lateral P-type resistor using the MOSFET P-body implant shown by Berthou et al. [95] could be applied to the JFET P+ gate implant. Integrating this sensing capability into a SiC JFET will enhance device functionality, and make JFETs an even more attractive option for high temperature applications.

To achieve this, the design of the monolithically integrated P-type resistor is investigated in detail using a first-principles model, and TCAD simulations. Specifically, electrothermal and transient simulations are employed to ensure that the sensor exhibits acceptable linearity, and does not cause significant cross-talk.

4.4 Fundamentals of Sensor Operation

The device structure of the proposed sensor design is shown in figure 4.1. Relevant dimensions used in simulation are shown on the figure. This design can be integrated into a SiC JFET without any further process steps, or mask layers. This is because the sensor can be formed concurrently with the main JFET gate junction, and even Floating Field Rings (FFRs) via ion implantation. Sidewall implantation has been included in the design to prevent any DIBL-induced failures as discussed in detail during chapter 3.

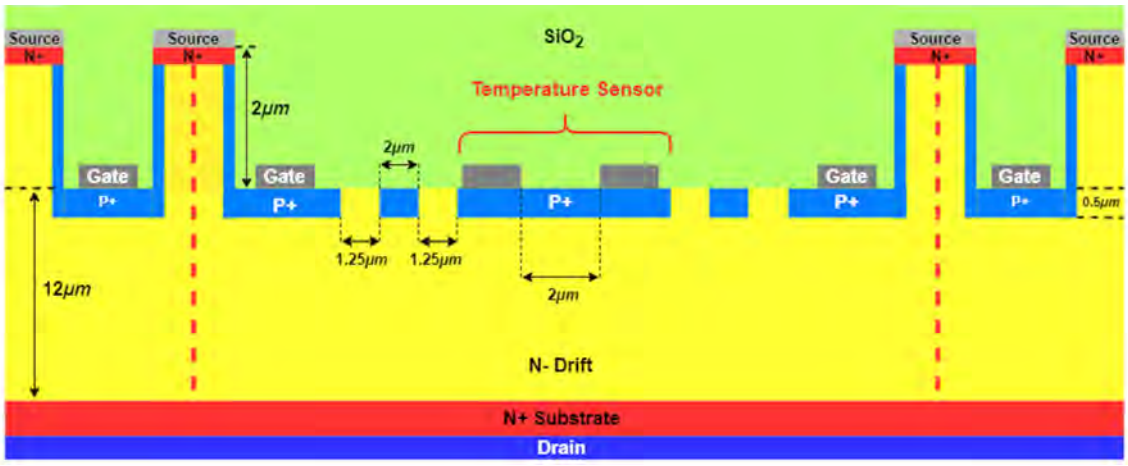


Fig. 4.1 Doping Profile of the proposed integrated temperature sensor utilising a P-type resistor. Active JFET unit cells are shown bordering the sensing element to show how the sensor may be integrated within a JFET stripe architecture. A FFR is also on included each side of the sensor. The area simulated in this work is indicated by the red dashed lines.

An example outline of the process flow which enables the JFET gate, FFR termination and sensor to be formed concurrently is shown in figure 4.2. Firstly, a blanket implantation of either nitrogen or phosphorous is completed to form the JFET N+ source region. Afterwards, an oxide hard-mask is deposited, and patterned to prepare for the JFET mesa etch. Post-mesa etch, another oxide mask is deposited and patterned to serve as the P+ implant mask. After JFET gate, sensor and termination are formed by the implant, an activation anneal is completed to activate the P-type aluminium (or boron) dopants. Next, the JFET gate and source contact metal, alongside the sensor contact metal are deposited and patterned by either

metal lift-off or an etch process. This metal is then subjected to a contact anneal to form an ohmic contact. Although not shown in the figure, at this point backside metallization and annealing would take place. An ILD is then deposited, and etched in the pad areas to open the pads, before a pad metal is deposited. If possible, a further dielectric layer should be deposited and etched away only in the pad areas to passivate the device.

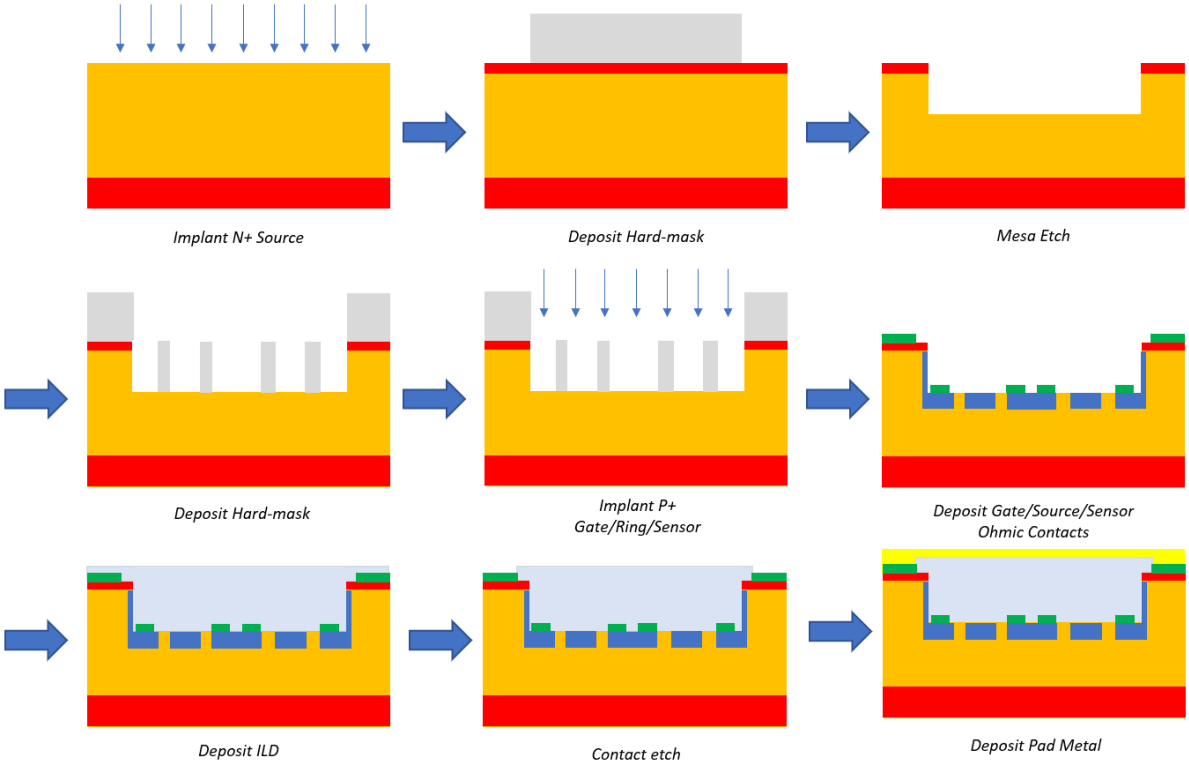


Fig. 4.2 Outline of the proposed process flow to form the JFET gate, FFR termination and sensor electrode simultaneously. The contact etch opening for the gate and sensor pads occurs in the third dimension, and as such is not shown. Additionally, the full edge termination which is also formed concurrently is not shown.

The lateral P-type resistor acts as a resistive sensor, where resistance varies with temperature. Due to the incomplete ionization effect, the number of active dopants increases with temperature, which causes resistance to vary. The resistivity of the P-type region is related to the number of ionized carriers (p) by the equation for resistivity ρ shown in equation 4.1, where μ_p is the hole mobility.

$$\rho = \frac{1}{q\mu_p p} \tag{4.1}$$

The sensor is operated by positively biasing to one of the sensor electrodes, whilst the other contact remains grounded. This is visualised in figure 4.3, where "S1" is the left hand

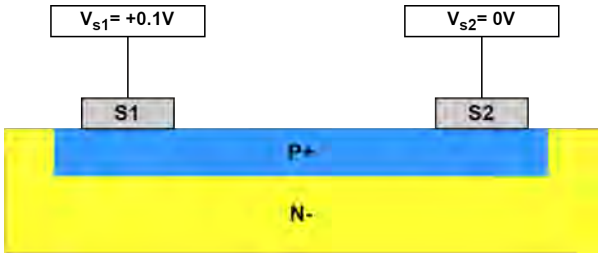


Fig. 4.3 Close up schematic of the integrated temperature sensor, indicating the bias which should be applied at each sensor contact.

contact pad, and "S2" is the right contact. This naming terminology is used throughout the remainder of this chapter.

Although +0.1V is a nominal positive voltage to cause the sensor to conduct current, this positive bias must not exceed the forward voltage drop of the vertical PN junction. If this occurs, current will be conducted vertically between the sensor contacts and the JFET drain contact. The forward voltage drop of a SiC PN junction has been experimentally measured as 2.6V [188]. Furthermore, the leakage current of 4H-SiC PN junctions has been measured on experimental devices as below 20nA in reverse bias [189], and therefore is negligible compared to the sensor current, and will not impact performance.

4.4.1 Incomplete Ionization

How incomplete ionization is modelled in Synopsys TCAD has already been discussed extensively in section 2.3 of chapter 2. For aluminium dopants used to achieve P-type in SiC, due to the large ionization energy of 265meV a significant proportion of aluminium dopants are not ionized at room temperature. The proportion of ionized carriers at a given temperature can be calculated by using equation 4.2.

$$p = \frac{N_a^-}{1 + g_a \frac{p}{N_v} \exp\left(\frac{E_{ion}}{kT}\right)} \tag{4.2}$$

Where g_a is the degeneracy of acceptors, which is equal to 4. Degeneracy is defined as the number of ways a state can be filled. For 4H-SiC, it is possible to create either a heavy-hole or a light hole in the valence band alongside the "spin up" and "spin down" possibilities for an electron to fill the acceptor state [138]. Therefore, there are four possible ways to fill a state in the valence band, thus $g_a = 4$. Conversely, the degeneracy of donors is equal to 2, as its only possible to fill a state in the conduction band with a "spin up" or "spin down" electron. The density of states of the valence band (N_v) is also temperature dependant, is

expressed in equation 4.3, where the hole effective mass is denoted as m_h, and is equal to 2.64 times the electron rest mass [146]. Finally, h is Plancks' constant.

$$N_v(T) = 2M_v\left(\frac{2\pi m_h kT}{h^2}\right)^{\frac{3}{2}} \tag{4.3}$$

Another effect which must be taken into account is that the ionization energy E_{ion} is reduced at high doping concentrations. Most commonly, the Pearson-Bardeen model is used [138]. This model is based on the average separation between acceptors ($N^{\frac{1}{3}}$). Equation (4.4) shows the Pearson-Bardeen model , where $E_{ion,0}$ is the initial ionization energy, ΔE_{ion} is the reduced ionization energy and α is an empirical fitting parameter, which is set to $3.6 \times 10^{-8} eV cm$ [141]. Recent work by Darmody and Goldsman [138] has proposed a different model to describe this effect, particular above $N_a = 10^{20} cm^{-3}$. However, as atypical JFET P+ gate region does not reach this concentration, the Pearson-Bardeen Model is used in this work.

$$\Delta E_{ion} = E_{ion,0} - \alpha N^{\frac{1}{3}} \tag{4.4}$$

Figure 4.4 shows the activation ratio ($\frac{p}{N_a}$) as calculated by analytical model using equations 4.2 - 4.4 as a function of temperature. Different doping concentrations have been modelled between $10^{17} cm^{-3}$ - $10^{19} cm^{-3}$, and $E_{ion,0}$ is 265meV.

As figure 4.4 shows, dopant activation rapidly increases from 200-500K, before beginning to saturate. For lighter doping concentrations, a larger percentage of dopants are active at all temperatures - at 300K 12% of dopants are active for N_a= $10^{17} cm^{-3}$, whilst only 4.2% for N_a= $10^{19} cm^{-3}$. This is exacerbated at higher temperatures, where at 600K N_a= $10^{17} cm^{-3}$ 88% of dopants are active, compared to 36.3% for N_a= $10^{19} cm^{-3}$. As the acceptor concentration increases, the Fermi level moves towards the valence band, which results in fewer dopants to become active [141]. Thus as N_a increases, neutral impurity concentration (i.e. un-activated P-type dopants) increases and activation ratio reduces.

At lower (≤300K) temperatures, less than 10% of aluminium dopants are active for all N_a values, even N_a= $10^{17} cm^{-3}$. This is due to the large initial ionization energy of Aluminium dopants as a consequence of the large bandgap of SiC. At 200K, the freeze-out regime is being approached.

4.4.2 Hole Mobility

Hole mobility within a P-type layer is dependant on scattering mechanisms in the bulk. The two dominant scattering mechanisms are phonon (also referred to as lattice) scattering and

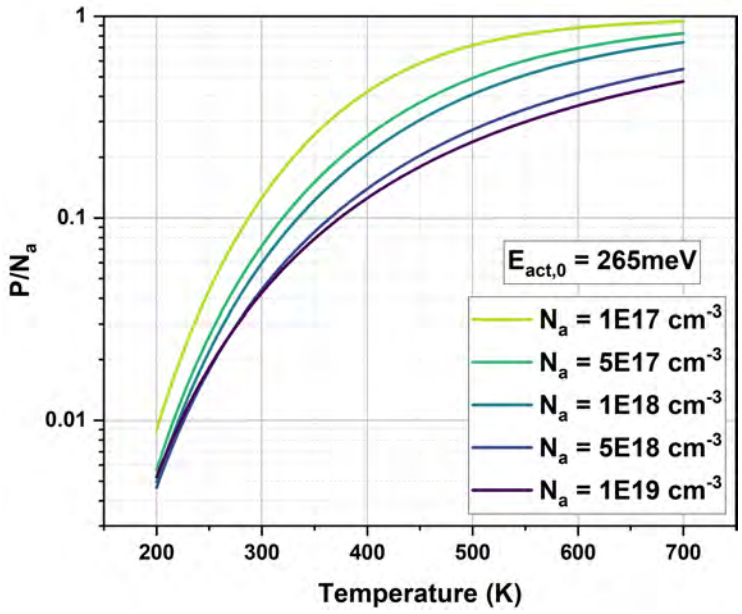


Fig. 4.4 Active doping concentration plotted as a function of temperature, for N_a values between $10^{17} cm^{-3}$ to $10^{19} cm^{-3}$. Active doping concentration increases with temperature, before beginning to saturate around 500K. This saturation effect is more significant in lower N_a values.

impurity scattering. Therefore, hole mobility μ_p is dependant on temperature and doping concentration. This is described by the Arora Model, as detailed in section 2.3 in Chapter 2.

$$\mu_{Arora} = \mu_{min}\left(\frac{T}{300}\right)^{\alpha_m} + \frac{\mu_d}{1+\left(\frac{N_{dop}}{N_{ref}}\right)^{A^*}} \tag{4.5}$$

Where:

$$\mu_d = \mu_{max}\left(\frac{T}{300}\right)^{\alpha_d} \tag{4.6}$$

$$N_{ref} = A_N\left(\frac{T}{300}\right)^{\alpha_N} \tag{4.7}$$

$$A^* = A_a\left(\frac{T}{300}\right)^{\alpha_a} \tag{4.8}$$

$$N_{dop} = N_d + N_a \tag{4.9}$$

Table 4.1 Arora model parameters for holes in the [0001] plane.

Parameter	Holes	unit
μ_{min}	0	cm^2/Vs
α_m	-0.57	1
μ_{max}	113.5	cm^2/Vs
α_d	-2.6	1
A_N	2.4×10^{18}	cm^{-3}
α_n	2.9	1
A_a	0.69	1
α_a	-0.2	1

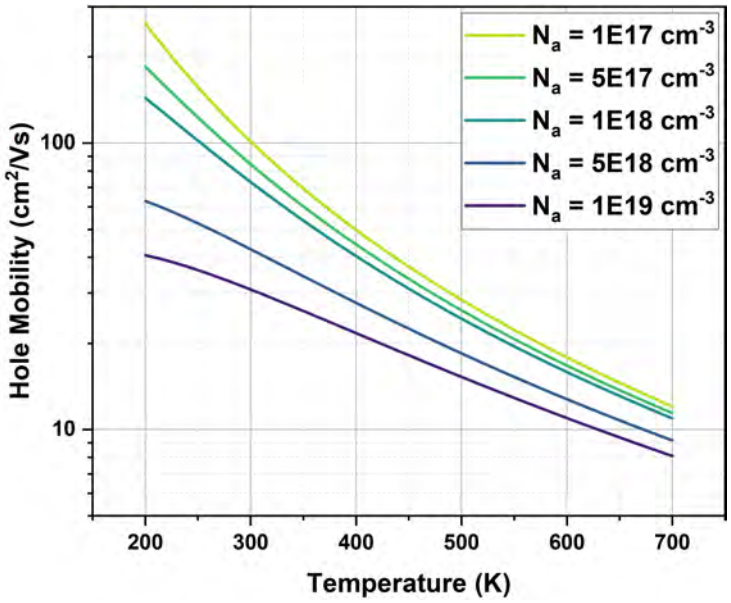


Fig. 4.5 Hole mobility plotted as a function of temperature, for N_a values between $10^{17}cm^{-3}$ to $10^{19}cm^{-3}$. Hole mobility reduces as temperature rises. This effect is more significant for lower N_a values.

Figure 4.5 plots the hole mobility as a function of temperature for the range of doping concentrations between $10^{17}cm^{-3}$ - $10^{19}cm^{-3}$. Lower N_a values result in a higher μ_p across all temperatures tested. At 300K, for $10^{17}cm^{-3}$ hole mobility is $101cm^2/Vs$ and for N_a= $10^{19}cm^{-3}$ hole mobility is $30.9cm^2/Vs$. As temperature increases, μ_p reduces significantly, especially for lightly doped regions such as N_a= $10^{17}cm^{-3}$. At 600K μ_p= $17.9cm^2/Vs$ for N_a= $10^{17}cm^{-3}$, which is a 82% reduction in hole mobility. Competitively, for N_a= $10^{19}cm^{-3}$ hole mobility only reduces by 64.7% to $10.9cm^2/Vs$.

At below room temperature, hole mobility increases significantly, especially for lightly doped regions. At 200K, μ_p= $262cm^2/Vs$, $185cm^2/Vs$ and $144cm^2/Vs$ for N_a= $10^{17}cm^{-3}$,

$5 \times 10^{17} cm^{-3}$ and $10^{18} cm^{-3}$, respectively. This increase is not observed for heavily doped layers - at 200K hole mobility only increases to $40.6 cm^2/Vs$ for N_a= $10^{19} cm^{-3}$, an increase of only $9.4 cm^2/Vs$ compared to room temperature.

4.4.3 Resistivity and Resistance

Combining the active doping concentration with the hole mobility allows calculation of the resistivity ρ of the P-type region using equation 4.1. Figure 4.6 plots the resistivity as a function for the same range of acceptor concentration between N_a= $10^{17} cm^{-3}$ - $10^{19} cm^{-3}$.

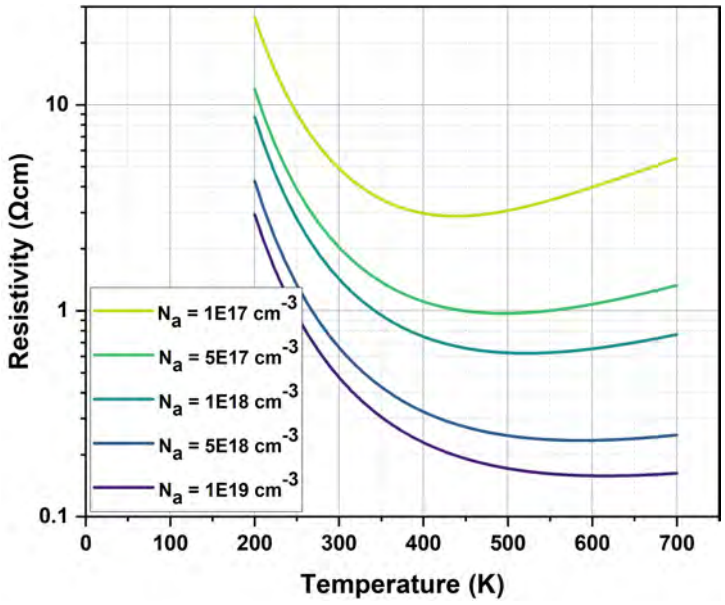


Fig. 4.6 P-type Resistivity plotted as a function of temperature, for N_a values between $10^{17} cm^{-3}$ to $10^{19} cm^{-3}$. Resistivity initially decreases, before saturating around 450K. For low values of N_a, the resistivity begins to increase above 450K, whilst for $N_a \geq 5 \times 10^{18} cm^{-3}$ the resistivity stays relatively constant.

As shown in figure 4.6, resistivity initially reduces with temperature. At 400 - 450K, resistivity begins to saturate for all N_a values and even begins to increase significantly for N_a= $10^{17} cm^{-3}$ - $10^{18} cm^{-3}$. For N_a= $10^{17} cm^{-3}$, at 400K ρ= $2.97 \Omega cm$ compared to $3.98 \Omega cm$ at 600K, which is a 34% increase in resistivity. This saturation and subsequent rise in ρ is attributed to the active acceptor concentration p saturating, whilst μ_p continues to decrease. This effect is less pronounced for high N_a values due to a combination of: less significant saturation of active acceptor concentration at 400-450K, and μ_p not decreasing as significantly with temperature.

The resistivity reduces for higher N_a values because of a larger active acceptor concentration p, even though the hole mobility is lower. At 300K, ρ= 4.9Ωcm for N_a= $10^{17} cm^{-3}$, compared to 0.47Ωcm for N_a= $10^{19} cm^{-3}$, which is order of magnitude lower. At the higher temperature of 600K, ρ= 3.98Ωcm for N_a= $10^{17} cm^{-3}$, and ρ= 0.16Ωcm for N_a= $10^{19} cm^{-3}$.

Overall, figure 4.6 shows that N_a values such as N_a= $10^{17} cm^{-3}$, are a poor choice to use as a temperature sensor, due to the saturation and subsequent increase in resistivity at high temperatures. Doping concentrations between N_a= $10^{17} cm^{-3}$ - $10^{18} cm^{-3}$ are found in a MOSFET P-body, which was used as a temperature sensor by Berthou et al. [95]. As higher doping concentrations ($10^{19} cm^{-3}$) are typically used for JFET P+ gate regions, thus this sensor type is more suitable for concurrent formation in JFETs rather than MOSFETs.

4.5 Comparing to TCAD

To ensure that drift-diffusion simulations agree with the first-principles model shown in the previous section, the sensor resistance was calculated using both methods and compared. In Synopsys TCAD, homogenous P-type doping 0.5μm thick was used, with N_a = $10^{18} cm^{-3}$, $5 \times 10^{18} cm^{-3}$ and $10^{19} cm^{-3}$. The lateral contacts were placed 2μm apart, with a contact width of 1μm. The length of the sensor in the Z direction is set at 1μm. Figure 4.7 shows the doping profile of the sensor in Synopsys TCAD.

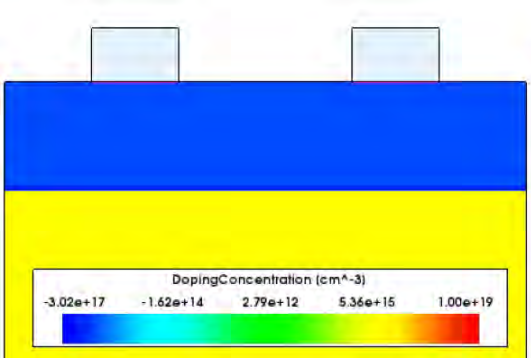
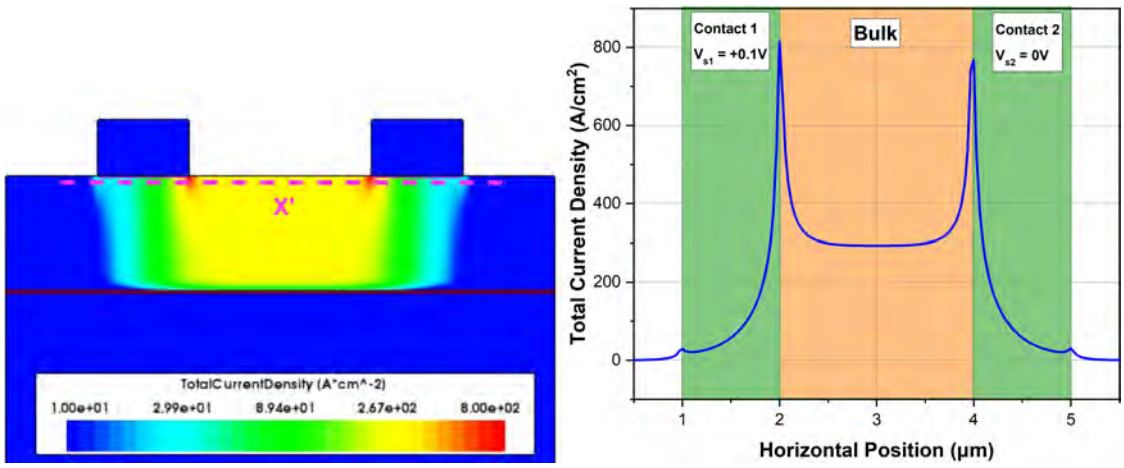


Fig. 4.7 Doping profile of the lateral P-type sensor that was used to verify in Synopsys TCAD simulations to validate and compare to the first principles resistance model.

To calculate the sensor resistance R_{sens} using the first principles model, the fundamental resistivity-resistance relationship shown in equation 4.10 is used, where L is the length of the region, and A is area of the region.

$$R_{sens} = \frac{\rho L}{A} \tag{4.10}$$

To calculate the effective length of the region conducting, current spreading vertically through the 0.5μm thick layer, and horizontally beneath the contacts must be considered. Figure 4.8a shows the total current density of the sensor with N_a= $10^{19}cm^{-3}$ at V_{s1}= +0.1V, with the position of the horizontal cut-line indicated. The magnitude of the current density along the cut-line is plotted in figure 4.8b.



(a) (b)

Fig. 4.8 (a) The 2D current density profile of the lateral P-type sensor at V_{s1}= 0.1V (b) Current density magnitude along the horizontal X' cut-line. Current density is highest at the inner edges of both contacts.

Figure 4.8a shows current is conducted throughout the whole thickness of the layer and is not localised to the surface, except near the contacts. Figure 4.8b illustrates current does spread slightly underneath both contacts. The current density at position in the centre of the first contact is 57Acm^2, compared to 139Acm^2 at 0.25μm from the right hand edge. Travelling towards the edge of the left hand contact, the current density increases rapidly before peaking at the contact edge at 814Acm^2. Current density between the contacts is 293Acm^2. Due the negligible current spreading further than 0.25μm from each of the contact edges, it is taken that the sensor length is 2.5μm.

The sensor resistance was extracted from drift-diffusion simulations at V_{s1}= +0.1V for all three values of N_a. The temperatures tested were 200-500K, in 50K steps. Figure 4.9 compares the resistance extracted from drift diffusion simulations to the first principles model.

The first principles model qualitatively agrees with the behaviour shown in drift-diffusion simulations, also showing R_{sens} saturating towards 500K, and beginning to increase as temperature approaches 700K for N_a= $1 \times 10^{18}cm^{-3}$. The analytical model is within 8.2% of R_{sens} values calculated by drift-diffusion at 200K, and 2.7% at 500K for N_a=$1 \times 10^{18}cm^{-3}$

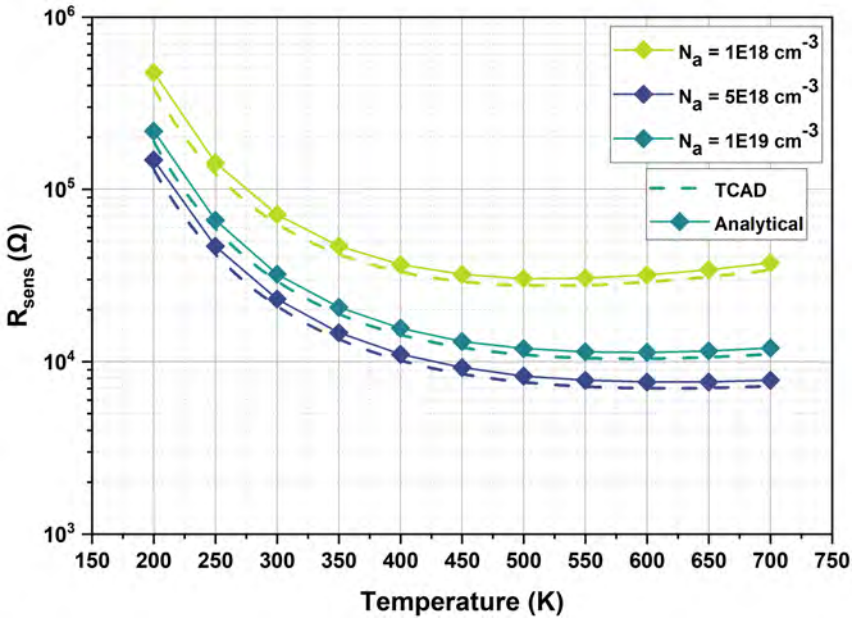


Fig. 4.9 Comparison between sensor resistance values obtained from drift-diffusion simulations and those calculated using the first-principles model. The resistance values from the first-principles model are within 10% of the drift-diffusion simulation results across all tested temperatures.

. When $N_a = 1 \times 10^{19} cm^{-3}$ the model shows a marginal improvement in predicting R_{sens} values to 0.6% at 200K, and 3.5% at 500K.

The discrepancy between the two models is attributed to two factors: firstly, the current spreading factor - although considered by using a 2.5μm sensor length as discussed previously, the current profile is not rectangular in drift-diffusion simulations. However, in the first principle models, it purely considers the resistance in a rectangular region. Therefore, there will be a slight discrepancy between the two. Secondly, the active acceptor concentration is marginally different due to the different models used in Synopsys and the first principles model. Although this discrepancy is within 5% at all temperatures tested, this will inevitably result in a slight difference in calculated R_{sens} values.

To further analyse the performance of the sensor over the 200-700K temperature range, the sensitivity was calculated for the N_a=$1 \times 10^{19} cm^{-3}$ design. Ideally, the sensitivity S of the sensor should be large enough to easily separate from the noise generated by the measurement circuit, but also relatively constant. A constant sensitivity indicates that the sensor exhibits linear behaviour. Equation 4.11 shows how sensitivity is calculated, which has been plotted for three different sensor lengths in figure 4.10: L_{sens}= 2μm, 5μm and 10μm. The I_{sens} value used to calculate sensitivity was 10μA.

$$S = \frac{\partial V}{\partial T} \tag{4.11}$$

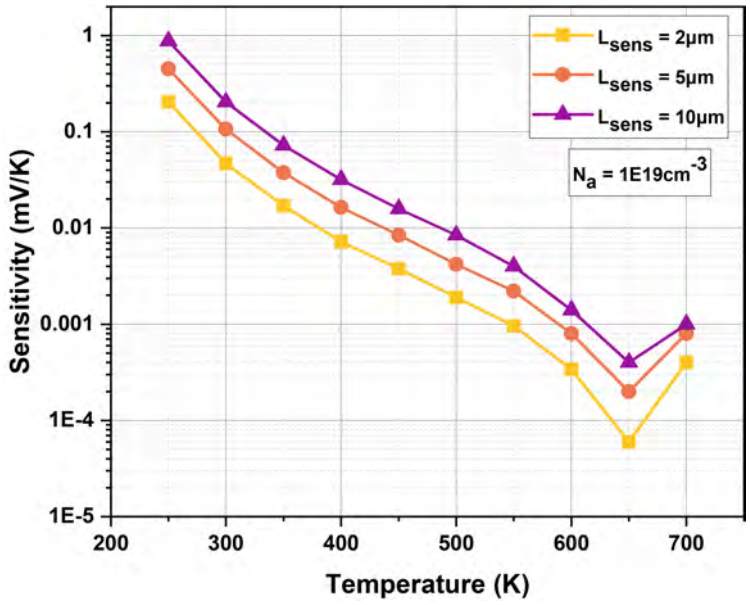


Fig. 4.10 Sensitivity of the N_a=$1 \times 10^{19} cm^{-3}$ design with different sensor lengths. Due to saturation of the incomplete ionization effect, S is close to 0 mV/K above 400K.

Due to the incomplete ionization effect saturating, S is below 0.01mV/K above 500K for all designs, as seen in the figure. On the other hand, the sensitivity below 400K is of a measurable magnitude, especially for the L_{sens}= 10μm design. This confirms that the optimum operating range for this sensor is between 200-400K. Sensitivity is also not constant throughout the temperature range, which agrees with figure 4.9 as R_{sens} does not decrease linearly with temperature. To improve S, sensor length could be further increased i.e. to 100μm which would enhance sensitivity values especially in the optimum 200-400K operating range.

4.5.1 Considering Contact Resistance

In practice, R_{sens} is the sum of three resistances - the resistance of the P-type bulk (R_{semi}) and the two contact resistances (R_c). Contact resistance is dependant on specific contact resistance (ρ_c) and contact area (A_c). Equation 4.12 shows the relationship between R_c, ρ_c and contact area A_c [190]. Specific contact resistance is a temperature dependant parameter, which is an effect which is not captured in TCAD simulations. The drift-diffusion results shown in figure 4.9 consider ideal contacts (i.e. $R_c = 0\Omega$), and therefore just calculate R_{semi}. To factor in the temperature dependence of R_c and to ensure this will not negatively affect the

sensor performance, R_c is calculated using experimentally found specific contact resistance values in existing literature.

$$R_c = \frac{\rho_c}{A_c} \tag{4.12}$$

Experimental studies have determined that ohmic contacts to highly doped P-type SiC are dominated by the Tunnelling Field Emission (TFE) transport mechanism [191]. Specific contact resistance has also been calculated in multiple works where $N_a \geq 1 \times 10^{19} cm^{-3}$ to be $\leq 1 \times 10^{-5} \Omega cm^2$ at 300K, and reduces as temperature increases [192, 193]. Typical metal stacks used to form ohmic contacts to P-type SiC include Ti-Al, Ti-Al-Ni and Al-Ti-Al, among others [194].

To capture a realistic R_c, experimental ρ_c values for Ni-Ti-Al contacts found by Yu et al. [192] between 275K and 475K have been used to calculate predicted R_c values for contacts with dimensions of 50μm by 100μm (A_c= $5 \times 10^{-5} cm^2$). The R_c values are compared to R_{semi} values for N_a= $1 \times 10^{19} cm^{-3}$ across the same temperature range calculated by drift-diffusion simulations in figure 4.11 for a contact spacing of 20μm. The values for ρ_c range from $2.4 \times 10^{-5} \Omega cm^2$ at 275K to $3 \times 10^{-6} \Omega cm^2$ at 475K. In drift-diffusion simulations, the sensor length in the Z direction is 100μm.

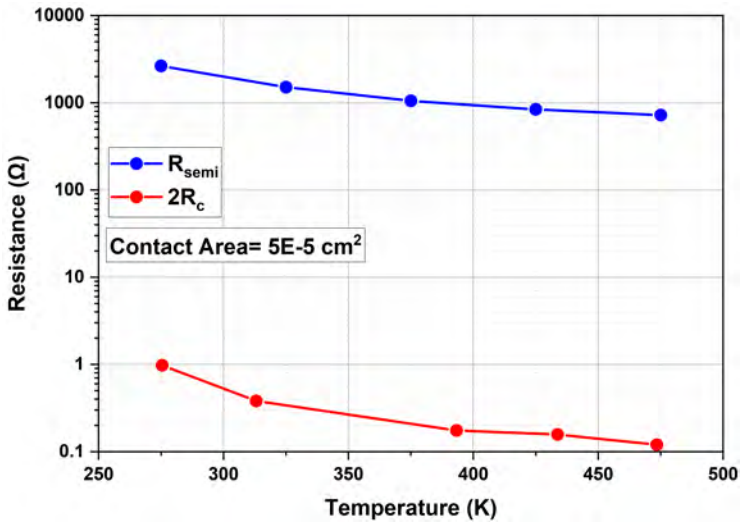


Fig. 4.11 Comparison between total contact resistance ($2R_c$) and R_{semi} between 275-475K, using experimentally extracted ρ_c values by Yu et al. Total contact resistance is less than 1% of the total resistance at all temperatures.

Both R_c and R_{semi} decrease as temperature rises. However, when R_c is largest at 275K it still remains at 1Ω. This is because of the excellent ρ_c of ohmic contacts formed a highly doped layer. Additionally, these contacts are relatively large, which reduces R_c. Conversely,

at 275K R_{semi}= 2.6kΩ, and reduces to 724Ω at 475K. Across the whole temperature range, the contribution of $2R_c$ is less than 1%. Therefore, R_c is negligible for this sensor design. This assumption would not hold if contacts were formed on a layer with lower N_a, as ρ_c will increase significantly. The contribution of contact resistance was found to be significant by Berthou et al. [95] in their sensor design due to the lower N_a value used.

4.6 On-State Behaviour

To assess the sensor temperature response under steady-state high current conditions, electrothermal simulations were employed. This enables the simulation of device self-heating (SH) using the Fourier heat equation. Neumann boundary conditions (i.e. ideal) were imposed on the left and right boundaries of the device. Dirichlet boundary conditions (i.e. thermal resistances) were imposed on the device backside, and on top of the dielectric layer. The thermal resistance (R_{th}) applied to device topside is much larger ($1.2cm^2W/K$) than at the back where R_{th}= $0.225cm^2W/K$. These values were chosen to emulate a realistic device package, in which the back of the die is bonded to a heatsink, causing the majority of heat to dissipate through the bottom surface.

For the remainder of this work, the area shown in figure 4.1 is used. Opposed to the previous section, inhomogeneous Monte-Carlo implantation is used to form the P-type regions in the device. Figure 4.12 compares the output (J_d-V_d) characteristics calculated for electrothermal simulations to isothermal simulations at 300K and 450K, for V_g= 0V and -1V.

When V_g= 0V, initially the electrothermal curve mimics the gradient of the 300K result in the linear region. At V_d= 1V, the 300K curve demonstrates a J_d of 102A/cm^2, compared to 90.1A/cm^2 for the SH result. In the SH result, power dissipation increases as V_d grows, which causes T_j to rise. This results in the SH curve to have a much more clearly defined saturation region than either of the isothermal results. The role of increasing T_j in the SH result is evident as there is an increasing disparity between the 300K and the SH curves. As V_d approaches 5V, T_j in the SH result nears 450K. This causes the SH curve to exhibit a similar J_d to the fixed 450K curve. At V_d= 4V, J_d= 153A/cm^2 and 134A/cm^2 for the SH and 450K results, respectively.

As negative gate bias constricts the channel region, J_d is reduced for both fixed temperature and SH results when V_g= -1V. As a consequence of lower current density, the JFET does not experience the same level of self-heating in the electrothermal simulation when V_d= -1V. This is illustrated by the 450K and SH curves not displaying similar J_d values at V_d= 5V, unlike the V_g= 0V curves.

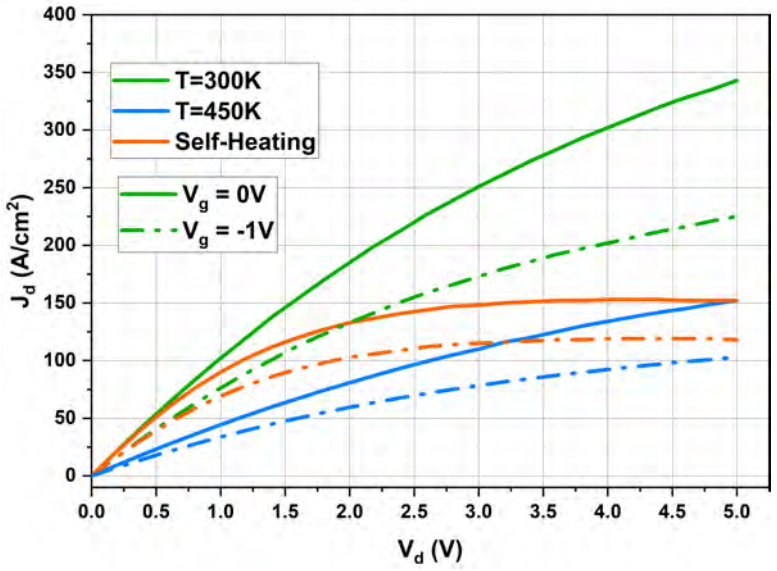


Fig. 4.12 Comparison between JFET output characteristics considering device self-heating, and at fixed temperatures of 300K and 450K for V_g= 0V, -1V. Device self-heating at high power results in a more distinct saturation region.

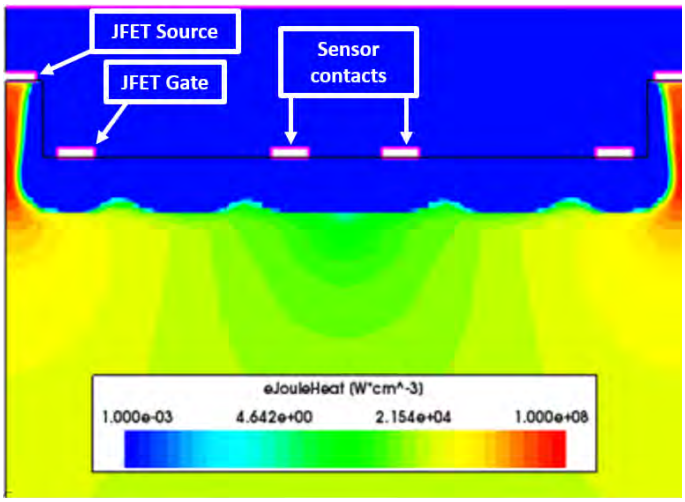


Fig. 4.13 Electron joule heat profile of the JFET at V_d= 5V, V_g= 0V under self-heating conditions. The areas of highest heat generation are the JFET channel regions.

The area of highest current density is the JFET channels, because of how narrow these regions are. Thus, the majority of localised heating should occur in the JFET channels. This is verified by the electron joule heat plot shown in figure 4.13, where the highest levels heating do occur throughout and below both JFET channel regions within the device.

The lattice temperature of the device is plotted in figure 4.14, which shows that the hottest areas within the structure at V_g= 0V, V_d= 5V are the JFET channels. More importantly, the

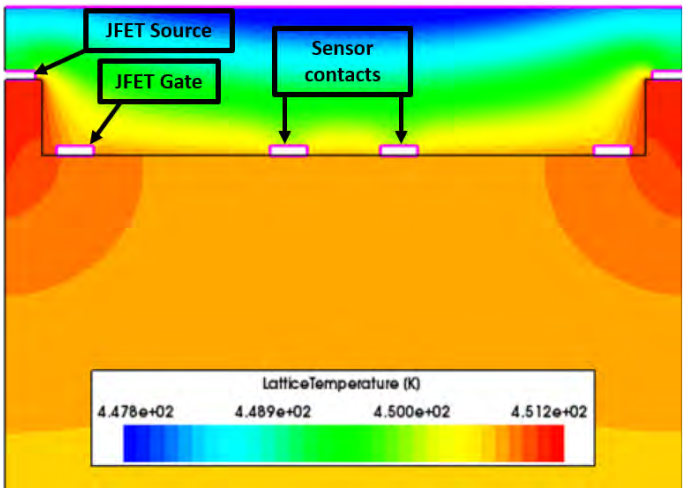


Fig. 4.14 Temperature profile of the JFET at V_d= 5V, V_g= 0V under self-heating conditions. The highest temperature is located in the JFET channels, which agrees with the electron joule heat profile. The lattice temperature of the sensor is within 1K of the JFET channels.

lattice temperature of the sensor in the centre of the device is within 1K of the JFET channels, verifying that the temperature sensor location enables accurate monitoring of T_j.

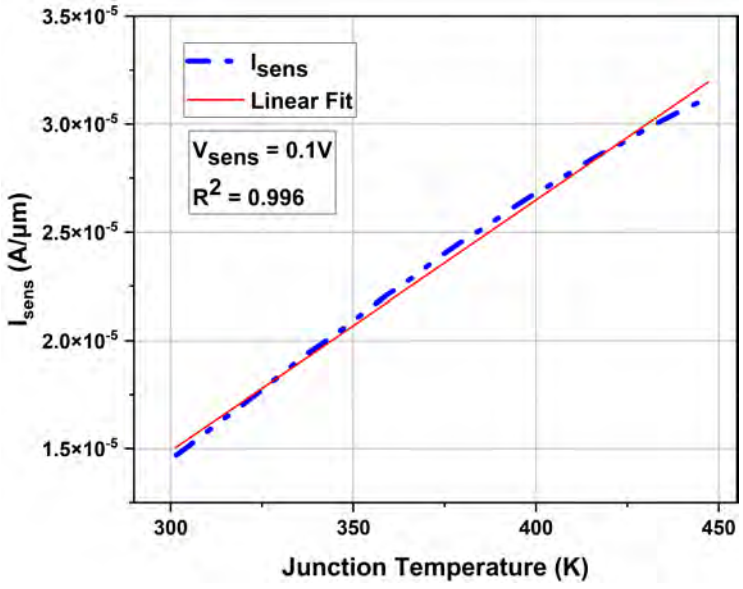


Fig. 4.15 Sensor current plotted against T_j for V_g= 0V for the device self-heating simulation, with a linear fit superimposed. The sensor current is highly linear with R^2=0.996.

Figure 4.15 shows the sensor current I_{sens} plotted as a function of T_j. Excellent linearity was observed between 300-450K with an R^2 of 0.996, although saturation of I_{sens} appears to begin near 450K. Table 4.2 compares this sensor design to other reported SiC devices with

integrated temperature sensors. The calculated R^2 value closely aligns with the experimental R^2 value of the MOSFET P-body sensor reported by Berthou et al. [95].

Table 4.2 Comparison of different reported 4H-SiC monolithically integrated temperature sensors. L-res denotes a lateral resistor based on incomplete ionization, whilst Res denotes a Tungsten Disilicide sensing resistor.

Parameter	This Work	[95]	[184]	[94]
Device Type	JFET	MOSFET	MOSFET	MOSFET
Sensor Type	L-Res	L-Res	Res	SBD
Range (°C)	25-150	25-175	25-125	15-200
R^2 (%)	99.6	99.7	>90	99.9

The integrated SBD demonstrated by Chen et al [94] does offer a higher R^2 over a larger temperature range. Diode-type temperature sensors offer improved linearity, but require additional processing and dedicated mask layers to form. This is because the sensors must be electrically isolated from the drain electrode of the main device by a PN junction. For example, the lateral SBD used by Chen et al. requires a further implantation step to create the lightly doped N-type region to form the SBD Schottky contact. Therefore, resistor type sensors are attractive as they offer frictionless process integration with the main device, whilst offering acceptable linearity over the temperature range tested.

4.7 Transient Behaviour

Alongside on-state behaviour, it must be verified that the temperature sensor is insensitive to high voltage or current transients which can be experienced during switching events. A key example of this specifically concerning the TBU is when over-current or voltage is detected, and the JFET is switched off. An isothermal simulation of a JFET turn-off event has been completed.

Figure 4.16 shows the equivalent circuit diagram of this transient simulation. A 100MΩ resistor has been connected in series with the drain, whilst the left hand sensor contact is connected in series with a 10kΩ resistor. The same sensor contact is biased at +0.1V, whilst the other sensor contact is grounded. The voltage source (V_{drain}) connected to the drain resistor is biased at 400V. A 1Ω gate resistor has also been used. For this section, the length of simulated cell (JFET and sensor) is equal to 1cm.

The JFET gate was initially held at 0V for 0.5μs, before a linear ramp to -20V in 1μs. The gate was then held at -20V for -0.5μs to enable the sensor current to settle. The total simulated time was 2μs. The waveform of the JFET gate and voltage at the contacts are

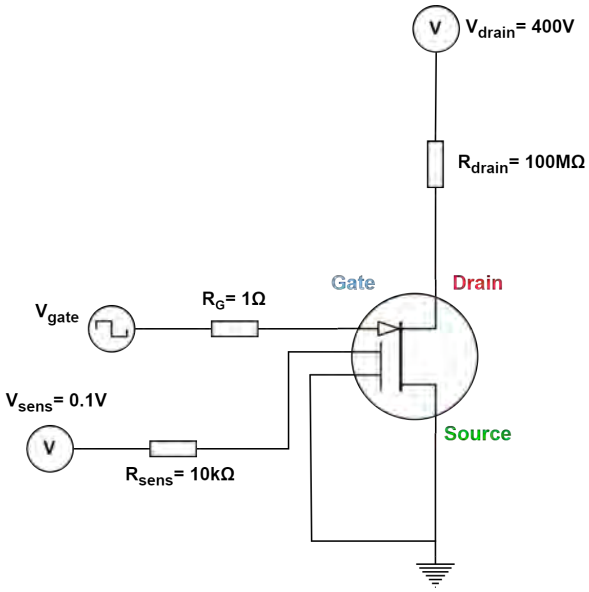
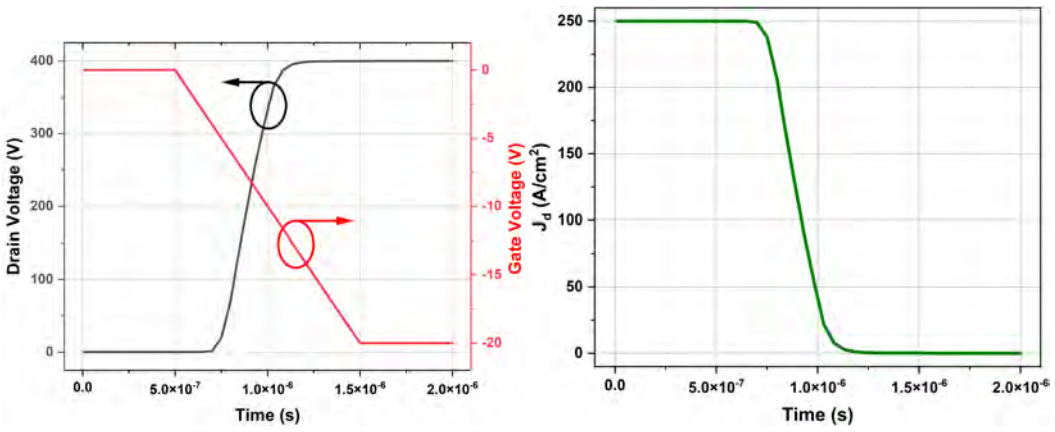


Fig. 4.16 Equivalent circuit which is used in transient simulation of the JFET with an integrated sensor. The gate voltage is modelled as a square wave, with a 1μs rise time.

plotted in figure 4.17a. Voltage at the drain contact increases from 0.15V in the JFET on-state to 400V in the off-state. Figure 4.17b shows the JFET drain current during the turn-off event. The drain current density J_d reduces from 250A/cm^2 to 0.002A/cm^2, indicating that the JFET has completely turned off.



(a) (b)

Fig. 4.17 (a) Gate and drain voltage and (b) drain current density during JFET turn-off.

To calculate the turn-off loss of the JFET, firstly the instantaneous power was calculated using the I_{ds} and V_{ds} data. Figure 4.18 plots the instantaneous power as a function of time during the simulation. Peak instantaneous power was 3.99W at t=0.88μs. By integrating

the area underneath this curve, the turn-off energy loss of the JFET was calculated as 0.9μJ. This energy is relatively low due to three factors: firstly and most importantly this is an isothermal simulation, and as such is approximate and underestimates energy losses (as energy is normally lost as heat during switching). Other effects which contribute to the energy losses are the low density of JFET channels which reduces the magnitude of I_{ds}, and the V_{drain} value of 400V.

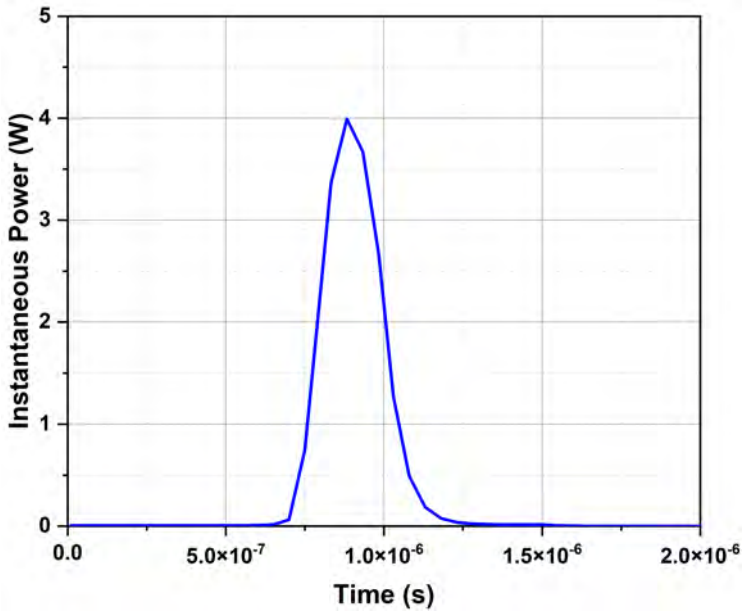


Fig. 4.18 Instantaneous power during the JFET turn-off simulation. Maximum power was 3.99W at 0.88μs.

During the turn-off event, both sensor contacts experience a negative current spike at between 0.8-0.9μs, as seen in figure 4.19. This spike occurs at the point of maximum instantaneous power, as shown in figure 4.18. The grounded sensor contact has a more pronounced spike of 2.74% compared to the other contact at +0.1V, which experiences a spike of 0.14%. It is concluded that this spike is due to displacement current in the space charge of the P-type region, which agrees with the findings of Berthou et al.

Once the spike has dissipated, both contacts exhibit a shift in sensor current towards 0A/μm. This shift is less than a 0.1% reduction in I_{sens} for both contacts. Nevertheless, this shift is attributed to an increase in depletion within the P-type resistor as the junction is now in reverse bias at 400V. The shift is negligible due to the high doping concentration in the P-type resistor which is used, which results in a minimal change in depletion width. Consequentially, if the P-type doping was lower such as used by Berthou et al. , the disparity between sensor current in the device on and off-state will be larger. It should be noted that during JFET turn-on, it would be expected that both the spike and the shift in sensor current

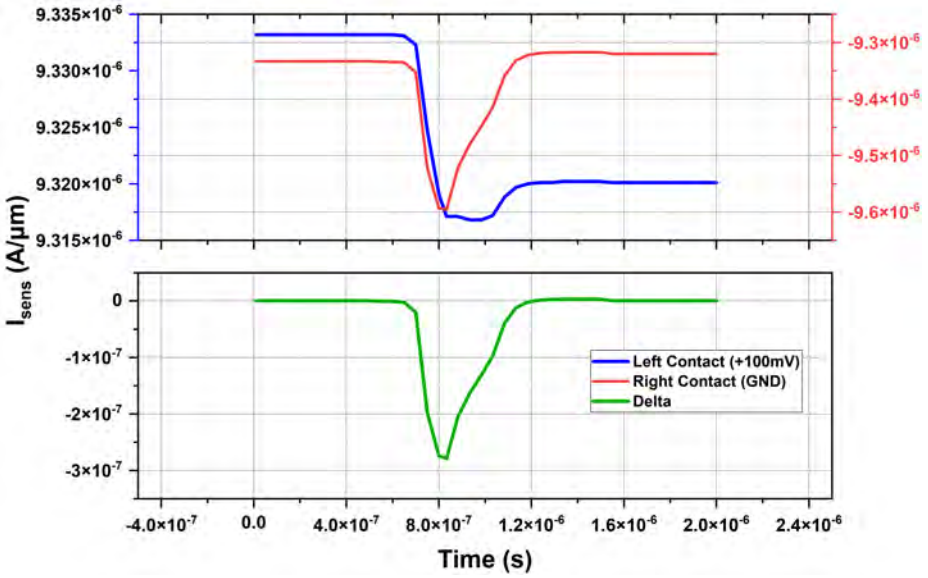


Fig. 4.19 Current simulated at both sensor contacts during the JFET turn-off. The discrepancy between the current at each contact is plotted as "Delta". A negative spike in current is measured at both sensor contacts during the switching event.

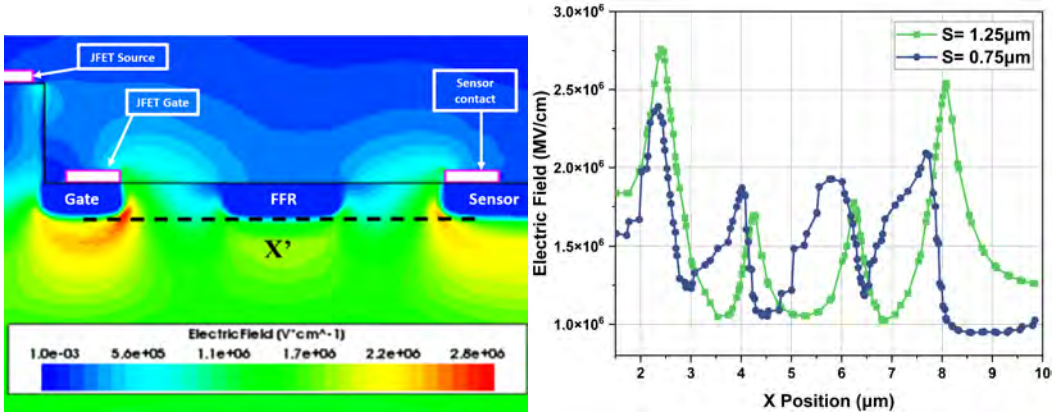
would be reversed i.e. the spike would be positive, and the shift in I_{sens} would be away from 0A/μm.

4.8 Off-State

The robustness of the JFET in the off-state must not be inhibited by the introduction of the sensing resistor. Furthermore, the sensor current should also remain stable under reverse bias. If the sensor current (I_{sens}) fluctuates significantly with drain bias, extensive calibration of the sensor would be required in the device off-state alongside the on-state. Additionally, cross-talk between the JFET and sensor must be minimized. If current flows between them, the JFET off-state leakage will be elevated which must be avoided.

When the JFET is in the on-state, the sensor is electrically isolated from the device by the PN junction. In the off-state, the JFET gate is held at -20V to ensure the device completely turns off, as shown in the transient section. For successful implementation of the sensor, JFET breakdown voltage should remain the same as a JFET without the temperature sensor. A

The spacing between the three adjacent junctions: JFET gate, FFR and sensor remain equal. This spacing S is then varied between 0.5μm - 1.25μm. Breakdown voltage is highly sensitive to the spacing between the main junction and adjacent FFRs, as has been discussed



(a) (b)

Fig. 4.20 (a) Electric field profile of the gate, FFR and left hand side of the sensor contact for $S = 1.25\mu$m at the point of breakdown, showing the position of cut-line X' (b) Electric field magnitude along cut-line X' for $S = 0.75$ and 1.25μm. The larger spacing results in a larger peak electric field at the gate and sensor junctions, indicating the spacing is unoptimised.

extensively in chapter 3. Figure 4.20a shows the electric field profile of the gate,FFR and sensor junctions when S= 1.25μm at the point of breakdown. The corresponding electric field magnitude shown in figure 4.20b illustrates that S=0.75μm shares the field almost equally between the three junctions, indicating near optimum placement. Conversely, S= 1.25μm shows peaks in electric field at both the sensor and gate junctions, indicating that this spacing is too large.

The breakdown voltages have been extracted for each spacing, and are plotted in figure 4.21. Avalanche breakdown is judged to have occurred when drain current is greater than 2.5×10^{-8}A/μm. Comparatively, BV remains above 1400V for $S \leq 0.75\mu$m, which is 94.5% of the simulated BV without the sensing element. This excellent blocking performance quickly degrades at larger S values, with BV reducing to 1225V and 1134V for $S = 1.15\mu$m and 1.25μm, respectively.

Figure 4.21 also plots the reduction in sensor current between V_d= 0V and V_d= 1000V denoted as ΔI_{sens}. At smaller spacings ΔI_{sens} is extremely large, especially at $S = 0.5\mu$m where ΔI_{sens} is equal to 42.3%. As S increases, ΔI_{sens} drastically reduces to 12.4% for 0.75μm, before saturating at near 4% for $S \geq 0.95\mu$m. The 4% change in I_{sens} is attributed to the same p-type depletion effect as discussed for transient operation, but at higher reverse bias (400V in the transient work compared to 1000V here).Therefore, although spacings of 0.5μm and 0.75μm result in the best breakdown performance, they are not suitable due to their high ΔI_{sens} values.

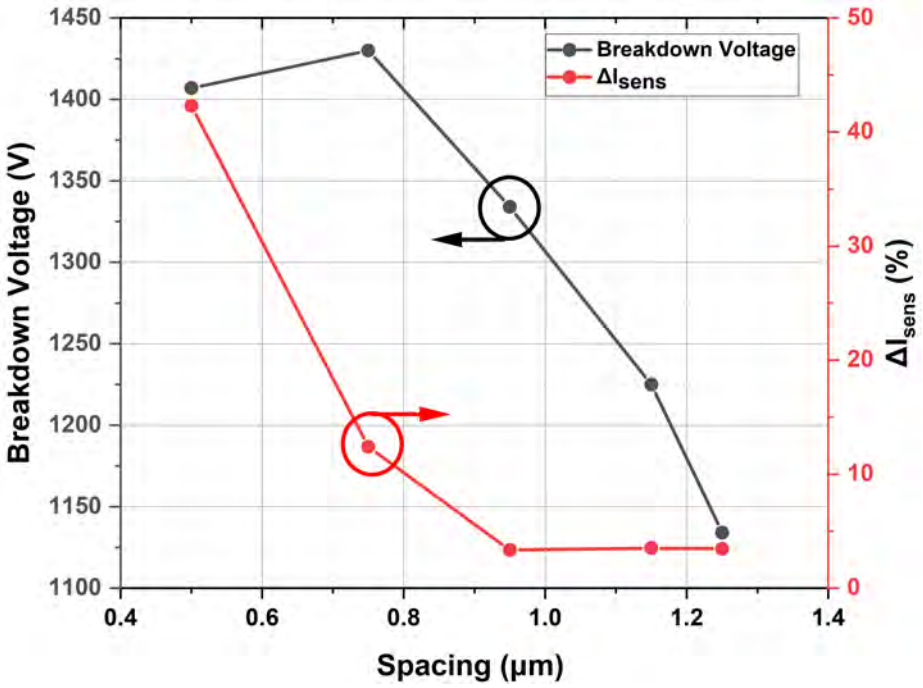
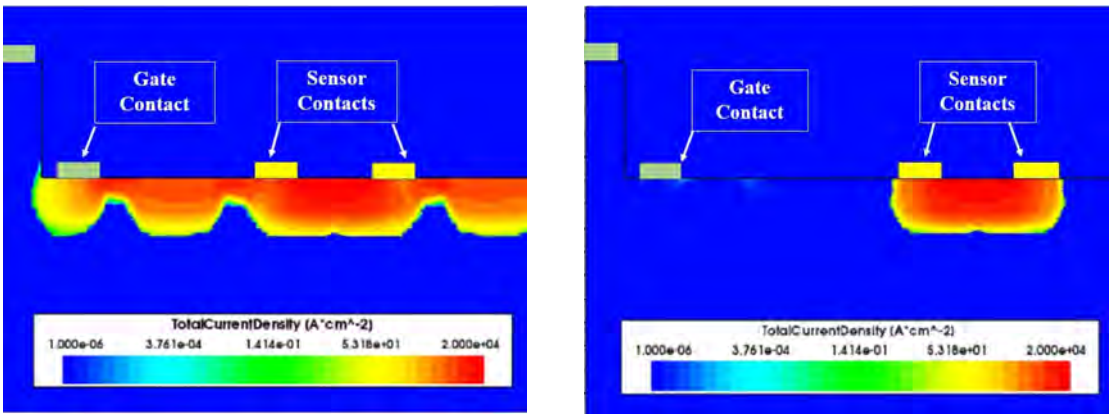


Fig. 4.21 Breakdown voltage and the reduction in I_{sens} between V_d= 0V and 1000V (ΔI_{sens}) are plotted as a function of S between $S = 0.5\mu$m and $S = 1.25\mu$m. Breakdown voltage and ΔI_{sens} reduce as S increases.

To further investigate the reason behind increased interaction between the sensor and JFET when S is small, 2-dimensional current density plots for S= 0.5μm and 1.25μm at V_d= 100V were studied. These plots are displayed in figure 4.22a and 4.22b, respectively.



(a) (b)

Fig. 4.22 Total current density at V_g= -20V, V_d = 100V for (a) S= 0.5μm, showing significant current flow between the gate and sensor junctions and (b) $S = 1.25\mu$m with far little to no current flow.

Upon studying 4.22a, it is clear that the high ΔI_{sens} for S= 0.5μm is due to current flow between the gate and sensor via the FFR. This is due to the close proximity of the junctions. As the gate is being held at -20V, and the left hand sensor contact at +0.1V, a significant hole current flows into the gate from the sensor. The divergence of holes from the sensor to the gate contact causes I_{sens} to reduce. Equally, this causes gate current to increase with applied V_d.

When spacing between the junctions is increased, the divergent hole current is significantly reduced as the electrostatic potential of the gate does not encroach the area near to the sensor contact. This is verified by figure 4.22b, which shows that no current path has been established between the junctions.

Overall, when taking breakdown performance and ΔI_{sens} into account, S= 0.95μm is the optimum spacing between junctions which results in a breakdown voltage of 1334V and ΔI_{sens}= 3.4%. It should be noted, that as with the FFR optimisation in chapter 3, due to the sensitivity of breakdown voltage and ΔI_{sens} to S, lateral straggling of implanted ions must be taken into account. One promising idea would be to introduce further FFRs with incremental spacing as shown in chapter 3, which would provide acceptable JFET breakdown voltage whilst increasing the spacing between adjacent junctions.

4.9 Conclusion

A novel device structure has been proposed to integrate a temperature sensor with a SiC JFET via a lateral resistor formed on a P+ region. This region can be formed concurrently with the main JFET gate junction and even FFR termination structures. This sensor displays a high degree of linearity between 300-450K (R^2= 0.996) and remains stable in the device off-state, with ≤4% variation in I_{sens}. It is also not prone to current spikes during transient events, such as when over-current/voltage is detected. The JFET breakdown voltage is marginally reduced to from 1473V to 1334V by implementing the sensor, however it is possible that with further optimisation of the FFR structures, this could be improved.

The first principles model developed to predict device behaviour illustrated that the resistivity ρ of the lateral resistor is governed by two effects: incomplete ionization, and hole mobility. As temperature increases, p increases and μ_p reduces. This results in ρ and thus sensor resistance R_{sens} reducing. At above 450K, the incomplete ionization effect begins to saturate, and thus p saturates. As hole mobility continues to decrease with temperature, ρ begins to increase again. This increase in ρ is more prevalent for lightly doped P-type regions opposed to the P+ gate region of the JFET. Therefore, highly doped P-type regions are preferable over lightly doped regions for this sensor type.

Finally, care must be taken when choosing the placement of the sensor with respect to adjacent FFRs and JFET gate junctions. If these junctions are located too close to the temperature sensor, the sensor experiences a large variation in I_{sens} in the JFET off-state, due to a current path being established laterally between the junctions. In practice, a balance must be struck between JFET off-state performance and ΔI_{sens}. Introduction of further FFRs such as the 12 ring design optimised in chapter 3 could be used to increase the spacing between adjacent junctions whilst achieving good breakdown performance.

Chapter 5

Correlating Material Defects with Unipolar Device performance

5.1 Preface

This chapter discusses material defects which are prevalent in SiC substrates and epitaxial layers, and how these defects could affect the performance of unipolar devices, such as JFETs or Schottky diodes. The work presented in this chapter comprises of two 150mm SiC wafers which were defect mapped using a Lasertec SICA tool. Nickel Schottky barrier diodes were subsequentially fabricated across the whole of both wafers, which were then tested electrically in forward and reverse bias to assess if any correlation between defects and device characteristics was observed. This includes analysis of diode forward voltage (V_f), Schottky barrier height (ϕ_b) and breakdown voltage (V_{br}).

5.2 A Review of Material Defects in 4H-SiC

Defects is a general term used to describe a range of crystallographic or morphological imperfections in a semiconductor layer. These can be propagated into an epitaxial layer from the substrate, or can be generated during epitaxial growth, and can be located at the wafer surface or buried within the epi-layer.

Different types of defects exist, such as Point Defects, basal plane dislocations (BPDs), Stacking Faults (SFs), Polytype and Carbon Inclusions, Micropipes and Carrots to name a few [195]. Each type of defect has its own cause, and effect on devices fabricated on the material. Electrically, defects can cause issues ranging from an reduction in carrier lifetime (important for bipolar devices) to a device killer. An overview of the different types of defects

in SiC, and where they occur in the wafer growth process is shown below in figure 5.1 [196]. The figure also indicates how these defects can propagate through different stages of the process i.e. from the substrate to the epi-layer.

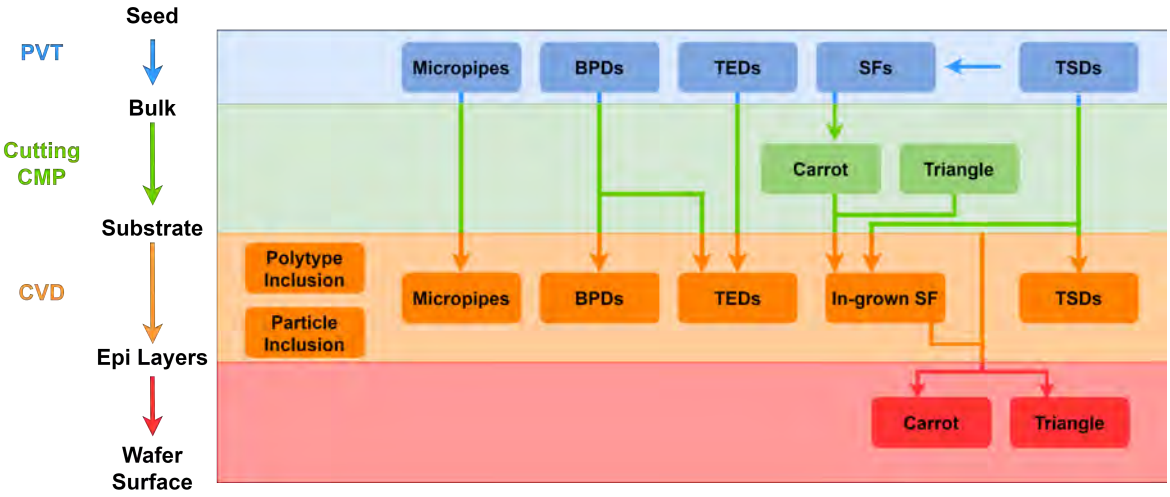


Fig. 5.1 Schematic of which step of SiC wafer manufacturing different material defects originate from. Arrows indicate how defects can propagate in subsequent manufacturing processes.

Crystallographic defects and contaminations during the epi-layer growth process may result in extended defects which reach the wafer surface [197], which can be detrimental to the performance of fabricated devices. An example of a crystallographic defect is a Basal Plane Dislocation (BPD). BPDs have a Burgers vector of $\mathbf{a}(< 11\bar{2}0 >/3)$, which describes a slip in the adjoining crystal planes contained within the lattice. This slip causes either an extra half plane to be formed, or a missing half plane. Threading Edge Dislocations (TEDs) have the same Burgers vector as BPDs: $\mathbf{a}(< 11\bar{2}0 >/3)$ [198]. Neither of these defects cause a fault in the stacking sequence of the lattice. The difference between BPDs and TEDs is purely dislocation direction. The same effect in the $< 1\bar{1}00 >$ plane is known as a Shockley Stacking Fault (SSF), however a slip occurring in this plane causes a fault in the stacking sequence [199]. SSFs have been demonstrated to cause significant bipolar degradation [200]. Threading Screw Dislocations (TSDs) occur when a stacking fault (SF) spans four Si-C bilayers [198]. Most dislocations in epitaxial layers originate from the substrate, and propagate through subsequentially grown material [198].

Common larger extended defects (also referred to as "morphological defects") are polytype inclusions, a Stacking Fault complex (referred to as a "carrot") and micropipes. A micropipe defect is a hollow core - essentially a hole in the substrate or epitaxial layer. This occurs due to a super screw dislocation in the crystal. Devices fabricated on top of a

micropipe will very likely not operate, or exhibit excessive leakage current and premature breakdown [201]. Micropipes are the most important of the "killer" macroscopic defects, and have now been reduced to a satisfactory $\leq 0.1cm^{-2}$ on commercial 4H-SiC wafers [198].

Carrot defects consist of two intersecting stacking faults, and can nucleate from a TSD [202]. Polytype inclusions can form as defects due to unoptimised growth conditions for an epilayer - the most likely polytype accidentally grown is 3C-SiC during 4H-SiC layer growth [203]. Triangular defects occur when a thick layer of inadvertently included 3C-SiC is sandwiched between two layers of 4H-SiC [204]. Finally, carbon inclusions occur due to instability in growth conditions, which results in the formation of graphite particles or silicon droplets. Inclusion of foreign material can also result in nucleation of TSDs or even micropipes [205]. Morphological defects have been associated with elevated reverse leakage [206, 207], destructive breakdown of devices [207].

When fabricating the SiC JFETs designed during this project, it is highly likely that some devices will be fabricated on areas of epitaxial wafers which contain defects. Thus, it is important to understand, and quantify how material defects such as the ones described above can effect unipolar device operation. If defects are found to significantly degrade device performance, this presents a serious issue for manufacture of 4H-SiC JFETs at a large scale across entire wafers.

Therefore, this work attempts to correlate the location of mapped defects to unipolar device characteristics at a wafer scale. To minimise the number of introduced variables, Schottky Barrier Diodes (SBDs) were selected as the unipolar devices to be fabricated instead of JFETs, as their fabrication does not strictly require ion implantation. Adding implants to the fabrication precess would introduce more variability to the study, as further defects could be introduced during ion implantation process [208], making it more challenging to correlate defect maps with device performance. Furthermore, defects including BPDs, TSDs and TED have been found to increase reverse leakage current in SBDs [209–211]. Fujiwara et al. reported that Stacking Faults lower ϕ_b, and decrease V_{br} [212].

5.2.1 Defect Detection Methods

To detect the various different types of defects that occur in 4H-SiC, an array of analysis techniques are used. For defects that occur on the wafer surface such as carrots, polytype inclusions and scratches, optical microscopy is commonly used. For crystallographic defects that occur deeper into the wafer e.g. SFs, TSDs, BPDs and micropipes, photoluminescense (PL) or X-ray Topography (XRT) are employed.

Optical microscopy detects defects by illuminating the wafer surface with light, and capturing the light that is scattered by defects. A key benefit of optical microscopy is its high

lateral resolution, which enables the detection of small carrots & micropipes, but has also been used to study polytype inclusions, surface pits and step-bunching [213].

To investigate defects found below the wafer surface, XRT has been proven to be very effective. The x-ray topography technique directs a beam of x-rays incident to the surface, which are either absorbed or diffracted through the wafer. To detect the diffracted x-rays, either a detector or a photographic plate are used. If defects are present, the spacing in the lattice will be uneven or the crystal plane will vary locally. A pure sample will result in several sharp, well defined peaks on the spectrum whilst a defective sample will have broader peaks. Skowronski et al. have demonstrated detection of BPDs and TEDs under current stress tests using XRT [214].

Photoluminescence involves exciting the sample with an a laser, which generates electron-hole pairs within the semiconductor. The carrier pairs then recombine via various mechanisms, including radiative recombination which releases a photon as a by-product. Depending on the wavelength of exciting laser, different defects will generate more electron-hole pairs, and thus cause the sample to emit more photons. This results in specific peaks in the spectra which can be attributed to specific types of defects.

Overall, commercially available defect detection tools such as the Lasertec SICA which has been used in this chapter combine multiple methods to ensure a minimum amount of defects are missed during inspection. For example, an optical microscope is used to scan the surface, and a PL scan is repeated across the same area to capture crystallographic defects. The results of the different techniques are then compared, and depending on the outcome the defect is classified e.g. if only the optical microscope detects a signal, it may be a scratch. If both scans detect the same defect, that indicates it is a crystallographic defect near the surface e.g. a carrot. If the defect is only detected on the PL scan, it is categorised as a BPD or SF depending on the shape observed on the scan.

5.3 Methodology

5.3.1 Mapping SiC Wafers for Defects

To attempt to correlate the device data with the location of material defects, two 150mm SiC epitaxial wafers from Aixtron were used. The epitaxial structure of these wafers is shown in figure 5.2. The substrate thickness was 350μm, with a 1μm buffer layer with a doping concentration of N_d= $10^{18} cm^{-3}$, and a 11μm thick N-drift layer with N_d= $6.5 \times 10^{15} cm^{-3}$. From this point onward, the two wafers are referred to as wafer 1 (WAF1) and wafer 2 (WAF2).

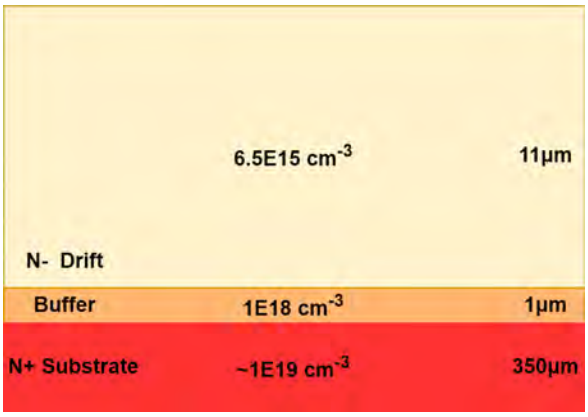


Fig. 5.2 Epitaxial structure of SiC wafers used for defect study. The N-drift region is 11μm thick, with a doping concentration of N_d=6.5 $\times$ $10^{15}cm^{-3}$. The substrate thickness is 350μm.

Average post-growth layer thickness (buffer and drift) and drift doping concentration were measured by the manufacturer across both wafers. WAF1 had an average thickness of 11.9μm and N_d= 6.5 $\times$ $10^{15}cm^{-3}$, whilst WAF2 had a thickness of 12.03μm and N_d= 6.67 $\times$ $10^{15}cm^{-3}$. The wafers were then mapped for defects using a Lasertec SICA tool, with a 3mm resolution.

The corresponding defect wafer maps of WAF1 and WAF2 are shown in figures 5.3 and 5.4, respectively. Different types of defects were detected including SFs, particle and polytype inclusions. The right hand side wafer map shows the overall "yield" of the wafers i.e. shows the usable area of the wafer free from any defects. It should be noted that even the presence of any defect is assumed to be a killer defect in this defect map. The SICA tool defect map did not display any information concerning micropipes, but it is assumed that none were present due to their rarity in present-day SiC wafers.

The defect map of WAF1 shows a high concentration of defects in the bottom right hand corner of the wafer. Stacking faults are by far the most common defect occurring on this wafer, with 142 individual SFs. There are 47 further stacking faults found via photoluminescence. A significant 75 polytype inclusions have also been found, whilst minimal propagated SFs (i.e. carrots) and particle inclusions are present. The yield of the wafer is 95.09%.

The map of WAF2 has a marginally higher yield of 95.19%, with significantly more SFs at 202. A further 71 SFs have been found via PL. Only 34 polytype inclusions have been found on this wafer, compared to the 75 of WAF1. Only 2 particle inclusions are present, and no carrots. The highest concentration of defects is located to the right of the wafer centre.

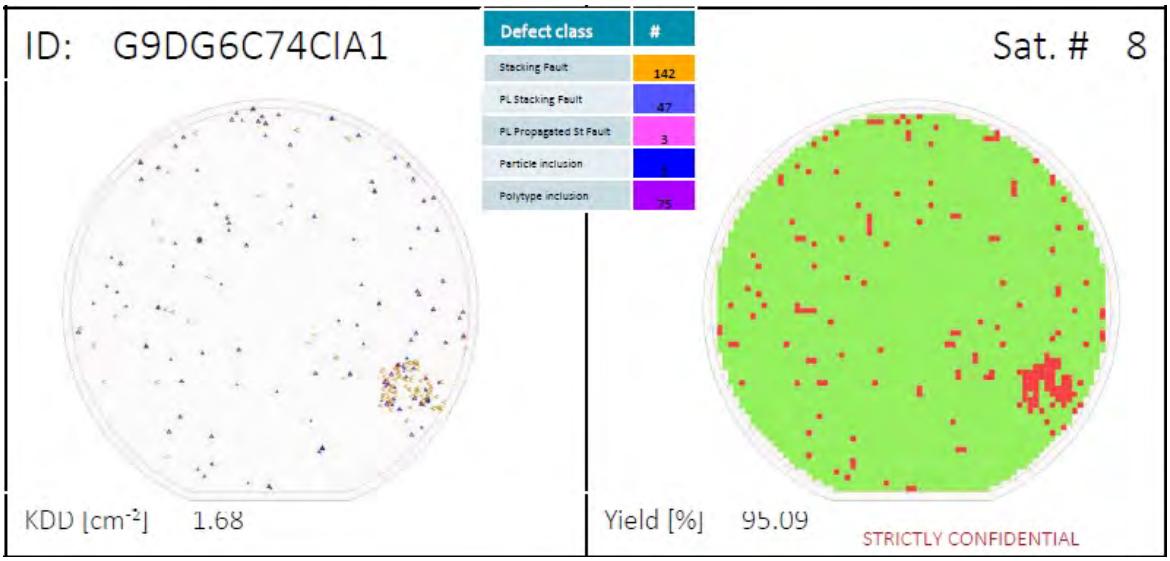


Fig. 5.3 Wafer Map of defect locations for WAF1 using a Lasertec SICA tool. The left hand side displays the location of the different type of defects, whilst the right shows yield of the wafer. The highest concentration of defects is in the bottom right hand corner of the wafer.

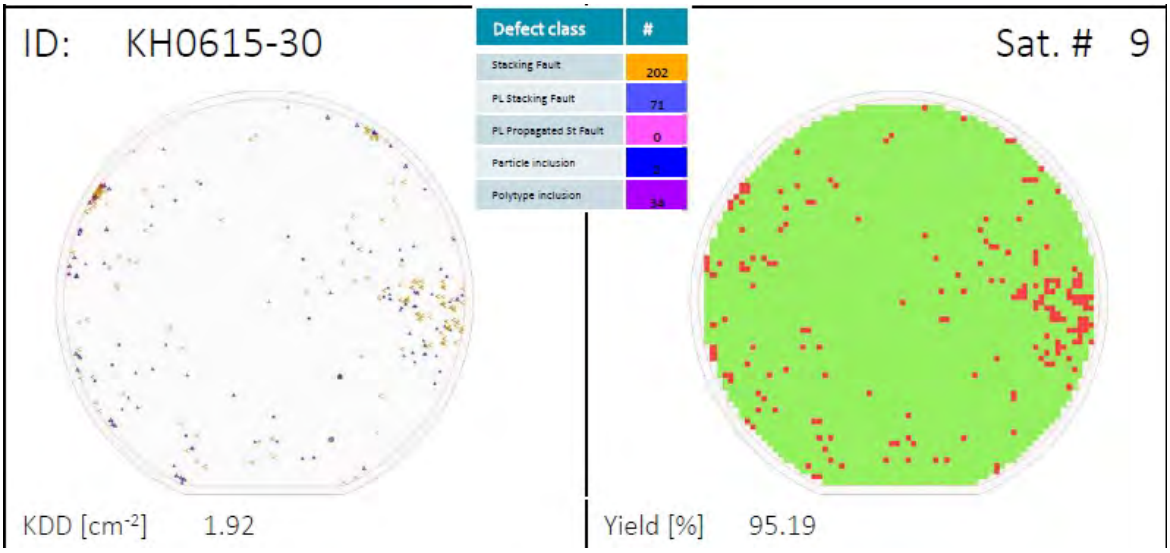


Fig. 5.4 Wafer Map of defect locations for WAF2 using a Lasertec SICA tool. The right hand side displays the location of the different type of defects, whilst the right shows yield of the wafer. The highest concentration of defects is found in the middle right hand side of the wafer.

5.3.2 Fabrication of Schottky Barrier Diodes

The diodes were fabricated across both wafers with a die size of $2.97mm^2$, using a 5mm edge exclusion. The fabrication process was as follows: initial clean in Acetone, Isopropyl

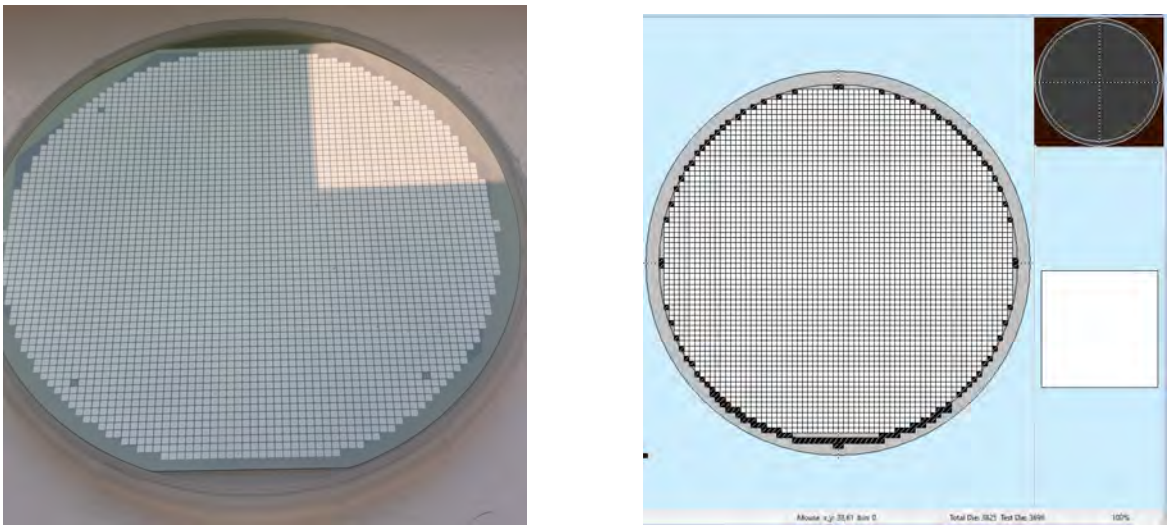
Fig. 5.5 Electrical test setup consisting of a Wentworth S200FA semi-automated probe station (left) and a Keysight B1505A Power Device Analyser (centre).

alcohol (IPA) and de-ionised water. A 200nm nickel layer was deposited on the backside of the wafers using a Moorefield 125 Sputter system. The backside ohmic contact anneal was completed at 1000°C for 2 minutes under vacuum using a Annealsys ASMaster RTA system. Following this, the 400nm nickel frontside contact pads were deposited and subsequentially patterned using a metal lift-off process. Finally, the frontside Schottky contact anneal was completed at 400°C for 2 mins using the same RTA system.

5.3.3 Characterisation of 150mm SiC SBD wafers

Each wafer contained 3695 diodes, each of which required testing in forward and reverse bias. To complete this, a setup consisting of a Keysight B1505A Power Device Analyser connected to a Wentworth S200FA semi-automated probe station was used. This test setup is shown in figure 5.5.

The probe station chuck was electrically connected to the B1505A high voltage Source Measure Unit (SMU), whilst the probe contacting the frontside pad was connected to a medium current SMU. The probe station was configured for automatic control by the B1505A via GPIB connection. This consisted of the stage moving to the next die on the wafer after the B1505A sent a command telling the probe station that the test was complete. One of the fabricated wafers, and the corresponding wafer map on the S200FA probe station are



(a) (b)

Fig. 5.6 (a) Wafer 1 after fabrication of SBDs has been completed. (b) Corresponding wafer map of the wafer generated on the S200FA software for automated testing program.

shown in figure 5.6a and 5.6b, respectively. A test plan was developed on the B1505A to evaluate the diodes in both forward and reverse bias. The tests for each diode were conducted sequentially. After completing the testing plan for one diode, the B1505A sent a command to the probe station to move to the position of the next diode based on the wafer map. This setup resulted in every diode on a wafer being tested both in forward and reverse bias automatically once the process was initialized.

Once an individual test was complete in the testing plan, the corresponding CSV file also recorded the position test die position on the wafer map. Using Python, the data for each set of tests was plotted. Python code was developed to extract V_f, ϕ_b and ideality factor (η) from the forward bias measurement, and V_{br} from the reverse measurement. These extracted values were then used in combination with the die position to generate heat-maps of the diode characteristics across each wafer. The Python code developed to generate these wafer maps can be found in Appendix A.

5.3.4 Methods to Determine Barrier Height and Ideality Factor

The barrier height of the Schottky metal-semiconductor contact, and subsequentially the ideality factor can be calculated using various different methods. This section summarises some of the different approaches.

Current-Voltage Method

Firstly, ϕ_b and η can be calculated from the forward characteristic (I_a-V_a) of the Schottky diode. According to the thermionic current-voltage relationship, I_a can be calculated using in equation 5.1 [190], where A_{diode} is diode area, $A^\star$ is Richardson's constant which is equal to $146\mathrm{A}/cm^2K^2$ for 4H-SiC [215], η is the ideality factor and I_s is the saturation current.

$$I_a = A_{diode}A^\star T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left(\exp\left(\frac{qV_a}{\eta kT}\right) - 1\right) = I_s\left(\exp\left(\frac{qV_a}{\eta kT}\right) - 1\right) \tag{5.1}$$

Ideality factor represents all of the unknown effects which make a Schottky diode non-ideal. An example of this is local variations in ϕ_b across the contact area.

To calculate ϕ_b using this method, I_s is found from extrapolating the semi-log I_a - V_a curve to where V_a = 0V [190]. Then, ϕ_b can be calculated according to equation 5.2. The ideality factor of the diode can be calculated from the slope of the same graph.

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^\star T^2}{I_s}\right) \tag{5.2}$$

Current-Temperature

When V_a is much larger than $\frac{kT}{q}$, equation 5.1 may be written as:

$$\ln\frac{I_a}{T^2} = \ln\left(AA^\star\right) - \frac{q(\phi_b - \frac{V_a}{\eta})}{kT} \tag{5.3}$$

This extraction method involves applying a constant forward bias to the diode, and varying the measurement temperature. The resulting plot of $\ln\frac{I}{T^2}$ against $\frac{1}{T}$ (also known as a *Richardson plot*) can be used to calculate ϕ_b using:

$$\phi_b = \frac{V_a}{\eta} - \frac{2.3k}{q}\frac{d[\log\left(I/T^2\right)]}{d(1/T)} \tag{5.4}$$

However, this method relies on the ideality factor being determined independently by another method e.g. the current-voltage method. Furthermore, this method relies on the key assumption that ϕ_b is temperature independent. The method can be adapted to consider a temperature-dependant ϕ_b, which is shown below in equation 5.5, where $\phi_b(0)$ is the barrier height at 0K, and ε is an empirical fitting parameter [190].

$$\phi_b(T) = \phi_b(0) - \varepsilon T \tag{5.5}$$

Equation 5.3 can then be re written as:

$$\ln \frac{I_a}{T^2} = \ln\left(AA^\star\right) + \frac{q\varepsilon}{k} - \frac{q(\phi_b(0) - \frac{V_a}{\eta})}{kT} \tag{5.6}$$

Capacitance-Voltage

A capacitative measurement may also be used to determine the barrier height. If an AC voltage is applied to a constant reverse dc bias, the relationship between capacitance C per unit area and V is defined as equation 5.7 [190].

$$\frac{C}{A} = \sqrt{\frac{-qK_s\varepsilon_0(N_a - N_d)}{2(-V_{bi} - V - kT/q)}} \tag{5.7}$$

By plotting $1/(C/A^2)$ against reverse dc bias V gives a curve with the slope of $2/[qK_s\varepsilon_0(N_a - N_d)]$, which can be used to calculate the N-type doping concentration. The x-intercept is equal to ($V_{int} = -V_{bi} + kT/q$). The barrier height is related to the built-in potential according to equation 5.8:

$$\phi_b = V_{bi} - V_o \tag{5.8}$$

where V_o is:

$$V_o = \frac{kT}{q}\ln\left(\frac{N_c}{N_d}\right) \tag{5.9}$$

Using equation 5.9 and V_{int}, the barrier height can be defined as:

$$\phi_b = -V_{int} + V_o + kT/q \tag{5.10}$$

.

5.4 Results and Analysis

5.4.1 Forward Bias

The method used to calculate the barrier height and ideality factor of the Schottky diodes was the I-V method. This is primarily due to the other methods not being able to calculate the ideality factor using the same data. The forward voltage is defined as the voltage at which $I_a \geq 0.1\mu$A. As I_a increases exponentially after ϕ_b is overcome, I_a will reach 0.1μA rapidly post diode turn-on. Therefore, this will give an accurate value for the voltage at which the diode

turns on. It should be noted that the maximum resolution ("noise floor") of the measurement setup is approximately 1nA, so further reducing the current at which V_f is extracted may result in extraction of an incorrect V_f value due to noise in the measurement.

Wafer 1

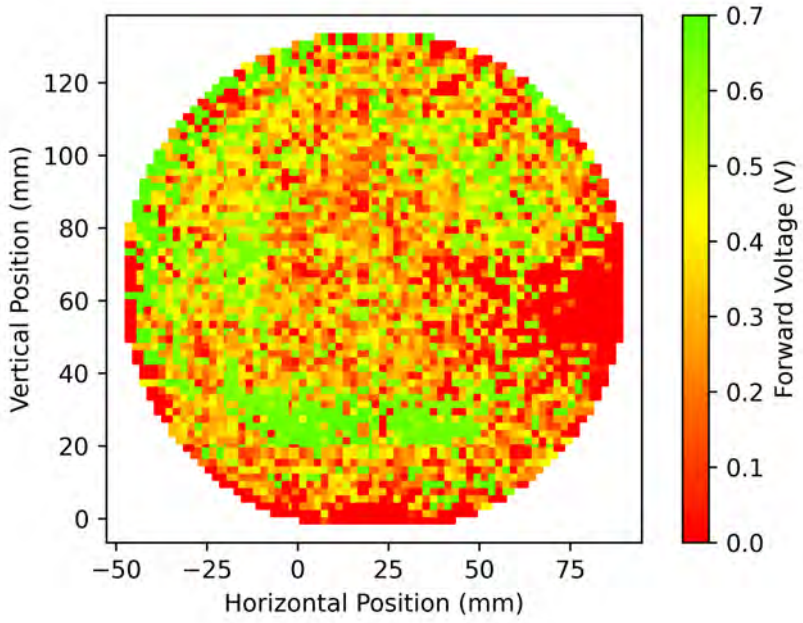


Fig. 5.7 Heat-map of forward voltage across WAF1. A significant proportion of diodes have V_f of near 0V, indicating that they are suffering from high leakage current, and are likely defective.

Figure 5.7 shows the distribution of V_f across WAF1. Devices in some regions of the wafer, predominantly the middle-right hand side and the bottom edge of the wafer exhibit a V_f near 0V. Other areas such as slightly below the wafer centre have a V_f of 0.7V or greater. Figure 5.8 compares the forward characteristics of two particular diodes found on WAF1 - one with high V_f and the other with low V_f. The devices chosen are the diodes found at position (0,26) and (80,60) on the heat-map.

Diode (80,60) is found in the middle-right hand side region where all diodes exhibited low V_f. It is observed that I_a increases immediately in a linear fashion. As the curve does not exhibit a linear gradient on the inset plot, this forward current is clearly not a result of standard diode current conduction as according to equation 5.1.

Based on these factors, it can be concluded that diode (80,60) is suffering from significant forward leakage current below where diode begins to conduct properly. This leakage path

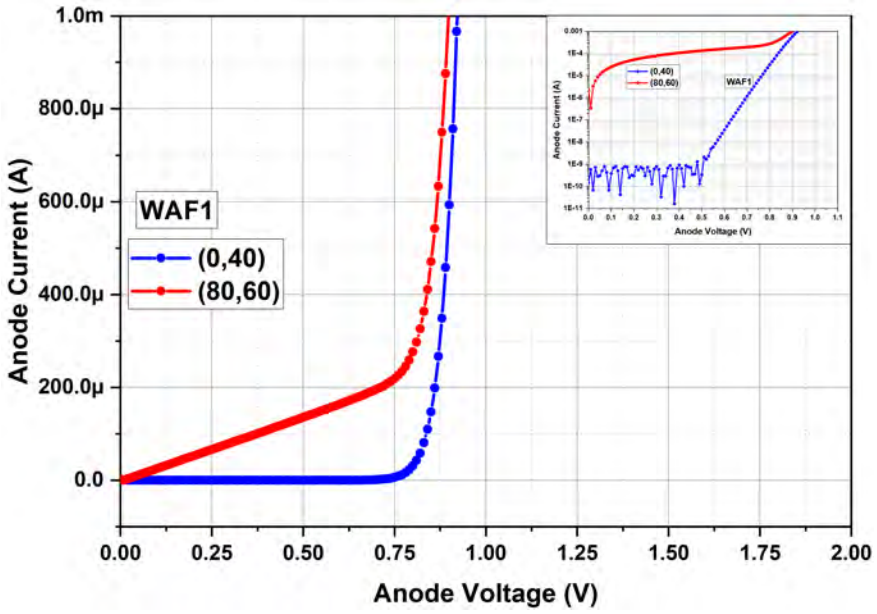


Fig. 5.8 Comparison between the diodes found at positions (0,26) and (80,60) on WAF1. Diode (80,60) conducts $I_a \geq 0.1\mu$A immediately, whilst diode (0,26) begins conducting current 0.55V. This indicates that diode (80,60) is not behaving as a SBD, and is defective.

acts as a low resistance resistor in parallel with the diode. This explains the linear increase in I_a immediately after V_a is applied. The diodes true V_f is likely closer to 0.7V, where exponential increase in I_a is observable. However, the true V_f is not able to be extracted due until the magnitude of the current attributed to the diode is larger than the magnitude of the leakage current, which is observed near 0.7V.

On the other hand, diode (0,40) which is located is slightly above the green area in the bottom-centre region of the wafer was found to have a V_f of 0.63V. The forward characteristic of this diode is typical of a SBD, conducting less than 1nA until 0.53V when current begins to increase exponentially.

The on/off ratio of a diode is typically defined as the ratio of I_a before and after the forward voltage. An higher on/off ratio indicates improved device quality. If the on-state current is taken at V_a= 1V, and the off-state current of diode (0,40) is assumed to be 1nA, this diode has an acceptable on/off ratio of 3.6×10^6. On the other hand, diode (80,60) has an off-state current of 3μA (taken at V_a= 0.02V), which results in an on/off ratio of only 1100, which is over 1000 times worse compared to diode (0,40).

Figure 5.9 shows the distribution of V_f across WAF1. It is clear from the histogram that a significant amount of diodes on WAF1 suffer from the same forward leakage issue as diode (80,60), which causes V_f to be near 0V. In total, 624 diodes had a V_f of between 0 and 0.05V, with a further 457 diodes exhibiting a V_f below 0.2V. It has been assumed that if V_f is below

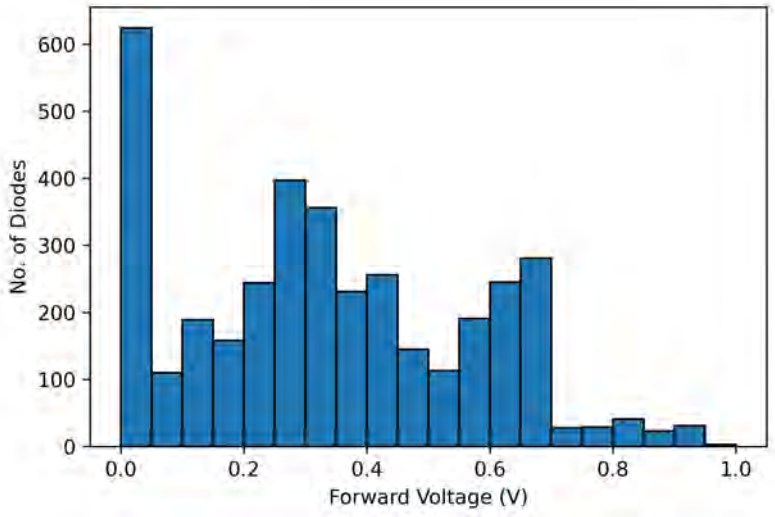


Fig. 5.9 Distribution of V_f at I_a= 1μA across WAF1. Over 600 diodes have V_f values of near 0V, indicating that they suffer from the same forward leakage issues as diode (80,60).

0.2V, then the diode suffers from the same forward leakage issue observed in diode (80,60). This corresponds to 29.2% of the diodes fabricated on the wafer. These diodes have been excluded from subsequent analysis to find ϕ_b and η as the extracted values will be erroneous.

Barrier height and ideality factor can be extracted by finding Y-intercept and slope of the semi-log forward plot respectively, which is shown in the inset of figure 5.8 [190]. The ideality factor η is a measure of all unknown effects which cause the diode to not be ideal. If the diode obeys thermionic emission theory and is completely ideal, η= 1.

In practice, η will be greater than 1 due to non-idealities such as Schottky Barrier Height Inhomogeneity (SBI). This effect describes when there are two Schottky barriers (one with a larger ϕ_b than the other) are connected in parallel [216]. This effect has been attributed to defects [217], but also to interface traps [218] and Fermi level pinning [219].

In fact, 4H-SiC Ni SBDs fabricated on as-grown surfaces have very similar forward characteristics to diode (80,60) in figure 5.8 [216], with very high leakage. Thus, further diodes have been excluded from the dataset if $\eta > 2$. This excluded a further 1235 diodes from the subsequent analysis of Schottky barrier height.

The distribution of ϕ_b in the remaining 1381 acceptable diodes is shown in figure 5.10. The minimum barrier height found was 0.95eV, and the maximum was 1.55eV. The average barrier height was 1.18eV. Barrier heights for Nickel SBDs in existing literature range from 1.12eV to 1.78eV [36, 216, 219–223]. It has also been observed that annealing of a Ni Schottky contact reduces ϕ_b by 0.15eV compared to an as-annealed contact, which would

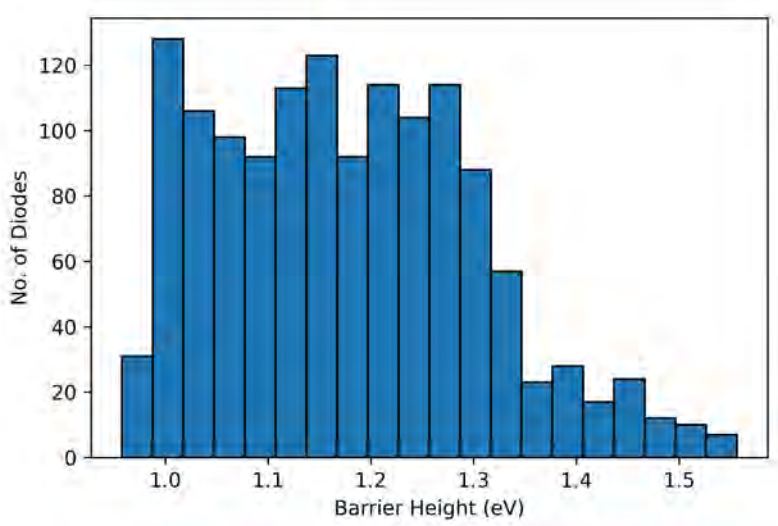


Fig. 5.10 Distribution of ϕ_b across WAF1 for the remaining acceptable 1381 diodes. The average ϕ_b was found to be 1.18eV, with a minimum of 0.95eV.

support why the average ϕ_b for these devices is towards the lower end of the reported range [224].

The calculated ideality factors range from 1.06 to 2, with an average of 1.49. It is concluded that due to the large size of these diodes, there is significant SBI across the contact area, which results in the high η values. Gao et al. have investigated this in depth using conductive Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM) coupled with I-V measurements and found that the formation of voids during Schottky contact anneals ≥ 400°C can lead to slight increase in SBI [224]. As the Schottky anneal temperature used was 400°C, it is possible that this has also contributed to the poor ideality of the diodes. With just 37.4% of the diodes on this wafer exhibited acceptable values for V_f and η, it is challenging to draw a definitive conclusion concerning the existence of any correlation between defect locations and diode characteristics.

Wafer 2

Wafer 2 contained far fewer diodes that suffered from the forward issue that caused V_f to be close to 0V, which was prevalent on wafer 1. As seen on heat-map shown in figure 5.11, the majority of diodes that had low V_f can be found near the wafer edge. The major trend which is observed on WAF2 is that the bottom-left quadrant has a lower V_f of between 0.4 - 0.5V compared to the rest of the wafer, which had V_f of nearer to 0.7V.

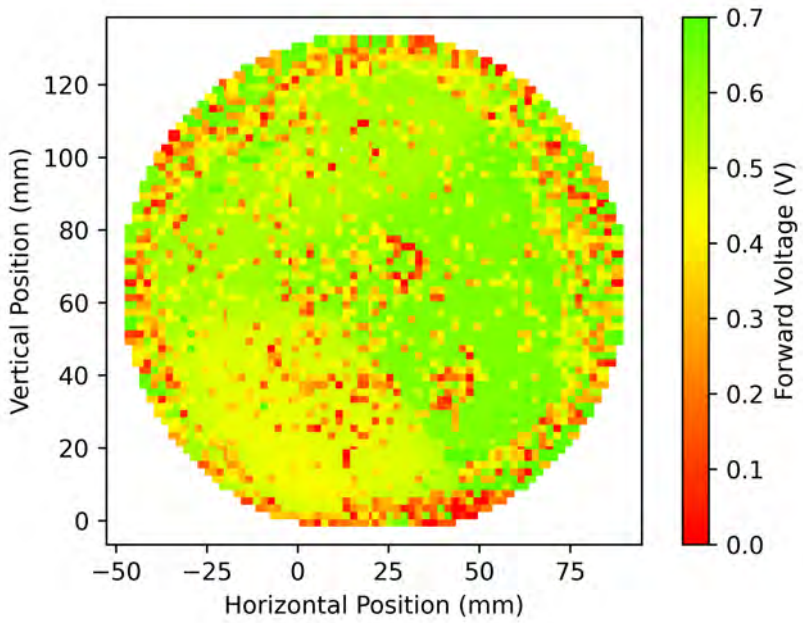


Fig. 5.11 Heat-map of V_f across wafer 2. Far fewer diodes exhibit a V_f close to 0V compared to WAF1. The diodes located in bottom-left quadrant of the wafer have a lower V_f.

Figure 5.11 plots the forward characteristics of two diodes from WAF2 - diodes (0,40) and (50,60). Diode (0,40) is located in the bottom left quadrant, where V_f is reduced. As the forward characteristic of the diode shows, the diode has a V_f of 0.32V. Diode (0,40) does not experience the forward leakage issue discussed previously, which is verified by I_a exponentially increasing with V_a. This indicates that the low V_f of this diode is not due to leakage current, which was the primary issue on WAF1. However, I_a does begin to increase at V_a= 0.05V. Thus, it is concluded that diodes such as (0,40) in the bottom-left quadrant of WAF2 appear to exhibit a lower ϕ_b compared to the rest of the wafer.

Comparatively diode (50,60) is located slightly to the right of the wafer centre and has a V_f of 0.64V, which is double the V_f of diode (0,40). As seen by the semi-log I-V plot, the diode conducts less than 1nA of current until 0.5V, when I_a begins to increase exponentially with voltage.

Figure 5.13 shows the distribution of V_f across wafer 2. Only 218 diodes had a V_f of below 0.2V, which is the first criteria for exclusion from ϕ_b analysis. A further 596 diodes had V_f values of between 0.2 and 0.4V, which can be attributed to the bottom-left quadrant in the heat-map. The most common ranges for V_f on the wafer were: 0.45-0.50V, 0.55-0.6V and 0.6-0.65V. Each of these ranges contained 560, 734 and 709 diodes, respectively. Only 35 diodes had V_f values above 0.7V.

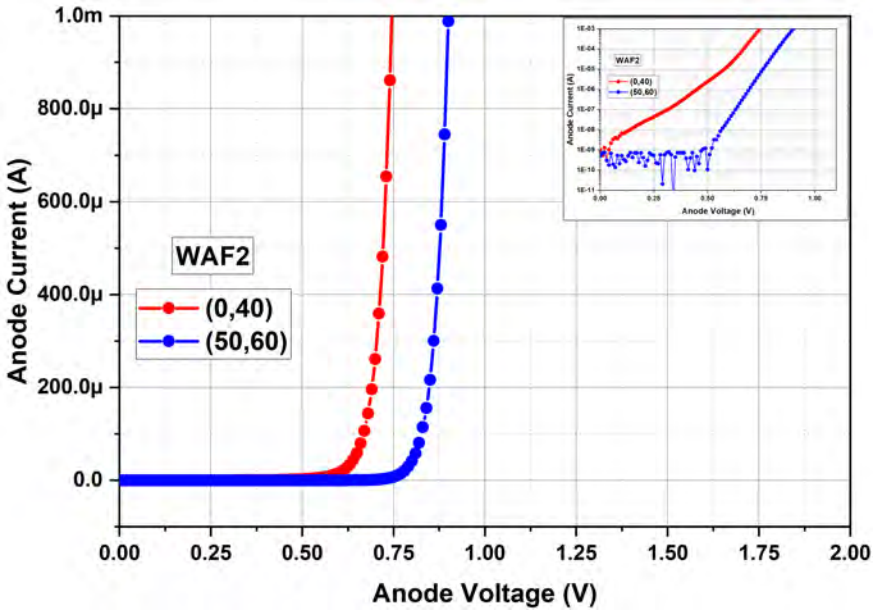


Fig. 5.12 Comparison of the forward characteristics of diodes (0,40) and (50,60) on wafer 2. Diode (0,40) has a V_f of 0.32V, whilst for diode (50,60) V_f= 0.64V. Anode current for diode (0,40) begins increasing almost exponentially at low V_a.

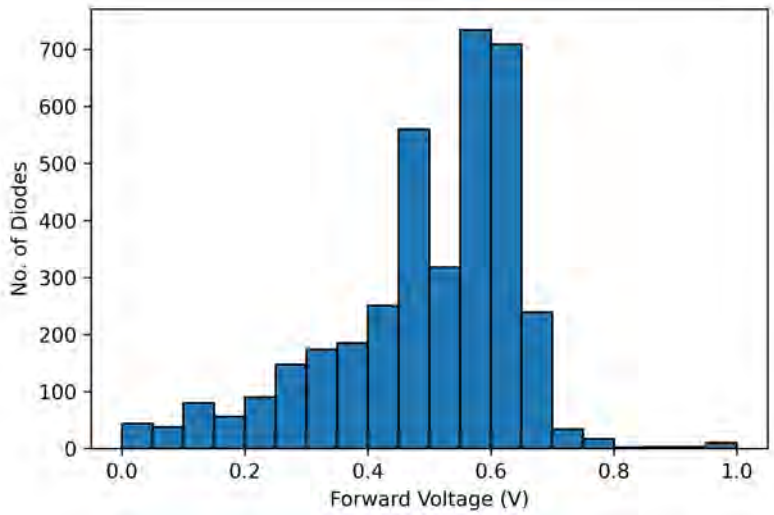


Fig. 5.13 Distribution of V_f across WAF2. The majority of diodes on the wafer had V_f values between 0.4-0.7V. The majority of diodes with V_f below 0.4V can be found in the bottom-left quadrant of the wafer.

The second criteria which was used to exclude poor diodes from ϕ_b analysis was a high ideality factor ($\eta \geq 2$). This criteria excluded another 859 diodes on the wafer which were far from ideal. This left 2618 good diodes with acceptable V_f and η, which is almost double

the 1381 good diodes on WAF1. The most common range of ideality factor on WAF2 was between 1.17-1.22, with 613 diodes falling within this range. The average ideality factor of the remaining good diodes on WAF2 was 1.46.

Figure 5.14 shows the distribution of barrier height for the 2618 diodes on WAF2. The range of ϕ_b on this wafer is far narrower than on WAF1, with 99% of diodes having ϕ_b of between 0.87-1.32eV. By far the most common range is between 1.25-1.29eV, with 582 diodes falling within this range. The second most common range is between 1.08-1.12eV, which contains 363 diodes. The average ϕ_b is 1.12eV for this wafer, marginally lower than the average of 1.18eV on WAF1. As with wafer 1, this value falls towards the lower end of the reported barrier heights of 4H-SiC Ni SBDs in existing literature.

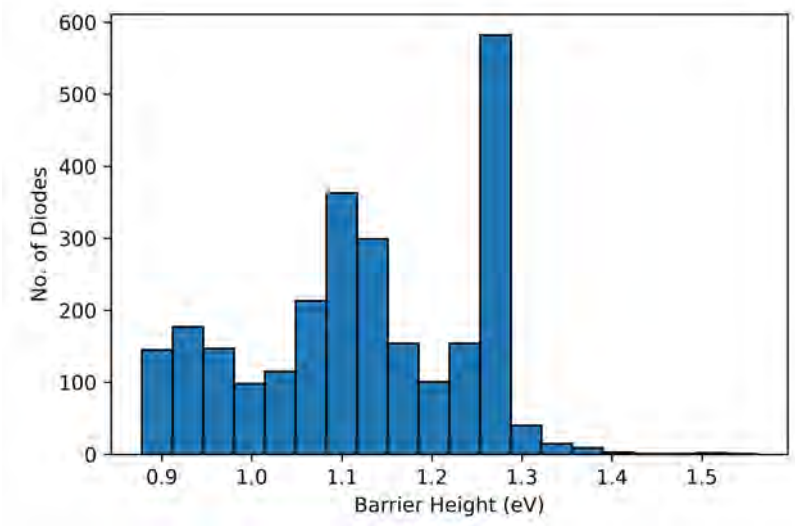


Fig. 5.14 Distribution of ϕ_b across WAF2. The most common ϕ_b range was 1.25 - 1.29eV, followed by 1.08 - 1.12eV. The average barrier height was 1.12eV.

Overall WAF2 has a much improved yield of acceptable diodes, with 70.8% meeting the V_f and η requirements to be considered in further analysis. It was observed that some diodes found on WAF2 did have a reduced ϕ_b towards 0.9eV, however the location of these diodes did not conclusively align the defect locations.

5.4.2 Reverse Bias

As discussed at the beginning of this chapter, morphological defects can significantly affect the reverse blocking ability of a device. Therefore, to investigate this a reverse bias measurement was carried out on both wafers. To achieve this, a bias of between 0-500V was applied

to the cathode contact (V_c). As these devices have been fabricated without edge termination structures, it is not expected for the diodes to fail near the rated voltage of the drift region (approx. 1200V). The SMU compliance has been set at 1mA. It has been assumed that if the reverse current (I_r) reaches 0.1mA, the diode has failed. The voltage at which this failure occurs is the "breakdown voltage" (V_{br}) of the device.

Wafer 1

Figure 5.15 shows the breakdown voltage heat-map of WAF1. As seen by the figure, there is a large variation in breakdown voltage across the wafer, with the poorest devices failing below 25V. Comparatively, the best devices do not reach an I_r of 0.1mA at 200V. The only localised area of poor devices is in the middle right region of the wafer. Devices in this region suffered from the forward leakage issues causing $V_f \leq 0.05$V, which is evidence of some correlation between forward and reverse performance of the SBDs.

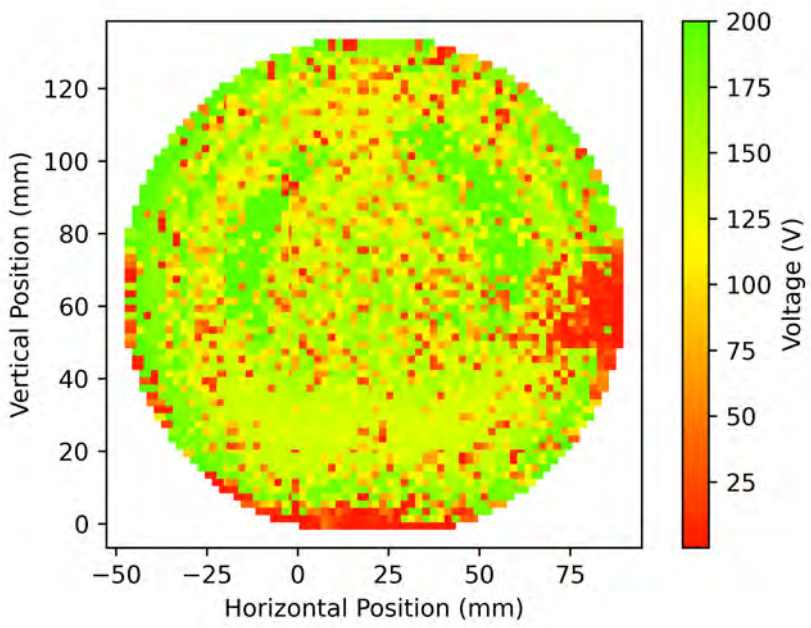


Fig. 5.15 Heat-map of breakdown voltage across WAF1. Localised areas of poor breakdown are observed on the middle right hand side of the wafer, and in the outer devices towards the bottom left.

However, this trend is not replicated for all bad devices which were identified in the forward bias section. Some devices exhibited V_{br} of ≥150V whilst being identified as bad diodes in the forward bias section. Equally, the area below the centre of WAF1 which was

found to have high V_f does not have the highest breakdown voltage across the wafer, as most diodes in this region have V_{br} between 100-150V. Therefore, there is not a clear relationship between forward and reverse behaviour of the diodes across the whole of wafer 1.

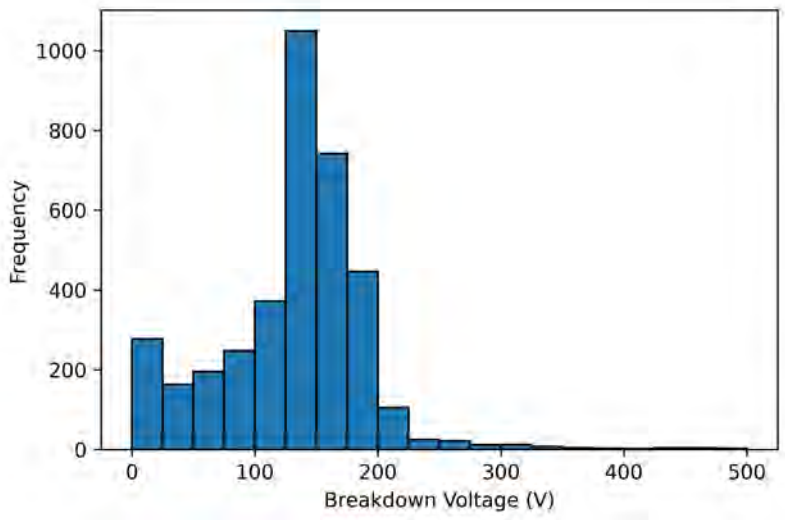


Fig. 5.16 Distribution of breakdown voltages on WAF1. Most devices failed between 100-200V. Very few devices sustained voltages above 300V. A significant amount of devices failed below 25V.

Figure 5.16 shows the distribution of V_{br} on wafer 1. The highest failure rate occurred between 125 - 150V where 1049 diodes failed, representing 28.3% of the devices on the wafer. Between V_c= 0-50V, 636 diodes experienced breakdown, accounting for 17.2%. Of those devices, 277 exhibited $V_{br} \leq$ 25V. Between 100 - 200V, 70.6% of the devices failed. Only 73 diodes sustained greater than V_c= 250V. Furthermore, only 40 diodes had $V_{br} \geq$ 300V. The average breakdown voltage was 131V.

Figure 5.17 compares the reverse characteristics of the same diodes on WAF1 which were discussed in the forward bias section - diode (0,40) and diode (80,60). Diode (80,60) reaches a current of 1mA at just 10V, while diode (0,40) shows a more gradual increase in current, reaching 1mA at 159V. This sharp contrast highlights the large variation between the average and poorest devices on wafer 1, particularly the diodes on the middle-right hand side of the wafer which fail almost immediately.

Overall, the reverse bias measurements of diodes on WAF1 appear far better than expected when compared to the forward bias results. Low V_{br} was observed around the wafer extremities, and on the right hand side of the wafer. Although some defects are located

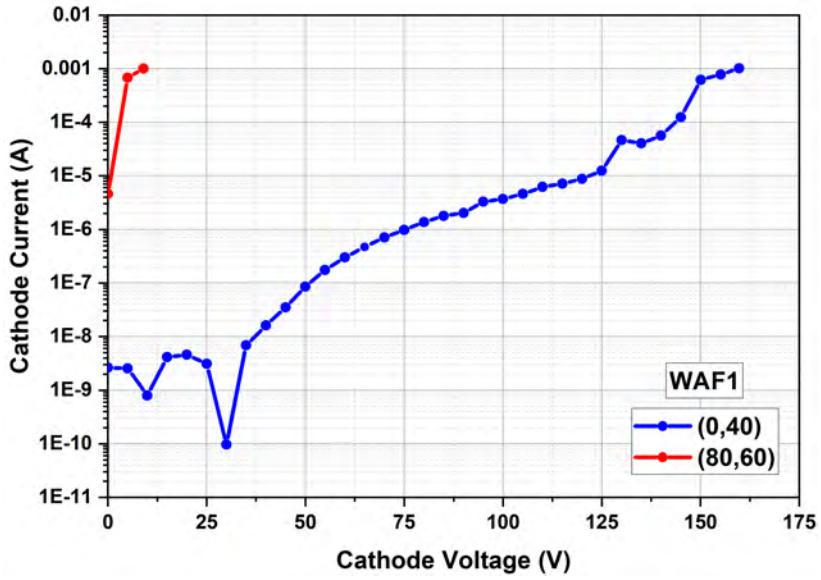


Fig. 5.17 Comparison between the reverse characteristics of diodes (0,40) and (80,60). Diode (0,40) experiences a gradual increase in current from 3nA at 10V to 1mA at 160V, compared to diode (80,60) which conducts 1mA by V_c=10V.

within these areas, there does not appear to be conclusive relationship between V_{br} and defect locations on this wafer.

Wafer 2

Figure 5.18 shows the heat-map of breakdown voltage for WAF2. The most immediate difference between the two wafers is that the majority of devices on wafer 2 had not failed at 500V. The diodes located on the wafer extremities had poorer breakdown performance, with most failing between 150 - 300V. There is some weak correlation between the forward and reverse performance, for example the localised areas around (40,40) and (30,70). These regions had V_f values near 0V, and have breakdown voltages of between 150 - 300V, far lower than the majority of diodes on the wafer. However, the bottom-left quadrant of devices which had a lower V_f of around 0.4V had excellent breakdown performance.

The distribution of diode breakdown voltages on the wafer is shown in figure 5.19 as a histogram. The majority of the 3695 diodes had breakdown voltages of 500V, which was the maximum V_c used during the test. This was the case for 46.6% of the diodes on the wafer. This indicates that a significant proportion of the diodes have not failed by 500V.

Only 56 diodes failed below 150V, which was above the average V_{br} of WAF1 (131V). The average breakdown voltage on WAF2 was 395V, however this is not representative due to nearly half of the devices not reaching failure at the maximum test voltage of 500V.

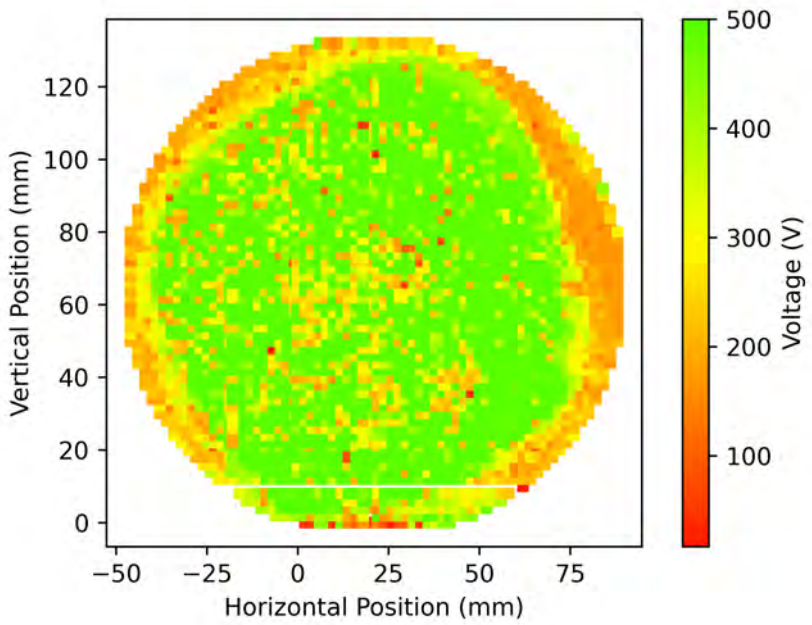


Fig. 5.18 Heat-map of breakdown voltage across WAF2. Degradation in breakdown voltage is observed around the edges of the wafer. It should be noted that the scale on this figure is not equivalent to figure 5.15, where the maximum value was 200V.

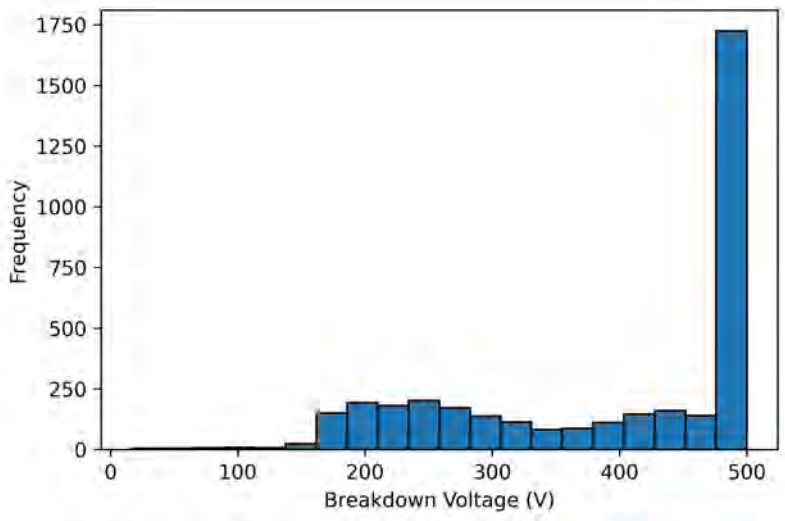


Fig. 5.19 Distribution of breakdown voltages on WAF2. Almost 50% of diodes did not fail at the maximum voltage of 500V.

Figure 5.20 displays the reverse characteristics for two diodes - diode (0,40) and diode (22,78) which have V_{br} values of 195V and 500V, respectively. Diode (0,40) exhibits a rapid

increase in reverse current when V_c reaches 15V. By V_c= 50V, the diode reverse current is 1.73μA, and at V_c= 100V I_c= 8.2μA. Reverse current gradually increases with V_c until 195V, when I_c reaches 1mA instantaneously.

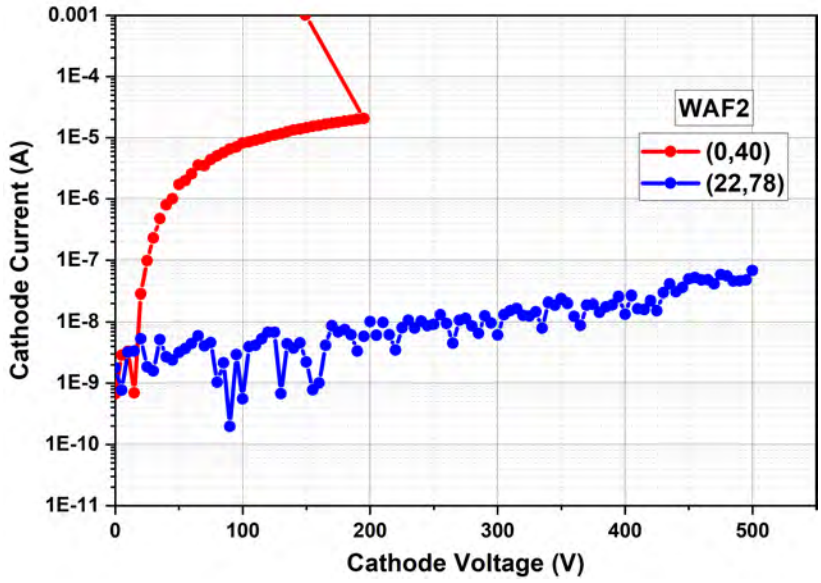


Fig. 5.20 Reverse characteristics of diodes (0,40) and (22,78). Diode (0,40) has a breakdown voltage of 195V, compared to diode (22,78) which has not failed when the maximum V_c=500V was applied.

On the other hand, the reverse current of diode (22,78) increases gradually from less than 10nA at 0V to 68nA at 500V. Evidentially, this diode has not reached the criteria for breakdown voltage (I_r≥0.1mA), and thus the maximum voltage value has been extracted instead by the Python script. This verifies that devices such as diode (22,78) have not failed at the maximum test voltage of 500V, indicating V_{br} is larger than 500V, and potentially could be significantly higher.

Overall, blocking performance of diodes on WAF2 was found to be excellent, with most diodes not having failed at the maximum test voltage of 500V. Some correlation was observed between the defect locations and the right hand side of the wafer. However, being near the wafer edge, it is possible that this could be circumstantial.

5.5 Conclusion

In conclusion, nickel Schottky Barrier Diodes have been successfully fabricated across two 150mm defect mapped N-type epitaxial 4H-SiC wafers to evaluate any correlation between the diode characteristics, and the location of mapped defects. All diodes have been tested in

forward and reverse bias to extract V_f, ϕ_b, η and V_{br}. Python code has been developed to generate heat maps of device characteristics across entire 150mm wafers, enabling assessment of variation in device performance across the wafer.

It was found that forward leakage issues prevented the extraction of ϕ_b for some diodes, particularly on wafer 1. Significant forward leakage has been observed previously for 4H-SiC Ni SBDs fabricated on as-grown surfaces [216]. Furthermore, the ideality factor of the remaining diodes that do not suffer from forward leakage issues was found be relatively large, with average η equal to 1.46 for wafer 2. As the Schottky contact area is large, it is concluded that there is significant SBI across the contact, which increases η. This may have been further exacerbated by the 400°C Schottky contact anneal, which has been shown to both reduce ϕ_b and increase η [224]. The average ϕ_b of the remaining diodes on wafer 1 and 2 which do not suffer from either of the above issues is 1.18eV and 1.12eV respectively, both of which fall within reported values in existing literature. Breakdown performance on wafer 1 was significantly worse than wafer 2, where most diodes did not fail under the maximum reverse biased tested (500V).

Correlation between the location of defects and forward or reverse performance was circumstantial. The majority of defects on both wafers were located towards the wafer edges, where diode performance was also poor. However, devices fabricated towards the wafer edges are expected to be exposed to higher process variability than devices towards the centre, which may partially explain the poor performance of these devices. The only area of strong association between poor forward and reverse characteristics was observed on the right hand side region of wafer 1, although it was also observed in small localised regions on wafer 2. Therefore, it can be concluded that majority of material defects such as SFs do not noticeably impact the performance of SBDs, and thus should not affect the performance of 4H-SiC JFETs.

It is also concluded that the poor yield of acceptable diodes, especially on wafer 1 could be improved with more intensive surface preparation than just IPA and Acetone prior to the Schottky contact being deposited. It has been shown that sacrificial oxide growth and strip, or a NO anneal can improve uniformity of Schottky contacts on 4H-SiC [225]. Furthermore, depositing a dielectric to passivate the SiC surface would assist in eliminating the possibility of elevated surface leakage contributing to high forward leakage. It may also be beneficial to reduce the size of the Schottky contacts to minimize the chance of inhomogeneities in the barrier height. Finally, RIE etching of the surface could be employed to minimize SBI, and possibly forward leakage issues [216].

Chapter 6

Process Development for 4H-SiC JFET Fabrication

6.1 Preface

This chapter discuses work concerning activation of implanted P-type dopants and P-type Ohmic contacts, both of which are critical to an optimised gate contact for SiC JFETs. Firstly, the Tranfer Length Method (TLM) and Hall characterisation methods used to optimise both of these processes are discussed, including their underlying theory and step-by-step extraction methods to find experimental parameters. This is followed by process development work on carbon capping layers used for surface protection during implantation anneals. Finally, results on optimizing aluminium dopant activation and Specific Contact Resistance (SCR) of ohmic contacts are presented and analysed.

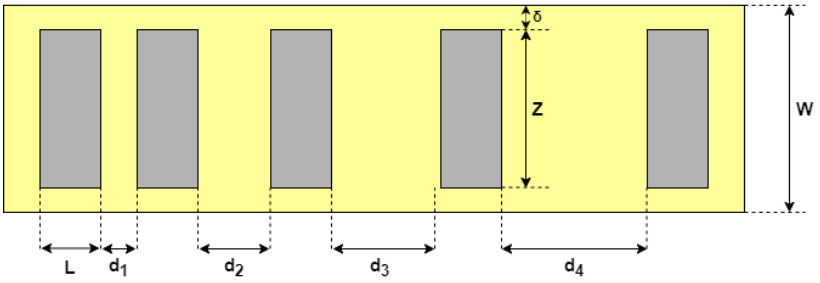
6.2 Characterisation Methods

6.2.1 Contact Resistance

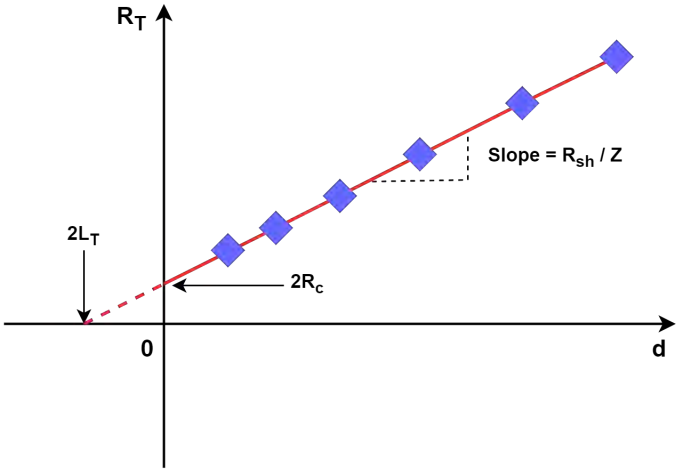
All semiconductor devices require metal contacts, which exhibit resistance as current passes through them. Therefore, to accurately analyse the overall performance of a device, it is essential to characterize the resistance of these contacts. Metal contacts can exhibit either Ohmic or Schottky (Rectifying) behaviour. Ohmic contacts have linear current-voltage characteristics, whereas Schottky contacts are characterized by a voltage drop before conducting due to their rectifying properties. In a JFET, all three contacts (Gate, Source and Drain) must exhibit Ohmic behaviour. The proposed process flow and mask layout for the JFET designed during this thesis can be found Appendix C.

The standard method used to characterize Ohmic contacts is the *transfer length method* (TLM) [190]. This method enables extraction of multiple parameters that quantify the quality of the contact, most importantly being the *specific contact resistance* (ρ_c).

Standard TLM structures



(a)



(b)

Fig. 6.1 (a) A standard TLM test structure, with rectangular spaced pads on a highly doped region of semiconductor, separated by incrementally larger distances. (b) The corresponding plot of R_T as a function of contact spacing d, illustrating parameters which may be extracted from the plot.

Standard TLM test structures consist of rectangular contacts incrementally spaced on an isolated region of highly doped semiconductor, as shown below in figure 6.1a. The relationship between the resistance of the contact R_T and contact spacing d is shown in equation 6.1. When R_T is plotted as a function of d multiple useful parameters concerning the contacts and the doped layer can be calculated. Firstly, the semiconductor sheet resistance R_{sh} can be determined from the slope of the linear fit ($\frac{\Delta R_T}{\Delta d} = \frac{R_{sh}}{Z}$). Additionally, contact

resistance R_C is found at the y-intercept ($d = 0$), and transfer length L_T at the x-intercept ($R_T = 0$) as shown in figure 6.1b. The specific contact resistance may then be calculated using equation 6.2 as both R_{sh} and L_T are known from the $R_T - d$ plot.

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}}{Z}(d + 2L_T) \tag{6.1}$$

$$\rho_c = R_c L_T Z \tag{6.2}$$

Circular TLM Structures

One drawback of using standard TLM structures to extract ρ_c is that they require the doped region of the semiconductor to be isolated. This requires either (i) a hard-mask to selectively implant the semiconductor or (ii) an isolation etch through a uniformly doped layer. This is required to prevent excessive current spreading around the contact edges [190]. An alternative version of the TLM structure which leverages the same theory is the circular TLM (CTLM). These consist of a circular inner region contact with a radius r, separated from a surrounding metal pad by a spacing d, as shown in figure 6.2.

Importantly, CTLM structures do not suffer from the current spreading issues like TLMs, and as such do not require the further isolation process step. However, a key assumption in TLM theory is that R_{sh} is identical throughout the doped layer. In practice, R_{sh} underneath contacts can be altered due to the formation of alloys silicides during the annealing process [190]. To account for this, a further measurement must be taken, which is achievable on linear TLMs but not on CTLMs [190, 226].

Fig. 6.2 Circular TLM structures, where the shaded area represents deposited metal, and yellow represents bare the bare semiconductor surface.

The same theory holds for the CTLMS as for the TLM structures, with some minor adjustments as the inner contact radius r is used instead of the width Z as in the standard TLM equation. Additionally, a correction factor C must be used to compensate for the difference between equations 6.1 and 6.3 to enable a linear fit to be used.The correction factor is calculated using equation 6.4.

$$R_T = \frac{R_{sh}}{2\pi r}(d + 2L_T)C \tag{6.3}$$

$$C = \frac{r}{d}\ln\left(1 + \frac{d}{r}\right) \tag{6.4}$$

If this correction factor is not included, then the sheet resistance will be underestimated, and conversely L_T will be overestimated. The effect of the correction factor is shown using some example ideal CTLM data in figure 6.3 below. Specific contact resistance can be extracted from CTLMs using equation 6.5.

$$\rho_c = R_c L_T 2\pi r \tag{6.5}$$

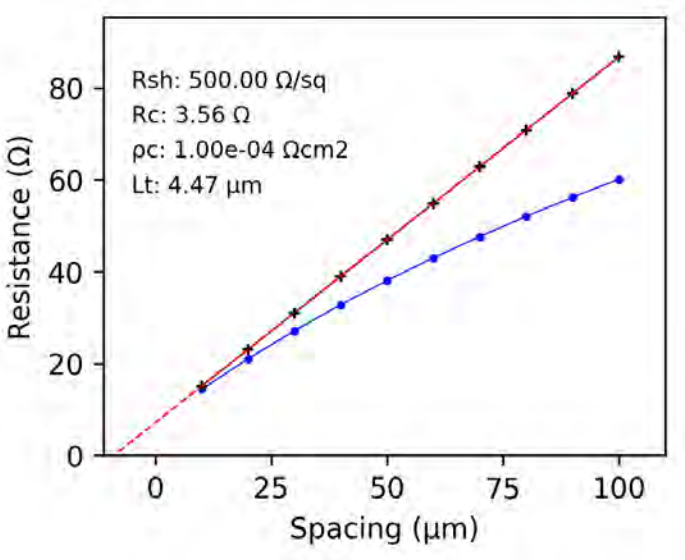


Fig. 6.3 Example fit of ideal CTLM data, with uncorrected data shown in blue, and corrected data shown in black.

6.2.2 Electrical Activation of Dopants

Verifying the properties of implanted regions is a crucial step in developing a device fabrication process. Understanding the relationship between activation anneal temperature (T_{anneal}) and the fraction of implanted dopants that become electrically active is especially important, particularly for aluminium dopants, which are commonly used to form P-type regions in SiC. Furthermore, other parameters such as carrier mobility (μ) and sheet resistance (R_{sh}) of the

layer are important characterisation tools to ensure that the implanted region is behaving as expected.

Sheet Resistance

A diagram of the Van der Pauw (VDP) test structure is shown in figure 6.4. Current - voltage measurements completed on VDP test structures can be used to calculate the sheet resistance (R_{sh}) of a thin, uniformly doped layer.

Equation 6.6 is used to find R_{sh}, where R is the resistance of the linear I-V curves of the VDP structure [190]. An Arrhenius plot of R_{sh} as a function of activation anneal temperature (T_{anneal}) enables calculation of the activation energy (E_{act}) of the dopant post-implant. This is the energy required for the dopant to substitute into the SiC crystal lattice, becoming electrically active.

$$R_{sh} = \frac{\pi}{\ln 2} R \tag{6.6}$$

An example of this plot is shown below using data from Spera et al. [1] for aluminium dopants is shown in figure 6.5, which result in E_{act}= 1.03eV. It can be seen that R_{sh} reduces as annealing temperature increases, indicating a higher T_{anneal} results in more aluminium dopants being active.

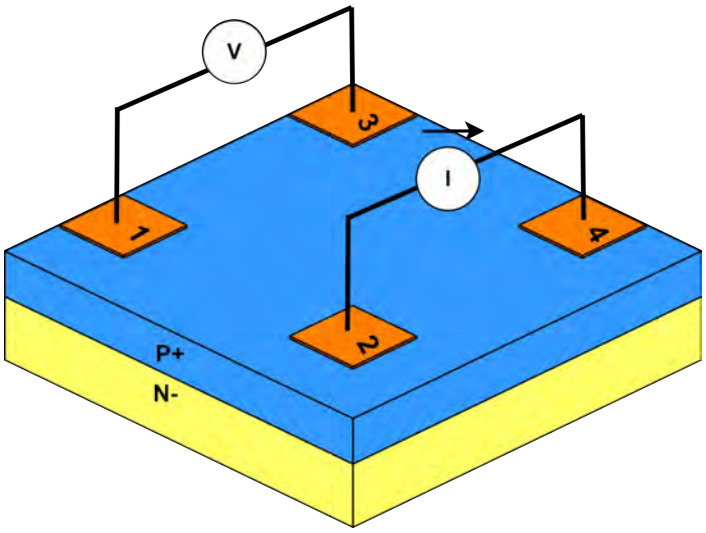


Fig. 6.4 Diagram of a Van der Pauw structure on a N- epitaxial layer which has been implanted with P-type species. Voltage is applied across contacts 1 and 3, whilst current is measured between contacts 2 and 4.

It must be noted that when discussing activation energy that this is the energy required for aluminium atoms to become electrically active i.e. to contribute as an acceptor towards the

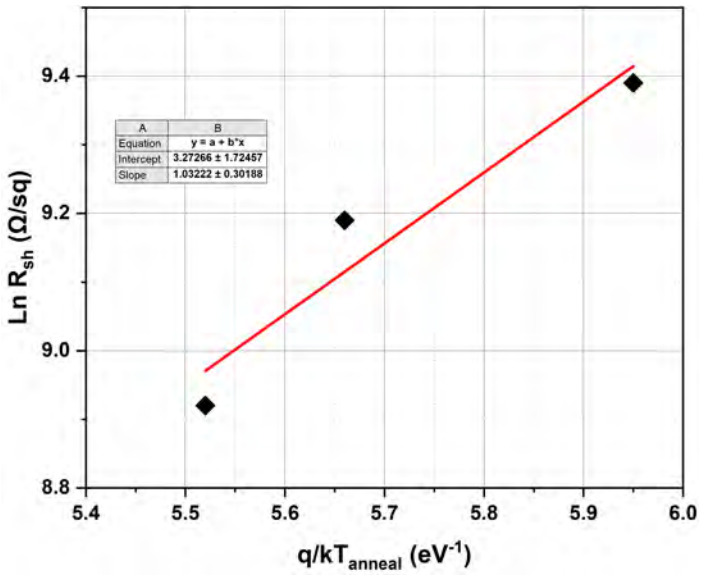


Fig. 6.5 Arrhenius plot of sheet resistance of an aluminium implanted 4H-SiC layer recreated using the data from Spera et al. [1] The extracted E_{act} is 1.03eV. R_{sh} reduces at higher activation anneal temperatures.

P-type doping of a layer. This is separate to the Ionization energy (E_{ion}) which is the energy required ionize the activated acceptor. The ionization energy determines how many free carriers are present in the doped layer at a given temperature. If E_{ion} is large, the incomplete ionization effect becomes more pronounced.

To find E_{ion}, the sample R_{sh} must be measured as a function of temperature. This enables use of an Arrhenius plot similar to the one shown in figure 6.5, but using measurement temperature opposed to T_{anneal}. An estimate of E_{ion} can be found by considering the temperature dependence of R_{sh} due to carrier mobility and concentration (in the case of P-type, the carrier type is holes). This is shown in equation 6.7, where hole mobility is μ_p, hole concentration is p and t_{imp} is the implanted layer thickness.

$$R_{sh}(T) = \frac{1}{q\mu_p(T)p(T)t_{imp}} \tag{6.7}$$

The hole concentration as a function of temperature is described by the neutrality equation. As 4H-SiC has a wide bandgap, and thus a very low n_i, hole concentration can be approximated as [227]:

$$p \approx 0.5[-N_d - x + \sqrt{(N_d - x)^2 + 4N_a x}] \tag{6.8}$$

where x is:

$$x = \frac{N_v}{g} \exp\left(\frac{-E_{ion}}{kT}\right) \tag{6.9}$$

The degeneracy of acceptors g is equal to 4 in 4H-SiC. Therefore, the temperature dependence of carrier concentration is predominantly related to E_{ion}:

$$p(T) \propto \exp\left(\frac{-E_{ion}}{kT}\right) \tag{6.10}$$

Carrier mobility μ_p is also influenced by temperature; the temperature dependence of μ_p can be expressed as [228]:

$$\mu_p(T) = \mu_p(N_a)\left(\frac{T}{300}\right)^{-2.56} \tag{6.11}$$

Hence:

$$\mu_p(T) \propto \left(\frac{T}{300}\right)^{-2.56} \tag{6.12}$$

As μ_p has a far weaker relationship with temperature than p, it is possible to neglect the effect of μ_p and approximate the temperature dependence of R_{sh} can be approximated using equation 6.13 [1]. As with the previous Arrhenius plot used to find E_{act}, E_{ion} is equal to the slope of the linear fit. This method to find E_{ion} can also be applied to R_{sh} values found from TLM measurements.

$$R_{sh}(T) \propto \frac{1}{\exp\left(\frac{-E_{ion}}{kT}\right)} \tag{6.13}$$

Hall Effect Measurements

Hall effect measurements can be taken on VDP test structures to extract active carrier density, and carrier mobility. This involves applying a magnetic field perpendicular to the surface of the sample during an electrical measurement. A constant current is applied across contacts 1 and 3, whilst the hall voltage (V_H) is measured across contacts 2 and 4. A visualisation of this is shown below in figure 6.6.

The hole concentration p can then be measured using equation 6.14, where t_{imp} is the thickness of the implanted layer, I is the applied current, B is the applied magnetic field, R_H is the Hall coefficient and r_H is the Hall scattering factor [190]. In previous works, r_H=1 has been assumed, however this leads to overestimation of carrier density [229]. Equally, to calculate the electron density (n), the polarity is of the equation is flipped.

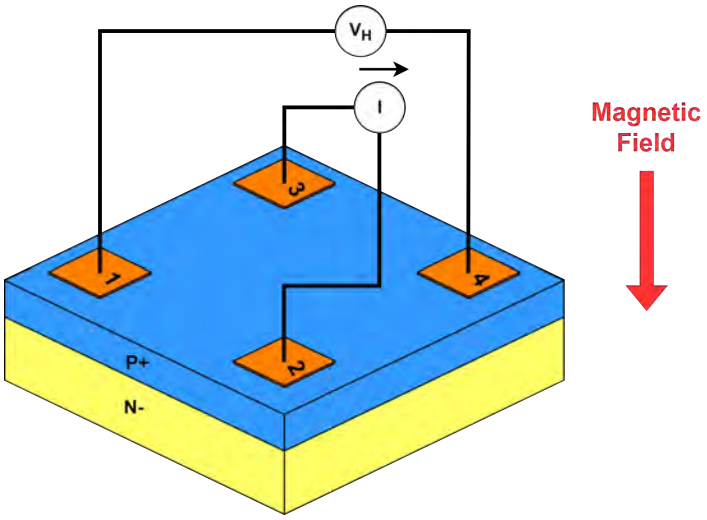


Fig. 6.6 Schematic of the Hall effect measurement setup on a Van Der Pauw test structure. Current is applied across contacts 1 and 3, whilst Hall voltage is measured between contacts 2 and 4. A magnetic field is applied perpendicular to the sample surface.

$$p = \frac{r_H}{qR_H} = \frac{r_H IB}{V_H q t_{imp}} \tag{6.14}$$

$$n = -\frac{r_H}{qR_H} = -\frac{r_H IB}{V_H q t_{imp}} \tag{6.15}$$

The theoretical hole concentration value calculated using the equation (6.8) can be compared to the experimental value for p when r_H is equal to 1. The temperature dependant Hall scattering factor can then be calculated using equation 6.16. Asada et al. have found r_H to ≈ 0.5 for N_A= $7 \times 10^{18} cm^{-3}$ at 300K, before reducing to 0.25 at 700K using this method [230]. Asada et al. also have proved that r_H reduces at higher values of N_a. Temperature dependant hall scattering factors found by Asada et al. for P-type 4H-SiC will be used for extracting p in this work to find the corrected hole concentration (p_{corr}) values.

$$r_H(T) = \frac{p_{theor}(T)}{p_{exp}(T)} \tag{6.16}$$

Once p_{corr} has been calculated, the carrier mobility μ_p can be calculated using equation (6.17):

$$\mu_p = \frac{1}{q p_{corr} R_{sh} t_{imp}} \tag{6.17}$$

6.3 Development of Carbon Caps for Surface Protection

Using Ion implantation to form selectively doped regions is a common practice in semiconductor manufacturing. It is used for fabrication of active regions, such as the JFET P+ gate and MOSFET P-body, but also for edge termination structures such as FFRs. Unfortunately, the high density of the 4H-SiC lattice necessitates the use of large implantation energies to form dopant profiles far from the sample surface. For example, the work completed in chapter 3 of this thesis showed that a beam energy of 760keV was required to form a P+ region 1μm into SiC.

As implantation is a kinetic process, it causes significant lattice damage, which is only further exacerbated by high beam energies and doses. Furthermore, very few as-implanted ions become electrically active, especially for the most common P-type dopant for 4H-SiC - aluminium. Hence, annealing is required post-implantation at 1600 - 1800°C to repair the lattice damage, and to cause substitutional doping to occur, making the ions electrically active [1, 231–234].

Whilst annealing solves the crystal damage and activation issues caused by ion implantation, the high temperatures used during the post-implant anneal result in a significant increase in surface roughness. This is caused by preferential evaporation of Si, resulting in ridges forming on the surface termed as "step bunching" [191]. Furthermore, diffusion of dopants towards the surface has been observed at higher annealing temperatures, [235, 236].

To prevent step-bunching, the SiC surface must be protected during the high temperature post-implant anneal. A protective layer on the surface has been shown to suppress the step bunching effect, and improve the quality of Ohmic contacts to P-type SiC [191]. Additionally, a capping layer should prevent any dopants diffusing out of the SiC sample. Various different protective layers have been demonstrated, such as SiO_2 [237] and Aluminium Nitride [238]. However by far the most common material used is a layer of graphite/carbon. A carbon capping layer is most commonly formed by annealing photoresist at temperatures above 750°C to which converts it into graphite [239]. Photoresist contains a significant amount of solvent, resin and other organic components, which when subject to pyrolysis will result in a layer of graphite being formed on the sample surface. This carbon capping layer can be removed by an oxidation process such as dry oxidation [240].

6.3.1 Formation of Carbon Cap

To develop a carbon cap recipe, firstly the photoresist (PR) film must be deposited. Additionally, it is advised to hard-bake the PR to evaporate most of the solvent contained in the film prior to the conversion anneal [239]. This helps to maintain a clean furnace chamber and

ensures the chamber pressure remains stable. For this development work, three 100mm Si wafers were used. This enabled a JP Woolam Ellipsometer to be used to measure PR film thicknesses.

The photoresist chosen for this process was Shipley Microposit S1818. The photoresist was deposited on the wafers using a spin coater, spun at 3000RPM for 30s. Each of the wafers under went a soft bake at 115°C for 1 minute on a hotplate. The initial PR thickness were found to be 2014nm, 1921nm and 1918nm for each of the wafers, respectively. All three wafers were then baked at a 210°C on the same hotplate in increments of 5 or 10 minutes, after which the PR thickness was remeasured. The relationship between bake time and PR thickness is shown in figure 6.7.

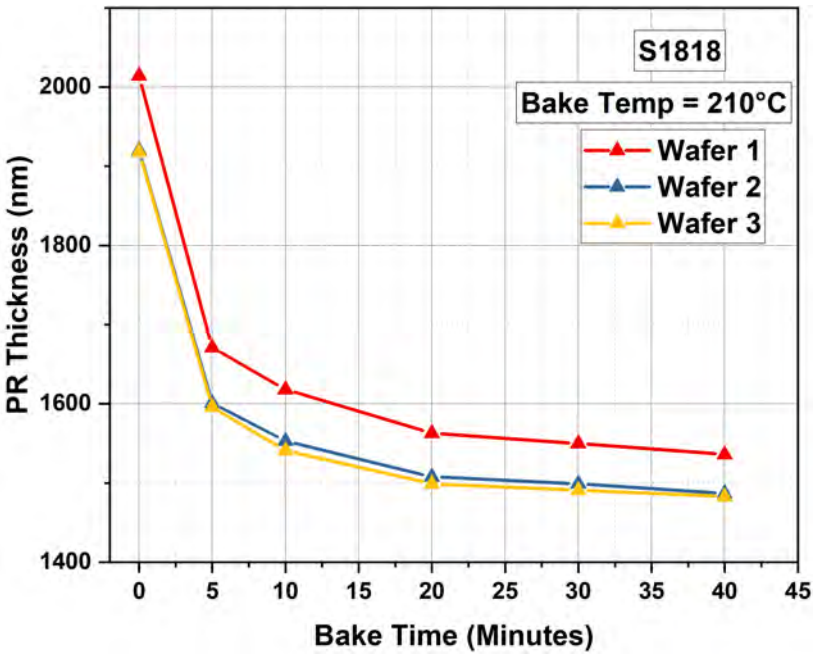


Fig. 6.7 Photoresist thickness on silicon wafers after hard-bakes at 210°C of different lengths. Initially, a significant decrease in PR thickness is observed. After an accumulative 30 minute bake, the reduction in thickness begins to saturate at 1nm/min.

As seen in figure 6.7, the PR film thickness initially decreases significantly, with an average reduction of 328nm after the first 5-minute bake. The large decrease in thickness is presumably due to the vast majority of the solvent evaporating from the film. The next bake results in a thickness reduction of 52nm on average, followed by a 10 minute bake which also reduced the thickness by nearly 50nm. The effect diminishes with the third bake, causing the PR to shrink by 10nm, and the final 10-minute bake also reduces the film by approximately 10nm. This is equal to a reduction of 1nm per minute, and as such it is assumed that all the

solvent has evaporated at this point. After a total bake time of 40 minutes, the PR thickness reduced from 1950nm to 1502nm on average.

Following the 40 minute high temperature bake step, the wafers were then annealed at 750°C for 15 minutes with in an Annealsys AS-Master RTA tool a N_2 flow of 200sccm. The heating rate was controlled at $2°Cs^{-1}$ to prevent excessive thermal stress to the film, whilst the cooling rate was left uncontrolled. Post annealing, the wafers appeared with a black mirror-like appearance as expected for a graphite film. The capping layer thickness was measured by cross-sectional SEM at approximately 870nm, which can be seen in figure 6.8.

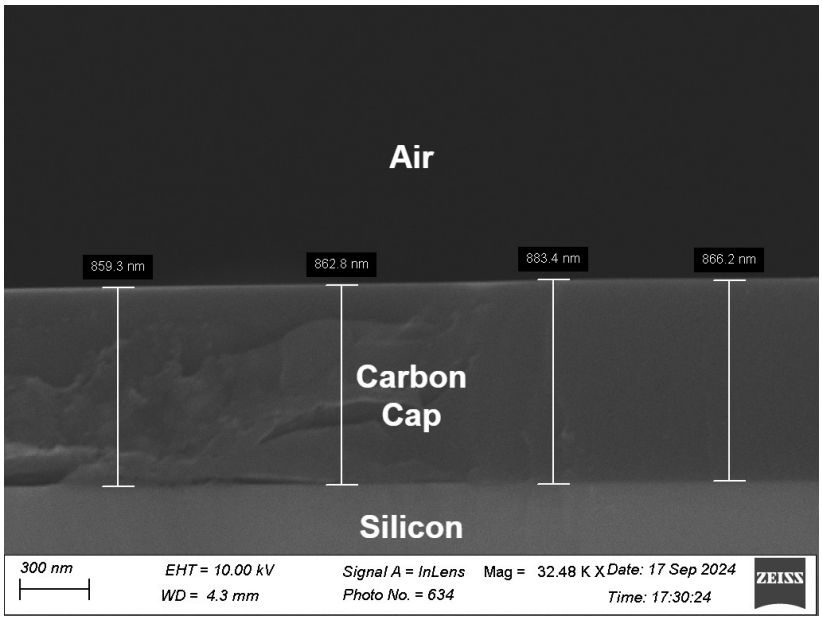


Fig. 6.8 Cross-sectional SEM image of the carbon cap formed on a silicon substrate after the conversion anneal. The average thickness of the layer is 870nm.

To ensure that this process could directly transfer to SiC, the above process was repeated for a SiC substrate. Due to the SiC substrate being transparent, ellipsometry was not used to measure PR thickness post-bake. The cross-sectional SEM image of the carbon cap formed is shown in figure 6.9. The average measured thickness of the carbon cap was 763nm, which is 107nm thinner compared to the cap formed on the silicon substrate using the same process. The difference in thickness is likely attributed to the substrates' different wettability, resulting in a thinner PR layer being formed during spin-coating on SiC, rather than any inconsistencies in the process itself.

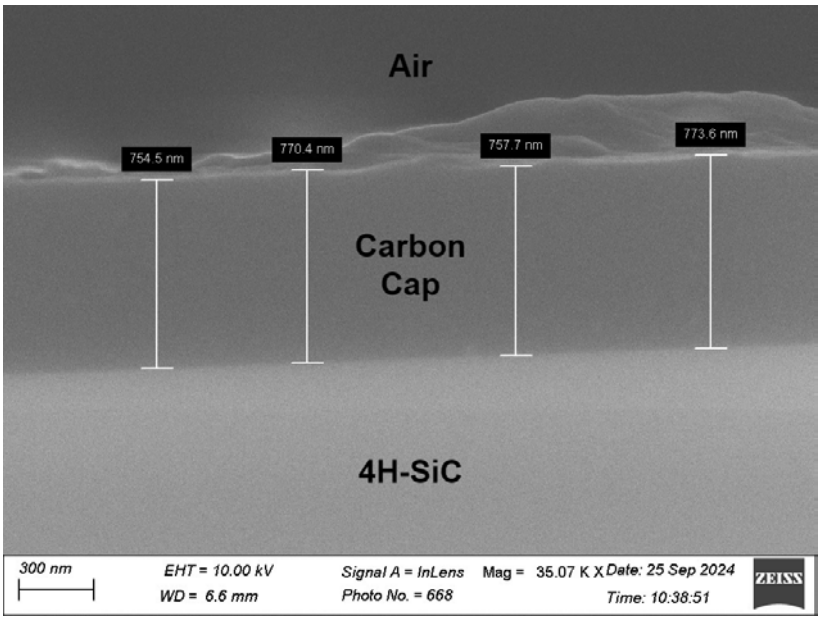


Fig. 6.9 Cross-sectional SEM image of the carbon cap formed on a SiC substrate after the conversion anneal. The average thickness of the layer is 763nm.

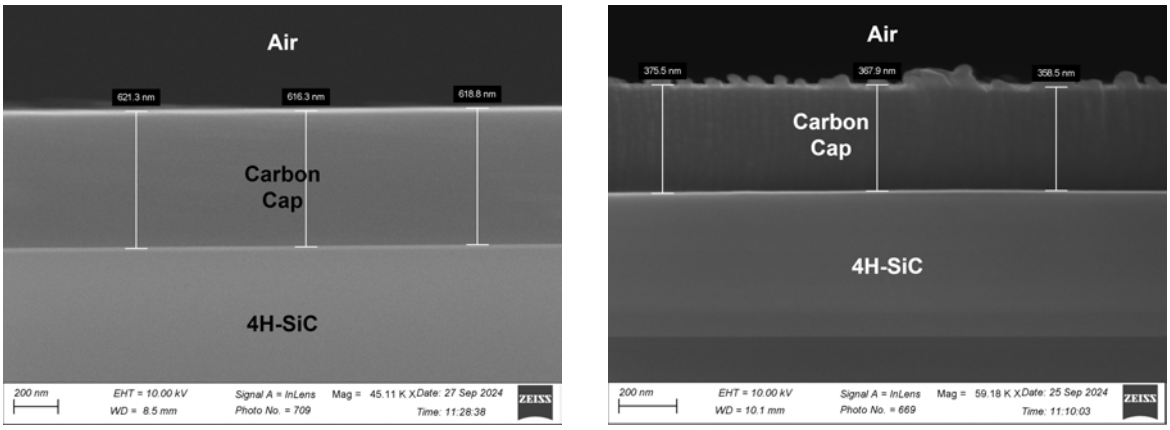
6.3.2 Carbon Cap Removal

After the implant activation anneal, the protective cap must be removed before subsequent processing steps i.e. deposition of metal contacts. Typically, this is achieved using dry oxidation at 900-1050°C for between 30 minutes to 4 hours [233, 239, 240]. However it also has been reported that an oxygen (O_2) plasma process can be used, offering a simpler and faster removal method which does not require the elevated temperatures needed for dry oxidation [241–243].

To achieve this, a plasma asher was used to subject the sample an O_2 plasma. To generate the plasma, an RF generator was set to a supply power of 150W. Different cleaved pieces of the carbon-capped SiC substrate used in the previous section were subjected to different O_2 plasma clean lengths to investigate the removal rate of this carbon cap. The thickness of the layers post O_2 plasma were found via cross-sectional SEM.

Figure 6.10 shows the cross-sectional SEM images of the carbon layer thickness on samples following a 2-minute and 5-minute plasma clean, respectively. The average thickness of the layer was 619nm after 2 minutes and 367nm after 5 minutes. Additionally, after 5 minutes the surface of the layer begins to exhibit roughening. After 10 minutes, the layer thickness varied locally between 34-77nm as seen in figure 6.11.

The remaining carbon layer thickness is plotted against O_2 plasma length in figure 6.12a. By taking the linear fit of the data points, the average removal rate was found to be 71 nm/min.



(a) (b)

Fig. 6.10 Cross-sectional SEM images of carbon cap thickness after (a) a 2 minute O_2 plasma and (b) a 5 minute O_2 plasma.

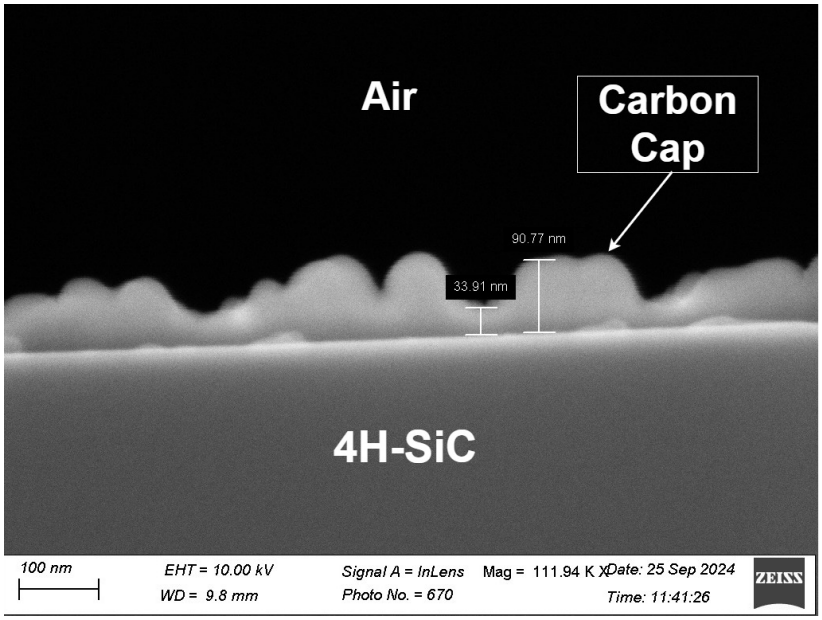
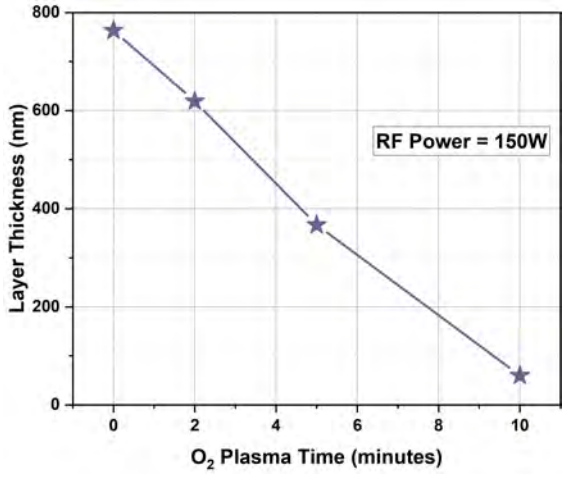


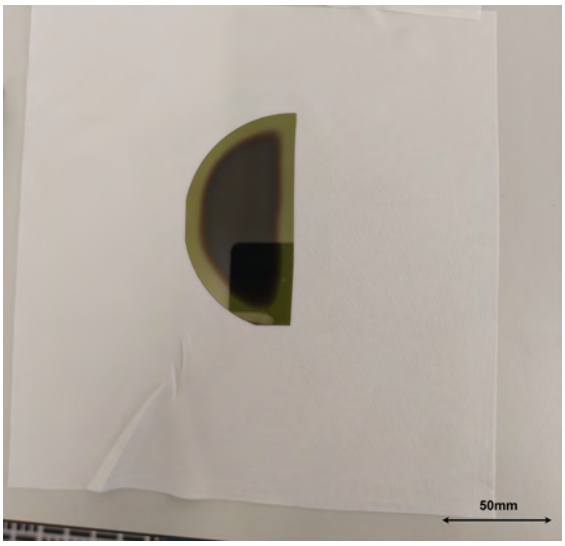
Fig. 6.11 Cross-sectional SEM of carbon cap after being subjected to a O_2 plasma for 10 minutes. Significant variation in thickness is observed. The average thickness was found to be 56nm.

It was also observed visually that remaining thickness of the carbon layer varied significantly across the sample. At the sample edge, the cap appeared to be completely removed, whilst the centre still appeared black, signifying that the layer was still present. This effect was replicated on half of the 100mm carbon-capped SiC substrate, as can be seen in figure 6.12b. Thus, to ensure that the carbon layer is completely removed from the whole wafer, a 20

minute O_2 plasma will be applied to the 100mm implanted 4H-SiC wafers in subsequent work within this chapter.



(a)



(b)

Fig. 6.12 (a) Carbon cap thickness plotted as a function of O_2 plasma time. The average removal rate is 71 nm/min. (b) Half the 100mm carbon-capped SiC substrate after being subjected to a 10 minute O_2 plasma. The layer has been completely removed from the extremities of the sample, but is still visible in the sample centre.

6.4 P-type Activation and Ohmic Contact Study

6.4.1 Fabrication Process

To optimise the P-type implant activation anneal, three 100mm N-type epitaxial SiC wafers were implanted by CuttingEdgeIons LLC. with aluminium dopants [244] at 500°C. This created a 150nm box-profile of P-type material on the wafer surfaces, with an aluminium concentration of $\geq 1.5 \times 10^{20} cm^{-3}$. The total implant dose was $3 \times 10^{15} cm^{-3}$, with implantation energies of 10keV, 40keV, 80keV and 120keV. The corresponding dose ratios were 0.06, 0.2, 0.3 and 0.44, respectively. The details of these implants can be found in table 6.1. The resultant profile of the implanted aluminium ions was simulated using SRIM [160], which can be seen in figure 6.13. Good agreement between SRIM simulations and Secondary Ion Mass Spectrometry (SIMS) measurements have been observed for implanted SiC [245].

Following implantation, the three wafers underwent the carbon capping procedure described in section 6.3 of this chapter. Implant activation anneals were subsequentially

Table 6.1 Implant specification used to form a 150nm box profile with $N_a \geq 10^{20}$ using aluminium. The total implant dose used was $3 \times 10^{15} cm^{-3}$.

	10keV	40keV	80keV	120keV
Fraction	0.06	0.2	0.3	0.44
Dose	1.8×10^{14}	6×10^{14}	9×10^{14}	1.3×10^{15}

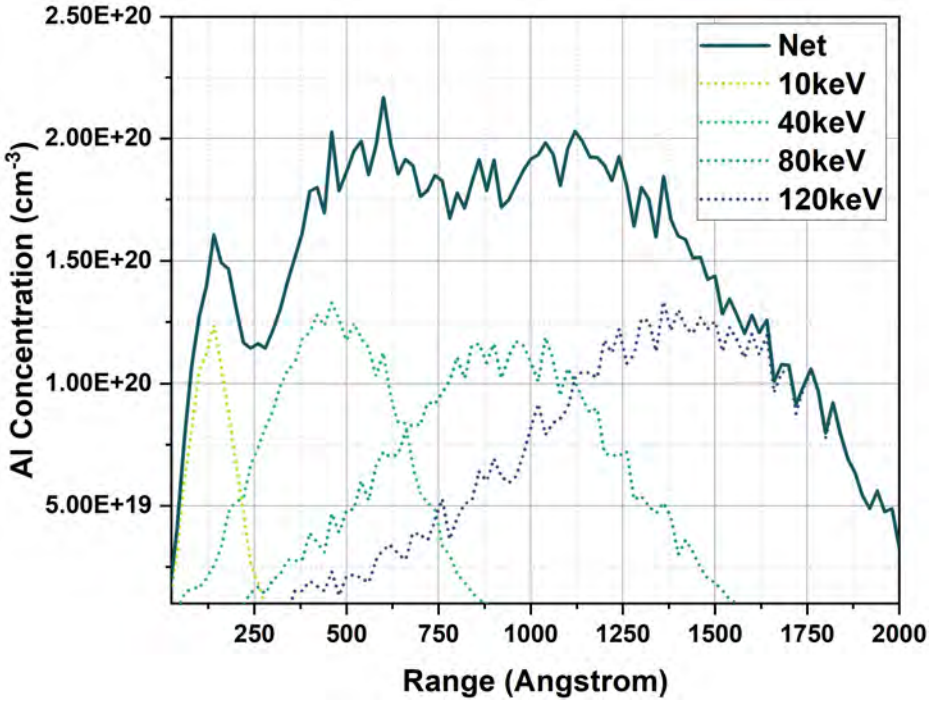


Fig. 6.13 Resulting simulated aluminium doping profile calculated using SRIM for the implant scheme in table 6.1.

completed at IMB CNM Barcelona in a Centrotherm Activator furnace. The wafers were annealed individually: one at 1600°C , another at 1650°C and the third at 1700°C. The anneals were performed in an argon ambient, with a duration of 20 minutes once the target temperature was reached for all three wafers.

After annealing, the carbon caps were removed on the wafers by a 20 minute O_2 plasma, following the process described in section 6.3.2. The wafers were then diced into 15mm square pieces using a DISCO dicing tool. To remove any remaining organic contaminants, and to ensure the SiC surface is properly prepared for deposition of contact metals, the diced samples were subjected to a full Radio Corporation of America (RCA) clean. The step-by-step procedure of this chemical clean can be found in Appendix B.

Following the RCA clean procedure, CTLM structures were formed on select samples by depositing either Ti/Al or Ti/Al/Ni metal stacks were deposited on the sample surface using a Moorfield Minilab 080 e-beam evaporation tool. The thickness of these stacks were 50nm/140nm and 80nm/350nm/50nm, respectively as per [246, 247]. Subsequentially, the metal was patterned using a metal lift-off procedure. Following this, samples were subjected to a contact anneal in an Argon ambient at a temperature ($T_{contact}$) between 1000-1100°C for 2 minutes to ensure the contacts followed Ohmic behaviour.

6.4.2 Hall Characterisation Results

Van der Pauw and Hall measurements were performed using soldered indium contacts placed at each corner of the samples with a Linesis HCS-1 system. Samples were taken from each of the three wafers annealed at different temperatures. The sheet resistance, carrier concentration and mobility at room temperature (RT) were measured at the three different activation anneal temperatures are shown in table 6.2.

Table 6.2 Summary of parameters extracted from both VDP and Hall measurements at RT on aluminium P-type implanted samples annealed at three different temperatures: 1600°C, 1650°C and 1700°C.

Activation Anneal Temperature (°C)	R_{sh}(Ω/sq)	ρ (Ωcm)	p (cm^{-3})	μ_H (cm^2/Vs)
1600	38500	0.578	2.45×10^{17}	44.1
1650	21800	0.326	7.35×10^{18}	26
1700	15400	0.231	1.15×10^{18}	23.5

The sheet resistance drops significantly as T_{anneal} increases, from 38.5kΩ/sq at 1600°C to 21.8kΩ/sq at 1650°C. A smaller reduction in R_{sh} is observed between 1650°C and 1700°C, where R_{sh} is 15.4kΩ/sq. The Arrhenius plot of the sheet resistance as a function of T_{anneal} is shown in figure 6.14. The activation energy E_A was found to be 0.93±0.11eV, which agrees with the value reported in [1]. Using R_{sh} values, the corrected hole concentration p (using r_H= 0.5) was found to be $2.45\times10^{17}cm^{-3}$, $7.35\times10^{18}cm^{-3}$ and $1.15\times10^{18}cm^{-3}$ for each of the T_{anneal} temperatures, respectively.

The carrier mobility decreases from $44.1cm^2/Vs$ at 1600°C to $23.5cm^2/Vs$ at 1700°C, which agrees with reported values for similar implantation doses and T_{anneal} conditions [1]. At T_{anneal}= 1700°C , mobility degrades further to $23.5cm^2/Vs$. The reduction of μ_p with T_{anneal} is consistent with an increased proportion of active Al acceptors, which results in

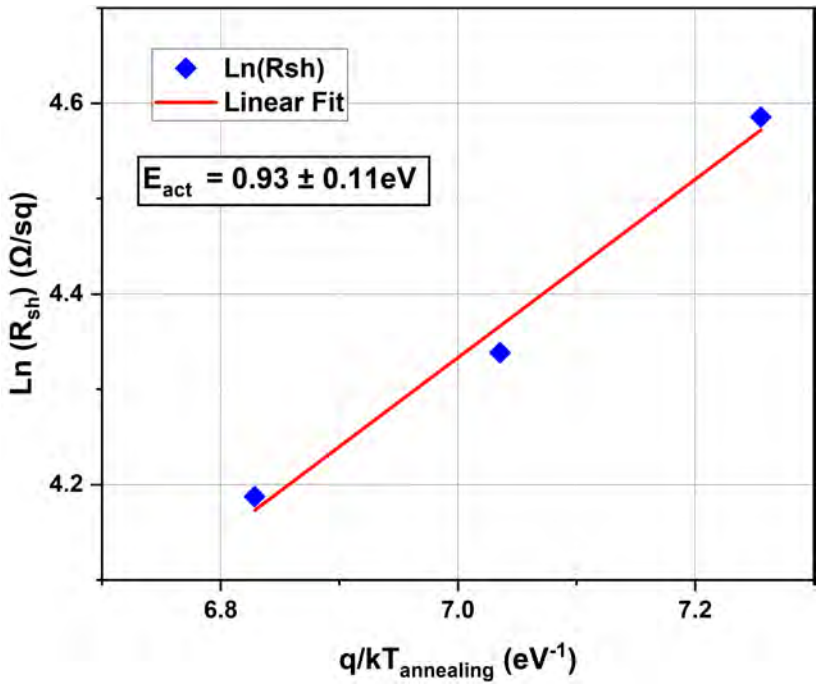


Fig. 6.14 Arrhenius plot of sheet resistance as a function of activation anneal temperature for implanted aluminium P-type. Sheet resistance reduces with T_{anneal}, indicating improved activation of implanted ions.

elevated impurity scattering. Both hole concentration and mobility are plotted as a function of T_{anneal} in figure 6.15.

6.4.3 Ohmic Contact Results

Current Transport Mechanisms in P-type Ohmic Contacts

An Ohmic contact at a metal-semiconductor interface will result in a linear I-V characteristic. An ideal Ohmic contact would have no potential barrier at the interface; however in practice a potential barrier is always present. Despite this, contacts can exhibit ohmic behaviour due to various carrier transport mechanisms at the interface.

There are two different mechanisms by which carriers can pass between the metal and semiconductor: carriers being thermally excited over the top of the barrier (Thermionic Emission) and carriers tunnelling through the barrier (Field Emission). Thermionic emission (TE) occurs due to the thermal energy of electrons, and is the dominant transport mechanism when doping is low, and at high temperatures [248].

When the doping concentration is high, as it is in this work, the depletion region is narrow on the semiconductor side of the contact. Therefore, carriers can tunnel through the

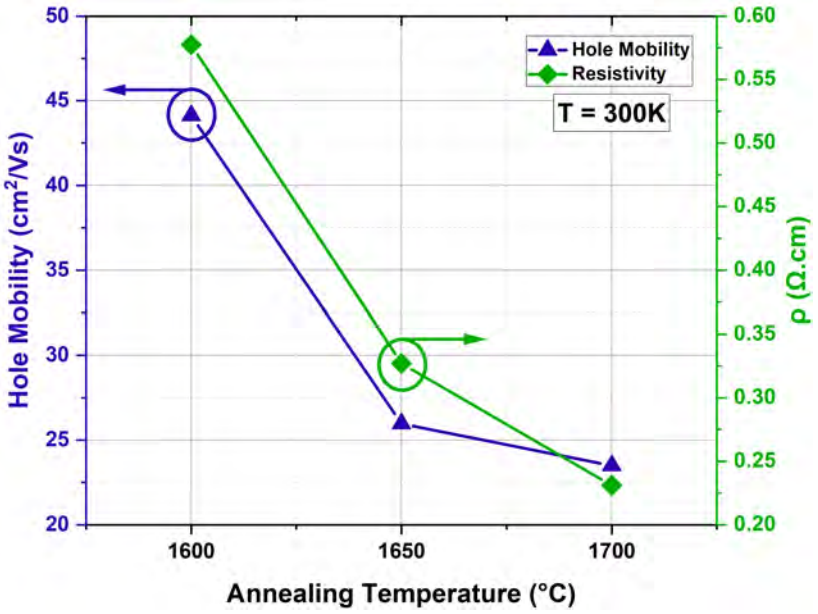


Fig. 6.15 Resistivity and hole mobility plotted as a function of annealing temperature. The reduction in μ_p and ρ is further supports that more active aluminium dopants are present when annealing at higher T_{anneal} temperatures.

potential barrier relatively easily [248]. The field emission (FE) process, when coupled with TE reduces the voltage drop across the contact, and causes the contact to be Ohmic in nature. The transport mechanism which is dominant is dependant on the doping concentration of the semiconductor (N_a), and is closely related to the characteristic energy (E_{00}) [249]:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_a}{m^*\varepsilon_s}} \tag{6.18}$$

Where $\hbar$ is Planck's constant h divided by 2π, and m^* is the effective mass of the tunnelling hole and ε_s is the dielectric constant of the semiconductor. Figure 6.16 plots E_{00} as a function of N_a [250]. As E_{00} increases, the probability of tunnelling occurring rises. Typically, the ratio $\frac{kT}{E_{00}}$ is used to indicate the dominant transport mechanism. When $\frac{kT}{E_{00}} \geq 1$, TE prevails. Conversely, if $\frac{kT}{E_{00}} \approx 1$, the contribution of the processes are comparable and the dominant mechanism of current flow is due to electrons with some thermal energy tunnelling through the centre of the potential barrier [249]. This phenomenon is referred to as Thermionic Field Emission (TFE) and has been identified as the primary transport mechanism in P-type Ohmic contacts to 4H-SiC [191, 251, 252]. Lastly, when $\frac{kT}{E_{00}} \leq 1$, then FE becomes the dominant mechanism.

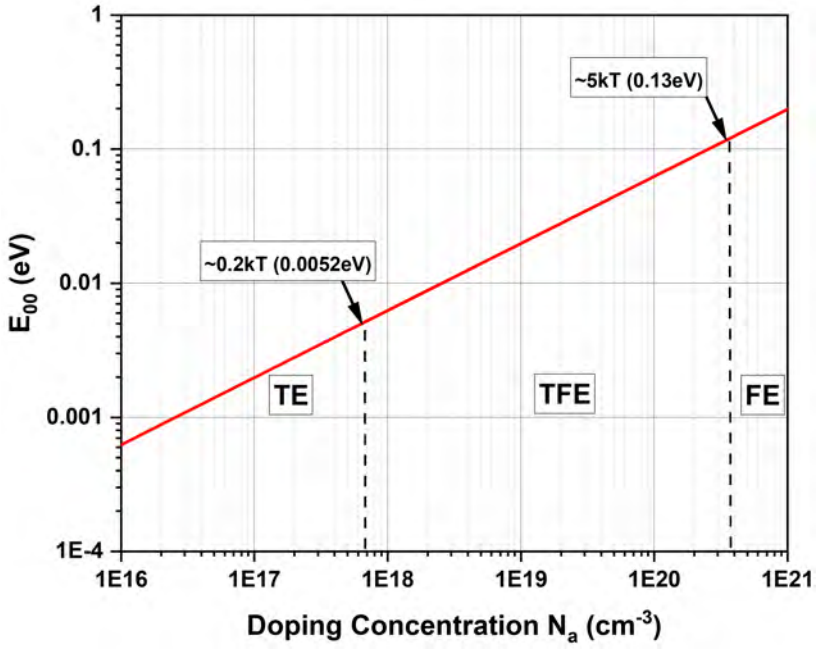


Fig. 6.16 E_{00} plotted as a function of N_a for 4H-SiC. As doping concentration increases, carrier transport by field emission rises. However, for the majority of N_a values typically used to form ohmic contacts, a mixture of FE and TE is expected to occur (TFE).

Activation Anneal Temperature

As has discussed previously and demonstrated in the Hall results presented, increasing activation anneal temperature (T_{anneal}) results in a greater proportion of active aluminium dopants. The specific contact resistance (ρ_c) when TFE transport mechanism dominates can be expressed using equation 6.19, where ϕ_b is Barrier Height and V_n is the position of the Fermi level. Therefore, if the doping concentration in the layer increases (i.e.$\frac{kT}{E_{00}}$ reduces) then ρ_c should also reduce. To verify this, samples from each wafer were patterned CTLM structures with the Ti/Al metal stack which were annealed at 1000°C.

$$\rho_c(TFE) = \frac{kT}{qA^*}\frac{kT}{\sqrt{\pi(\phi_b + V_n)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\left[\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\right]\exp\left(\frac{\phi_b + V_n}{E_0} - \frac{V_n}{kT}\right) \quad (6.19)$$

Figure 6.17 presents the extracted R_{sh} and ρ_c values for the three T_{anneal} conditions. As anticipated, ρ_c decreases notably from $8.66 \times 10^{-3}\Omega cm^{-2}$ at T_{anneal}= 1600°C to $5.61 \times 10^{-3}\Omega cm^{-2}$ and $4.25 \times 10^{-3}\Omega cm^{-2}$ at 1650°C and 1700°C, respectively. Additionally, sheet resistance (R_{sh}) also reduces significantly, from 56.6kΩ/sq at 1600°C to 33.3kΩ/sq at 1650°C and 23.7kΩ/sq at 1700°C.

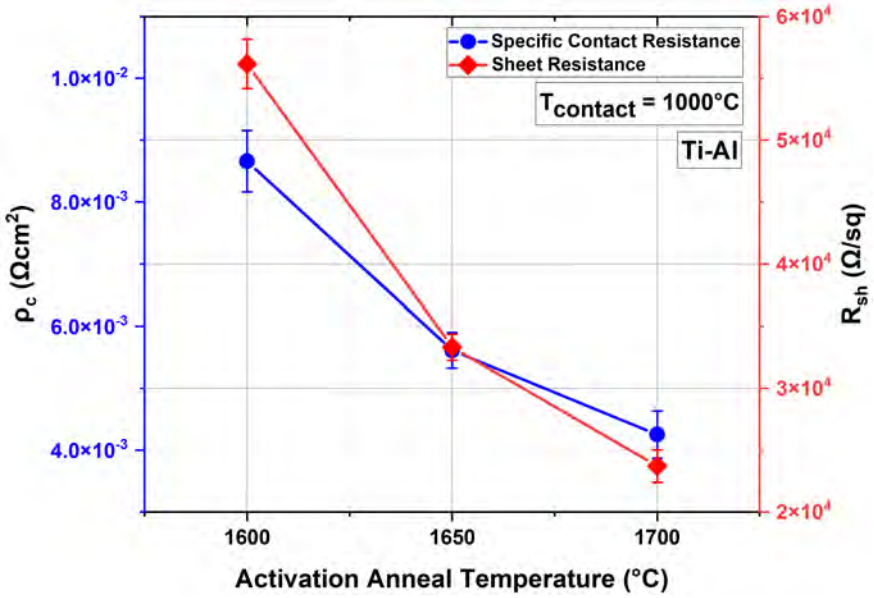


Fig. 6.17 Sheet resistance and ρ_c plotted as a function of T_{anneal} as calculated from CTLM measurements. Both ρ_c and R_{sh} reduce at higher T_{anneal}, indicating improved activation of aluminium dopants at higher temperatures.

The R_{sh} values derived from CTLM measurements are between 8.3-17.6kΩ/sq larger than results of Hall measurements. This difference between the two methods can partially be attributed to R_{sh} not being identical under the contacts and between contacts, which cannot be isolated in CTLM structures [190, 226]. Sheet resistance can vary under contacts due to silicides which form at the surface, including Ti_3SiC_2 for titanium based 4H-SiC contacts such as the ones used in this work [251, 253]. The formation of these silicides has been identified as the key mechanism of ohmic contact formation to 4H-SiC [193, 254, 255]. On the other hand, this does not have to be considered in Hall measurements to find R_{sh}.

Nevertheless, the results in figure 6.17 qualitatively align with the Hall measurement data, with both methods indicating that the highest T_{anneal} of 1700°C yields the largest fraction of electrically active implanted aluminium dopants.

Contact Anneal Temperature

The temperature at which the deposited contacts are anneal has been observed to be the most influential parameter when optimising the ρ_c of Ohmic contacts to P-type SiC [194]. Therefore, samples taken from the wafer annealed at 1700°C were used to find the optimum metal contact anneal temperature ($T_{contact}$) for both Ti/Al and Ti/Al/Ni metal stacks. The temperatures tested were 1000°C, 1050 °C and 1100 °C whilst the anneal length remained constant at 2 minutes. All anneals were carried out in an argon ambient.

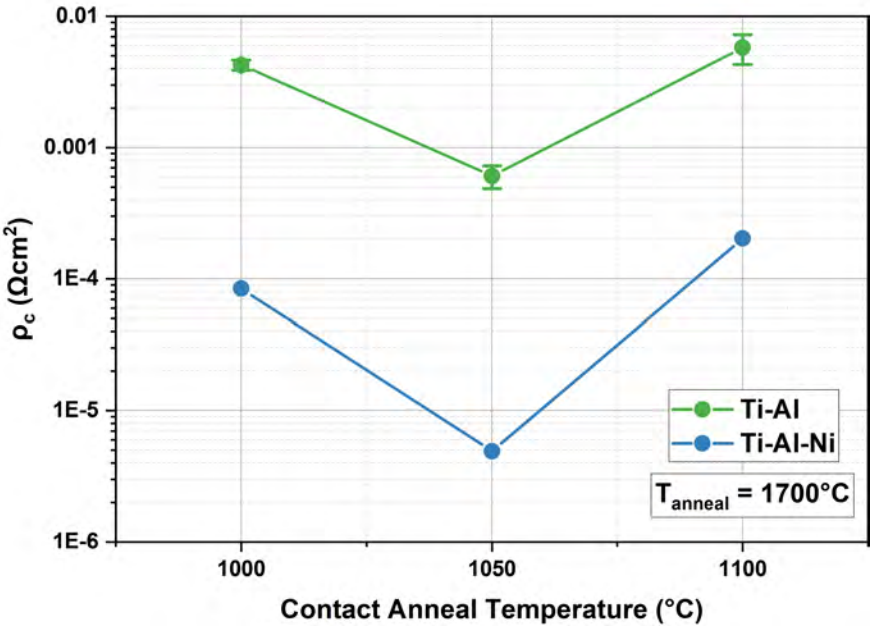


Fig. 6.18 Specific contact resistance plotted as a function of $T_{contact}$ for both Ti/Al and Ti/Al/Ni samples. The Ti/Al/Ni metal stack achieves significantly lower ρ_c values for all anneal temperatures.

Figure 6.18 shows ρ_c as a function of $T_{contact}$ for both metal stacks tested. The Ti/Al metal stack exhibited a ρ_c of $4.25 \times 10^{-4} \Omega cm^{-2}$ at 1000°C , while ρ_c values of $6.07 \times 10^{-4} \Omega cm^{-2}$ and $5.77 \times 10^{-3} \Omega cm^{-2}$ were measured at 1050°C and 1100°C, respectively. The best ρ_c value found for the Ti/Al stack remains an order of magnitude higher than was reported by Tang et al. [246], indicating further optimisation is required for this metal stack.

Comparatively, the Ti/Al/Ni metal stack outperformed the Ti/Al stack across all $T_{contact}$ conditions used, with at least an order of magnitude improvement. Specifically, a ρ_c of $8.45 \times 10^{-5} \Omega cm^{-2}$ was measured at 1000°C , whilst $\rho_c = 4.91 \times 10^{-6} \Omega cm^{-2}$ at 1050°C, and $2.03 \times 10^{-4} \Omega cm^{-2}$ at 1100°C. The best performing contact at 1050°C has a ρ_c comparable to the values reported by Fedeli et al. for the same metal stack [247]. In contrast, annealing at 1100°C yields the poorest ρ_c for both metal stacks.

6.4.4 Temperature Dependence of Ohmic Contacts

By repeating the CTLM measurements at elevated temperature, it is possible to elucidate the temperature dependence of R_{sh} and ρ_c. The relationship between these parameters and temperature allow determination of additional key properties of the aluminium implanted layer, and the ohmic contact. Specifically, the ionization energy (E_{ion}) of aluminium dopants, the active doping concentration N_a and the contact barrier height ϕ_b.

Sheet Resistance

As explained in detail in section 6.2.2, it is possible to estimate the ionization energy (E_{ion}) by utilizing the temperature dependence of $R_{sh}(T)$. Typically, this method is used for Hall measurements at elevated temperatures, but it can also be applied to CTLM measurements.

Therefore, an E_{ion} value can be determined from the slope of the linear fit to the plot of $\ln(R_{sh})$ versus $\frac{q}{kT}$. Figure 6.19 shows this plot for each of the activation temperatures, alongside their respective linear fits. The extracted E_{ion} were found to be 127.6meV, 117.8meV and 113.1meV for T_{anneal}= 1600°C, 1650°C and 1700°C, respectively.

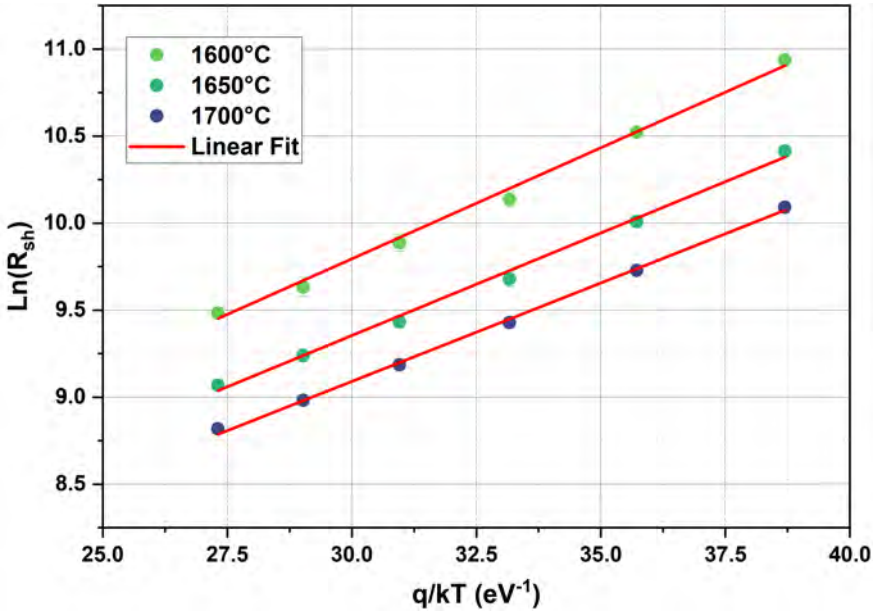


Fig. 6.19 Arrhenius plots of R_{sh} for each of the three activation anneals. Data from all three samples gives a good linear fit. It is found that E_{ion} reduces as $T_{contact}$ rises, indicating improved activation of dopants.

For Hall measurements by finding E_{ion} and $p(T)$, it is possible to fit to the neutrality equation to find N_a. This is not possible when using CTLM measurements, as p can not be extracted. Here it is proposed that an alternative, approximate method may be used to find N_a. The dependence of E_{ion} on the acceptor concentration N_a can be described by equation 6.20 [256], where E_0 is the ionization energy for an isolated impurity centre for aluminium equal to 216meV, and α is material dependant fitting parameter equal to $3 \times 10^{-5} meV cm^{-1}$ [1].

$$E_{ion} = E_0 - \alpha N^{\frac{1}{3}} \tag{6.20}$$

It has been shown that equation 6.20 is in good agreement with N_a values found from both Hall and TLM measurements for P-type implanted 4H-SiC. This is visualized in figure

6.20 below, which plots equation 6.20 alongside reported E_{ion} values in existing literature determined by Hall [1, 257, 258] and TLM measurements [191].

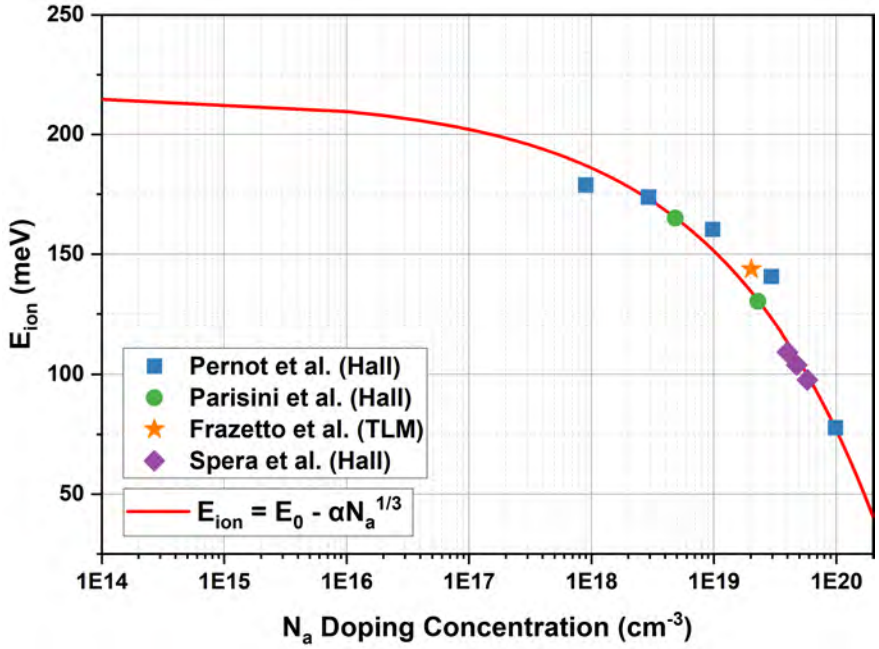


Fig. 6.20 Ionization energy of aluminium acceptors in 4H-SiC as a function of N_a determined by Hall and TLM measurements from existing literature. The solid line corresponds to the expression for E_{ion} as a function of N_a which is presented in equation 6.20, using E_0 = 216meV and α= 3×10^{-5}meVcm^{-1}.

Therefore, equation 6.20 may be used to find approximate N_a values corresponding to the E_{ion} results derived from figure 6.19. Using this method, the N_a values are found to be $2.56 \times 10^{19} cm^{-3}$, $3.51 \times 10^{19} cm^{-3}$ and $4.04 \times 10^{19} cm^{-3}$ for T_{anneal}= 1600°C, 1650°C and 1700°C, respectively. Assuming that the implanted P-type doping profile is a uniform 150nm thick layer with N= $1.5 \times 10^{20} cm^{-3}$, this results in aluminium activation rates of 17%, 23.4% and 26.9%.

Table 6.3 presents all the results found in this section and compares them to previously reported work on aluminium implanted 4H-SiC. It is noted that the activation ratios reported in existing literature is higher than has been found in this work, however it should be noted that to the best of the authors knowledge, no current literature has attempted to estimated Al activation rates by using CTLM data. Therefore, the difference in values can be attributed to a number of reasons discussed below.

Firstly as previously mentioned when using the CTLM method it is not possible to account for R_{sh} varying underneath metal contacts, due to the formation of silicides during the contact anneal process. This introduces an element of error into the R_{sh} values found

Table 6.3 The combined results of ionization energy E_{ion}, approximated N_a and Al activation percentage for aluminium implanted samples annealed at 1600°C, 1650°C and 1700°C.

Reference	Measurement	Implanted conc. (cm^{-3})	T_{anneal}	E_{ion} (meV)	N_a (cm^{-3})	Al Activation
This Work	CTLM	1.5×10^{20}	1600°C	127.6	2.56×10^{19}	17%
This Work	CTLM	1.5×10^{20}	1650°C	117.8	3.51×10^{19}	23.4%
This Work	CTLM	1.5×10^{20}	1700°C	113.1	4.04×10^{19}	26.9%
[1]	Hall	1×10^{20}	1675°C	110	3.87×10^{19}	39%
[258]	Hall	3.33×10^{19}	1670°C	162	1.7×10^{19}	51%

during CTLM measurements. This can be rectified by using linear TLMs, where it is possible to isolate the difference in R_{sh} underneath contacts.

Secondly, the approximate N_a values in this work have been found from the E_{ion}-N_a relationship shown in figure 6.20. It has been shown that α and E_0 can vary depending on the data which is being fitted from existing measurements [229]. Therefore, the approximate values of N_a are found in this work are dependant on the E_0 and α values used. For example, if E_0 was increased, the approximate N_a values and subsequentially aluminium activation percentage would significantly increase.

Finally, when using temperature dependant Hall measurements to find E_{ion}, it is standard to fit to the neutrality equation which enables calculation of N_a, E_{ion} but also compensating donor concentration N_d. This compensation has been found to be significant, reaching 9.4% of the implanted concentration by Spera et al. [1]. Due to the approximate method used in this work, it is not possible to account for N_d, which likely results in an underestimation in N_a and Al activation ratio.

Specific Contact Resistance

As samples are subjected to elevated temperature, both R_{sh} and ρ_c will vary. Sheet resistance will drop as progressively more aluminium dopants become ionized, whilst ρ_c will also reduce according to equation 6.19. Furthermore, by fitting the measured ρ_c data to equation 6.19, repeated here for convenience, it possible to estimate active dopant concentration (N_a) and the barrier height of the contact (ϕ_b).

$$\rho_c(TFE) = \frac{kT}{qA^*}\frac{kT}{\sqrt{\pi(\phi_b+V_n)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\left[\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\right]\exp\left(\frac{\phi_b+V_n}{E_0}-\frac{V_n}{kT}\right) \quad (6.21)$$

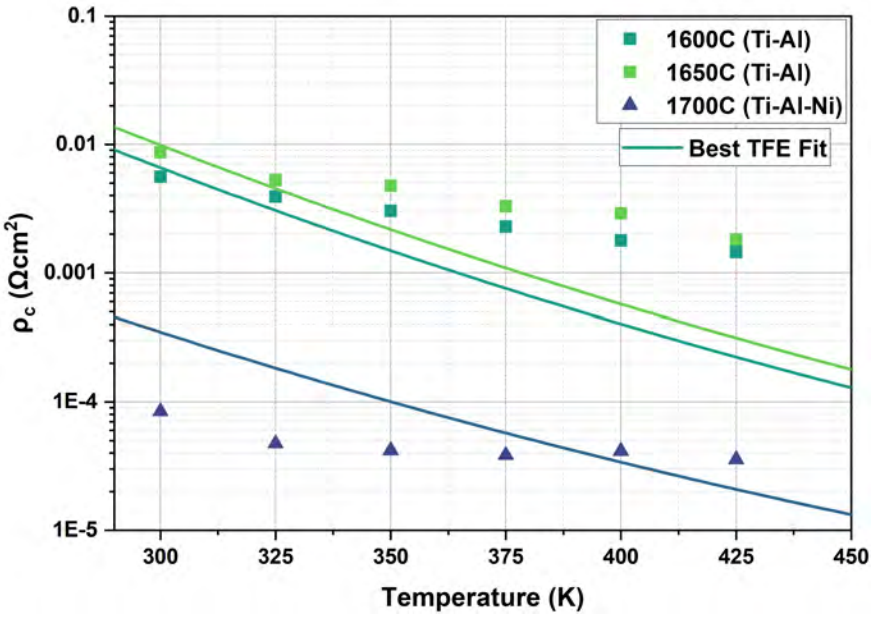


Fig. 6.21 Specific contact resistance plotted as a function of measurement temperature, for all three T_{anneal} temperatures. The Thermionic Field Emission equation is fitted to the data using N_a values from the previous section. The TFE fit to all three sets of data is poor, indicating that TFE may not be the primary transport mechanism across the contact.

Figure 6.21 plots ρ_c as a function of temperature, for all three T_{anneal} values. At T_{anneal}= 1600°C, ρ_c drops from $8.66\times10^{-3}\Omega cm^{-2}$ at RT to $1.82\times10^{-3}\Omega cm^{-2}$ at 150°C. Similarly, for T_{anneal}= 1650°C SCR is reduced from $5.61\times10^{-3}\Omega cm^{-2}$ at RT to $1.45\times10^{-3}\Omega cm^{-2}$ at 150°C.

In contrast, the T_{anneal}= 1700°C exhibits a different trend. The ρ_c initially reduces from $8.45\times10^{-5}\Omega cm^{-2}$ at RT to $4.75\times10^{-5}\Omega cm^{-2}$ at 50°C, but remains nearly constant with further temperature increases, only reaching ρ_c= $3.57\times10^{-5}\Omega cm^{-2}$ at 150°C.

Also shown in figure 6.21 is the provisional best fit of the TFE equation for each T_{anneal}. Since N_a was approximated in the previous section, the only fitting parameter used was ϕ_b. However, when fitting equation 6.19 to the experimental data, it is clear that the results of all three T_{anneal} samples do not fit well to the TFE equation. In particular, ρ_c does not decrease as drastically with temperature as predicted by the TFE mechanism. Furthermore, it is found that ρ_c reduces less with temperature at higher T_{anneal}, resulting in a poorer fit for T_{anneal}= 1700°C than T_{anneal}= 1600°C for example. This also suggests that the transportation mechanism being observed is possibly Field Emission.

As discussed previously, by definition the TFE mechanism is a combination of thermionic and field emission occurring with equal probability. However as doping concentration N_a increases, FE becomes increasingly dominant. The weak temperature dependence observed, combined with the high N_a values ($\geq 2\times10^{19}cm^{-3}$) in the P-type layer, suggests a transition

towards field emission as the primary transport mechanism across the potential barrier. This is further supported by the sample annealed at 1700°C, which has the highest N_a value and shows the minimal temperature dependence, indicating that FE is becoming more progressively more dominant.

6.5 Conclusion

In this chapter, work has been presented on carbon capping layers, P-type activation anneals and P-type Ohmic contacts. This included the process development of carbon caps, alongside Hall and CTLM measurements on aluminium-implanted 4H-SiC wafers which were used to optimize T_{anneal} and $T_{contact}$.

CTLM structures were successfully fabricated on samples subjected to different T_{anneal} temperatures, with all designs exhibiting ohmic behaviour after contact annealing. It was found that R_{sh} reduces as T_{anneal} rises, which is attributed to improved activation of implanted aluminium dopants. This trend was successfully replicated by Hall measurements.

It was found that the optimum $T_{contact}$ was 1050°C to minimize ρ_c on both metal stacks tested. The Ti/Al/Ni metal stack exhibited an impressive result of $\rho_c = 4.91 \times 10^{-6} \Omega cm^2$, which is close to the best value reported by Fedeli et al. [247].

Finally, CTLM measurements repeated at elevated temperature allowed calculation of E_{ion} and subsequentially approximate activation rates of implanted dopants. To the best of the authors knowledge, this is the first time approximate activation rates have been reported using CTLM data for 4H-SiC. The best value found was 26.9% activation at T_{anneal}= 1700°C , which is lower than has been reported for similar temperatures using temperature-dependent Hall measurements. This is likely due to the approximate nature of the CTLM method used, compared to the greater precision of Hall measurements.

Overall, a low ρ_c ohmic contact process has been successfully developed, which will be essential for full JFET fabrication. Furthermore, it has been verified that a high activation anneal temperature above 1650°C is required to achieve acceptable activation rates of implanted aluminium dopants.

Chapter 7

Conclusion and Future Work

In this final chapter, comprehensive conclusions drawn from the research contained in this thesis is summarized. The key findings are highlighted, and potential areas of future work are discussed , aiming to further advance the state-of-the-art in 4H-SiC JFET technology.

7.1 Conclusion

The primary aim of this thesis is to explore the integration of SiC JFETs into cascode-based circuit protection products, particularly the Bourns TBU product line which currently utilise silicon MOSFETs. Due to the material benefits of 4H-SiC compared to silicon, power consumption of these products is expected to significantly reduce by utilising 4H-SiC JFETs. This is anticipated to improve TBU performance, and unlock opportunities in new markets for the product-line.

From a device design viewpoint, it is important to identify the primary sources of resistance in the JFET cell structure. From the analytical discussion in Chapter 2 [put chapter labels in?], it was determined that drift and JFET region resistance dominate at all voltages between 200-3300V. Additionally, the benefit of including a carrier storage layer was shown, preventing JFET region resistance and threshold voltage from varying with breakdown voltage.

As the target value for threshold voltage for the TBU was -3V, it was also discovered that V_{th} is incredibly sensitive to the JFET region width. Chapter 3 investigated this in detail using TCAD simulations, presenting the relationship between V_{th}, doping concentration and JFET region width. It was also found that the length of the JFET region plays a crucial role in the off-state performance of the device, as short channel lengths lead to extremely premature breakdown caused by DIBL. Introduction of P-type implants to the JFET sidewall was shown to substantially improve breakdown performance, whilst having minimal impact

on V_{th} and R_{on}. Furthermore, the design of floating field ring edge termination structures was optimised to achieve near ideal breakdown voltage. These termination structures can be formed simultaneously with the gate P+ junction, reducing the complexity and cost of the JFET fabrication process.

The following chapter built upon the findings of Chapter 3 by proposing a novel JFET design with a monolithically integrated temperature sensor consisting of a lateral P-type resistor. This design can be used to enhance the TBU by enabling real-time condition monitoring at the device level, allowing customers to accurately predict device lifetimes and monitor safe operating areas. Electrothermal TCAD simulations were employed to evaluate the sensors response to device self-heating, while an analytical model of the sensor was also developed, demonstrating excellent agreement with the TCAD simulations.

Chapter 5 investigated the how material defects in 4H-SiC wafers may impact the performance of unipolar devices, specifically SBDs. This work successfully fabricated Ni SBDs across the entirety of two defect mapped 150mm wafers, which were characterized on a semi-automated probe state and subsequentially analysed using Python code developed during this Thesis. No strong correlation was observed between the location of defects and the device characteristics, indicating that defects such as SFs may not degrade the performance of unipolar devices such as SBDs or JFETs. However, the yield of acceptable diodes across these wafers was found to require significant improvement.

Finally, to fabricate future 4H-SiC JFET prototypes it is key to develop optimized processes for the different steps in the full fabrication process. Two of the most important of individual steps are the activation annealing of the aluminium-implanted gate regions, and subsequentially gate Ohmic contacts to the implanted region. It was found that the highest activation anneal temperature of 1700°C resulted in the greatest proportion of aluminium dopants being electrically active - 26.8%. Furthermore, it was found that the Ti/Al/Ni annealed at 1050°C metal stack resulted in the best Ohmic contact, with $\rho_c = 4.61 \times 10^{-6} \Omega cm^2$ which is comparable to existing literature. It was also found that the behaviour of these contacts did not follow Thermionic Field Emission model as expected, indicating that contacts fabricated might be approaching the threshold where Field Emission is the dominant current transport mechanism.

7.2 Future Work

In this section, potential areas of future research are identified and discussed. Although 4H-SiC JFETs are commercial devices, there remains significant scope for improving the understanding of device operation and enhancing device design.

7.2.1 Simulation

The simulations of the JFET used to optimize cell and edge termination design were extensive. However there were two areas which in the future could be used investigated to provide more comprehensive analysis: 3D simulations and transient simulations.

As most of the simulations in this work are 2D, 3D effects which occur at corners of the device have been ignored - particularly at the edges of the termination structures. By utilising 3D simulations, more robust optimisation of the termination structures could be achieved, such as the optimal radius of curvature for FFRs. Another 3D simulation study which would be beneficial would be to model the ends of JFET mesa stripes, to ensure that V_{th} is not adversely affected at the end of the mesa.

Transient simulations are also an incredibly important to ensure a complete picture of device performance. Although a JFET implemented in a TBU will be in the on-state ≥99%, only switching off during a over-current/voltage event, it is also important to ensure the JFET switches off and back on in a timely manner. Furthermore, the transient simulations can be further expanded to incorporate electrothermal models used in Chapter 4 to consider device self-heating. Transient simulations can be applied to not only the JFET unit cell, but also the integrated sensor design proposed in Chapter 4, to verify that the sensor's robustness under transient switching conditions.

Finally, another aspect of future simulation work is to calibrate the TCAD process simulation to devices fabricated in the Swansea University cleanroom. This can be achieved using the Synopsys TCAD "AdvancedCalibration" library, to tune ion implantation and dry etching models to accurately replicate real processes carried out in the cleanroom. A simulation model calibrated to the actual fabrication process would enable incredibly precise predictions of how natural variations in the process i.e. plasma densities in dry etch tools would influence device performance.

7.2.2 Fabrication and Characterisation

The fabrication progress made in this thesis is substantial, including the development of the first P-type Ohmic contact process and the fabricating the first full 150mm 4H-SiC wafers processed in the Swansea University cleanroom. However, the most significant scope for further fabrication work is evident - the fabrication of full 4H-SiC JFET devices using the optimised cell and termination design found using TCAD. This would enable a working TBU demonstrator using a 4H-SiC JFET could be built, and tested to realise to potential efficiency improvements.

Specifically, by fabricating 4H-SiC JFETs further work would include optimisation of a number of different process steps, namely: dry etching to produce JFET mesas, N-type Ohmic contacts and passivation opening to form contact pads. This would involve multiple different studies using a combination of physical (SEM, AFM) and electrical (CTLM) methods to qualify these processes. In particular, a study on ohmic contacts to N-type 4H-SiC using the Ti/Al/Ni metal stack found to be the best choice for P-type material would be of use, as formation of simultaneous P and N-type ohmic contacts would enable a single mask layer to be used, as intended in the provisional fabrication process set out in this thesis.

Subsequentially, characterisation of the JFET devices will elucidate the relationship between V_{th}, V_{br} and R_{on} with JFET mesa width. Specifically, investing the JFET off-state behaviour would be valuable for assessing off-state leakage as a function of mesa width. By characterising the relationship between the chosen design parameters and device performance, it would be possible to evaluate the feasibility of mass manufacture of the JFET designed in this work in terms of reproducibility i.e. If V_{th} is insensitive enough to provide an acceptable min-max range. Additionally, the optimized termination design presented in this thesis could be validated, particularly in relation to FFR incremental spacing.

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Appendix A

Python Code for Heatmaps of Device Characteristics

Introduction

This Appendix contains the Python code developed to create heatmaps to visualize the variation in diode characteristics across 150mm SiC wafers which are shown in chapter 5. This comprises of data extraction from .csv files generated by the analyser, subsequent analysis and manipulation of data, and finally plotting of heatmaps. This code also uses the extracted data points to generate histograms which are also shown in the chapter.

Python Code

```
import csv
import os
import matplotlib.pyplot as plt
from matplotlib.colors import ListedColormap
import numpy as np
import matplotlib



# export path
output_folder = r'C:\Users\monag\OneDrive - Swansea University\
                                process\Rob SBD\data\Plots' #-
                                Laptop user
```

```
#output_folder = r'C:\Users\Finn\OneDrive - Swansea University\
                                process\Rob SBD\data\Plots' # -
                                desktop user

# parameters
window_size = 25  # Adjust based on your data
step_size = 10 # Adjust based on your data - left the same as bens
                                as step size is the same
#constants
k = 1.38e-23  # Boltzmann constant
T = 300       # Temperature in Kelvin
q = 1.6e-19   # Elementary charge
A = 0.030625    # Diode area in square centimeters
A_star = 146  # Effective Richardson's constant in A/cm^2/K^2

# Slide the window across the data to find the most linear segment
min_residuals = float('inf')
best_start = 0
best_fit_line = None
best_coefficients = None

def read_csv_as_decimals(filename, ignore_lines=0,
                                trim_single_item_lists=False):
data = []
with open(filename, 'r') as file:
csv_reader = csv.reader(file)
for _ in range(ignore_lines):
next(csv_reader)  # Skip the specified number of lines
for row in csv_reader:
row_data = []
for item in row:
try:
decimal_value = round(float(item), 12)
row_data.append(decimal_value)
except ValueError:
pass  # Skip if conversion to float fails
if trim_single_item_lists and len(row_data) == 1:
continue  # Skip if there's only one item in the row after
                                conversion
if row_data:
# Splice to include only the 3rd and 4th elements
row_data = row_data[0:4]
data.append(row_data)
return data
```

```
# Function to splice the desired items from the lists
def splice(lists, index):
return [sublist[index] for sublist in lists]

def find_correspond(x_array, y_array, threshold):
x_value = None
for x, y in zip(x_array, y_array):
if y >= threshold:
x_value = x
break  # Stop once the first y value corresponding to x >=
                                    threshold is found
return x_value

# Function to calculate the sum of squared residuals for a linear
                                    fit
def calculate_residuals(voltage_segment, current_segment):
log_current = np.log(current_segment)
coefficients = np.polyfit(voltage_segment, log_current, 1)
fit_line = np.poly1d(coefficients)
residuals = log_current - fit_line(voltage_segment)
return residuals, coefficients


# Create a master plot with subplots
#fig, (ax1, ax2) = plt.subplots(1, 2, figsize=(16, 6))

# Initialize lists to store x_pos, y_pos, and extract
x_pos_list = []
y_pos_list = []
extract_list = []
extract_crit_list = []


slope_list= []
intercept_list = []
barrier_list = []
ideality_list = []
# Iterate through all CSV files in the directory
directory = '.'  # Change this to your desired directory
for filename in os.listdir(directory):
if filename.endswith(".csv"):
filepath = os.path.join(directory, filename)
result = read_csv_as_decimals(filepath)
```

```
# Finding xy position
try:
pos = result[32]
x_pos = int(pos[0])*2
y_pos = int(pos[1])*2
result_check = result
result = np.abs(result[105:208]) # data is repeated twice for some
                                 reason, shortening array

# Extracting data for plotting
V_data = splice(result, 1)
I_data = splice(result, 0)
# Screening out tests which didn't sucessfully complete (No probe
                                 contact)
if np.max(I_data) > 1e-8:
for start in range(0, len(V_data) - window_size, step_size):
min_residuals = float('inf')
end = start + window_size
voltage_segment = V_data[start:end]
current_segment = I_data[start:end]
residuals, coefficients = calculate_residuals(voltage_segment,
                                 current_segment)
sum_residuals = np.sum(residuals**2)
if sum_residuals < min_residuals:
min_residuals = sum_residuals
best_start = start
best_fit_line = np.poly1d(coefficients)
best_coefficients = coefficients

# Extract the best linear segment
best_end = best_start + window_size
voltage_linear = V_data[best_start:best_end]
current_linear = I_data[best_start:best_end]

slope = best_coefficients[0]
intercept = np.exp(best_coefficients[1])

ideality = (1/slope)*(q/(k*T))
barrier_height = (k * T / q) * np.log((A * A_star * T**2) /
                                 intercept)

else:
# Appending previous value of the array if no measurement
```

```
slope_list.append(slope_list[-1])
intercept_list.append(intercept_list[-1])
barrier_list.append(barrier_list[-1])
ideality_list.append(ideality_list[-1])

threshold = 1E-7 # extraction critera = 0.1uA
extract = find_correspond(V_data, I_data, threshold)
if extract is None:
extract = 1
print(pos[0],pos[1])
if ideality < 2 and extract > 0.2:
x_pos_list.append(x_pos)
y_pos_list.append(y_pos)
extract_list.append(extract)
ideality_list.append(ideality)
slope_list.append(slope)
intercept_list.append(intercept)
barrier_list.append(barrier_height)

# Store x_pos, y_pos, and extract for each iteration
#x_pos_list.append(x_pos)
#y_pos_list.append(y_pos)
#extract_list.append(extract)

except IndexError:
# Handle the error if 'list index out of range' occurs
print(f"Skipped file due to IndexError: {filename}")
except Exception as e:
# Handle any other exceptions that might occur
print(f"Skipped file due to unexpected error: {filename}. Error: {e
                                    }")



#df = pd.DataFrame({'X':x_pos_list,'Y':y_pos_list,'Barrier':
                                    barrier_list,'Ideality':pd.Series(
                                    ideality_list)})
# Add heatmap plot to the second subplot
#heatmap_data = np.zeros((3,len(x_pos_list)))

#for i in range(len(x_pos_list)):
#  heatmap_data[x_pos_list[i], y_pos_list[i]] = barrier_list[i]
hsv_modified = matplotlib.colormaps.get_cmap('hsv')
```

```
newcmp = ListedColormap(hsv_modified(np.linspace(0, 0.28, 256)))


hsv_modified1 = matplotlib.colormaps.get_cmap('hsv_r')
newcmp1 = ListedColormap(hsv_modified1(np.linspace(0.72, 0.98, 256)
                                       ))


#sns.heatmap(heatmap_data, annot=True, cmap='coolwarm')
#sc = ax2.scatter(x_pos_list, y_pos_list, c=barrier_list, s=300,
                                       alpha=1)
fig1, ax2 = plt.subplots()  # Create a new figure and axis for the
                                       first scatter plot
sc = ax2.scatter(x_pos_list, y_pos_list, c=extract_list, cmap=
                                       newcmp,s=15, alpha=1, marker="s",
                                       vmax=0.7)
ax2.set_xlabel('Horizontal Position (mm)')
ax2.set_ylabel('Vertical Position (mm)')

ax2.set_aspect("equal")

cbar = plt.colorbar(sc, ax=ax2)
cbar.set_label('Forward Voltage (V)')

file_path = os.path.join(output_folder, 'Vf_SAT8.png')
plt.savefig(file_path, dpi=600)


plt.show()

##
#fig2, ax1 = plt.subplots()
#sc1= ax1.scatter(x_pos_list, y_pos_list, c=barrier_list, cmap=
                                       newcmp,s=15, alpha=1, marker="s",
                                       vmax=1.2)

#ax1.set_xlabel('Horizontal Position (mm)')
#ax1.set_ylabel('Vertical Position (mm)')
#ax1.set_aspect("equal")
#plt.colorbar(sc1, ax=ax1, label='Barrier Height (eV)')

#file_path = os.path.join(output_folder, 'BH_SAT8.png')
#plt.savefig(file_path, dpi=600)
```

```
#plt.show()


##
counts,bin_edges = np.histogram(extract_list,bins=20)

plt.figure()

plt.hist(extract_list, bins=20,edgecolor='black')
plt.xlabel('Forward Voltage (V)')
plt.ylabel('No. of Diodes')


file_path = os.path.join(output_folder, 'Vf_hist_SAT8.png')
#plt.savefig(file_path, dpi=600)


plt.show()

for i in range(len(bin_edges) - 1):
bin_min = bin_edges[i]
bin_max = bin_edges[i + 1]
values_in_bin = [v for v in extract_list if bin_min <= v < bin_max]
                                    # Get values that fall in the
                                   current bin
print(f"Bin {i+1}: Range ({bin_min}, {bin_max}), Count = {counts[i]
                                   }")
#print(f"Values in bin: {values_in_bin}\n")

average_e = np.mean(extract_list)

print(f"average = {average_e}")
plt.show()

##
print("-----------------BH---------------")


##
counts,bin_edges = np.histogram(barrier_list,bins=20)

plt.figure()

plt.hist(barrier_list, bins=20,edgecolor='black')
```

```
plt.xlabel('Barrier Height (eV)')
plt.ylabel('No. of Diodes')


file_path = os.path.join(output_folder, 'barrier_hist_SAT8.png')
plt.savefig(file_path, dpi=600)

for i in range(len(bin_edges) - 1):
bin_min = bin_edges[i]
bin_max = bin_edges[i + 1]
values_in_bin = [v for v in extract_list if bin_min <= v < bin_max]
                                    # Get values that fall in the
                                   current bin
print(f"Bin {i+1}: Range ({bin_min}, {bin_max}), Count = {counts[i]
                                   }")
#print(f"Values in bin: {values_in_bin}\n")

average_bh = np.mean(barrier_list)

print(f"average_barrier = {average_bh}")


plt.show()

##
print("-----------------Ideality---------------")


##
counts,bin_edges = np.histogram(ideality_list,bins=20)

plt.figure()

plt.hist(ideality_list, bins=20,edgecolor='black')
plt.xlabel('Ideality Factor')
plt.ylabel('No. of Diodes')


file_path = os.path.join(output_folder, 'ideality_hist_SAT8.png')
#plt.savefig(file_path, dpi=600)

for i in range(len(bin_edges) - 1):
bin_min = bin_edges[i]
bin_max = bin_edges[i + 1]
```

```
values_in_bin = [v for v in extract_list if bin_min <= v < bin_max]
                                        # Get values that fall in the
                                    current bin
print(f"Bin {i+1}: Range ({bin_min}, {bin_max}), Count = {counts[i]
                                    }")
#print(f"Values in bin: {values_in_bin}\n")

average_id = np.mean(ideality_list)

print(f"average_ideality = {average_id}")


plt.show()
```

Appendix B

RCA Sample Clean Procedure

Introduction

This Appendix contains the details for full Radio Corporation of America (RCA) chemical cleaning process used to prepare the SiC sample surface before contact metal deposition. This process was used during the P-type Ohmic contact fabrication work presented in chapter 6.

Step-by-Step RCA Clean

1. Place sample in Acetone for 5 minutes in ultrasonic bath, rinse with deionised (DI) water and dry.
2. Place sample in isopropanol (IPA) for 5 minutes in ultrasonic bath, rinse in DI water and dry.
3. Place sample in RCA Standard Clean 1 (SC-1) solution comprised of ammonium hydroxide (N_4OH), H_2O_2 and DI water in the ratio 1:1:5 heated to a temperature of 70-80°C for 10 minutes. Rinse in DI water.
4. Place sample in 5% Hydrofluoric acid (HF) solution for 1 minute. Rinse in DI water.
5. Place sample in RCA Standard Clean 2 (SC-2) solution comprised of hydrochloric acid (HCL), H_2O_2 and DI water in the ratio 1:1:5 heated to a temperature of 70-80°C for 10 minutes. Rinse in DI water and dry.

Appendix C

SiC JFET Mask Layout and Process Flow

A JFET process flow and corresponding mask design has been completed using Klayout driven by its Python API [259]. This enables the automated creation of different design variations i.e. JFETs with different mesa widths. Furthermore, device cross-sections were generated using the Xsection package. The mask layout of the 20x20mm piece stepped intended to be repeated across a SiC wafer is shown below in figure C.1.

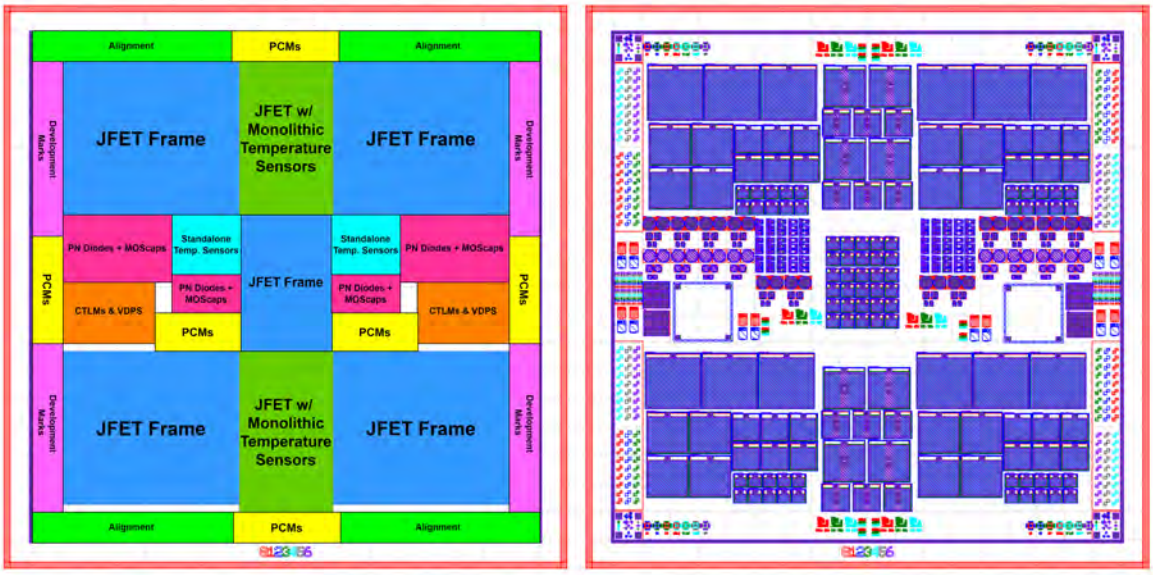

Fig. C.1 Mask layout designed for the proposed SiC JFET process flow. The left hand side image indicates which areas contain different device and test structures across the piece. On the right, the full layout design is displayed.

Alongside SiC JFET devices with varying design parameters and die sizes, other structures were included. JFETs with monolithically integrated sensors were designed to test the feasibility of the design proposed in chapter 4. PiN diodes were included to allow comparison

between diode and JFET off-state leakage current and breakdown voltage. This enables an assessment of if the JFETs are reaching the full voltage blocking capability of the N- drift layer. Van der Pauws and CTLMs are included to measure ρ_c and P-type dopant activation, respectively. Metal-oxide-semiconductor capacitors (MOScaps) have also been designed to measure the fixed charge in the inter-layer dielectric (ILD). Stand-alone lateral P-type resistors have been included to measure the linearity of the resistor temperature response. This can be compared to the performance of the resistor when monolithically integrated into the JFET. Finally, Process Control Monitor (PCM) structures have been included to monitor critical dimensions (CDs), etch depths and deposited thicknesses of metals and dielectrics.

An overview of the process flow designed to fabricate SiC JFETs is shown in figure C.2. This fabrication process requires 5 individual photolithography mask layers. First, the N-type epitaxial wafers are blanket implanted with Phosphorous to form an N+ layer. An oxide hardmask layer is then deposited and patterned by Inductively Couple Plasma (ICP) dry etching. Then, the SiC etch is then performed via ICP etching. The gate P+ implant is then performed as a self-aligned process (i.e. the oxide etch mask is not removed). The oxide mask is then removed, and the wafer undergoes carbon capping and a subsequent activation anneal. Although not shown in Figure C.2, a further mask layer is then used to perform an isolation etch around the device extremities post-anneal. Termination structures were not included in this design.

The contact metal for the gate and source contacts is then deposited concurrently, and patterned via lift-off procedure. The backside ohmic metal is then deposited, and the sample then undergoes ohmic contact anneals for both frontside and backside metals. An ILD is deposited to isolate the gate contacts from the source pad, and subsequentially patterned to open a window to enable contact to the source metal. In the third dimension, a window is also opened to make contact to the gate pad. Finally, a passivation layer is deposited and patterned to prevent surface leakage, and potential device degradation.

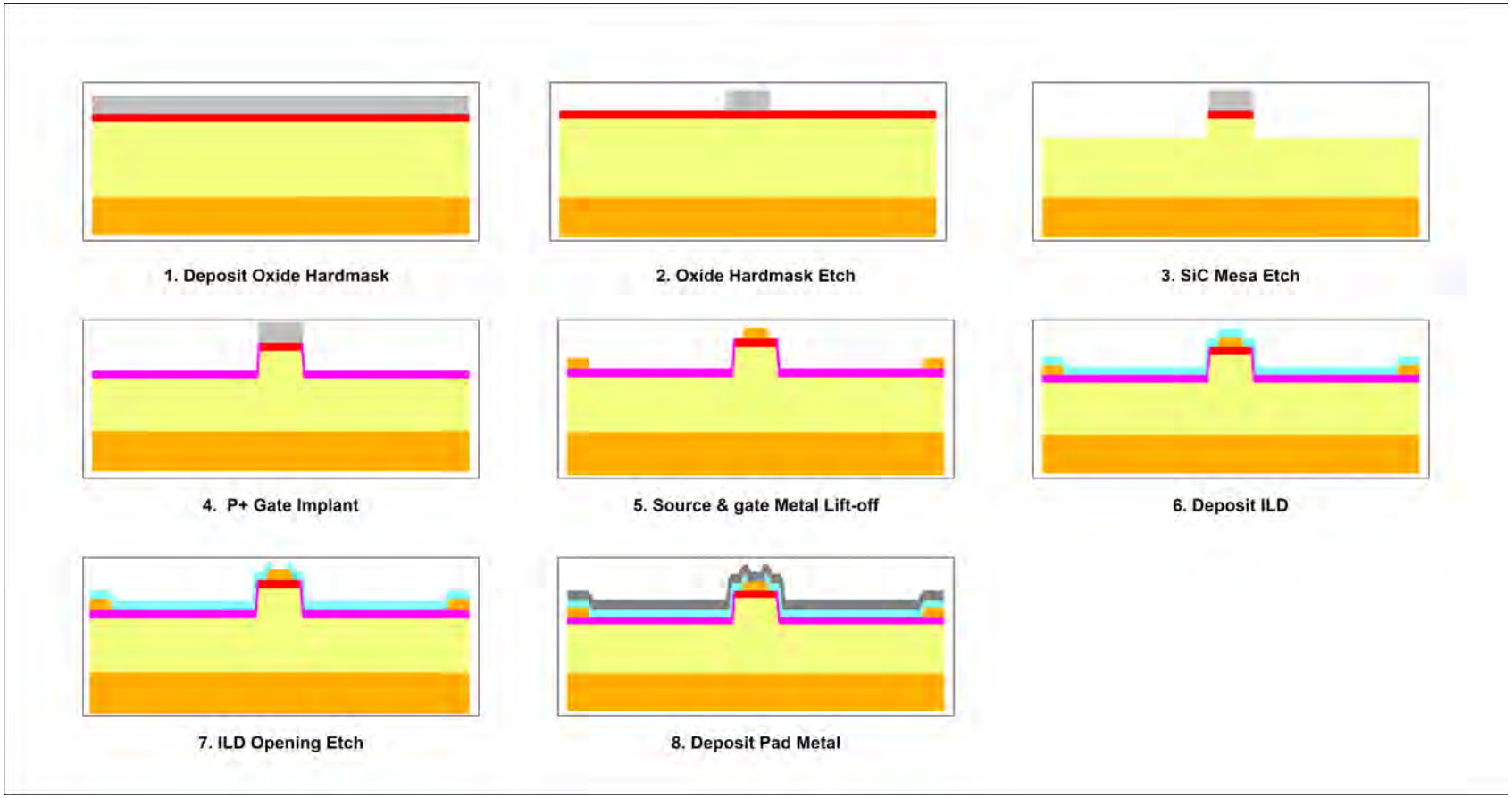

Fig. C.2 Outline of proposed SiC JFET fabrication process flow. Five individual mask layers are required for this process: Oxide Hardmask/SiC Mesa Etch, Device Isolation etch (not shown), Source & Gate contact metal, ILD Opening Etch, Pad Metal lift off and Passivation etch back (not shown). The isolation etch and passivation layers are not shown in this flow diagram as they have no bearing on the unit cell structure of the JFET.