3D Monte Carlo Simulations of n-type Nanowire-FETs: The Effect of Gate Scaling

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***Abstract*—The potential of gate-all-around (GAA) nanowire (NW) field-effect transistors (FETs) to replace sub-3 nm complementary metal-oxide-semiconductor (CMOS) technology has attracted significant interest. This simulation study investigates the impact of gate length (L_G) scaling on the drain drive current (I_{DD}) in NW-FETs using an advanced in-house 3D finite-element ensemble Monte Carlo (MC) simulation toolbox that incorporates quantum corrections via the Schrödinger equation. The MC-simulated I_D-V_G characteristics show excellent agreement with experimental data across both low and high drain biases. Our results reveal that scaling the gate length down to 10 nm leads to an unexpected decline in I_{DD} beyond 16 nm. While I_{DD} initially increases from 22 nm to 16 nm, consistent with scaling theory, it subsequently decreases by up to 12% at 10 nm. This reduction is attributed to intensified back-scattering and enhanced fringing electric fields resulting from the shorter source-to-drain distance. This study uniquely demonstrates the critical role of these effects in limiting drive current at sub-16 nm gate lengths in NW-FETs—providing predictive insight into non-ideal short-channel transport behaviors and highlighting key challenges for performance optimization in future transistor architectures.**

***Index Terms*—Gate-all-around, Monte Carlo, nanowire, scaling, Quantum correction.**

I. Introduction

FinFETs have dominated semiconductor technology due to their scalability, strong electrostatic control, and reliable performance [1], [2]. However, as device scaling advances, FinFETs face physical limitations such as Fin height, heat dissipation, and leakage currents [3], [4]. Their three-sided gate structure also struggles to maintain electrostatic control at smaller nodes [5], [6], driving the search for alternative architectures. Gate-all-around (GAA) FETs are emerging as a promising successor, offering superior electrostatic control and enhanced scalability [7]–[9]. However, several challenges must be addressed, including fabrication complexities, thermal management, 3D channel stacking, doping uniformity, scaling, drain current, switching speed, and power consumption [10].

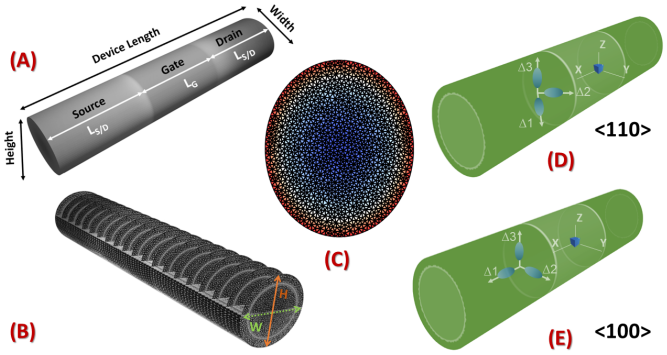

Fig. 1. (A) 3D schematic of NW-FET, showing channel width (W), height (H), gate length (L_G), and source/drain length ($L_{S/D}$). (B) Illustration of evenly spaced 2D slices along the channel in a 3D view. (C) A 2D finite element (FE) mesh slice used for Schrödinger equation solutions across the channel. (D) Δ valley positions in a NW-FET with a $\langle 110 \rangle$ channel orientation. (E) Δ valley positions in a NW-FET with a $\langle 100 \rangle$ channel orientation.

A deeper understanding of MOSFET physics is essential to improve performance and reliability. These challenges have slowed widespread adoption [11]. Hence, this study analyzes silicon n-type GAA nanowire (NW) FETs (see Fig. 1) and explores key performance optimization factors using a 3D finite element quantum-corrected Monte Carlo (MC) simulation toolbox, providing insights into the adaptation and optimization of NW-FET designs for future technology.

II. Modelling and Simulation

This study employs MC simulations to analyze the NW-FET device using the in-house VENDES tool [12]. Unlike conventional TCAD software [13], our toolbox utilizes a 3D finite element (FE) tetrahedral mesh to accurately model the irregular shapes, nanoscale geometry, and quantum confinement effects. It solves the Poisson equation and models carrier transport

with high spatial precision. Moreover, it integrates 3D drift-diffusion (DD) and ensemble MC simulations, coupled with the 2D Schrödinger equation. Quantum corrections (QC) are computed along uniformly spaced 2D slices (Fig. 1 B). The 3D DD method provides initial approximations in the subthreshold region, while 3D MC simulations, essential for capturing non-equilibrium transport at high biases, ensure accuracy despite their computational demands. The MC engine includes a non-parabolic and anisotropic silicon band structure, considering the Γ, L, and Δ valleys and key scattering mechanisms such as phonon interactions, ionized impurity scattering, and interface roughness (IR) using Ando's model [10]. A static screening approximation is applied for electron-ionized impurity scattering, with self-consistent calculations of the Fermi energy and electron temperature [14]. The simulation domain fully includes the source/drain (S/D) regions, eliminating the need for post-processing to correct for contact resistance. Additionally, the effective electric field for electron-IR scattering is dynamically computed at each electron position in real time [12], [15].

III. Simulation Technique

A. Verification of the simulation toolkit

An experimental NW-FET with a gate length (L_G) of 22 nm was simulated for two channel orientations: ⟨100⟩ and ⟨110⟩, to validate the accuracy of the toolbox. The ⟨110⟩ NW-FET, fabricated by IBM [16], features an ellipsoidal cross-section resulting from the etching process, with a height of 14.22 nm, width of 11.3 nm, source/drain length ($L_{S/D}$) of 30.8 nm, and an elliptical perimeter of 40.21 nm. The simulated I_D-V_G characteristics at high (1.0 V) and low (0.05 V) drain biases closely match the experimental results [16], as shown in Fig. 2. This strong agreement confirms the simulation toolbox's accuracy for nanoscale devices. The precision is achieved by integrating Schrödinger equation-based QC with DD and ensemble MC simulations. Using the constant current extraction method, a threshold voltage (V_T) of 0.26 V was obtained from simulations of 22 nm gate length devices.

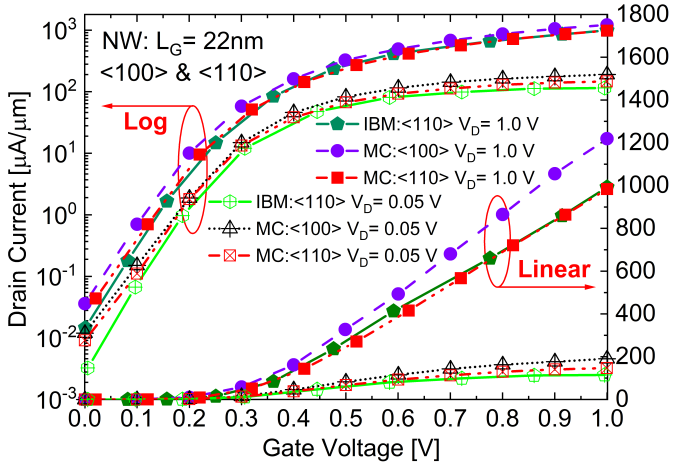

Fig. 2. I_D–V_G characteristics of NW-FETs with a gate length of 22 nm at high (1.0 V) and low (0.05 V) drain biases, for ⟨110⟩ and ⟨100⟩ channel orientations, obtained from 3D MC simulations and compared with experimental IBM data [16] for a 22 nm gate-length NW-FET fabricated with a ⟨110⟩ channel orientation. The extracted threshold voltage (V_T) is 0.26 V.

TABLE I
Dimensions and Parameters for the Simulated NW-FETs

Device dimensions	
Gate length (L_G) [nm]	22 → 10
S/D region length ($L_{S/D}$) [nm]	14
High-κ thickness (EOT) [nm]	1
Channel orientation	⟨110⟩
Channel height (H) [nm]	7.17
Channel width (W) [nm]	5.7
Perimeter [nm]	20.28
Doping parameters	
Max n-type (Gaussian) S/D [cm^{-3}]	5×10^{19}
Uniform p-type channel [cm^{-3}]	1×10^{15}
Tight-Binding Energy Variations for Silicon Δ-Valleys	
Δ_x (E_{G1}-Δ_{x1}) [eV]	1.12 → 1.282
Δ_y (E_{G2}-Δ_{x2}) [eV]	1.12 → 1.247
Δ_z (E_{G3}-Δ_{x3}) [eV]	1.12 → 1.247

B. Cross-Section Scaling

The nanowire field-effect transistor (NW-FET) was scaled to a smaller cross-sectional area after validating the simulation toolbox. The device features a channel height of 7.17 nm, a width of 5.7 nm, and a source/drain length ($L_{S/D}$) of 14 nm (see Fig. 1), with an equivalent oxide thickness (EOT) of 1.0 nm. To analyze the quantum-confined **k**-space of the nanowire, the tight-binding (TB) model [17] was employed to compute the band structure, enabling the extraction of electron effective masses [15]. The longitudinal effective mass, m_l, was determined to be 0.92 m_0, closely matching the bulk silicon value of 0.916 m_0. Meanwhile, the transverse effective mass, m_t, was found to be 0.233 m_0, compared to the bulk value of 0.19 m_0. To accurately represent experimental conditions, a peak n-type doping concentration of 5×10^{19} cm^{-3} was established using a reverse-engineering approach [18], based on the subthreshold characteristics of measured I_D-V_G data [16]. All current values were normalized to the NW-FET perimeter (20.28 nm) to ensure a consistent basis for comparison. A detailed list of device dimensions and doping parameters is provided in Table I. The drain drive current, I_{DD}, a critical performance parameter that dictates both switching speed and power consumption, was assessed at $V_G - V_T$ and $V_D = 0.7$ V, in alignment with IRDS guidelines [19]. A higher I_{DD} facilitates faster switching but also increases power consumption, highlighting the trade-off between speed and efficiency in device optimization.

IV. Simulation Results

The scaling process begins with a gate length of 22 nm and extends down to an aggressively reduced 10 nmn length. Further reductions beyond this point is not advisable as further scaling leads to significant source-to-drain tunneling [20], which hinders transistor switching by preventing complete

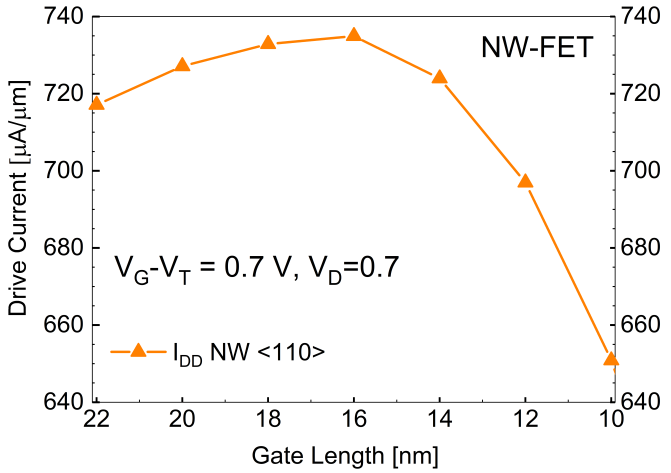

Fig. 3. The effect of gate length scaling on the drain-drive-current (I_{DD}) defined at $V_G - V_T = 0.7$ V and $V_D = 0.7$ V [19] in n-type GAA NW-FETs for $\langle 110 \rangle$ channel crystallographic orientations.

turn-off. We will assume in this gate scaling study that NW-FETs retain the same cross-sectional area, as presented in Table I, for all scaled gate lengths, to clearly separate the quantum confinement effects from the scaling. As the L_G is reduced from 22 nm to 16 nm, the drain current, I_{DD}, follows the expected trend predicted by scaling theory [21], showing an increase. However, as the L_G is further reduced to 14 nm and then to 10 nm, I_{DD} begins to decline significantly, contradicting conventional scaling expectations. This deviation is attributed to intensified back-scattering effects. Initially, as the gate shortens, the fringing electric field at the drain side strengthens, accelerating electrons and increasing the drain current. However, when the L_G drops below 14 nm, the fringing field at the source side also intensifies due to the close proximity between the source and drain because the source-side potential becomes influenced by the drain-side potential through long-range Coulomb interactions [22]. The resulting increase in back-scattering redirects electrons toward the source rather than allowing them to contribute to current flow, leading to a reduction in I_{DD} as illustrated in Figure 3.

A. Electron Velocity in the Device Channel

To better understand the physical behavior of NW-FETs as they scale down, we analyze the average electron velocity for L_G ranging from 22 nm to 10 nm. Figure 4 illustrates the variation in average electron velocity for NW-FETs with scaled gate lengths along the $\langle 110 \rangle$ channel orientation at a high drain bias of 0.7 V and a gate overdrive of 0.7 V. In the gate-controlled region, devices with longer gate lengths (22 nm to 14 nm) exhibit lower velocity peaks near the gate entrance. As the L_G is further reduced to 12 nm and 10 nm, these velocity peaks increase due to more pronounced electron back-scattering. This velocity reduction for larger gate lengths is primarily attributed to enhanced electron interactions with acoustic and non-polar optical phonons [10], [23]. Additionally, in longer gate devices, fringing electric fields (which extend beyond the controlled region) have a minimal impact. However, as the L_G shrinks, fringing fields become increasingly significant, complicating electron velocity modulation. A distinct trend emerges as electrons traverse the gate-controlled region: while scattering initially redistributes electron momentum, reducing velocity, an acceleration phase follows as electrons approach the gate exit, where the electric field propels them into the drain region. However, within the heavily doped drain, intensified scattering from ionized impurities causes another velocity reduction due to the redistribution of momentum, limiting further acceleration. A particularly striking observation is the emergence of two distinct velocity peaks in devices with 12 nm L_G and 10 nm L_G—one at the gate entrance and another near the gate exit. This dual-peak behavior provides direct evidence of intensified back-scattering effects, reinforcing our finding that aggressive gate scaling down to 10 nm leads to a deviation from expected drain current behavior. Scaling the L_G to 12 nm and 10 nm amplifies the fringing electric field intensity beneath the gate. This effect concentrates the electric field near the gate edge, producing a sharp velocity peak at the gate entrance. The stronger field enhances carrier acceleration, allowing electrons to reach higher velocities, as shown in Fig. 4. For a 10 nm L_G, the average electron velocity peak reaches 1.05×10^7 cm/s, and with a 12 nm L_G, the electric field is slightly smaller, and the fringing field effect is less pronounced, resulting in a lower electron velocity of 9.2×10^6 cm/s. This corresponds to a 12% reduction in peak velocity for the 12 nm compared to the 10 nm case. Nevertheless, this decline can be partially mitigated through architectural enhancements such as incorporating alternative materials (e.g., germanium with silicon), introducing channel strain [10], optimizing source/drain doping, or reducing oxide thickness by replacing the high-κ gate dielectric [24]. Addressing these challenges to meet future technology demands may further require novel design strategies and advanced fabrication techniques [25].

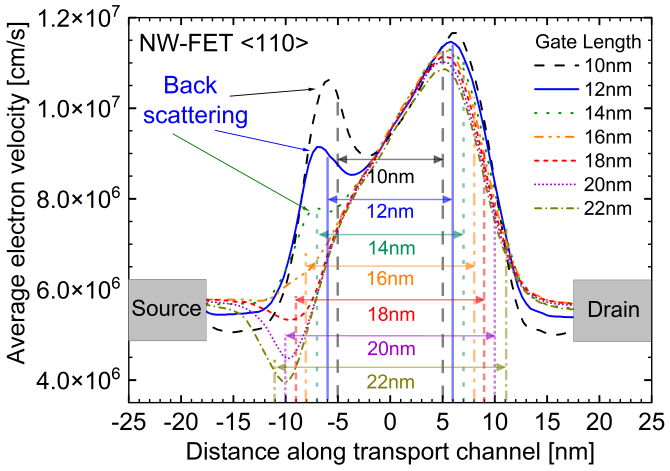

Fig. 4. Average electron velocity in scaled n-type NW-FETs with gate lengths ranging from 22 nm to 10 nm, at $V_G - V_T = 0.7$ V and $V_D = 0.7$ V, in the $\langle 110 \rangle$ channel orientation.

Conclusion

Using a state-of-the-art 3D FE MC toolbox, we investigated the effect of gate length scaling on the drain drive current in n-type GAA NW-FETs. Our findings show that while scaling L_G effectively reduces the poly pitch and enhances integration density, it also exacerbates short-channel effects—such as threshold voltage degradation (V_T is 0.24 V in 12 nm L_G, and 0.23 V in 10 nm L_G), increased subthreshold swing (SS), and drain-induced barrier lowering (DIBL)—all of which negatively impact device performance [7], [26]. Furthermore, reducing L_G below 16 nm introduces significant challenges, including a 12% decline in I_DD due to intensified electron back-scattering at the source side of the gate, driven by long-range Coulomb interactions between the source and drain. This study also identifies a novel impact of fringing electric fields as L_G is scaled down, providing new insights into electron transport mechanisms and performance limitations in ultra-scaled NW-FETs, despite the presence of stronger quantum confinement. As L_G decreases, fringing fields at both the source and drain edges intensify due to potential penetration from the drain, which enhances back-scattering and reduces electron injection efficiency. This leads to a lower channel electron density and a corresponding reduction in I_DD. These findings offer valuable guidance for optimizing NW-FET architectures, emphasizing the trade-offs between aggressive gate-length scaling and the fundamental transport limitations inherent in next-generation semiconductor technologies.

References

[1] S. D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M. H. Na, "Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond," in *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S)*, Oct. 2015, pp. 1–3, DOI: https://doi.org/10.1109/S3S.2015.7333521.

[2] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Advances in Electronics*, vol. 2014, p. 21, 2014, DOI: https://doi.org/10.1155/2014/365689.

[3] W. Ahn, C. Jiang, J. Xu, and M. A. Alam, "A new framework of physics-based compact model predicts reliability of self-heated modern ICs: FinFET, NWFET, NSHFET comparison," in *2017 IEDM Tech. Dig.*, 2017, pp. 331–333, DOI: https://doi.org/10.1109/IEDM.2017.8268386.

[4] P. Oldiges, R. A. Vega, H. K. Utomo, N. A. Lanzillo, T. Wassick, J. Li, J. Wang, and G. G. Shahidi, "Chip power-frequency scaling in 10/7nm node," *IEEE Access*, vol. 8, pp. 154 329–154 337, 2020, DOI: https://doi.org/10.1109/ACCESS.2020.3017756.

[5] X. He, J. Fronheiser, P. Zhao, Z. Hu, S. Uppal, X. Wu, Y. Hu, R. Sporer, L. Qin, R. Krishnan, E. M. Bazizi, R. Carter, K. Tabakman, A. K. Jha, H. Yu, O. Hu, D. Choi, J. G. Lee, S. B. Samavedam, and D. K. Sohn, "Impact of aggressive fin width scaling on FinFET device characteristics," in *2017 IEDM Tech. Dig.*, Dec 2017, pp. 493–496, DOI: https://doi.org/10.1109/IEDM.2017.8268427.

[6] K. Karimi, A. Fardoost, and M. Javanmard, "Comprehensive review of FinFET technology: History, structure, challenges, innovations, and emerging sensing applications," *Micromachines*, vol. 15, no. 10, 2024, DOI: https://doi.org/10.3390/mi15101187.

[7] D. Nagy, G. Espiñeira, G. Indalecio, A. J. García-Loureiro, K. Kalna, and N. Seoane, "Benchmarking of FinFET, Nanosheet, and Nanowire FET architectures for future technology nodes," *IEEE Access*, vol. 8, pp. 53 196–53 202, March 2020, DOI: https://doi.org/10.1109/ACCESS.2020.2980925.

[8] N. A. Kumari and P. Prithvi, "Performance evaluation of GAA nanosheet FET with varied geometrical and process parameters," *Silicon*, vol. 14, no. 15, pp. 9821–9831, Oct. 2022, DOI: https://doi.org/10.1007/s12633-022-01695-7.

[9] M. Ehteshamuddin, S. A. Loan, and M. Rafat, "Stacked nanosheet based reconfigurable FET," in *2020 32nd Int. Conf. Microelectronics (ICM)*, 2020, pp. 1–4, DOI: https://doi.org/10.1109/ICM50269.2020.9331813.

[10] M. G. K. Alabdullah, M. A. Elmessary, D. Nagy, N. Seoane, A. J. García-Loureiro, and K. Kalna, "Scaling challenges of nanosheet field-effect transistors into sub-2 nm nodes," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 479–485, 2024, DOI: https://doi.org/10.1109/JEDS.2024.3416200.

[11] C. Yoo, J. Chang, S. Park, H. Kim, and J. Jeon, "Optimization of gate-all-around device to achieve high performance and low power with low substrate leakage," *Nanomaterials*, vol. 12, no. 4, 2022, DOI: https://doi.org/10.3390/nano12040591.

[12] N. Seoane, D. Nagy, G. Indalecio, G. Espiñeira, K. Kalna, and A. J. García-Loureiro, "A multi-method simulation toolbox to study performance and variability of nanowire FETs," *Materials*, vol. 12, no. 15, pp. 2391–2406, 2019, DOI: https://doi.org/10.3390/ma12152391.

[13] M. Lundstrom, "Computational electronics for the 21st century: Reflections on the past, present, and future," in *2015 45th European Solid State Device Research Conference (ESSDERC)*, 2015, pp. 36–39, DOI: https://doi.org/10.1109/ESSDERC.2015.7324707.

[14] N. Seoane, J. G. Fernandez, K. Kalna, E. Comesaña, and A. García-Loureiro, "Simulations of statistical variability in n-type FinFET, nanowire, and nanosheet FETs," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1416–1419, 2021, DOI: https://doi.org/10.1109/LED.2021.3109586.

[15] N. Seoane, K. Kalna, X. Cartoixà, and A. García-Loureiro, "Multilevel 3-D device simulation approach applied to deeply scaled nanowire field effect transistors," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5276–5282, 2022, DOI: https://doi.org/10.1109/TED.2022.3188945.

[16] S. Bangsaruntip, K. Balakrishnan, S. L. Cheng, J. Chang, M. Brink, I. Lauer, R. L. Bruce, S. U. Engelmann, A. Pyzyna, G. M. Cohen, L. M. Gignac, C. M. Breslin, J. S. Newbury, D. P. Klaus, A. Majumdar, J. W. Sleight, and M. A. Guillorn, "Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond," in *2013 IEDM Tech. Dig*, 2013, pp. 526–529, DOI: https://doi.org/10.1109/IEDM.2013.6724667.

[17] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*, 1st ed. Saunders College Publ., Jan. 1976.

[18] D. Nagy, M. Aldegunde, M. A. Elmessary, A. J. García-Loureiro, N. Seoane, and K. Kalna, "Modelling of nanoscale multi-gate transistors affected by atomistic interface roughness," *J. Phy: Cond. Matt.*, vol. 30, p. 144006, April 2018, DOI: https://doi.org/10.1088/1361-648X/aab10f.

[19] IEEE, "International Roadmap for Devices and Systems (IRDS): 2023 Edition," 2023, [Online]. Available: https://irds.ieee.org/editions/2023.

[20] N. Seoane and A. Martinez, "A detailed coupled-mode-space non-equilibrium Green's function simulation study of source-to-drain tunnelling in gate-all-around Si nanowire metal oxide semiconductor field effect transistors," *J. Appl. Phys.*, vol. 114, no. 10, p. 104307, 2013, DOI: https://doi.org/10.1063/1.4820390.

[21] K. Kalna, S. Roy, A. Asenov, K. Elgaid, and I. Thayne, "Scaling of pseudomorphic high electron mobility transistors to decanano dimensions," *Solid-St. Electron.*, vol. 46, no. 5, pp. 631–638, 2002, DOI: https://doi.org/10.1016/S0038-1101(01)00331-8.

[22] M. V. Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electron mobility in thin-oxide structures," *J. Appl. Phys.*, vol. 89, no. 2, pp. 1232–1250, 2001, DOI: https://doi.org/10.1063/1.1332424.

[23] M. V. Fischetti, P. D. Yoder, M. M. Khatami, G. Gaddemane, and M. L. Van de Put, "Hot electrons in Si lose energy mostly to optical phonons: Truth or myth?" *Appl. Phys. Lett.*, vol. 114, no. 22, p. 222104, 2019, DOI: https://doi.org/10.1063/1.5099914.

[24] M. G. K. Alabdullah, N. Seoane, A. J. Garcia-Loureiro, and K. Kalna, "Ultra scaled nanosheet & nanowire FETs performance evaluation with 3D Monte Carlo simulations for future technology," in *2024 Int. Semiconductor Conf. (CAS)*, 2024, pp. 333–336, DOI: https://doi.org/10.1109/CAS62834.2024.10736781.

[25] W. Liao, W. Qian, J. An, L. Liang, Z. Hu, J. Wang, and L. Yu, "High-performance gate-all-around field effect transistors based on orderly arrays of catalytic Si nanowire channels," *Nano-Micro Lett.*, vol. 17, no. 1, p. 154, Feb 2025, DOI: https://doi.org/10.1007/s40820-025-01674-8.

[26] R. Kaur and N. R. Mohapatra, "Comprehensive analysis of sheet thickness scaling on the performance of nanosheet nfets," *IEEE Trans. Electron Devices*, vol. 71, no. 5, pp. 2856–2862, May 2024, DOI: https://doi.org/10.1109/TED.2024.3377606.