

High-Sensitivity and Fast-Response Piezotronic Pressure Sensors by Mechanical Stacking in Silicon Wafer

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Abstract: CMOS-compatible pressure sensor capable of seamlessly bridging external stimuli with modern electronics is essential for advancing applications in wearable systems, human-machine interfaces, and robotics. However, the weak mechano-electrical coupling of silicon, together with its epitaxial difficulty with piezoelectric semiconductors, has long challenged the development of high-performance Si-based sensors. Here, we report a generalizable mechanical stacking strategy that realizes epitaxial-free, wafer-scale Si/GaN pressure sensors. Both nn and pn junction architectures are constructed to yield electrically tunable pressure response due to the piezotronic effect driven by asymmetrical interfaces and carrier shielding. As a result, the device delivers high pressure sensitivity of 43.34 meV/MPa, exceptional gauge factors of 5.8×10^6 , and sub-millisecond response times. We show that these piezotronic pressure sensors can be used to detect impulsive forces with high temporal resolution, as well as monitor signals of finger rhythms. This work establishes mechanical stacking as a universal integration paradigm for epitaxial-free heterogeneous electronics, enabling high-performance, CMOS-compatible piezotronic sensors.

Keywords: Piezotronic Sensors, Mechanical Stacking, Epitaxial-Free Heterogeneous Electronics, Si/GaN, High Sensitivity, Fast Response.

1. INTRODUCTION

Silicon (Si) serves as the cornerstone of modern semiconductor technology, underpinning the global infrastructure of complementary metal-oxide-semiconductor (CMOS) electronics¹. As electronic systems increasingly extend beyond computation into intelligent interaction, the ability to sense mechanical stimuli directly on the Si platform has become highly desirable²⁻⁷. Such Si-compatible mechanical sensors would allow seamless “sense–process–actuate” integration, unlocking tremendous potential in wearable electronics, soft robotics, and human-machine interfaces⁸. In these scenarios, the ability to detect mechanical signals with high sensitivity and fast response is critical for accurate and real-time mechanical perception^{9,10}. However, the centrosymmetric crystal structure of Si suffers from weak mechano-electrical coupling^{11,12}, which delivers modest sensitivity and requires complex amplifying circuit, thereby hampering its applicability in advanced sensing systems¹³.

The piezotronic effect emerges as a firenew modulation mechanism based on piezoelectric semiconductors such as GaN and ZnO, where strain-induced polarization charges can produce a piezo-potential acting as an effective ‘gate voltage’ to control carrier transport¹⁴. Such polarization engineering enables direct tunability of interfacial barrier in semiconductor devices, yielding unprecedented mechano-electrical coupling, ultrafast response, and versatile device functionality¹⁵⁻²³. The potential of piezotronics has been widely demonstrated in diverse prototypes, including Schottky diodes¹⁵, tunneling transistors^{16,18,19}, and pn junctions²². Realizing such advances at scale requires seamless integration of piezotronic devices with the state-of-the-art Si-based CMOS platform that is foundations of modern electronics. However, epitaxial integration of piezoelectric materials with Si wafers is constrained by large lattice and thermal mismatches²⁴, which inevitably introduce high defect densities and degrade device reliability. Considerable effort have been made to alternative strategies, such as mimicking piezoelectric-like responses in Si through flexoelectricity^{4,5} or electrostriction effects²². A prominent example is nanoscale flexoelectricity, which, activated by an atomic force microscope tip, enables the generation of high strain gradients and spatially varying polarization capable of modulating interfacial barrier^{4,5}. Similarly, strong built-in electric field in the narrow depletion regions of Schottky junction causes symmetry breaking and, when combined with electrostriction, drives anisotropic piezoelectricity^{25,26} and piezotronic response

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4 22. These methods allow tunable piezoelectricity and thus more functionalities, due to the strain-
5 induced polarization response depending on size effect (e.g., tip radius in flexoelectricity ²⁷) or
6 built-in electric field (bias tunability in electrostriction ²⁸). Despite their great promise, these
7 technologies remain limited by either modest strain sensitivities (typically 2000–3000 ^{4,5}), low
8 piezoelectric constants (effective $d_{31} \approx -0.013$ pC/V ²⁵), or instable operation due to fragile size
9 effect ²⁷. Thus, achieving strong piezotronic modulation in a CMOS-compatible architecture
10 remains a significant challenge.
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17 In this work, we propose a wafer-scale mechanical stacking strategy that enables epitaxial-
18 free construction of Si/GaN heterojunctions with uniform pressure transfer, stable interfaces,
19 and piezotronic modulation. This approach is demonstrated in both n-Si/n-GaN (nn junction)
20 and p-Si/n-GaN (pn junction) configurations, which reveal distinct transport characteristics and
21 enable tunable piezotronic response through bias and doping engineering. The resulting
22 piezotronic transistors exhibit ultrahigh pressure sensitivity, ultrafast response, and exceptional
23 gauge factors. To further illustrate the versatility of this stacking devices, we demonstrate two
24 applications including high-speed impact force detection and stable tactile sensing, which
25 highlights the potential of this CMOS-compatible platform for scalable heterogeneous
26 integration in intelligent sensing systems.
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38 2. RESULTS AND DISCUSSION

39 2.1 Wafer-Scale Epitaxial-Free Si/GaN Heterojunctions via Mechanical Stacking

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41 The centrosymmetric crystal Si is non-piezoelectric with weak mechanolectrical coupling
42 ^{11,12}. To enhance its sensing performance, wurtzite GaN is used for combination due to its
43 technological maturity, excellent piezoelectric response and mechanical features ²⁹. However,
44 conventional epitaxial growth of Si/GaN heterostructures is hampered by significant lattice-
45 and thermal-mismatch ²⁴. Alternatively, we here employ an approach referred as "mechanical
46 contacting", for which, polished Si and GaN wafers are contacted face-to-face to form
47 heterojunctions by mechanical compression, as illustrated in Fig 1(a). Small pieces of Al-coated
48 GaN and Si (~ 6 mm \times 3 mm in size) is used to form an overlap area (~ 4 mm \times 3 mm), with
49 the Al electrodes extending beyond the contact area [Fig 1(a-i)].
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4 Upon applying pressure on the top wafer (overlap area), Si/GaN stacked devices
5 undergoes three distinct regimes, including insulating, tunneling and piezotronic regimes [see
6 Note S1 and Fig S1]. Initially, at low pressure, a wide air gap persists between Si and GaN
7 surfaces, which prevents carrier transport under an applied bias, resulting in an insulating
8 regime ①. When increasing pressure, the air gap narrows to nanoscale and the carriers enable
9 tunnel between two surfaces, which is tunneling regime ②. Since the tunneling current
10 depends exponentially on barrier width (i.e., air gap)³⁰, the current grows sharply with pressure
11 [see Fig 1(a-iii), ②]. As pressure increases to a critical value P_0 , the air gap almost vanishes
12 with two semiconductors in direct contact with each other. Here, the tunneling is replaced by
13 piezotronic effects ③, where strain-induced piezoelectric charges at GaN interface control
14 carrier transport [see Fig 1(a-iii), ③]. Notably, regimes ① and ② are inherent to wafer-
15 contact heterojunction formation, and our focus lies on regime ③, where the piezotronic effect
16 governs device performance.
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30 2.2 Working Mechanism of Piezotronic Modulation

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32 Wurtzite GaN has a hexagonal honeycomb structure with inherent polarity along the (0001)
33 direction. When pressure is applied along this axis, polarization charges are induced at interface
34 to modulate the barrier and thereby govern carrier transport via piezotronic effect. Given the
35 shielding effect of free carriers, piezotronic response depends on semiconductor doping²¹. Here,
36 we fix n-GaN (resistivity: 100 Ω) as the piezotronic incentive layer, whereas the used Si
37 (resistivity: 20 ~ 300 Ω) is p- and n-doped with light and heavy doping for comparisons.
38 Moreover, the coated Al electrodes has been confirmed to have an Ohmic contact with both Si
39 and GaN [see Note S2 and Fig S2], and thereby, the device characteristics depend primarily on
40 interface.
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50 Although the intrinsic Si/GaN band offsets are identical for n- and p-type Si, the doping-
51 dependent depletion configuration and dominant carrier transport lead to distinct piezotronic
52 responses in the nn and pn stacked junctions (see Note S3 and Fig. S3). For n-Si/n-GaN stack,
53 a depletion region is formed in both materials with a high barrier. When subjected to pressure,
54 positive piezoelectric charges are induced and attract electrons toward the interface, lowering
55 the barrier and enhancing electron transport [Fig 1b, lower]. The distinct affinity energy
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4 between Si and GaN causes a large conduction band offset (~ 0.91 eV), which, together with
5 the formed interfacial barrier, leads to asymmetrical electron transport. This is confirmed
6 experimentally by the rectified I-V characteristic in Fig 1c for n-Si/n-GaN. As a comparison,
7 we also measure the case of n-Si/n-Si contact, which shows linear I-V characteristic. This
8 indicates no energy barrier formed at Si-Si interface, and n-GaN has influence on the electric
9 transport of n-Si/n-GaN device.
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15 Besides n-Si/n-GaN, the depletion region also exists in pn junctions. This pn junctions can
16 be expediently constructed by combining n-GaN with p-Si [see Fig 1d]. The diffusion of
17 electrons in n-GaN and holes in p-Si causes wide depletion region and thereby a prominent
18 rectified I-V curve [see Fig 1e]. Such rectified behavior is also observed in a p-Si/n-Si pn
19 junction, but has output current far higher (~ 300 times at $V = 2$ V) than that in p-Si/n-GaN [see
20 Fig 1e, inset]. The notably reduced current in p-Si/n-GaN arises from a barrier due to the band
21 offset and interfacial charges, that drastically suppresses carrier diffusion. This barrier is tunable
22 by pressure-induced piezoelectric charges due to weak shielding effect of depleted carriers [see
23 Fig 1d].
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34 **2.3 Mechanical Properties of Stacked Heterojunctions**

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36 To demonstrate the uniformity of stress distribution, we model the mechanical behavior
37 of stacked Si/GaN heterojunctions by using the simulation [the detail illustrated in Note S4].
38 To match practical device configuration, we construct 3 mm \times 8 mm \times 0.5 mm single crystal Si
39 and GaN films (5 μ m GaN on 495 μ m Al₂O₃ sapphire substrate), forming a stacked pattern with
40 a 3 mm \times 4 mm overlap region [see Fig 1f]. A pressure P is applied on the top surface of overlap
41 area. The cases of $P = 1$ and 2 MPa are displayed in Fig 1f-i. As we can see, the generated stress
42 increases with pressure, and shows high uniformity over the bulk, interface and bottom [see Fig
43 S4]. Slight fluctuation appears at narrow boundaries of bulk and interfaces due to the boundary
44 discontinuity³¹. However, the stress within the electrically active overlap region remains highly
45 uniform. The edge perturbation decays rapidly toward the interior, and the GaN layer receives
46 efficient pressure transfer from the external load. Therefore, the center and peripheral areas
47 contribute similarly to the measured current modulation, as verified by the stable I-V
48 characteristics measured in n-Si/n-GaN and p-Si/n-GaN.
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To further examine the internal mechanical response, we extract stress profiles along z axis (depth direction) at the center of overlap area [see Fig 1f-ii]. The slight reduction in stress from top to bottom arises from the wider contacting area (i.e., Si size) at low surfaces when putting on an objective table. In addition, the stress has an obvious jump at GaN-Si interface, which is due to their different elasticity modulus under the application of force [see Table S1]. This jump occurs also at GaN-sapphire (Al_2O_3) interface [Fig 1f, inset]. In spite of varied stress, their local distributions nearby interface remains highly uniform, with a high transferring efficiency from external pressure to interfacial stress [see Fig S5]. Taking $P = 2$ MPa as an illustration, the uniformity is $\sim 99.96\%$ and the transferring efficiency is $\sim 83.37\%$ at GaN layer. These results indicate that, heterojunctions based on mechanical stacking enable wafer-scale uniform pressure transfer and stable interfaces without the need for epitaxial growth, which, alongside strong piezoelectricity of GaN, provides an efficient and scalable platform for designing piezotronic sensors.

Next, we investigate the impact of the electrical properties for n-Si/n-GaN transistors. A home-made pressure stage is employed to apply and detect pressure subjected on the stacked wafer devices [see Note S5, Fig S6 and Method/Experiment]. This stage enables application of substantial pressure (up to ~ 100 MPa) until wafer fracture. Given the influence of shielding effect on piezotronic modulation, we compare devices with light and heavy doping for n-Si/n-GaN and p-Si/n-GaN.

2.4 The n-Si/n-GaN Piezotronic Transistors

The piezotronic effect on device performance is highly doping-dependent, as shown from the I-V characteristics of n-Si/n-GaN in Fig 2a and n⁺-Si/n-GaN in Fig 2b. The n-Si/n-GaN device shows notably pressure-dependent current, whereas n⁺-Si/n-GaN exhibits negligible change. Figure 2c summarizes the current-changed ratio $J(P)/J(P=0)$ at $V = 2$ V. For n-Si/n-GaN, the current increases 7.5-fold, far exceeding that of n⁺-Si/n-GaN. This indicates weak shielding effect of carrier in light doping n-Si/n-GaN that allows substantial barrier modulation even under small strain ($\sim 10^{-5}$ at 3.5 MPa) [see Fig 2d, upper]. By contrast, for heavy doping n⁺-Si/n-GaN, the Fermi-level is pinned in n⁺-Si layer [see Fig 2d, lower], causing high interfacial electron density that shields piezoelectric charge and suppresses the pressure

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4 response. Here, the band diagrams in Fig 2d are obtained at $V = 0$ via the simulation (see Note
5 S6). The doping-dependent screening mechanism can be described by the screening length
6 which has a pressured-induced change strongly depending on the doping (see Note S7 and Fig.
7 S8).
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11 Fermi-level pinning makes n⁺-Si behave like a quasi-metallic electrode, and the n⁺-Si/n-
12 GaN device shows a Schottky-diode-like I-V curves, which is exponential (thermionic emission)
13 at low bias and linear (Ohmic) at high bias [Fig 2b, inset]. The extracted Schottky barrier height
14 of 0.67 eV is much close to the theoretical 0.77 eV. In contrast, light doping n-Si/n-GaN hosts
15 a wide depletion region with higher barrier, sustaining thermionic emission and notable
16 piezotronic response even at higher bias (e.g., 2 V). The simulated band diagrams in Fig 2e
17 further confirm the asymmetrical transport of n-Si/n-GaN that arises from the band offset,
18 showing a barrier of 0.61 eV at $V = 1$ V but 1.04 eV at $V = -1$ V.
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27 The piezotronic effect is known to surpass the piezoresistive effect in device modulation
28 ³². Using mechanical stacking, we can readily verify it by comparing piezotronic n-Si/n-GaN
29 (n⁺-Si/n-GaN) transistors with piezoresistive n-Si/n-Si (n⁺-Si/n⁺-Si) devices [see Note S8 and
30 Fig S9]. The absence of piezoelectricity in n-Si/n-Si and n⁺-Si/n⁺-Si greatly suppresses
31 pressure-induced current changes. Such pressure insensitivity of n-Si/n-Si and n⁺-Si/n⁺-Si
32 implies the elimination of interfacial air gap during contact [Fig 1a-ii], demonstrating a stable
33 contact interface in mechanically stacked heterojunctions.
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40 Pressure sensitivity is evaluated by extracting the strain-induced barrier height change
41 $\Delta\Phi_{\text{BH}}$ from thermionic emission theory ³⁰
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$$44 \quad \Delta\Phi_{\text{BH}}(P, V) = -kT \ln \left[\frac{J(P, V)}{J(P_{\text{ref}}, V)} \right] \quad (1)$$

45 where the reference pressure is $P_{\text{ref}} = 0$ for all the cases, k is the Boltzmann constant, and $T =$
46 300 K. The pressure sensitivity is the change slop of barrier height and pressure [see Note S9].
47 Figure 2f shows that $\Delta\Phi_{\text{BH}}$ increases linearly with pressure for both devices at $V = 2$ V, giving
48 a sensitivity of 15.14 meV/MPa for n-Si/n-GaN, 28 times higher than n⁺-Si/n-GaN (0.54
49 meV/MPa).
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The piezotronic modulation depends not only on doping but also on bias-tunable interface depletion. Figure 2g presents the bias-dependent $\Delta\Phi_{\text{BH}}$ (upper) and pressure sensitivity (PS, lower). For n-Si/n-GaN (left), $\Delta\Phi_{\text{BH}}$ grows with reverse bias, but under forward bias exhibits a valley due likely to the competition of depletion region that is shrunk in n-GaN but expanded in n-Si [see Note S10 and Fig S11]. At 1.6 V, both $\Delta\Phi_{\text{BH}}$ and pressure sensitivity saturate, and the latter reaches 15.14 meV/MPa, comparable to 10.19 meV/MPa at reverse bias. However, situation becomes different for n⁺-Si/n-GaN (right), where the pressure sensitivity becomes saturated with high value (9.5 meV/MP) at reverse bias but ultralow value (0.54 meV/MP) at forward case. The tunability is up to 17.6 times, far higher than that reported in p-GaN/p-GaN (2 times)²⁰. This indicates n⁺-Si/n-GaN piezotronic sensor with an excellent switchable sensing performance by electrical way.

High pressure sensitivity also indicates an excellent strain sensor. Strain sensitivity is given by the gauge factor

$$GF(P, V) = \frac{\Delta J / J(P_{\text{ref}}, V)}{\varepsilon} \quad (2)$$

here the current change is $\Delta J = J(P, V) - J(P_{\text{ref}}, V)$, and the pressure-generated strain is $\varepsilon = P / E$, with the Young modulus $E = 352$ GPa for GaN [see Note S9]. The gauge factor shows similar bias dependence [see Fig S12]. At optimal bias (1.7 V for n-Si/n-GaN, -0.3 V for n⁺-Si/n-GaN), peak GF values reach 6.8×10^5 and 2.9×10^5 , respectively. These GF values are exceptionally high for wafer-scale devices and outperforms conventional Si-based sensors ($200 \sim 5000$)^{11,12,33}.

2.5 The p-Si/n-GaN Piezotronic Transistors

Besides homogeneously doped n-Si/n-GaN (nn junction), the piezotronic effect is also strong for heterogeneously doped systems (i.e., pn junctions). The I-V characteristics of p-Si/n-GaN and p⁺-Si/n-GaN are presented in Figs. 3a and 3b, respectively. Both transistors show the same rectification characteristic and pressure response of forward current. By contrast, the reverse current response to pressure is more significant in p-Si/n-GaN [see Figs 3a and 3b, inset], leading to a rectification ratio that decreases from 662.4 at 0 MPa to 41.5 at 3.5 MPa.

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4 Fig 3c plots their current-changed ratio at $V = -2$ V. As we can see, as pressure increases from
5 0 to 3.5 MPa, the ratio in p-Si/n-GaN increases to 27.2, far higher than that for p⁺-Si/n-GaN
6 (3.8). These results demonstrate that high doping enhances the shielding effect of free carriers,
7 thereby suppressing the piezotronic response.
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11 As a comparison with piezoresistive effect, both p-Si/n-Si and p⁺-Si/n⁺-Si devices are also
12 measured [see Note S8 and Fig S10]. Their I-V characteristics show the well-defined
13 rectification behavior, as well as the same high robust response to pressure. This result aligns
14 with the n-Si/n-Si and n⁺-Si/n⁺-Si devices, further demonstrating inferior modulation capability
15 of piezoresistive effect. Moreover, the pressure-insensitive I-V response in p-Si/n-Si and p⁺-
16 Si/n⁺-Si further confirms stable wafer-scale interface formation, which, combined with the
17 well-defined pn-junction characteristics, reinforce the effectiveness of mechanical stacking in
18 device fabrication.
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27 To explain bias-dependent piezotronic effect, we simulate the band diagrams of p-Si/n-
28 GaN in Fig 3d at $V = 1$ V (left) and -1 V (right). Under reverse bias ($V = -1$ V), the wide
29 depletion region hosts a strong built-in electric field that suppresses carrier diffusion. However,
30 this strong field severely bends the p-Si interfacial band, leading to hole depletion but electron
31 (minority carrier) accumulation. The accumulated electrons overcome interfacial barrier (due
32 to band offset) to enter n-GaN layer, causing thermionic emission and drastically increasing
33 reverse current. Meanwhile, strain-induced positive piezoelectric charges attract electrons
34 toward the interface, which enhances electron injection and simultaneously lowers the effective
35 barrier height. Consequently, the reverse current increases significantly with pressure. In
36 contrast, at forward bias ($V = +1$ V), the majority carriers are diffused into narrow depleted
37 region, greatly shielding pressure-induced piezoelectric charges and suppressing piezotronic
38 response.
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50 Figure 3e summarizes the barrier height change $\Delta\Phi_{BH}$ versus P for p-Si/n-GaN and p⁺-
51 Si/n-GaN at reverse bias $V = -2$ V. Both transistors display approximately linear $\Delta\Phi_{BH} \sim P$,
52 with pressure sensitivity of 24.29 meV/MPa for p-Si/n-GaN, much higher than 9.95 meV/MPa
53 for p⁺-Si/n-GaN. Despite high pressure sensitivity for p-Si/n-GaN, this value is not the
54 maximum one due to its bias dependence. To demonstrate this, we obtain the $\Delta\Phi_{BH}$ (upper)
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4 and optimal pressure sensitive (PS, lower) versus V in Fig 3f for p-Si/n-GaN (left) and p⁺-Si/n-
5 GaN (right). The detailed pressure sensitivity (and gauge factor) versus bias at different applied
6 pressure can be found in Fig S13. The $\Delta\Phi_{BH}$ shows bias dependence for both devices,
7 particularly at forward bias, where $\Delta\Phi_{BH}$ first increases, peaks, and then declines with bias.
8 The peak $\Delta\Phi_{BH}$ occurs at $V = 0.3 \sim 0.4$ V for p-Si/n-GaN but $V = 0.2 \sim 0.5$ V for p⁺-Si/n-GaN.
9 This peak behavior is also observed in p-GaN/p-GaN piezotronic transistors²⁰, but here, can be
10 attributed to the competition between diffusion and thermionic emission [see Note S12 and Fig
11 S14]. Such competition appears also at reverse bias with a steady peak $\Delta\Phi_{BH}$ at $V = -1.0 \sim 1.3$
12 V for p-Si/n-GaN but $V < -2$ V for p⁺-Si/n-GaN.

21 Due to the peak behavior in $\Delta\Phi_{BH}$, the maximum pressure sensitivity reaches as high as
22 43.34 meV/MPa for p-Si/n-GaN at $V = -1.40$ V [Fig 3f, lower left] and 28.03 meV/MPa for p⁺-
23 Si/n-GaN at $V = 0.54$ V [Fig 3f, lower right]. The p-Si/n-GaN has another peak of 29.79
24 meV/MPa at $V = 0.40$ V but decreases rapidly with bias before saturating at 7.59 meV/MPa.
25 This indicates that p-Si/n-GaN transistor also has a good electric tunability (~ 5.7 times) of
26 pressure sensing performance, similar to n⁺-Si/n-GaN (~ 17.6 times). The peak pressure
27 sensitivity is also observed for strain sensitivity (i.e., gauge factor) [see Fig S13]. Fig 3g shows
28 the optimal gauge factor versus pressure. The maximum GF reaches 5.8×10^6 for p-Si/n-GaN,
29 approximately 10 times higher than that of p⁺-Si/n-GaN. To verify device-to-device
30 repeatability and quantify uncertainty, we measure nine independently fabricated mechanically
31 stacked p-Si/n-GaN devices and compile statistics of the peak (highest) pressure sensitivity and
32 peak gauge factor, together with their statistical distribution (see Note S13 and Fig. S16-S18).
33 The results show consistent performance trends across devices, which supports the robustness
34 of the reported high sensitivity. Meanwhile, our n-Si/n-GaN devices also show nearly consistent
35 pressure response (low deviation) under different temperature and dark/light condition,
36 indicating their environmental robustness (see Note S14 and Fig. S19).

37 2.6 Sub-Millisecond Response and Sensing Performance Comparison

38 In the following, we demonstrate the stability and response property of Si/GaN piezotronic
39 transistors for nn and pn junction cases. A periodic square-wave pressure (frequency: 5 Hz)
40 driven by a piezo stack, is applied to the Si/GaN transistor under a bias voltage of 2 V, and the
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4 current response is simultaneously measured [see Fig S6 and Method/Experiment]. A baseline
5 pressure P_0 is subjected to the device, and the time-dependent current variation $\Delta I = I(P) -$
6 $I(P_0)$ is recorded at different $\Delta P = P - P_0$. The P_0 is fixed at 1.84 MPa for n-Si/n-GaN [see
7 Fig 4a, inset] and 2.50 MPa for p-Si/n-GaN [see Fig 4c, inset]. For both n-Si/n-GaN and p-Si/n-
8 GaN, ΔI exhibits a stable increase with growing ΔP . This suggests that even under dynamic
9 conditions, both piezotronic devices still retain excellent pressure-modulated performance. To
10 evaluate long-term stability, time-dependent ΔI is tested for n-Si/n-GaN ($\Delta P = 2.6$ MPa, Fig 4b)
11 and p-Si/n-GaN ($\Delta P = 1.6$ MPa, Fig 4d). The results show consistency in periodic current over
12 approximate 500 cycles. An enlarged view of five cycles further confirms the stable temporal
13 response of the current to pressure [Figs 4b and 4d, inset], indicating that the mechanically
14 stacked Si/GaN transistors maintain robust under dynamic operation.

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16 To determine the response and recovery times, time-dependent ΔI of n-Si/n-GaN in Fig
17 4e and p-Si/n-GaN in Fig 4g are measured within a single cycle. The results show that the n-
18 Si/n-GaN transistor exhibits a response (rise) time of 0.8 ms and a recovery (fall) time of 0.98
19 ms, both lower than 1 ms. These values are close to those of p-Si/n-GaN (1.22 ms for response
20 and 0.63 ms for recovery time). To further confirm these times, we plot a statistical response
21 and recovery time for n-Si/n-GaN (nn) and p-Si/n-GaN (pn) over applied pressure of 1 ~ 3 MPa
22 in Figs 4f and 4h, respectively. The statistical data is obtained from twenty consecutive periods.
23 The mean response(recovery) time is within 0.76 ~ 0.91 ms (0.95 ~ 1.11 ms) for n-Si/n-GaN,
24 and 1.09 ~ 1.24 ms (0.61 ~ 0.67 ms) for p-Si/n-GaN, showing high uniformity with sub-
25 millisecond response times.

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27 We further measure the dynamic response of the Si/GaN devices under high-frequency
28 mechanical excitation. Both n-Si/n-GaN and p-Si/n-GaN sensors show stable transient current
29 responses under periodic loading from 50 to 500 Hz, and the sub-millisecond response is
30 maintained (see Note S15 and Fig. S20). We note that, although self-powered vibration sensing
31 without external bias has been demonstrated in recent studies^{34,35}, our mechanically stacked
32 Si/GaN devices are not yet ready for reliable vibration detection. This is because robust
33 packaging is still unavailable and continuous vibration can destabilize the interface (e.g., micro-
34 slip and contact fluctuation).

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4 To compare response speed, Fig 4i summaries the response and recovery times of three
5 typical pressure sensors: piezotronic (red), piezoresistive (blue), and capacitive (green)
6 [detailed data listed in Table S3]. For most pressure sensors, the response time matches well
7 the recovery time (dashed diagonal line). In addition, piezoresistive sensors, based on graphene
8 ³⁶, PDMS ³⁷, and tissue paper ³⁸, typically exhibit response (or recovery) times in the range of
9 10-100 ms. Capacitive sensors, however, show significant variation depending on the material.
10 For example, twisted yarn-based sensors achieve an ultralow response time of 2 ms ³⁹, whereas
11 loofah sponge-based sensors exhibit much slower responses (290 ms) ⁴⁰. On the other hand,
12 some of reported piezotronic sensors have a relatively low response time (5–10 ms) ^{16,20,41,42}.
13 Nevertheless, our Si/GaN transistors, with sub-millisecond response and recovery times (≤ 1
14 ms), is fastest to date among all reported piezotronic transistors. This rapid response originates
15 from the wafer-scale materials, that possesses the exceptional hardness (Young modulus of 169
16 GPa for Si and 352 GPa for GaN) producing a minimal strain ($10^{-6} \sim 10^{-5}$), high-sufficient
17 pressure transfer, and low surface roughness, enabling the device to react swiftly to external
18 stimuli.

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21 To benchmark the overall sensing performance, we compare the pressure sensitivity (see
22 Fig 4j and Table S4) and gauge factor (see Fig 4k and Table S5) of the mechanically stacked
23 Si/GaN piezotronic transistors with representative state-of-the-art mechanical sensors. The p-
24 Si/n-GaN transistor exhibits a maximum pressure sensitivity of 43.34 meV/MPa, which is more
25 than twice that of wafer-scale p-GaN/p-GaN devices ²⁰ ($19.83 \text{ meV MPa}^{-1}$) and far higher than
26 GaN/Al₂O₃¹⁶ or bulk ZnO sensors⁴³ (≤ 5.6 and $0.12 \text{ meV MPa}^{-1}$, respectively). Meanwhile, its
27 gauge factor reaches 5.8×10^6 , far surpassing conventional Si nanowires (200 - 5000)^{11,12,33} and
28 bulk ZnO (800 ~ 1250)^{15,43} by three to four orders of magnitude, and even exceeding many
29 high-performance GaN thin-film^{44,45} or quantum-well devices (10^3-10^4)⁴⁶.

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32 There are several mainstream pressure sensors, including Si-based MEMS piezoresistive
33 and capacitive devices ⁴⁷⁻⁴⁹. Si piezoresistive MEMS sensors are widely commercialized
34 because they have simple readout circuits and mature packaging and compensation, which
35 provide good linearity and long-term stability ^{47,48}. Si capacitive MEMS sensors usually show
36 near-zero static power consumption because the sensor does not require bias current ⁴⁹.

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4 Heterojunction-based mechanical sensing has been widely studied in platforms such as Si/SiC
5 and 2D stacked materials. For instance, Si/SiC sensors are commonly implemented as
6 piezoresistive MEMS devices with robust operation, low hysteresis, and good linearity⁵⁰.
7
8 Meanwhile, 2D-material mechanical sensors are often constructed on soft substrates, where
9 strain transfer and interlayer coupling (including possible sliding in stacked heterostructures)
10 can influence calibration and uniformity^{51,52}. In contrast, our Si/GaN stacked devices use the
11 piezotronic effect, where piezoelectric polarization modulates the junction barrier and leads to
12 higher strain/pressure sensitivity through an exponential transport response. The rigid Si and
13 GaN wafers also support ultrafast dynamic response and enable wafer-scale processing through
14 epitaxial-free mechanical stacking. These high-performance features firmly establish the
15 mechanically stacked Si/GaN heterojunction as a new benchmark for CMOS-compatible
16 piezotronic sensing.
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28 **2.7 Demonstrations of Impact Force Detection and Tactile Sensing**

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30 To further demonstrate the versatility of the stacked Si/GaN heterojunctions, we explore
31 two representative application scenarios in Fig 5, i.e., impact force detection and tactile sensing.
32 Leveraging the high stiffness of wafers and the sub-millisecond electrical response, the devices
33 are well suited for capturing transient mechanical impacts. To emulate tapping processes, we
34 apply periodic pulsed forces to the n-Si/n-GaN heterojunction using a piezo stack actuator
35 under impulse voltage stimuli [see Fig 5a]. For device at a fixed bias of 5 V, the output current
36 in Fig 5b exhibits stable and repeatable spikes with time that coincides with the applied force
37 pulses over multiple cycles. A magnified single cycle shows that the sharp current spike occurs
38 within ~1% of the pulse duration [see Fig 5c], precisely overlapping with the applied force
39 profile, demonstrating the ultrafast detection capability. Tests under varied pulsed force
40 amplitudes shows in Fig 5d that the peak current increases stably with the applied load.
41 Meanwhile, statistical peak current at different pulsed forces in Fig 5e displays narrow region
42 with excellent reproducibility. These results highlight the ability of the Si/GaN heterojunctions
43 to function as robust high-speed impact sensors, capable of distinguishing different impulsive
44 forces with high fidelity.
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Beyond transient impact events, we further evaluate the devices as robot tactile sense for continuous pressure monitoring [see Fig 5f]. To mimic this functionality, the stacked Si/GaN heterojunction is mounted on the fingertip of a human hand using a thin adhesive patch, and a soft elastic ball is compressed against it. When the finger gradually compresses a soft elastomeric ball, the device produces continuous current variations reflecting the increasing contact force. As shown in Fig 5g, the current rises steadily during the grip phase and decreased reversibly upon release, indicating robust bidirectional detection of applied and released forces. Under repeated grip-release cycles [see Fig 5h], the current response remains good consistent in amplitude and temporal profile, confirming excellent stability and repeatability. Additional tests involving different grip-release rhythm [see Note S17 and Fig S21] further verifies the capability for real-time monitoring of complex tactile interactions. Actually, wearable tactile application has widely reported based on flexible piezoresistive and capacitive sensors^{53,54}. However, due to the soft materials, most flexible sensors are difficult to realize fast response. The combination of wafer-scale fabrication, ultrafast response, and stable operation underscores the promise of Si/GaN heterojunctions as building blocks for tactile feedback in human-machine interfaces and soft robotics.

3. CONCLUSION

In summary, we demonstrate an epitaxial-free mechanical stacking strategy to realize wafer-scale Si/GaN heterojunctions with strong piezotronic modulation. Various devices have been constructed including nn and pn junctions of Si/GaN and Si/Si combinations. Our piezotronic transistors possess high pressure sensitivity of 43.34 meV MPa⁻¹, exceptional gauge factor of 5.8×10^6 , sensitivity tunability of 17.6 times, and sub-millisecond response times, far exceeding conventional Si piezoresistive and other piezotronic sensors. Practical applications are validated for impact detection, where transient pulsed force is precisely captured, and tactile sensing, where fingertip-mounted devices reliably track grip-release motions on a soft ball. These demonstrations highlight the capability of stacked Si/GaN junctions for both transient and continuous force monitoring. Our mechanical stacking strategy establishes a scalable pathway for epitaxial-free integration of dissimilar semiconductors, paving the way toward CMOS-compatible piezotronic sensors with high performance.

Acknowledgements

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4. METHOD/EXPERIMENT

4.1 Si and GaN Single-Crystal Wafer Materials

The (100)-oriented single-crystal Si wafers (Hefei Kejing Materials Technology) were grown using Czochralski method. The wafers include four types, i.e., p-type (B-doped; 1-10 $\Omega\cdot\text{cm}$ for light doping, and 0.001-0.005 $\Omega\cdot\text{cm}$ for heavy doping) and n-type (P-doped: 1-10 $\Omega\cdot\text{cm}$ for light doping; As-doped: 0.001-0.005 $\Omega\cdot\text{cm}$ for heavy doping). Si wafers have basic parameters including cubic structure ($a = 5.4301 \text{ \AA}$), single-side polished ($R_a < 10 \text{ \AA}$), 4-inch diameter, 0.5 mm thickness. The (0001)-oriented GaN wafers (Suzhou Nanowin) were grown on sapphire substrates ($\sim 650 \mu\text{m}$) via MOCVD with film thickness of 4.5 μm . The used GaN wafers have 4-inch diameter, single-side polished. At 300K, n-type GaN (Si-doped) has resistivity $\rho > 0.5 \Omega\cdot\text{cm}$ and $n < 2 \times 10^{17} \text{ cm}^{-3}$, while p-type GaN (Mg-doped) exhibits $\rho < 10 \Omega\cdot\text{cm}$ and $p > 2 \times 10^{17} \text{ cm}^{-3}$.

4.2 Device Fabrication of Si/GaN Piezotronic Transistor

Commercial Si and GaN wafers were diced into 3 mm \times 6 mm pieces using a diamond knife. The samples underwent sequential ultrasonic cleaning in acetone ($\sim 3 \text{ min}$), ethanol ($\sim 5 \text{ min}$), and deionized water ($\sim 5 \text{ min}$), followed by 80-s oxygen plasma treatment. Al electrodes were deposited within 5 minutes via the magnetron sputtering to form Ohmic contacts. The I-V measurements confirmed (approximately) linear characteristics for all Al/Si/Al and Al/GaN/Al configurations (p-type, n-type, and their doped variants), verifying the formation of Ohmic contact [see Fig S2]. After these preparatory tasks, GaN wafers were flip-mounted onto the surface of Si wafer with large overlapping areas, keeping electrodes exposed.

4.3 Application of Static and Dynamic Pressure to Stacked Devices

Herein, mechanical pressure was applied to the material using a home-made pressure stage [see Note S5 and Fig S6]. The core assembly consists of a threaded screw coupled with a movable iron pillar, where the Si/GaN heterojunction sample is mounted between the lower pillar and a rigid backing block. Clockwise rotation of the upper nut induces downward displacement of the screw, thereby transmitting uniaxial force to the sample (static pressure). To prevent torque-induced sample rotation and ensure mechanical stability, anti-rotation clips

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4 were incorporated on both sides of the iron pillar. In addition to the static pressure, dynamic
5 forces were introduced using a piezoelectric stack actuator, providing a high-frequency and
6 precise control of force variation. This actuator, integrated into the pressure stage, allows the
7 generation of dynamic, periodic pressure fluctuations (such as square-wave and impulse
8 pressure signals), which can be applied to the Si/GaN heterojunction under electrical control.
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13 14 15 **4.4 Electrical Measurements of Si/GaN Piezotronic Transistors**

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17 The electrical measurements were performed using a suite of specialized instruments,
18 including low-noise preamplifiers (SR570, Stanford Research Systems), Keithley 2614b digital
19 source meter, a piezo stack equipped with a controller (PSt150/10×10/20L, E53.C1K-H,
20 CoreMorrow), and a digital oscilloscope (Tektronix TBS1000X Series). The Keithley source
21 meter was used to measure I-V characteristics at a voltage range of -2 to +2 V, with 20 mV
22 increments. Under periodic dynamic pressure conditions, the output current was measured with
23 high temporal resolution using an SR570 amplifier combined with digital oscilloscope.
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31 32 **4.5 Simulations of Device Physics and Mechanical Properties**

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34 We numerically simulated the modulation of band diagram and carrier distributions in (nn
35 and pn) Si/GaN heterojunctions by pressure using COMSOL Multiphysics, a semiconductor
36 device physics simulation software [see Note S6]. The simulations were performed through
37 self-consistent solutions of semiconductor physics equations coupled with Poisson equation. A
38 one-dimensional device model is modeled, and pressure-induced piezoelectric charges are
39 implemented as interfacial charge density at the Si/GaN interface, with Ohmic contacts
40 imposed on both terminals. Furthermore, we also employ the solid-state physics module to
41 simulate the strain distribution across the Si/GaN heterojunction under external pressure
42 loading [see Note S4]. All simulated material parameters are summarized in Table S1 and S2.
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51 **ASSOCIATED CONTENT**

52 **Supporting Information**

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54 The Supporting Information is available free of charge at XXXXXX

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56 Contacting process and conduction regimes in wafer-stacked Si/GaN heterojunctions; ohmic
57 contact of Al electrodes with Si and GaN; origin of distinct piezotronic responses in n-Si/n-
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3 GaN and p-Si/n-GaN; finite-element simulation of stress distribution in Si/GaN mechanically
4 stacked heterojunctions; pressure stage for application of pressure on Si/GaN heterojunctions;
5 simulations of Si/GaN piezotronic transistors; the shielding length of piezoelectric charges and
6 doping; comparison of piezotronic and piezoresistive modulation; calculation formulas and
7 parameter sources for pressure sensitivity and gauge factor; competition of depletion regions
8 and shielding effect in n-Si/n-GaN; bias-dependent pressures sensitivity and gauge factor; the
9 competition of diffusion and thermionic emission in p-Si/n-GaN; device-to-device repeatability
10 and uncertainty of peak pressure sensitivity and gauge factor; high-frequency dynamic response
11 and bandwidth verification; performance comparison of response time, pressure sensitivity and
12 gauge factor; tactile sensing under varied grip force and motion rhythm.
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Figures and Captions

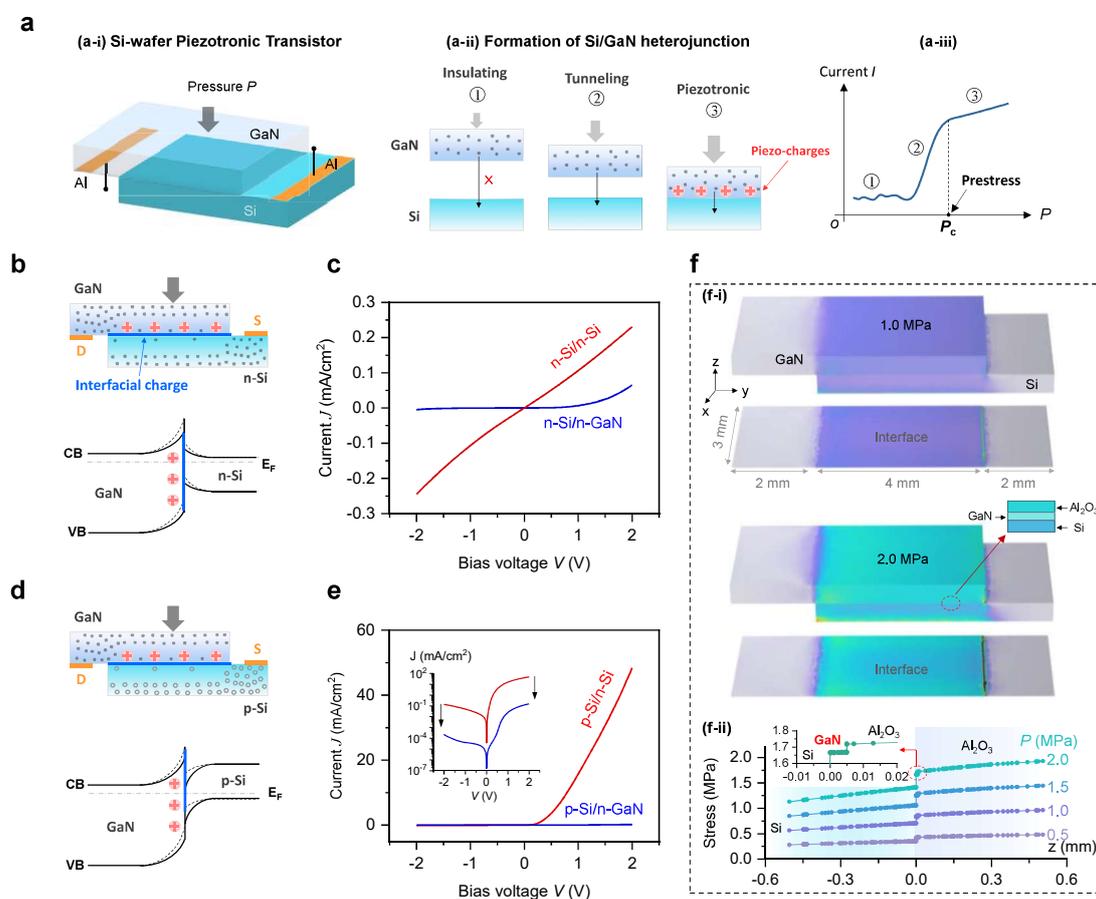


Figure 1. Epitaxial-free, wafer-scale Si/GaN heterojunctions using mechanical stacking. (a) Schematic of the Si/GaN heterojunction (a-i), and its formation process with three pressure-dependent conductivity regimes, including insulating, tunneling, and piezotronic (a-ii), and corresponding current-pressure response (a-iii). Carrier distribution and band diagram for n-Si/n-GaN (b) and p-Si/n-GaN (d) before (solid) and after (dashed) pressure application. Measured I-V characteristics for (c) n-Si/n-Si and n-Si/n-GaN, and (e) p-Si/n-Si and p-Si/n-GaN, with its logarithmic I-V plots (inset). (f) Simulation of stress distribution for Si/GaN heterojunction. 3D bulk and interface mechanical profile are shown under an external pressure of 1 and 2 MPa (f-i), and stress is distributed along depth (z) direction at the center of overlap area (f-ii), with an enlargement at interface (inset, 2 MPa).

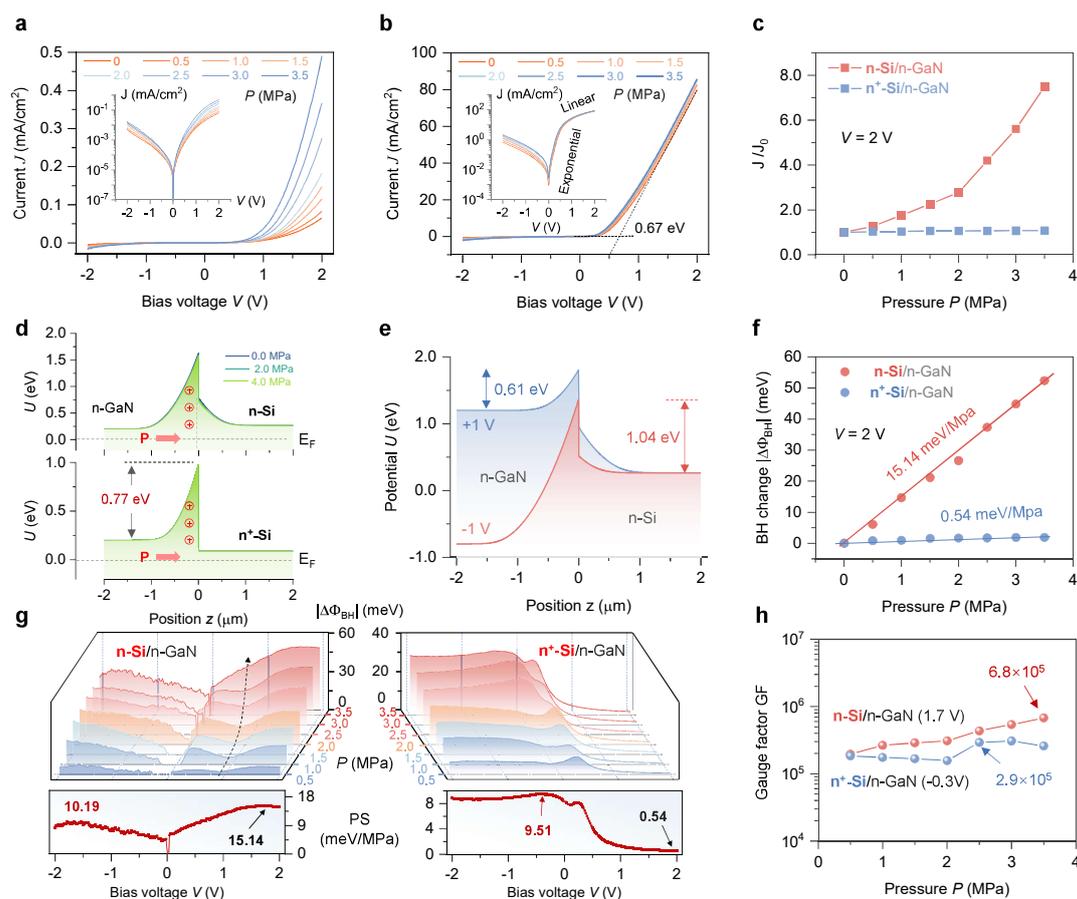


Figure 2. Piezotronic modulation in nn junctions. The I-V characteristics of n-Si/n-GaN (a) and n⁺-Si/n-GaN (b) stacks, and their logarithmic plots (inset). (c) The current-changed ratio versus pressure under bias voltage of $V = 2$ V. (d) Zero-bias band diagrams under pressure of 0, 2, and 4 MPa for n-Si/n-GaN (top) and n⁺-Si/n-GaN (bottom). The barrier height is 0.77 eV for n⁺-Si/n-GaN. (e) Simulated band diagrams of n-Si/n-GaN at $V = \pm 1$ V. (f) The change of barrier height $\Delta\Phi_{\text{BH}}$ against pressure at $V = 2$ V, yielding pressure sensitivities of 15.14 meV/MPa (n-Si/n-GaN) and 0.54 meV/MPa (n⁺-Si/n-GaN). (g) Bias-dependent $\Delta\Phi_{\text{BH}}$ (top) and pressure sensitivity (bottom) for n-Si/n-GaN (left) and n⁺-Si/n-GaN (right). (h) Gauge factor versus pressure for n-Si/n-GaN ($V = 1.7$ V) and n⁺-Si/n-GaN ($V = -0.3$ V).

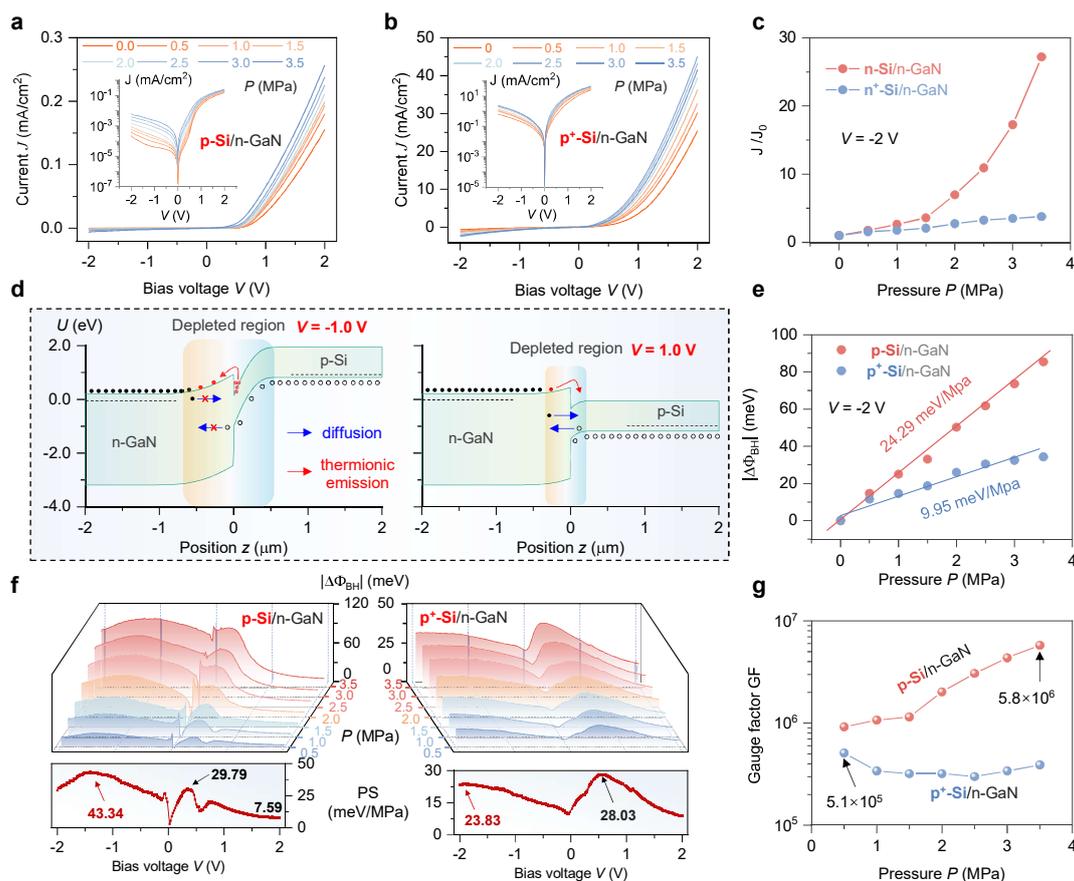


Figure 3. Piezotronic modulation in pn junctions. The I-V characteristics of p-Si/n-GaN (a) and p⁺-Si/n-GaN (b), with logarithmic plots (inset). (c) The current-changed ratio against pressure under bias voltage of $V = -2$ V. (d) Simulated band diagrams of p-Si/n-GaN at $V = -1$ V (left) and $+1$ V (right). (e) The pressure-dependent change of barrier height $\Delta\Phi_{BH}$ with linear slopes of 24.29 meV/MPa for p-Si/n-GaN and 9.95 meV/MPa for p⁺-Si/n-GaN. (f) $\Delta\Phi_{BH}$ (upper) and optimized pressure sensitivity (lower) as a function of bias voltage for p-Si/n-GaN (left) and p⁺-Si/n-GaN (right). (g) Optimized gauge factor versus pressure.

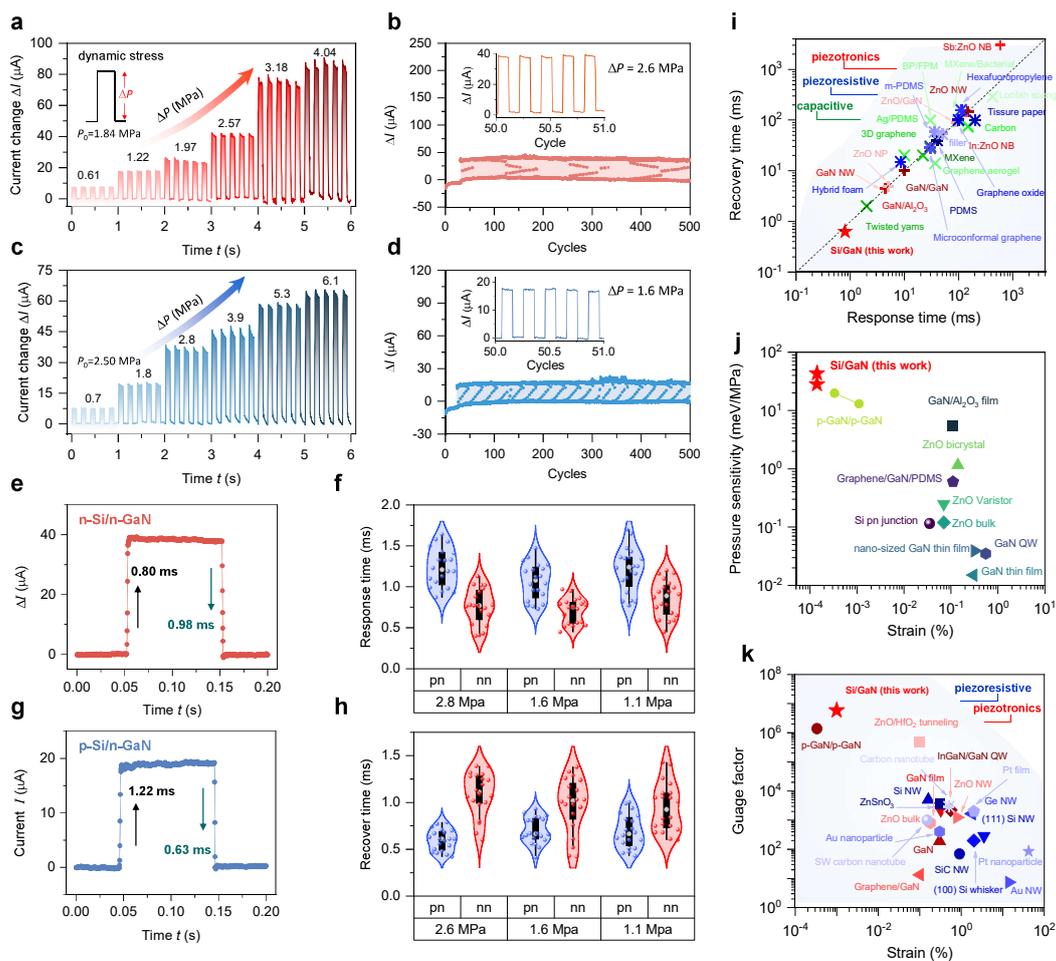


Figure 4. Dynamic response and performance comparison of mechanical stacking Si/GaN piezotronic transistors. The response of current variation (ΔI) to pressure ΔP at 5 Hz, with a baseline pressure $P_0 = 1.84$ MPa for n-Si/n-GaN (b) and $P_0 = 2.50$ MPa for p-Si/n-GaN (c). Long-term ΔI under repeated pressure loading of $\Delta P = 2.6$ MPa for n-Si/n-GaN (c) and $\Delta P = 1.6$ MPa for p-Si/n-GaN (d), with an enlarged view of five cycles (inset). Dynamical response in a single cycle for n-Si/n-GaN (e) and p-Si/n-GaN (g), and their statistical response (f) and recovery times (h) over twenty cycles. (i) The comparison of response/recovery times of Si/GaN with other piezoresistive, piezotronic, and capacitive pressure sensors. (j) Pressure sensitivity comparison between Si/GaN and reported bulk-material-based sensors. (k) Gauge factor comparison of Si/GaN with piezoresistive (Si, Ge, Au, Pt) and piezotronic strain sensors.

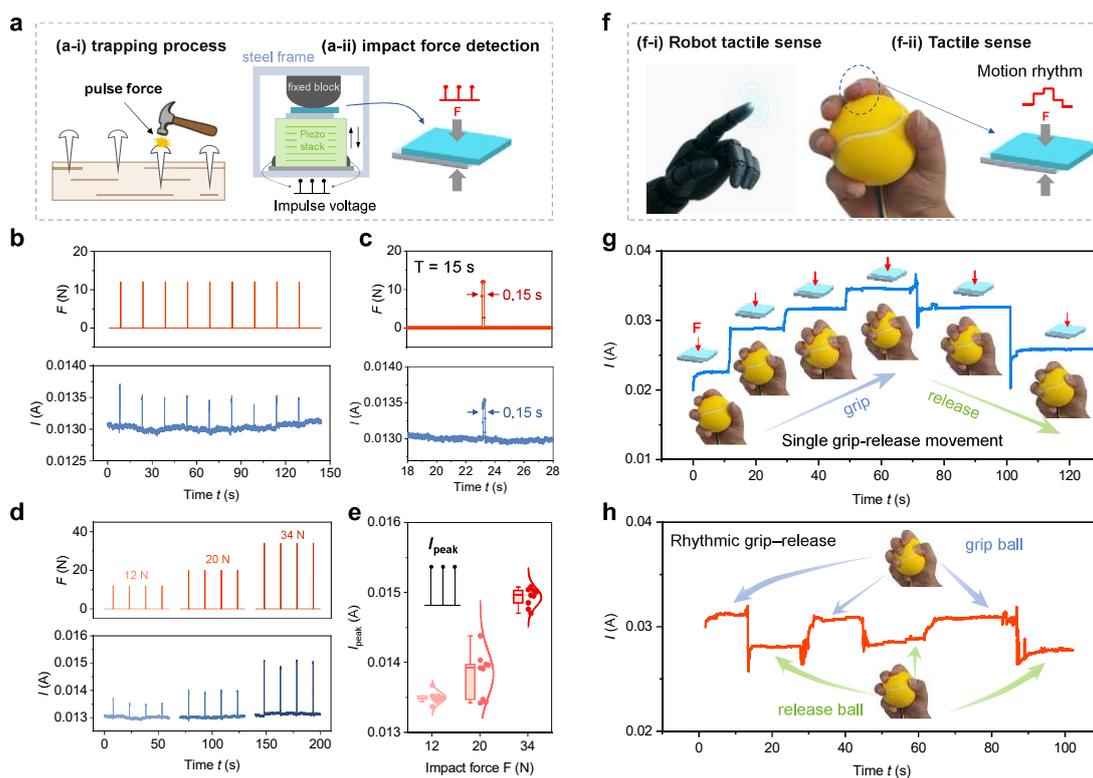


Figure 5. Impact force detection and tactile sensing using Si/GaN piezotronic devices. (a) Schematic of trapping process (a-i), where periodic pulsed forces are applied on the Si/GaN device using a piezo stack to mimic tapping-induced impacts (a-ii). (b) Time-resolved current response under repetitive pulsed forces over several cycles at a fixed bias of 5 V. (c) Enlarged view of a single cycle (period of $T = 15$ s) with the temporal correlation between the applied force pulse ($\sim 1\%$ of the cycle) and the current response. (d) Current response as a function of different pulsed force amplitudes. (e) Statistical distribution of peak current signals (inset) under varied pulse forces. (f) Photograph of robot tactile sense (f-i) and schematic of a tactile sensing demonstration, where the stacked Si/GaN device is mounted on a human fingertip to probe the force applied on a soft ball (f-ii). (g) Current response during a single grip-release movement with real-time detection of increasing pressure followed by gradual release. (h) Current response during repeated pressing-releasing cycles.

TOC Graphic

