A Comparison of Plasma and Mechanical Dicing of Indium Phosphide

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Abstract

Compound semiconductor materials such as Indium Phosphide (InP) are widely used in devices such as optoelectronic devices. As these materials and devices become more advanced they become increasingly expensive to fabricate. These high fabrication costs mean that yield has to be high to reduce wasted material. These demands necessitate the need for a lower defect inducing dicing method as an alternative to conventional saw dicing. This work focuses on developing a novel dicing process for InP using an inductively coupled plasma reactive ion etcher (ICP-RIE). A SiO_2 hard mask as well as two photoresist masks SU-8 and polyimide were evaluated under two different plasma chemistries to etch InP. The aim of the work was a >100 µm deep etch to show that plasma dicing is applicable to InP. As the work was focused on dicing a particular focus was placed on achieving a high etch rate and selectivity while still maintaining a vertical anisotropic etch. The concept was first demonstrated on a 15 mm by 15 mm piece using an SU-8 mask with a HBr plasma chemistry, an etch depth of 137.75 ± 9.95 µm was achieved in 60 minutes, corresponding to an average etch rate of 2.30 ± 0.15 µm/min and a selectivity of 20.9:1. Scaling the up the surface area to a 25 mm by 25 mm pieces only reduced the etch rate by 0.32 µm/min, indicating the process can be extended to whole wafer dicing. Post-etch removal of the SU-8 mask was also investigated with P1316 yielding the lowest surface roughness of the removal methods trialled (5.68 nm compared to the original 3.19 nm). Plasma induced defects were assessed and compared with a saw diced sample. Saw dicing exhibited defect regions with reduced recombination efficiency extending from 1 µm at 5 keV to >4 µm at 20 keV on both sides of the trench. In contrast, the average defect region width was 2 µm and 1.28 µm for the HBr and Cl/Ar chemistry respectively. These results have demonstrated that plasma dicing is a applicable process for low defect die singulation of InP.

Declarations

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

Signed.....[redacted].....

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This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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I hereby give consent for my thesis, if accepted, to be available for electronic sharing **after expiry of a bar on access approved by the Swansea University.**

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Abbreviations

AFM	Atomic force microscopy
CD	Critical dimensions
CL	Cathodoluminescence
Cl	Chlorine
CVD	Chemical vapour deposition
Cz	Czochalski
DI	Deionized water
ESC	Electrostatic chuck
FWHM	Full width at half maximum
HBr	Hydrogen Bromide
HEMT	High electron mobility transistors
HF	Hydrofluoric acid
ICP	Inductively coupled plasma
InP	Indium Phosphide
IPA	Isopropyl alcohol
PEB	Post exposure bake

RIE	Reactive ion etcher
RMS	Root mean square
SCCM	Standard cubic centimetre
SEM	Scanning electron microscope
Si	Silicon
UV	Ultraviolet

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Chapter 1

Introduction

Indium phosphide (InP) is a semiconductor material with unique properties that have applications in high-speed electronics, optoelectronic components and photonics. The current widely used method to dice InP wafers is saw dicing however this has many disadvantages including: introducing mechanical stress to the wafer that can ultimately lead to defects, wasted material due to the wide profile of the saw blade, high cost of the diamond tipped saw blade and water cooling requirements to reduce the thermal energy transferred to the wafer. This work aims to dice InP wafers by plasma etching specifically using an inductively coupled plasma reactive ion etcher (ICP-RIE). This method has many advantages compared to saw dicing such as: less mechanical stress meaning less defects, high precision, higher yield due to less damage and more die per wafer using smaller dicing lanes. ICP parameters are investigated for their effect on the etch profile alongside different masking materials to find the optimal process. The optimal process providing an anisotropic, fast etch rate and high selectivity. Once an optimal process was determined the aforementioned benefit of defect reduction was investigated using cathodoluminescence to image and compare defects between plasma diced samples and a saw diced sample.

1.1 Scope of Thesis

The primary aim of the work was to evaluate plasma dicing as a viable alternative to conventional saw dicing. To demonstrate this different masking materials were fabricated to compare their performance when plasma etching. The SU-8 photoresist mask was fabricated using photolithography with parameters first being optimised for silicon (Si) then subsequently transferred to InP. A 125NXT photoresist was also fabricated in order to etch a SiO_2 hard mask. This SU-8 photoresist mask and SiO_2 hard mask were compared as well as a polyimide mask provided by the KLA corporation. The effectiveness of these masking materials was assessed in terms of selectivity and stability when exposed to plasma for prolonged periods of time. The recipe development for the deep etching of InP was completed using an ICP. Two different plasma chemistries were trialled on the different masked pieces with their respective recipe developments being discussed. Different methods of removing crosslinked SU-8 photoresist after being plasma treated are discussed. Finally, cathodoluminescence was used to compare defects between the plasma etched and saw diced InP.

Chapter 2

Background

2.1 Semiconductor materials

Semiconductors are materials that have conduction properties between that of an insulator and a conductor. Chemically pure semiconductors are referred to as "intrinsic" semiconductors and have an equal number of negative charge carriers (electrons) and positive charge carriers (holes). Intrinsic semiconductors tend to have poor conductivity and their conductive properties are highly temperature dependent. To improve conductivity, intentional chemical impurities are introduced referred to as "doping". Once doped the semiconductor is then referred to as an "extrinsic" semiconductor. Selective doping can alter the conductivity of a semiconducting material to be more insulating or conductive. [1]

2.1.1 Compound semiconductors

Inorganic semiconductors separated into two categories elemental or compound semiconductors. Elemental semiconductors are comprised of a single element with notable examples being Silicon (Si) and Germanium (Ge). Compound semiconductors on the other hand are comprised of two or more different elements (A and B) such as Indium phosphide (InP) or gallium Nitride (GaN) [2]. A simple rule of thumb for predicting semiconducting behaviour is if the sum of the

elemental group numbers of the constituent elements, divided by the number of unique elements equals four, then the compound is likely to be a semiconductor. Both elemental and compound semiconductors have tetrahedral covalent bonds due to their hybridised sp^3 orbitals but compound semiconductors also have additional ionic bonds arising due to the difference in electronegativity between elements. These tetrahedral bonds give rise to the distinct crystal lattice structures of compound semiconductors being either zincblende (Zb) or wurtzite (Wz). A zincblende crystal lattice structure closely resembles a diamond structure, which is the crystal structure of elemental semiconductors. Both A and B atoms form a face centred cubic lattice such that A atoms are surrounded by 4 B atoms due to the tetrahedral bonds. The inverse is true for B atoms. Rotating the Zb structure 180° along the [111] axes gives the Wz structure. This structure forms due to both A and B atoms forming a hexagonal lattice. Again due to the tetrahedral bonds, A atoms are surrounded by 4 neighbouring B atoms and vice versa for B atoms. This structure is more common amongst compounds with higher ionic bond energy. Ternary compound semiconductors form a structure similar to zincblende named chalcopyrite with the caveat that there cation sites are replaced alternating group I and III elements for I-III-VI_2 and for II-IV-V_2 group II and IV [3].

2.1.2 Bandgap

A "bandgap" is a fundamental property of solid state materials such as semiconductors and insulators. The bandgap refers to difference in energy between the top of the highest occupied state at 0 K (valence band edge) and the bottom of the lowest unoccupied state (conduction band edge). This bandgap can either be direct or indirect depending on the absorption process. For direct bandgap semiconductors, the valence band edge and conduction band edge occur at the same quantum number k or wave-vector. This means the optical transition is direct as there's no significant change in the wavevector. For the indirect bandgap semiconductor a optical transition also involves a phonon to conserve momentum.

2.2 Indium Phosphide

2.2.1 Properties

Indium phosphide (InP) is a III-V compound semiconductor with a direct band gap [4,5]. InP has a band gap of 1.42 eV or 1.35 eV at room temperature depending on it's crystalline form of either Wz or Zb, respectively [4]. The latter InP crystal structure in particular has one of the longest lived optical phonons compared to other Zb compound semiconductors [6]. Long-lived phonons could be particularity useful for applications such as quantum computing, metrology as well as ultra-fast optical data processing [7].

2.2.2 Production

InP crystal growth can be traced back to the late 1950s, when researchers first demonstrated methods of preparing single crystal InP. Herman et al presented a method of reacting Indium and phosphorous within a sealed quartz tube within a series of temperature controlled furnaces. A furnace set to 1000°C with an adjacent furnace set to 1060°C provides a temperature gradient which is maintained across the Indium crucible while an additional furnace influences the pressure of the phosphorous vapour. Through a process known as directional recrystallisation InP crystals are subsequently formed at the cooler end of the Indium crucible. A crystal puller was also designed for this process addressing issues not present in pre-existing Czochalski (Cz) crystal pullers such as volatile phosphorus vapour [8].Between the late 1960s and early 1980s, liquid encapsulation Czochalski and vertical gradient freeze were used to grow InP crystals with both methods still being commonly used today [9, 10]. By the late 1990s both two and three inch bulk InP wafers were available for manufacturers. While the market for InP based devices was valued at $1 billion in 1998, the market for InP substrates was only $17 million. For comparison the InP substrate market was approximately one two hundredth of the Si wafer market and a tenth of the Gallium arsenide

(GaAs) market at this time. This discrepancy in device value and substrate value is most likely caused by the high usage in high value telecommunications as well as almost 40% of InP wafers being used for research and development [11, 12]. By 2021 this market had increased to $2.5 billion and is forecasted to more than double to $5.6 billion by 2027 due to further growth in datacom and telecom industries as well as emerging markets such as automotive LiDAR [13]. Despite four inch InP wafers being commercially available since the late 90s their adoption has been slow with <20% of InP wafer shipments being four inch in 2022 compared to two and three inch both of which having an almost even split of the remaining 80% of the shipment size. The reluctance of manufactures to switch to four inch wafers is primarily due to the poor return on investment when taking into account the high costs involved in transitioning equipment, namely their back end of the line (BEOL) equipment. The recent emergence of six inch InP wafers however provides a much greater return on investment for manufacturers allowing up to four times more chips per wafer compared to three inch wafers. This corresponds to a cost reduction per chip of up to 60% as well as being able to use pre-existing BEOL equipment from the vertical cavity surface emitting laser market [14–16].

2.2.3 Applications

InP High Electron Mobility Transistors (HEMTs)

Another intrinsic property of InP that out preforms other III-V compound semiconductors is the high electron mobility of InP which is approximately $4500\,\mathrm{cm^2V^{-1}s^{-1}}$ at $290\,^\circ\mathrm{K}$ [17]. As a result, lots of research has been put into high electron mobility transistors (HEMTs) grown on InP substrates [18]. InP HEMTs have the lowest noise particularly in the microwave wavelength range making them particularly good for applications such as sensitive low noise detectors [19]. The noise can be reduced further through cryogenic cooling as InP has a low thermal generation rate compared to other III-V semiconductors [20]. Typically at low temperatures traditional Si based power devices have an increased carrier mobil-

ity due to phonons having less thermal energy thus causing less electron-phonon interactions. A higher electron mobility should increase device performance but the carrier density is also decreased at low temperatures due to dopant freeze-out leading to shifts in device properties such as threshold voltage. The net result is marginal device performance gains or even device degradation. InP HEMTs on the other hand have much better performance at lower temperatures as they do not require doping to achieve high carrier concentrations [21].

Solar Cells

The Shockely-Queisser (SQ) limit is the maximum conversion efficiency a single bandgap material solar cell can achieve under a given spectrum of illumination. The original limit was calculated using a 6000 K black body spectrum as the source of illumination giving a maximum efficiency of 33% with the ideal bandgap being 1.1 eV [22]. Instead of approximating the sun as a black body, modern calculations of the SQ limit use a definition given by the American Society for Testing and Materials for the spectrum of sunlight. Two distributions are given for the terrestrial spectrum, one is the direct irradiance and the other is the irradiance on a 37° tilted surface. The latter of these distributions when applied to a solar cell at 25°C gives the standard solar cell test conditions. Applying these conditions gives a maximum conversion efficiency of light to power of 33.16% at a bandgap of 1.34 eV [23]. With a bandgap of 1.35 eV, InP is theoretically one of the most ideal materials for a solar cell [24]. However the current record is 24% efficiency for single crystalline InP solar cells. This is significantly lower than other III-V solar cells namely GaAs at 29% [25].

Photonics and Optoelectronics

The idea of a photonic integrated circuit (PICs) was first proposed in 1969 by Stewart Miller in which he envisioned "laser beam circuitry" [26]. PICs utilises light generating, modulation, amplification and detection components integrated into the integrated circuit to transmit data via photons where electrons would

previously have been used. The motivation for switching to PICs are mainly motivated by the issues stemming from traditional electrical interconnects such as, heat dissipation, latency and power consumption. In contrast, photons offer a much higher rate of data transfer as well as providing a greater protection from electromagnetic interference [27]. The main material platform being explored for PIC fabrication is Si due to compatibility with existing CMOS processes making the shift to large-scale fabrication more cost effective. However, the indirect bandgap of Si makes it unsuitable for laser and light emitting diode (LED) devices. The bandgap of Si also does not fall within the standard fibre optic telecommunications wavelengths being 1.3 µm or 1.55 µm. Due to these factors monolithic integration on a Si platform is currently not possible. To continue using Si hybrid integration with III-V semiconductors such as InP would be required. This hybrid integration approach would require laser structures being separated using a liftoff method from their native substrate then subsequently bonded onto Si or a layer of InP could be grown on Si and subsequently processed. Both techniques present their own sets of challenges. The relatively large lattice mismatch (4% for GaAs and 8% for InP) combined with the disparity in thermal expansion coefficients make direct growth of these compound layers difficult while maintaining the low defect density required for producing lasers. The liftoff method involves a chemical etch to liftoff the III-V structure which is then subsequently bonded via the van der Waals force to the Si wafer. This bond is then further improved using a wafer fusion process in which the wafer is exposed to a hydrogen atmosphere at 450°C while close contact between the Si wafer and III-V structure is maintained. This process leads to the formation of strong chemical bonds between the two materials [28]. Monolithic integration of InP on the other hand offers the unique benefit that all the components of a PIC such as lasers and detectors can be fabricated directly on the same InP substrate [29].

2.3 Device fabrication

When fabricating integrated circuits (ICs) hundreds of identical ICs are manufactured on the same wafer through a series of manufacturing steps. Wafers are mostly circular flat pieces of semiconductor material. Depending on the size of the wafer a notch or a primary and secondary flat are used to denote the crystal orientation [30]. Depending on the complexity of the ICs hundreds of processing steps are typically required in order to fabricate a complete IC. These processing steps can be broadly simplified to photolithography, etching and deposition. A typical process flow includes transferring a pattern using photolithography then selectively removing or adding material (etching and deposition). After these processing steps the wafer contains hundreds of identical ICs which are then singulated into die by dicing [31].

2.4 Photolithography

Photolithography is the process of transferring a pattern by projecting light through a transparent medium onto a photosensitive material typically a photoresist. Typically, ultraviolet (UV) light in the 350 to 450nm range is used. This specific range is common as mercury discharge lamps were commonly used as the UV source for photolithography before the advent of UV LEDs with mercury having a series of strongly emitting spectral lines in this range namely the i-line at 365nm [32, 33].

2.4.1 Photoresists

A photoresist has 2 possible tones also known as polarities. In a positive photoresist areas exposed to UV light undergo a chemical reaction increasing solubility. The soluble areas are then readily removed in the presence of developing solution leaving behind the unexposed regions. The opposite occurs in a negative photoresist where the exposed regions undergo a chemical reaction that decreases solubility meaning the unexposed regions are washed away by developer. Photore-

sists contain a resin,a photo-active compound (PAC), and a solvent. The solvent content dictates the viscosity of a photoresist. Solvents, such as ethyl lactate, comprise anywhere from 60 to 90 percent of the photoresist. Assuming constant exposure dose, as the wavelength of the exposure dose decreases the quantity of photons also decreases. This is because of the inverse relationship between photon energy and quantity. With less photons the amount of a photons interacting with a PAC decreases. Eventually the photosensitivity becomes too poor to consider use the photoresist. Chemical amplified photoresists (CAR) were formulated to alleviate this using a catalyst that is formed at the exposure step. This catalyst then causes a chain reaction making exposed areas more soluble (in a positive resist). Less common additives in a photoresist are quenchers and dyes. A quencher can be added to a CAR to neutralise acid that may diffuse into unexposed areas. This is particularly important as without control of the acid diffusion length then line edge roughness can increase from partially exposed areas being removed in developer [34]. SU-8 is a negative tone epoxy resin photoresist that was first discovered by IBM. The excellent mechanical properties of this resist means it is widely used in micro-electromechanical systems (MEMS) [35]. The EPON SU-8 resin by the Shell corporation used in SU-8 photoresists is comprised of 8 epoxy rings per monomer giving SU-8 its name as well as mechanical properties. SU-8 is a chemically amplified resist with cross-linking being induced by exposure to UV radiation and further cross-linking caused by exposure to heat [36].

2.4.2 The photolithography process flow

Cleaning

The crucial first step in photolithography is the cleaning step. Cleaning removes particulate contaminants which can lead to defects such as pinholes in the mask. Wafers are typically cleaned using wet methods in which chemicals are used are dependent on the type of contamination that is being removed. For example an undesirable native oxide layer can be removed using hydrofluoric acid.

Applying photoresist

Depending on the photoresist being used an adhesion promoter can be used to ensure the photoresist adheres to the surface of the wafer. A spin coater is used to apply this adhesion promoter with parameters such as spin acceleration and spin speed being controlled via software. To obtain a specified thickness the following relation is used

$$h = \frac{a}{\sqrt{\omega}} \tag{2.1}$$

where h is the final height or thickness, typically measured in microns, a is a constant determined experimentally, and ω is the spin speed or angular speed given in revolutions per minute (rpm). After an adhesion promoter is applied then the photoresist can be applied using the same principles as applying the adhesion promoter.

Soft baking

Once the photoresist is applied the next step is to remove the solvent in the photoresist in a step called soft baking or pre-baking. Both bake time and temperature depend on the photoresist being used.

Exposure

Since photoresist undergo chemical reactions when exposed to light, a photomask is used to selectively control which areas are exposed. A photomask is typically a thin layer of patterned chrome on glass either soda lime or fused silica. Depending on the tone of the photoresist being used the photomask is either referred to as a bright-field or dark-field mask. Bright-field photomasks are transparent with opaque patterns and are typically used in conjunction with negative tone photoresists. The transparent regions define the pattern being transferred as these areas are exposed to the UV radiation and become insoluble at the development stage. The inverse is true for dark-field photomasks used in conjunction with positive photoresists [37].Figure 2.1 depicts a brightfield mask that is used in conjunction

with a negative photoresist.

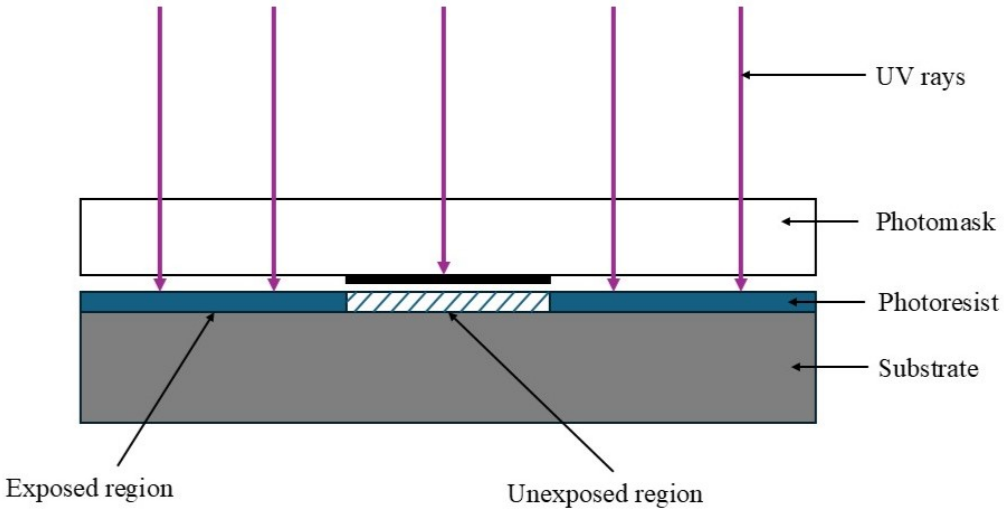


Figure 2.1: A diagram of a brightfield photomask used with a negative photoresist.

Post exposure bake

Depending on the photoresist, a baking step after exposure is sometimes required to promote additional chemical reactions. This process is referred to as a post exposure bake (PEB).

Development

After the PEB, the areas of the photoresist that are soluble are removed using a developer solution leaving behind the exposed area in a negative photoresist and unexposed area in a positive photoresist [38].

Hardbake

Another additional step is a hardbake. The hardbake is typically at a temperature above both the soft and post exposure bake. The hardbake removes volatile

organic compounds as well as any remaining water content. The hardbake occurs last due to these elevated temperature degrading the PACs [39].

2.5 Plasma processing

2.5.1 Plasma

A plasma forms when a molecular gas is sufficiently heated causing the molecular bonds to break leaving behind an atomic gas. Further heating adds more thermal energy to the gas allowing the electrons in the valence shell of the gas atoms to overcome the binding force leaving behind free electrons and ions with this being referred to as a plasma. This transition isn't a phase transition by the thermodynamic definition as this transition happens gradually as the temperature increases [40]. Despite the lack of a thermodynamically defined phase transition, plasma is still commonly referred to as the fourth state of matter due to the unique properties it exhibits. These unique properties mainly arise due to the dominance of the longer range Coulomb force for inter-particle reactions in a plasma compared to the comparatively short range Van der Waals in a neutral gas. As the Coulomb force is the dominant force, particles in the plasma can react simultaneously with other particles in the plasma. These simultaneous reactions give rise to a collective behaviours which are characteristic of a plasma and resemble the way red and white blood cells move in blood plasma which is how the name was derived [41].

2.5.2 Glow discharge plasma

A plasma etcher can be simplified to a parallel plate plasma reactor as depicted in Figure 2.2.

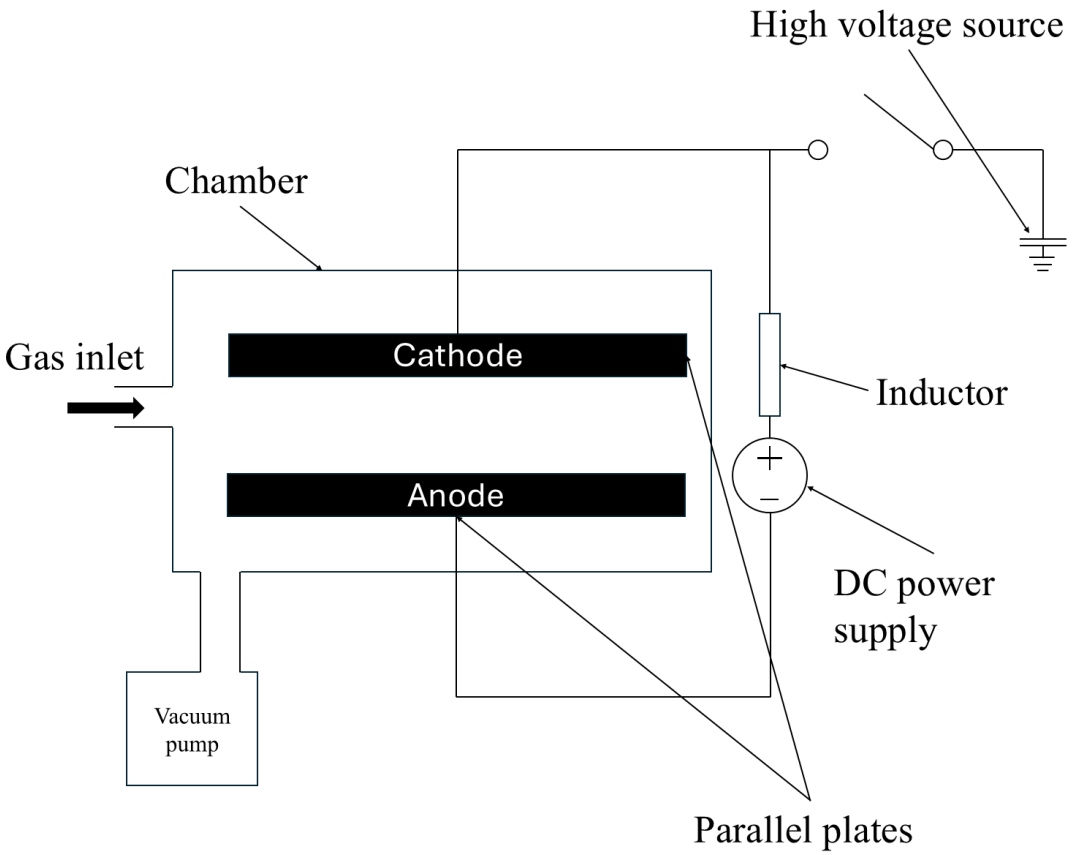


Figure 2.2: A diagram of a simple parallel plate plasma reactor.

In a simple plasma reactor, 2 parallel plates are connected to a DC power supply and contained within a vacuum. A high voltage source such as a charged capacitor is briefly connected. If the voltage is higher than the breakdown field of the gas then an arc is formed between the two plates. This arc ionizes the gas in the chamber leaving behind a plasma [42]. Electrons with their negative charge are attracted to the anode and the ions with their positive charge are drawn to the cathode. Once an ion strikes the cathode a cloud of secondary electrons are released which are then subsequently accelerated towards the anode. If

these electrons have a high enough energy (determined by the potential difference between plates), they can collide in-elastically with neutral atoms. This release of secondary electrons and the subsequent ionization of neutral atoms is what maintains the plasma after the initial arc. Electrons with an energy less than approximately 15 eV; however, excite the neutral atom rather than ionizing. This excited state is short lived and quickly decays back to its ground state emitting visible radiation. This visible radiation release is what provides the "glow" of a glow discharge plasma.

2.5.3 Chemical vapour deposition

Chemical vapour deposition (CVD) is a process in which a thin film of a material is deposited on a substrate via a chemical reaction. The chemical being used to deposit this material is referred to as a precursor and is selected based on properties such as vapour pressure and not forming an aggregate or reacting in the gas phase. The most common precursors are solid and liquid precursors as they more often meet the aforementioned criteria as opposed to gas precursors which rarely meet this criteria as well as having additional safety and storage concerns [43]. The first stage of CVD is converting the precursor to a gas. Depending on the phase of the precursor there are different ways of converting a precursor into a gas. Gaseous precursors are typically the easiest to control but storage and safety concerns make this type of precursor problematic for full scale production use. For liquid precursors, particularly more volatile precursors, a process called bubbling is used in which an inert carrier gas such as nitrogen is pumped into the liquid precursor. The carrier gas becomes saturated with the liquid precursor and is transported to the reactor chamber. For process requiring more precise deposition, the reactants are allowed time to stabilise before entering the reactor chamber. The gas flow is monitored and controlled through a combination of a mass flow controller above the bubbler and a manifold that can rapidly adjust the flow of gas into the chamber. For solid precursors higher temperatures than liquid precursors are typically required with heating above the sample's sublimation

temperature sometimes being a requirement as well. Heating of tubes and sensors is also required to avoid the vapour from condensing and potentially blocking the system [44, 45]. To reduce the temperature requirements of CVD a plasma can be introduced with the process being referred to as plasma-enhanced chemical vapour deposition (PECVD). The resulting plasma produces highly reactive species such as radicals, ions and excited neutral atoms. These species allow alternative chemical reactions to occur with lower activation energies [46].

2.5.4 Inductively coupled plasma

Inductively coupled plasma (ICP) systems are widly employed due to their ability to generate high density plasmas with low electrode bias. This high density plasma is generated through the use of a radio frequency (RF) coil connected to an alternating current (AC) power source. According to Amperes law, an AC flowing through the RF coil generates an alternating magnetic field. Which in turn induces an electric field within the plasma according to Faradays law. An electron with charge q in a magnetic field $\overline{B}$ is subject to the Lorentz force $\overline{F}$ and will deflect an electron perpendicular to the velocity $\overline{v}$ and magnetic field

$$\overline{F} = q\overline{v} \times \overline{B} \tag{2.2}$$

If the velocity is constant than the electron with mass m would follow a circular motion described by

$$r = \frac{mv}{qB} \tag{2.3}$$

where the circular radius r increases the distance the electron travels which increases the likelihood of the electron colliding and ionizing a neutral atom. The electric field alternates causing electrons to strike the top and bottom electrodes during each half cycle. Both electrodes acquire a net negative bias due to the high mobility of electrons compared to ions. A region with a strong electric field begins to develop between the electrodes and the plasma referred to as the sheath. By symmetry electrodes with the same area would have the same potential difference so the electrodes are designed to maximise the potential difference between

the plasma and the bottom electrode. This is achieved with the top electrode typically being grounded and connected to the chamber wall creating a larger effective surface area. This asymmetry also enhances ion bombardment on the bottom electrode. [47, 48].

RF source power

The RF source power refers to the amount of RF energy delivered from a generator to the induction coil that sustains the plasma. Increasing the RF source power increases the energy delivered to the plasma resulting in higher levels of plasma excitation. This leads to an increase in the electron density as well as the average ion density [49, 50]. This increase in density causes the etch rate to also increase [51].

Platen power

The platen power controls the bias voltage between the substrate and the plasma [52]. Increasing platen power increases the ion bombardment energy which increases physical etch rate. Increasing the platen power generally increases the anisotropy of the etch but ions striking the masking material at an oblique angle can cause the edges of the mask to erode in a process called mask faceting. This erosion leads to a sloped etch profile [53].

2.5.5 Plasma etching

Masking materials

Analogous to the photomask used in photolithography, an etch mask is used selectively etch material using a plasma. A thin film is deposited and patterned to protect areas that are not being etched. This masking layer can either be a photoresist or a thin film of material such as Silicon dioxide or Silicon Nitride. The latter examples are commonly referred to as hard masks and are typically more resistant to plasma etching conditions compared to photoresists. A caveat

to these hard masks is they need to be selectively etched using a photoresist mask to define the pattern. Figure 2.3 shows the additional steps required in using a hard mask.

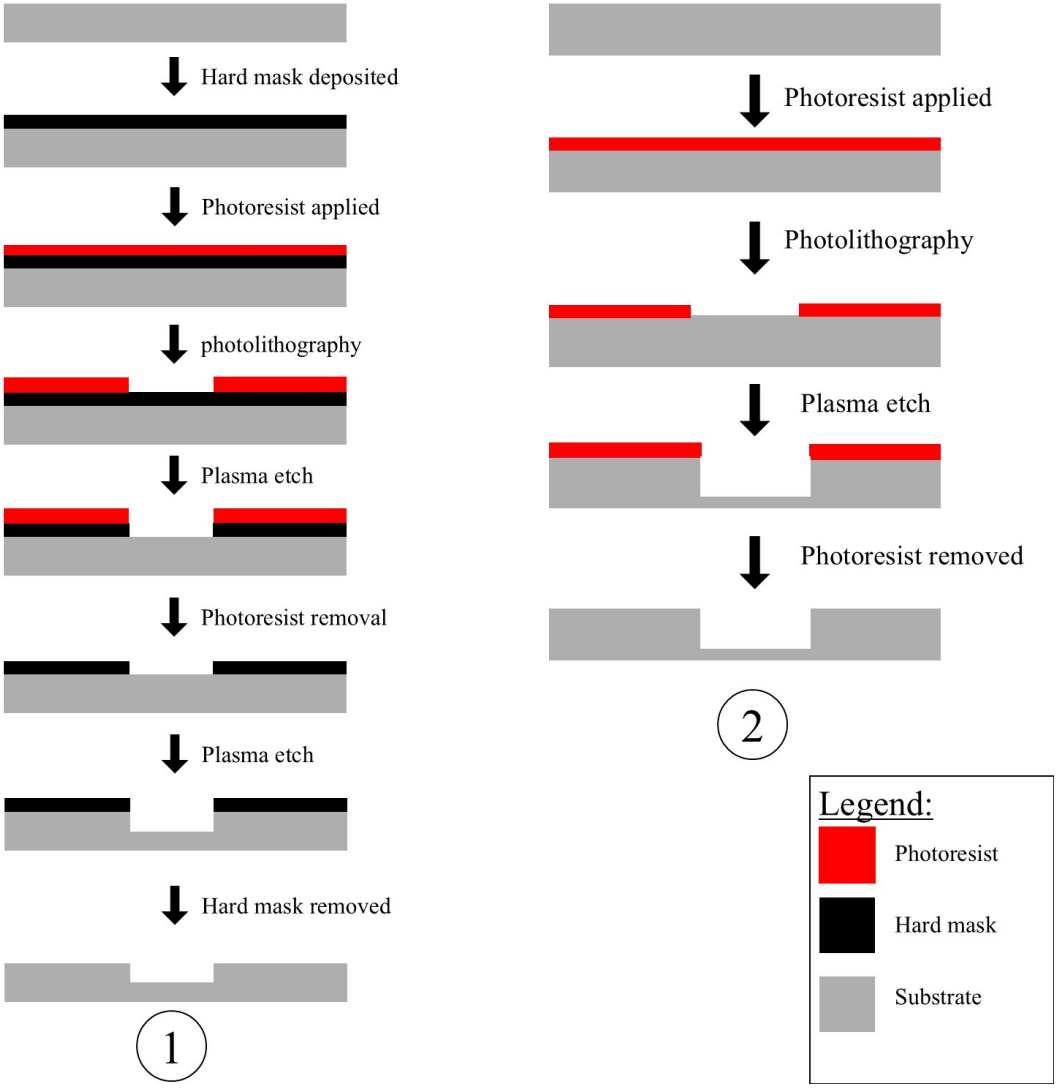


Figure 2.3: A standard process flow for a plasma etch using a hard mask (1) and photoresist (2).

Conditioning

Before any wafers can be processed the plasma chamber is first conditioned. The chamber is typically cleaned then exposed to a conditioning plasma either using the main processing chemistry or passivating chemistries such as O_2/N_2. This

process coats the chamber in a thin film close to that of the chemistry during the main etching step. Without a conditioning step or an improperly optimised conditioning step there can be a significant process drift in terms of etch rate drifts, selectivity changes and uniformity issues. As processing windows become tighter these issues become more pronounced if not properly conditioned. The most pronounced process shift is typically found within the first wafer processed in a batch referred to as the "first wafer effect". When a chamber is cleaned but not conditioned the chamber walls are exposed allowing for the sputtering and redeposition of Si and SiO_2 from the chamber walls. This affects the electron density near the chamber walls for the first wafer which as a result causes the uniformity of the etch, particularity at the edges, to be affected [54].

Chamber pressure

The chamber pressure refers to the pressure maintained in the plasma chamber typically measured in mTorr. At high pressures the probability of collisions increases which reduces the amount of ions striking the surface of the substrate perpendicularly [55].

plasma chemistry

An important parameter to consider is the plasma chemistry being used. The main species of gas is the etchant gas which enters the plasma chamber as a molecule and is broken down into radicals. If a high energy electron collides with the molecule, the molecule decomposes to form neutral radicals. These resultant radicals experience little to no attraction towards the anode or cathode due to having an overall neutral charge. Eventually these radicals impinge on the surface of the material being etched creating a volatile product that can be desorbed from the surface. Once the volatile reaction product is desorbed, it is removed from the chamber using a vacuum pump. The resulting profile is typically that of an isotropically etched material due to the chemical nature of the etch and the little to no directionality. An isotropic etch is depicted in figure 2.4 and is characterised

by rounded edges and a concave shape due to uniform etching in all directions.

Figure 2.4: An isotropic etch profile

Figure 2.5: An anisotropic etch profile

Some reaction products can only be desorbed from the surface when heated above room temperature. However, the choice of masking material decreases with increases in temperature with many photoresist formulations being unsuitable for temperature above 100°C due to degradation and re-flow affecting mask quality. Another consideration is that the reaction to form the volatile reaction product has to be exothermic in order to etch the material [56, 57]. A second species of gas can be added which after ionization from a collision with a high energy electron forms a positively charged ion. These ions are then attracted towards the cathode impinging on the surface assisting in the desorption of volatile etch by-products [58]. Ions with sufficiently high energy strike the surface of the substrate physically removing material via momentum transfer, a process referred to as ion bombardment. This means the masking material and substrate are etched at a similar rate. The etch profile of a substrate dominated by this process is typically anisotropic due to the ions following the electric field towards the cathode. The anisotropy can be affected by sidewall passivation from redeposited mask material on the sidewalls [59]. An additional gas can be added to deposit a thin layer of material such as a polymer to "passivate" the sidewalls. This passivation makes the sidewalls more resistant to chemical etching which can improve the anisotropy of the etch [60].

Cleaning

A chamber cleaning step becomes imperative as deposition builds up on the chamber walls affecting the reproducibility and eventually leading to a phenomenon called "process drift". As the deposit on the chamber walls get thicker there is also an increased risk of particle contamination from small pieces of the polymer being dislodged. Historically these build-ups were removed using wet etching which massively affected throughput necessitating a faster in situ dry etching method to remove the build up [61]. It was discovered that an O2 rich SF6/O2 plasma used after each wafer is etched is sufficient to keep the chamber clean with this being commonly referred to as a inter-wafer clean (IWC) [62].

2.5.6 Plasma etching metrics

Etch rate

The etch rate for a given process is the rate at which a specified material is etched. The following equation is used to determine the etch rate

$$\text{Etch rate} = \frac{\Delta\text{Thickness}}{\Delta\text{Etch time}} \tag{2.4}$$

Where the thickness is typically given in microns and etch time in minutes giving the etch rate in terms of microns per minute.

Selectivity

Selectivity is the ratio of etched material between two different materials. For plasma etching this is usually the ratio between the masking material and the substrate being etched. For example a selectivity of 15:1 substrate to mask would mean for every 15 µm of the substrate material etched 1 µm of mask would be etched. In general the higher the selectivity between mask and substrate the better as less masking material is required for deeper etches.

Profile

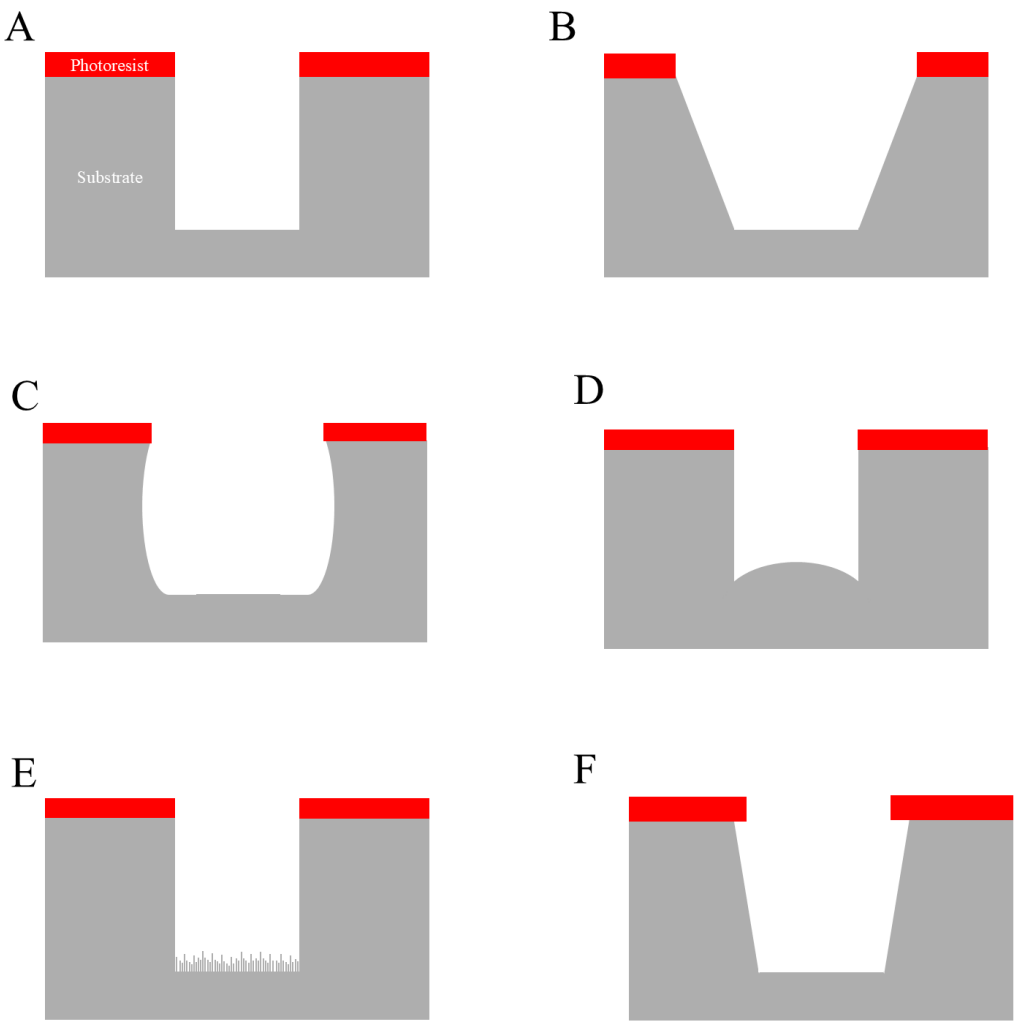


Figure 2.6: A)A vertical etch profile B)A tapered etch profile C)Bowing D)Microtrenching E)Micrograss F)Undercutting.

Figure 2.6 depicts various etch profiles with figure 2.6A being the ideal etch profile for plasma dicing.

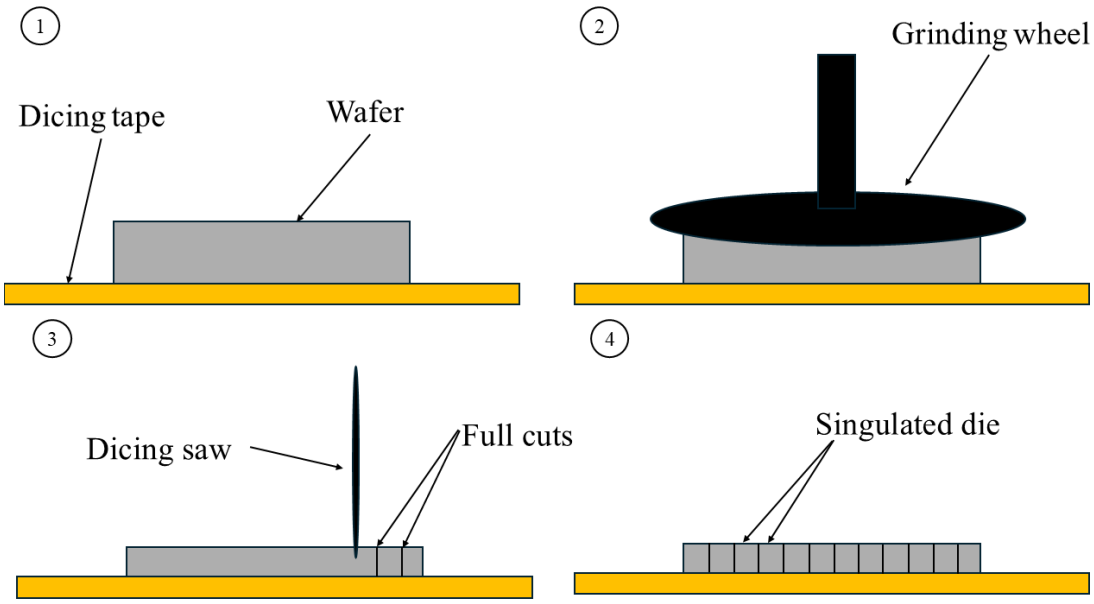
2.5.7 Challenges of etching III-V compound semiconductors

The main challenge of etching InP is in establishing a balance between the quality of the resultant etch profile and a fast etch rate >1 µm/min. The most widely used chemistries to etch InP are Cl_2, HBr_2, BCl_3 and CH_4 based. Historically, CH_4 was the most commonly used enchant for InP due to the quality of the pattern transfer as well as the smoother surface roughness. The downsides to CH_4 based plasma chemistries is the slow etch rate (<100 nm/min), passivation of dopants near the surface and polymer build up. Additionally, carbon build up on the chamber walls requires frequent cleaning using an O_2 plasma. Cl_2 based chemistries typically offer higher etch rates (>1 µm/min) with no polymer deposition. However, an elevated temperature of >180°C is required to to desorb the relatively unreactive etch product $InCl_x$ [63]. This limits the amount of masking materials available with most photoresists degrading at such high temperatures [64].

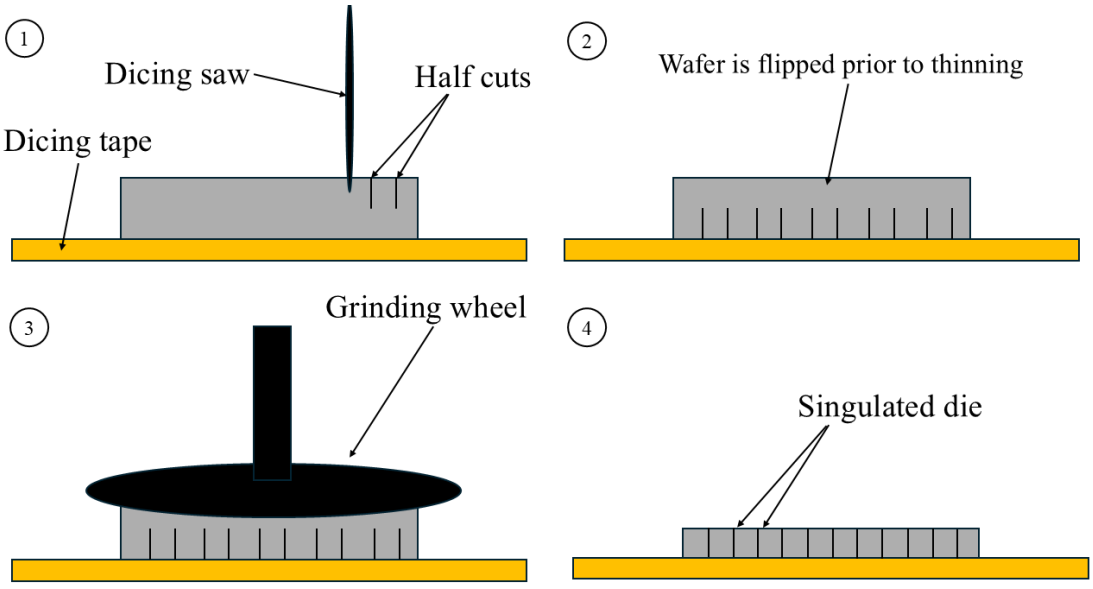
2.6 Backend processing and Dicing

2.6.1 Die singulation processes

Traditionally to singulate die, wafers are first thinned using a grinding wheel to reduce the thickness shown in Figure2.7a. Wafers are attached active side down on tape to protect the die during grinding. Once the wafer is sufficiently thinned, then die are singulated by cutting or etching material in streets/dicing lanes using a saw, laser or plasma [65]. With a growing demand for high strength thin die, a new method of die singulation was developed referred to as dice before grind (DBG) depicted in Figure2.7b. In a DBG process the wafer is first partially diced through half cuts. Then the wafer is thinned with the die being singulated once the wafer is thinned to the half-cut. Further thinning is used to thin the die to a set thickness [66].



(a) The conventional die singulation process flow



(b) A dice before grind die singulation process flow

Figure 2.7: Diagrams of two die singulational methods: a.)Conventional b.)Dice before grind

2.6.2 Blade Dicing

The first widely used dicing method in production was diamond scribing and breaking along the scribed line. This method utilized the crystal structure to create a straight cleave along the crystal plane. Laser surface scribing soon followed to avoid the frequent and expensive replacement of the diamond tip. Both laser and diamond scribing suffered from problems such as die breakage, die not separating properly, and high surface contamination from scribing. These problems were alleviated with the advent of full cut diamond-edge saw dicing in the early 1970s [67]. Since saw dicing's inception and later development into full in-line automation by 1983, saw dicing has dominated as the most prominent die singlulation method [68]. This market dominance is primarily due to the cost effectiveness of saw dicing. However, as a mechanical process there is a high amount of stress imposed on the die which can lead to cracks during the saw dicing process or micro cracks which can propagate into more serious defects leading to device failure after dicing [69].These defects can be caused directly by the blade interacting with the surface or by subsequent cleaning processes. The placement accuracy and alignment of the saw is crucial to avoiding damage to the active area of an IC. Additionally, changes in the kerf width can cause defects in a die. The kerf width is mainly dependent on the width of the saw blade but can become wider due to misalignment and from vibrations. Material can also build up on the saw blade causing protrusions that also widen the kerf width [70]. A typical mechanical dicing system consists of a diamond studded disk saw that can spin up to speeds of 60,000rpm. The depth of the cut is controlled via software allowing for partial or full cut depth. A cooling system is often used to continuously dispense a cooling lubricating solution that helps reduce the heat generated from friction as well as remove debris from the wafer [71]. Before the blade can be used for cutting the blade must first be dressed in order to achieve the most optimal cut

2.6.3 Laser dicing

There has been a general trend in the semiconductor industry towards thinner wafers and die [72]. This trend has been driven by the growing demand for RFID cards, nfc cards and 3D packaging as well as potential applications for flexible and wearable electronics [73,74]. Another reason for the shift towards thinner die is the inherent thermal and electrical benefits. Ultrathin die (<100 µm) have a reduced junction temperature and can dissipate heat more readily to the case as there is less material obstructing. These thermal properties improve the output power as well as the efficiency of the device [75]. However, ultrathin dies are prone to defects such as micro cracks and chipping with mechanical processes like saw dicing only exacerbating these issues [76]. These issues created a niche that laser dicing sought to occupy. Laser dicing utilises the mechanism of laser ablation to remove material from a patterned wafer to singulate die [77]. The first working laser was created in 1960 by Theodore Maiman named "the ruby laser". Soon after it was discovered pulsed lasers can cut through metal with a unit of laser power know as "gillettes" being devised by bell labs scientists to refer to the amount of razor blades a laser could cut through [78]. The cultural zeitgeist of the period generally favoured scientific advancement which in combination with growing interest from the military lead to unprecedented levels of funding for laser development [79]. These external factors helped fuel the rapid growth of laser technology leading to the discovery of both the CO2 and YAG lasers in 1964 by bell labs [80,81]. In May 1967, an experiment was conducted by Peter Houldcraft using a oxygen gas assisted CO2 laser to cut a 1mm steel sheet [82]. This marks an important milestone in laser material processing. proving the lasers usefulness in industry to cut materials. These lasers soon started to be used commercially to machine metallic parts with companies such as Boeing being early adopters of the technology helping to drive demand and further research into lasers [83]. After decades of refinement, lasers became powerful and precise enough to be used to singulate die with the first patent for laser dicing being filed in 2002 and

approved in the United States in 2004 [84]. Demand for laser dicing increased with the demand for ultra-thin wafers as well as for dicing brittle materials. In a saw dicing system the cutting speed would have to be slowed down to cut ultra-thin wafers to decrease the risk of defects. Whereas in a laser dicing system, due to the non mechanical nature of the cutting mechanism, the same cutting speed can be maintained [85]. The laser dicing process also allows for control over die shapes with rounded corners offering higher mechanical stability in singulated die [86]. However, laser dicing is comparatively more expensive than saw dicing for both the initial cost of the tool and maintenance. These costs reduce laser dicing to only being economically viable for dicing ultra-thin wafers when compared with saw dicing [87].

2.6.4 Plasma dicing

Plasma dicing is the most recent dicing technology utilizing a plasma generated from a plasma etching system such as an ICP RIE (Inductively coupled plasma reactive ion etcher) to etch dicing lanes on a processed wafer. Plasma dicing has many unique benefits such as increased yield, throughput and strength of the singulated die. As a primarily chemical etching mechanism there is a lower risk of defects being introduced compared to conventional mechanical dicing methods. With less micro cracks introduced that can potentially propagate into serious defects, plasma dicing can produce consistently higher yields of functional die. Another benefit to the lower number of defects is that dies can be designed with a smaller or no "seal rings" which are regions designed to protect the active region of a die from cracks. The reduction or possible elimination of these seal rings would allow designers to fit more structures onto the same size die. The other dicing methods are more constrained in terms of dicing lane width by the width of the saw blade or laser. Whereas, plasma dicing can consistently dice at lane widths that would be much harder to replicate with conventional dicing equipment. Depending on the wafer and die dimensions, this can further increase yield by allowing more die per wafer. Unlike saw dicing, there is no requirement for

dicing lanes to be perpendicular straight lanes. This freedom could allow unique positioning of die to maximize the usable area of a wafer. While the etch rate may be quite low at any given point (<1 µm per minute), plasma dicing etches the dicing lanes simultaneously rather than saw and laser dicing that dice lanes sequentially. This unique property is particularly advantageous for smaller die sizes as there are more dicing lanes that would decrease the throughput of saw and laser dicing. For plasma dicing there would only be a small reduction in etch rate due to more material being etched and thus more etchants being used, a phenomenon commonly referred to as the "loading effect" [88, 89]. Another increase in throughput when compared to saw and laser dicing is seen in ultra-thin wafers. While saw and laser systems would have to adjust their saw speed and laser output power, plasma dicing can maintain the same etch rate without sacrificing die strength. The biggest drawback and largest factor affecting widespread adoption of plasma dicing is the high initial cost of the ICP RIE [90]. However, this high initial cost is offset by the improved throughput and die strength meaning a higher yield of usable die and less money wasted on defective die [91].

2.6.5 Die per wafer

An important metric in the manufacturing of integrated circuits is the maximum number of die per wafer known as the gross die per wafer (GDW). Maximising GDW is an important consideration as optimising for a high GDW means a potentially higher yield (ignoring losses due to defects). Many equations exist to estimate the GDW the simplest of which being:

$$GDW = \frac{r^2\pi}{l \times w} \tag{2.5}$$

where r is the radius of the wafer, l is the length and w is the width of the die. This simple approximation does not take into account: the effective area of the wafer, incomplete die on the wafer edge, the wafer flat and the placement of the die. Adding a correction term that precludes die at the edge of the wafer gives:

$$GDW = \frac{r^2\pi}{l \times w} - \frac{2r\pi}{\sqrt{l^2 + w^2}} \tag{2.6}$$

where the correction term is the ratio of the wafer circumference to the diagonal length of the die [92].

2.7 Metrology

2.7.1 Optical microscopy

An optical microscope is an instrument that focuses visible light through a series of lenses to generate a magnified image [93]. An illumination element such as an LED illuminates the subject while the objective lens collects the emitted and transmitted light of the subject producing three parallel beams of light. A tube lens then focuses the beams forming a real intermediate image. The light is then either collected on a camera sensor or further magnified through an eyepiece for visual observation [94].

2.7.2 Scanning electron microscopy

A Scanning electron microscope (SEM) is a type of microscope that uses a focused electron beam instead of light. The advantage of using electrons is the nanometre-scale resolution. An electron gun generates the beam of electrons which are accelerated to energies typically in the range of 0.5 keV to 30 keV. The beam is focused using a series of electromagnetic lenses analogous to those found in a optical microscope. Using these electromagnetic lenses the beam can be focused to a spot just a few nanometres wide. Deflection coils, located in front of objective lens electromagnet, are controlled by a scan generator that deflects the electron beam causing it to scan the sample line by line. The electrons strike and interact with the material giving off secondary and back scattered electrons depending on the energy. Other types of signals are given off which are discussed in greater detail below in section 2.8.2. Specialised detectors collect the signal from these interactions which is then converted into an image that is displayed on a graphical interface such as a computer monitor [95].

2.7.3 Energy Dispersive X-ray spectroscopy

Energy Dispersive X-ray (EDX) spectroscopy is a technique of elemental analysis that uses the characteristic X-ray emission to determine the presence of elements in a sample [96]. An electron beam with sufficient energy can ionize an atom creating a vacancy in the inner shell. An electron from an outer shell then fills the aforementioned vacancy releasing the binding energy either by emission of a characteristic x-ray or transferring to an Auger electron. These x-rays are then subsequently detected by a EDX detector. Incident x-rays on the detector generate an electron hole pair with the number of pairs being equal to the x-ray energy [97].

2.7.4 Ellipsometry

Ellipsometry is a measurement technique used to measure properties of thin films. The method is based on measuring the change in the polarization state of light reflecting off a surface. The standard ellipsometry configuration consists of a: light source, linear polarizer, compensator, sample and analyser. One arm consists of the light source, linear polarizer and compensator the other arm has the analyser. The first arm produces a light of known polarization state and the other detects changes in this polarized state [98].

2.7.5 Profilometry

A profilometer is a measurement tool that measures surface texture. A stylus is moved across the surface ,typically with a motor, it rises and falls with the surface irregularities. This stylus connected to an electrical pickup which converts and amplifies this movement into electrical signals which are then subsequently processed by a computer. From this the roughness average and average maximum height can be determined. The roughness average is the arithmetic mean of all the deviations from the mean line of the sample length. The average maximum height is an average of the five highest and lowest peaks in a sample length [99].

2.8 Defect analysis

2.8.1 Defects

A defect is any deviation from the perfect crystal structure. These defects can range from small defects at a specific location in a crystal known as a point defects to larger defects such as chipping. These defects affect properties of the semiconductor such as mechanical, electrical and optical limiting or degrading device performance [100]

2.8.2 Electron beam surface interactions

When an electron beam penetrates a material, a series of elastic and inelastic collisions occur. The transfer of energy from the incident electron beam to the material gives rise to the emission of electrons and photons, depending on the energy transferred and type of collision. Electrons emitted due to inelastic collisions are referred to as "secondary" electrons. They are defined as having an energy $<50\,\text{eV}$ though typically are in the range of $0.5\,\text{eV}$ to $5\,\text{eV}$. Electrons originating from deeper in the material occur due to elastic collisions, with these electrons being referred to as "backscattered" electrons. These electrons are defined as having an energy $>50\,\text{eV}$ but not higher than the primary electron beam typically of the order of keV. Distinct peaks in the energy spectrum of backscattered electrons arises from the Auger effect causing inner shell vacancies to be filled by outer shell electrons. The resultant emitted electrons are referred to as "Auger" electrons and have distinct energy peaks based on the material. Additionally the interaction between the electron beam and the material also leads to the emission of photons in the visible spectrum (cathodoluminescence, see below Section 2.8.3) as well as x-rays [101].

2.8.3 Cathodoluminescence

Cathodoluminescence (CL) refers to the emission of light due to excitation from an electron beam. Historically, the first reported cases of CL were in the mid nineteenth century in which evacuated glass tubes were found to emit light when excited via a "cathode" ray (electron beam). This phenomenon prompted the discovery of the electron. When an electron beam, typically in the regime of keV, is incident on a surface it is subject to a series of both elastic and inelastic scattering events. The depth these electrons penetrate is determined as a function of the electron beam energy E_b

$$R_e = \left(\frac{k}{\rho}\right) E_b^{\alpha} \tag{2.7}$$

where k and α are constants depending on the atomic number of the material being bombarded by the electron beam and ρ is the density of the material. Knowing this one can then calculate the electron-hole generation factor which is the number of electron-hole pairs generated per incident electron beam. The electron-hole generation factor is given by

$$G = E_b \frac{(1-\gamma)}{E_i} \tag{2.8}$$

where E_i is the ionisation energy required to form an electron-hole pair and γ is the fractional electron beam energy loss from backscattered and emitted electrons. For a photon to be emitted there must be a relaxation from the excited state (E_2) caused by the electron beam to lower energy state (E_1). The emitted photon has wavelength

$$\lambda = \frac{hc}{(E_2 - E_1)} \tag{2.9}$$

Where h is Planck's constant and c is the speed of light. The rate of CL emission can be given by the expression:

$$R_{CL} = \frac{f\eta G I_b}{e} \tag{2.10}$$

Where f is the correction function to takes into account that not all photons generated are from optical emission and internal reflection losses. This function

f is based on parameters of the specific CL system. I_b is the beam current and e is the elementary charge of an electron. η is the internal quantum efficiency or the radiative recombination efficiency. η is a material dependent on factors such as temperature and defect density [102].

2.8.4 Electron beam penetration depth

A popular model for estimating the penetration depth of an electron beam is the Kanaya–Okayama model. This semi-empirical model used experimental data to determine α and k from equation 2.7 giving the following equation

$$R_{KO} = \frac{0.0276 A E_b^{1.67}}{Z^{0.89}\rho} \tag{2.11}$$

Where R_{KO} is the penetration depth in µm, ρ is the density of the material in gcm^{-3}, A and Z are the atomic weight and atomic number of the material [103]. To determine the maximum electron penetration depth for InP the average atomic number and average molecular mass first needs to be calculated. The average molecular mass M is given by

$$M = \sum_i n_i A_i \tag{2.12}$$

where n_i is the number of atoms of element i and A_i is the atomic average of element i. For Indium phosphide using values from the international union of pure and applied chemistry (IUPAC) and using equation 2.12 gives a molecular weight of $147.79\,\mathrm{gmol}^{-1}$. The average atomic number $\bar{Z}$ is typically calculated using the following equation

$$\bar{Z} = \sum_i c_i Z_i \tag{2.13}$$

where c_i is the mass fraction of element i and Z_i is the atomic number of element i. For InP $\bar{Z}$ is equal to 32. Using these values in equation 2.11 gives Figure 2.8 for the electron beam penetration for InP.

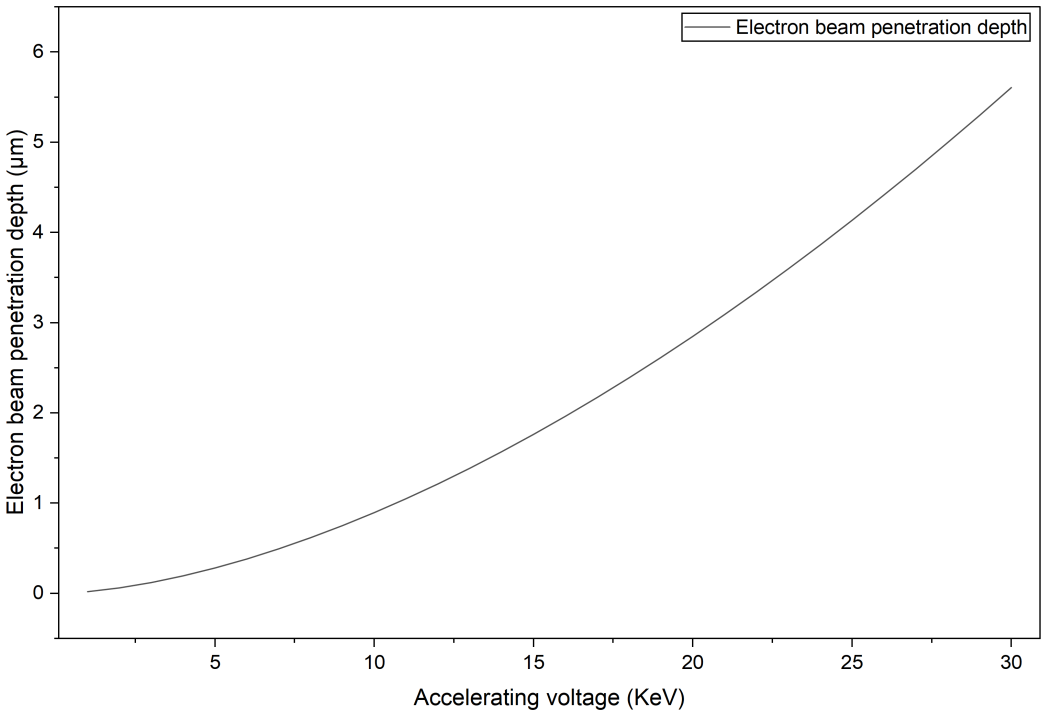


Figure 2.8: The electron beam penetration depth as a function of acceleration voltage for InP as calculated using the Kanaya–Okayama model

Chapter 3

Materials and methodology

3.1 Photolithography

Photolithography was first developed on three inch 325 µm thick silicon wafers due to the limited number of InP wafers. A solvent clean using the recipe A.1 was performed on all silicon wafers before use to remove particulate contamination.

3.1.1 Preparing the InP wafers

The InP wafers provided by KLA were previously used reclaimed wafers which were coated in a layer of oxide and unknown photoresist both of which had to be removed before applying photoresist. Due to the composition of the previous photoresist being unknown, the wafers were exposed to 50 sccm of a pure oxygen plasma in a plasma asher for 10 minutes to remove the photoresist layer. The photoresist strip was preformed first to avoid any possible adverse reaction with the subsequent hydrofluoric acid (HF) clean. Once the photoresist was removed a HF strip was preformed to remove the oxide layer. A 10% hydrogen fluoride solution and 2 beakers of water were used to rinse the acid. The wafer was then transported in a beaker of water to a spin coater to dry off.

Figure 3.1: An optical microscope photo of the surface of the cleaned InP wafer

Optical microscopy after the wafers had been dried, revealed a faint subsurface etch shown in Figure 3.1. However, profilometry measurements revealed that the depth of these subsurface etches are < 6 nm with the average surface roughness of the surrounding surface being 3.19 nm and are thus considered negligible .

3.1.2 Photomask design

The photomask used to pattern the photoresist was designed using the Klayout computer software [104]. 2mm by 2mm squares were designed to simulate die with alternating pairs of 25 µm and 50 µm lanes to test two different dicing kerf widths shown in Figure 3.2. The mask was designed right reading facing up meaning text in Figure 3.3 was on the same side that faces the wafer. This was to ensure the photomask was placed in the correct orientation when loading into the mask aligner.

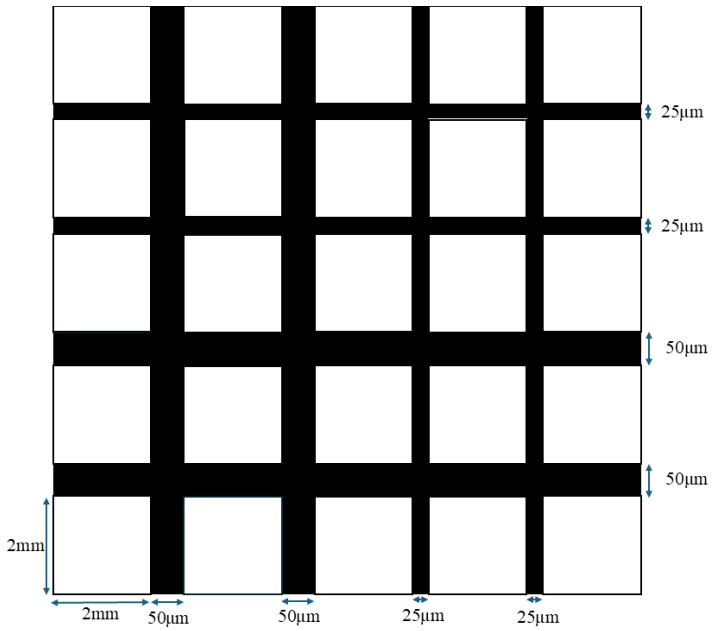


Figure 3.2: A diagram of a section of the photomask pattern.

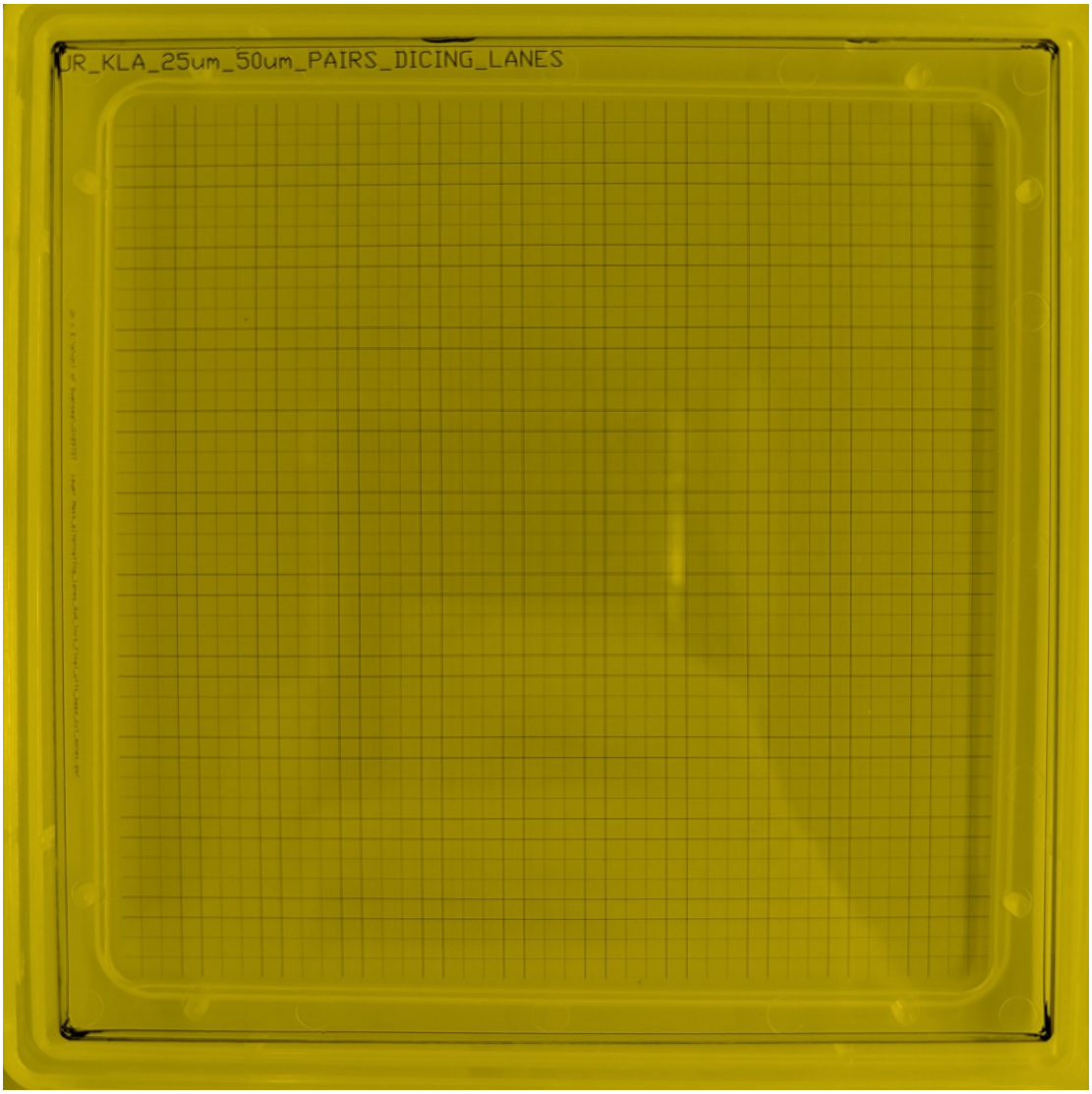


Figure 3.3: A photo of the photomask used throughout the project

3.1.3 SU8 on silicon

The specific formulation of SU-8 used was SU-8 3100 which will be referred to as SU-8. This formulation can achieve thicknesses between 20 µm and 8 µm. The 3000 series of SU-8 is an improvement on previous iterations providing better adhesion and reduced coating stress. The initial photolithography trial were completed using the SU-8 data sheet as a starting point see A.2.

Su-8 thickness

The target thickness for the SU-8 layer was selected to be >10 µm to ensure there was enough masking material to survive a deep >100 µm etch of InP assuming the selectivity would be approximately 10. To ensure a consistent 10 µm thick layer of SU-8 was being spin coated an experiment was carried out to determine the optimal spin speed. The softbake, hardbake and expose dose were kept constant with five different spin speed being increased from 2700rpm to 3100rpm in 100rpm/min steps.

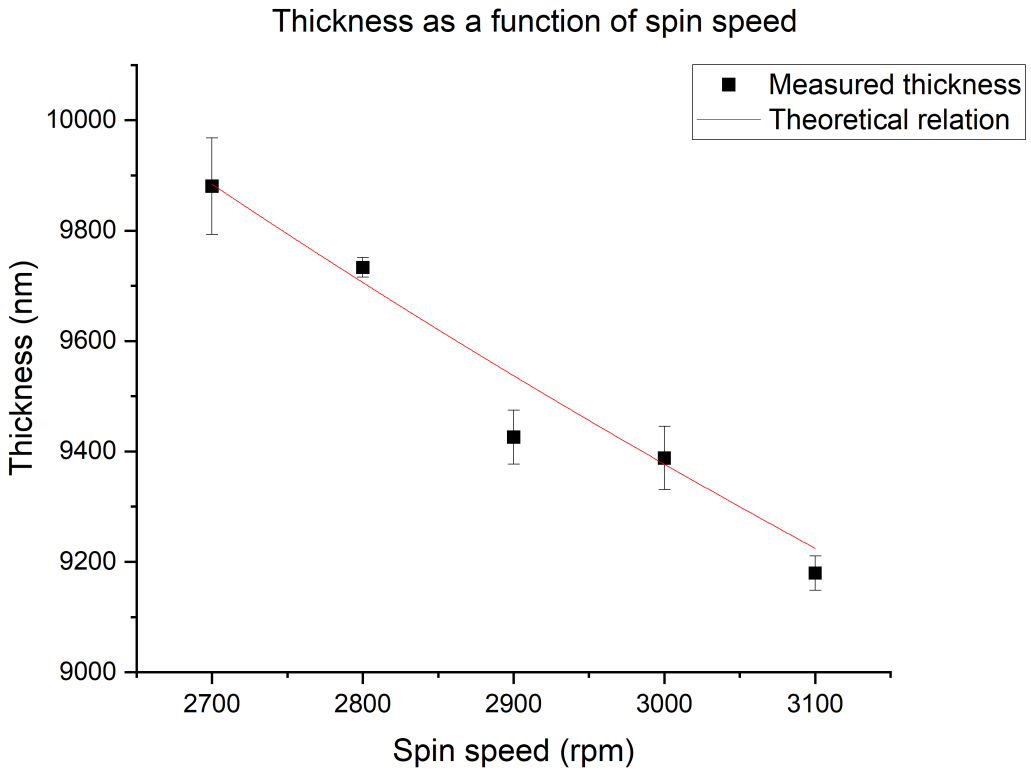


Figure 3.4: A graph of spin coater spin speed plotted against thickness.

Figure 3.4 shows the thickness as measured by ellipsometry as a function of spin speed. Rearranging 2.1 for spin speed gives

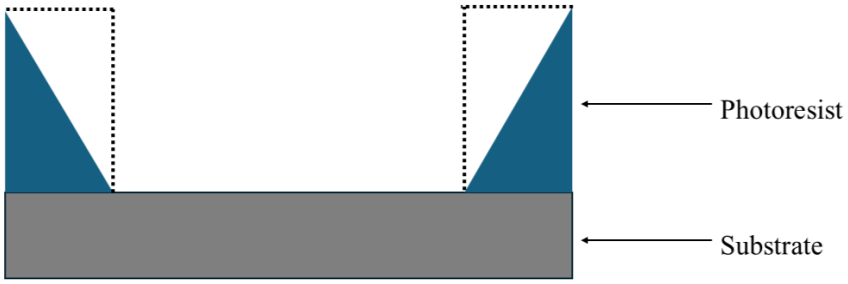
$$\omega = \left(\frac{a}{h}\right)^2 \tag{3.1}$$

Where a is a constant of proportionality determined experimentally and h is the

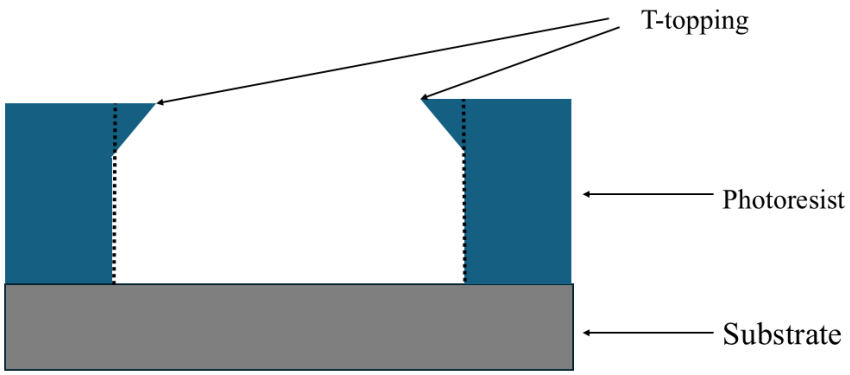
thickness. Using the value of the constant a from the fitted curve gives a spin speed of 2600rpm to achieve a 10 µm thickness.

Su-8 optimal exposure dose

Careful control of the exposure dose is required to pattern the desired 90° vertical sidewalls. If the SU-8 is overexposed then the top of the feature will protrude further than the bottom referred to as "t topping" shown in Figure3.5b. The inverse is true for underexposure where the base of the feature protrudes more than the top shown in Figure3.5a.



(a) An underexposed profile



(b) An overexposed profile

Figure 3.5: Diagrams of an over and underexposed profile

Aside from the aforementioned affect on the sidewall angle extreme under exposure can cause the SU8 layer to "lift off" from the substrate [105]. two exposure

series tests were conducted one from 230 mJcm^{-2} to 260 mJcm^{-2} in 10 mJcm^{-2} steps. The other exposure dose series was from 280 mJcm^{-2} to 340 mJcm^{-2} in 20 mJcm^{-2} steps. The softbake, hardbake and spin coating parameters were kept constant in both series.

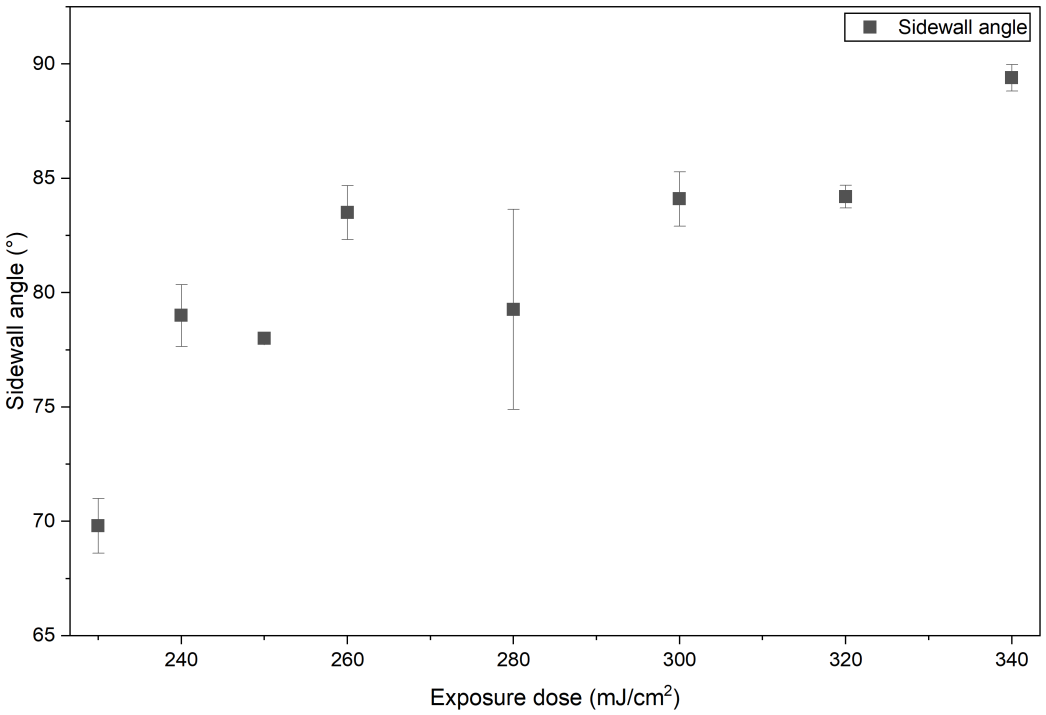


Figure 3.6: The sidewall angle as determined by trigonometry using SEM measurements plotted as a function of exposure dose.

Figure 3.6 shows that increasing exposure dose improves the sidewall angle up to 340 mJcm^{-2} which is the optimal exposure dose. Beyond this the photoresist would start becoming overexposed causing t topping. Sidewall angles were calculated using a combination of measurements from SEM images and trigonometry.

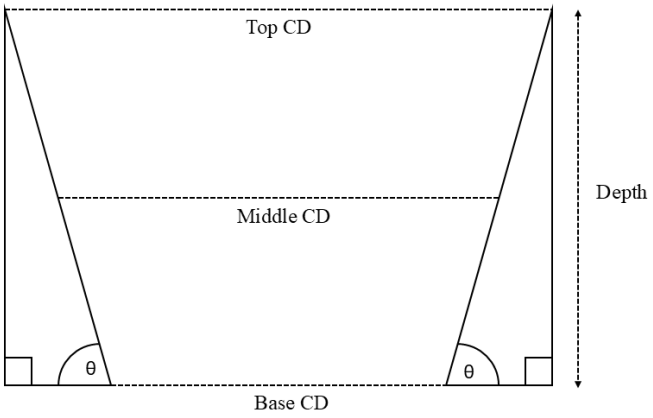


Figure 3.7: A digram showing the measurements used to calculate the sidewall angle θ.

In this work, the sidewall angle was calculated via:

$$\theta = \arctan\left(\frac{\frac{\text{Top CD}-\text{Base CD}}{2}}{d}\right) \tag{3.2}$$

Where d is the depth of the trench.

3.1.4 125NXT 10B on SiO_2 and Si

The next masking material being investigated for its suitability for plasma dicing was a 5 µm SiO_2 hard mask. The 5 µm SiO_2 layer was deposited on both silicon and InP using CVD, discussed in Section 2.5.3. To pattern this hard mask, a combination of photolithography and dry etching was required as shown in process flow 1 in figure 2.3. Initial photolithography runs were performed on silicon wafer coated in SiO_2 to establish a process flow before transferring to the InP wafers with a 5 µm SiO_2 layer. The photoresist 125NXT 10b was selected for the photolithography due to its negative tone meaning it can be used with the existing bright-field photomask used for patterning the SU8 mask. Additionally, 125NXT 10b is easier to strip than SU8 especially after prolonged plasma treatment being

readily dissolved in standard photoresist stripping solutions. Since the 125NXT was to be used as an etching mask for the SiO_2 layer the thickness of the 125NXT didn't need to be optimised unlike the SU8.

Optimal Exposure Dose

The first photolithography run using 125NXT on Si was done following the data sheetA.4. An exposure dose series from 1300 $mJcm^{-2}$ to 1800 $mJcm^{-2}$ in 100 $mJcm^{-2}$ steps to determine the optimal exposure dose.

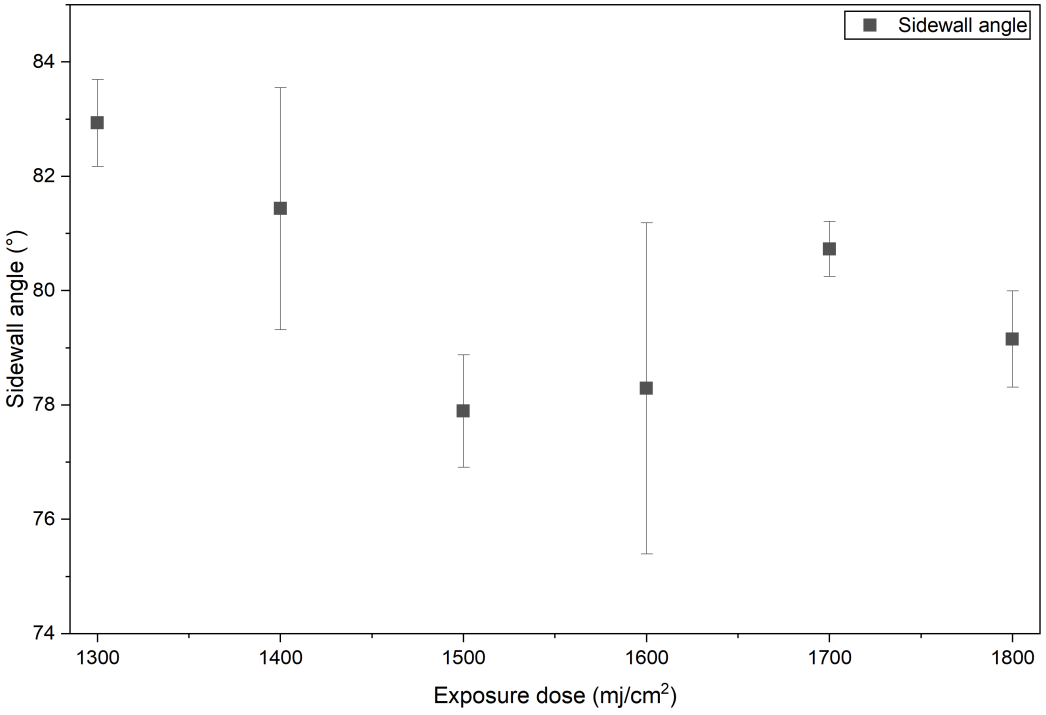


Figure 3.8: The sidewall angle for each exposure dose for 125NXT.

Figure 3.8 shows the most vertical sidewall angle was achieved at the exposure dose 1300 $mJcm^{-2}$. The large uncertainties is due to to a high numerical uncertainty between 25 µm and 50 µm trenches most likely due to the 125NXT photoresist being expired. As the photoresist was expired and a 83° sidewall angle was achieved this was deemed sufficient enough to etch the SiO_2 hard mask.

3.1.5 Transferring Process flows to InP

Once a suitable profile was achieved for both SU-8 and 125NXT on a 76 mm 325 µm Silicon wafer and a SiO_2 coated si wafer then the process flow could be transferred to InP. The processes were repeated on the 600 µm thick 76 mm InP wafer and SiO_2 coated InP wafer.

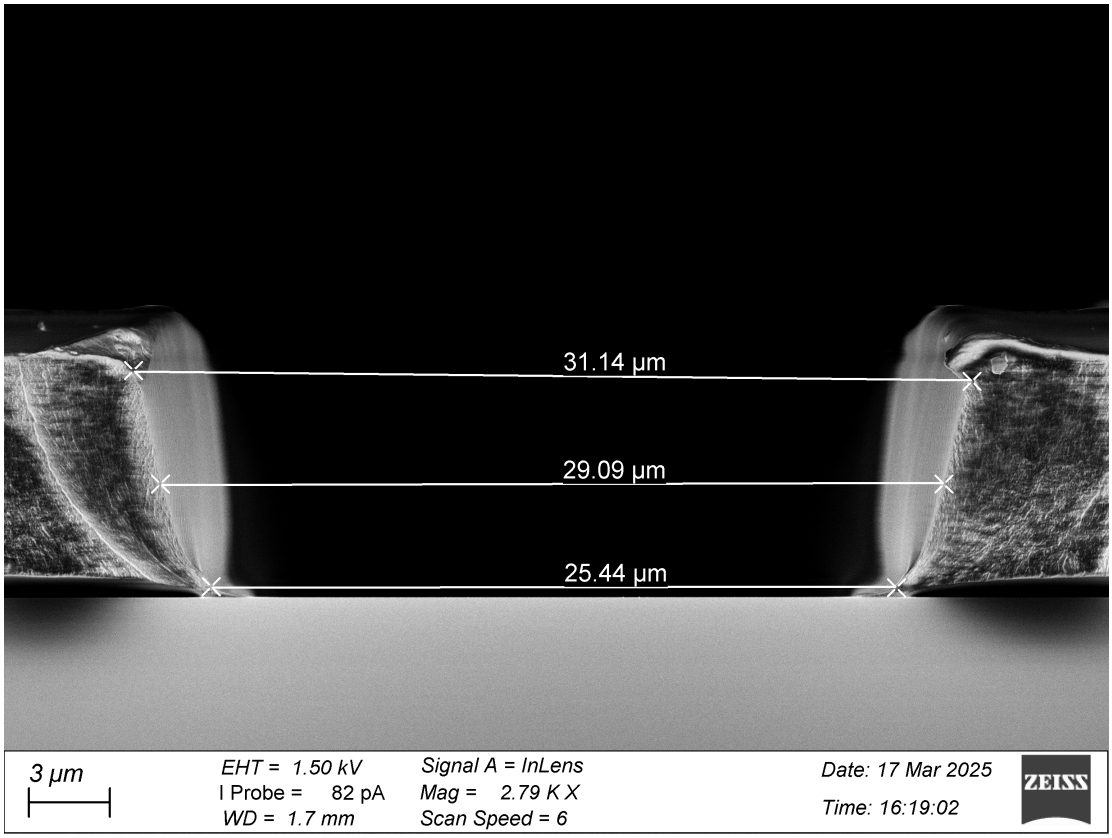


Figure 3.9: A cross section of a 25 µm trench on InP using the Si recipe for SU-8. Sidewall angle calculated to be 79.7°.

As shown in Figure 3.9 the SU-8 sidewall angle decreased by approximately 10° when transferring to the InP substrate. This was most likely caused by the difference in thermal properties from Si to InP namely the specific heat capacity and thermal conductivity. This, combined with the InP wafers being 275 µm thicker, means there is a discrepancy in the temperature of the SU-8 layer acheived during the soft and hard bake steps. Keeping the exposure dose and the spin coating parameters the same the soft bake and hard bake temperatures were investigated

for their effect on the profile. The soft bake and PEB times were increased by 25% and 50% to compensate for the difference in thermal properties with the effect on sidewall angle shown in Figure 3.10.

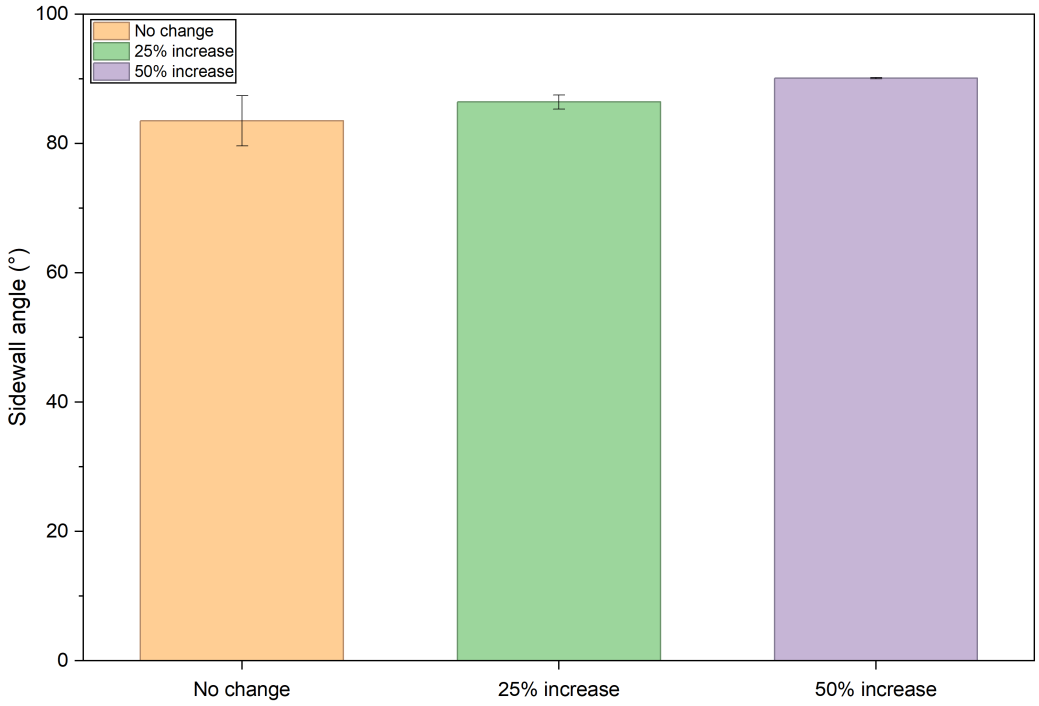


Figure 3.10: The calculated sidewall angle of SU-8 on InP for increasing soft and post exposure bake time.

Figure 3.10 shows the sidewall angle improved back to the original 90° value for the SU-8 recipe on si. Using this information the 125NXT soft bake and hardbake times were increased by 50%

3.1.6 Polyimide

Polyimide masked InP wafers were provided by the KLA corporation as another photoresist masking material to use when plasma etching to compare with SU-8. The widths of the dicing lanes for this mask was slightly different with 20 µm, 30 µm, 40 µm.

Chapter 4

Plasma etching

4.0.1 Etching the SiO_2 hard mask

Once a suitable photoresist profile was achieved the SiO_2 mask was then etched using an ICP (SPTS ICP). To determine the etch rate the initial thickness of the SiO_2 layer on the Si test wafers were verified to be 5.1 µm using ellipsometry. A C4F8:CF4:Ar plasma chemistry was used to etch the SiO_2 layer with the final thickness after a 1 minute etch being measured to be 4850 nm. Using Equation 2.4 gives an etch rate of 253 ± 6 nm/min for the oxide layer. So for a 5 µm thick oxide layer this corresponds to an etch time of 20 minutes. Running this recipe on a 125NXT patterned Si wafer gave the profile shown in Figure 4.1.

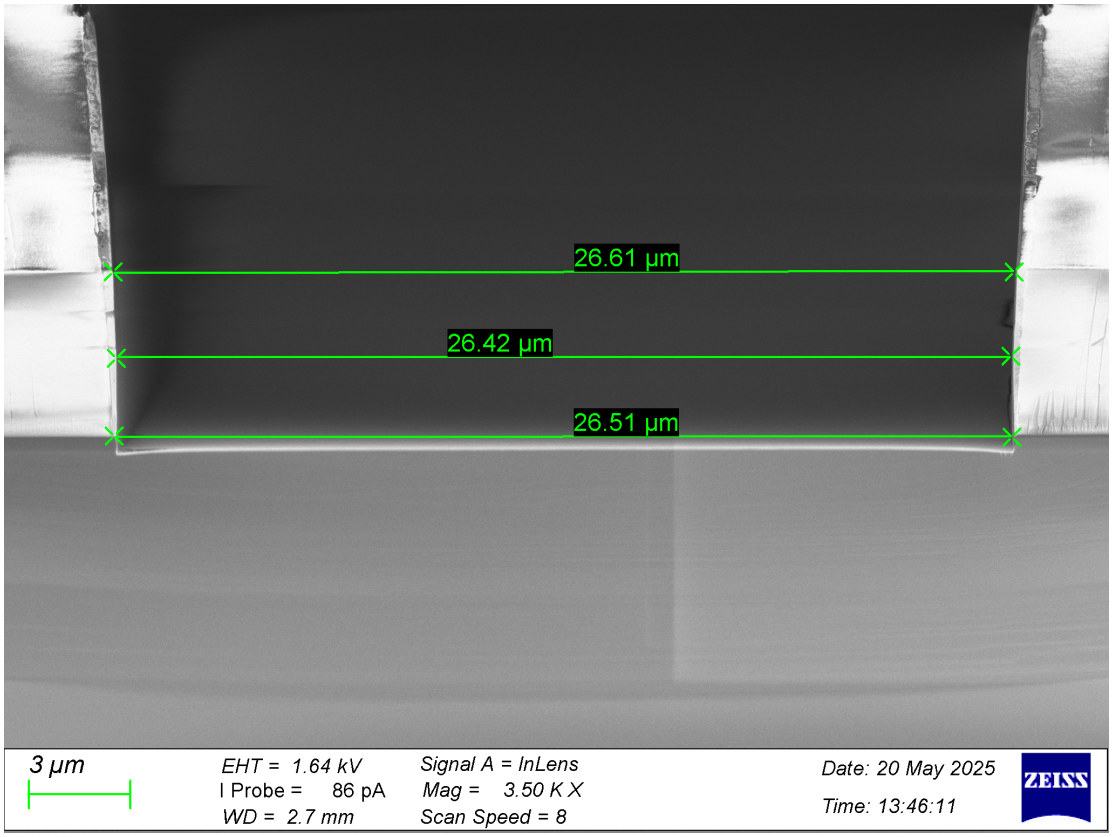


Figure 4.1: An SEM image of the etched SiO_2 mask on Si using a 125NXT 10B photoresist mask.

Since the etch profile in Figure 4.1 was anisotropic and vertical the same recipe was transferred to the SiO_2 coated InP wafers.

4.0.2 Plasma etching InP

The deep etching of InP took place at KLA corporation's Ringland way site utilising their Omega ICP etching module and *fxp* wafer handling platform. Small test pieces, sometimes referred to as coupons, were cleaved into approximately 15 mm by 15 mm coupons and mounted using high temperature crystal bond onto a 75 mm silicon carrier wafer with a 5 µm SiO_2 layer. These wafers were then subsequently loaded into a 20 wafer cassette that loads the wafers via a loading arm into the plasma etching module. Wafers were clamped using a electrostatic chuck (ESC) which clamps the wafer via a electrostatic charge preventing the wafer from

moving or flipping when the continuous backflow of helium is introduced. The target depth for the etch was >100 µm to test if InP is suitable for a plasma dicing process. An etch to this depth would allow for a subsequent backside grind to singulate the die after the etch following a DBG approach as shown in Figure2.7b.

4.1 Cl:Ar chemistry

4.1.1 SU-8 mask

Starting recipe

An existing recipe was tested on the InP coated in SU8 to see how the SU8 would react when subject to 180°C. The process used was as follows:

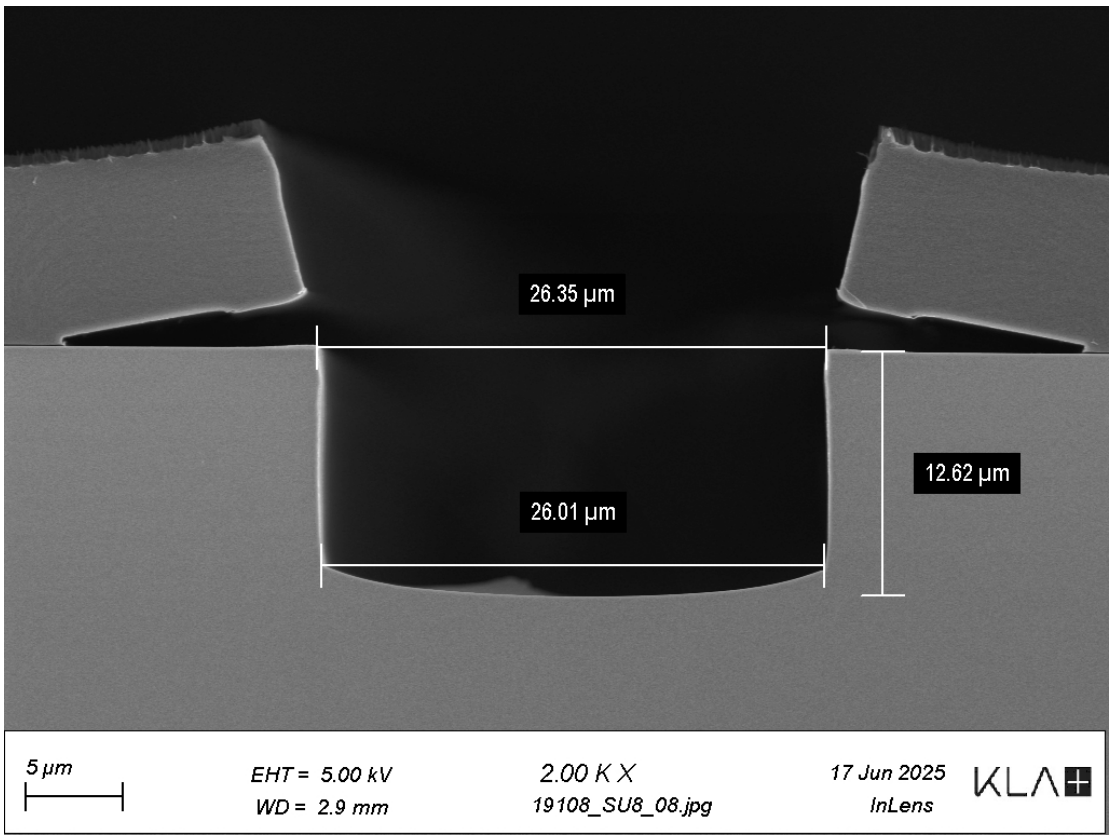
- [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
    - [redacted]
- Etch:
  - Time: [redacted]
  - Primary source power: [redacted]
  - Platen power: [redacted]
  - Chamber pressure: [redacted]
  - Helium backflow pressure: [redacted]

  - Plasma chemistry
    - Argon: [redacted]
    - Hydrogen: [redacted]
    - Chlorine: [redacted]

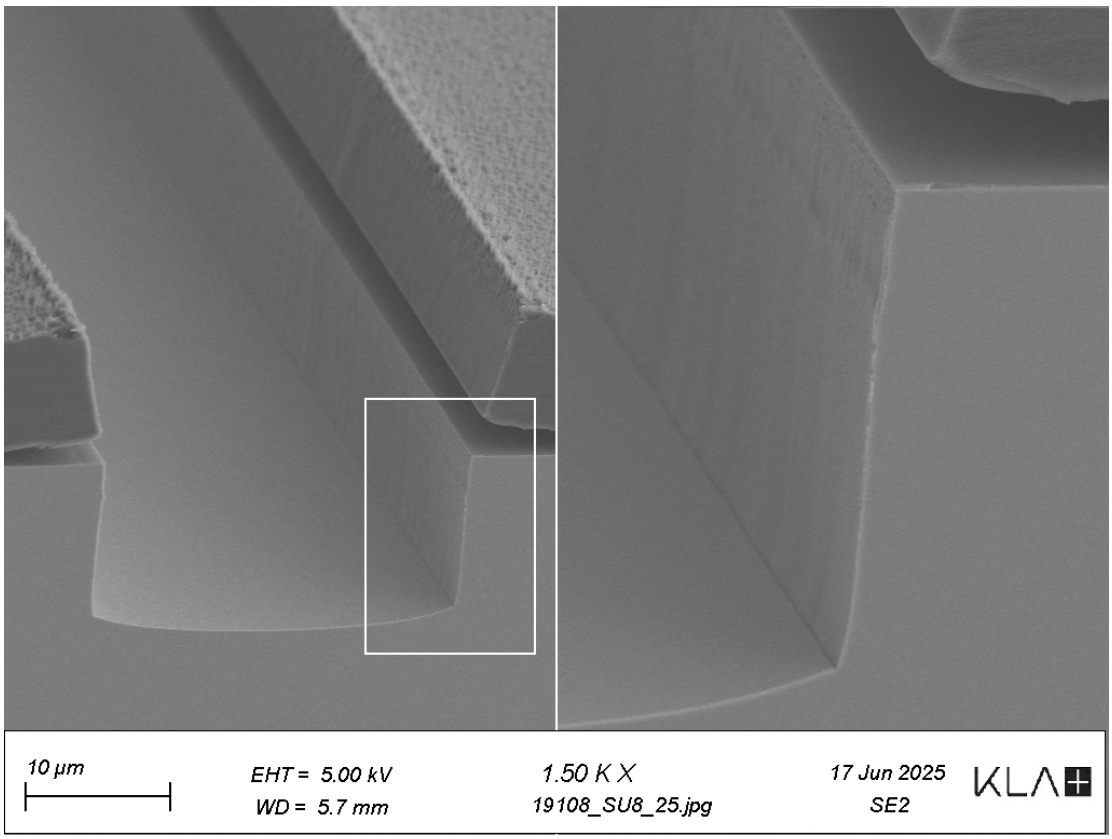
- Oxygen clean:
  - Time: [redacted]
  - Primary source power: [redacted]
  - Platen power: [redacted]
  - Chamber pressure: [redacted]
  - Helium backflow pressure: [redacted]
  - Plasma chemistry
    - Argon: [redacted]
    - Oxygen: [redacted]

The [redacted] warm up step was to allow the substrate to get up to temperature as well as stabilise the plasma before introducing the reactive species in the etch step. Running this step before the main etch step ensured the chamber conditions were similar before the etch step improving reproducibility. The chlorine in the etch step introduces a chemical aspect to the etch through introducing reactive species that react with the InP forming $InCl_x$ and PCl_x. The former being more less reactive than the latter which is why the process requires a [redacted] processing temperature in order for the etch by-products to be desorbed from the surface. The inclusion of hydrogen is multifaceted, in literature the addition of hydrogen is widely reported to provide a small passivation layer as well as also creating an additional reaction pathway for the phosphorous forming the volatile etch by-product PH_x. This passivation helps provide a smooth anisotropic sidewall profile as well as preventing undercutting while the additional reaction pathway for the phosphorous offsets what would otherwise be a decrease in the etch rate [106].

The argon provides a physical component to the etch via ion bombardment. The energy transfer from the Ar ions also assist in decreasing the energy required for the volatile etch products to desorb from the surface. Running this recipe on the InP piece gave the following profile shown in Figure 4.2.



(a) A 25 µm trench post plasma etch using a SU8 mask



(b) SEM of the sidewall quality post plasma etch using a SU8 mask

Figure 4.2: SEM images of the resulting profile

Partial mask lift off as shown in Figure 4.2a and 4.2b was only observed in the initial test run and was only found along some trenches. This was most likely caused by poor adhesion of the SU8 to the InP due to poor surface quality after repeated uses of this piece for photolithography refinement of SU8 on InP. Aside from the mask liftoff, the etch profile is anisotropic in agreement with literature. The average etch rate was 2.7 µm/min meaning for a 100 µm deep etch this would correspond to an approximate processing time of 37 minutes, assuming the etch rate remains constant. However, the average selectivity of InP to SU8 being 5.9 means a 10 µm SU8 mask would be insufficient for etching to a depth of 59 µm which is short of >100 µm goal.

Effect of primary source power

Following on from the initial recipe, the etch time was increased to 600 s and kept constant. The primary source power was changed to study its effect on the etch rate and selectivity. To investigate the effect of the primary source power on etch rate as well as the selectivity of the SU-8 three different primary source powers were tested while keeping the platen power constant.

Figure 4.3: A graph of etch rate and selectivity of SU8 to InP as a function of primary source power.

Figure 4.3 the etch rate of the InP increases with increasing primary source power suggesting the mechanism of etching is primarily chemical in nature. Increasing the source power would also increase the plasma density meaning a higher Cl radical concentration. [redacted]. Etching for a longer time (300 s

compared to 600 s) than in the initial recipe also decreased the selectivity from 5.9 to 4.2 for the same processing parameters. This decrease in selectivity is most likely caused by a reduction in the etch rate of InP with more etchants being consumed. This means that to increase the selectivity either the etch rate of InP has to be increased to compensate or a more passivating gas needs to be added to protect the mask.

Effect of platen power

The effect of the platen power was investigated at source powers [redacted] and [redacted] which were the highest and lowest source powers used.

(a) A comparison of etch rate and selectivity for increasing platen power at [redacted] source power

(b) A comparison of etch rate and selectivity for increasing platen power at [redacted] source power

Figure 4.4: Plots of etch rate and selectivity for increasing platen power

Figure 4.4a and 4.4b shows etch rates improved with increasing platen power for both low and high source power respectively. This is most likely due to more energetic ion bombardment.

Gas ratios and using BCl_3

To increase the etch rate of the InP to boost the selectivity the effect of gas flow rates was investigated as well as using Boron trichloride (BCl). The other processing parameters were kept constant to investigate the effect of different gas ratios on the selectivity and etch rate.

Table 4.1: Gas flow rates

[redacted]

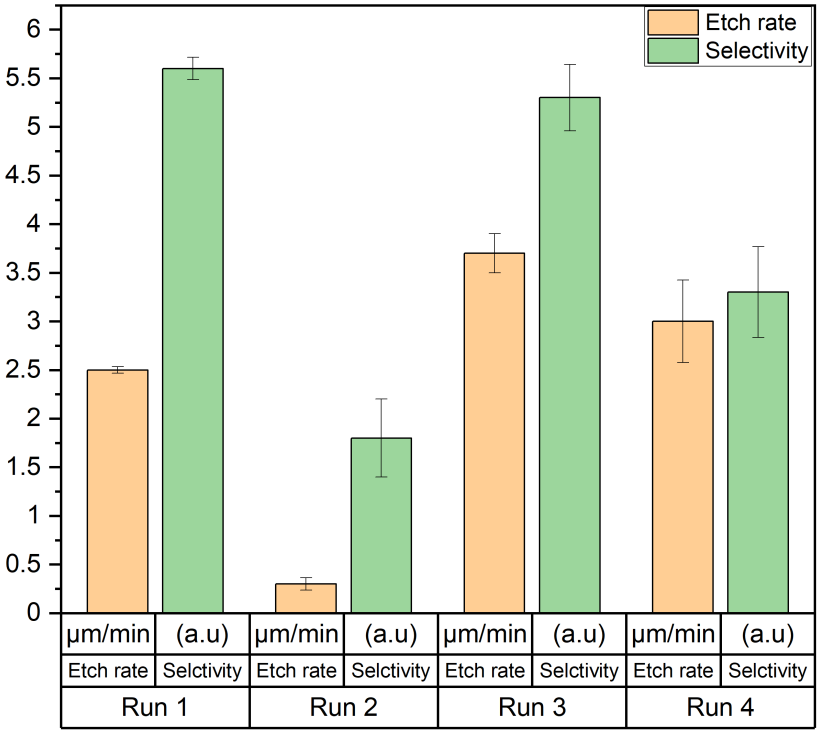
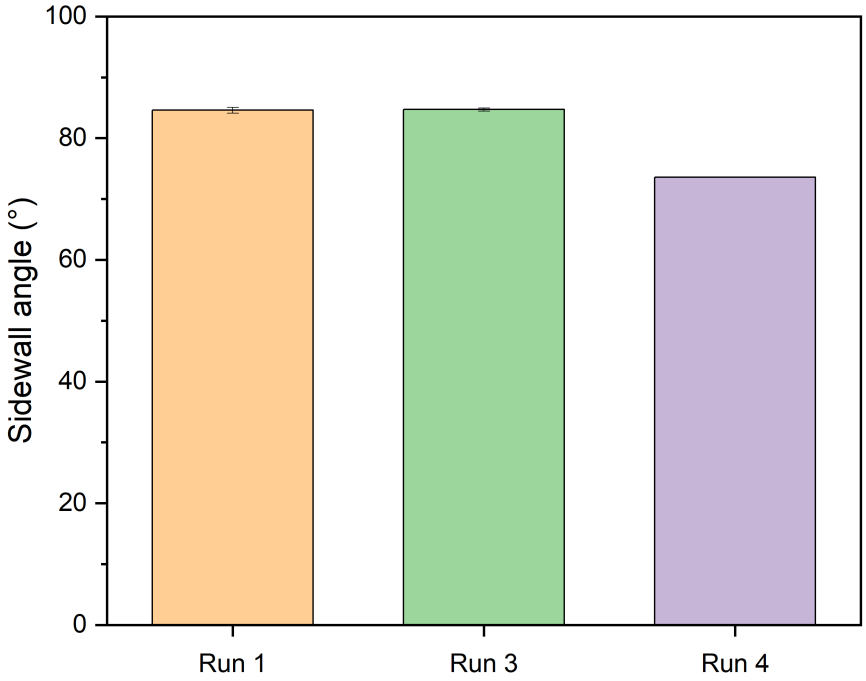


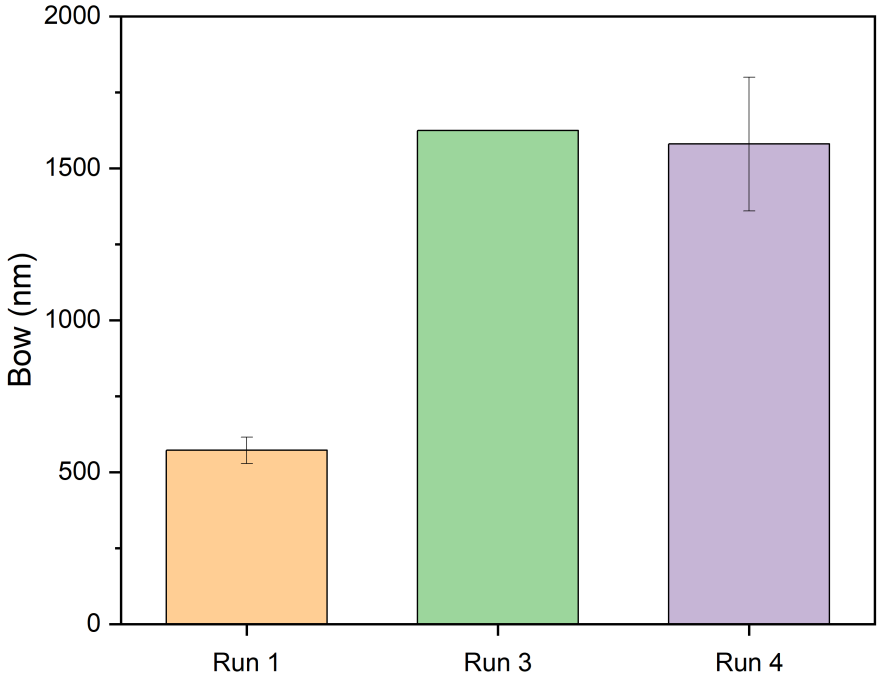
Figure 4.5: A comparison of the effect on selectivity and etch rate for different flow rates.

Figure 4.5 shows the etch rate and selectivity using the gas flow rates shown in Table 4.1. [redacted]; however, the profile quality suffers as the etch becomes more isotropic with the increased chemical etching. The increase in isotropic etching

can be seen by the increase in bow of the sidewalls resembling profile c in Figure 2.6. [redacted] BCl_3 [redacted] likely due to less chlorine ions being available to etch the InP. This reduction is also seen in run 4 when BCl_3 is introduced.



(a) A comparison of sidewall angle for different runs



(b) A comparison of sidewall bow for different runs

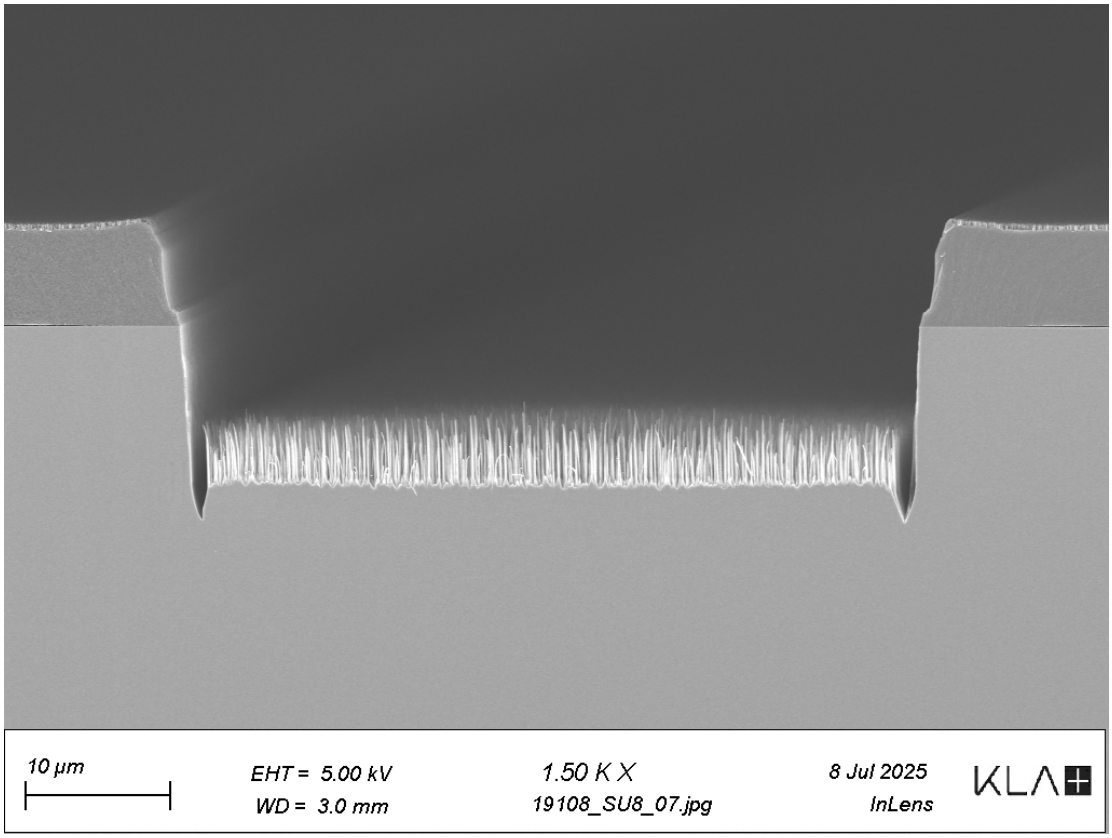
Figure 4.6: Plots comparing: a.) sidewall angle and b.)sidewall bow

Figure 4.6a shows the measured sidewall angle and bow for each run in Table 4.1. The reduction in the quality of the etch profile is shown by the <90° sidewall angles as well as the significant bowing shown in 4.6b. Note run 2 was excluded due to the depth of the etch only being 1.74 µm and thus the profile was difficult to determine.

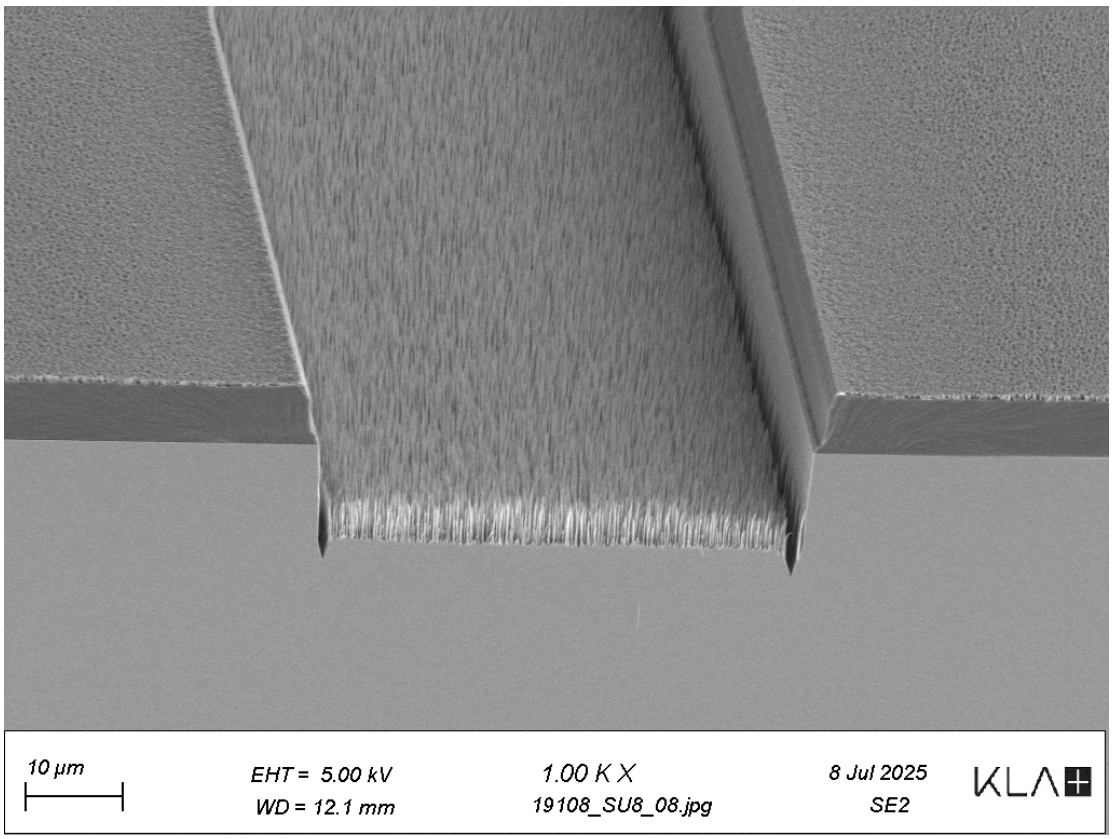
Passivation

Since the etch rate couldn't be increased by increasing gas rates without sacrificing sidewall quality the next option to improve selectivity was to passivate the mask. To improve selectivity, passivation using different flow rates of [redacted] was investigated. The highest etch rate recipe from the previous gas flow rate test was used as the starting point with two different flow rates of [redacted] being added

to passivate the sidewalls in order to achieve a more anisotropic etch profile while still trying to maintain the higher etch rate.



(a) A cross-sectional view of the etch profile of an SU-8 masked piece



(b) An oblique view of the micrograss in the trench of an SU-8 masked piece

Figure 4.7: SEM images of the micrograss

Micrograss shown in Figures 4.7a and 4.7b is caused by over passivation making the desorption of volatile etchant by-products more difficult, this leads to the formation of tiny pillar or needle like structures that resemble blades of grass.

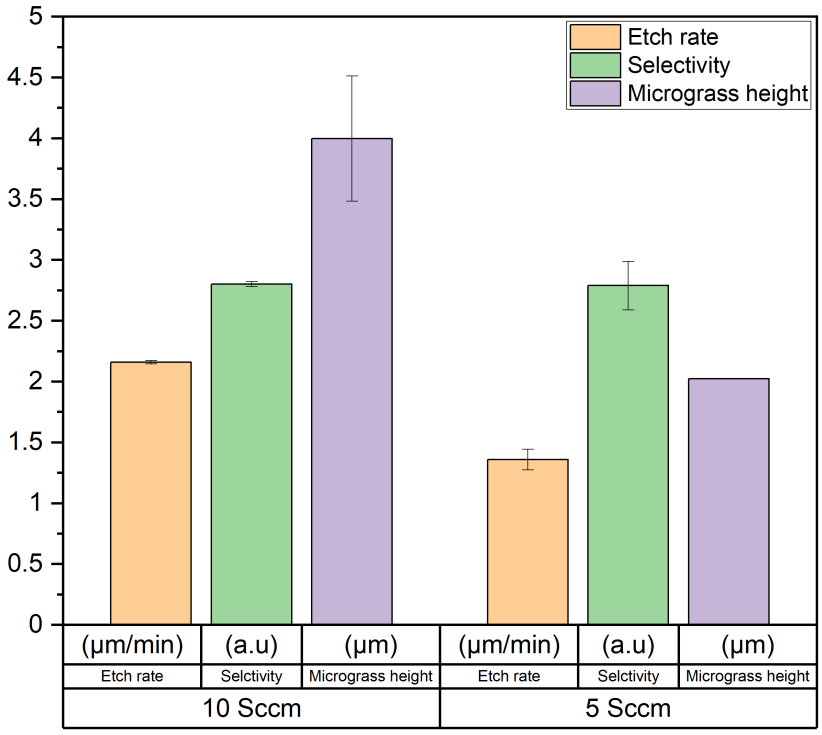


Figure 4.8: A comparison of the effect on selectivity and etch rate for different flow rates of [redacted]

Figure 4.8 shows the relationship between the [redacted] flow rate and the height of micrograss. As the [redacted] flow rate so does the micrograss height meaning [redacted] is unsuitable as a passivating gas.

Temperature

The SU8 used in the previous experiments wasn't previously hardbaked; however the [redacted] processing temperature essentially hard baked the SU8 during the etch. To test this theory as well as the effect of lower processing temperature had on the mask, the temperature was lowered to 140°C which is below the hardbaking temperature of SU8 as well as the recommended >150°C to etch the volatile InClx byproduct. For comparison one piece was hardbaked on a hotplate set to 180°C for 20 minutes while another piece was left untreated.

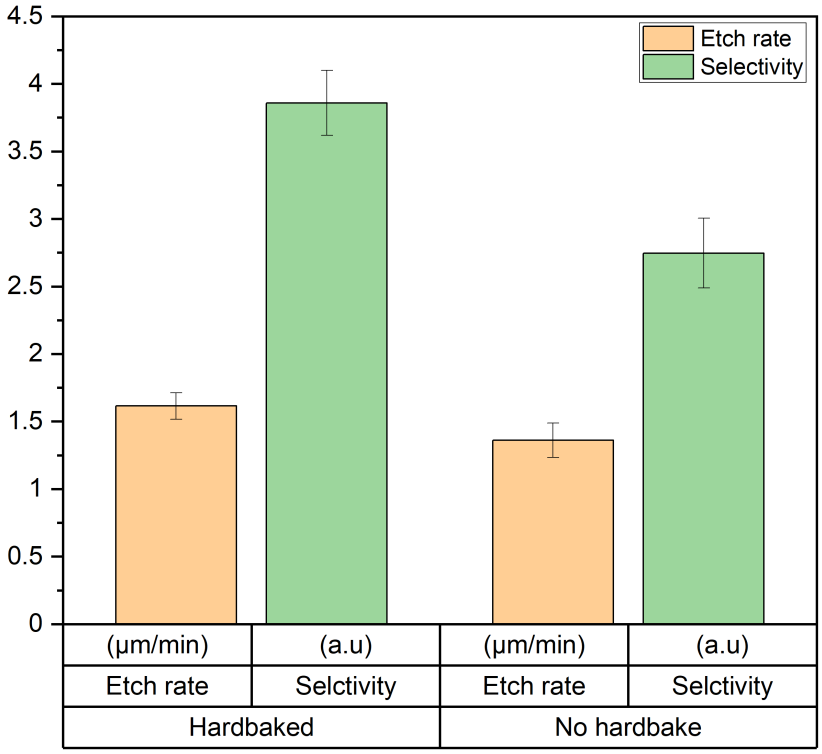


Figure 4.9: A comparison of the effect of processing temperature on the selectivity and etch rate between a hardbaked sample etched at 180 °C and a non-hardbaked sample etched at 140 °C

As expected, Figure 4.9 shows etch rate was reduced in both samples due to the lower temperatures and crosslinked SU8 improves the selectivity from 3:1 to 4:1.

4.1.2 SiO_2 mask

The recipe that achieved the deepest etch on SU8 was then repeated on a SiO_2 masked piece to compare the etch rate and selectivity shown in Figure 4.10.

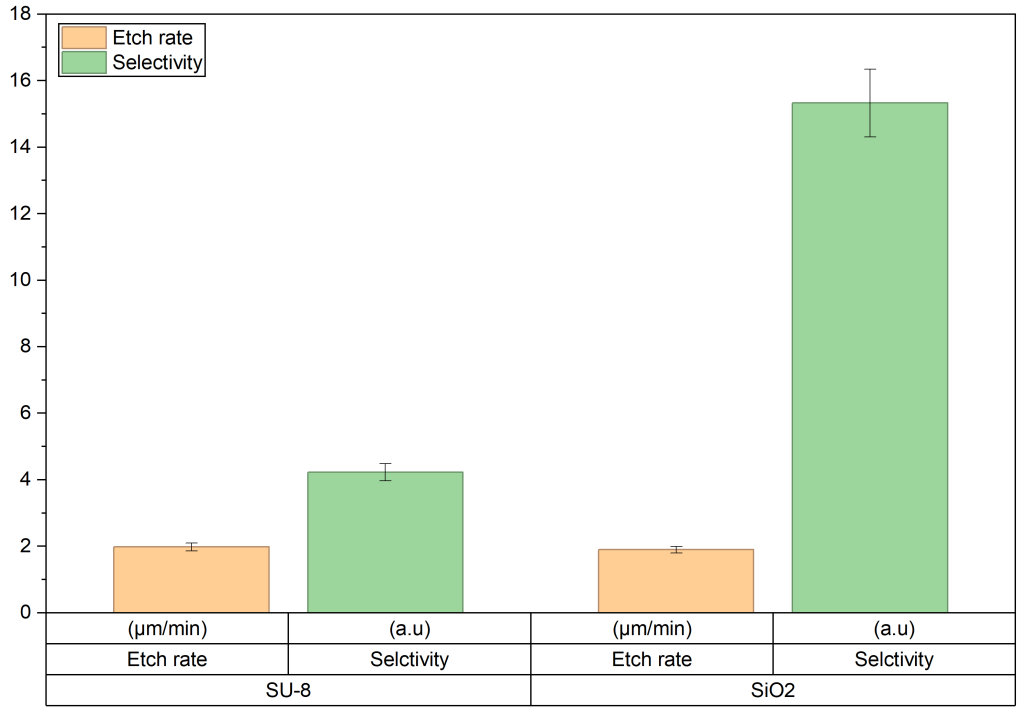
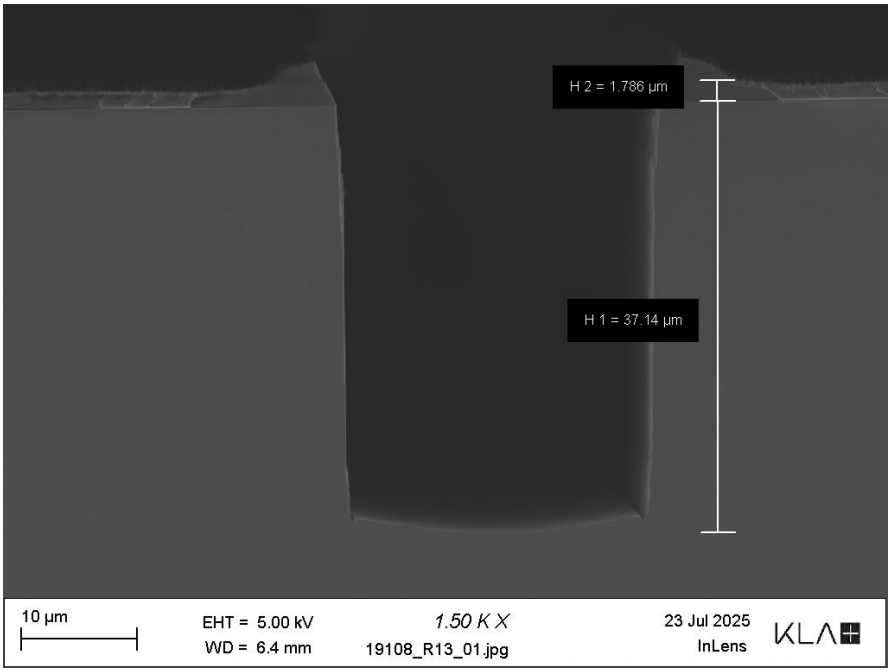
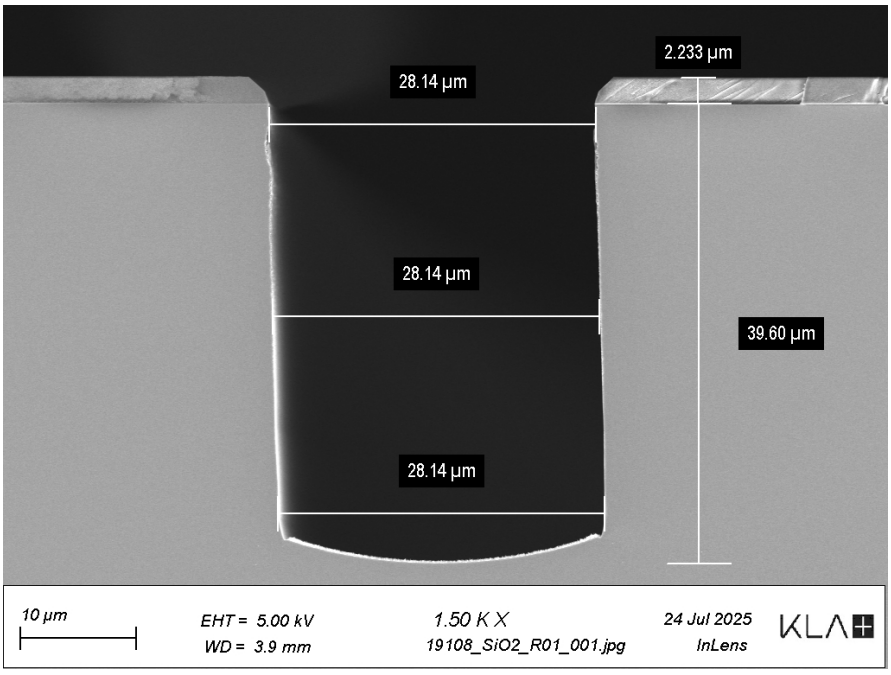


Figure 4.10: A comparison of etch rates and selectivity of mask to InP for SU-8 and SiO_2 using the same recipe

Figure 4.10 shows a significant increase in selectivity from 4.2 to 15.3 for SU-8 and SiO_2, respectively. The etch rates remained the same and the resultant etch profiles remain the same as well as shown in Figure 4.11. With this selectivity the SiO_2 mask would have to be approximately 6.5 µm to etch to a >100 µm



(a) A cross-sectional view of the etch profile for the SU-8 masked piece



(b) A cross-sectional view of the etch profile of the SiO_2 masked piece

Figure 4.11: A cross-sectional view of the etch profiles of the SU-8 and SiO_2 masked piece.

4.1.3 Polyimide mask

Polyimide (PI) is a polymer found in materials such as kapton tape which is used in electronics due to its high heat resistance and electrical insulation properties.

Temperature

Running the same recipe as the SiO_2 and SU-8 mask for polyimide caused the PI mask to reflow shown in Figure 4.12.

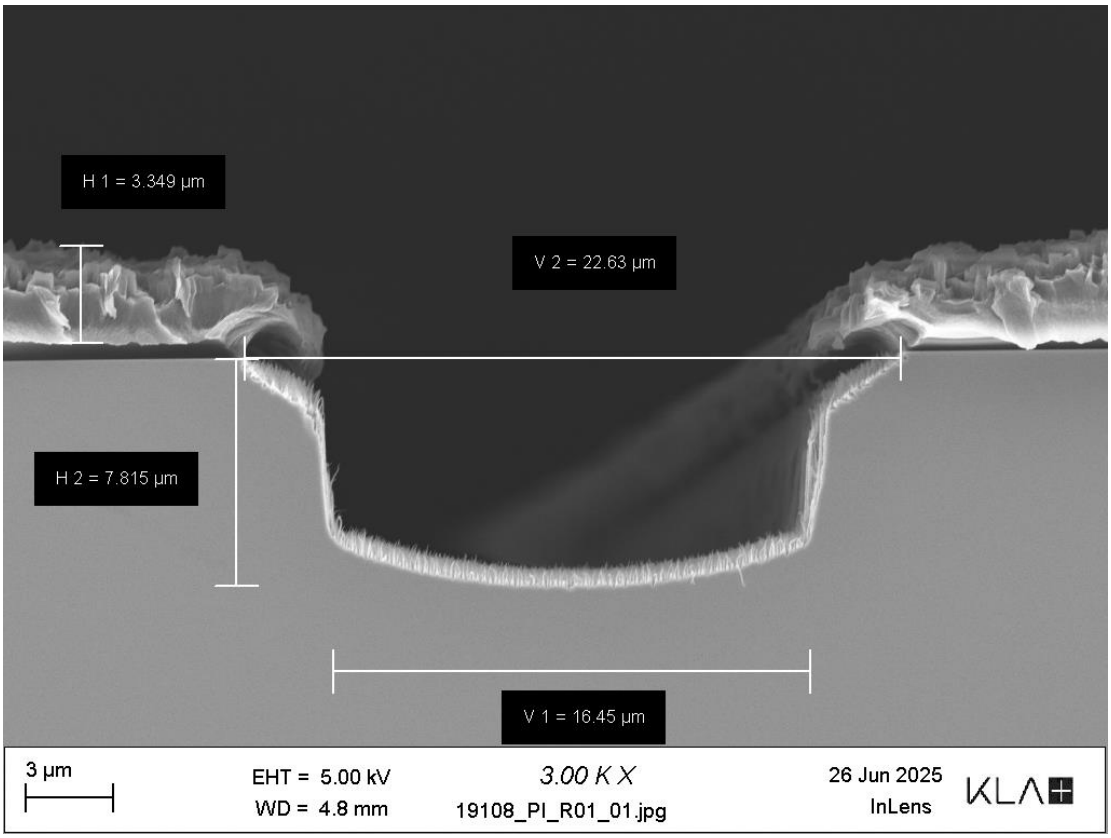


Figure 4.12: An SEM image of the etch profile of a PI masked piece after being etched at 180 °C showing signs of mask reflow.

To work around this limitation the effect of temperature was investigated. To investigate the effect of temperature on profile and reflow of PI the processing temperature was lowered to 160°C and 140°C.

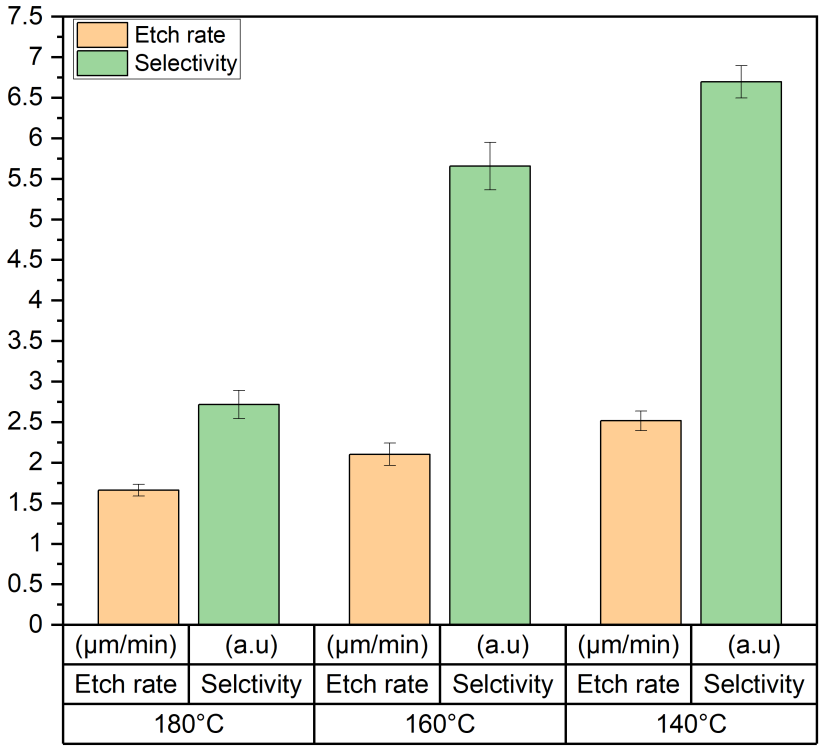
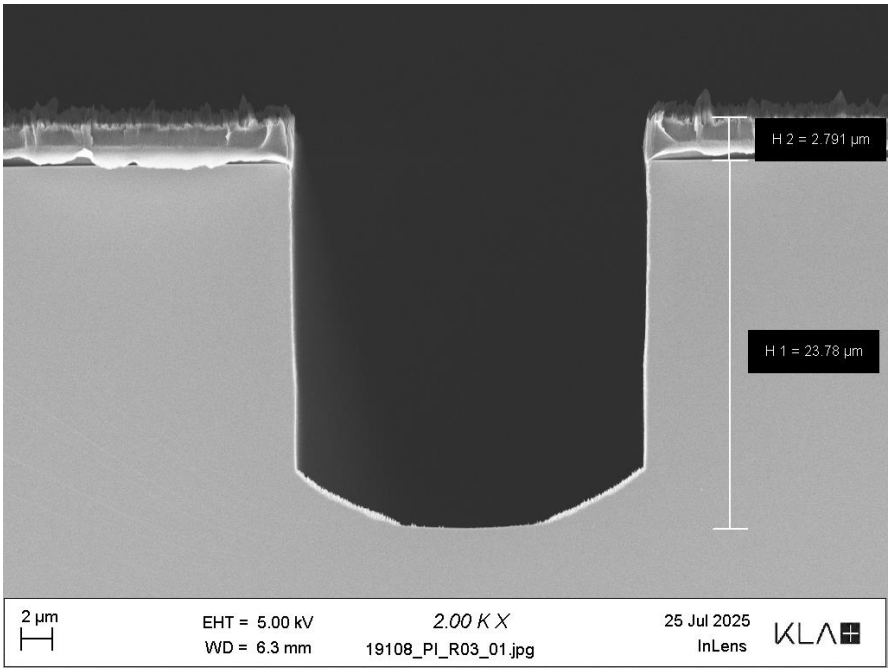
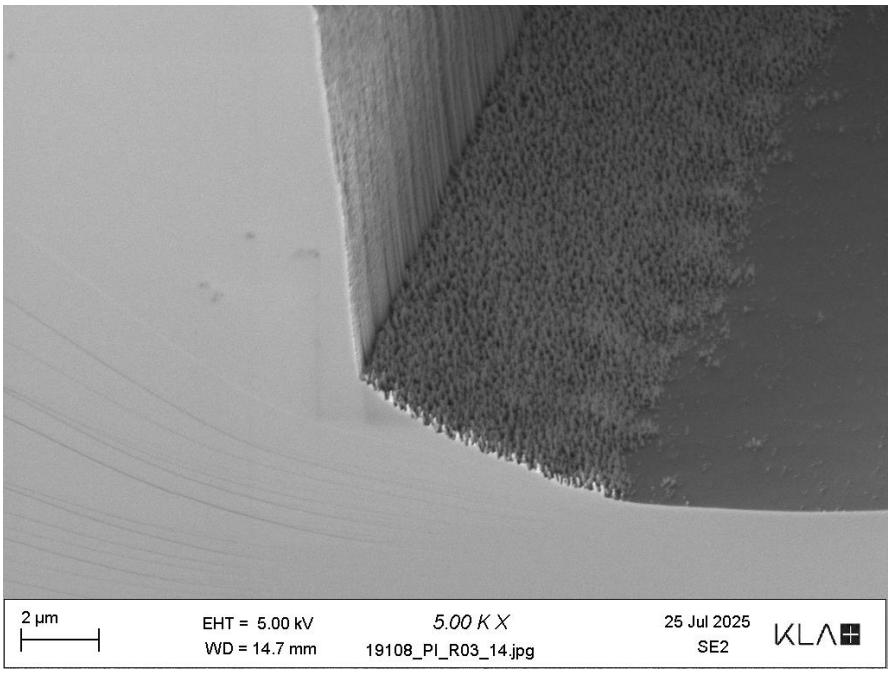


Figure 4.13: A comparison of the etch rate and selectivity of a PI masked piece etched at 180 °C,160 °C and 140 °C

Figure 4.13 shows both the selectivity and etch rate improved primarily due to the mask reflow being less pronounced at 160°C and completely eliminated at 140°C shown in Figure 4.14.



(a) A cross-sectional view of the etch profile for the 20 µm trench of a PI masked piece etched at 140°C



(b) An oblique view of the micrograss along the base of the 20 µm trench sidewalls of a PI masked piece

Figure 4.14: SEM images of the etch profile of the 140°C run on a PI masked piece.

Figures 4.14a and 4.14b both show an etch profile similar to that of the SU-8 runs at 180°C despite being run at 140°C. The only evidence of poor desorption due to low energy of the volatile etch byproduct $InCl_x$ is the micrograss at the base of the sidewalls.

Affect of sample size

Since more PI coated InP material was available the effect of increasing the surface area or open area could be investigated as well as whole wafer tests. Previous runs were tested on approximately 10 mm by 10 mm this was increased to 25 mm by 25 mm pieces correspondence to a 525% increase in surface area. The same recipe that produced figure 4.14a was rerun on a larger test piece as well as the effect of changing gas flow rates to compensate for the increase in surface area.

Table 4.2: Gas flow rates for the 25 mm by 25 mm pieces.

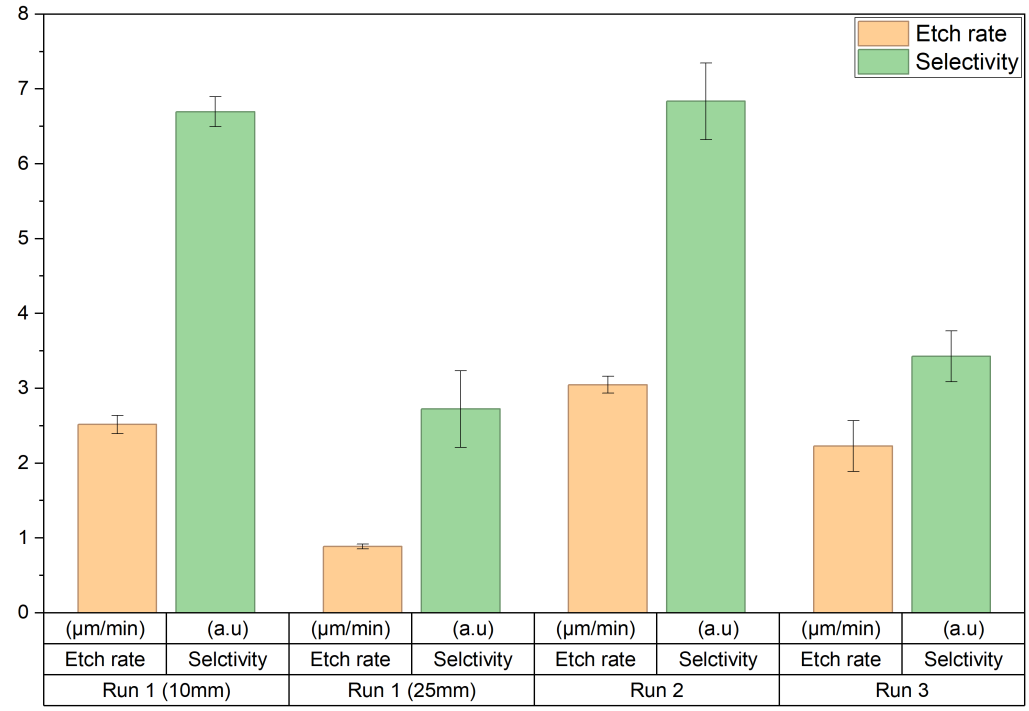
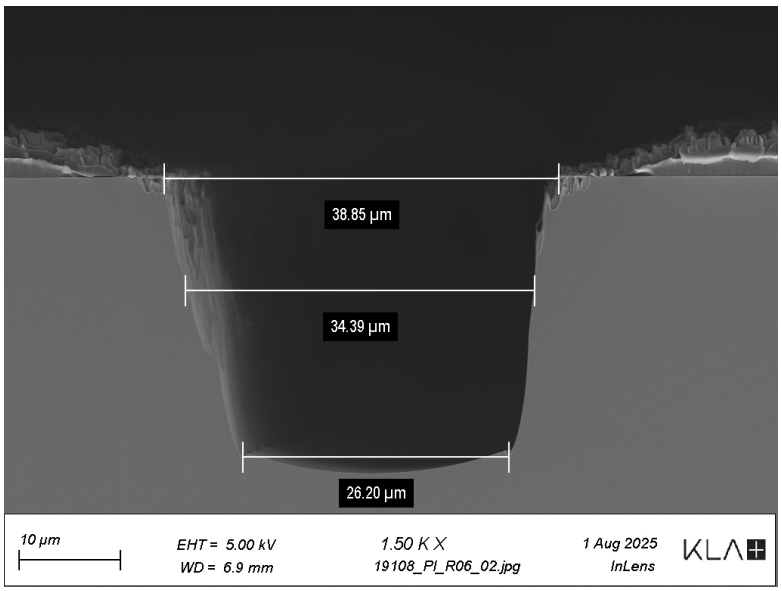
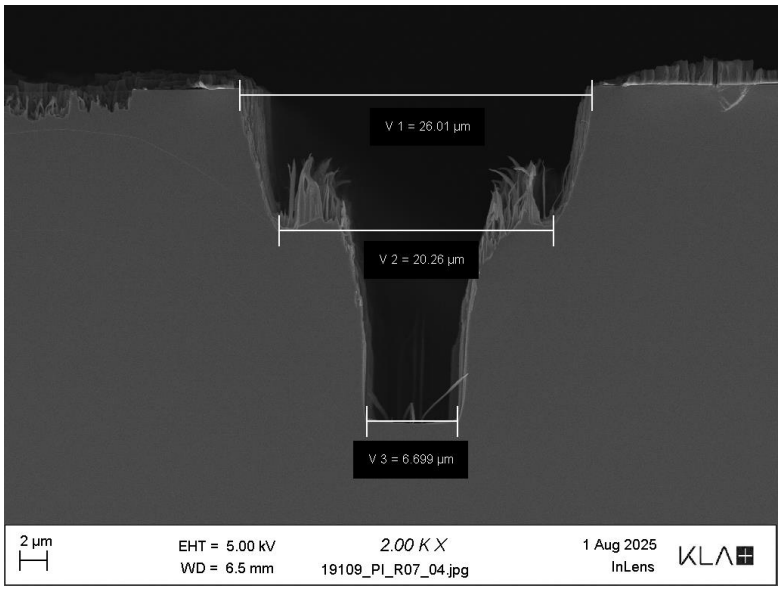


Figure 4.15: A comparison of etch rates and selectivity on 25 mm by 25 mm samples for different gas flow rates and pressure. Run 1 (10mm) and run 1 (25mm) correspond to a sample size of 10 mm by 10 mm and 25 mm by 25 mm respectively.

Figure 4.15 shows running the same recipe on a larger open area piece caused a significant process shift reducing both the etch rate and selectivity. By increasing the gas flow rates to compensate for the increase in open area the etch rate and selectivity of run 2 increases to that of the etch rate and selectivity in Figure 4.13. Run 3 shows a reduction in etch rate and selectivity when doubling the pressure from run 2. [redacted]. This was exacerbated in the narrower 20 µm trenches where the mean free path is further reduced. This is shown in Figures4.16a and 4.16b



(a) A cross-sectional view of the etch profile for the 20 µm trench for run 2 using a PI mask



(b) A cross-sectional view of the etch profile for the 20 µm trench for run 3 using a PI mask

Figure 4.16: SEM images of the etch profile of the 20 µm trenches for run 2 and 3.

4.1.4 Summary

For the Cl/Ar plasma chemistry, the SiO_2 hard mask provided the best selectivity and etch rate while maintaining a vertical anisotropic etch profile. SU-8 provides a good profile for a photoresist and the ability to withstand a 180°C processing temperature allows for a larger processing window when comparing to PI. SU8 is evidently easily etched by volatile Cl ions as well as from ion bombardment leading to a low selectivity. The PI reflowing at temperature > 150°C severely limits the processing window making PI incredibly sensitive to changes in processing parameters and open area.

4.2 HBr:Ar chemistry

Once all options were exhausted to achieve a >100 µm deep trench by increasing the selectivity and etch rate the main etchant gas was switched from Cl to Hydrogen bromide (HBr). Due to limited ICP tool availability there was less opportunity to optimise as much as the Cl/Ar chemistry.

4.2.1 SU-8 mask

- [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
  - [redacted]
    - [redacted]
- Etch:

  - Time: [redacted]
  - Primary source power: [redacted]
  - Platen power: [redacted]
  - Chamber pressure: [redacted]
  - Helium backflow pressure: [redacted]
  - Plasma chemistry:
    * Argon: [redacted]
    * Nitrogen: [redacted]
    * HBr: [redacted]

- Oxygen clean:
  - Time: [redacted]
  - Primary source power: [redacted]
  - Platen power: [redacted]
  - Chamber pressure: [redacted]
  - Helium backflow pressure: [redacted]
  - Gas flows
    * Argon: [redacted]
    * Oxygen: [redacted]

Running this recipe gives the profile shown in Figure 4.17

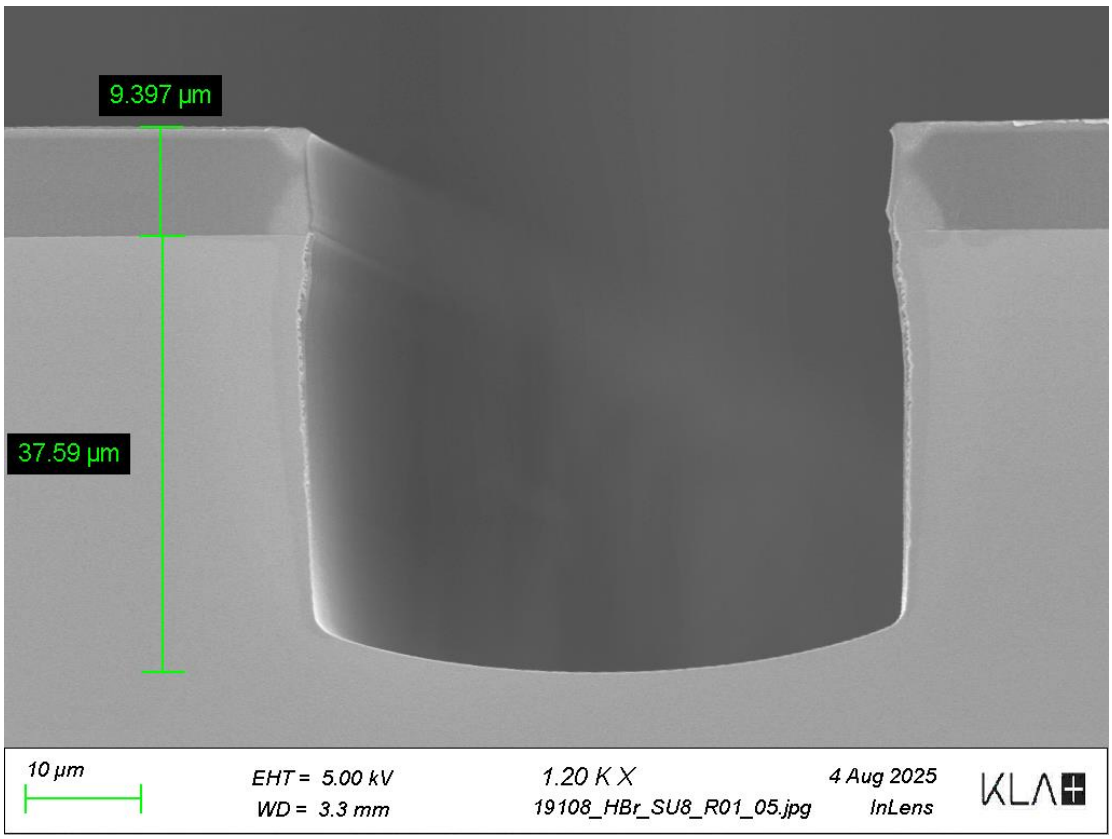


Figure 4.17: The resultant etch profile of a 50 µm trench of an SU8 masked piece using a HBr based plasma chemistry.

Figure 4.17 shows a slightly isotropic etch profile evident by the sidewalls being slightly rounded. This isotropic etching still occurred despite passivation from the [redacted]. This means the pressure is most likely causing the anisotropy of the etch. The selectivity however has improved to 23.5:1 compared to 5.6:1 which was the best selectivity achievable for a [redacted] chemistry. This increase in selectivity appears to be caused by the [redacted] forming a stronger polymer with the SU-8. To address the under cutting and slightly isotropic etch the processing pressure was reduced from [redacted]. Running the recipe gave the following profile shown in Figure 4.18.

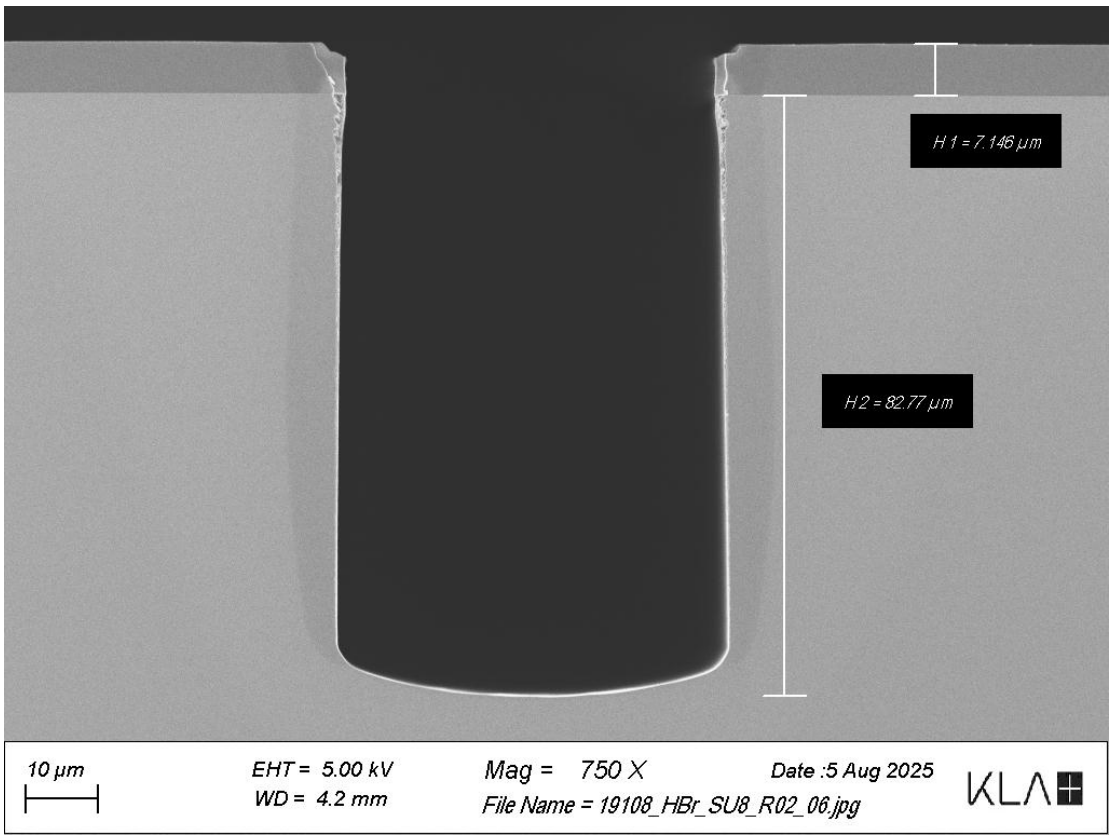


Figure 4.18: The resultant etch profile for a 50 µm trench of a SU8 masked piece using the lower pressure recipe

Figure 4.17 shows a reduction in the isotropy of the etch with a more vertical anisotropic etch profile. Since the etch profile had improved by decreasing the pressure the same recipe was run for longer to see if a deep >100 µm etch could be achieved.

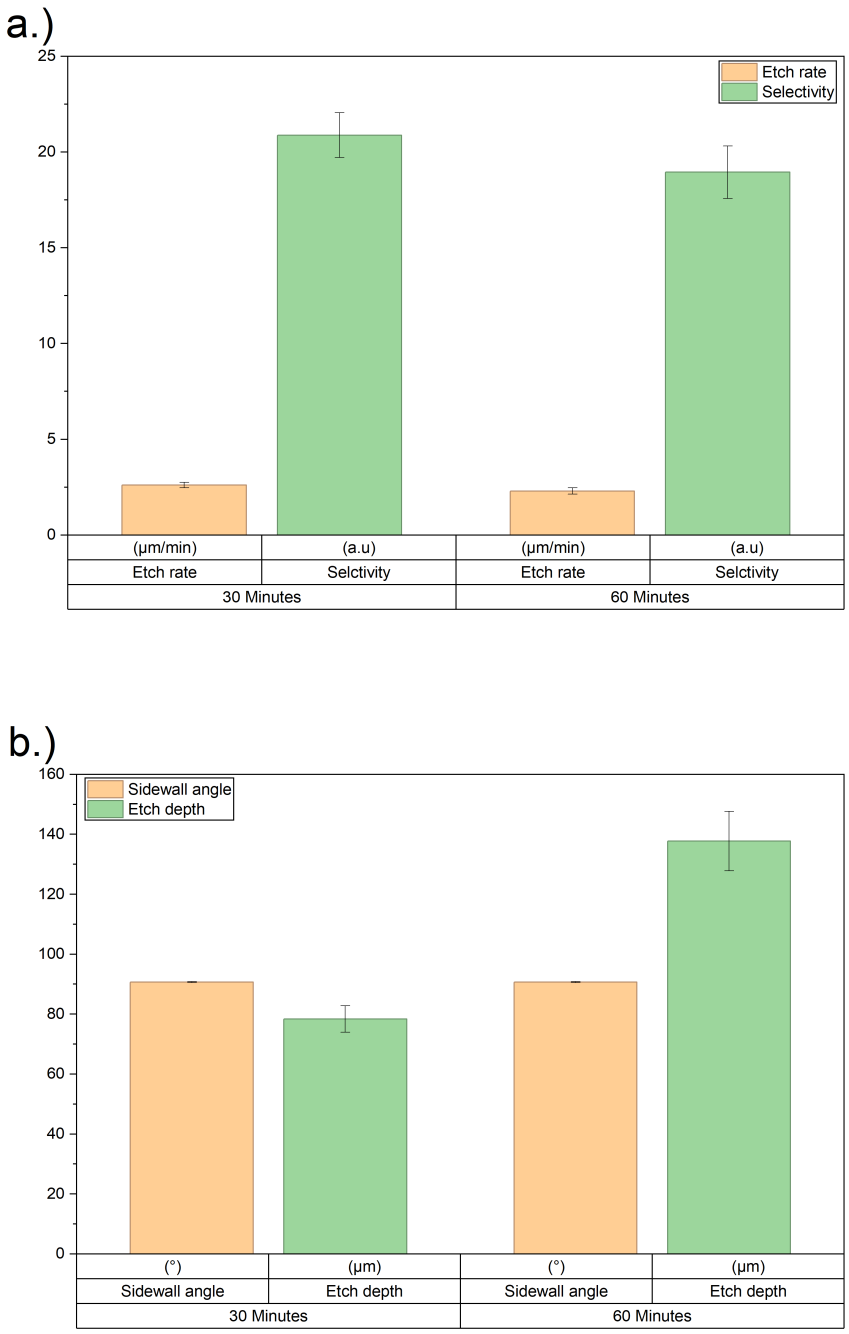


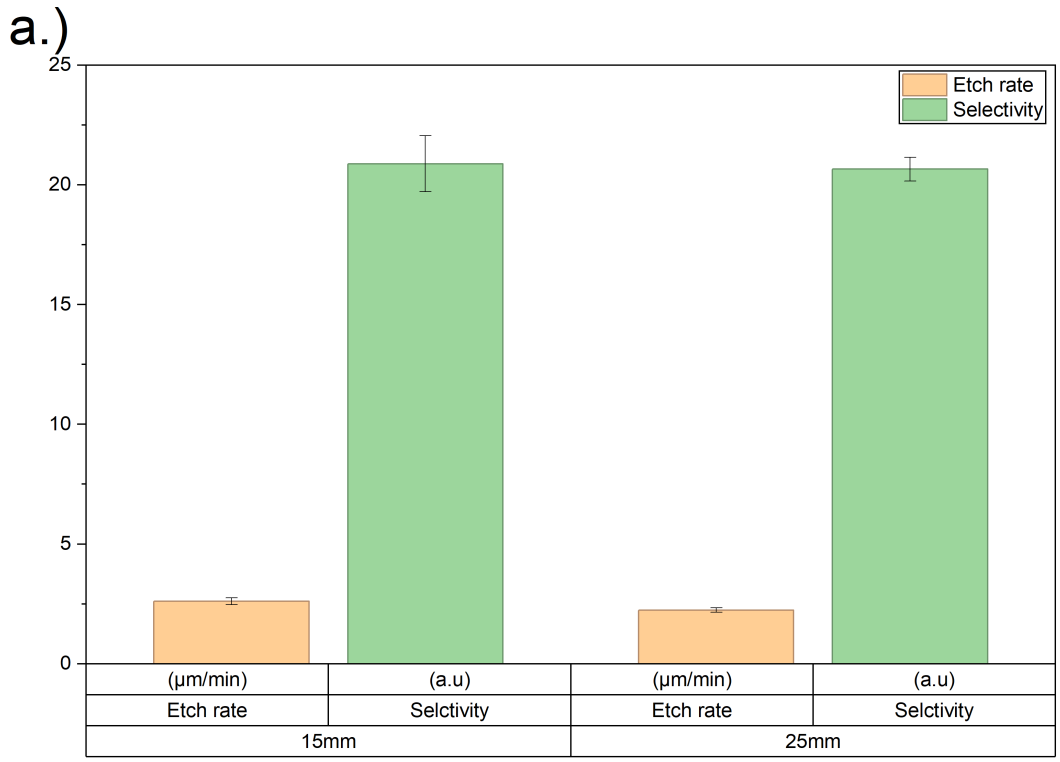
Figure 4.19: a) Comparison of etch rate and selectivity for increasing process time b) Comparison of sidewall angle and etch depth for increasing process time. Both runs were done on an approximately 15 mm by 15 mm test piece

Figure 4.19b shows the vertical profile is maintained for the full 60 minute etch

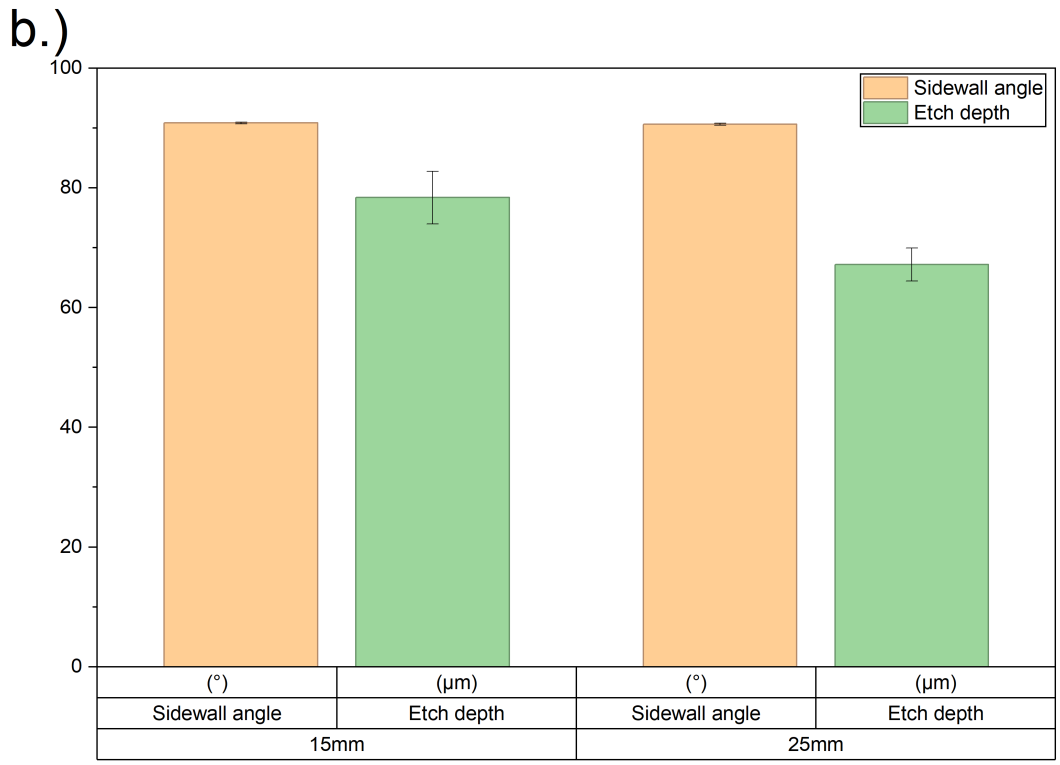
and a >100 µm depth etch was achieved. The etch rate in figure 4.19a decreased from 2.6 µm/min to 2.3 µm/min.

High open area

The effect of open area was tested going from 15 mm by 15 mm test pieces to 25 mm by 25 mm test pieces.



(a) Comparison of etch rate and selectivity for increasing open area



(b) Comparison of sidewall angle and etch depth for increasing open area

Figure 4.20: a.) Comparison of etch rate and selectivity for increasing open area b.) Comparison of sidewall angle and etch depth for increasing open area

Figure 4.20a shows a 0.3 µm/min decrease in etch rate as the open area increases which is expected as more radicals are being used to etch a larger open area. In Figure 4.20b the 90° sidewall angle is maintained when increasing the open area. With the only process shift when moving to bigger pieces being a small reduction in etch rate, the recipe should work on a whole wafer albeit with a further reduction in etch rate.

4.2.2 SiO_2 mask

Running the same recipe as Figure 4.20 on the SiO_2 hard masked piece gave the following etch profile shown in Figure 4.21.

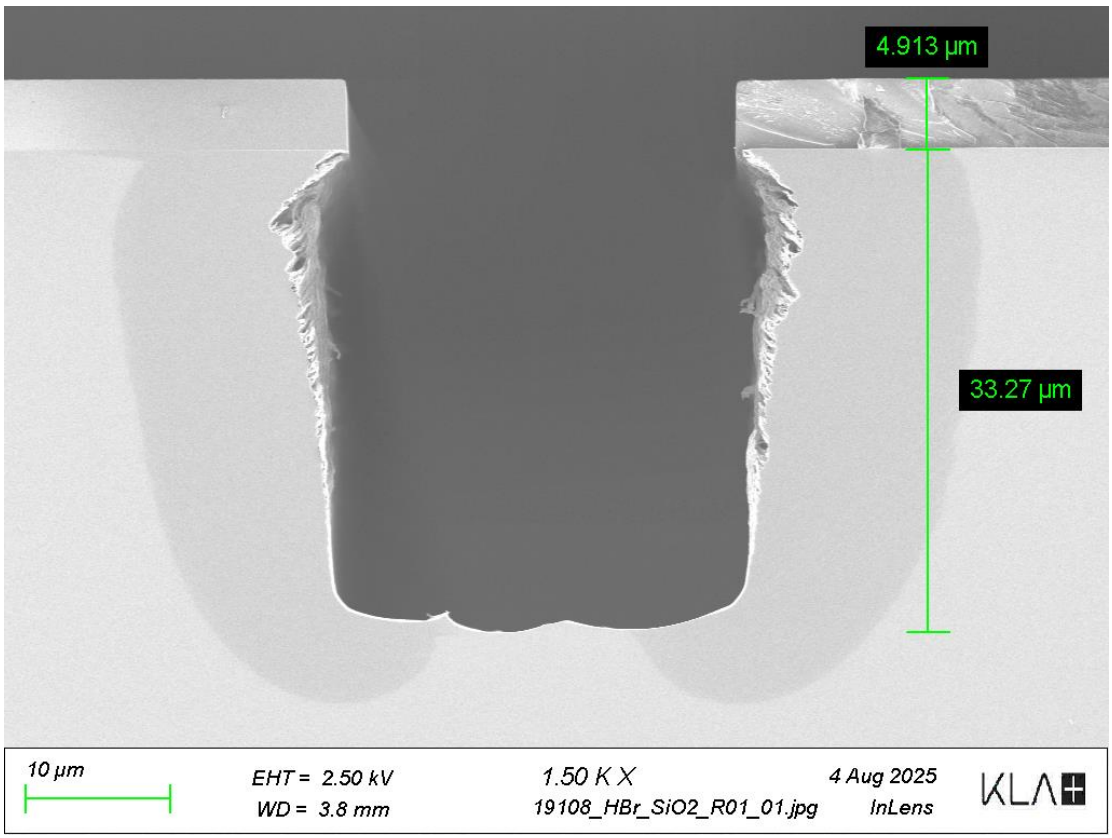


Figure 4.21: A SEM image of the etch profile of a SiO_2 masked piece post etch using a HBr plasma.

Figure 4.21 shows undercutting suggesting the [redacted] is not enough to passivate the sidewalls unlike the polymer that's formed with the SU-8 mask. However, the etch rate and selectivity however has improved to 400.3 and the etch rate was 3.5 µm/min. With additional passivation to protect the sidewalls this hardmask could be used to etch the full wafer thickness.

4.2.3 Polyimide mask

Due to limited tool time only one run using the PI mask could be done. This recipe was the same as the lower pressure recipe which gave the best result on SU-8. The processing temperature was kept the same at 180°C this again was due to limited tool time as the ICP module didn't have active cooling meaning the temperature had to drop to 140°C naturally. Running this recipe gave the

following profile shown in Figure 4.22

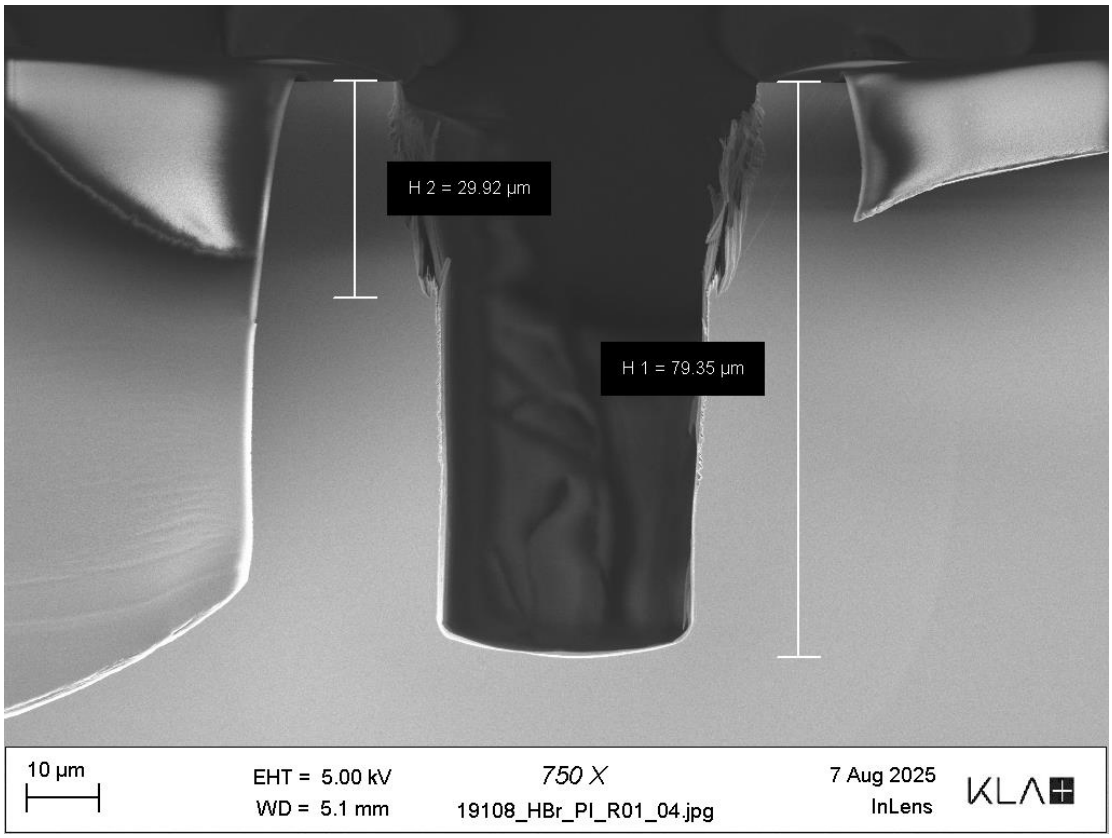


Figure 4.22: A SEM image of the etch profile of the PI masked piece post etch using a HBr plasma at 180 °C

Figure 4.22 shows mask reflow caused by the high processing temperature. The sidewalls also show signs of mask recession.

4.2.4 Summary

Using a combination of an SU-8 photoresist mask and a HBr plasama a $137.75 \pm 9.95\,\mu m$ deep etch was achieved while maintaining an average etch rate of $2.30 \pm 0.15\,\mu m/min$ and a selectivity of 20.9:1. This increased selectivity was most likely caused by a strong polymer being formed [redacted]. The SiO_2 mask had a high selectivity of $400.3 \pm 17.9\,\mu m/min$ but, the undercutting shown in Figure 4.21 means that additional process optimisation is required to passivate

the sidewalls to reduce the undercutting. At a processing temperature of 180°C the PI mask started to reflow again leading to mask recession.

Chapter 5

Metrology and defect analysis

5.1 EDX of SU8 mask

To investigate why the SU8 mask had a much higher selectivity in the HBr plasma EDX was used to get an idea of the chemical composition of the SU8 mask after plasma etching. The EDX spectrum is given in Figure 5.1.

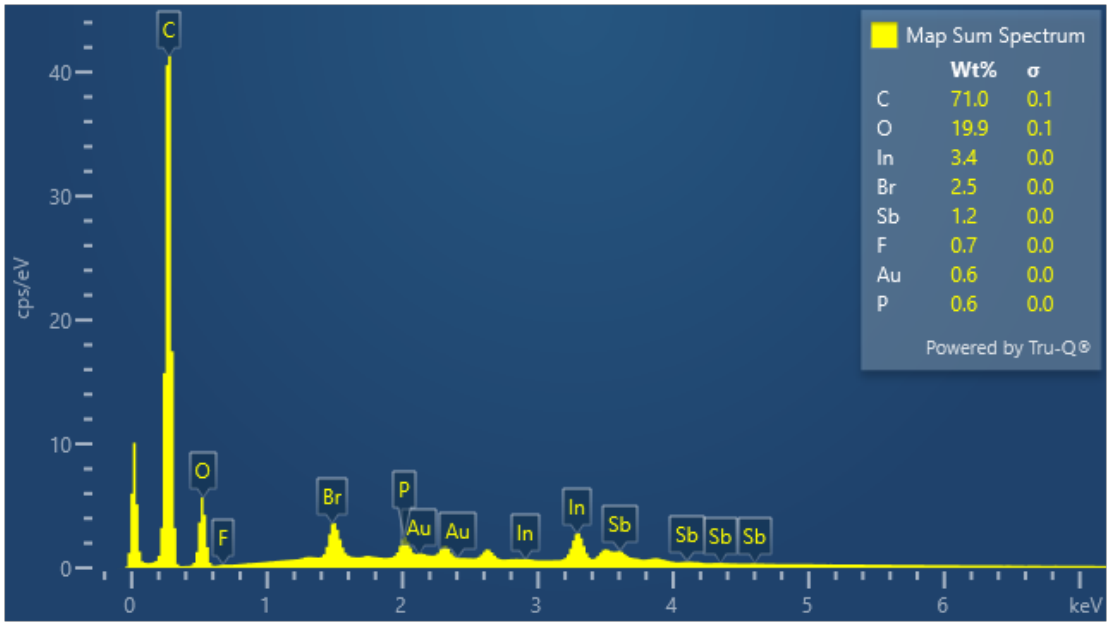


Figure 5.1: The EDX spectrum of the SU-8 mask after the HBr plasma

Figure 5.1 shows the SU-8 has [redacted]

[redacted] appears to make the SU-8 more resistant to etching.

5.2 Removing the masking material

Before any potential defects could be analysed the masking material had to be removed. The same properties that make SU8 chemically resistant also make cross-linked SU8 is notoriously difficult to remove. Various methods were tested to remove both the SU8 and the polyimide mask with there effectiveness and subsequent surface quality investigated to determine the best removal method.

5.2.1 Dry etch removal

Plasma ashing

Using a plasma asher the following recipe was used to remove the crosslinked SU8 via plasma ashing

- Plasma chemistry: 20sccm O2
- RF power: 250 W
- Etch time: 15 minutes

This recipe was chosen as 250 W was the maximum source power available on this specific plasma asher. The step height of a trench was measured before and after the etch using profilometry. From this using Equation 2.4 the etch rate was determined to be 479.41 nm/min

5.2.2 Wet etch removal

Technistrip P1316

Technistrip P1316 is a photoresit remover designed to remove highly crosslinked photoresists. Approximately 200 mL of P1316 was poured into a beaker that was resting on a hotplate set to 70°C. This was to add thermal energy in order to

break down the polymer chains in the photoresist. The Polyimide was completely dissolved in this heated solution after 30 minutes. The SU8 took two and a half hours in total for the photoresist to eventually swell off. This is the same mechanism of removal noted in the SU8 datasheet using the recommended SU8 remover. Once the SU8 has swollen off the InP there appears to be little to no residue.

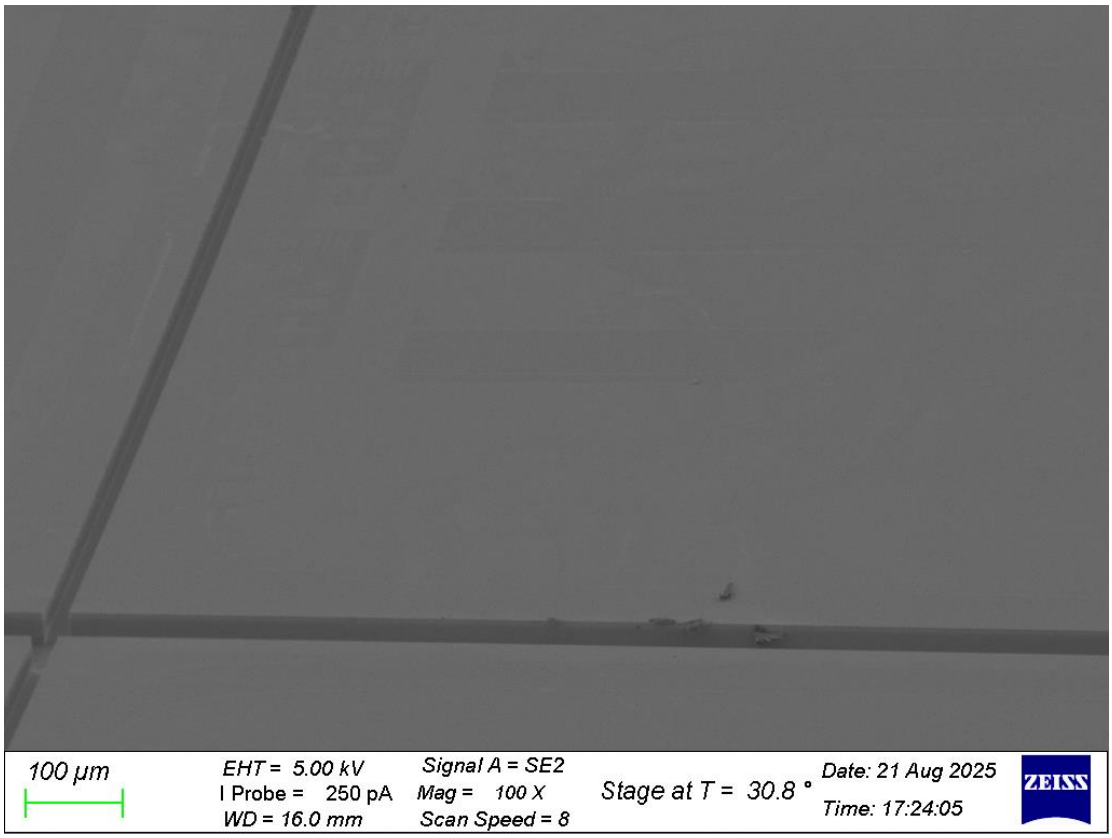


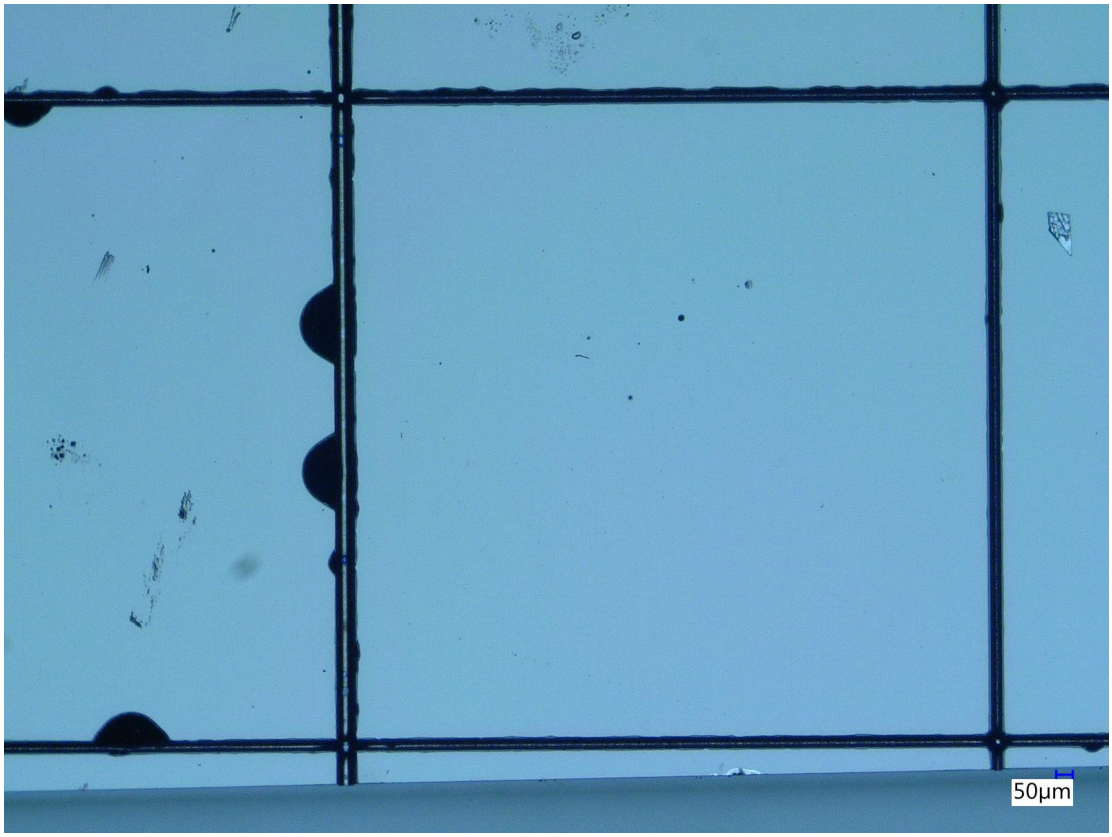
Figure 5.2: An oblique SEM view of the etched InP after the P1316 strip

The subsurface etches from Figure 3.1 are visible in Figure 5.2 suggesting the SU8 has been completely stripped.

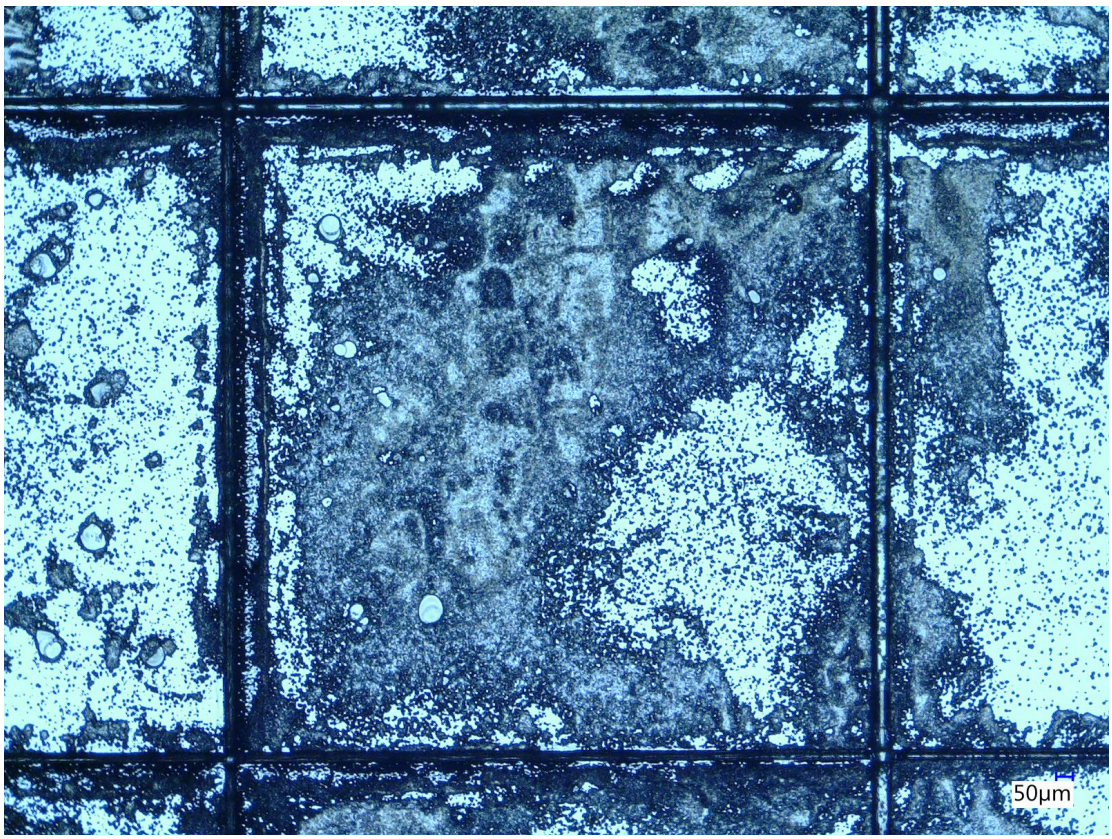
Pirahna solution

Pirahana solution is a combination of sulphuric acid and hydrogen peroxide typically in a ratio of 3:1 or 7:1 (Sulfuric acid to hydrogen peroxide). A 7:1 ratio was used to try and strip the SU8 layer shown below in Figure 5.3a. Initially the

SU8 appeared to quickly react with the piranha solution, but this subsided after 5 minutes when the solution no longer appeared to react. After 10 minutes the pieces were rinsed in deionized water before being dried using a nitrogen gun. A residue was left behind after the wet etch. To try and remove this residue piranha solution was tried again using a fresh solution. After the additional 10 minutes in piranha solution the surface was examined using an optical microscope, the results are shown in Figure 5.3.



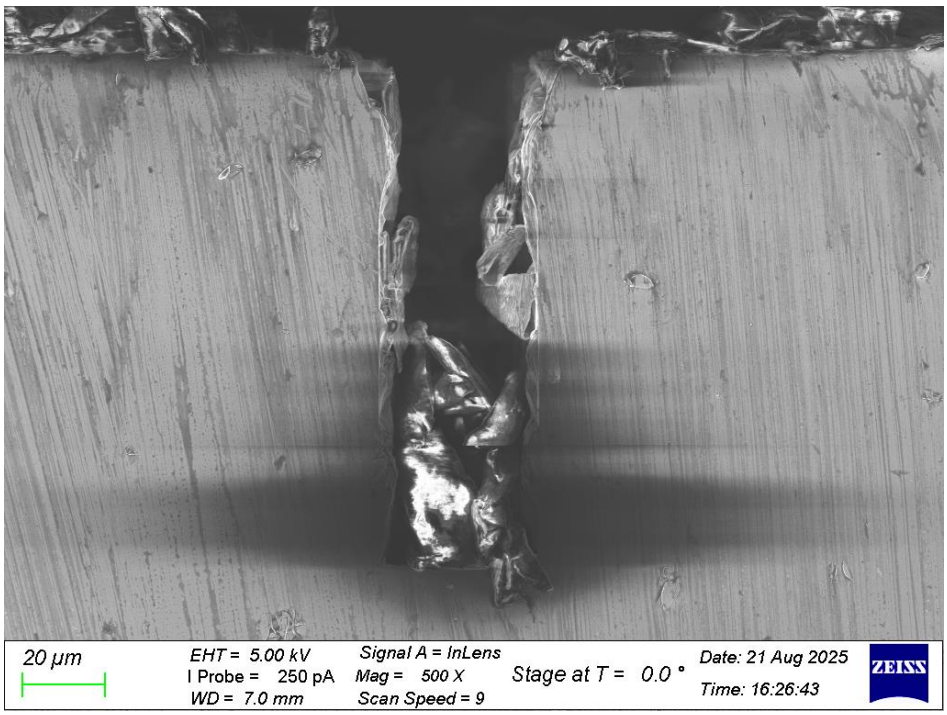
(a) The SU8 mask before the Piranha solution



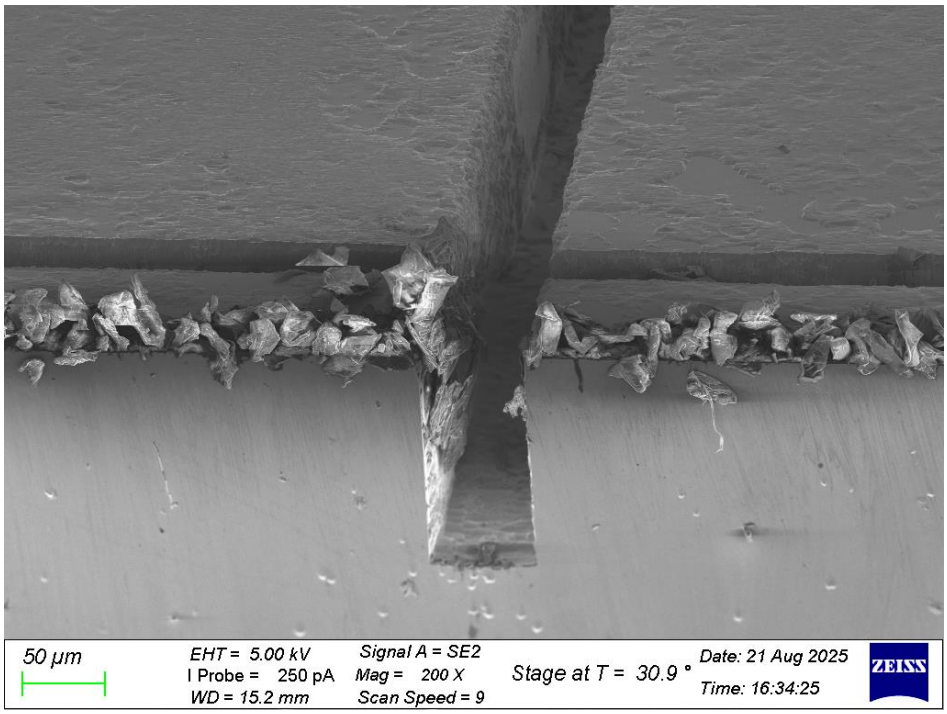
(b) The SU8 mask after the Piranha solution

Figure 5.3: Optical microscope photos pre and post wet etch.

The lighter regions in Figure 5.3b Show the the piranha solution only stripped some of the SU-8 to the surface. The darker regions are most likely highly crosslinked SU-8 that was not easily broken down by the pirahana solution



(a) Cross sectional view of the trench after piranha solution



(b) Oblique view of the surface post Piranha solution

Figure 5.4: The cross sectional (a) and oblique (b) SEM images of the etched InP post piranha solution

Figure 5.4a show the piranha has little affect on the polymer deposition on the sidewalls and appears to attack the InP as well shown in Figure 5.4b.

Removing the SiO_2 mask with HF

Due to a combination of health and safety considerations and a limited time frame the SiO_2 mask could not be removed using HF post plasma etch. The SiO_2 mask should be readily dissolved in HF following a procedure similar to the one outlined in 3.1.1.

5.2.3 Additional removal method

Though not applicable to industry it should be noted that the SU8 was easily removed using tape to peel off the SU8. This could be theoretically scaled up by using UV cured dicing tape sticking the InP SU8 side down then once the InP is removed from the tape the SU8 should peel off.

5.3 Summary of removal methods

A Bruker DektakXT profilometer was used to determine the roughness average and average maximum height shown below in Table 5.1.

Table 5.1: Roughness average and average maximum height as measured using profilometry for each removal technique. "InP surface" refers to the roughness of the InP wafer surface before processing

Removal method	Roughness average (nm)	Average maximum height(nm)
InP surface	3.19	3.6
O2/SF6 plasma	24.97	169.92
O2 plasma ash	18.34	131.03
Piranha	97.79	498.95
P1316	5.68	25.69

Table 5.1 shows that the P1316 removal provided the highest surface quality giving a surface roughness of 5.68 µm. However, the 2 hour 30 minute time to strip would severely limit throughput. The O2 plasma ash and O2/SF6 plasma both left a similar amount of residue but were much quicker both taking 20 minuets.

5.4 Saw dicing InP

A clean 600 µm InP wafer was partially cut to a depth of 100 µm to compare with the plasma etched samples. An ultra-thin 10 µm kerf width ZHZZ-SD4800-H1-70 blade by the Disco corporation was used as the dicing blade. This blade was chosen as it is the thinnest dicing blade currently available to customers and thus represents some of the best results saw dicing can currently achieve. Before the InP was saw diced the blade was first dressed a process in which the diamonds are sharpened and exposed to improve material penetration and cutting quality. Once the blade was dressed the following parameters were chosen to saw dice the sample.

- Saw dicing parameters:

– Spindle rev (rpm):20000

– Feed speed (mm/s): 0.5

These specific parameters were chosen to minimise chipping and limit the potential for cracks to form.

5.5 Defect analysis

A sigma crossbeam 550 SEM with a parabolic mirror and CL photomultiplier tube attachment was used in conjunction with a visible to near IR filter. Odemis software was used to control the alignment as well as process the images. An example of a CL image is depicted in Figure 5.5.

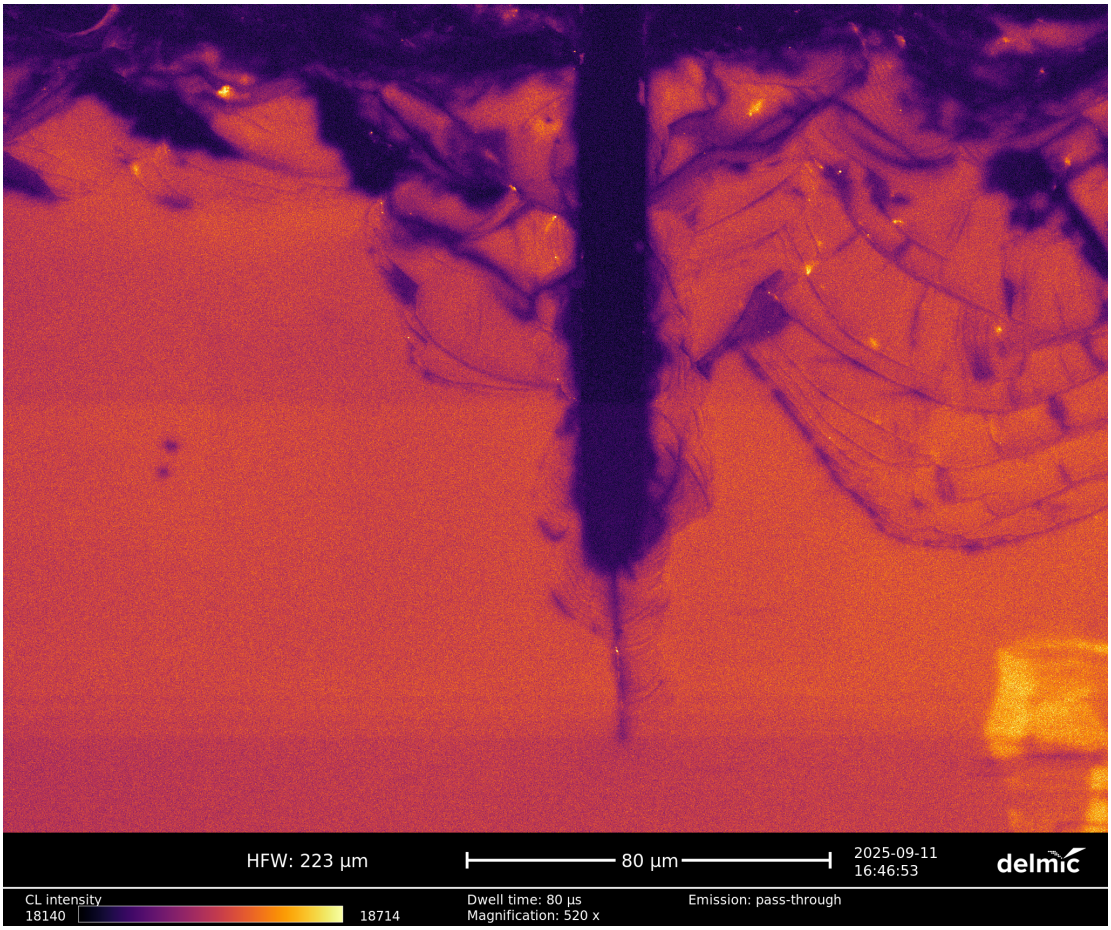


Figure 5.5: A CL intensity image of a saw diced trench at 20 keV.

Regions in dark blue/purple are areas which have a lower CL intensity meaning less photons are detected from these regions. This is primarily caused by defects causing a lower recombination efficiency which means less photons are emitted and therefore detected. The raw intensity $I_n(x)$ rises with increasing accelerating voltage so this is normalised I_{bulk} to account for differences in the raw CL intensity. This was done using the following equation

$$I_n(x) = \frac{I(x)}{I_{bulk}} \tag{5.1}$$

Where $I_n(x)$ is the normalised intensity at position x, $I(x)$ is the raw intensity at position x and I_{bulk} is the raw intensity of a section of defect free bulk InP far from the trench. The accelerating voltages were varied from 5 keV to 20 keV in the following order 5 keV, 7.5 keV, 10 keV, 15 keV, 20 keV.

Table 5.2: Electron beam penetration depth according to the Kanaya–Okayama model.

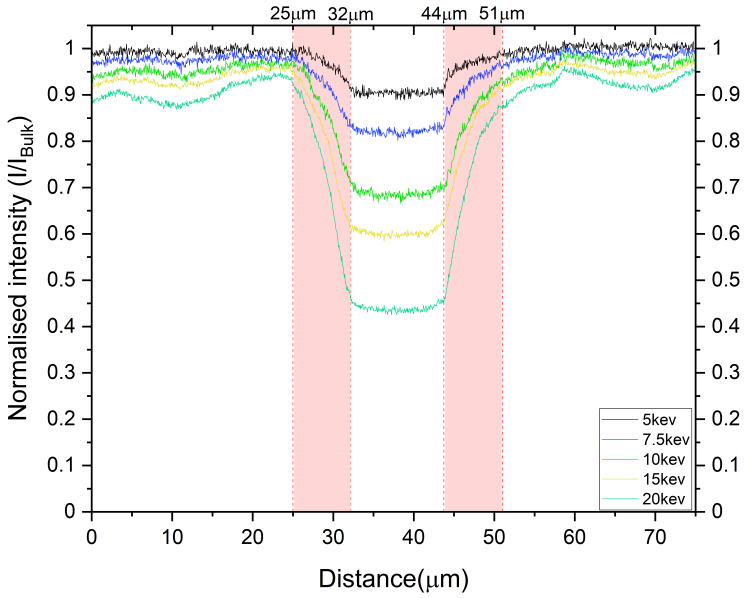
Accelerating voltage (keV)	Electron beam penetration (µm)
5	0.281
7.5	0.554
10	0.895
15	1.762
20	2.848

Table 5.2 shows the corresponding beam penetration depth for each accelerating voltage using the Kanaya–Okayama. These accelerating voltages were selected to identify defects both at the surface and deeper within the material. The maximum accelerating voltage was chosen to be 20 keV as going beyond this could start to introduce damage from the electron beam of the SEM. Additionally higher accelerating voltages could cause the sample to heat up causing the recombination efficiency to be altered.

5.5.1 Comparison of samples

The saw diced sample was compared to the best masking materials for their respective chemistries. For the HBr plasma chemistry the SU-8 photoresist mask and for the Cl/Ar plasma chemistry the SiO_2 hard mask. The SU-8 and SiO_2 were selected as they represent the deepest etches for their respective chemistries whilst maintaining a vertical 90° etch profile.

a.)



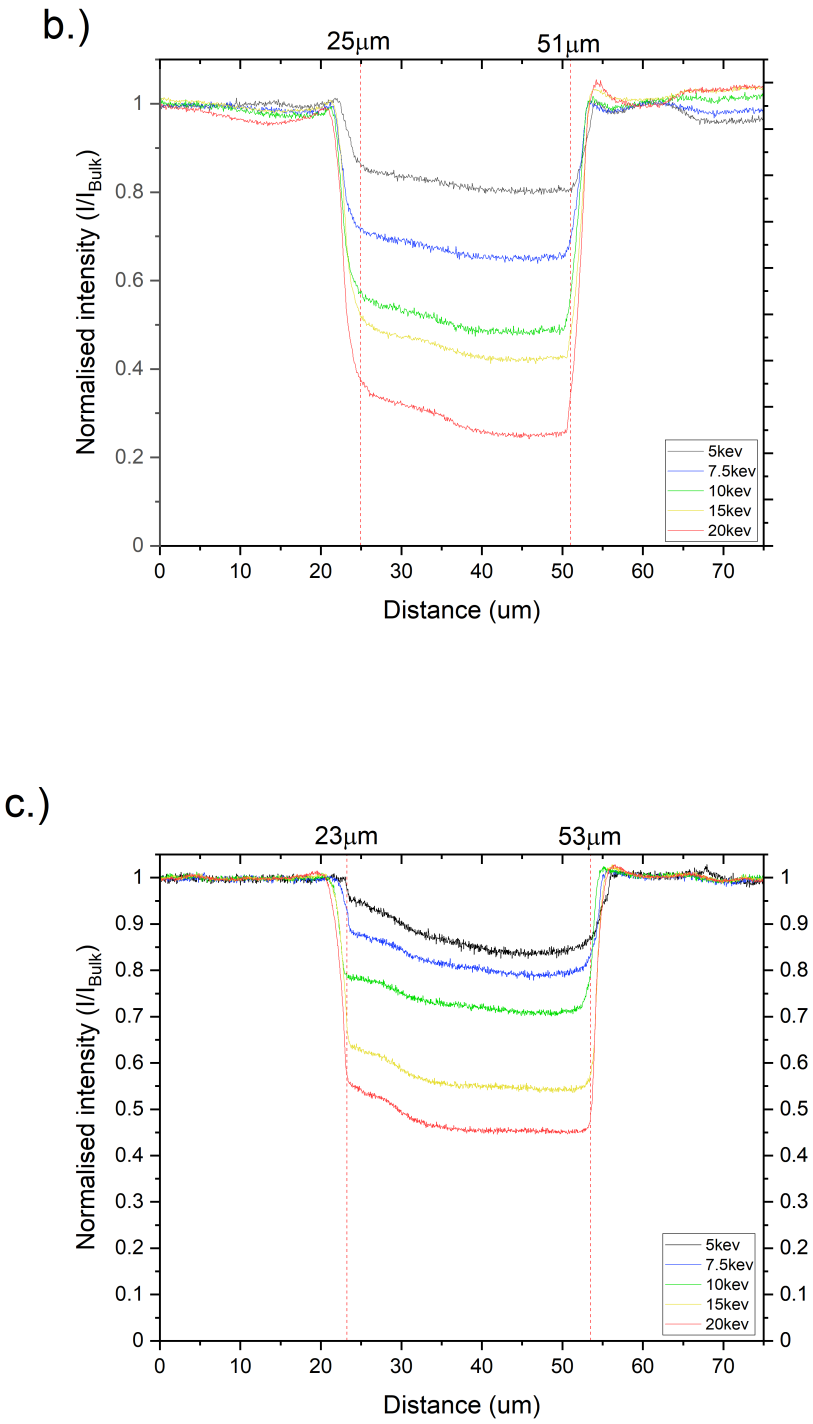
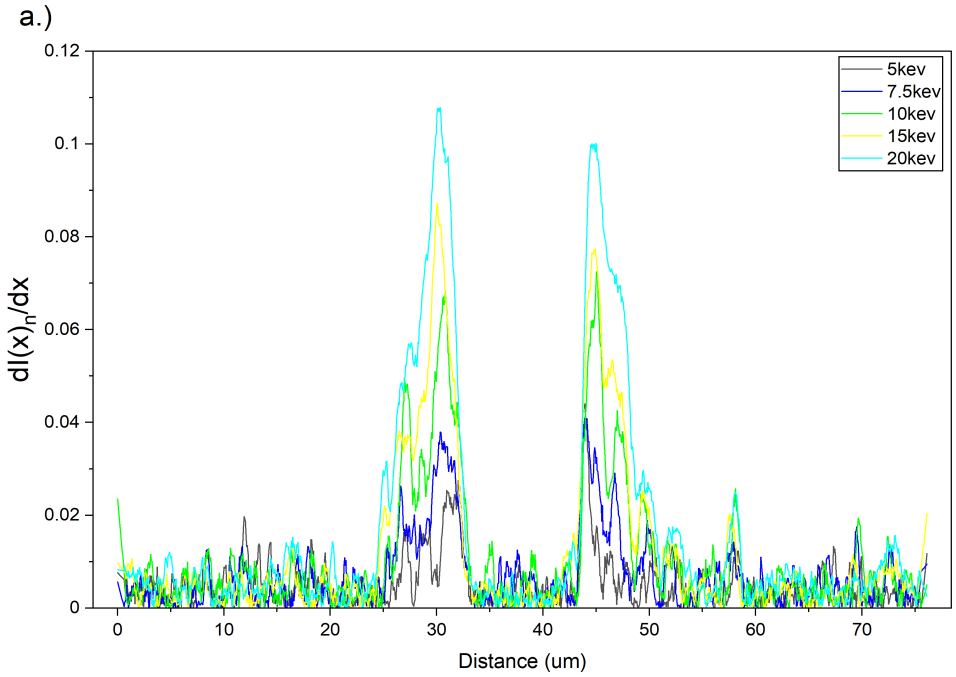


Figure 5.6: Normalised CL intensity graphs of a cross-section of: a.)saw diced b.) HBr plasma chemistry c.) Cl/Ar plasma chemistry. The red dashed lines denote the edges of the trench.

Figure 5.6 shows the normalised CL intensity for a 75 µm region of interest surrounding a trench etched using different methods. Figure 5.6a a saw diced sample, Figure 5.6b a SU-8 masked piece etched in a HBr plasma and Figure 5.6c a SiO_2 hard masked piece etched in the Cl/Ar plasma. The CL intensity is plotted as a function of lateral distance for different accelerating voltages. A reduction in normalised CL intensity corresponds to increased non-radiative recombination, which suggests the presence of defects. The section in the middle of the graphs with a substantial reduction in the normalised intensity corresponds to the etched trench. This reduction in normalised intensity is due to the absence of InP for the electron beam to radiatively recombine with and thus a lower detected CL signal. The remaining signal can be attributed to the trench floor. This region is of less concern than the sidewalls as this region would be removed in a subsequent backside grinding step in a DBG singulation approach. The regions shaded in red in Figure 5.6a show there is a 6 to 7 µm wide region on both sides of the trench before the CL intensity returns to 95% of the bulk InP CL signal. This area of reduced recombination efficiency is most likely caused by defects induced by the saw such as chipping. The gradient of the slopes represent the rate of change of normalised intensity with respect to distance or how quickly the signal recovers back to the bulk signal. A steeper slope means quicker recovery with the opposite being true for gradual slopes. The gradient of the slope does not improve with increasing accelerating voltage suggesting these defects are deep within the bulk and not just induced by the cleave of the cross section which would primarily create defects on the surface. For the HBr plasma chemistry on SU-8 shown in Figure5.6b the recovery to the bulk is quick as evident by the steep gradients at the sides of the trenches. The defect area appears to be much narrower than Figure 5.6a suggesting the defects are limited to the sidewall whereas the defects propagate out further in the saw diced sample. The SiO_2 hard masked piece shown in Figure 5.6c has a similar shape to the SU-8 masked piece suggesting both chemistries have a smaller region of defects and recover to the bulk signal quicker. Differentiating the graphs in Figure 5.6 with respect to lateral position gives the rate of change

of normalised intensity with respect to distance or how quickly the signal recovers back to the bulk signal. Using Savitzky-Golay smoothing to filter the noise in the raw CL signal, the derivative was calculated and plotted in Figure 5.7



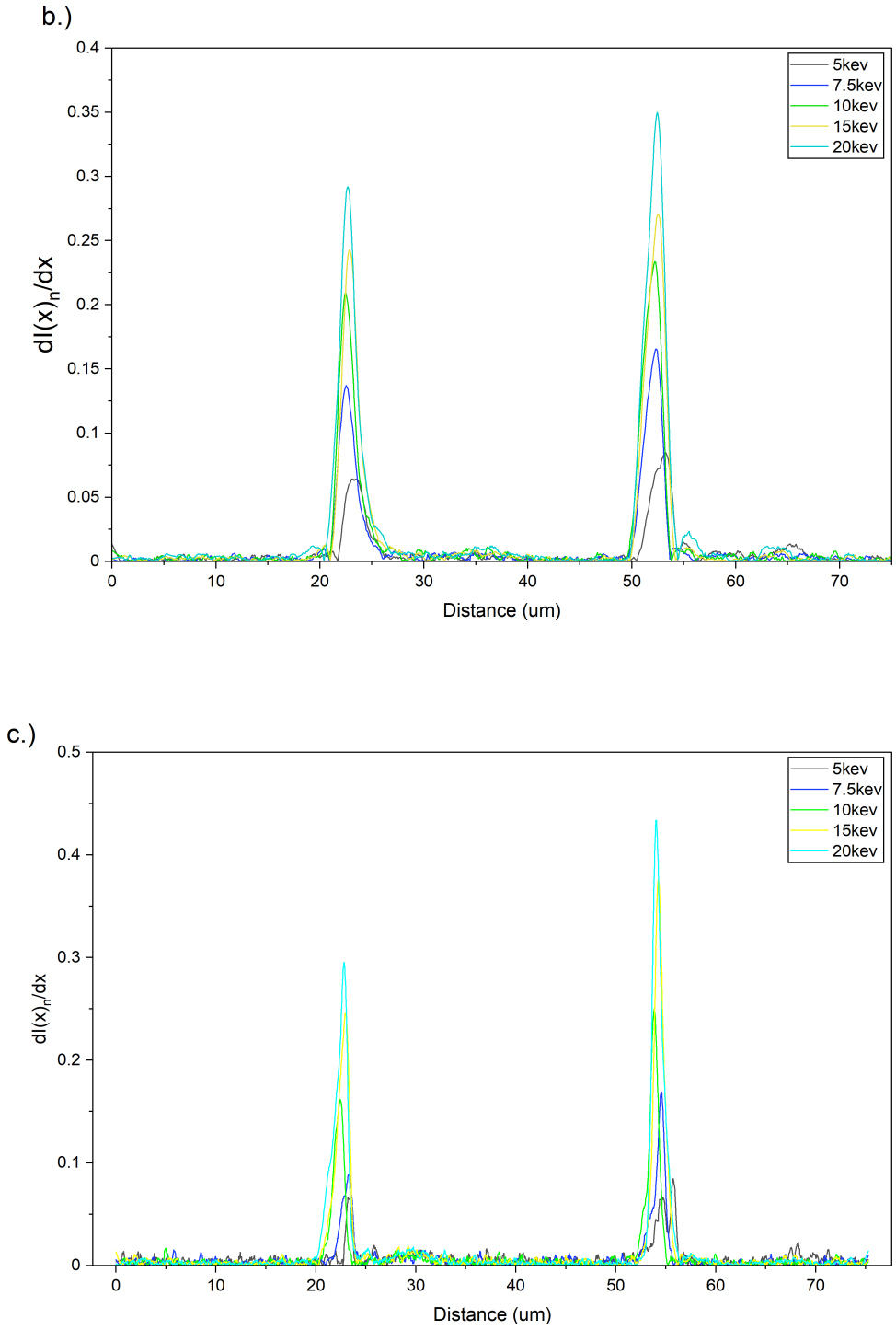
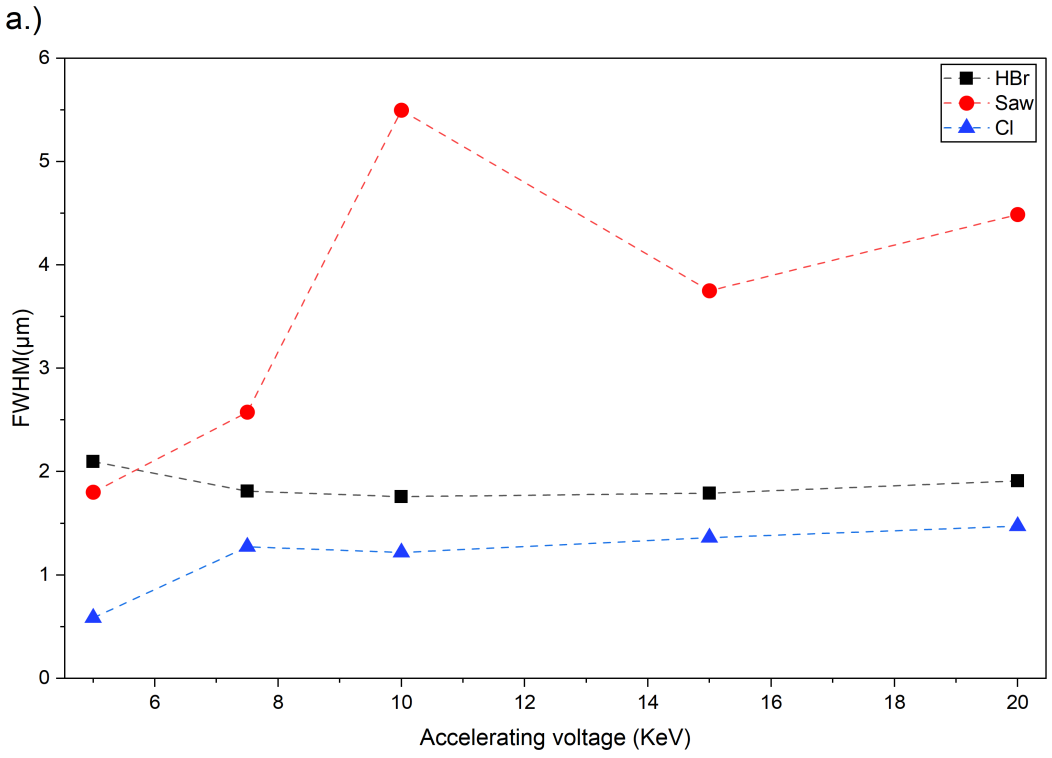


Figure 5.7: Differentiated normalised CL intensity graphs of a cross-section of: a.)saw diced b.) HBr plasma chemistry c.) Cl/Ar plasma chemistry

Quantitive analysis of the derivates peaks was done using OriginLab's single peak fitting tool to fit the slopes to a Gaussian curve. The left and right peaks were isolated then a Levenberg-Marquardt algorithm was used to refine the parameters of the Gaussian until convergence. From this the full width at half maximum (FWHM) was determined. In a gaussian context the FWHM is the distance between two points on the Gaussian where the function falls to half its peak height. In the context of the CL intensity this FWHM is the width of the transition zone from trench to bulk intensity. Calculating the FWHM for both the left and right derivative peaks gives the results shown in Figure 5.8



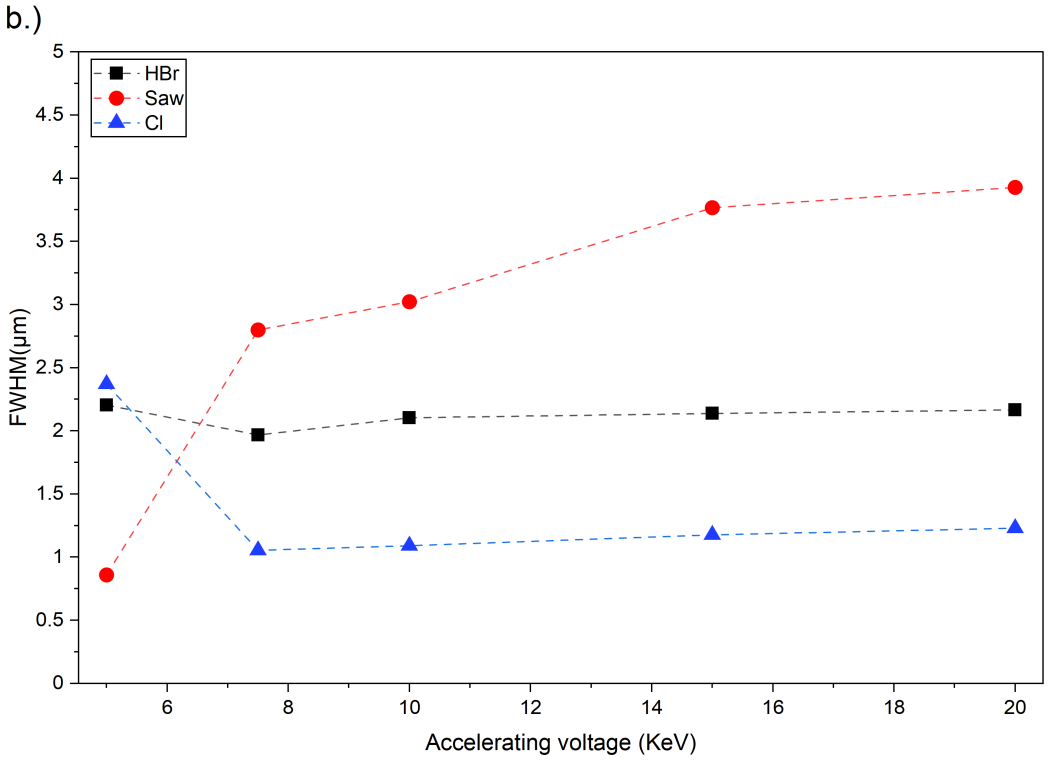


Figure 5.8: The FWHM of the derivative peaks in Figure 5.7 for increasing accelerating voltage for a.)left sidewall b.)right sidewall

The higher FWHM of the saw diced samples in both Figure 5.8 a and b show the damaged region is approximately double that of the plasma diced sample particularly at higher accelerating voltage. At 20 keV in Figure 5.8a the reduced recombination efficiency region region was 3.93 µm, 2.16 µm and 1.23 µm for saw, HBr and cl respectively. At 20 keV in Figure 5.8b this region was 4.49 µm, 1.91 µm and 1.47 µm for saw, HBr and cl respectively. From these 2 sidewalls the largest regions of reduced recombination efficiency indicative of defects was saw dicing then HBr and Cl. The Cl plasma piece having a smaller reduced recombination efficiency region is most likely due to this piece having half the processing time at 30 minuets compared to the HBr sample at 60 minuets. The FWHM of the saw diced sample increases with increasing accelerating voltage meaning the damage penetrates deeper into the bulk. The FWHM of both the plasma diced samples

however, remains flat suggesting the damage is confined to a small region of the sidewall.

Chapter 6

Conclusion

InP is a compound semiconductor material widely used in optoelectronic devices. This work proposed a novel way to dice InP using an ICP to plasma etch dicing lanes. The two main benefits of a plasma dicing process is the control over the dicing lane widths. With saw dicing the dicing lane width is determined by the width of the saw blade being used. With plasma dicing the limit to the kerf width is determined by the CD of the masking material. A reduced dicing lane width means more die can be fabricated on a wafer of the same size increasing yield. This improvement in yield from a reduced dicing lane width is further improved with increasing wafer sizes. This becomes increasingly more relevant as semiconductor manufacturing companies switch from existing 3 and 4 inch wafers to 6 inch. As a non-mechanical process plasma dicing induces less defects when compared to saw dicing. This also increases yield by decreasing the amount of die failures from defects. A SiO_2 hard mask and two photoresist masks (SU-8 and PI) were used and compared in two different plasma chemistries. The best results were achieved using a HBr plasma chemistry and a SU-8 photoresist masked piece of InP with a $137.75 \pm 9.95\,\mu m$ deep etch being achieved in 60 minuets at an average etch rate of $2.30 \pm 0.15\,\mu m/min$ and a selectivity of 20.9:1 between the SU8 and the InP. Repeating on a bigger surface area piece only slightly reduced the etch rate by $0.32\,\mu m/min$ meaning the recipe should be able to be scaled up to a whole wafer. While the etch rate remained similar across

chemistries the selectivity improved from 5.6:1 in a Cl plasma to 20.9:1 in the HBr plasma. This significant increase in selectivity is attributed to a strong polymer forming between the Br and the SU-8 as evident by the 2.5Wt% of Br as determined by EDX. The SiO_2 hard mask provided the highest selectivity across both plasma chemistries that being 14.1:1 and 400:1 for the Cl and HBr plasma chemistries respectively. The SiO_2 hard mask provided the deepest etch of InP in the Cl chemistry at $57.3 \pm 3.2\,\mu m$ with a selectivity and etch rate of 14.1:1 and $1.90 \pm 0.11\,\mu m/min$ respectively. In the HBr plasma however, there was significant undercutting meaning additional passivation was required as there was no polymer deposition as was the case with the SU-8. The PI reflowed at temperatures >180°C making process development particularly difficult as this narrowed the process window meaning small changes in ICP parameters produced drastically different results. Different removal techniques were used on the SU-8 photoresist mask to remove the crosslinked SU-8 post plasma etch, with the P1316 providing the lowest average roughness 5.68 nm with the original surface roughness average being 3.19 nm. The damage from the plasma etching was compared with a saw diced sample using CL. The saw diced sample exhibited the largest region of reduced recombination efficiency ranging from approximately 1 µm at 5 keV to >4 µm at 20 keV. The plasma diced samples had a much smaller range of approximately 2.5 µm and 2 µm at 5 keV to 2 µm and 1.5 µm at 20 keV for the HBr and Cl/Ar chemistry respectively. The small range of the plasma diced samples suggests the defects are limited to a small 2 µm region of the sidewall on both sides. Whereas the increase in the reduced recombination efficiency region with increasing accelerating voltage for the saw diced suggests the defects are not just confined to the surface and propagate further the deeper the electron beam penetrates. This shows that the defects induced by saw dicing is higher than plasma dicing.

Chapter 7

Future work

While this project has shown the viability of ICP plasma etching as a method of dicing for reduced defects, further improvements could be made. SU-8 proved to be a good choice of masking material due to it's relative ease of application and selectivity when using a HBr plasma chemistry. The subsequent removal however needs further investigation. Ideas to improve the removal include a sacrificial lift-off layer as well as further investigation of plasma removal. Due to limited resources the plasma etching of InP was primarily done on 15 mm by 15 mm test pieces. When increasing the open area there was a process shift reducing etch rate and selectivity. Further investigations using larger active areas as well as whole wafer test need to be done to further validate plasma dicing as a viable option for InP. An investigation comparing plasma dice before grind and plasma dice after grind or ideally plasma dice on tape should also be done to identify the best process flow to fully singulate die. These sigulated die could then be compared with saw diced samples for die strength and defects.

Appendix A

Experimental procedures

A.1 Standard substrate clean

Standard solvent clean:

- 10 minutes acetone at 50°C
- 10 minutes IPA at 50°C
- Rinse in DI water
- Spin dry at 3000rpm for 60 seconds

A.2 SU-8 datasheet

Photolithography:

- Dehydrate at 120°C for 2 minuets
- Ti prime 3000rpm 1000rpm/s 30 seconds
- Bake at 120°C for 2 minuets
- Spin SU-8:
  - Step 1: 500rpm 500rpm/s 10 seconds

  - Step 2: 3000rpm 1000rpm/s 30 seconds

- Bake at 120°C for 5 minuets
- Expose at 230mj/cm i-line 90%
- Post exposure bake at 120°C for 2 minuets
- Developer solution 60 seconds
- Acetone 30 seconds
- IPA 15 seconds

A.3 SU-8 InP recipe

Photolithography:

- Dehydrate at 120°C for 2 minuets
- Ti prime 3000rpm 1000rpm/s 30 seconds
- Bake at 120°C for 2 minuets
- Spin SU-8:
  - Step 1: 500rpm 500rpm/s 10 seconds
  - Step 2: 2600rpm 1000rpm/s 30 seconds
- Bake at 120°C for 8 minuets
- Expose at 340mj/cm i-line 90%
- Post exposure bake at 120°C for 3 minuets 30 seconds
- Developer solution 60 seconds
- Acetone 30 seconds
- IPA 15 seconds

A.4 SiO_2 hard mask standard recipe

Photolithography:

- Dehydrate at 120°C for 2 minuets
- Ti prime 3000rpm 1000rpm/s 30 seconds
- Bake at 120°C for 2 minuets
- Spin 125NXT 10b:
  - Step 1: 500rpm 500rpm/s 10 seconds
  - Step 2: 3000rpm 1000rpm/s 30 seconds
- Bake at 120°C for 5 minuets
- Expose at 1800mj/cm broadband
- Developer solution 60 seconds
- Fresh developer solution 60 seconds
- DI rinse

Dry etching:

- Plasma chemistry: C4F8:CF4:Ar at 8:20:42 sccm
- Coil power: 800w
- Platen power: 125w
- Etch rate: 253±6nm
- Time: 20 minutes

Photoresist removal:

- 30 minutes AZ 100 at 80°C
- Di water rinse

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